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Compute Project

AI Native Edge-MHS Base Specification

Part of the

AI-Native Edge-Modular Hardware Systems (AI Native Edge-MHS) Rev 1.0.0 Family

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1.2 Acknowledgements

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback of various individuals and companies that participated in AI Native Edge-MHS.

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3 Compliance with OCP Tenets

3.1 Openness

The AI Native Edge-MHS specification is developed collaboratively with industry contributors and is publicly available for third-party adoption and enhancement. The open workstream model actively removes barriers to participation, enabling global community members to build, modify, and extend HPM designs while maintaining ecosystem interoperability. All mechanical, electrical, and interface specifications are fully documented to ensure third parties can develop compliant solutions without proprietary constraints.

3.2 Efficiency

The AI Native Edge-MHS specification delivers significant efficiency gains by enabling HPM design reuse across multiple compute core generations and reducing both design and validation investment costs. The variable HPM outline methodology with fixed and floating features allows HPM designers to optimize their designs while maintaining compatibility with common chassis infrastructure, eliminating costly chassis proliferation. The modular architecture supports scalable power delivery and I/O configurations that minimize operational expenses and improve resource utilization across diverse deployment scenarios.

3.3 Impact

This specification has transformative impact by establishing open, standardized form factors that accelerate time-to-market for AI-Native edge solutions and enable deployment across global supply chains with minimal modifications. By making advanced edge computing capabilities accessible to many customers worldwide through widely-adopted specifications, the specification creates meaningful positive impact and establishes trust through open, interoperable design principles. The specification supports multiple HPM classes and deployment models (monolithic, multi-node, pole-mount, and outdoor) that address diverse industry needs and enable rapid innovation.

3.4 Scale

The specification is engineered for easy implementation and deployment at any scale, from single-node monolithic systems to dense multi-node configurations, with comprehensive documentation including installation guides, CAD files, and detailed implementation examples. The defined Common Chassis Intervals (260mm, 280mm, 305mm, 350mm, 365mm) and two HPM classes (Class N and Class L) enable incremental scaling while maintaining interoperability across different chassis depths and form factors. All necessary tools including CAD files, connector specifications, and power zone guidance are publicly available, and management functions leverage the open DC-SCM R2.2 specification for standardized support.

3.5 Sustainability

The specification promotes sustainability through efficient use of materials by enabling design reuse and minimizing the need for multiple chassis variants, reducing electronic waste and material consumption across the supply chain. The modular HPM architecture supports flexible power configurations and enables optimization of power delivery to match actual deployment requirements, supporting energy-efficient edge deployments. The standardized, interoperable approach encourages circular economy principles by allowing HPMs of different generations and classes to be deployed in common chassis infrastructure, extending product lifecycles and minimizing environmental impact.

4 Version Table

Date	Version #	Description
11/18/2024	0.3	• Initial Draft Version
07/16/2025	0.5	• Initial Draft Release
09/18/2025	0.7	• Updated the contributors list • Corrected date of Initial Public Release from 07/16/2024 to 07/16/2025 • Updated Figure 4 – Example Fixed and Floating Features • Updated Figure 9 – Class N Overview • Updated Figure 10 – Class L Overview • Updated Figure 11 – Common 19” Chassis Supporting Multiple HPMs • Updated Figure 12 – First CPU (CPU 0) Support on HPM • Updated Figure 13 – Class N Board Outline • Updated Figure 14 – Class L Board Outline • Updated Figure 15 – HPM Negative Features • Updated Figure 17 (Mounting hole placement changes) • Updated Figure 18 (Mounting hole placement changes) • Updated Figure 21 Chassis Hook locations (Added Datum and Mounting Holes) • Updated Figure 22 Chassis Hook locations (Added Datum and Mounting Holes) • Updated Figure 23 Chassis Hook locations (Added Datum and Mounting Holes) • Updated Figure 24 Chassis Hook locations (Added Datum and Mounting Holes) • Updated Figure 34 PIC connector recommended placements (Datum and Mounting Hole moves) • Updated Figure 35 (Datum and mounting hole moves, enlarging of MPIC Placement Zones) • Updated Figure 36 (Datum and mounting hole moves, enlarging of MPIC Placement Zones) • Updated Figure 37 Class N Riser Locations (Added Datum and Mounting Holes) • Updated Figure 38 Class L Riser Locations (Added Datum and Mounting Holes) • Updated Figure 39 – Class N Height Restriction Zones • Updated Figure 40 – Class L Height Restriction Zones • Updated Figure 41 – AI Native Edge-MHS Power Zone • Updated Figure 43 – Class N PIC Power Connector Recommended Locations • Updated Figure 44 Class N PIC Power Connector

		Recommended Locations • Updated Figure 45 – Recommended PIC Power Connector Ordering • Added DC-SCM CFF Implementor's Note to avoid mounting hole conflicts to section 12.7.1 OCP NIC and DC-SCM
12/08/2025	0.9	• Updated Section 6 – the compliance table • Modified Section 8 – to include MHS and DC-MHS applicable specifications and added M-PNP and DC-SCM • Added link to CAD files in section 15.4 • Modified Section 15.5 to include 162mm HPM support and Blind Mate HPM support as possible future topics for the workstream to solve as well as changed the heading title to be Potential Future Material • Updated the document header to change from Revision 0.7 to Revision 0.9 • Updated Table of contents so headings matched document with the title change to section 15.5
July 2026	1.0.0	• First Official Public Specification Release for AI Native Edge-MHS – Note: All previous versions are from previous workstream Edge-MHS • Updated document header from Revision 0.9 to Revision 1.0 • Updated CLA revision from Revision 1.0 to Revision 0.9 • Change to AI Native Edge-MHS • Updated Authors • Removed Ampere • Added section 2 Compliance with OCP Tenets • Corrected typo's • Changed Section of Table of Contents to no section. Section 1 starts with License. Had to update links. • Addressed OCP Feedback • Added Copyright/Trademarks • Updated References
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		•
		•

5 Scope

This document defines technical specifications for the Edge optimized form factors used in AI-Native Edge-Modular Hardware Solutions (AI Native Edge-MHS).

Any supplier seeking OCP Marketplace Recognition for a hardware product based on this specification shall be 100% compliant with all features or requirements listed in **Section 6** of this specification.

5.1 Items Not in Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc.)
- Risers
- Chassis

5.2 Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

- Rack Compatibility (Discussed in **Section 10**)
- Physical Spec
- Thermal Design
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management (Leverages OCP DC-SCM R2.x)
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

6 AI Native Edge-MHS Base Specification Compliance Table

The following table is meant to point the reader to sections containing Base Spec compliance required items. The table should not be used as a checklist as each row could contain multiple requirements. Base Spec compliance items are underlined. "Shall" means it is a requirement for compliance.

Table 1: AI Native Edge-MHS Base Specification Compliance

Item	Base Spec Requirement	Reference
1	Any supplier seeking OCP Marketplace Recognition for a hardware product based on this specification shall be 100% compliant with all features or requirements listed in **Section 6** of this specification	Section 5 Scope
2	Unless otherwise specified, PCB dimensions shown in this specification shall comply to **Table 4**	Table 4
3	The required board outlines are defined in **Figure 15: AI Native Edge-MHS Class N HPM Board Outline (PRIMARY SIDE)**. AI Native Edge-MHS HPMs shall comply with these board outlines.	Section 12.1 HPM Outlines
4	All negative PCB features implemented shall comply to the following restrictions: 1. Negative PCB features shall not violate or conflict with any required features such as mounting holes and connector placement. 2. The negative PCB feature shall not extend the full length of the left or right edge of an HPM (i.e., this feature shall not be used to essentially create a non-standard HPM width).	Section 12.1.3 Allowances for Negative PCB Features
5	All holes shall adhere to the specified size, ground pad dimensions, component KOZ and route KOZ.	Section 12.2 Board Datum and Mounting Hole Information
6	All additional holes shall adhere to Standard Mounting Hole requirements (Detail A in **Figure 18).**	Section 12.2 Board Datum and Mounting Hole Information
7	There are required holes associated with each Near IO fixed riser location (Detail D in **Figure 18)** that shall be implemented when a fixed riser connector is implemented	Section 12.2 Board Datum and Mounting Hole Information
8	Required and recommended board mounting hole locations shall be adhered to and are specified for AI Native Edge-MHS HPM Class N and L in **Figure 19 and Figure 20**	Section 12.2 Board Datum and Mounting Hole Information
9	There are 5 required mounting/riser holes on the Class N HPM near side that shall be implemented when risers are implemented and two required mounting holes on the Class N near side when risers are not implemented (the Datum Hole and Alignment Hole).	Section 12.2.1 Class N HPM Riser/Mounting Hole
10	There are 6 required mounting/riser holes on the Class L HPM near side that shall be implemented when risers are implemented and two required mounting holes on the Class L near side when risers are not implemented (the Datum Hole and Alignment Hole).	Section 12.2.2 Class L HPM Riser/Mounting Hole
11	All AI Native Edge-MHS HPMs shall implement the Zone 1 universal secondary side component height restriction of 1.6mm for all board Classes.	Section 12.3.1.1 Zone 1: Exceptions for Secondary Side Tall Components
12	1. Exceptions are contained to small areas of the secondary side and shall not exceed 400mm^2 area per instance. 2. No two instances of a secondary side exception shall be closer than 10mm, as to not drive excessive cutouts in Chassis-to-HPM bracketry.	Section 12.3.1.1 Zone 1: Exceptions for Secondary Side Tall Components
13	The maximum length of a connector's Alignment Post or Retention Barb shall be 3.20mm MAX such that it will not interfere with chassis hook features.	Section 12.3.2 Zone 2: Chassis to HPM Board Bracket (Board Pan) KOZ Requirements
14	Each AI Native Edge-MHS HPM Class shall support required zero height KOZ locations for chassis hook features that interface between the chassis base and the chassis to board bracket (board pan) as depicted in **Figure 23**: **through Figure 26**.	Section 12.3.2 Zone 2: Chassis to HPM Board Bracket (Board Pan) KOZ Requirements
15	The floating far side edge KOZs shall be required for all HPM depths	Section 12.3.2 Zone 2: Chassis to HPM Board Bracket (Board Pan) KOZ Requirements

16	If the far side edge of the HPM intersects this KOZ area, then a partial KOZ shall be implemented. The resulting KOZ should be colinear with the PCB edge.	Section 12.3.2 Zone 2: Chassis to HPM Board Bracket (Board Pan) KOZ Requirements
17	The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by: • Backing Plate allowed Height = 6.2mm – HPM thickness - 0.08mm standoff height tolerance – allowances for other backplate design req's (insulators, deflections, etc)	Section 12.3.4 Zone 4: CPU Backing Plate Requirements
18	The maximum allowed HPM thickness shall be 3.18mm nominal and assumes +/-10% tolerance is allowed	Section 12.4 HPM Board and Assembly Thickness
19	There shall be a hole required for HPM retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc., hole size required Primary / Secondary side KOZs (and height restrictions around this hole), are defined in **Figure 32.**	Section 12.5 HPM to Chassis Retention
20	The HPM shall require a hole interface to a mechanical handle	Section 12.6 HPM Handle Hole
21	The hole location shall be near the Far side edge of the HPM.	Section 12.6 HPM Handle Hole
22	The HPM shall implement a battery backed voltage interface per DC-SCM R2.2 "Battery Voltage" requirement	Section 12.7.1 OCP NIC and DC-SCM
23	The electrical implementation for each connector shall follow the M-PIC specification	Section 12.8.1 Connector Requirements
24	**Intrusion Switch** • **M-PIC Section Reference:** "Intrusion Switch" • **Connector Requirement:** Shall be Required (may be de-populated)	Section 12.8.1 Connector Requirements
25	**Control Panel** • **M-PIC Section Reference:** "Control Panel Interfacing" • **Connector Requirement:** Shall Be Required (may de-pop)	Section 12.8.1 Connector Requirements
26	**PDB Management Connector** • **M-PIC Section Reference:** "PDB Management Connector" • **Connector Requirement:** Shall Be Required (may be de-populated)	Section 12.8.1 Connector Requirements
27	Placement of these connectors shall always be within the specified zone.	Section 12.8.2 Class N and Class L M-PIC Connector Locations (Non-Power)
28	All HSIO connectors shall be compliant with the M-XIO specification and be listed in **Table 6**.	Section 12.9.1 DC-MHS Compliant HSIO Connectors
29	HPMs which implement near side fixed risers shall: • Use a Fixed Riser connector defined in **Section 12.9.1** • Place them in the location(s) defined in **Section 12.9.2.1**	Section 12.9.2 Near Side Fixed Riser Connectors
30	SFF-TA-1033 fixed riser connectors which are implemented shall follow **Figure 39 and Figure 40,** define the required location of the SFF-TA-1033 connectors	Section 12.9.2 Near Side Fixed Riser Connectors
31	All SFF-TA-1033 Near Side Fixed riser connectors shall use a 21A power block version	Section 12.9.2 Near Side Fixed Riser Connectors
32	All implemented HSIO connectors shall be defined in M-XIO and listed in **Table 6.**	Section 12.9.3 Other HSIO Connectors
33	All AI Native Edge-MHS Classes shall adhere to a common approach of three different component height restriction zones as shown in **Figure 39 and Figure 40.**	Section 12.10 Primary Side Component Height Restrictions and KOZs
34	Adherence to the 11.3mm Zone shall be required when PCI CEM cards are implemented directly above the HPM and its peripherals (adherence to this requirement is not mandatory if PCIe CEM cards directly above the HPM are not being implemented).	Section 12.10 Primary Side Component Height Restrictions and KOZs
35	Adherence to the 6mm Zone shall be required when PCIe risers are implemented	Section 12.10 Primary Side Component Height Restrictions and KOZs
36	Zone height restrictions apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of soldered components	Section 12.10 Primary Side Component Height Restrictions and KOZs
37	To maximize reuse of power delivery across all AI Native Edge-MHS HPMs, the required connectors for all cabled Ingress / Egress power shall be the 2x6+12SB or 2x3+6SB PICPWR	Section 13.2.1 Ingress / Egress Cabled Power Connector
39	HPMs shall deliver a minimum of 87W of power to the riser connector	Section 13.3 Fixed I/O Riser Power
40	Riser connector shall comply with M-PIC PICPWR sideband signaling requirements	Section 13.3 Fixed I/O Riser Power

41	AI Native Edge-MHS HPMs shall provide power to the DC-SCM R3.2 connector as defined in the OCP DC-SCM R3.2 spec (Refer to **Section 15**).	Section 13.4 DC-SCM R2.x Power
42	When implemented, AI Native Edge-MHS HPMs shall provide power to OCP NIC 3.0 connector(s) as defined in the OCP NIC 3.0 specification (Refer to **Section 15**).	Section 13.5 OCP NIC 3.0 Power
43	The HPM shall be required to implement electrical interfaces that are in compliance with the AI Native Edge-MHS family of specifications. Refer to **Section 8** for additional details, specifically M-PIC, M-XIO, M-CRPS, and M-PESTI specifications.	Section 14.0 I/O System (Electrical Interfaces)

7 Overview

The objective of this specification is to outline the requirements of a family of Edge optimized Host Processor Module (HPM) form factors. This Edge specification embodies design considerations for CPU, DIMMs, and other processor related features commonly used by the industry today but is not limited to only those functions. For instance, a GPU, FPGA, DPU, etc. being placed within the Compute Area of the HPM is allowable per this specification. The HPM is designed with standard 19" rack enclosures in mind, also known as compliant with EIA -310-E. However, the HPMs may be utilized in other environments such as Pole Mount, larger 21" racks, and other environments.

Implementors Note:

As a Base Specification, AI Native Edge-MHS contains and allows for optionality in many areas. In addition to this base specification, it is recommended that HPM designers create and maintain an HPM Design Specification that further details the needs and requirements of their own unique design.

Examples of information that may be included in a Design Specification are:

- Quantity and location of fixed/hybrid risers
- Quantity and location of other HSIO connectors
- Power zone requirements
- I/O Region use case
- Etc.

The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs implemented to the specification to enable reuse of chassis and system level components over multiple generations, ability to utilize a single HPM in multiple design environments, and scalability of HPMs across short depth (450mm or less) monolithic and multi-node environments. Implementing this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of Edge optimized service provider products but may be applicable to Enterprise and Cloud environments. Examples of these attributes are mechanical form factors, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections.

8 Applicable MHS and DC-MHS Family of Specifications

The **O**pen **C**ompute **P**roject (OCP) **M**odular **H**ardware **S**ystem (MHS) and **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specifications that are applicable:

- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (i.e., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PNP** (**M**odular Hardware System **P**lug-**N**-**P**lay) – (Modular Hardware System Peripheral Sideband Tunneling Interface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (i.e., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination
- **M-DNO** (**M**odular Density Optimized) – (Modular Hardware System Density Optimized) – Specifies a This document defines technical specifications for the Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.
- **M-SDNO** (**M**odular Scalable Density Optimized) – (Modular Hardware System Scalable Density Optimized) – Specifies a This document defines technical specifications for the Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.
- **DC-SCM** (**D**ata **C**enter – **S**ecure **C**ontrol **M**odule) – The DC-SCM specification is designed to decouple server management and security functions from traditional server motherboards. This allows for the development of server management solutions that are independent of server architecture, facilitating greater flexibility and efficiency in data center operations.

- To access additional DC-MHS specifications please visit the OCP Contribution Database. https://www.opencompute.org/contributions

- To access additional DC-SCM specifications please visit the OCP Contribution Database. https://www.opencompute.org/contributions

9 Terminology

Table 2: Terminology

Standardized Term	Meaning	Alternative Terms
19” ½ Width HPM	210mm wide HPM, enables systems with 2 HPMs side by side in 19” Rack	
19” Full Width HPM	426mm wide HPM, uses full width of 19” Rack	
21” ½ Width HPM	250mm wide HPM, enabled systems with 2 HPMs side by side in 21” Rack, also used in 19” systems	
21” Full Width HPM	512mm wide HPM, intended only for 21” Rack	
Adapted HPM	An HPM that utilizes a Compliant HPM as a construct, with a specific set of repeatable modifications which form the adaptation.	
Chassis-Board Bracket	Bracket that attaches to an HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan Sub Pan
Common Chassis Interval	Refers to the maximum HPM Length supported within common chassis infrastructure. Exceeding these intervals will impact the addressable market for HPM designs.	CCI
Common Redundant Power Supply Specification	Refer to Section 8	M-CRPS, CRPS PSU
Compliant HPM	An HPM which meets every item listed in this base specification compliance table.	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
CPU	Central Processing Unit	Processor
CSP	Cloud Service Provider	

CXL	Compute Express Link	
Datum	A plane, axis or point location from which dimensions and tolerances are referenced.	
DC-SCM	Datacenter Secure Control Module as defined by OCP DC-SCM R2.x spec	SCM
DC-SCM CFF	Datacenter Secure Control Module Compact Form Factor as defined by OCP DC-SCM R2.2 spec	CFF
DPU	Data Processing Unit	Smart NIC
Edge	The network between data centers and end users/devices	
AI Native Edge-MHS	Workstream Name	E-MHS
Extensible I/O Specification	Refer to Section 8	M-XIO
Far	Board location or zone, opposite of location of datum	Far Side
Fixed Feature	HPM features with a consistent location relative to the datum	
Floating Feature	Features that shift relative to the HPM board edge as the length changes	
FPGA	Field Programmable Gate Array	
Full Width Specification	Refer to Section 8	M-FLW
GPU	Graphics Processing Unit	
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
HPM Class	Defines HPM width and feature set	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements this base specification.	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
KOZ	Keep Out Zone, a design term for PCB designs that defines the area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	

May	Indicates it's allowable for Base Spec compliance	
Near	Board location or zone, related to section of board closer to the datum	Near Side
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
PCB	Printed Circuit Board	PCBA
PCIe	Peripheral Component Interconnect Express	
Platform	Complete system including HPM, power, peripherals, etc	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	
Platform Infrastructure Connectivity Specification	Refer to Section 8	M-PIC
Shall	Indicates a requirement for Base Spec compliance	
Should	Indicates a recommendation for Base Spec compliance	
System Designer	The person or organization designing a system which incorporates HPMs (whether compliant or adapted) into the system design.	

10 Background and Assumptions

AI Native Edge-MHS HPM specification primarily targets single-socket platforms for monolithic and dense (multiple-nodes in common chassis) edge applications due to use case size constraints. In these applications the size of the targeted chassis can be extremely varied, as can the location of the HPM within the chassis. Systems are typically, but not limited to, 1RU or 2RU designs. 21" rack-based systems may also be supported. Front access for I/O and servicing models is the primary consideration.

When considering representative system depth targets, the most common environments were distilled into the following categories:

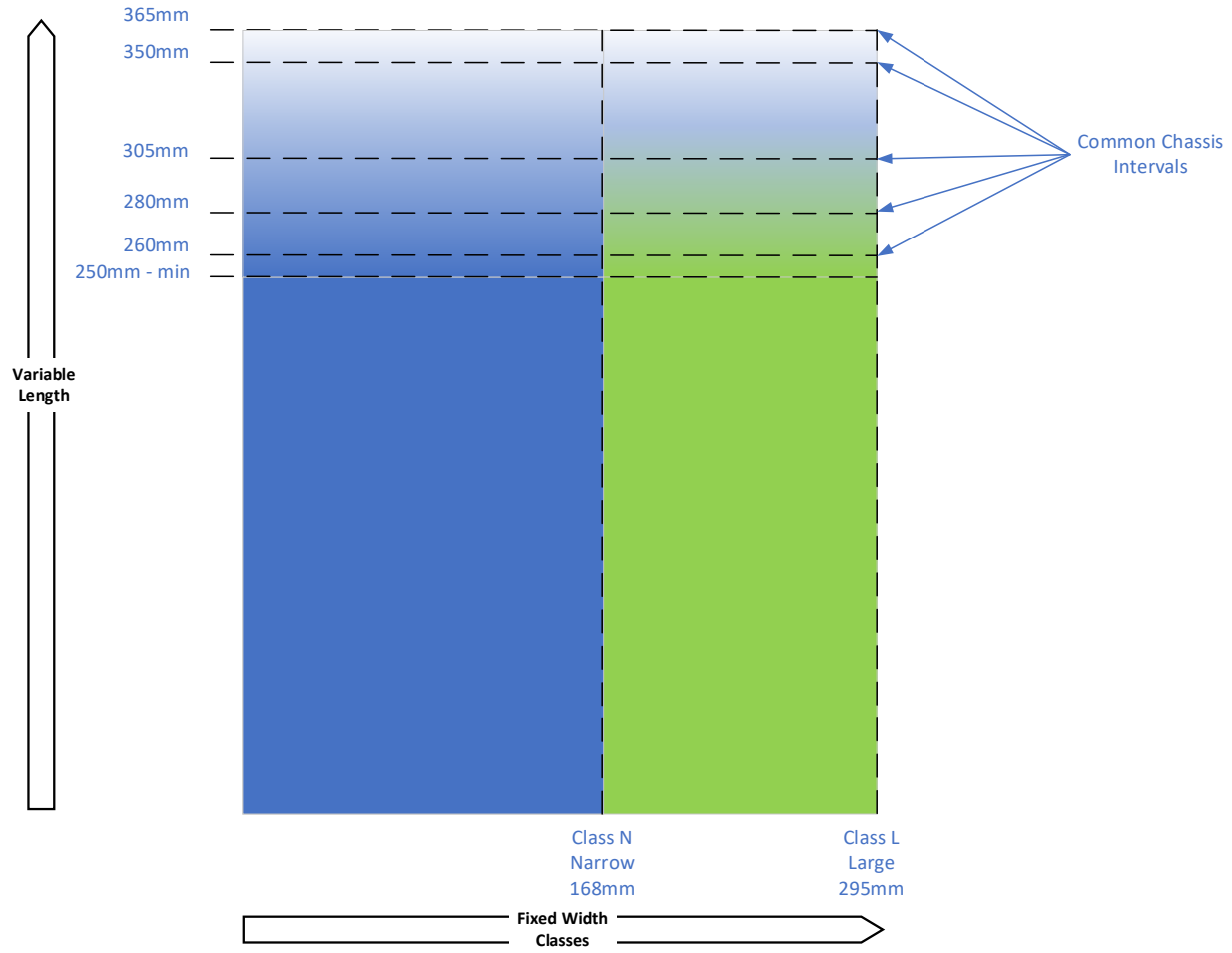
1. **Standard Depth Rack / Solution**
   - ~430 to 500mm deep with single or multiple HPMs
2. **Mid Depth Rack / Solution**
   - ~350mm to 430mm deep with single or multiple HPMs
3. **Short Depth Rack / Solution**
   - ~300mm to ~320mm deep with single or multiple HPMs
4. **OTII-E Compatible Rack / Solution**
   - >470mm deep with single or multiple HPMs

5. **IP65/IP67 Outdoor Solutions** IEC 60529

This specification shall focus on products targeted to these primary environments. **Section 16.1** illustrates design scenarios for each of these solutions providing the reader with a clearer understanding of each category. This specification does not in any way prohibit alternate environments.

10.1 AI Native Edge-MHS HPM Classes and Common Chassis Intervals (CCIs)

Figure 3: AI Native Edge-MHS HPM Framework



AI Native Edge-MHS is intended to enable a variety of interoperable HPMs targeted primarily for 19" rack ecosystems. For purposes of this specification, 19" refers to EIA-310 19" racks. AI Native Edge-MHS targets both monolithic and multi-node systems optimized to Edge Applications (short depth and pole mount) but may also be applicable to Enterprise and Cloud applications. To cover this solution space, AI Native Edge-MHS defines 2 "HPM Classes" as shown in **Figure 3**.

An HPM Class defines a fixed HPM width and corresponding feature set, for example, all Class N HPMs are 168mm wide, while Class L are 295mm wide.

For each HPM class, length is variable up to a specification defined maximum. HPMs are defined such that the only major difference between different length HPMs of the same class is the space available for the compute core.

AI Native Edge-MHS HPM Classes Include:

- Class N – Narrow Width – 168mm
  - Primarily targets 19” rack and pole mounted solutions but can also be used in other environments.
  - Can be used in a traditional monolithic chassis, utilizing a single HPM with lots of I/O or placed with two HPMs in a horizontal side-by-side scheme or in a vertical orientation.
  - Dense multi-node edge architectures are a possible use case.

- Class L – 19” Large Width – 295mm
  - Exclusively targets 19” racks.
  - Typically horizontally oriented and consume the full 19” rack width.

AI Native Edge-MHS also specifies “Common Chassis Intervals” (CCIs). These are important design points that are common in the industry which HPM designers should take careful consideration of when selecting the length of an HPM. The value specified by CCI ‘n’ means that common industry chassis infrastructures support HPMs up to a maximum length of n. For example, with a CCI at 260mm HPM designers should be aware that an HPM length of 261mm reduces the addressable market of that HPM.

AI Native Edge-MHS Common Chassis Intervals, as depicted in **Figure 3**, include:

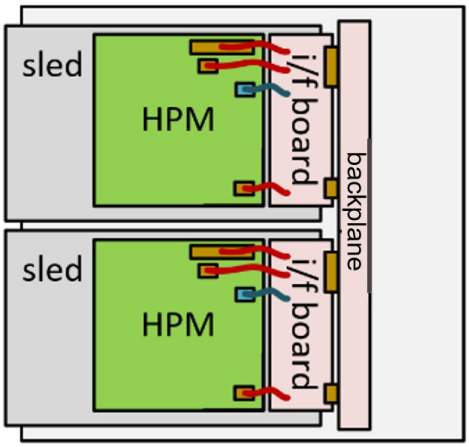
- 260mm
  - Short / dense chassis support – 310mm chassis length is the target
- 280mm
  - Mid length chassis support – 350mm chassis length is the target
- 305mm
  - Compatible with M-DNO Type 4 Lengths (305.59mm)
- 350mm
  - Large length chassis support – 420mm to 450mm length is the target
- 365mm
  - Backplane length chassis support – 470mm to 500mm length is the target

This specification will focus on products targeted to these primary chassis environments. **Section 16.1 AI Native Edge-MHS Conceptual Implementation Examples** illustrates design

scenarios for each of these solutions providing the reader a clearer understanding of each category. This specification does not prohibit alternate environments.

This version of the AI Native Edge-MHS specification does not address native “direct plug” or “blind mate” options for HPMs, these scenarios may be added in a future release. At this time, it is assumed that compliant HPMs will leverage an interface board to enable these use cases as demonstrated in **Figure 4**. However, placing these “direct plug” or “blind mate” option does not necessarily preclude specification compliance.

Figure 4: AI Native Edge-MHS HPM with Multi-node Interface Board



10.2 AI Native Edge-MHS HPM Intent and Methodology

The goal of AI Native Edge-MHS is to enable a variable HPM outline which:

1. Allows HPM designers more flexibility in optimizing their designs (e.g. to reduce panelization cost)

2. Provide highly interoperable solutions so system designers do not experience chassis proliferation

The “scaled” or variable HPM outline is enabled by dimensioning features of the HPM in two different ways:

- Fixed features are features which are dimensioned to the datum, these features simply “fall off” the HPM if they are outside the board outline.

- Floating features are features which are dimensioned to a board edge, these features are always present in a consistent location relative to the HPM boundary and never “fall off” the HPM.

More detailed information is provided in **Section 10.7** through **10.9.**

10.3 AI Native Edge-MHS HPM Designators

AI Native Edge-MHS HPMs will be referred to as ‘N###’, where:

N = HPM Class (N or L)

= The length of the HPM in mm, rounded down to the nearest mm

Following this methodology, as shown in **Table 3**, a 305.59mm Class 'N' HPM would be referred to as E-HPM 'N305'.

Table 3: HPM Designators at CCIs

	260 CCI	280 CCI	305 CCI	350 CCI	365 CCI
Class N HPM	N260	N280	N305	N350	N365
Class L HPM	L260	L280	L305	L350	L365

10.4 AI Native Edge-MHS Interoperability Goals

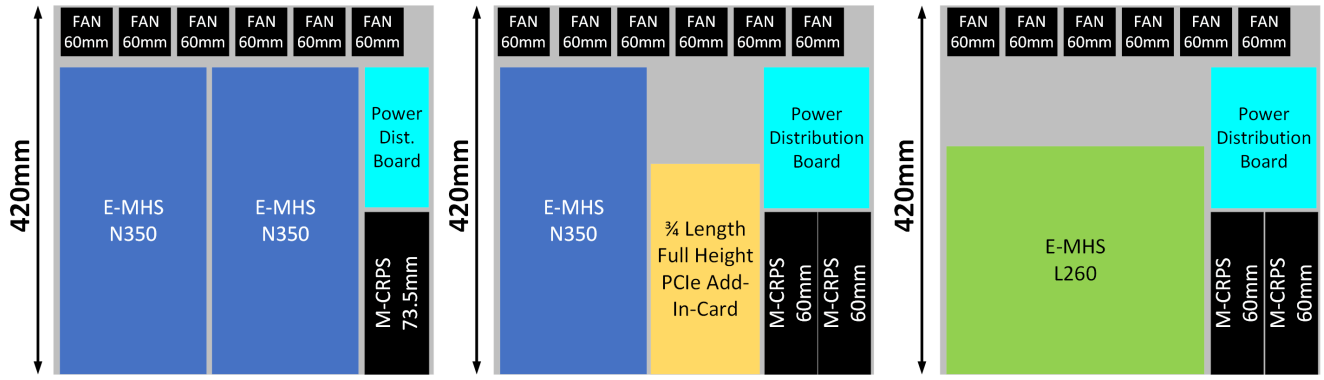
The goal of this specification is to provide HPM Interoperability of *most* smaller AI Native Edge-MHS HPMs in systems designed for larger AI Native Edge-MHS HPMs with minimal modifications (e.g. HPM tray or cable changes). In summary, the HPM Class interoperability goals are as follows:

1. All AI Native Edge-MHS HPMs of the same class are interoperable
2. Class N HPMs are interoperable with Class L

This high degree of interoperability is intended to minimize chassis proliferation amongst AI Native Edge-MHS system providers, this concept is demonstrated in **Figure 5:**

- All designs depicted below support 19" Class L AI Native Edge-MHS HPMs, as such the design may support a single Class N, two class N's, or a single Class L of varying lengths.
- The chassis is a 420mm chassis which can accept CCI's of 260mm, 280mm, and 350mm. This chassis would not be able to support a CCI of 365mm.

Figure 5: 19" AI Native Edge-MHS Chassis Examples



10.5 Common Industry Platform Features Considered

Mechanical

- Chassis installation within EIA-310-E (19”) and OpenRack V3 (21”) racks
- High-speed I/O Riser Connector fixed placement
- High-speed I/O Cable route considerations
- Additional fixed connector placements
- Board pan (HPM tray) enablement
- 1RU chassis constraints

I/O

- PCIe (Version 3.0, 4.0, 5.0, 6.0 and future) Card configurations typically offered by Enterprise TEMs/OEMs/CSPs/CoSPs
- Optional use of Open Compute peripherals connectors on the HPM
    - OCP NIC 3.0
    - DC-SCM R2.2
- Ethernet, USB, and other I/O connectivity natively on the HPM exposed directly to the front or rear of the chassis
- DC-SCM R2.2 CFF utilization

Power

- HPM supplied power to each fixed riser locations
- HPM Power Ingress and Egress connector placement for a variety of power layouts (PSUs with Cabled PDB, blind mate to bus bar, multi-node backplane, etc.)
- Considerations for Power Delivery to important chassis subsystems.

Thermal

- Thermal Design considerations including keep-out zone to enable thermal solutions that extend beyond the CPU and Memory sockets.

10.6 Architecture Specific Assumptions

Mechanical / Systems

- AI Native Edge-MHS based systems
    - HPMs are not considered to be direct plug PSUs but instead leverage Power Distribution Boards (PDB) or other system / rack level power infrastructure. Direct plug power implementations to the HPM do not necessarily preclude compliance with this specification.
    - Use remote fan designs in air cooled platforms (there is no HPM spec provision for Fan connectors on the HPM) – liquid cooling options are not precluded
    - Support riser based I/O cards, cable based I/O cards or a mix of both
    - Leverage a variety of front and rear service models of I/O, PSU, HPM, etc.

- Systems designed for longer HPMs may support use of shorter HPMs of the same Class in a common chassis or sled with minimal changes (e.g. cables, riser quantities, standoff locations)

- Chassis Width Assumptions
    - 19” Multi-node (2x Class N Width) chassis designs leverage static rails with overall inner chassis opening width of 443mm (in 19” rack) and chassis length of 470mm or less
    - 19” Monolithic chassis designs leverage slide rails with overall inner chassis width of 431mm (in 19” rack) and chassis length of 470mm or less

I/O

- AI Native Edge-MHS HPMs will predominately utilize I/O that is above or adjacent to the HPM to fit in the shorter chassis desired in Edge products. Another I/O option would be to integrate capabilities on the HPM and mount the I/O connector directly on the HPM.
- Most systems are expected to leverage coplanar OCP NIC 3.0 Small Form Factor (SFF) layouts when utilized
- Very Short depth (i.e. 350mm or less) systems may require alternate non-coplanar implementation such as “floating” the OCP NIC (or no-pop)
- If OCP NIC 3.0 v1.6 Dual Small Form Factor (D-SFF) is utilized, it is expected to be implemented in a non-coplanar fashion
- PCIe CEM, OCP NIC 3.0v1.6 Dual Small Form Factor (D-SFF), E1, and E3 based I/O will be the predominant use case for consideration but alternate form factors are not prohibited

DC-SCM

- All AI Native Edge-MHS HPM Classes enable (but do not require systems to utilize) use of the DC-SCM R2.2 CFF
- Most systems are assumed to typically leverage the DC-SCM CFF, but management solutions integrated on the HPM shall comply with the DC-SCM 2.2 specification.
- Any solutions implementing the DC-SCM functionality down on the AI Native Edge-MHS HPM shall be software compatible with a DC-SCM R2.2. Failure to do this will result in the AI Native Edge-MHS HPM not being compliant to this specification

10.7 HPM Outline Scalability Enablement – Fixed and Floating Features

AI Native Edge-MHS dimensions various HPM “Features” in two different ways, an example is shown in Figure 6.

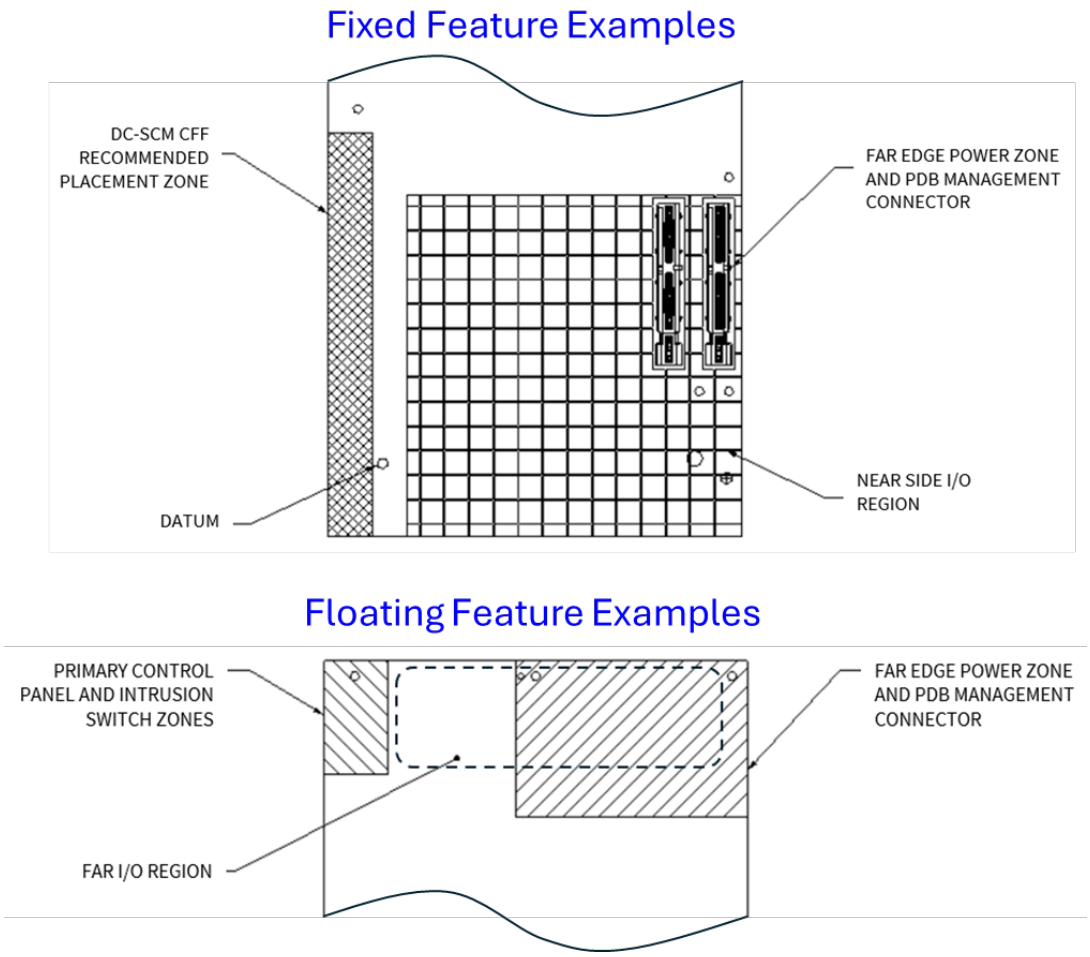
Fixed Features

- Are dimensioned to the Common Datum
- Never move when HPM outline changes
- In some instances, may “drop off” and be not applicable to a smaller HPM
- Examples of fixed features include Risers, the DC-SCM connector, HPM retention hole, etc.

Floating Features

- Are dimensioned to board edges
- Move with the board edges as the edge changes relative to the datum
- Never “drop off” the HPM
- Examples floating features include the Far Side Ingress / Egress power zone, control panel header zones, far side mounting holes, etc.

Figure 6: Example of Fixed and Floating Features

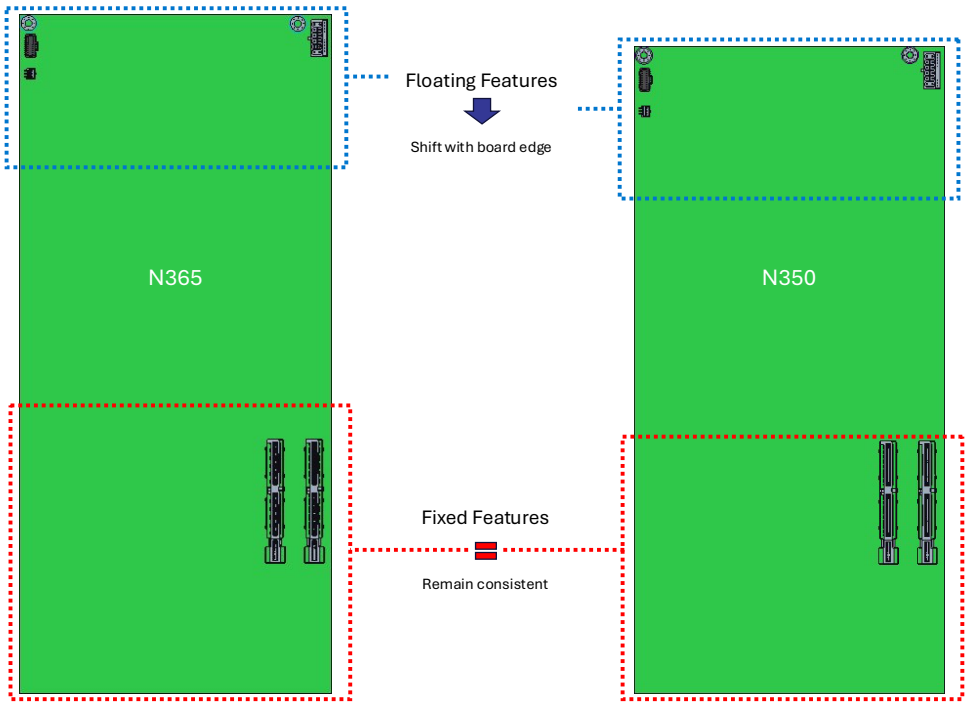


10.8 HPM Outline Scalability Examples

The intent of AI Native Edge-MHS scalability is to provide additional flexibility to HPM designers without causing proliferation of chassis designs required by System designers. This is enabled by ensuring interoperability of smaller HPMs in Chassis designed for larger HPMs (Refer to **Section 10.4 AI Native Edge-MHS Interoperability Goals**) and encouraging HPM designers to carefully consider when their HPM crosses a Common Chassis Interval boundary.

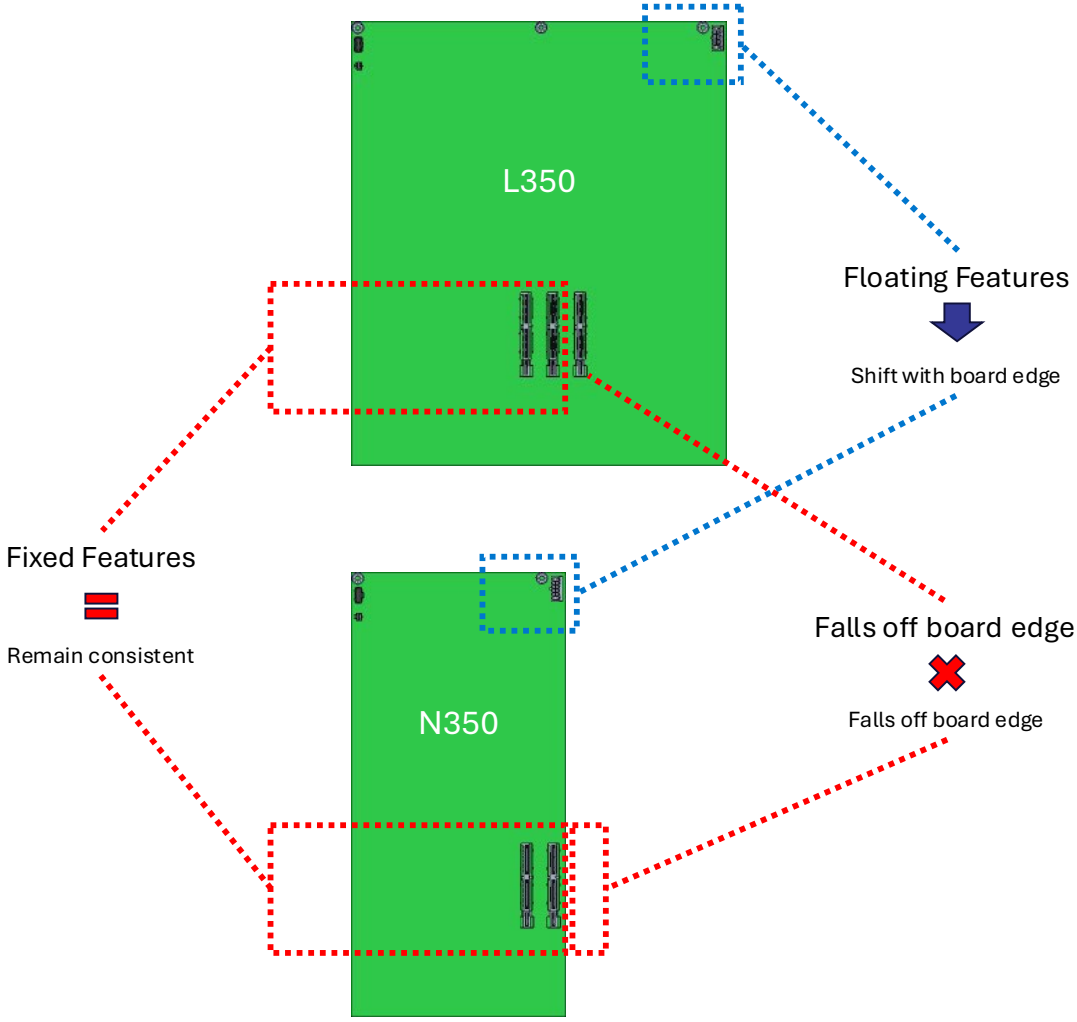
Figure 7 provides an example of Fixed and Floating features when choosing to scale the length of the HPM down from the 365 CCI to a shorter length. Note that both the N365 and N350 HPM can be deployed in a chassis designed to the N365 CCI. If instead the length was scaled longer to N370, the HPM would be incompatible with N365 CCI chassis reducing the scope of systems that HPM could intercept.

Figure 7: Example of Variable Length Scaling



While the width of AI Native Edge-MHS HPMs is not entirely variable, the same Fixed and Floating feature concepts are used to provide consistent layouts across HPM Classes. **Figure 8** demonstrates how Fixed and Floating features enable Class N and Class L HPMs to be leveraged with minimal change into a common system infrastructure.

Figure 8: Example of HPM Consistency Across Class Fixed Width Variability



10.9 Chassis Design Approach for HPM Interoperability - Example

Chassis to HPM interoperability is built on the premise that an HPM tray is used as a form of physical abstraction. This tray will employ features for:

1. Mounting the HPM to the tray
2. Interlocking the HPM tray to the chassis base

The details of these features (standoffs, sheet metal forms, etc.) are outside the scope of this specification, however an example is provided in **Section 16.3 Example Chassis Base Geometry for Chassis-to-Board Bracket interface**.

The bottom side zone 3 KOZs of the deepest HPM supported will dictate the location of the chassis-to-tray interlock features – see **Section 12.3.2 Zone 2: Chassis to HPM Bracket (Board Pan) KOZ** Requirements) for KOZ details.

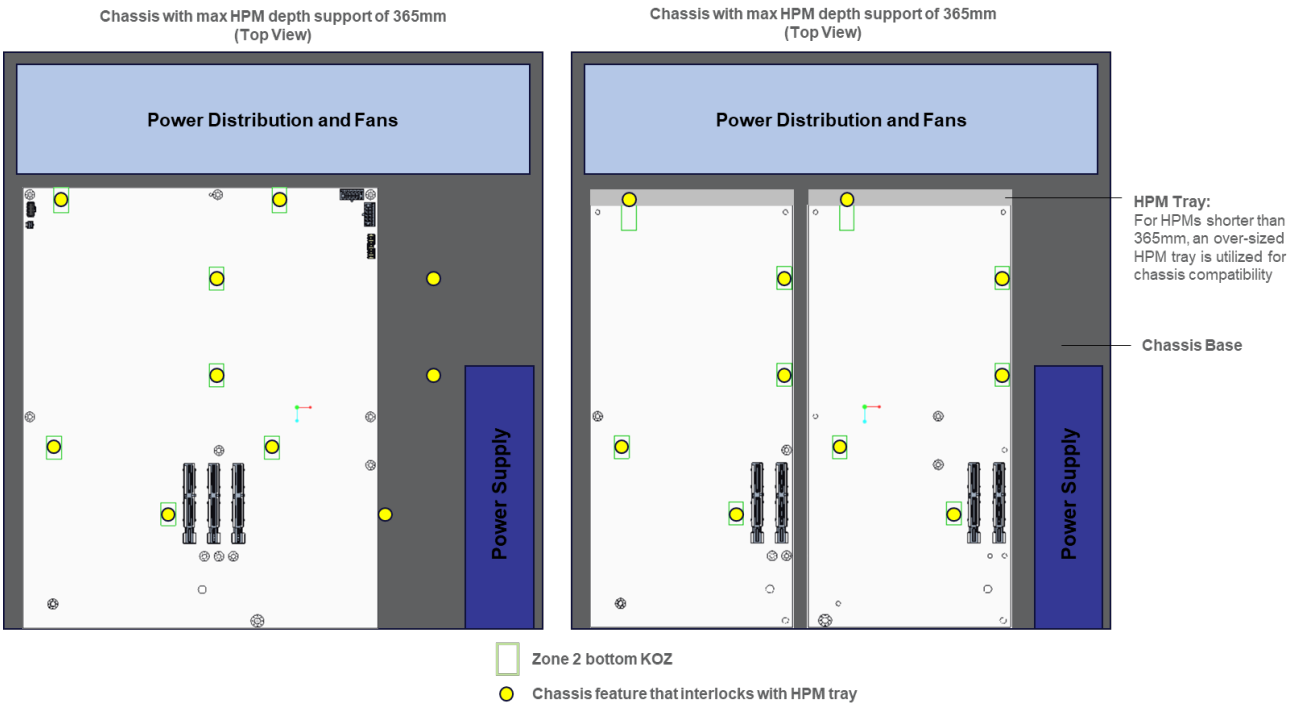
The chassis design will dictate the maximum supportable HPM depth. Any HPM of a lesser depth should also be supportable via an HPM tray that is deeper than the HPM and designed to be fully compatible with the chassis' fixed interlock features.

The following example illustrates this concept. While this example uses two specific HPMs (L365 and N350), the same concept applies to any interoperable HPM combination noted in **Section 10.4 AI Native Edge-MHS Interoperability Goals**.

In this hypothetical example, a chassis has been designed for compatibility with a 19" rack. The chassis design also limits the maximum HPM depth to 365mm. The left-side image of **Figure 9: Example Chassis Interface and Pan Strategy for Shorter HPMs** depicts a L365 HPM in this chassis. The green rectangles represent the HPM zone 2 bottom side KOZs. The yellow circles represent the chassis features used to interlock with the HPM tray. In the left image the HPM tray is not visible because it is fully under the HPM.

The right-side image of **Figure 9: Example Chassis Interface and Pan Strategy for Shorter HPMs** represents this same chassis but now populated with two N350 HPMs (placed on a 181mm pitch). The same chassis interlock features are used for securing these two HPM assemblies. But note that the N350 tray is longer than the HPM and includes the mating interlock features just beyond the HPM Far Side edge.

Figure 9: Example Chassis Interface and Pan Strategy for Shorter HPMs



Finally, note that the N350 HPM, when assembled in this example chassis, does not make use of its Far Side edge bottom side zone 2 KOZs. This does not mean these KOZs are not required to be implemented on this HPM. They are needed in a scenario where this same HPM is utilized in different chassis that is limited to maximum HPM depth equal to ~350mm.

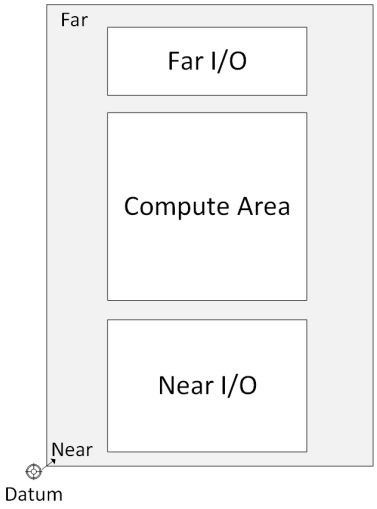
11 HPM Concepts and Layouts

Definitions and concepts that apply to AI Native Edge-MHS HPMs are described below:

1. Due to the wide array of potential HPM and Chassis configurations, this specification defines a **Near** <<Element>> as the <<Element>> closer to the Datum (0,0 reference) and **Far** <<Element>> as the <<Element>> further from the Datum, examples for <<Element>> include:
    a. Side
    b. Corner
    c. Edge
    d. I/O Zone

    An example of Near and Far terminology usage is shown in **Figure 10**.

Figure 10: Near and Far Terminology Example (Class N Depicted)



2. Consistent Riser locations are used across interoperable AI Native Edge-MHS HPMs

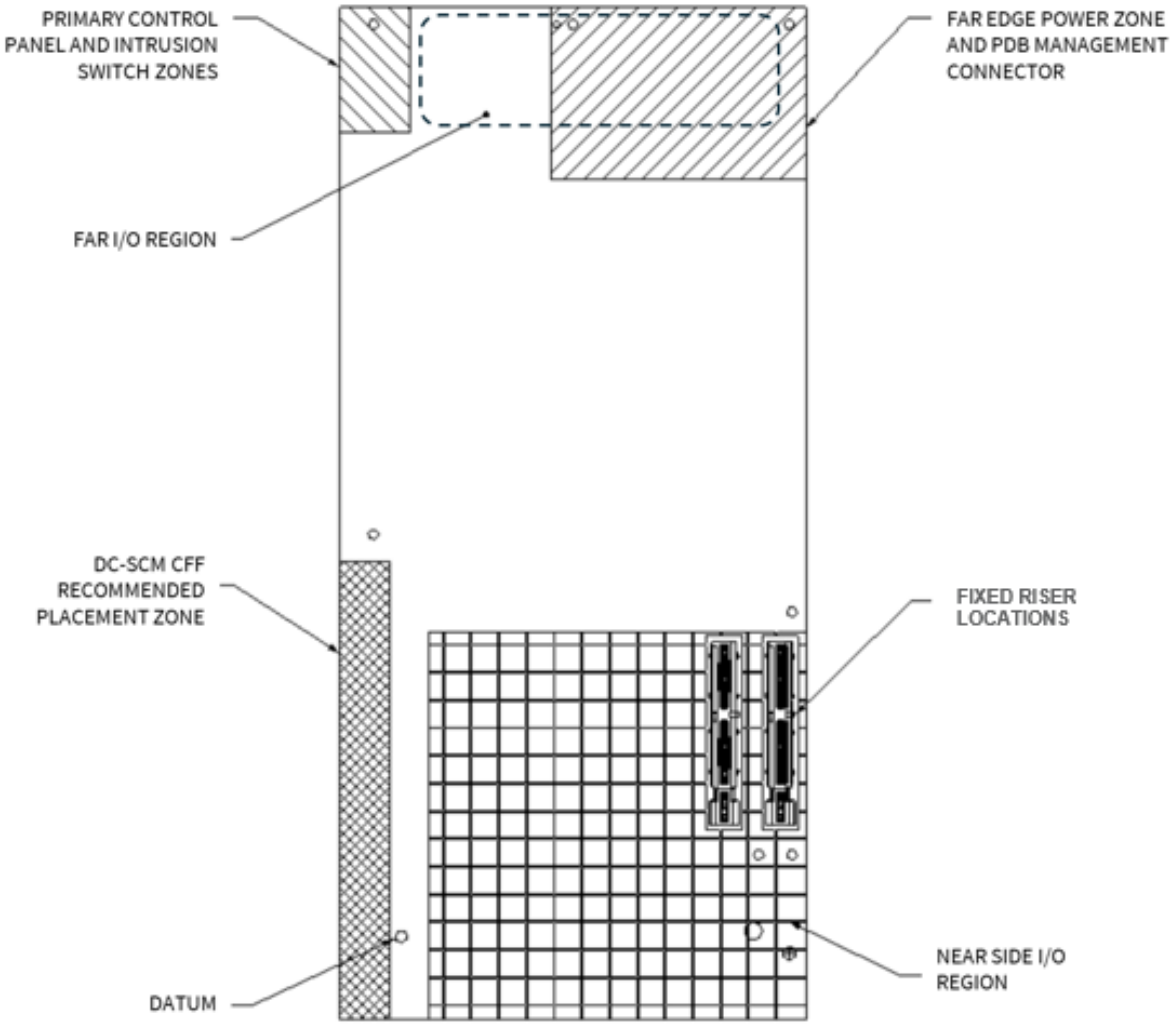
3. HPM width references refer to the following dimensions:

    a. AI Native Edge-MHS Narrow refers to the common 168mm HPM width shared by all Class N HPMs
    b. AI Native Edge-MHS Large refers to the common 295mm HPM width shared by all Class L HPMs

11.1 Class N HPM Layout

Class N is considered a form factor optimized for single node or multi-node 19” rack environments targeted at Edge applications with chassis depths typically between 350mm and 470mm. **Figure 11** shows the layout and approximate locations of major subsystems of this HPM. IO Connector zones depicted are representative only and not strictly defined.

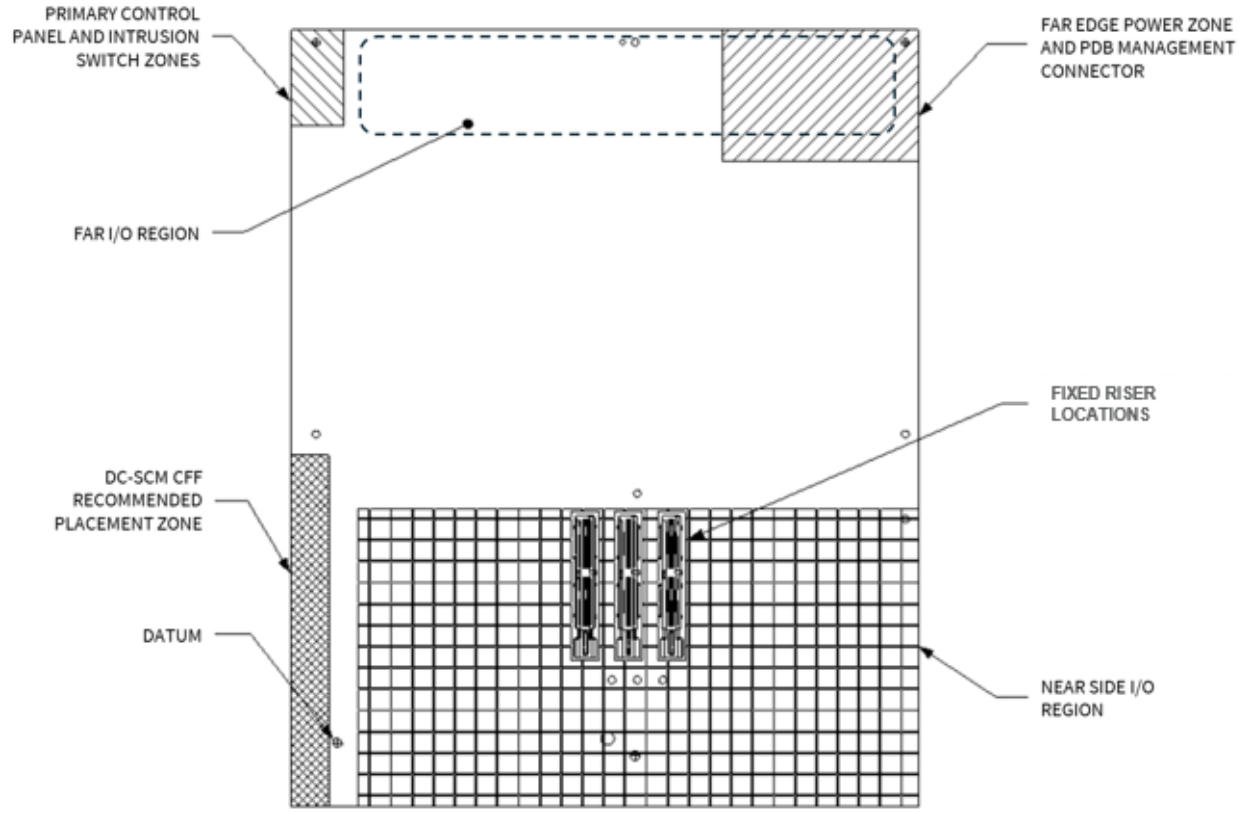
Figure 11: Class N HPM Overview (PRIMARY SIDE)



11.2 Class L HPM Layout

Class L is form-factor optimized for single node 19” rack environments targeted at Edge applications with chassis depths typically between 310mm and 470mm. **Figure 12** shows the layout and approximate locations of major subsystems of this HPM. IO Connector regions depicted are representative only and not strictly defined.

Figure 12: Class L HPM Overview (PRIMARY SIDE)



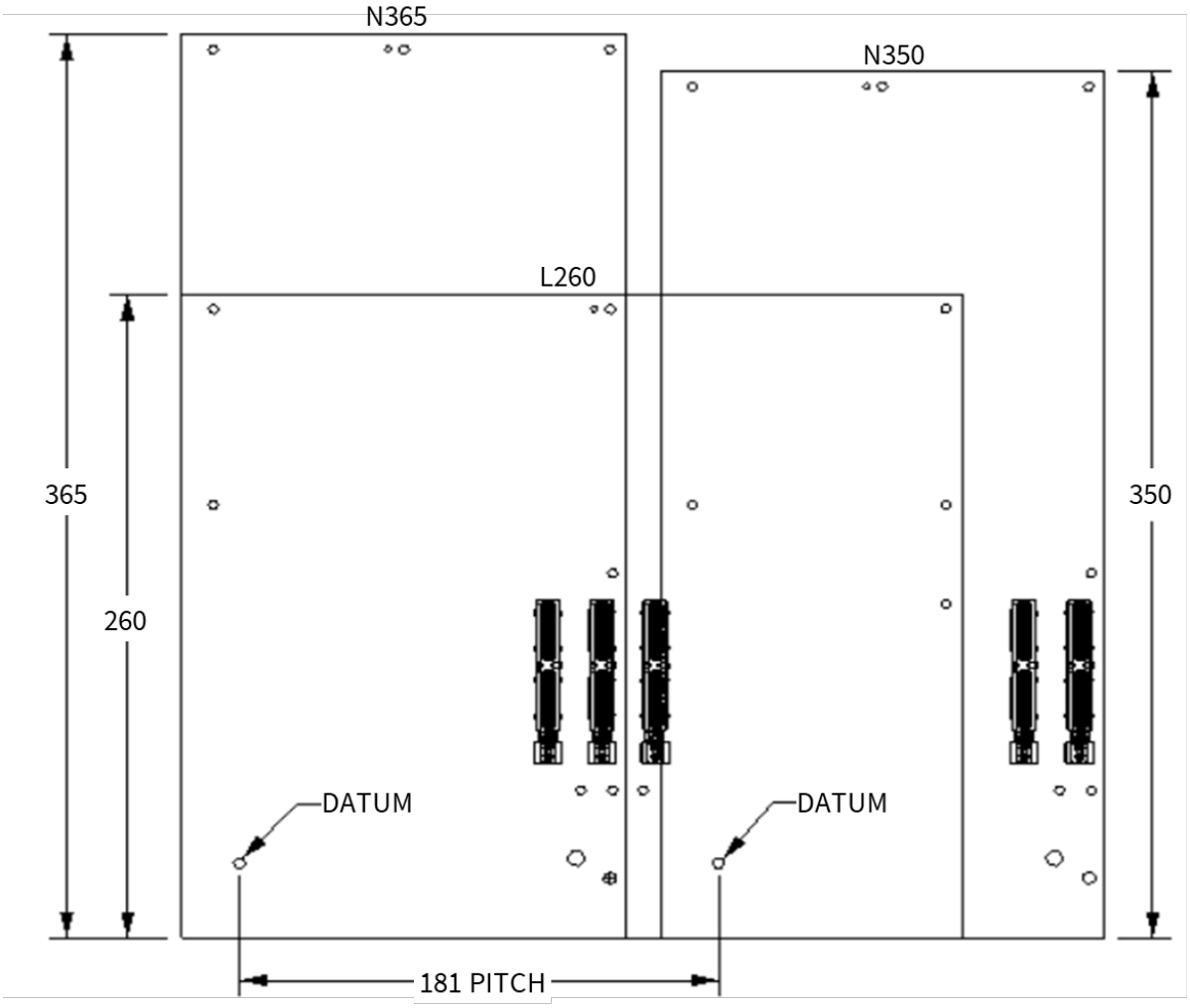
11.2.1 19 Common Chassis Supporting Classes N and L

HPM Classes N and L are defined such that they can share a common 19” chassis if desired. The chassis could be designed to support a single Class N, a single Class L, two Class N (1U), or up to four Class N (2U) AI Native Edge-MHS HPMs

Figure 13 illustrates the HPM positioning required for such a common chassis. The HPMs on the left are aligned at their origins. The Class N HPM on the right is offset from the left Class N HPM by 181mm. When positioned in this manner the I/O (i.e DC-SCM R2.2 CFF, Ethernet I/O, the SFF-TA-1033 riser connectors), and the HPM retention holes are all aligned. HPM trays are utilized to facilitate this chassis compatibility.

The HPM depths shown are illustrative only. The scheme can apply to any HPM depth combinations. The maximum supportable HPM depth is determined by the chassis design which is outside the scope of this specification. Whatever maximum depth is supported, any HPM of a lesser depth should also be supportable.

Figure 13: Common 19” Chassis Supporting Class N and Class L (PRIMARY SIDE)



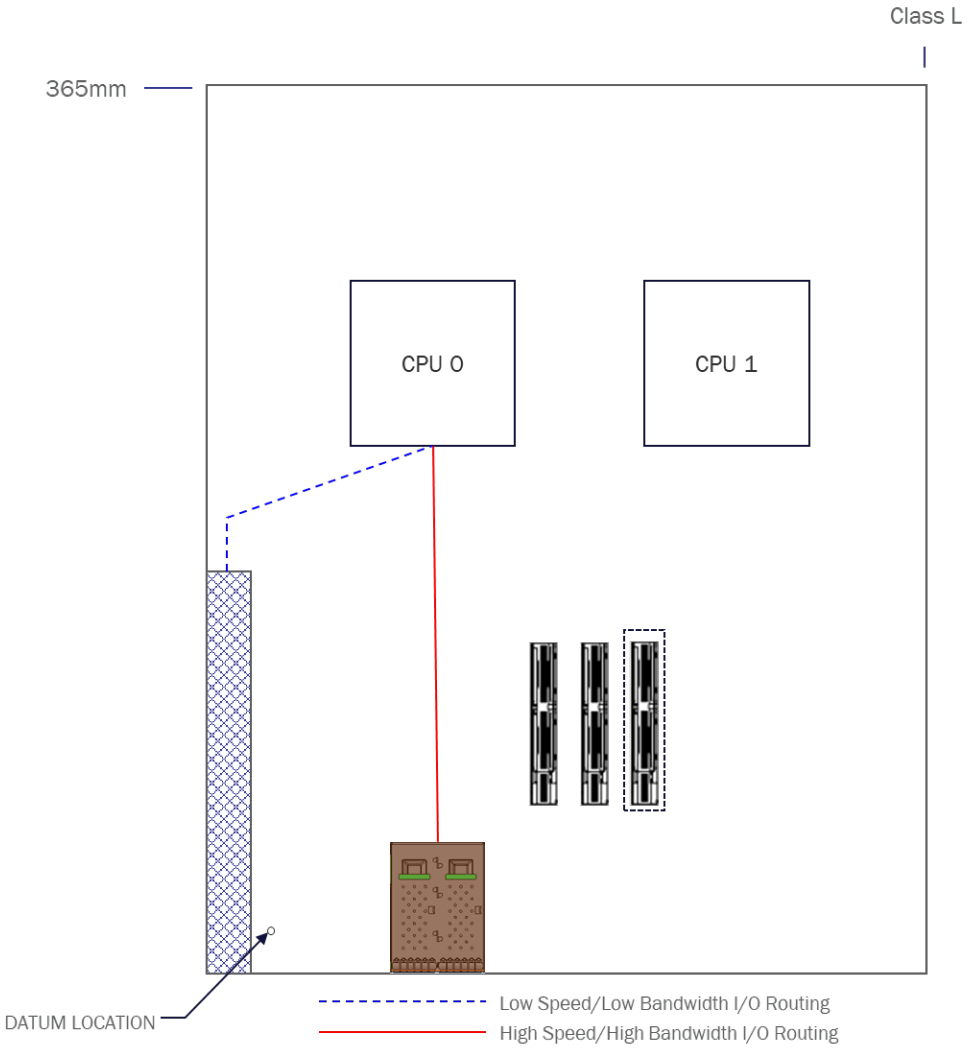
11.3 Class L Two Socket (CPU) Assumptions

The recommended location for the DC-SCM R2.2 CFF is positioned to the left, as seen in **Figure 14**. To maintain as much commonality between AI Native Edge-MHS HPM specifications and multi-node placement compatibility the following rules apply:

- In a two socket (CPU) HPM the first/boot CPU is positioned to the left.
- High-speed I/O, such as Ethernet or OCP NIC 3.0, is directly routed through the HPM PCB to the first/boot CPU.

These high-speed I/O interfaces are intended to be located closer to the boot CPU to facilitate high-speed signal routing. Ethernet and OCP NIC 3.0 interfaces typically require high-bandwidth routing and should be optimized for material selection and cost considerations.

Figure 14: AI Native Edge-MHS HPM First CPU Assumed Position (Class L PRIMARY SIDE Shown)



12 Mechanical Requirements

In addition to the drawings and details within this document, DFX/CAD files will be provided for further detail.

Unless otherwise specified all units are in mm.

Unless otherwise specified, PCB dimensions shown in this specification shall comply to **Table 4**.

Table 4: Standard Tolerances

Dimension Type	Tolerance, unless otherwise specified
FROM Origin/Datum hole center TO round fiducial center	+/- 0.076mm (+/- 0.003 inch)
FROM Origin/Datum hole center) TO profiled card edge	+/- 0.254mm (+/- 0.010 inch)
FROM Origin/Datum hole center TO drilled hole center	+/- 0.127mm (+/- 0.005 inch)
FROM Profiled card edge TO profiled card edge	+/- 0.127mm (+/- 0.005 inch)
Feature of size (hole diameter, slot width, etc.)	+/- 0.100mm (+/- 0.004 inch)
PCB thickness	+/- 10% of nominal

Route KOZ's referenced in this specification, at a minimum, refer to surface layers and microstrip routing. Further application of the Route KOZ to other layers is the choice of the HPM designer and/or Design specification.

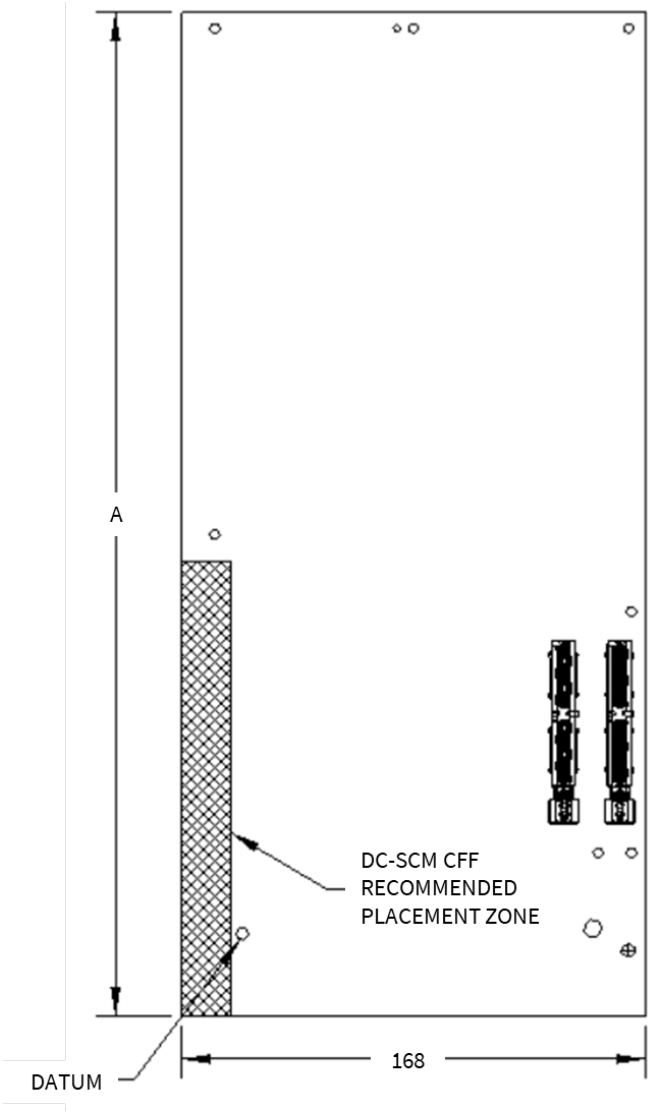
12.1 HPM Outlines

There are two classes of HPMs in this specification release, each class has recommended depths aligned to Common Chassis Intervals. The required board outlines are defined in **Figure 15: AI Native Edge-MHS Class N HPM Board Outline (PRIMARY SIDE)**, AI Native Edge-MHS HPMs shall comply with these board outlines.

12.1.1 Class N HPM Board Outline

The Class N HPM is defined as a fixed 168mm width and an allowed depth ranging between 250mm and 365mm. Although a compliant HPM may be designed to any depth within this range, there exists four distinct Common Chassis Intervals (CCI) which it is recommended that HPM designers attempt to utilize these intervals for maximum ecosystem compatibility**. Figure 15** Illustrates a Class N HPM.

Figure 15: AI Native Edge-MHS Class N HPM Board Outline (PRIMARY SIDE)

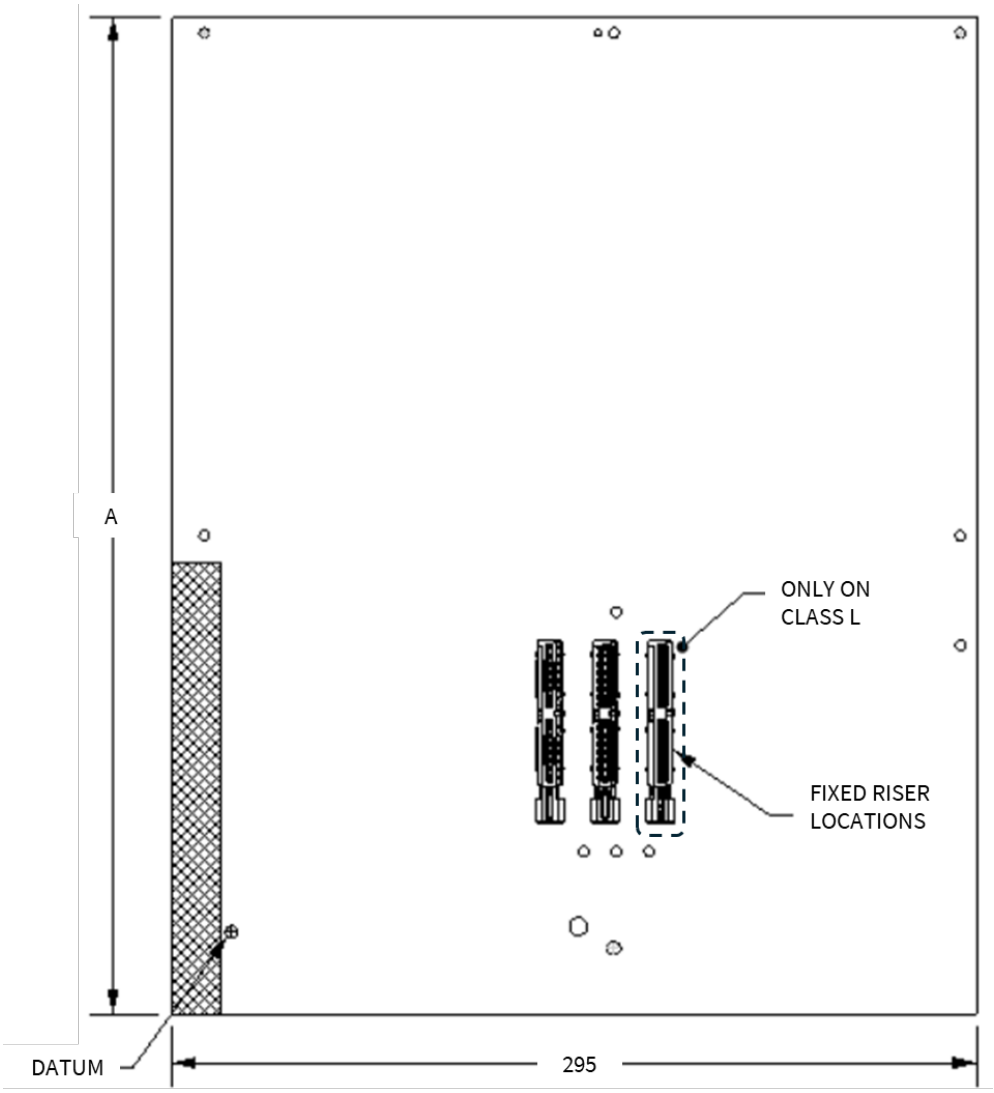


HPM Designator	A	Targeted 19” Server Depth
N260	260mm	310mm Server
N280	280mm	350mm to 420mm Server
N305	305.59mm	Compatible with M-DNO Type 4 Size
N350	350mm	420mm to 450mm Server
N365	365mm	OTII-E Class Server

12.1.2 Class L HPM Board Outline

The Class L HPM is defined as a fixed 295mm width and an allowed depth ranging between 250mm and 365mm. Although a compliant HPM may be designed to any depth within this range, there exists several distinct Common Chassis Intervals (CCI) which it is recommended that HPM designers attempt to utilize for maximum ecosystem compatibility.

Figure 16: Class L HPM Board Outline (PRIMARY SIDE)

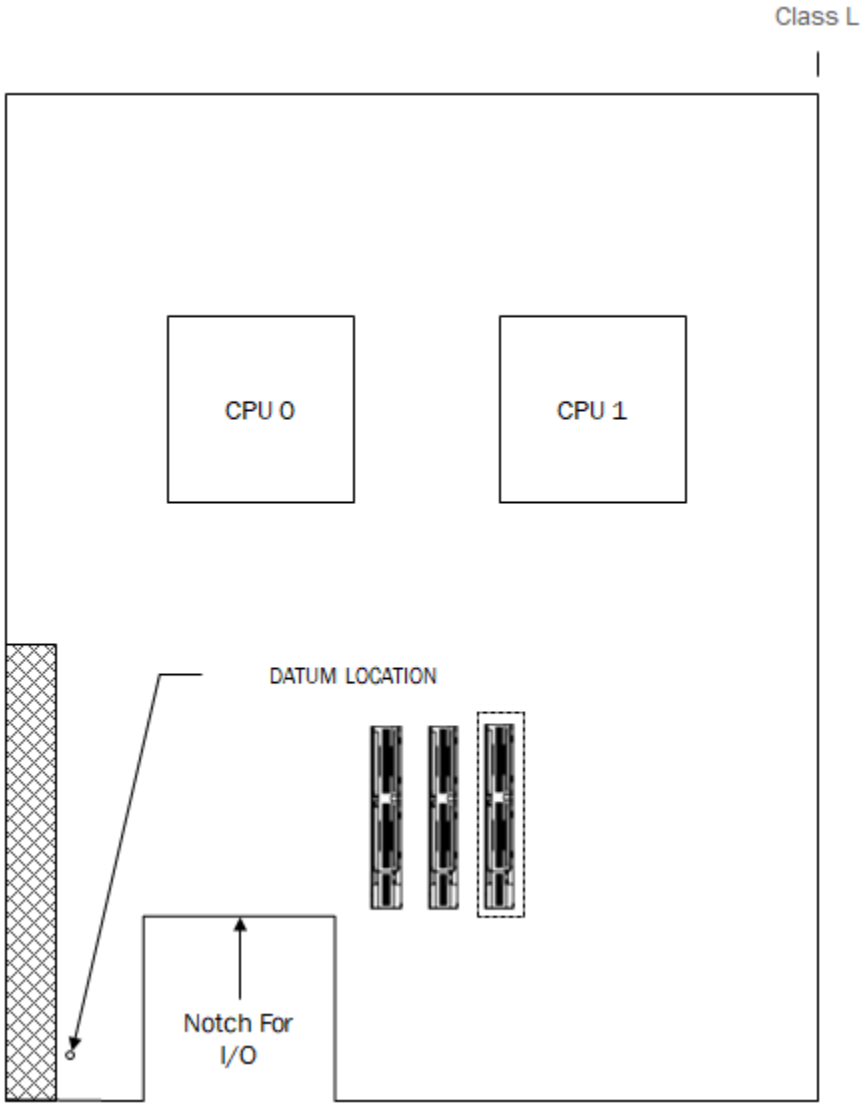


HPM Designator	A	Targeted 19” Depth
L260	260mm	310mm Deep Server
L280	280mm	350mm to 420mm Server
L305	305.59mm	M-DNO Type 4 Size
L350	350mm	420mm to 450mm Server
L365	365mm	OTII-E Class Server

12.1.3 Allowance for Negative PCB Features

All HPM Classes may include “negative PCB features” with the noted limitations. A negative PCB feature is defined as removal of PCB material in localized areas of the HPM outline. Examples of negative PCB features include notches along a board edge or openings of any geometric shape within the HPM outline. See **Figure 17** for illustrative example.

Figure 17: L365 HPM with Compliant Negative PCB Features



All negative PCB features implemented shall comply to the following restrictions:

3. Negative PCB features shall not violate or conflict with any required features such as mounting holes and connector placement.
4. The negative PCB feature shall not extend the full length of the left or right edge of an HPM (i.e., this feature shall not be used to essentially create a non-standard HPM width).

Implementors Notes:

HPM-level and system-level manufacturing, handling, shipping, and operational environments must be considered by the HPM designer. When implementing negative PCB features the HPM designer should consider the implications on HPM structural integrity.

The use of a negative PCB feature can afford the option of a chassis or HPM tray feature to reside within this evacuated area. However, it should be noted that if this chassis or HPM tray feature must always be present, then other specification compliant HPMs that do not have these negative PCB features may not be interoperable with this system. An ideal system implementation would not require these negative PCB features to be present on all supported HPMs.

An example application of a negative PCB feature is depicted in Figure 15: L365 HPM with Compliant Negative PCB Features above.

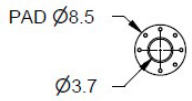
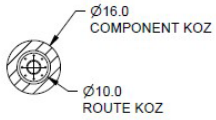
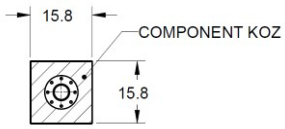
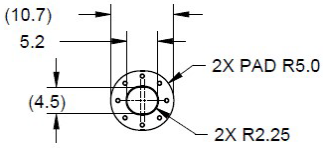
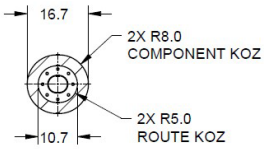
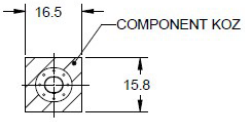
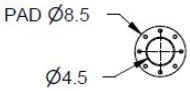
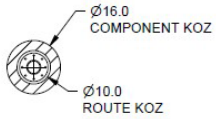
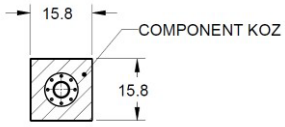
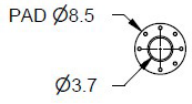
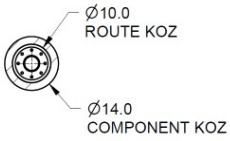
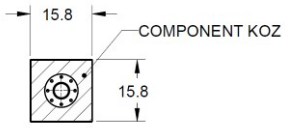
12.2 Board Datum and Mounting Hole Information

All AI Native Edge-MHS board Classes leverage a common datum location at the center of a specific near side edge mounting hole as illustrated in **Figure 19** and **Figure 20**. This allows for fixed elements (riser connectors, peripheral connectors, …) to have a common reference across all board Classes.

Detailed hole information common to all board Classes are provided in **Figure 18**. The vias that are shown in Figures are for reference only. Via requirements are NOT in scope of this specification. All holes shall adhere to the specified size, ground pad dimensions, component KOZ and route KOZ.

The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension (i.e. a DIMM connector), it is considered more robust and may encroach on the Component KOZ's.

Figure 18: Hole Detail Reference

	Hole and Pad Sizes	Top Side KOZs	Bottom Side KOZs
DETAIL A Standard Mounting Hole			
DETAIL B Unique Alignment Slot			
DETAIL C Unique Alignment Hole			
DETAIL D Riser Retention Holes			

It is expected that HPM designers will add additional mounting holes based on their HPM layout. All additional holes shall adhere to Standard Mounting Hole requirements (Detail A in **Figure 18).**

A design should follow good engineering practices in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

There are required holes associated with each Near IO fixed riser location (Detail D in **Figure 18)** that shall be implemented when a fixed riser connector is implemented.

Riser retention holes are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). System designers may choose the hardware and utilization method for riser retention.

Required and recommended board mounting hole locations are specified for AI Native Edge-MHS HPM Class N and L in **Figure 19 and Figure 20 .**

Implementors Note:

The PCB Datum hole (Detail C) is defined such that a collared standoff with tight tolerance fit can be used to control X-Y tolerances in HPM mounting. Additionally, a slotted hole (Detail B) is defined to control rotation around the datum, by allowing, as an example, a collared standoff to be used with tight fit to the top/bottom edge of the slot.

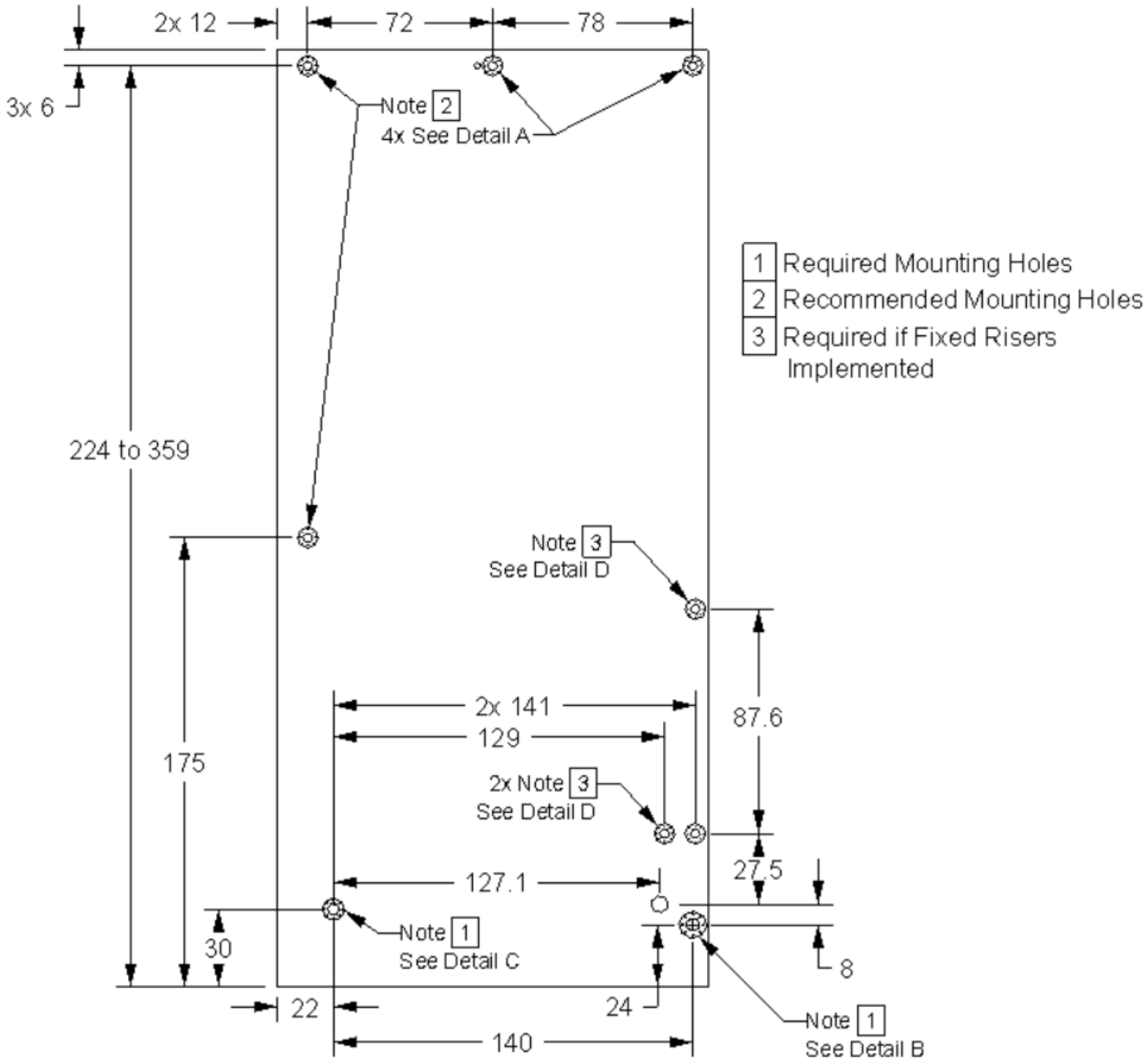
All other mounting holes follow standard mounting hole guidance (Detail A). These mounting holes are expected to have clearance fits to screw hardware.

12.2.1 Class N HPM Mounting/Riser Holes

There are 5 required mounting/riser holes on the Class N HPM near side that shall be implemented when risers are implemented and two required mounting holes on the Class N near side when risers are not implemented (the Datum Hole and Alignment Hole).

There are three recommended mounting holes on the Class N HPM Far Side. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm with a recommended span of 78mm. **Figure 19** shows the placement of the required and recommended holes.

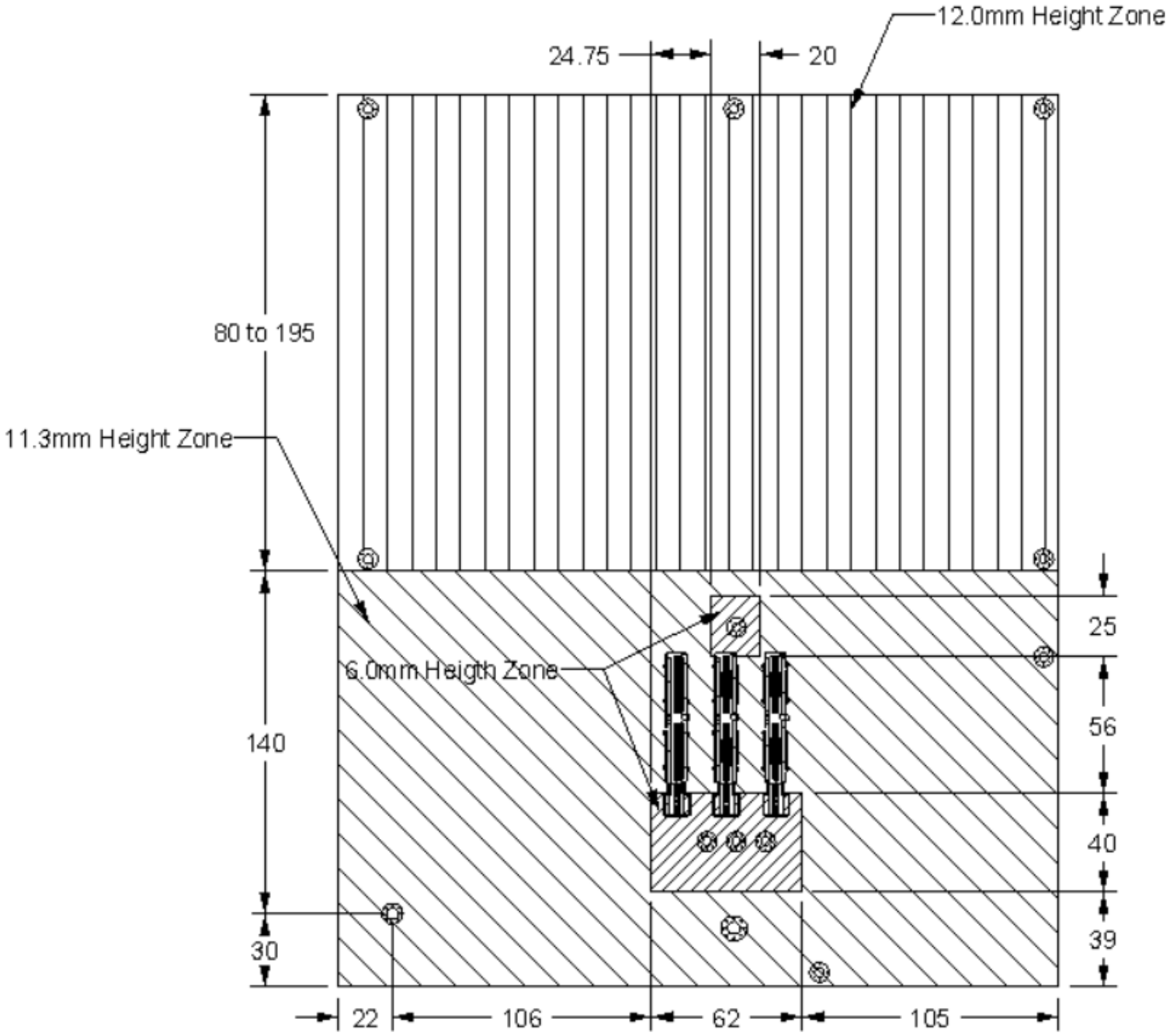
Figure 19: Class N HPM Mounting/Riser Holes (N365 PRIMARY SIDE illustrated)



12.2.2 Class L HPM Mounting/Riser Holes

There are 7 required mounting/riser holes on the Class L HPM near side that shall be implemented when risers are implemented and two required mounting holes on the Class L near side when risers are not implemented (the Datum Hole and Alignment Hole). Additional recommended mounting holes for specific optional near side custom zone implementations are indicated in **Section 12.10.1: Class L HPM** Primary Side Component Height Restrictions

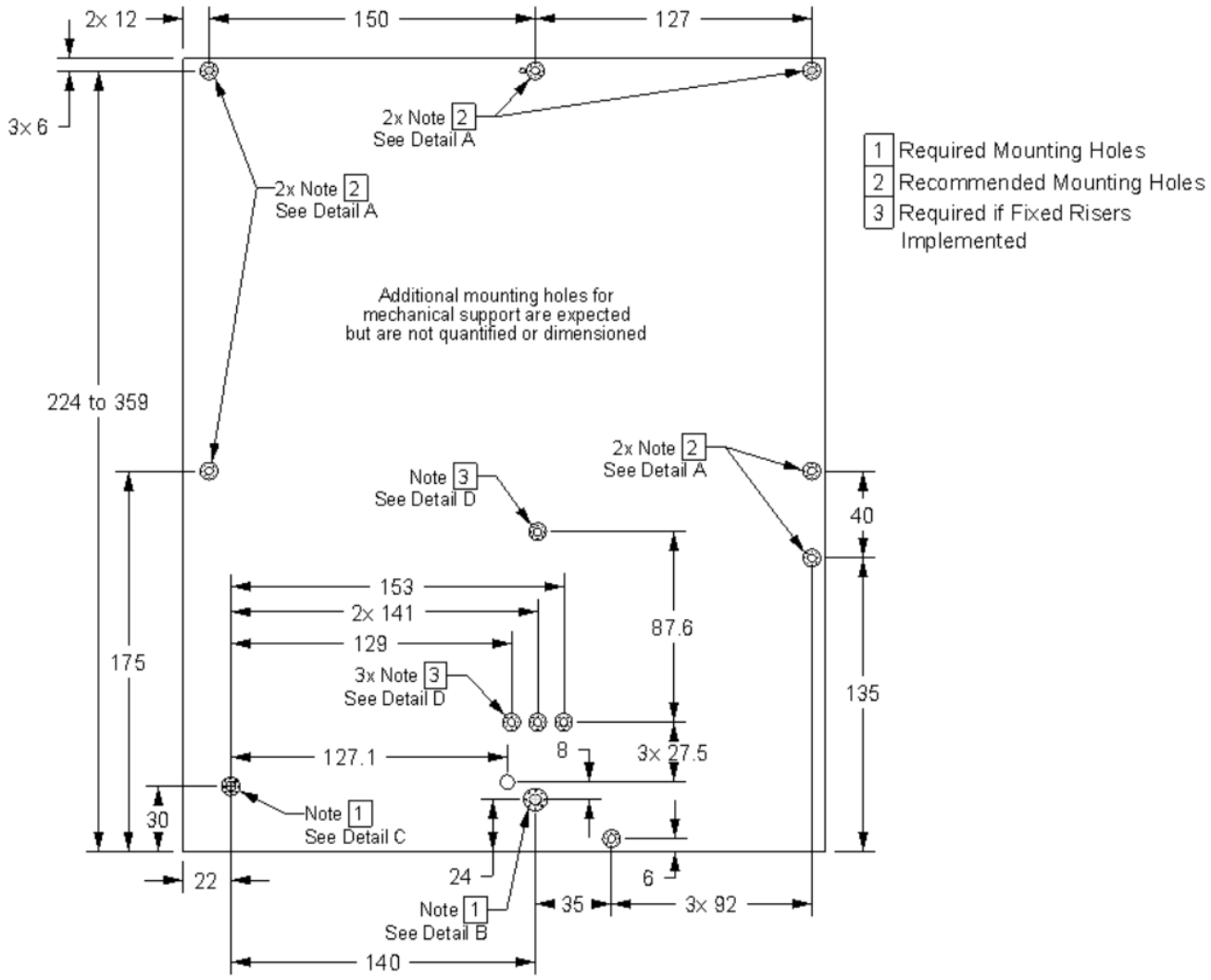
Figure 42: Class L Component Height Restriction Zones (PRIMARY SIDE)



Platform Custom Zone.

There are three recommended mounting holes on the Class L Far Side. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 156mm. **Figure 20** shows the placement of the required and recommended holes.

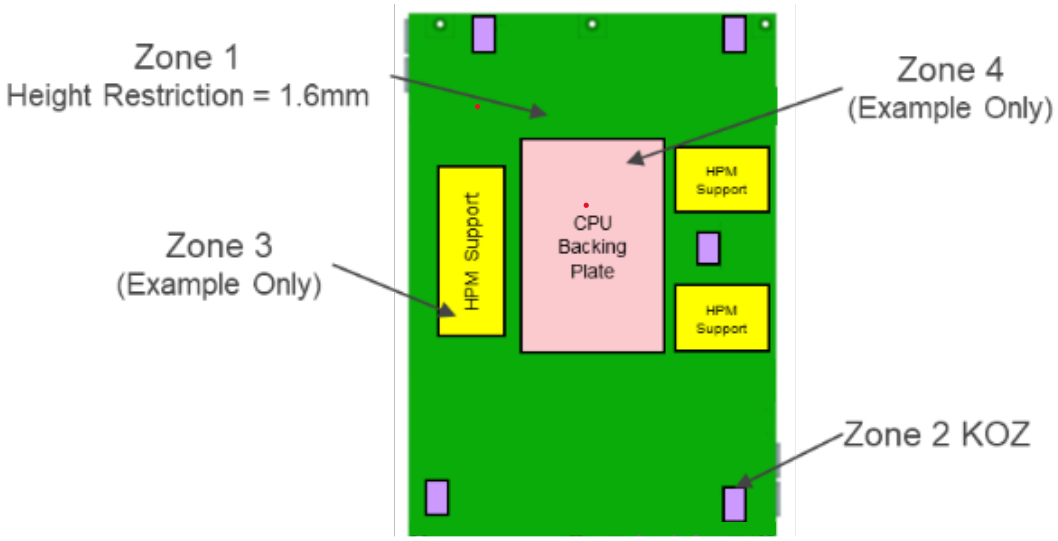
Figure 20: Class L HPM Mounting/Riser Holes (L365 PRIMARY SIDE illustrated)



12.3 Secondary Side Zones and Height Restrictions

There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 21**:. Each zone serves a unique purpose. Zones 1, 2, 3 and 4 define different requirements for compliance.

Figure 21: Secondary Side Zone Definitions



12.3.1 Zone 1: Secondary Side Height Restriction

Zone 1 universally applies to the entire secondary side of the HPM, except for the defined Zones 2, 3, and 4. HPM electrical components are expected to utilize Zone 1.

All AI Native Edge-MHS HPMs shall implement the Zone 1 universal secondary side component height restriction of 1.6mm for all board Classes. This requirement ensures HPM component clearances to chassis base or board pan structures. This is especially important with a max allowable board thickness as defined in **Section 12.4: HPM Board and Assembly Thickness**.

12.3.1.1 Zone 1 Exceptions for Secondary Side Tall Components

In some instances, an HPM Designer may desire placement of tall secondary side components (such as special capacitors) that exceed the secondary side height restriction. Although this should be avoided, an HPM Designer may implement local exceptions if the following conditions are met:

1. Exceptions are contained to small areas of the secondary side and shall not exceed 400mm^2 area per instance.
2. No two instances of a secondary side exception shall be closer than 10mm, as to not drive excessive cutouts in Chassis-to-HPM bracketry.

It is recommended that (HPM Thickness + Height of Components) in Exception Areas never exceed 5.2mm. This total height enables common 2mm components on all AI Native Edge-MHS compliant HPM thicknesses while mitigating potential system compatibility issues, for example:

- 5.2mm – 2.36mm thick HPM = 2.84mm max component thickness
- 5.2mm – 3.18mm thick HPM = 2.02mm max component thickness

Care should be taken to ensure that there is no risk if components in the exception areas touch uninsulated chassis elements.

Implementors Note:

Secondary side exceptions for tall components may cause compatibility challenges between the HPM and System. HPM designers should work closely with the intended System Designers to ensure the exception locations and specific component heights are acceptable.

Numerous considerations outside the scope of this specification will determine the severity of compatibility issues. Examples include but are not limited to shock and vibration, chassis mechanical features, HPM uniformity, tolerancing, solder thickness, etc.

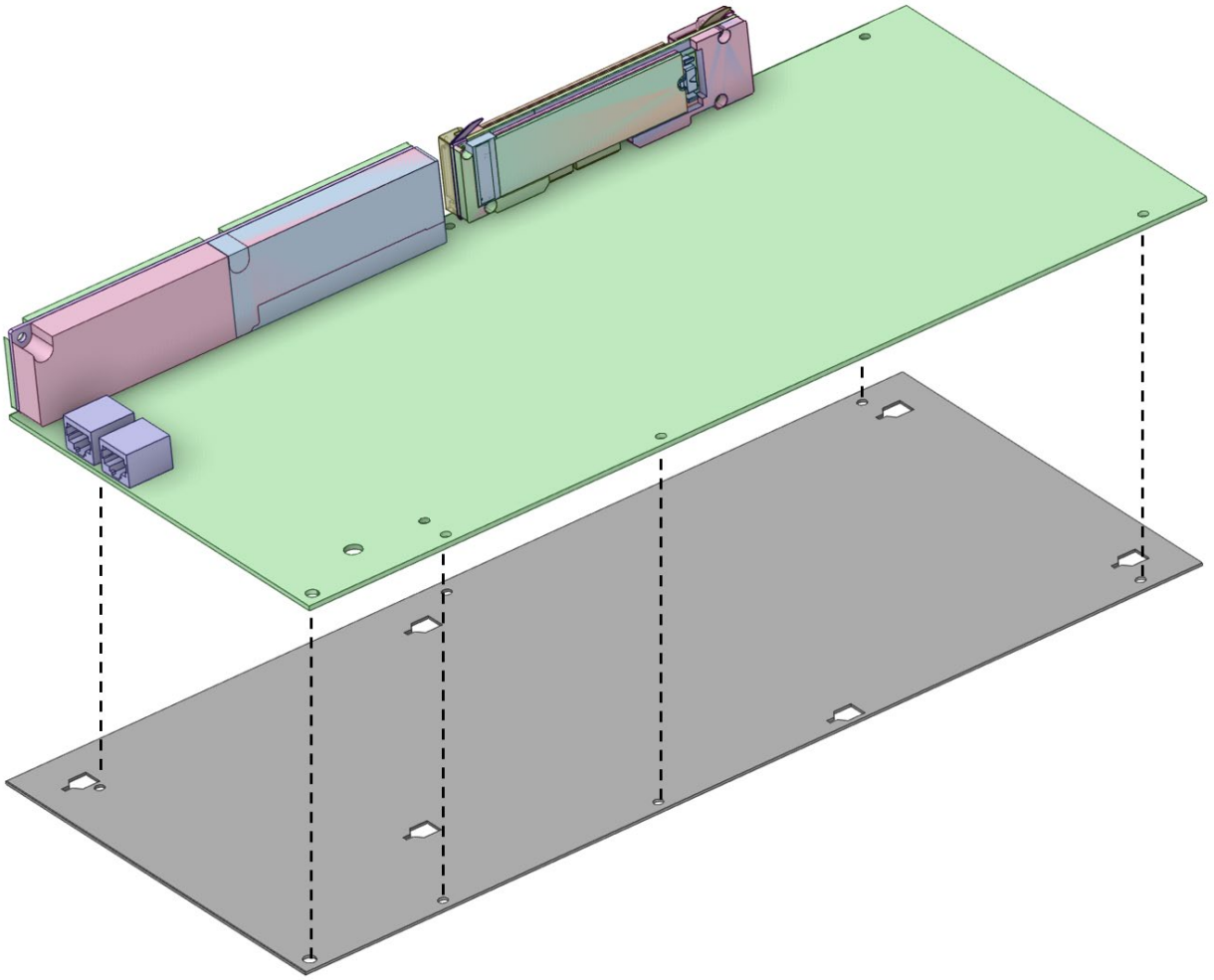
12.3.2 Zone 2: Chassis to HPM Bracket (Board Pan) KOZ Requirements

AI Native Edge-MHS HPMs allow for a Chassis-to-Board Bracket (Board Pan) which enables different board layouts (and mounting hole locations) between HPM Classes and Compute Core designs, while maintaining compatibility to a common chassis.

An example AI Native Edge-MHS Class N Board Pan is shown in **Figure 22**.

Figure 22: Example of Chassis-to-Board Bracket

(Board Pan – note that the hole placement below may not match the HPM specification as the illustration is to showcase how the mounting apparatus will work)



A supporting chassis base shall provide geometry to interface the cutouts on the Chassis-to-Board Bracket (Board Pan). For an example of a chassis hook concept, see **Section 16.3 Example Chassis Base Geometry for Chassis-to-Board Bracket interface**. The geometry of the Board Bracket is not specified and is a design choice for the System Designer.

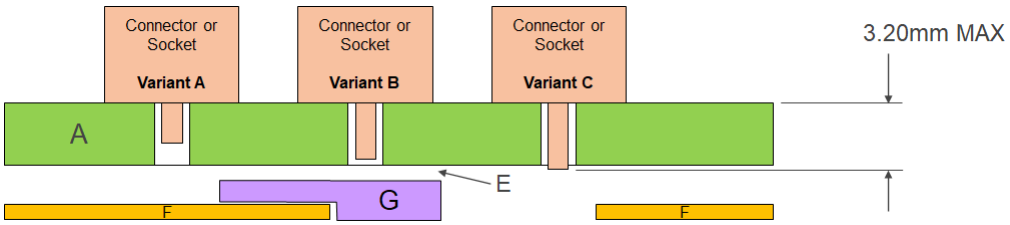
Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb shall be 3.20mm MAX such that it will not interfere with chassis hook features.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout.

Implementors Note:

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly. Refer to **Table 5: Example Z-Height Compliant Stack-Up, Per Zone** for details on 'A'. 'E', 'F' and 'G'.



Implementors Note:

While most monolithic server designs benefit from a Board Pan, it is NOT expected that all systems supporting AI Native Edge-MHS HPMs will require a Board Pan. Specifically, sled-based designs common in multi-node systems typically do not require a board pan. An example sled based secondary side zone stack-up can be derived by referring to Table 3 and replacing the space allocated to item 'F' and 'G' with the sled mechanicals.

Each AI Native Edge-MHS HPM Class shall support required zero height KOZ locations for chassis hook features that interface between the chassis base and the chassis to board bracket (board pan) as depicted in **Figure 23**: **through Figure 26**.

The floating far side edge KOZs shall be required for all HPM depths.

For each HPM Class, two drawings are provided. The first drawing illustrates the minimum anticipated depth for a given HPM class and the second illustrates the largest anticipated HPM length for that same class.

Figure 23: and **Figure 25** depict all KOZ locations for the minimum anticipated HPMs in each Class N. **Figure 24** and **Figure 26** depict all KOZ locations for the maximum anticipated HPMs in each Class L.

If the far side edge of the HPM intersects this KOZ area, then a partial KOZ shall be implemented. The resulting KOZ should be colinear with the PCB edge.

For additional information, refer to **Section 10.9 Chassis Design Approach for HPM Interoperability - Example**.

12.3.2.1 Class N HPM Zone 2 Secondary Side Chassis KOZ

Figure 23: Class N250 Chassis Hook Locations (SECONDARY SIDE)

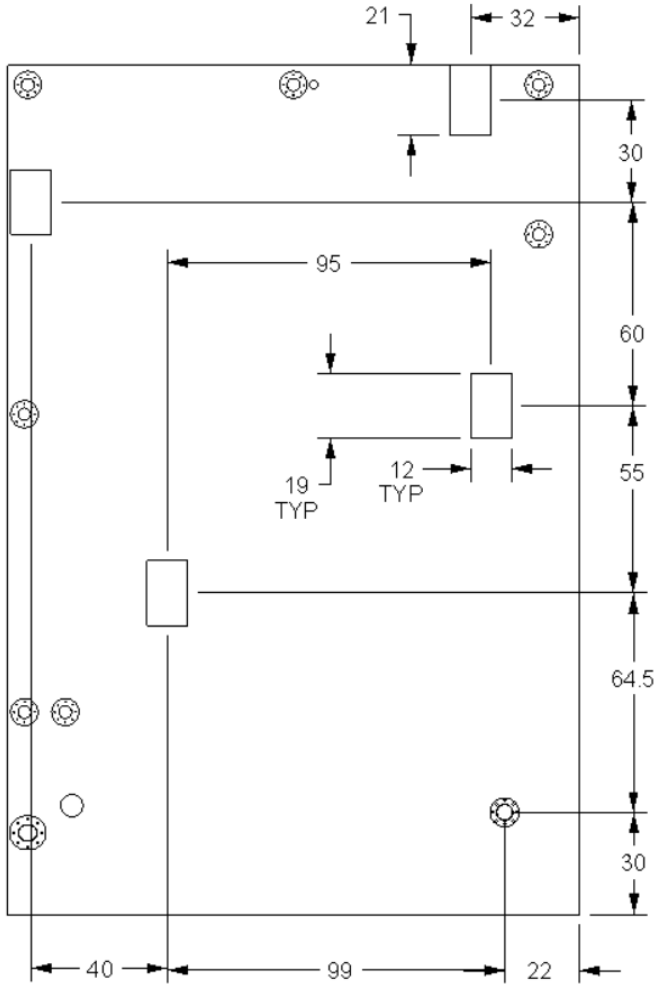
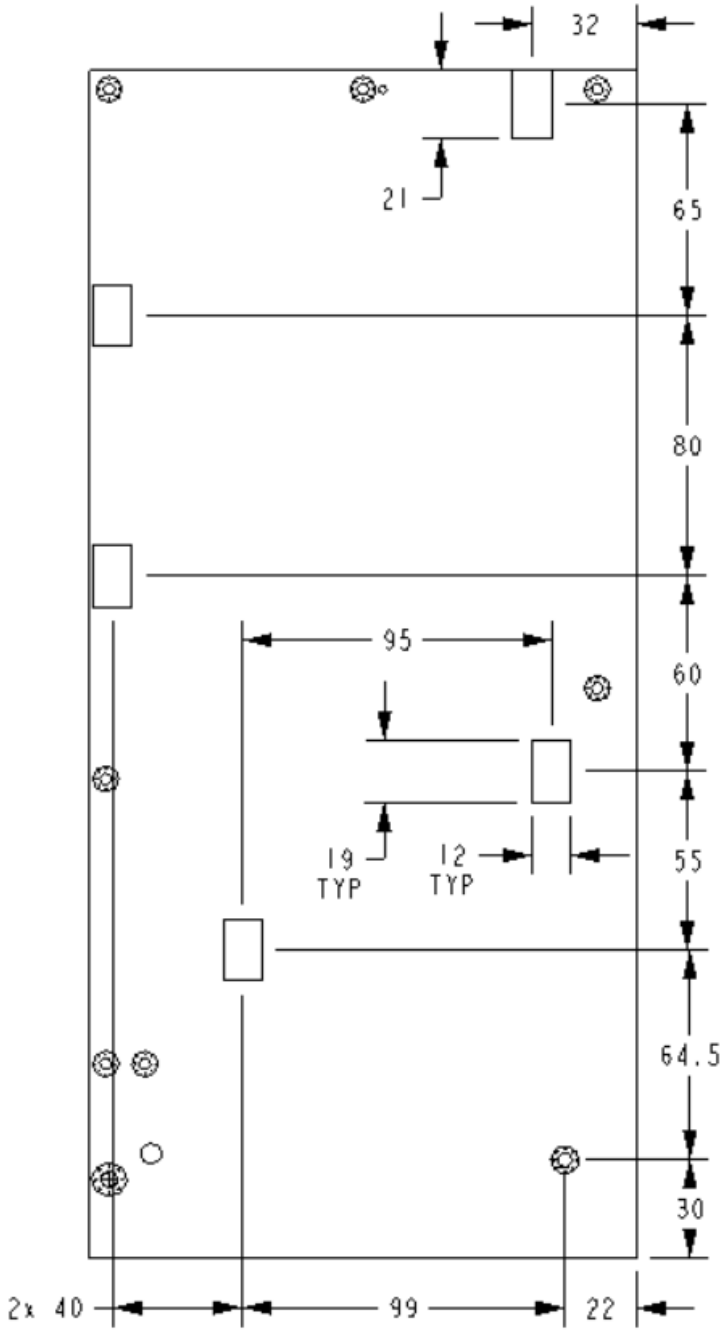


Figure 24: Class N365 Chassis Hook Locations (SECONDARY SIDE)



12.3.2.2 Class L260 Zone 2 Secondary Side Chassis KOZ

Figure 25: Class L260 Chassis Hook Locations (SECONDARY SIDE)

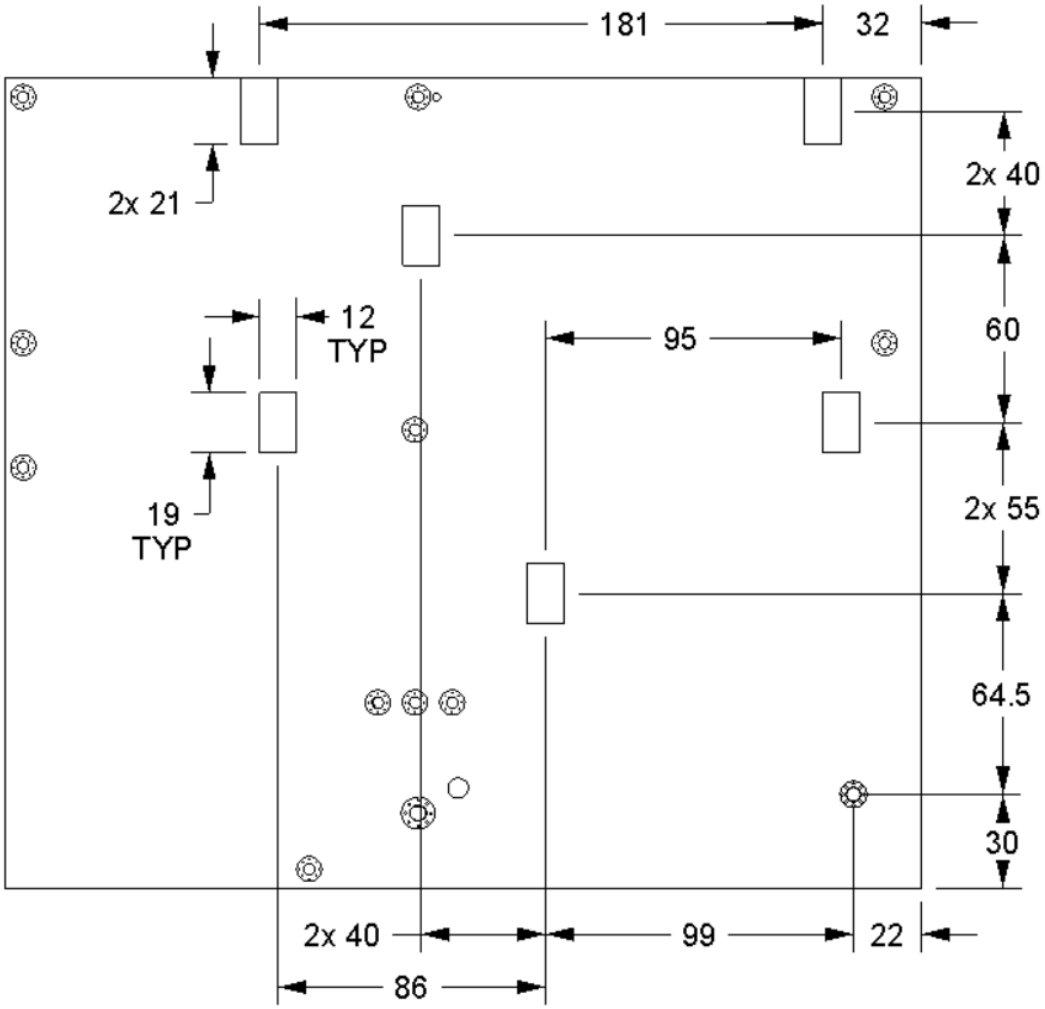
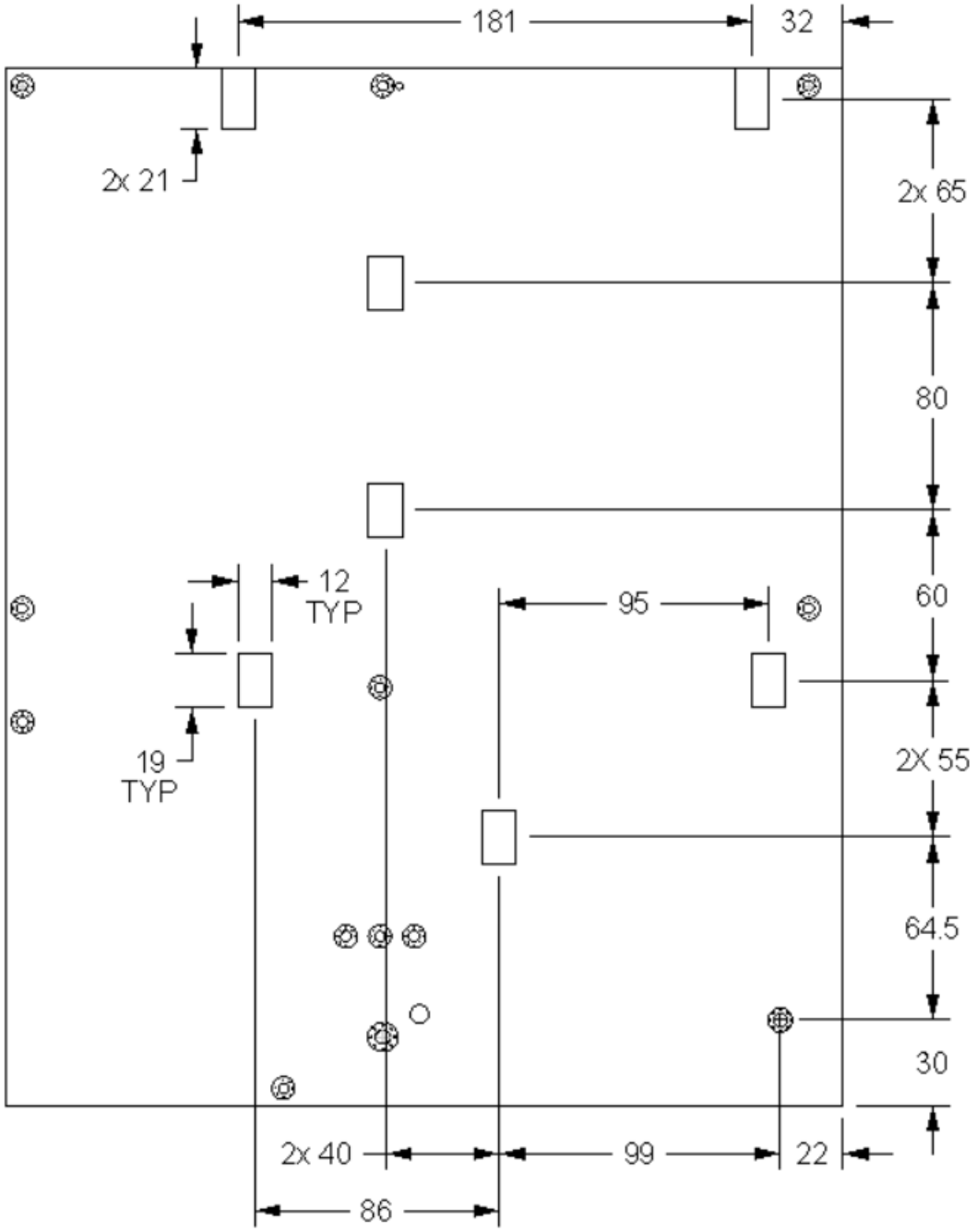


Figure 26: Class L365 Chassis Hook Locations (SECONDARY SIDE)



12.3.3 Zone 3: HPM Secondary Support Requirements

HPMs may require secondary side support under the DIMMS and other semi-supported areas where HPM deflection is likely to occur during normal assembly processes. Two common design approaches to provide this support are:

1. HPMs can identify and provide areas for chassis designs to directly support the HPM PCB surface. These areas need to be clearly identified and free from any conductors or risk of shorting (no exposed vias, traces or components). Chassis designers may choose to support these areas with Board Pan formed features (metal) or bumpers/fillers (rubber or plastic).

2. HPMs can include bumpers or fillers in their design that are tuned in Z height (2.12mm +/- 0.10mm) to match with the Board Pan and exceed the height of all bottom side components.

Figure 27: Example Secondary Side Supports



12.3.4 Zone 4: CPU Backing Plate Requirements

Most server HPM designs need to support CPU backing plates or stiffeners placed under the CPU as part of the CPU Socket design.

The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by:

- Backing Plate allowed Height = 6.2mm – HPM thickness - 0.08mm standoff height tolerance – allowances for other backplate design req's (insulators, deflections, etc)
- See Implementors Note below for examples.

Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and / or HPM sled as shown in **Figure 29: CPU Backing Plate (Zone** 4).

Implementors Note:

HPM and CPU designers should consider these example scenarios supported by DC-MHS HPM board and Backing plate thickness requirements.

Board Thickness (Nominal, mm)	Maximum Allowable CPU Backing Plate Including Allowances (mm)
1.57	4.55
1.93	4.19
2.36	3.76
2.55	3.57
3.18	2.94

12.4 HPM Board and Assembly Thickness

- The maximum allowed thickness and zone heights in the specification assume a maximum 6.2mm board mounting height within a system chassis.
    - Thickness and zone heights are established to ensure forward compatibility with 1U & 2U System Chassis assumptions.
    - Exceeding the thickness and zone height target values would result in system design impacts and incompatibilities.
    - The board mounting height for a given system is not within scope of the HPM specification and is at the discretion of the System designer.
- The maximum allowed HPM thickness shall be 3.18mm nominal and assumes +/-10% tolerance is allowed.
    - Note that PCB Tolerances of +/- 10% are supported but are not a factor in determining the fit of the CPU Backing Plate when the HPMs are mounted to standoffs by their bottom surfaces.

Implementors Note:

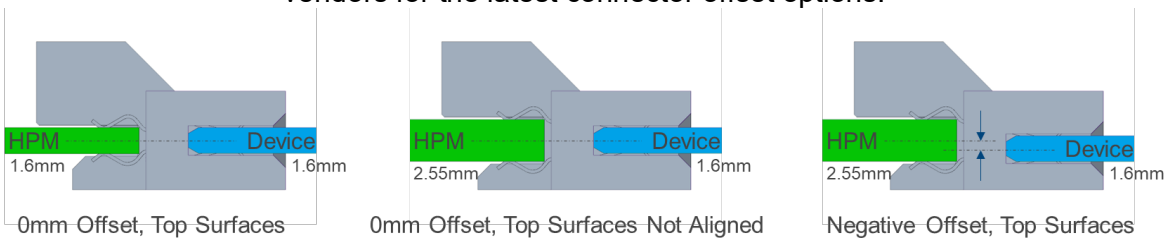
Offset connector choices and requirements may vary when a common chassis design supports multiple HPM thicknesses. For the AI Native Edge-MHS specification, this could include but is not limited to connectors for OCP NIC 3.0 designed to be used in a coplanar fashion to the HPM.

Failure to select the appropriate offset may result in peripheral cards not aligning with the chassis opening, as illustrated in the figure below.

There is no recommendation for connector offset for MHS compliance. Connector offset is out of scope of AI Native Edge-MHS HPM specifications.

Connector offset is a BOM (bill of material) choice by the system / HPM designers.

Refer to the latest OCP NIC 3.0 and DC-SCM R2.x specifications for a list of connector choices available at the time those specifications were published. Refer to connector vendors for the latest connector offset options.



0mm Offset, Top Surfaces and Centerlines Aligned

0mm Offset, Top Surfaces Not Aligned but Centerlines are Aligned

Negative Offset, Top Surfaces and Centerlines Not Aligned

Implementors Note:

HPM and Chassis designers should consider the height stack-up of each of the 4 zones identified in **Section 10.3: Secondary Side Zones and Height Restrictions**. **Table 5** and **Figure** 26 **- Figure** 29 demonstrate an example of a compliant stack-up for consideration. Note that the "total Z" value across the 4 zones must always be equivalent (maximum allowed value of 6.2mm shown for example only).

Table 5: Example Z-Height Compliant Stack-Up, Per Zone

		Zone 1	Zone 2	Zone 3	Zone 4	
Item	Description	Z Value (mm)	Z Value (mm)	Z Value (mm)	Z Value (mm)	Notes
A	HPM	3.18	3.18	3.18	3.18	MAX Thickness (w/o Added tolerance, Assumes bottom mounting)
B	Bottom Component Z	1.60	0			MAX Height
C	CPU Backing Plate				2.94	MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray
D	HPM Bottom Support			2.12		HPM Support Thickness +/- 0.10mm, must exceed Bottom Component Z
E(1)	Resultant Gap	0.62	0.58			Gap is Larger, Requires Insulation and/or Clearance
E(2)	Resultant Gap			0.10	0.08	Gap is Small, Contact between Parts is either Desired or Permissible
F	Board Pan	0.80		0.80		
G	Chassis Hook		2.44			MAX Height from Inside Surface of Chassis
	TOTAL	6.2	6.2	6.2	6.2	Example Solution Stack-up

Figure 28: Secondary Side Components (Zone 1)

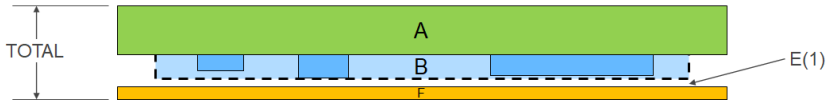


Figure 29: Chassis Hook Keepouts (Zone 2)



Figure 30: HPM Secondary Support (Zone 3)

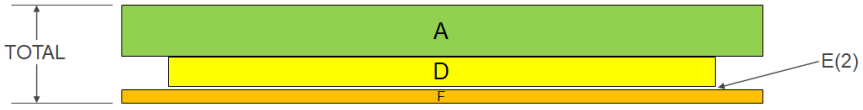
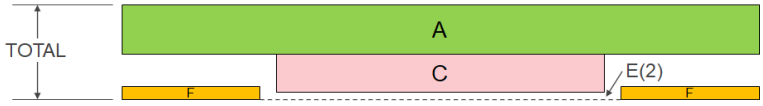


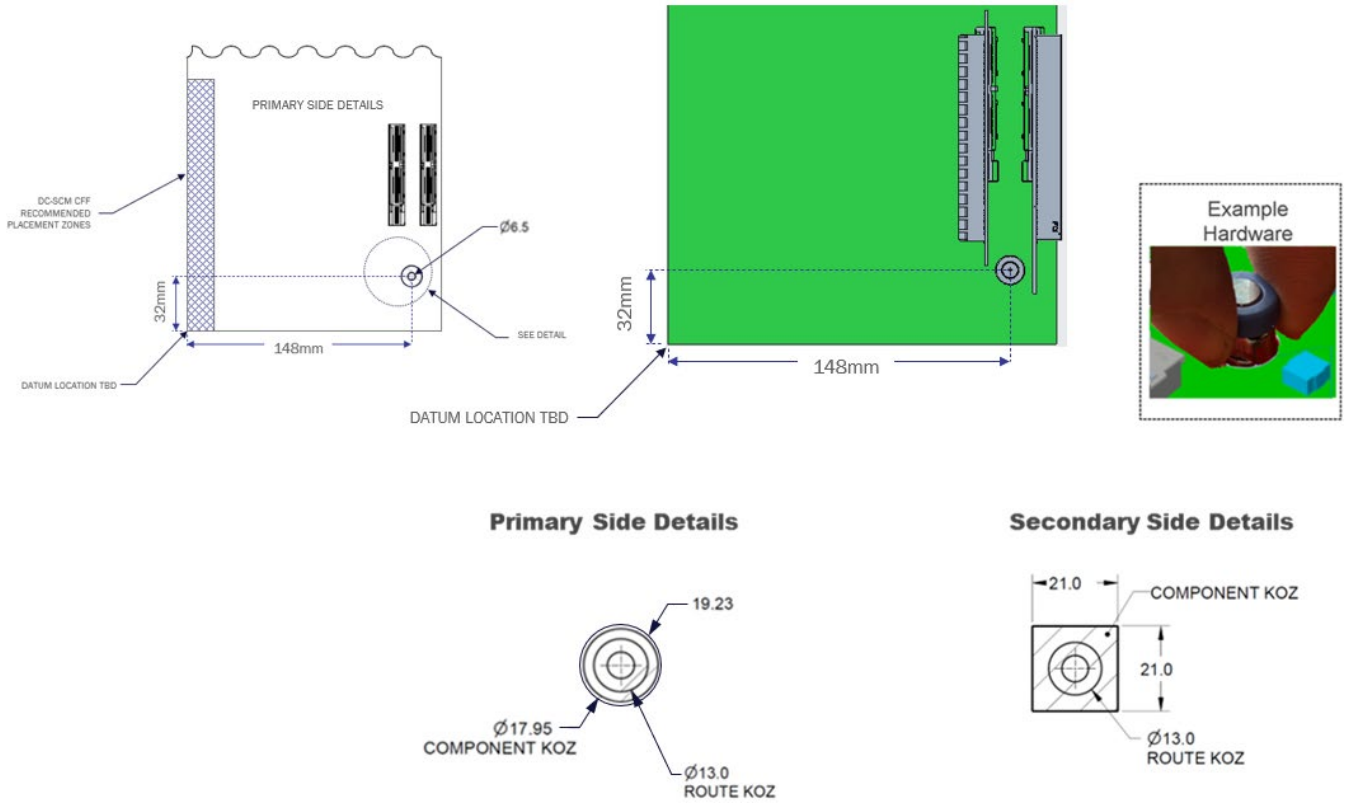
Figure 31: CPU Backing Plate (Zone 4)



12.5 HPM to Chassis Retention Mounting

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required for HPM retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc., hole size required Primary / Secondary side KOZs (and height restrictions around this hole), are defined in **Figure 32.** This definition applies to all HPM classes.

Figure 32: HPM Assembly to Chassis Retention Enablement (Class N Depicted)



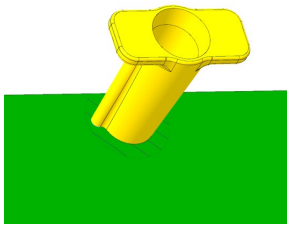
Implementors Note:

Notice a key difference between the DC-MHS S-DNO specifications and the AI Native Edge-MHS specifications is the exclusion of the wide shaped primary side 0.5mm Height Restriction zones to allow a place for finger grip allowances around the retention hardware (which could be a plunger, thumbscrew, wing screw, etc.). It is still suggested that due to hardware and touchpoints being in this area, the goal is to minimize the size of components that could potentially be damaged by fingers coming in close contact to the board surface and/or build a different type of retraction mechanism which is outside the scope of this specification.

12.6 HPM Handle Hole

The HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with, but is not limited to, a plastic handle. An example is shown in **Figure 33**.

Figure 33: Example Board Handling Feature



Implementors Note:

While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

The hole location shall be near the Far side edge of the HPM. HPM Designers may choose to either:

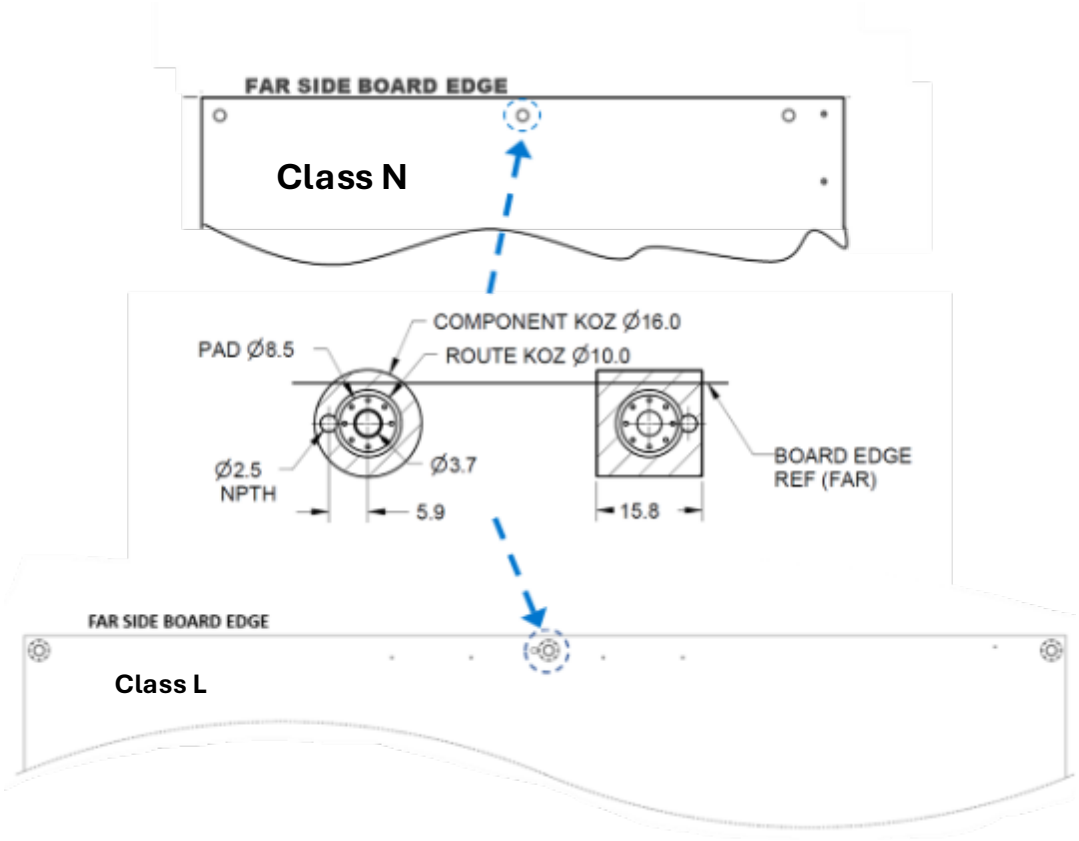
1. Replace a recommended mid-board mounting hole along the Far Side edge with the board handle hole. **Figure 34** demonstrates this approach.

2. Add an additional hole near the Far Side Edge with consideration for Compute Core Details such as cabling for HSIO.

The Board Handle hole may also be considered a mounting hole for structural purposes. For example, a designer does NOT need to place a board mounting hole in close proximity to the Board Handle Hole.

The board handle hole shall follow the required dimensions and KOZ in **Figure 34.**

Figure 34: Geometry and KOZ for HPM Handle Hole and Optional Placement Location



12.7 OCP NIC 3.0 and DC-SCM R2.2 Locations

This specification defines fixed recommended placement for certain peripheral connectors to maximize reuse across designs. These fixed peripheral subsystem connectors are OCP NIC 3.0 and DC-SCM R2.2 CFF. Each of these peripherals leverage connectors defined by SFF-TA-1002, including centerline definitions referenced in the figures of this specification https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/

12.7.1 OCP NIC and DC-SCM

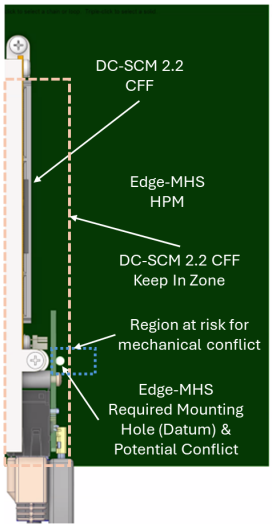
It is recommended that the DC-SCM R2.2 CFF module and connector placement be implemented within the DC-SCM R2.2 CFF Recommended Zones defined in **Figure 37** and **Figure 38.** The HPM shall implement a battery backed voltage interface per DC-SCM R2.2 "Battery Voltage" requirement.

The OCP NIC 3.0 connector is only recommended for use on the Class L designs, if

Implementors Note:

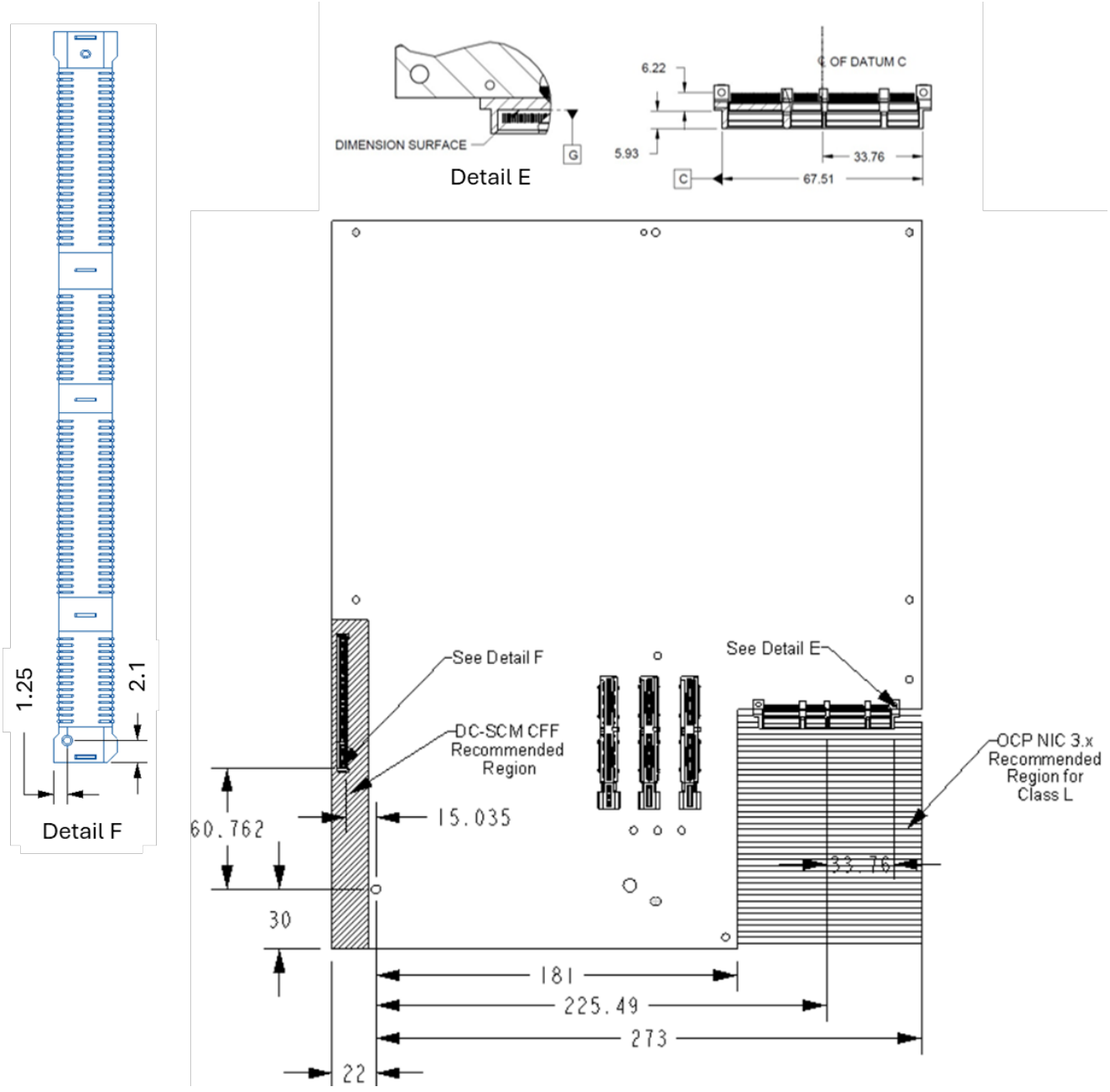
If CFF DC-SCMs utilize heat sinks or daughter/mezz cards, the implementor should be aware of the location of relevant mounting holes in some AI Native Edge-MHS Form Factors. A screw or some other retention device that utilizes the impacted mounting hole could interfere with the CFF's DC-SCM Keep-In-Volume (KIV) dimensions. This is due to the vertical height of that a screw, or some other retention method may require.

The image below illustrates where a mounting hole resides and the potential interference on a hypothetical edge design. Care must be taken to avoid this conflict.



implemented, it shall be placed as defined in **Figure 35.**

Figure 35: OCP NIC 3.x and DC-SCM R2.2 (PRIMARY SIDE)



12.8 Platform Infrastructure Connector Placement (non-power)

12.8.1 Connector Requirements

The electrical implementation for each connector shall follow the M-PIC specification.

Internal USB

- **M-PIC Section Reference:** “Internal USB4 Connector”

- **Connector Requirement:** Recommended
- **Connector Placement:** Fixed location not required.
- **Connector:** Type A or C USB Compliant. It is strongly recommended that HPMs implement a Type A connector.

Intrusion Switch

- **M-PIC Section Reference:** "Intrusion Switch"
- **Connector Requirement:** Shall be Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification

Boot Storage

- **M-PIC Section Reference:** "Boot Storage"
- **Connector Requirement:** Recommended
- **Connector Placement:** Fixed location not required.
- **Connector:** Refer to M-PIC Specification

Due to HPM layout density Cable Optimized connector locations may be more considered in Class N designs. Class L HPMs may choose to utilize the Near Side I/O region to enable the Direct Attach Boot Storage option.

Control Panel

- **M-PIC Section Reference:** "Control Panel Interfacing"
- **Connector Requirement:** Shall Be Required (may de-pop)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed
- **Connector:** Refer to M-PIC Specification

PDB Management Connector

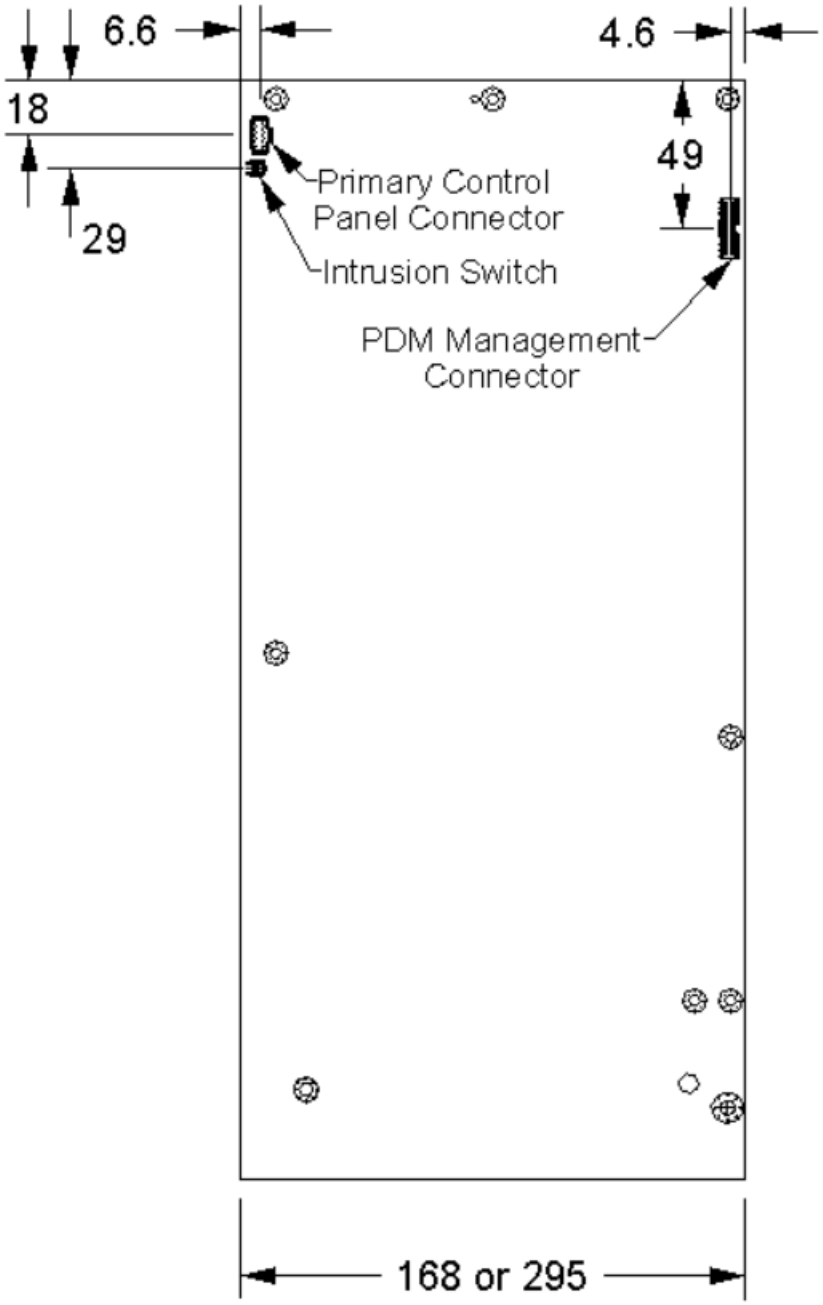
- **M-PIC Section Reference:** "PDB Management Connector"
- **Connector Requirement:** Shall Be Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification

12.8.2 Class N and Class L M-PIC Connector Locations (non-power)

Figure 36 depicts the recommended location of the miscellaneous connectors defined in the M-PIC specification which are relevant to AI Native Edge-MHS HPMs Class N and Class L. Additional information on these connectors is available in **Section 12.8.1.**

These dimensions are intended to provide recommended connector locations that are consistent relative to the closest board corner across all Class N HPMs.

Figure 36: Class N-L Platform Infrastructure Connector Recommended Placements



To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 37** and **Figure 38** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone.

Figure 37: Class N Intrusion, Control Panel, and PDB Management Placement Zones

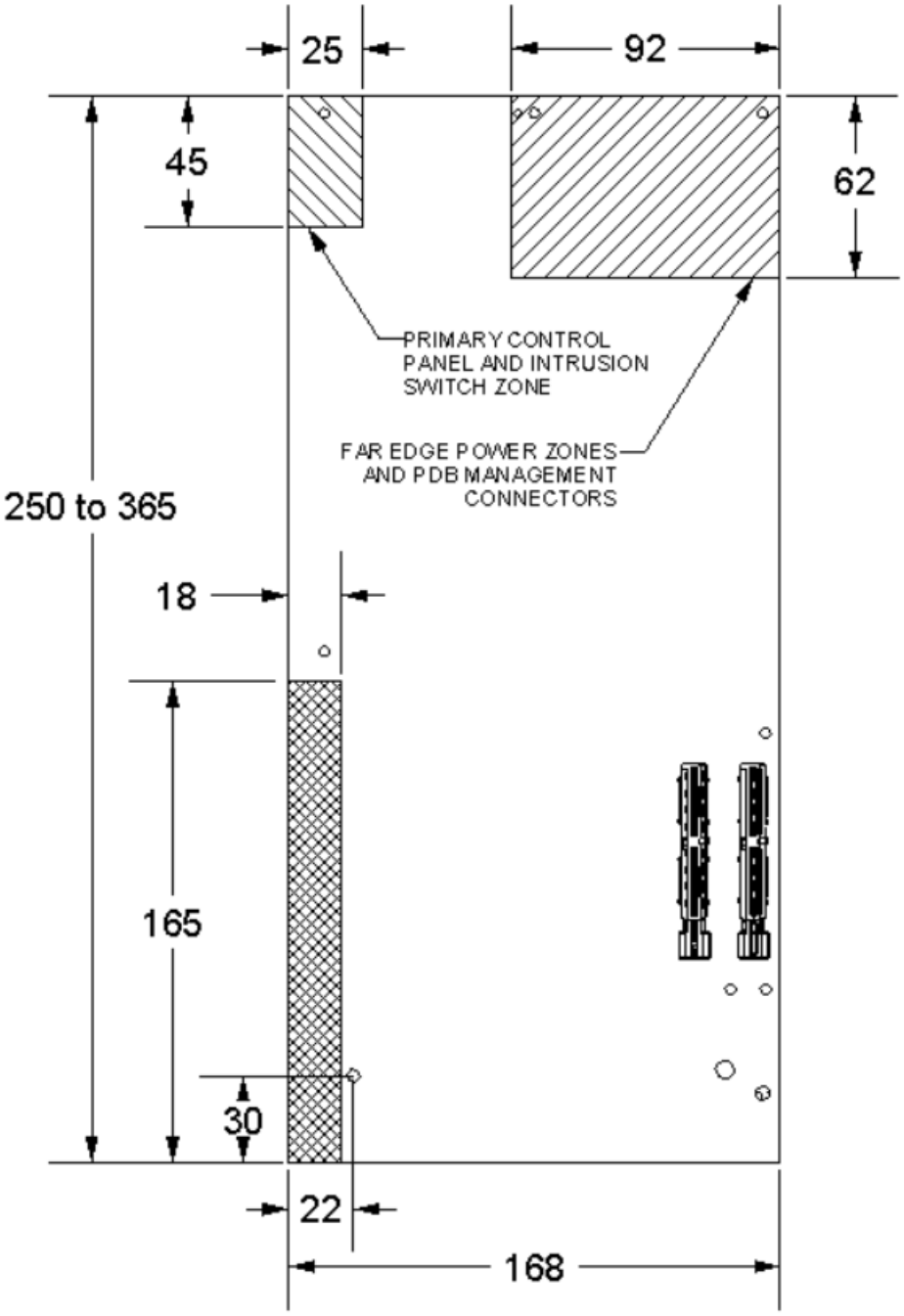
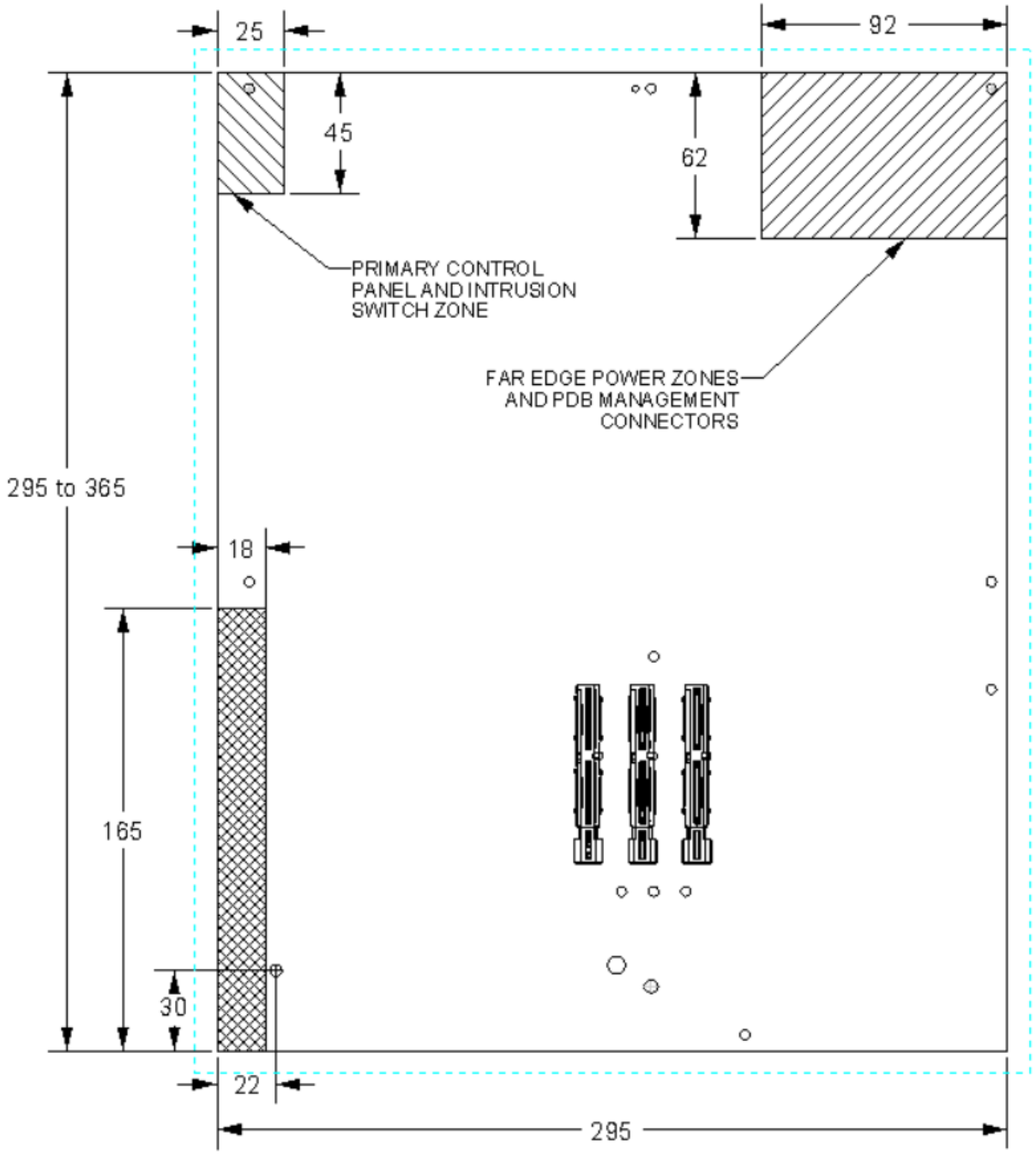


Figure 38: Class L Intrusion, Control Panel, and PDB Management Placement Zones



12.9 High-speed I/O (HSIO) Connectors

This base specification seeks to allow for flexible high-speed I/O (HSIO) routing options while also enabling HPM to system compatibility.

Board-to-board (B2B) connections are defined as connections that mate two separate PCBs without cabling. B2B connections are typically used to route HSIO from the HPM to a riser PCB or direct dock peripherals (i.e. DC-SCM R2.x, OCP NIC 3.0).

Board-to-Cable (B2C) connections are defined as connections that mate two separate PCBs entirely with cabling. B2C connections are typically used to route HSIO from the HPM to a riser PCB or to other subsystems such as NVMe storage devices or backplanes.

Hybrid connections are defined as those which utilize both B2B and B2C elements to create a single mated interface between two PCBs. For example, if a Riser has a PCB with card edge fingers utilizing B2B to receive Power and Low Speed IO while also using a Twinax B2C connection for HSIO.

Implementors Note:

SFF-TA-1033 is an example of a connector supporting Hybrid connections, it can be used for B2B, B2C or Hybrid connections. While the HPM designer places the SFF-TA-1033, they do not necessarily know beforehand what style of connection the System designer will implement.

B2C

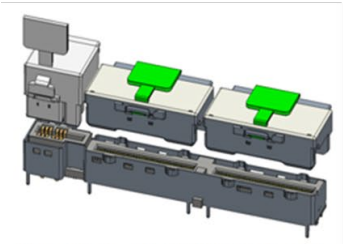


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

B2B



Figure 4-1 Combo x16+21A Power AIC Application

Hybrid

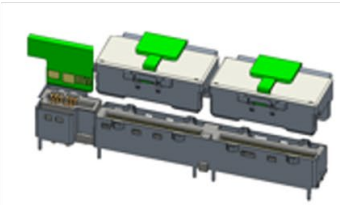


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

12.9.1 DC-MHS Compliant HSIO Connectors

All HSIO connectors shall be compliant with the M-XIO specification and be listed in **Table 6**.

Table 6: AI Native Edge-MHS Specification Compliant HSIO Connectors

Use	Compliant Connectors
Near Side Fixed Risers Locations	SFF-TA-1033 (with 21A Power)
All Other HSIO	SFF-TA-1016 SFF-TA-1026 SFF-TA-1033

Note: Additional connectors may be added to future revisions of this specification *after* electrical definition by M-XIO.

AI Native Edge-MHS HPMs allow for B3B, B3C or Hybrid risers. For best compatibility with many AI Native Edge-MHS system designs, HPMs should implement riser connectors adhering to the guidance in **Section 12.9.22**.

All other HSIO connectors adhere to common guidance in **Section 12.9.3**.

Implementors Note:

HSIO cable choices are outside the scope of AI Native Edge-MHS specification. The SFF-TA-1016 and SFF-TA-1033 connectors can accept both cable types but mixing cable/connector types may result in loss of the anti-tilt feature.

12.9.2 Near Side Fixed Riser Connectors

An AI Native Edge-MHS riser may utilize B2B, B2C or Hybrid connectivity schemes. Riser and other endpoint device definition are outside of the scope of this specification.

To enable chassis and I/O subsystem compatibility and reuse, fixed riser locations are defined:

- AI Native Edge-MHS HPM Class N supports two riser locations.
- AI Native Edge-MHS HPM Class L supports three riser locations.

Note that Riser 4 is only available on Class L HPM's. Refer to **Section 11: HPM Concepts and Layouts** for more information.

HPMs which implement near side fixed risers shall:

- Use a Fixed Riser connector defined in **Section 12.9.1**
- Place them in the location(s) defined in **Section 12.9.2.1**
- Full population of all Near Side Fixed Risers Locations is not required, as there may be technical or other reasons to exclude certain positions. It is recommended to implement as many fixed riser locations as possible.

12.9.2.1 SFF-TA-1033 Fixed Riser Implementation Details

SFF-TA-1033 fixed riser connectors shall be placed in locations defined by **Figure 39 and**

Implementors Note:

For maximum ecosystem compatibility, designing an HPM to utilize as many Fixed Riser locations as possible is strongly encouraged. Utilizing these connectors in a fixed location allows System Designers to use B2B, B2C or Hybrid connections as best suits their use case. In the figure below, all four Class N layouts are AI Native Edge-MHS compliant, however, layout '1" is recommended because it implements all defined Fixed Riser connectors.

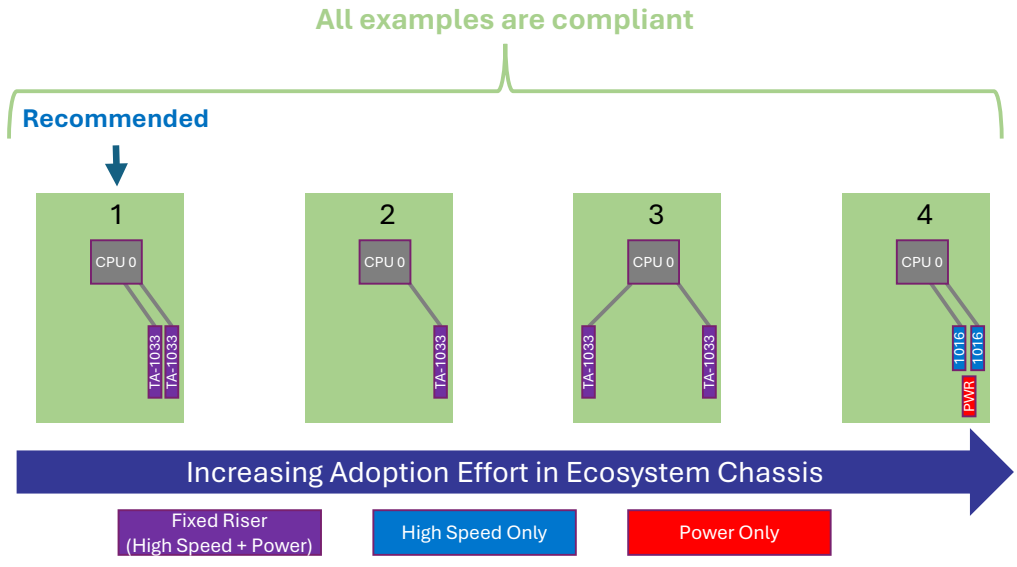


Figure 40, define the required location of the SFF-TA-1033 connectors. This is noted in #30 of the Compliance Table.

Note that SFF-TA-1033 has various versions. All SFF-TA-1033 Near Side Fixed riser connectors shall use a 21A power block version.

Figure 39: Class N Required Riser Locations with Recommended Connector

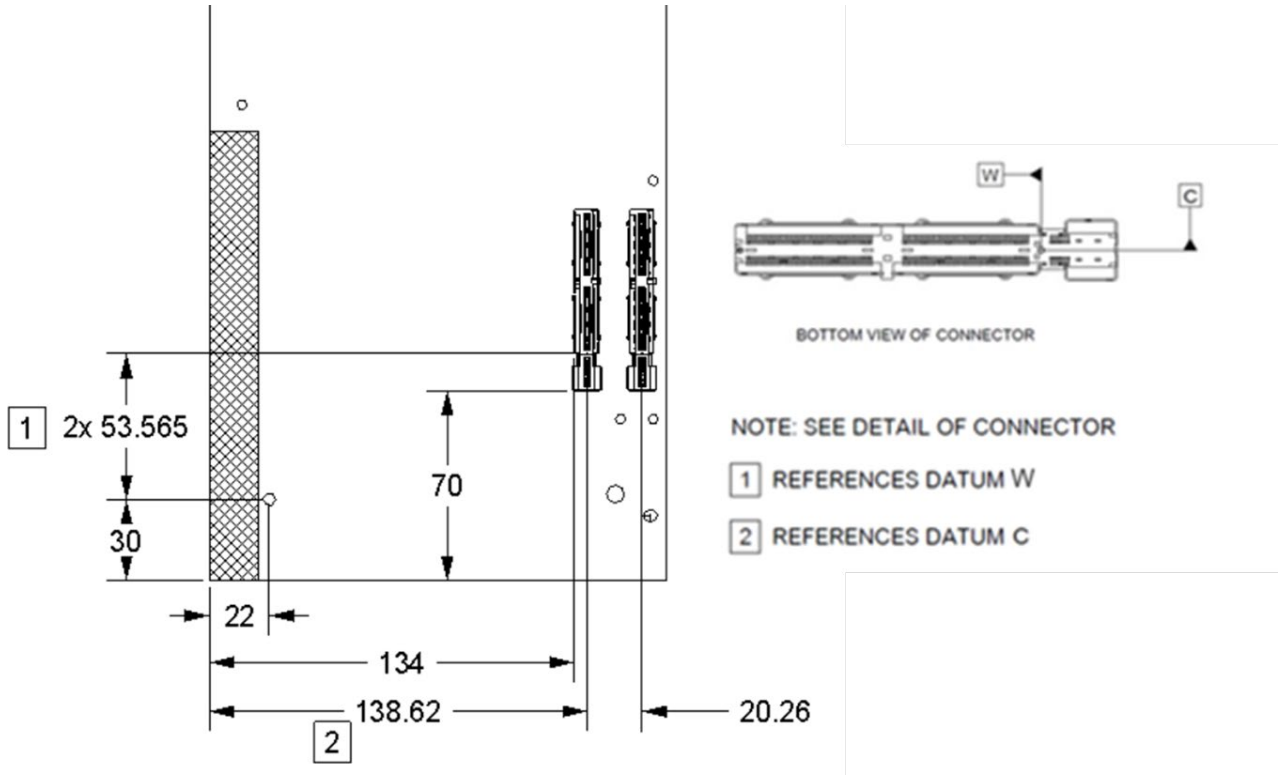
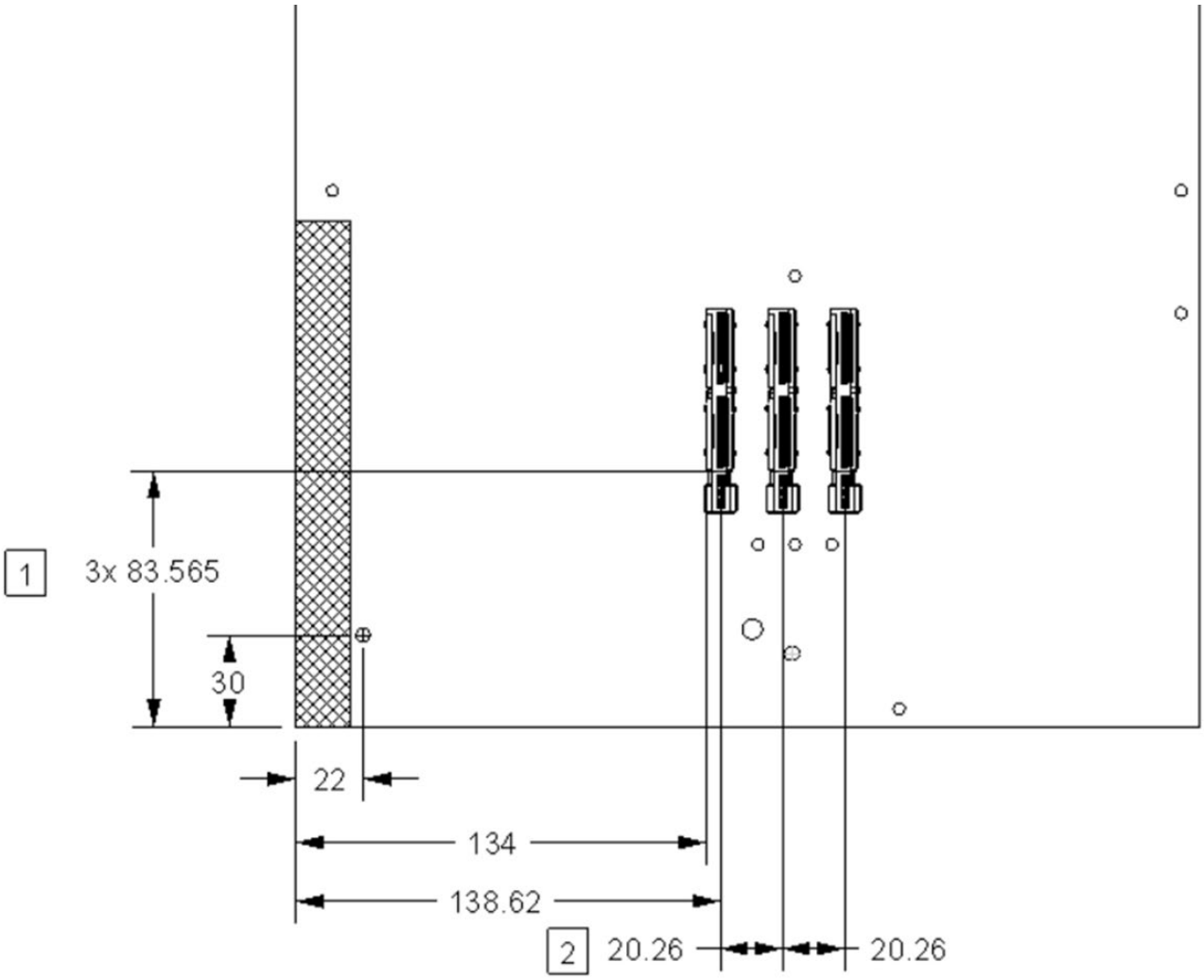


Figure 40: Class L Required Riser Locations with Recommended Connector



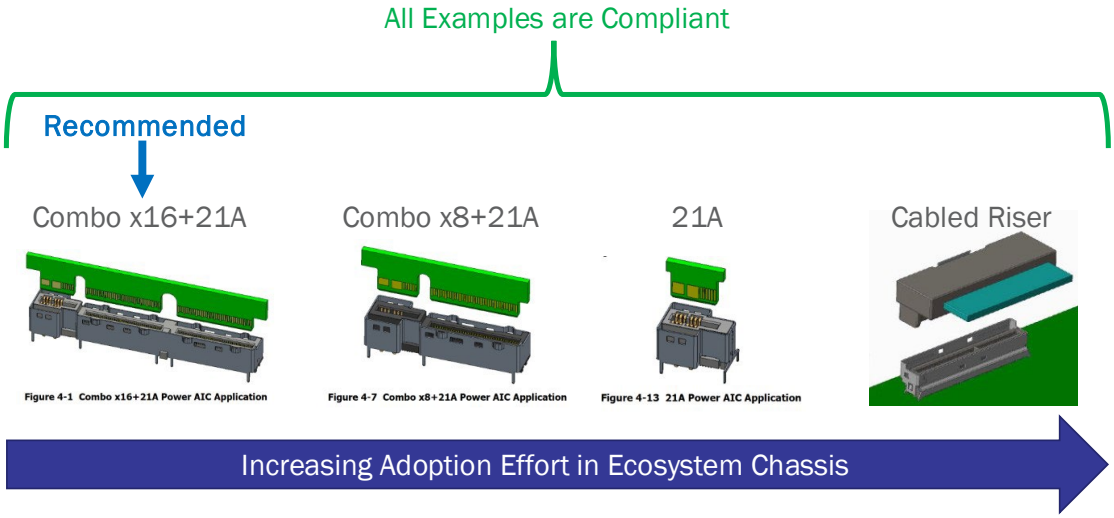
NOTES:
1. VERTICAL DIMENSION TO SFF TA-1033 DATUM W.
2. HORIZONTAL DIMENSIONS TO SFF TA-1033 DATUM C.

Implementors Note:

Use of the Combo x16+21A connector, wired as a x16, is highly recommended for ecosystem compatibility. If HPMs are unable to support the maximum number of Fixed Riser connectors, it is recommended that the HPM designer consider reduced ecosystem compatibility in the following order:

1) Use the SFF-TA-1033 Combo x16+21A, wired as a x8 in compliance with M-XIO
2) Change the SFF-TA-1033 Combo x16+21A to the SFF-TA-1033 Combo x8+21A
3) Change the SFF-TA-1033 Combo x16+21A to the 21A Power only
4) Change to a B2C Riser with connectors adhering to **Section 11.9.3**

SFF-TA-1033 Fixed Riser Connector Options



12.9.3 Other HSIO Connectors

Except for the Fixed Riser Connectors described in **Section 12.9.2**, HSIO connector positions and quantity are not defined by this AI Native Edge-MHS base specification. The HPM Designer is free to place them wherever they wish so long as they do not interfere with other required features (e.g. a required mounting hole) and while adhering to the component height restrictions in **Section 12.10**.

All implemented HSIO connectors shall be defined in M-XIO and listed in **Table 6.** Any combination of these connectors is allowed.

12.10 Primary Side Component Height Restrictions and KOZs

All AI Native Edge-MHS Classes shall adhere to a common approach of three different component height restriction zones as shown in **Figure 41 and Figure 42**

- The **12mm Zone** is intended to allow for extended heatsinks and other thermal solutions while not prohibiting cabling of HSIO. Adherence to the 12mm zone is strongly recommended. While deviations are allowed, HPM designers should limit component selections which exceed the restriction to reduce interference with system design elements which will expect to inhabit this space and may cause system compatibility issues.
- The **11.3mm Zone** is intended to avoid interference with PCIe CEM cards directly above the HPM and its peripherals. Adherence to the 11.3mm Zone shall be required when PCI CEM cards are implemented directly above the HPM and its peripherals (adherence to this requirement is not mandatory if PCIe CEM cards directly above the HPM are not being implemented). Note that the DC-SCM CFF is exempt from this restriction.
  If the HPM design has the compute complex positioned towards the near area such that PCIe cards could not be supported, the 11.3mm zone can be disregarded.
- The **6mm Zone** is the most restrictive and is intended to prevent interference with mechanical elements in support of the fixed riser locations and retention holes. Adherence to the 6mm Zone shall be required when PCIe risers are implemented.

Zone height restrictions apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of soldered components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

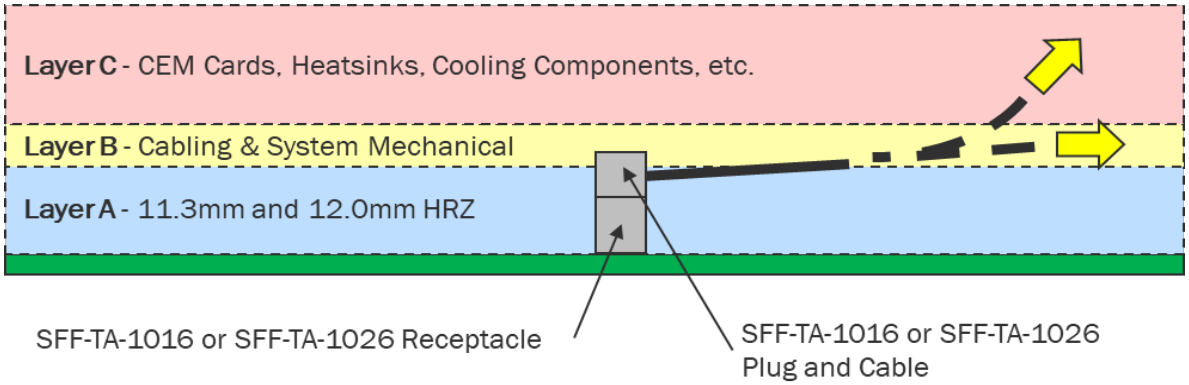
Allowed exceptions to these zones are:

- DIMM connectors
- Connectors in specified Fixed Riser locations (**Section 12.9.2**)
- Plugs to connectors placed by this specification (e.g. vertical PICPWR or USB plugs).
- Connectors listed in **Table 6: AI Native Edge-MHS Specification Compliant** HSIO Connectors may be placed in the 11.3mm and 12.0mm Component Height Restriction Zones. The mating plugs for these connectors may exceed the HRZ depending on which connectors and plug types are chosen. As a result, an exception is allowed for these two connector types in the 11.3mm and 12.0mm HRZs. HPM designers should place these connectors with careful consideration of potential system use cases for their HPM.

This specification does not specify a specific Keep Out Zone for cable enablement.

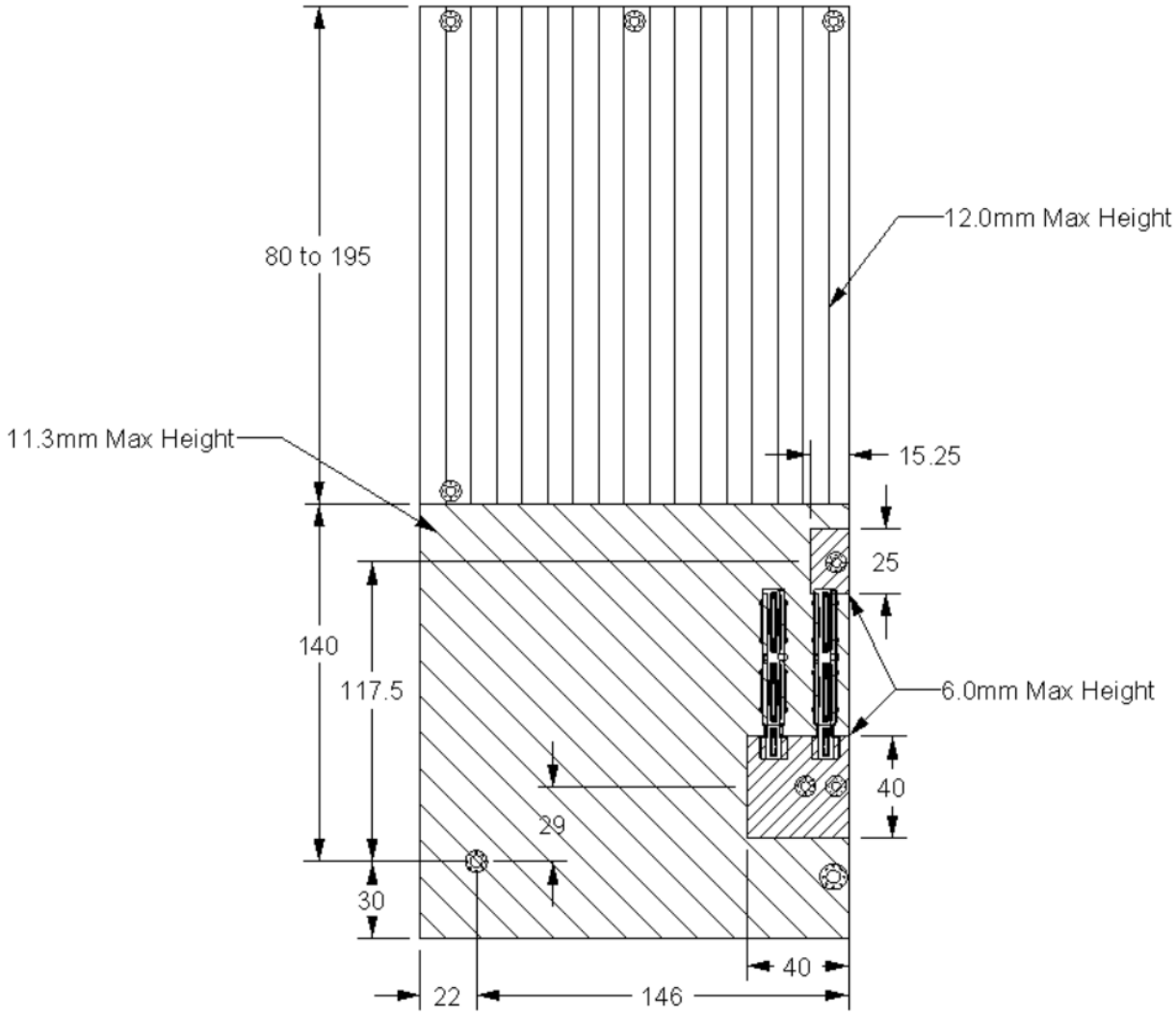
Implementors Note:

A height exception may be needed for the SFF-TA-1016 & SFF-TA-1026 connector + cable plug based on an understanding that a system design layer exists between the HPM HRZs (Layer A) and the Major Component Layer of a system (Layer C). Layer B is a mechanical design layer where cabling may route and sheet metal structures may be created in the system's chassis design. A system designer needs to understand the mated heights of plug + receptacle for the SFF-TA-1016 and SFF-TA-1026 connectors to be able to accommodate their occasional and purposeful intrusions into Layer B.



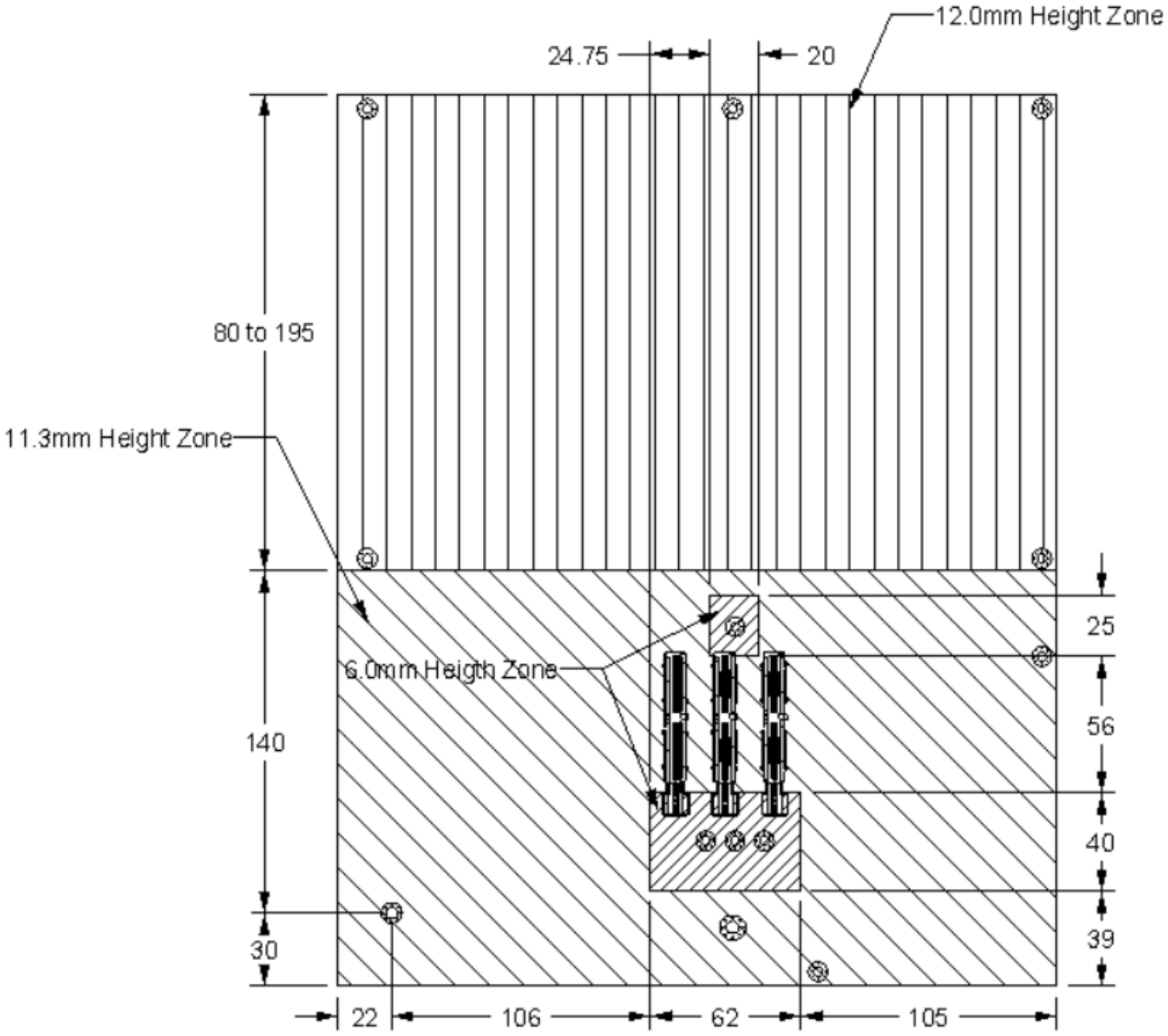
12.10.1 Class N HPM Primary Side Component Height Restrictions

Figure 41: Class N Component Height Restriction Zones (PRIMARY SIDE)



12.10.1 Class L HPM Primary Side Component Height Restrictions

Figure 42: Class L Component Height Restriction Zones (PRIMARY SIDE)



12.11 Platform Custom Zone

The AI Native Edge-MHS specification does not formally contain a Platform Custom Zone, but with that stated, to maintain as much compatibility as possible with other MHS specifications it is desired that common connectors be utilized when implementing storage solutions or OCP NIC solutions.

12.11.1 Direct Dock E1.S

An HPM design may want to support direct docking E1.S (SNIA EDSFF) in a potential Platform Custom Zone. These HPM designs should utilize a connector like the SFF-TA-1002, 2C connector. Specific placement and implementation are outside the scope of this specification.

12.12 Class L I/O Region utilizing OCP SFF NIC R3

Class L includes a I/O Region that runs along the near side board edge between the DC-SCM CFF Recommended Placement Zone and the “right” board edge of the PCB as shown in **Section 11.2: Class L HPM** Layout. The specification defines one option considered common use case to promote greater compatibility between future HPMs.

12.12.1 Class L OCP SFF NIC R3

A Class L HPM design may support an OCP NIC 3.0. Please refer to Section 12.7.1 for recommended implementation details.12.7.1

Implementors Note:

The DC-SCM DC-SCI is designed to support up to two RMII/NC-SI RMII-based transport interfaces, facilitating sideband communication between the DC-SCM to the NIC(s).

For DC-SCM applications utilizing a single NC-SI, it is advised to employ the first NC-SI interface instance (utilizing pins B43-B49). If a second NIC, NIC 2, is implemented into the HPM with a single DC-SCM, it is strongly recommended to establish an NC-SI RBT connection to NIC 2, rather than leaving it disconnected. The connection of NC-SI to NIC 2 can be achieved through one of the following methods:

1. A multidrop topology extending from the first NC-SI, or
2. An active MUX/Switch derived from the first NC-SI, or
3. A second NC-SI originating from the DC-SCM (illustration not provided).

The selection of the optimal topology is not covered within this specification; for further guidance, please consult the OCP NIC & DC-SCM Base Specifications. For additional information on NC-SI, refer to DMTF DSP0222.

NOTE: When implementing DC-SCM 2 (illustration not provided), DC-SCM 1 and NIC 1 may share a dedicated NC-SI, while DC-SCM 2 and NIC 2 can utilize a dedicated NC-SI.

12.12.2 OCP NIC 3.0 DSFF

Direct support of an OCP NIC 3.0 DSFF on the HPM is outside the scope of this specification. Cabled DSFF cards may be implemented in upper areas of the server; however, specific implementations are not defined.

13 Power Zones

While alternate voltages are under consideration for future versions (e.g. 48V DC implementations), this version assumes the burden for alternate power sources is placed on the system power delivery infrastructure (PDB, bus bar, etc.). For information on Power Management (including Power Gating and use of sideband signals) refer to the M-PIC specification.

Implementors Note:

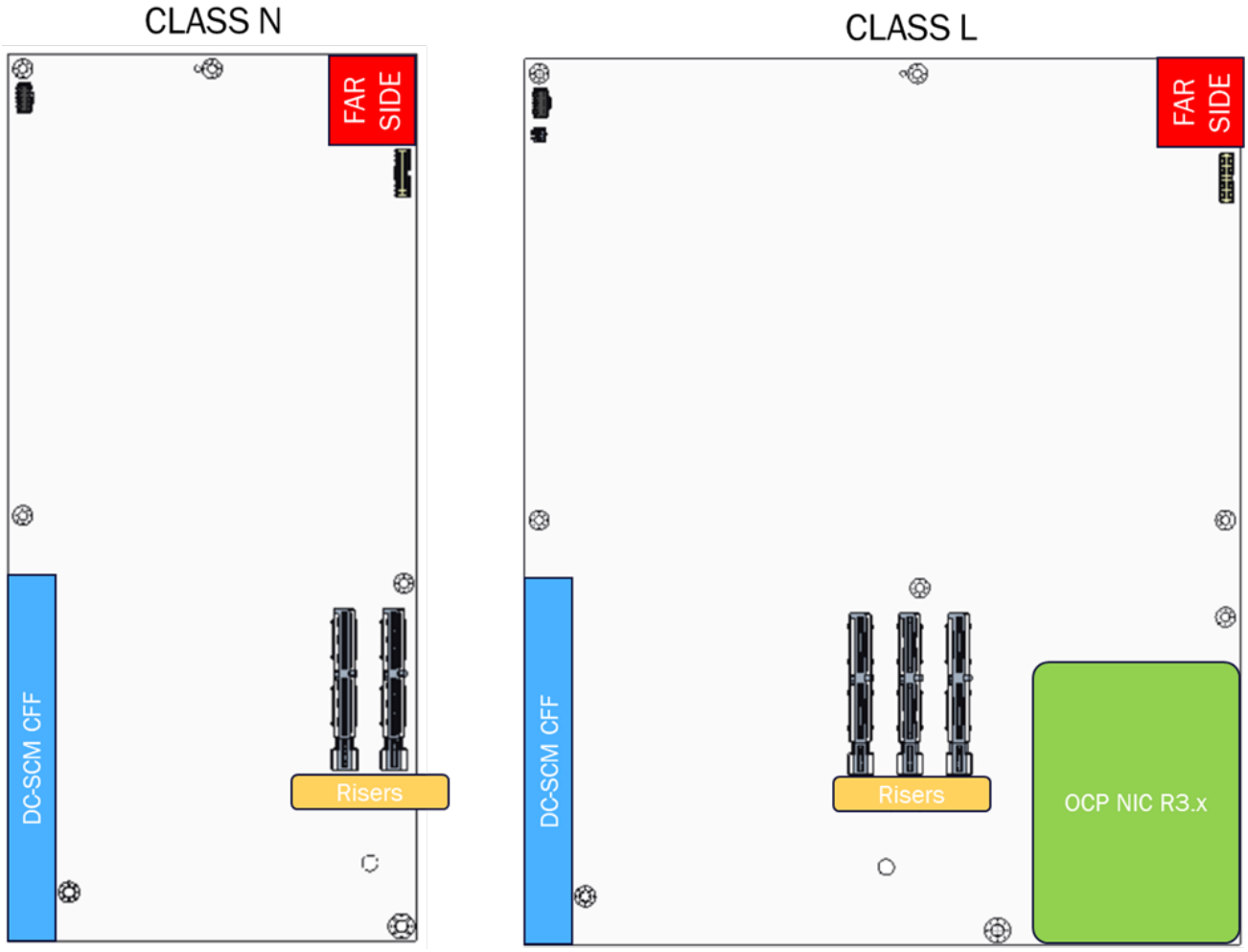
The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in private and/or public HPM design specification(s) for system configurations supported per HPM design.

13.1 HPM Power Zone Overview

To enable a variety of system power configurations (See **16.2 AI Native Edge-MHS Power Zone Usage Examples**) there is a uniquely defined bi-directional power zone for each HPM Class referred to as the “Far” Ingress / Egress zones as shown in **Figure 43**. This zone is intentionally placed on the HPM to optimize around short depth constrained form factors.

Additional power zones may include power egress to DC-SCM, OCP NIC and each fixed Riser location.

Figure 43: AI Native Edge-MHS Power Zone Overview (Class N and L Depicted)



13.2 Far Bi-Directional (Ingress / Egress) Power Zones

13.2.1 Ingress / Egress Cabled Power Connector

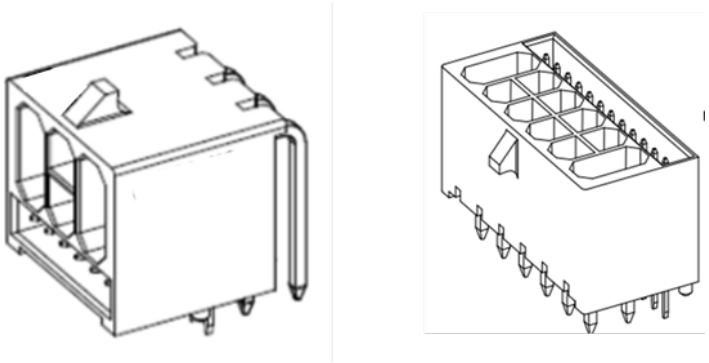
- **Power Connector Type**: 2x6+12SB and/or 2x3+6SB PICPWR
  Refer to M-PIC Specification https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/ for additional details.
- **Connector Power Rating**: 864W (2x6) / 486W (2x3)
- **Typical usage**: Power ingress to HPM and / or egress to peripheral subsystems

It is assumed that most systems will provide power to AI Native Edge-MHS based HPMs via a cabled solution from a Power Distribution Board (PDB).

To maximize reuse of power delivery across all AI Native Edge-MHS HPMs, the required connectors for all cabled Ingress / Egress power shall be the 2x6+12SB or 2x3+6SB PICPWR. An example of the 2x3+6 and 2x6+12SB is depicted in **Figure 44**.

Refer to the M-PIC specification for more information on PICPWR compliant connectors.

Figure 44: Example 2x3 + 6SB (Right Angle) and 2x6 + 12SB PICPWR Connector (Vertical)



Implementors Note:

HPMs which implement the cabled PICPWR connectors may still be used in multi-node systems via an interposer or interface board to enable blind mate into system backplane / infrastructure. Refer to **Section 15.1 AI Native Edge-MHS Conceptual Implementation Examples** for an example of such a system.

13.2.2 Power Requirements (All Classes)

13.2.2.1 Common Far Power Zone Requirements

Each HPM Class defines a Far side Zone where PICPWR connectors shall be placed. In addition, recommended placements are provided within the Zone for each HPM Class.

The far power zone shall include the body of at least 1 2x6+12SB PICPWR connector, additionally, enough connectors shall be placed within the zone such that the far power zone is capable of meeting the full HPM power budget when used for ingress.

2x3+6SB may also be used within the far power zone.

There are no additional Class specific requirements for the Far Power Zone.

13.2.2.2 Near Side Power Zone Considerations

There are no Near Side Power Zone's specified in the AI Native Edge-MHS specification due to the density of the solution presenting space limitations in providing a unified location. Near side power may be implemented and if implemented it is recommended that the common M-PIC connectors utilized in the M-SDNO specifications be utilized.

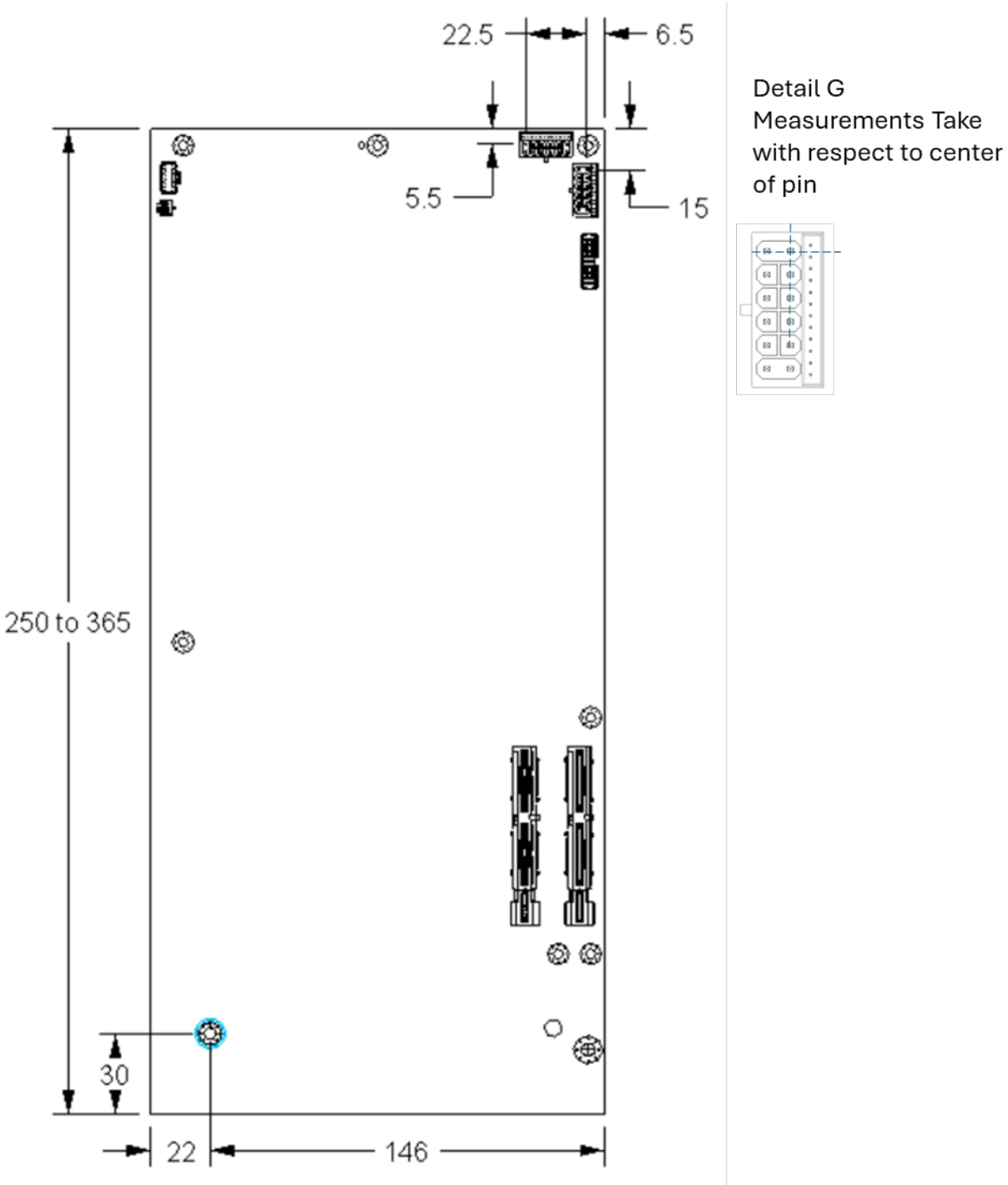
2x6+12 and 2x3+6SB may be used if implementing Near Side Power.

13.2.3 Class N Ingress / Egress Power Connector Locations

13.2.3.1 Near Side Power Zone– Class N Specific

The Near Side Power Zone is not defined for Class N HPMs.

Figure 45: Class N HPM Far Power Zone Recommended Connector Locations (PRIMARY SIDE)



13.2.4 Class L Ingress / Egress Power Connector Locations

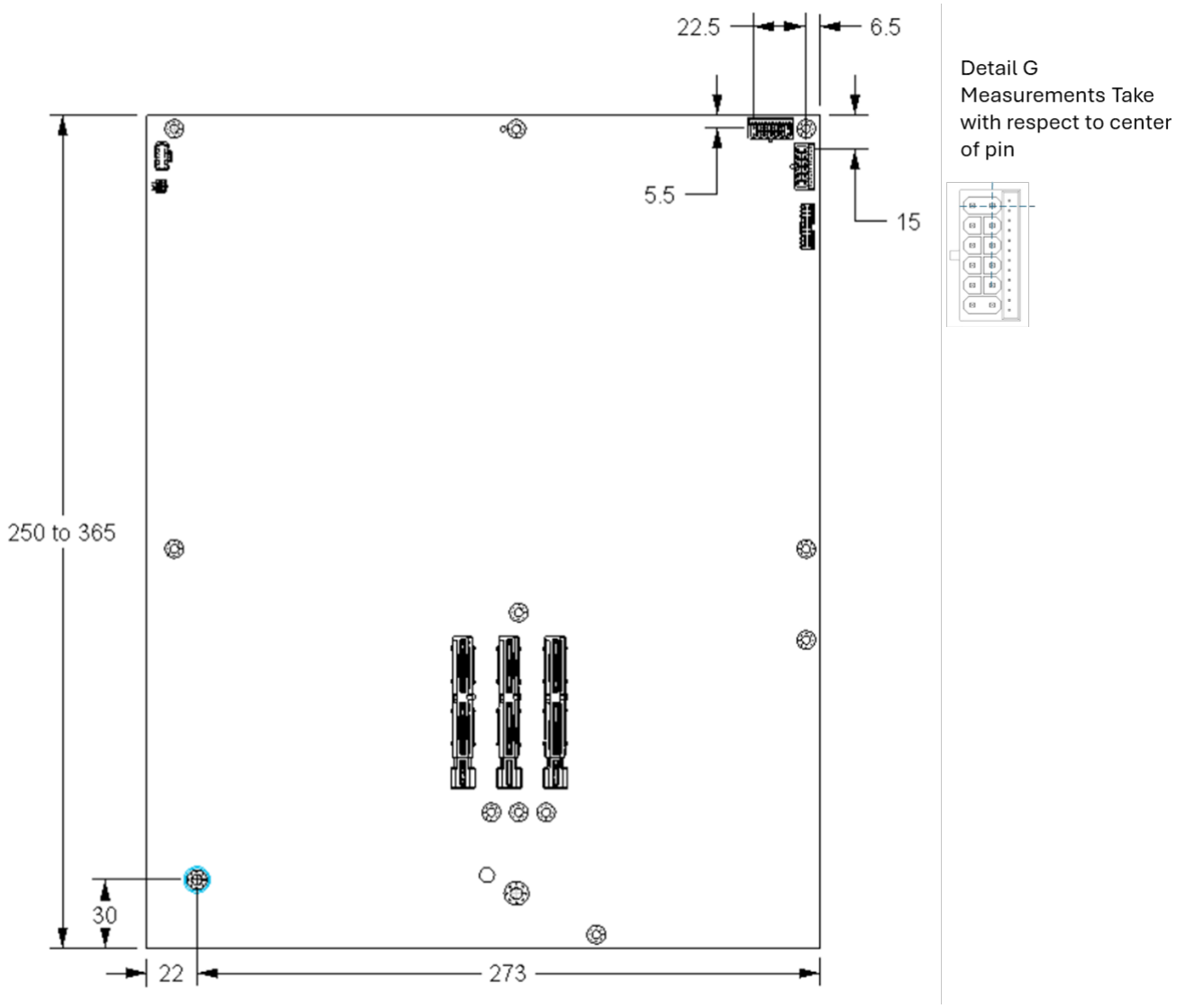
13.2.4.1 Near Side Power Zone– Class L Specific

The Near Side Power Zone is not defined for Class L HPMs.

13.2.4.2 Far Side Power Zone– Class L Specific

Figure 46 depicts two recommended positions for PICPWR connectors in the Class L Far Side Zone. It is recommended that HPMs implement Position 1 and Position 2 if the solution requires additional power. HPMs which require additional power capability (i.e. to support near side egress power) may choose to implement all additional PICPWR connectors.

Figure 46: Class L HPM Far Power Zone Connector Recommended Locations (PRIMARY SIDE)



13.3 Fixed I/O Riser Power

- **Power Connector Type**: Integrated within SFF-TA-1033 Recommended

Refer to M-PIC Specification https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/ for additional details.

- **Connector Power Rating**: 252W
- **Minimum Power Delivered to Connector by HPM**: 87W
- **Typical usage**: Power egress for 1 (required) or more (optional) 75W PCIe CEM Devices per Riser

For each implemented fixed riser location, as specified in **Section 12.9.2**:

- HPMs shall deliver a minimum of 87W of power to the riser connector (See **Table 7** for calculation of 87W effective total power required *per riser*). This requirement is defined to guarantee each riser location can support a minimum of one 75W PCIe CEM card and reduce power cabling requirements in dense systems.
- HPMs may deliver additional power to the riser connector to enable additional cards at each riser location.
- Additional supplemental I/O power (e.g. auxiliary power for a GPU) is not defined and is assumed to be provided directly by system infrastructure (e.g. cable from PDB).
- Riser connector shall comply with M-PIC PICPWR sideband signaling requirements.

Table 7: Minimum HPM Power Provided to Fixed Riser Locations

Power Rail	75 W Slot
+3.3Vaux	Generated on PCIe riser. Derived from +12V
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from +12V
+12V Voltage Current	12V nominal 7.25A total: 5.5 A (Aligned to CEM Specification) + 1.0A (VR conversion to V_{cc3_3}) + 0.35A (VR conversion to +3.3Vaux) + 0.40A (misc.)

13.4 DC-SCM CFF Power

AI Native Edge-MHS HPMs shall provide power to the DC-SCM CFF connector when implemented as defined in the OCP DC-SCM R3.2 spec (Refer to **Section 15**). As the power requirements of DC-SCM peripherals will vary, HPM designers are encouraged to support as close to the specification defined maximum power as possible to optimize ecosystem compatibility.

13.5 OCP NIC 3.0 Power

When implemented, AI Native Edge-MHS HPMs shall provide power to OCP NIC 3.0 connector(s) as defined in the OCP NIC 3.0 specification (Refer to **Section 15**). As the power requirements of NIC peripherals will vary, HPM designers are encouraged to support as close to the specification defined maximum power as possible to optimize ecosystem compatibility.

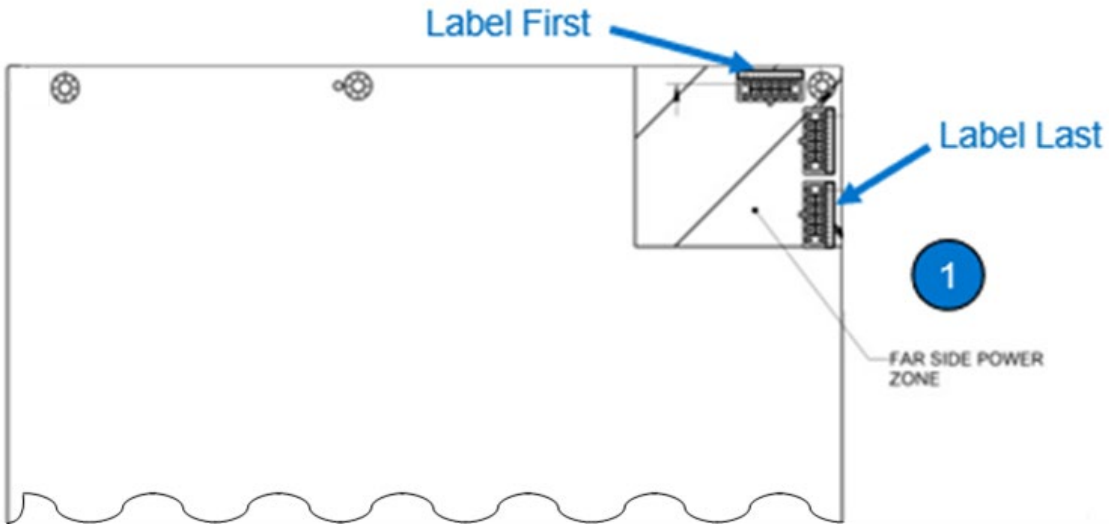
13.6 PICPWR Labeling Order

It is recommended to label PICPWR connectors in the following order, as shown in **Figure 47**.

1. Label PICPWR connectors in the Far power zone based on PICPWR Connector 1 See "Label First" below in **Figure 47** location beginning at the Far Side board edge and moving towards the Near Side board edge. When multiple connectors are aligned horizontally, label connectors from left to right.

For specific details on how to label each PICPWR connector, refer to the M-PIC specification.

Figure 47: Recommended PICPWR labeling order



14 I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces that shall be in compliance with the AI Native Edge-MHS family of specifications. Refer to **Section 8** for additional details, specifically M-PIC, M-XIO, M-CRPS, and M-PESTI specifications.

For information on connector placements, refer to **Section 12.8: Platform Infrastructure Connector Placement (non-power)** and **Section 12.9: High-speed I/O (HSIO) Connectors**.

15 References

Relevant Open Compute Specifications

This specification also relies on the following Open Compute Project specifications

1. OCP Server Network Interface Card (NIC) R3 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
   Mezz (NIC) » Open Compute Project

2. OCP Datacenter Secure Control Module (DC-SCM) R2.2 – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
   Hardware Management/Hardware Management Module - OpenCompute

3. OCP Open Rack V3 – Class N opportunistically allows 3 HPMs wide in an Open Rack v3 scenario and there was some considerations for this implementation while developing the AI Native Edge-MHS Base Specification, please refer to the Open Compute Project specifications for more information
   https://www.opencompute.org/wiki/Open_Rack/SpecsAndDesigns

Additional Industry References

- ASMEY14.5 – 2018 Dimensioning and Tolerancing
- SNIA SFF-TA-1002 - Protocol Agnostic Multi-Lane High Speed Connector
  Rev 1.6a - May 16, 2025.
- SNIA SFF-TA-1016 - Internal Unshielded High Speed Connector System
  Rev1.3 - November 15, 2024.
- SNIA SFF-TA-1026 - Storage System High Speed Cable Interconnect
  Rev2.0a - July 23, 2025.
- SNIA SFF-TA-1033 - Internal High-Speed Cable / Modular Connector System
  Rev2.0 - March 28, 2025.
- SNIA EDSFF E1.S (SFF TA 1046) - EDSFF E1.A Samsung Proposal
  Presented: 30th Jan
- Open19 - Open19 System Level Specification
  Revision 1.0 – 3rd Nov 2019
- EIA-310-E - Electronic Industries Alliance, *Cabinets, Racks, Panels, and Associated Equipment*, EIA/ECA-310-E, Dec. 2005
- Open Rack V3 - Open Rack V3 Base Specification
  Revision 1.0 - 24 AUG 2022
- OTII-E - ODCC-2023-01002 OTII-E Modular Server Technical Specification
  Revision 1.0 – May 2023
- IEC 60529 - IEC 60529 Consolidated version
  Edition 2.2 – 29 Aug 2013
- CXL - Compute Express Link® Specification 4.0
- USB – USB Implementers Forum, Inc.
- DMTF DSP0222 - Network Controller Sideband Interface (NC-SI) Specification
  Version: 1.2.1 – 21 Jul 2021

16 Supplemental Material

16.1 AI Native Edge-MHS Conceptual Implementation Examples

The AI Native Edge-MHS specification has two form factor classes to address various product types and sizes. In this section some of the possible configurations and usages for the different classes will be shown.

It is understood that the configurations shown represent a small sample of what could be possible. This section also conveys the reasoning behind the different sizes of HPM associated with the HPM classes.

16.1.1 Class N

The Class N being the narrow HPM, can be utilized in numerous ways. In a 1U chassis a single Class N HPM can support a PCIe device over the HPM and more PCIe devices adjacent to the HPM through a cabled riser. The Class N is the primary HPM form factor for high density 4 node configurations in a 2U chassis. Dimensioning for the Class N HPM facilitates fixed mounting or sled-based implementations.

Figure 48: AI Native Edge-MHS Class N

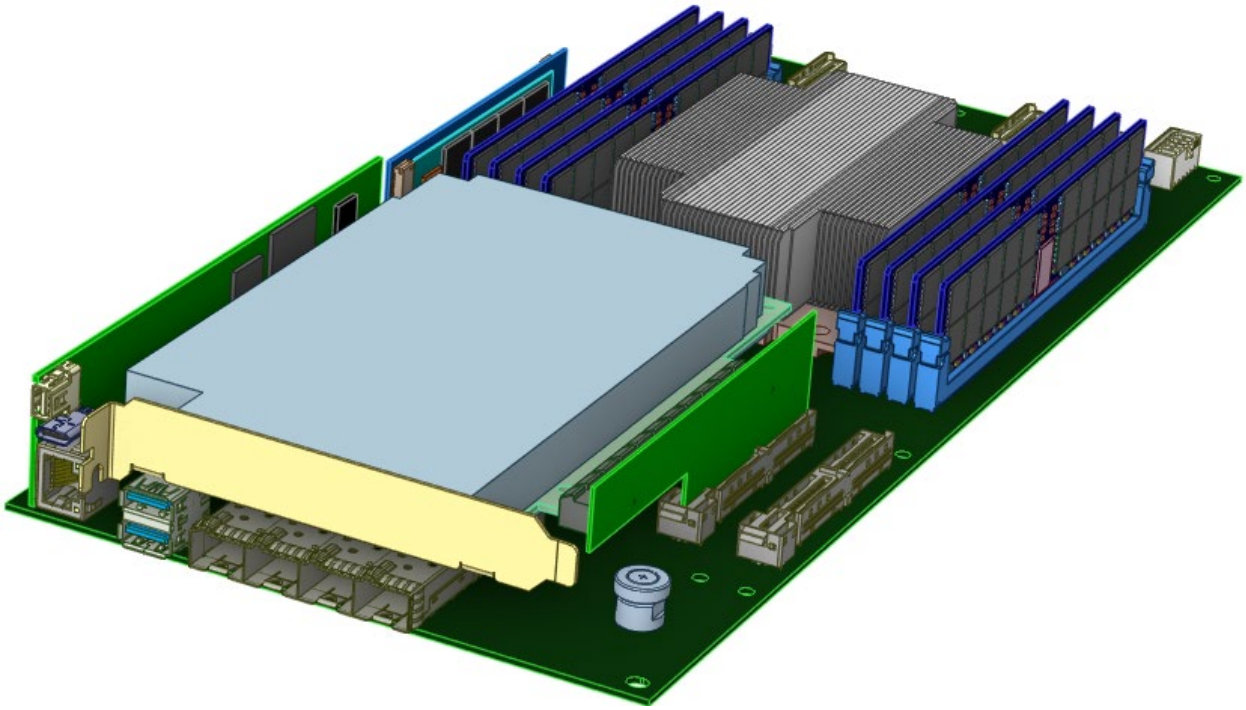


Figure 49: Class N In 1RU Chassis

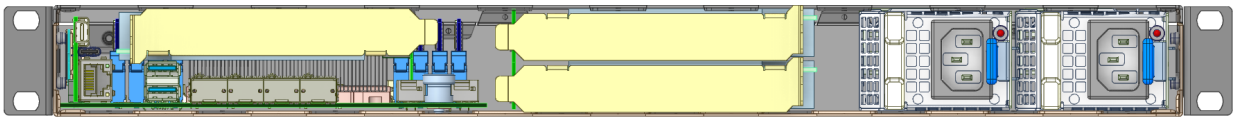
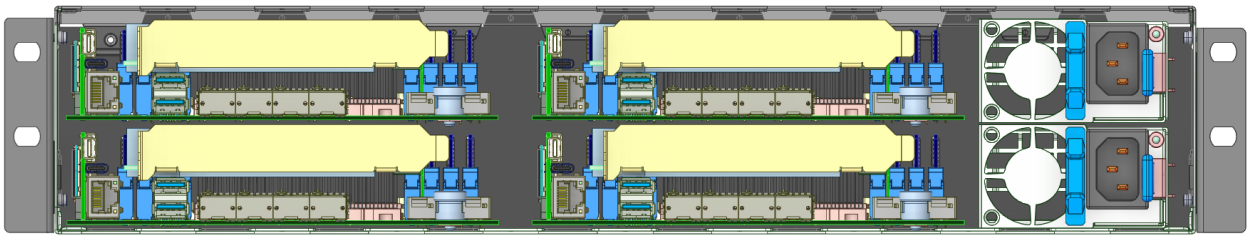


Figure 50: Class N In 2RU Chassis (4 Nodes)



16.1.2 Class L

The Class L HPM is optimized to support short depth chassis designs. **Figure 51** depicts a short Class L length of 260mm which could enable a ~330mm overall chassis. This figure also shows the optional OCP NIC 3.0 integrated into the HPM.

Figure 51: AI Native Edge-MHS Class L260

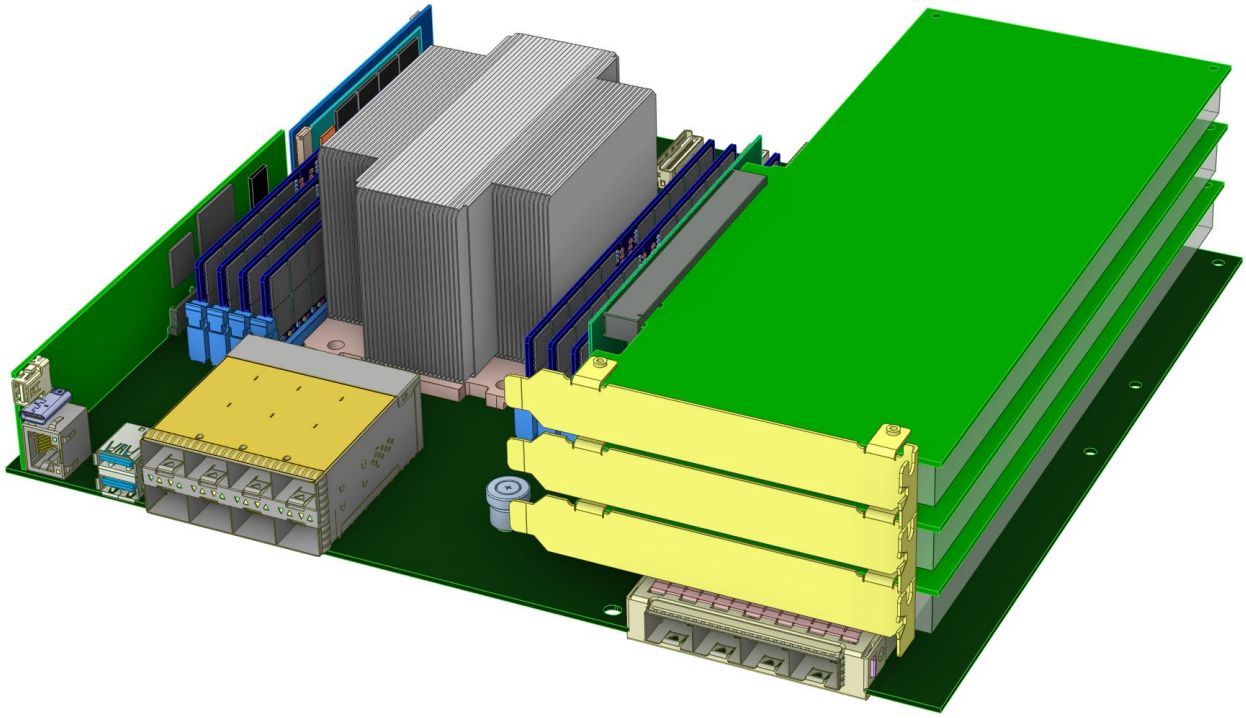


Figure 52

Figure 52: Class L260 in 2RU Chassis

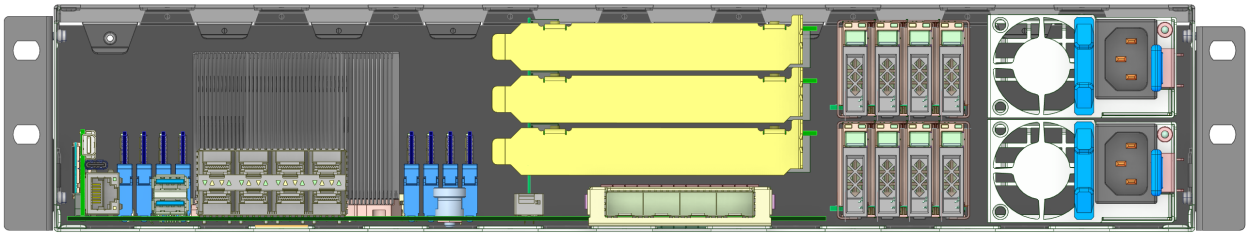
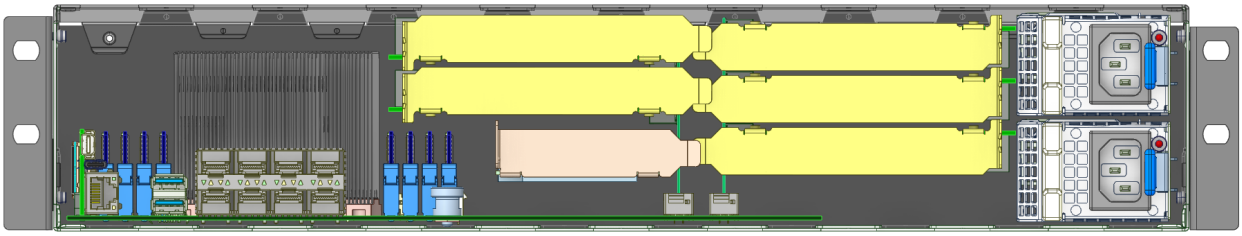


Figure 53 depicts another example product using the Class L260 form factor**.** In this scenario the riser connector placements are not in the specified locations. To make this configuration viable the left and right PCIe cards shall be offset so the tabs can overlap. There would be area below the PCIe cards for other I/O or storage devices.

Figure 53: Class L260 in 2RU Chassis



16.1.3 Class L350+ Considerations

Figure 52 depicts a system with a Class L365 HPM. When longer Class L HPM's are used, the CPU complex can be aligned to the far section. This allows the option of placing half length PCIe cards in the near area.

16.1.4 Multi-Node Specific

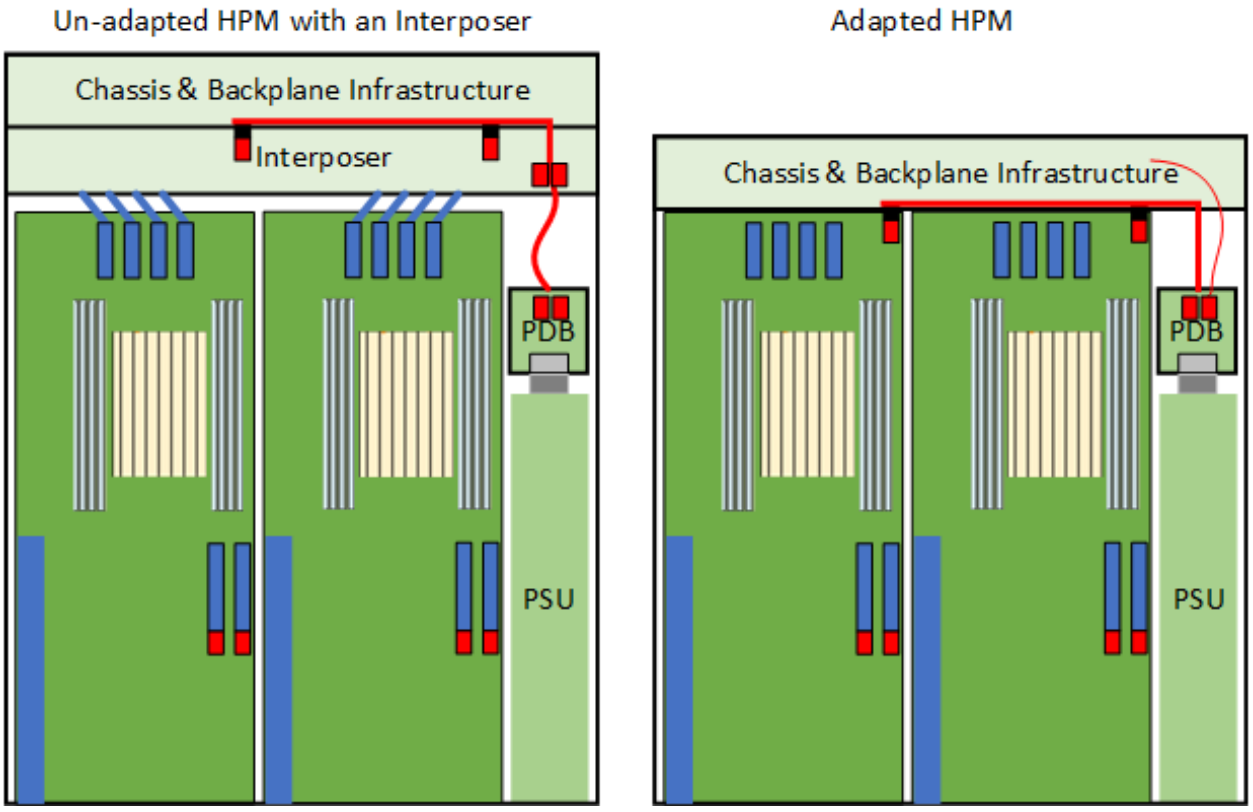
Multi-Node Adaptation

As described in the Power Zone **Section 13.1 HPM Power Zone Overview,** multi-node HPMs may choose to adapt the HPM to add board to board connectors on the Far board edge intended to directly mate into chassis power infrastructure (mid-plane, PDB, bus bar etc.).

Un-adapted HPMs can also be leveraged with this type of chassis infrastructure by leveraging an interposer board between the HPM and the chassis infrastructure.

The example below depicts using an un-adapted HPM on the left and an adapted HPM on the right in a similar system. For this example, shown is two Class N nodes in a short depth 19" chassis. Both HPMs are the same length HPMs so one chassis would be slightly longer than the other.

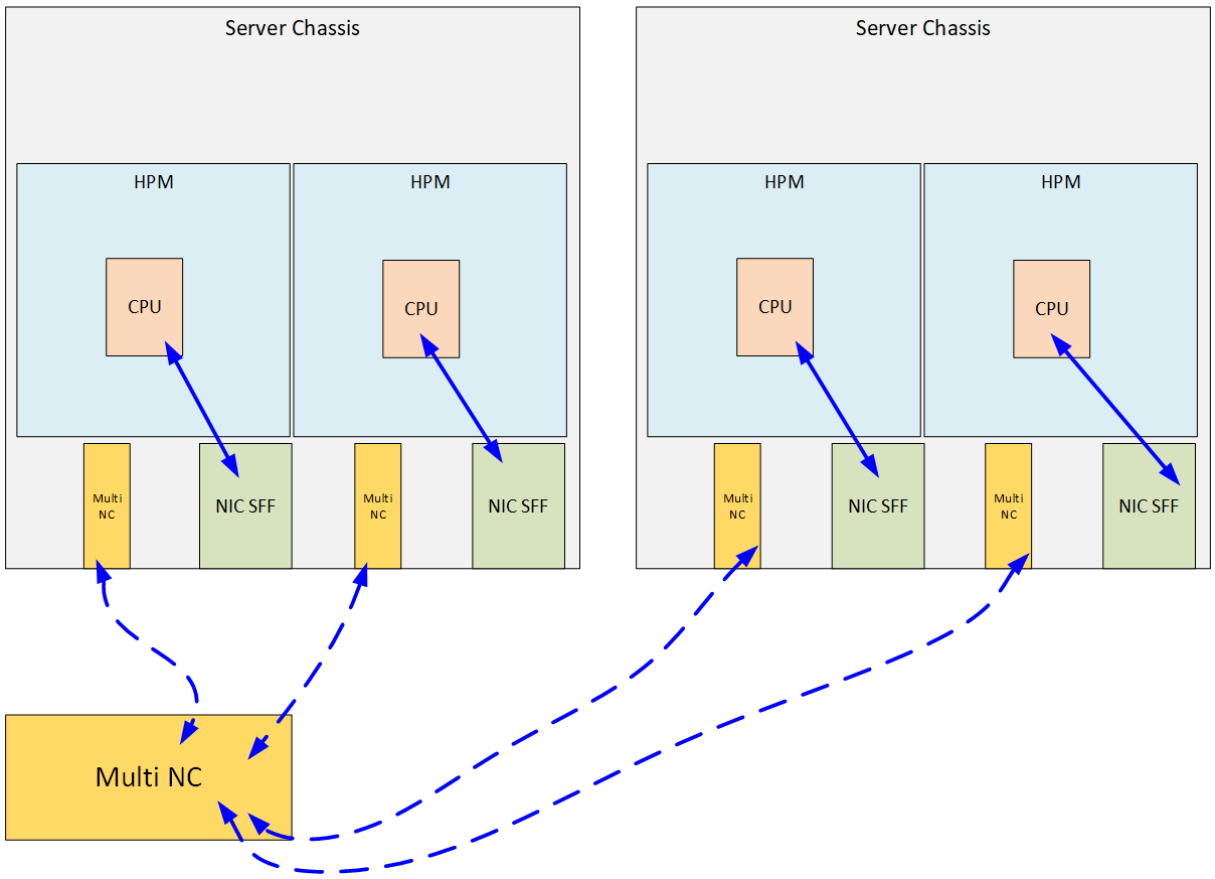
Figure 54: Multi-Node Adaptation Example



Multi-Node Management

How to deploy a multi-node management infrastructure using base specification compliant HPMs is outside of the scope of this specification. However, various common methodologies were evaluated to ensure that AI Native Edge-MHS compliant HPMs could be leveraged into these infrastructures. As an example, a small low-cost local node controller could be connected to the DC-SCM 4C+ connector and then connected to a chassis manager or multi-node controller.

Figure 55: Multi-Node Management Example



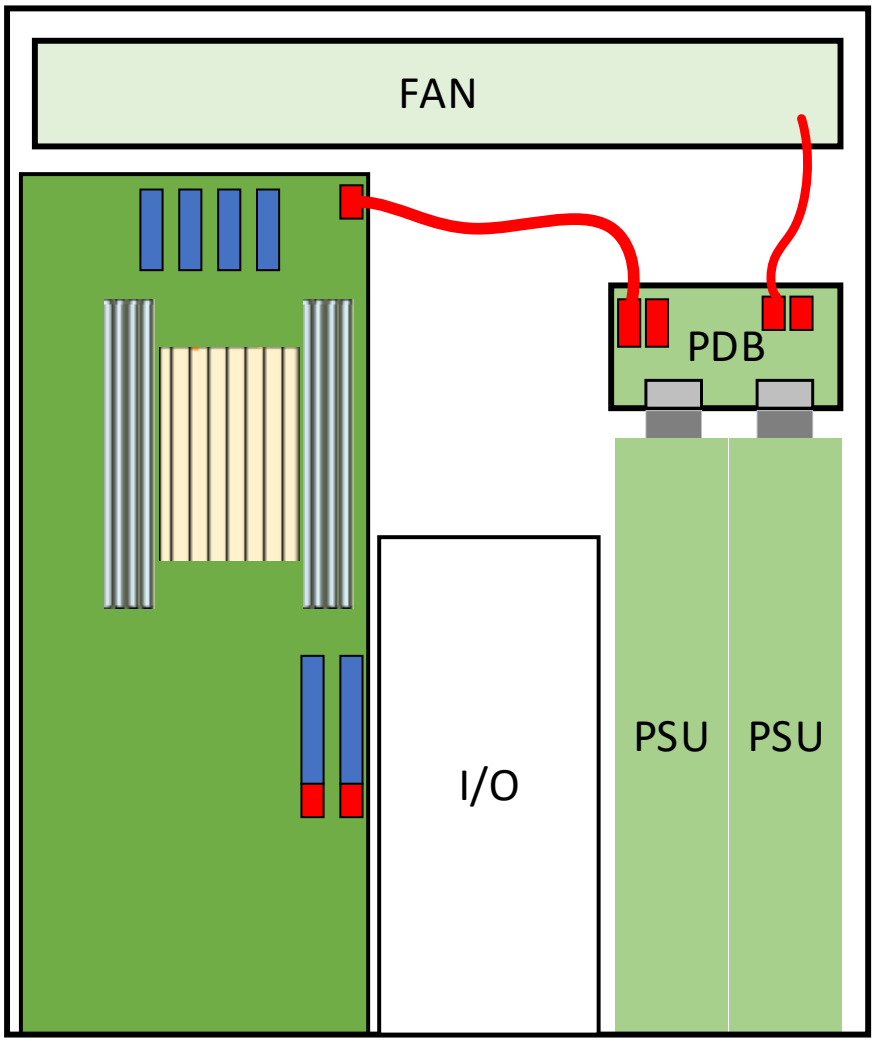
16.2 AI Native Edge-MHS Power Zone Usage Examples

The AI Native Edge-MHS specification provides some flexibility to HPM implementors and system designers when it comes to Power Zone Usage. In this section, demonstration of some expected configurations leveraging these various options are conveyed. For simplicity's sake, the different power flows are demonstrated using the same Class N HPM board, however the power zone use case flexibility is similar across all Classes.

The first example listed below shows a simple monolithic (one HPM) system where PSUs feed power to the system PDB, the HPM power zones are utilized in the minimum required model:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: None

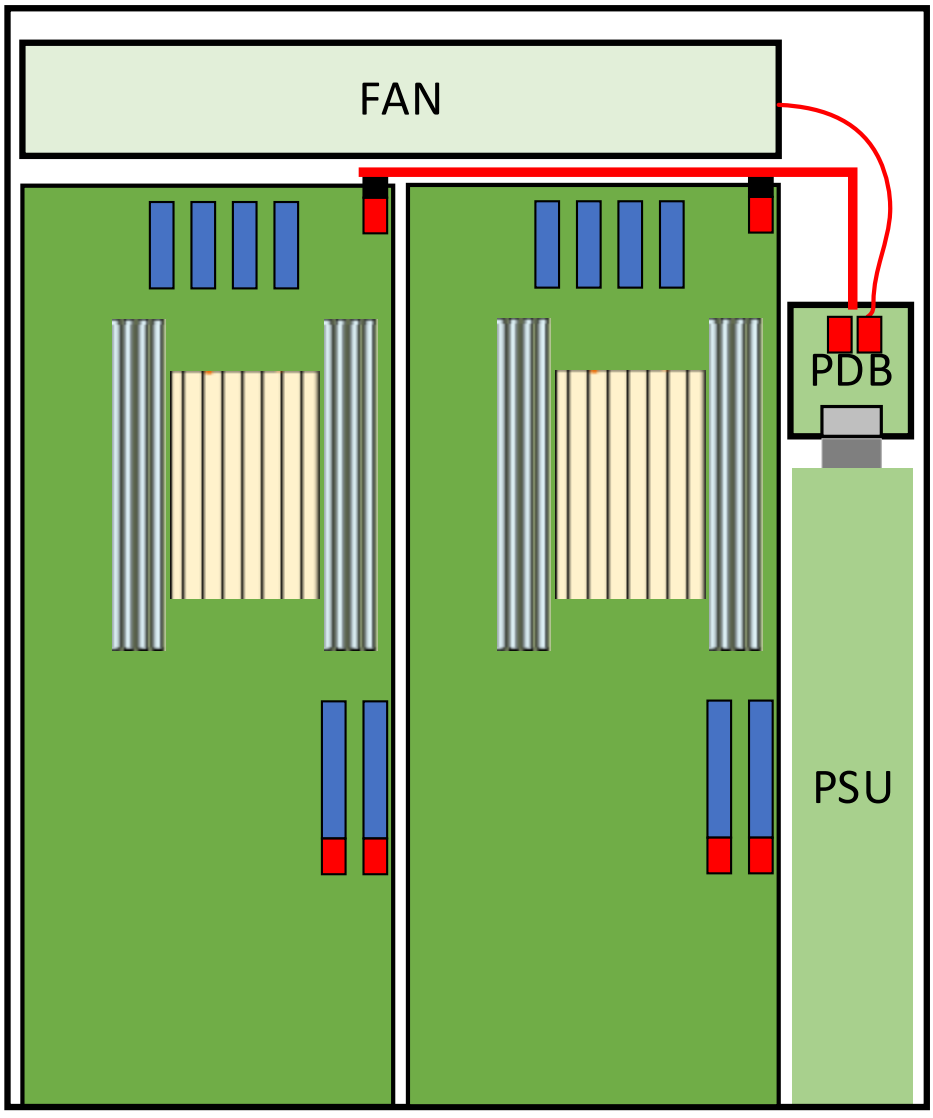
Figure 56: Power Zone Example 1: Monolithic Basic One Zone Ingress



The second example below illustrates a multi-node (>1 HPM) system with a Far Side PDB that could be supplied via PSUs, system level bus bars, or even rack level power distribution.

- Far Side Ingress: Power from PDB to HPM (while these connections are depicted with cables the HPM could also be adapted to support a board-to-board connector to chassis power infrastructure like a PDB as noted in **Section 13.1 HPM Power Zone Overview**)
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: From the PDB directly (does not require a “puck” as control logic could be based on the PDB)

Figure 57: Power Zone Example 2: Multi-node with Far Side PDB

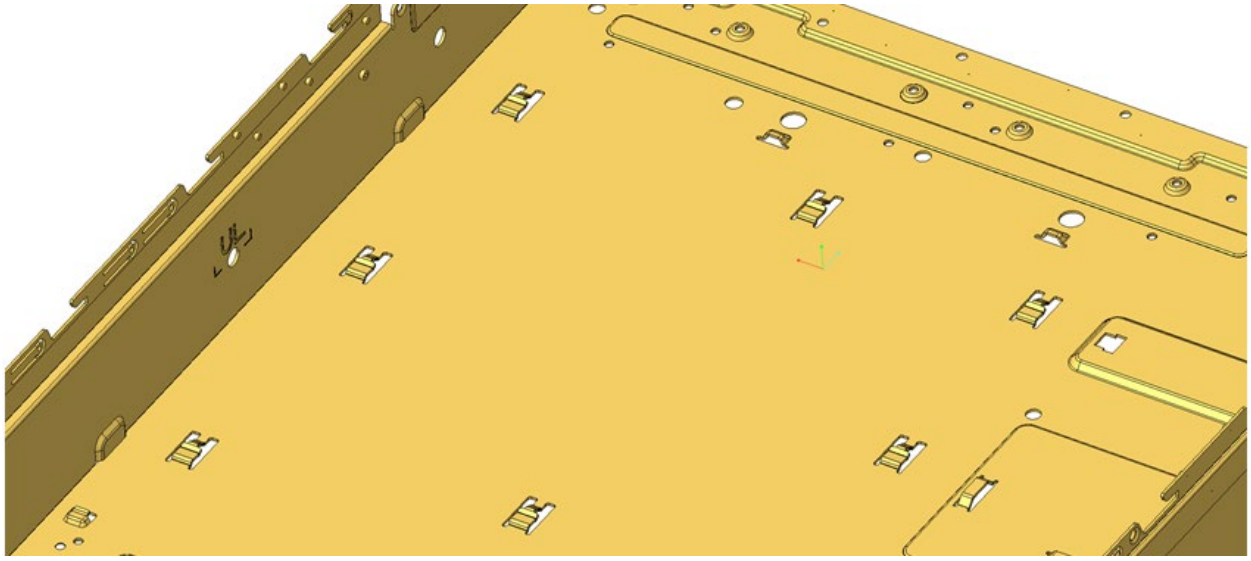


16.3 Example Chassis Base Geometry for Chassis-to-Board Bracket interface

Below is an example geometry required in the chassis base to interface to the Chassis-to-HPM bracketry in **Figure 22: Example of Chassis-to-Board Bracket**

(Board Pan – note that the hole placement below may not match the HPM specification as the illustration is to showcase how the mounting apparatus will work)**.** The exact geometry is not specified, but considerations shall be made for maximum board thickness (see **Section 12.4 HPM Board and Assembly Thickness)** and HPM Keepout Zone sizes (See **Section 12.3 Secondary Side Zones and Height Restrictions**

Figure 58: Example Chassis Base Geometry for Board Bracket Interface



16.4 Potential Future Material

- Timing Support – edge and edge AI inferencing solutions often require tight timing control. The intent of this material/specification would be to provide guidance on how to implement that timing support.
- Blind Mate Support for HPM's – many edge solutions deployed require field servicing which leads to sled-based servers that need blind mate connections for power and signaling. The intent of this material/specification would be to provide guidance on how to implement blind mate support to HPM's.
- 162mm HPM – 162mm is an HPM size which is interesting due to the fact that it allows rear power supply support in short depth enclosures (450mm or less) and it can allow 3 sled wide implementations in a 21-inch chassis. The intent of this specification update would be to provide support for a 162mm wide HPM in the AI Native Edge-MHS specification. Provisions have already been taken to provide common mounting in the current HPM specification by moving the mounting holes on one side of the Class N and Class L HPMs to allow common support for a 162mm HPM. See Class N example image below (Mounting holes on left encapsulated by dashed box have been shifted by 6mm to the right – moving from 6mm from the board edge to 12mm from the board edge):

Figure 58: Mounting Hole Changes from Edge-MHS 0.5 to 0.9

