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Dual-Stripline Configuration for Efficient Signal Routing in the Bunch-of-Wires Interface

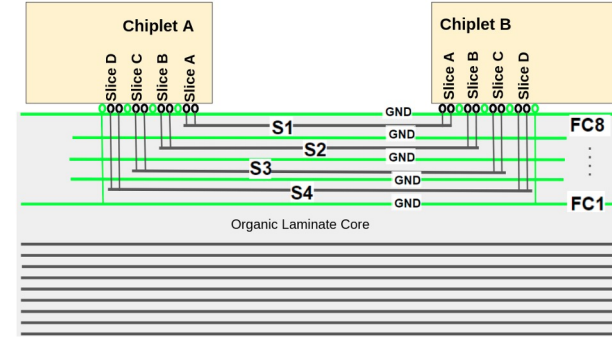
(Chiplet Design and Architecture - June 19, 2022)

Shekar Geedimatla, Robin James Payyappillil, Devi Sreekumar, and Shalabh Gupta

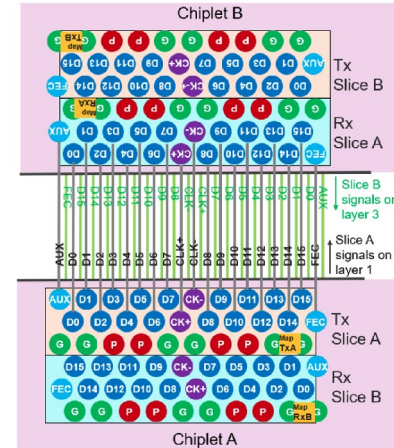
Department of Electrical Engineering,
IIT Bombay, Mumbai – 400076, INDIA

Introduction

- Bunch-of-Wires (BoW) standard supports high-density interconnect routing on organic substrates.
- BoW modes: BoW-32, BoW-64, BoW-128 and BoW-256
- BoW 1-slice: 16 signal lines, max 256 Gbps with 16 Gbaud/wire
- Standard 8-2-8 stackup: Signals routed on striplines in four layers, with BoW-256 providing a throughput of ~ 1 Tbps/mm with 4 slices

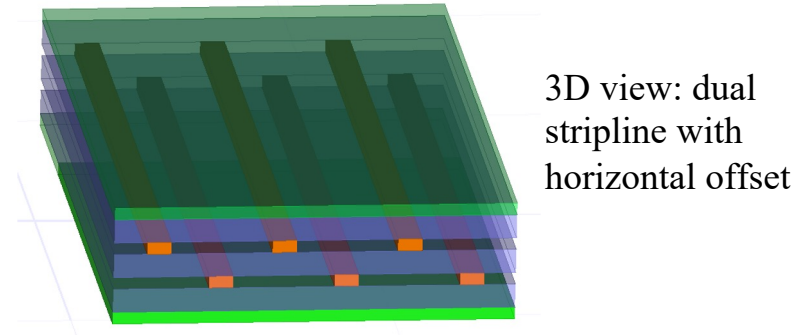


8-2-8 stackup with 4 signal layers



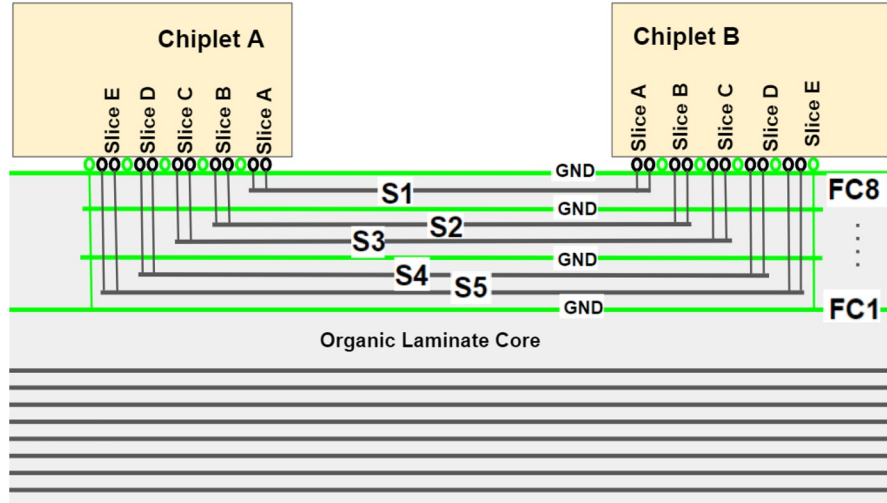
Goal

- Increase the routing efficiency in the 8-2-8 stackup
- Sufficient wire-to-wire pitch in the standard BoW bump-map makes it possible to route the signals in the dual-stripline configuration
- In dual-stripline configurations, two vertically adjacent signaling layers used between the reference/ground planes
- Routing density improves by 33%



- Drawbacks: Increase in crosstalk – signal layers are routed adjacent to one another
- Solution: The signal lines in one layer are offset horizontally by half the wire-to-wire pitch in one of the layers

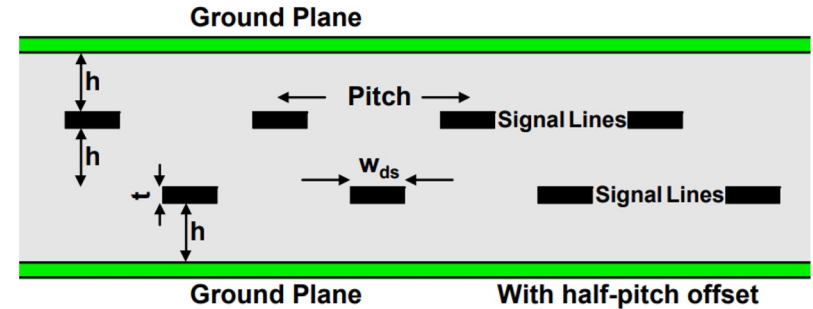
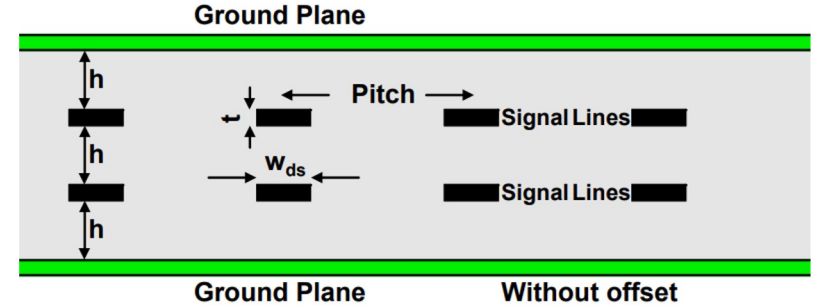
Dual stripline



8-2-8 stackup with 5 signal layers
(including dual-striplines)

Target specifications: BoW

- Insertion loss: 4dB @8GHz and 12dB @16GHz
- Powersum crosstalk: Below -15dB upto 16GHz



Simulation setup

Requirement:

- Insertion loss: less than 4dB @8GHz
- Power-sum crosstalk < -15dB @16GHz
- horizontal eye opening $\cong 0.5UI$ @BER of 10^{-15}
- Characteristic impedance: 50Ω

Physical parameters and material properties:

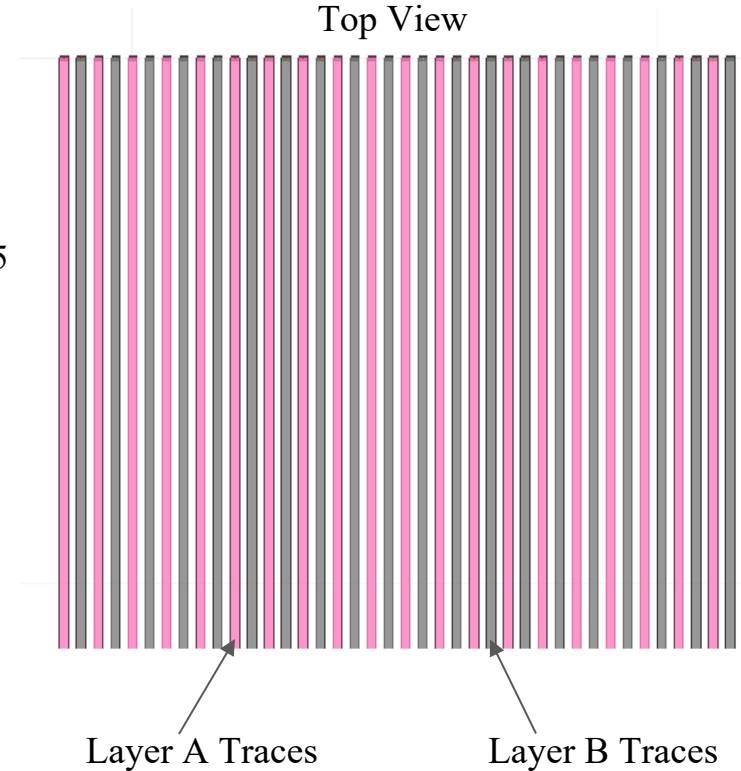
Substrate(ABF) height(h): $30\mu\text{m}$

Metal thickness(t): $15\mu\text{m}$, Trace pitch: $65\mu\text{m}$,

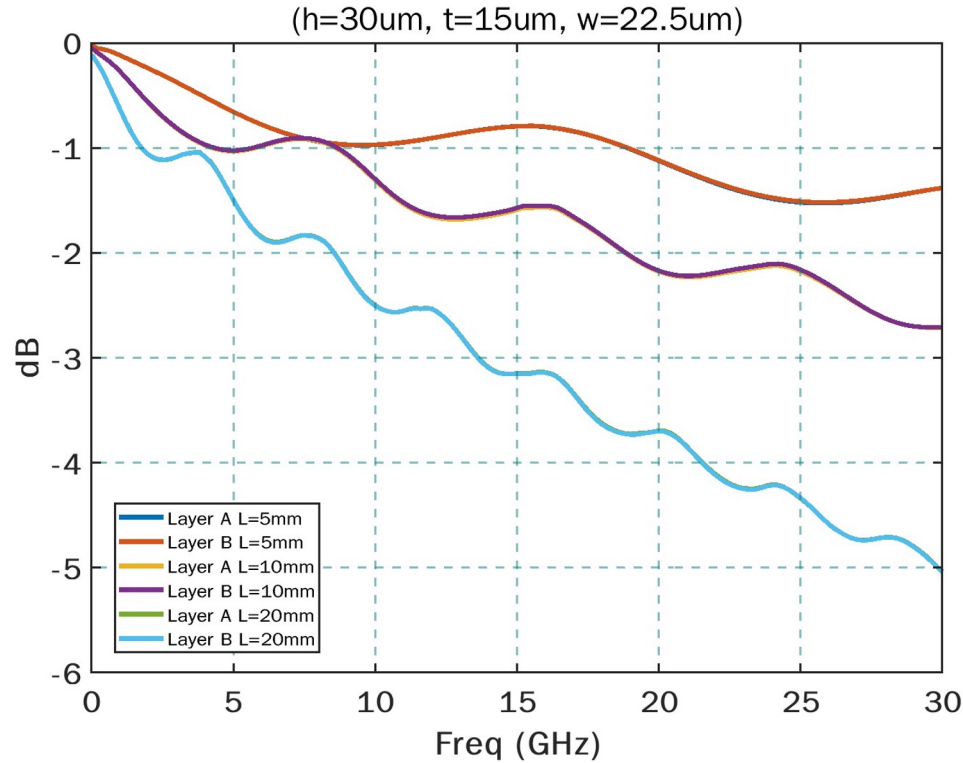
Trace length: 20mm, Roughness: $0.4625\mu\text{m}$,

Dielectric constant: 3.4, Loss tangent: 0.019

Number of lines: 20 in each layer



Insertion loss

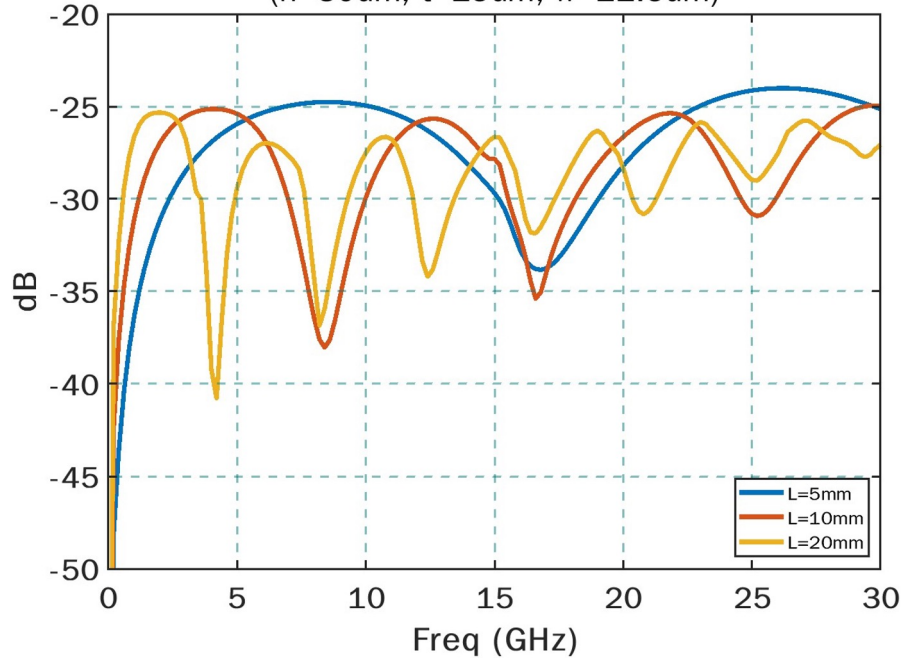


Length (mm)	Insertion Loss @ 8GHz	Insertion Loss @16GHz
5	0.93dB	0.8dB
10	0.93dB	1.55dB
20	1.86dB	3.14dB

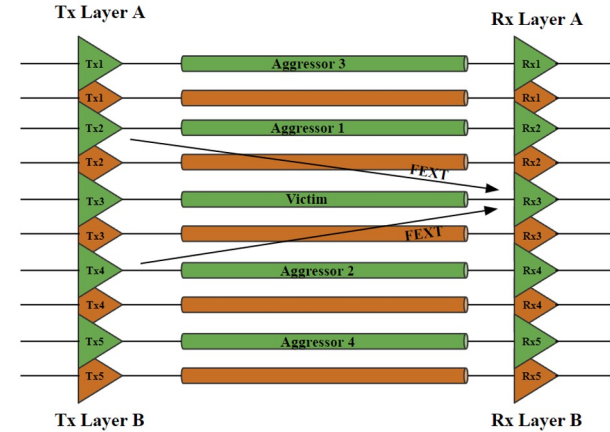
The dual-stripline structure meets the insertion loss specification: below 4dB @8GHz and 12dB @16GHz

Powersum crosstalk: Co-propagating signals

(h=30um, t=15um, w=22.5um)

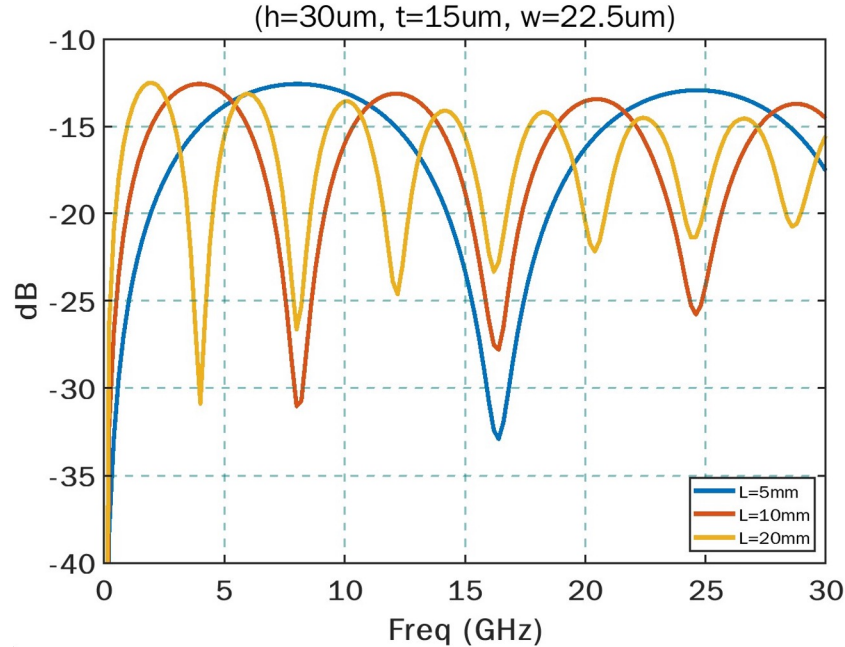


The dual-stripline structure meets the powersum crosstalk specification (below -15dB) for co-propagating signals

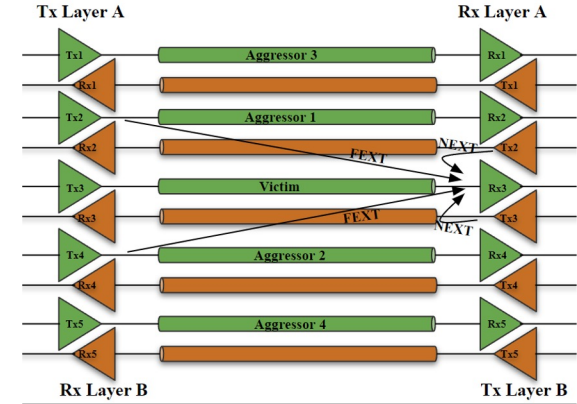


Length (mm)	Crosstalk @8GHz	Crosstalk @16GHz	Maximum crosstalk
5	-24.78dB	-32.77dB	-24dB
10	-36.5dB	-32.07dB	-24.94dB
20	-34.42dB	-29.76dB	-25.32dB

Powersum crosstalk: Counter-propagating signals



The dual-stripline structure does not meet the powersum crosstalk specification (of <-15dB) for counter-propagating signals for h=30um (dielectric height)



Length (mm)	Crosstalk @8GHz	Crosstalk @16GHz	Maximum crosstalk
5	-12.57dB	-30.81dB	-12.57dB
10	-31.03dB	-26.16dB	-12.57dB
20	-26.63dB	-22.30dB	-12.50dB

Far end crosstalk

$$\text{FEXT} = \frac{V_f}{V_a} = \frac{\text{Len}}{\text{RT}} \times k_f = \frac{\text{Len}}{\text{RT}} \times \frac{1}{2v} \times \left(\frac{C_{mL}}{C_L} - \frac{L_{mL}}{L_L} \right)$$

where:

FEXT = far-end cross-talk coefficient

V_f = voltage at the far end of the quiet line

V_a = voltage on the signal line

Len = length of the coupled region between the two lines

k_f = far-end coupling coefficient that depends only on intrinsic terms

v = speed of the signal on the line

C_{mL} = mutual capacitance per length, in pF/inch (C_{12})

C_L = capacitance per length of the signal trace, in pF/inch (C_{11})

L_{mL} = mutual inductance per length, in nH/inch (L_{12})

L_L = inductance per length of the signal trace, in nH/inch (L_{11})

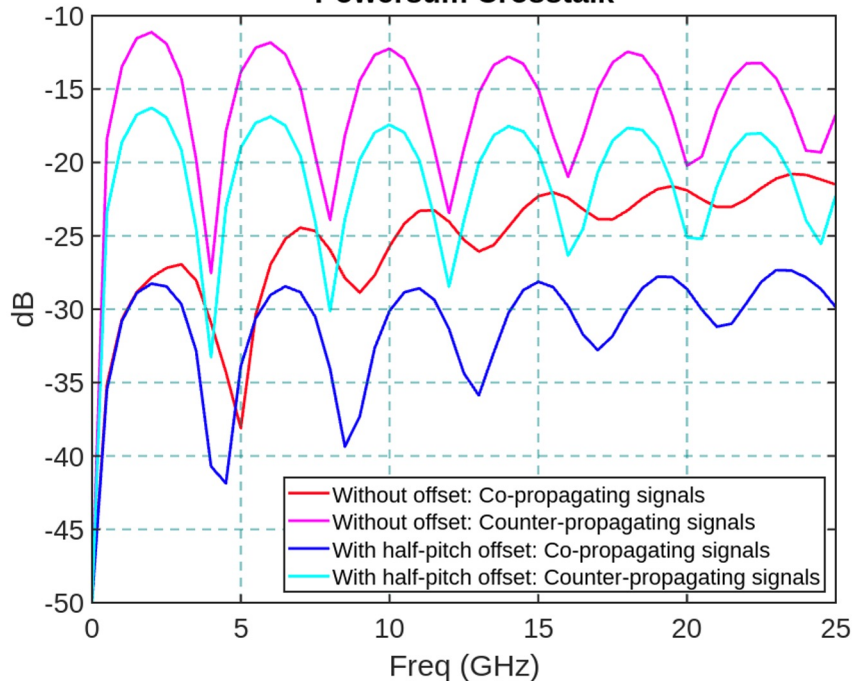
RT = signal rise time

Eric Bogatin. (2018). Chapter 10 - Crosstalk in Transmission Lines, Signal and Power Integrity - Simplified, Third Edition. Prentice Hall modern semiconductor design series.

Crosstalk: Dual stripline with reduced height

($h = 20\mu\text{m}$, $t = 5\mu\text{m}$, $w = 17\mu\text{m}$)

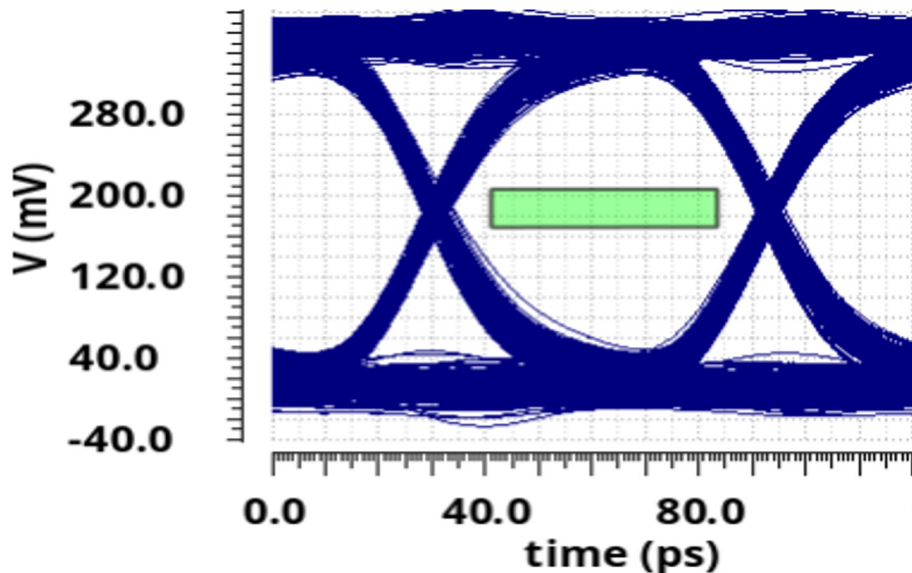
Powersum Crosstalk



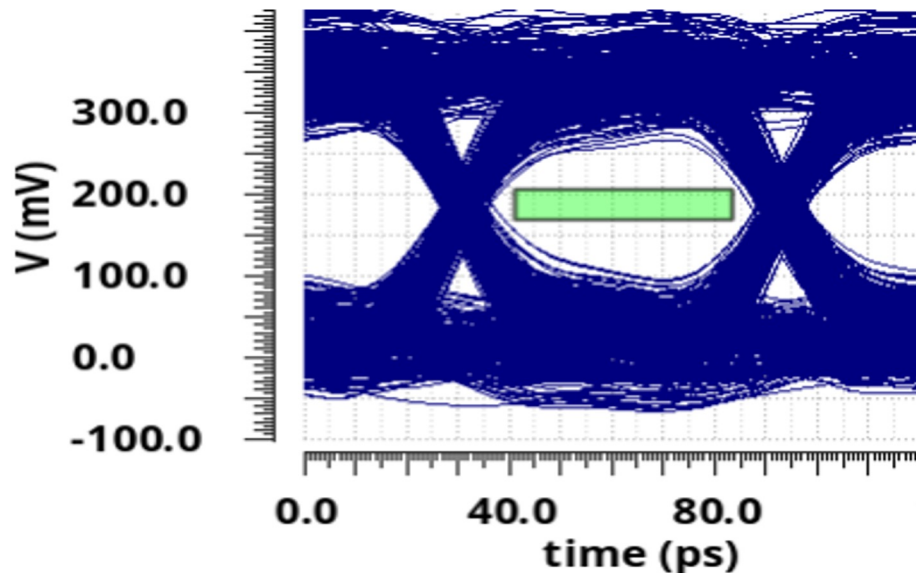
Configurations		Maximum powersum crosstalk (dB)
Without offset	Co-propagating signals	-20.87
	Counter-propagating signals	-11.13
With half-pitch offset	Co-propagating signals	-27.36
	Counter-propagating signals	-16.27

Dual-stripline structure with reduced dielectric height (20 μm) and half-pitch offset meets the crosstalk specification (below -15dB) with counter propagating signals as well

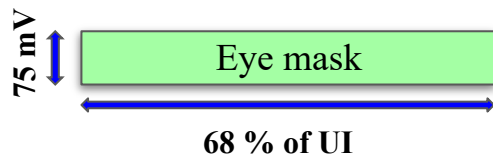
Eye diagram: Transient simulations ($h=30\mu\text{m}$, 20mm channel)



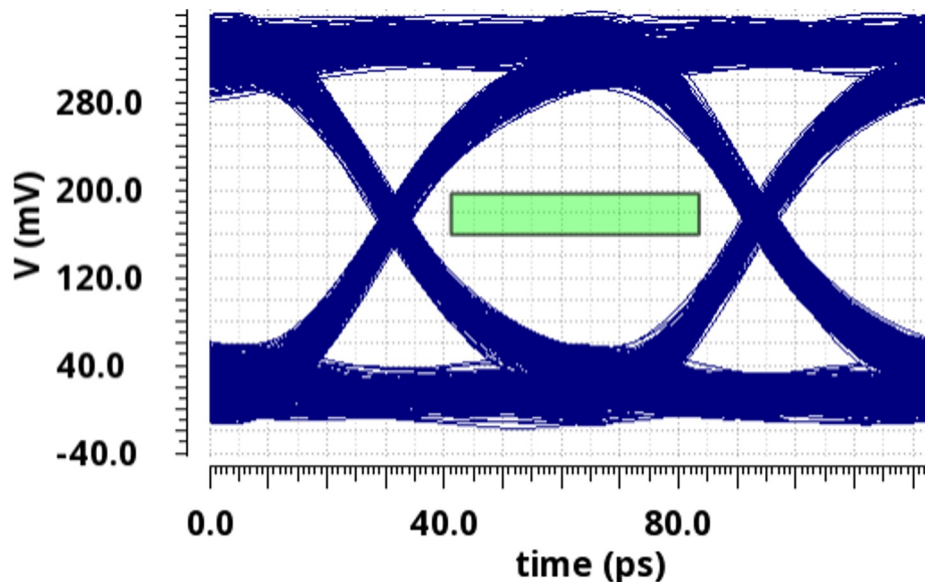
Co-propagating signals



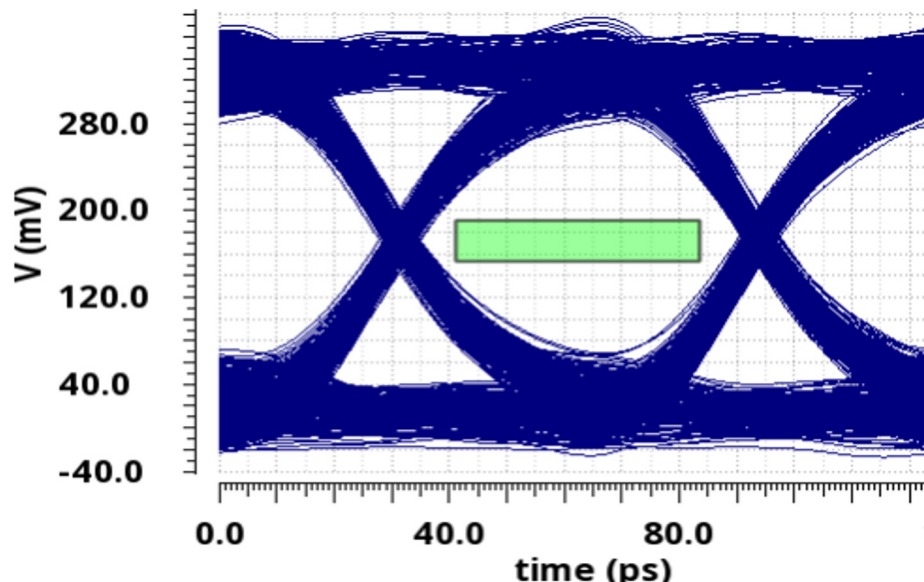
Counter-propagating signals



Eye diagram: Transient simulations ($h=20\mu\text{m}$, 20mm channel)



Co-propagating signals



Counter-propagating signals

Simulations carried out for the dual-stripline configuration indicate that horizontal eye opening specifications (0.68UI) are met

Summary

- Dual Strip line configuration can be adopted for the BoW interface as a viable option to increase the routing density
- Cross talk effect can be reduced by providing half-pitch offset between adjacent layers
- Simulation results validate that performance metrics such as crosstalk and horizontal eye opening requirements are met

References

- [1] Heterogeneous integration roadmap, 2021 <https://eps.ieee.org/>.
- [2] S. Ardalan et al., "Bunch of Wires: An Open Die-to-Die Interface," IEEE Symposium on High-Performance Interconnects (HOTI), 2020, pp. 9-16.
- [3] Intel, 2019. "Advanced interface bus (AIB) specification" 2019.9.18 revision 1.2. <https://www.intel.com/content/dam/altera-www/global/enUS/pdfs/literature/manual/advanced-interface-bus-specification.pdf>.
- [4] UCIE, Universal Chiplet Interconnect Express (UCIE): Building an open chiplet ecosystem, 2022, <https://www.uciexpress.org/>.
- [5] OCP-ODSA, 2021. The open domain specific architecture - a technical introduction, <https://www.opencompute.org/wiki/Server/ODSA>.
- [6] J. Hsu and K. Xiao, "Broad-side crosstalk mitigation in dual-stripline designs," 2012 IEEE 62nd Electronic Components and Technology Conference, 2012, pp. 1955-1959.
- [7] H. Lin, B. -C. Tseng and J. Yen, "Optimization of Far-End Crosstalk Equations and Parameters for Single-Ended Dual-Stripline," 2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI PI), 2018, pp. 116-121.
- [8] G. Servel, D. Deschacht, F. Saliou, J. -. Mattei and F. Huret, "Inductance effect in crosstalk prediction," in IEEE Transactions on Advanced Packaging, vol. 25, no. 3, pp. 340-346, Aug. 2002, doi: 10.1109/TADVP.2002.806732.

Thank you