200Gb/s QSFP56 FR4 3km Optical Transceiver

T-FX4FNT-HF8

Product Specification for Suzhou Site

with TI Power IC



Features

- IEEE802.3bs 200GBASE-FR4 compliant
- QSFP56 MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- Supports 212.5Gb/s aggregate bit rate
- Up to 3km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 15 to 65°C
- 200GAUI-4 electrical interface
- Compliant to 200G FR4 OCP Sepcification
- Maximum power consumption 6.5W
- LC duplex connector
- RoHS compliant

Applications

- Data Center Interconnect
- 200G Ethernet
- Enterprise networking

Part Number Ordering Information

T-FX4FNT-HF8	QSFP56 FR4 3km with FEC optical transceiver with full real-time digital diagnostic monitoring and pull tab

1. General Description

This product is a 200Gb/s transceiver module designed for 2km optical communication applications. The design is compliant to IEEE802.3bs 200GBASE-FR4 standard. The module converts 4 inputs channels (ch) of 50Gb/s (PAM4) electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 200Gb/s(PAM4) optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 200Gb/s(PAM4) input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP56 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

This product converts the 4-channel 200Gb/s(PAM4) electrical input data into CWDM optical signals (light), by a driven 4-wavelength EMLs. The light is combined by the MUX parts as a 200Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 200Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 50Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA and a post amplifier. Analog CDR is used to recovery PAM4 signals. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a

reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Transceiver Block Diagram

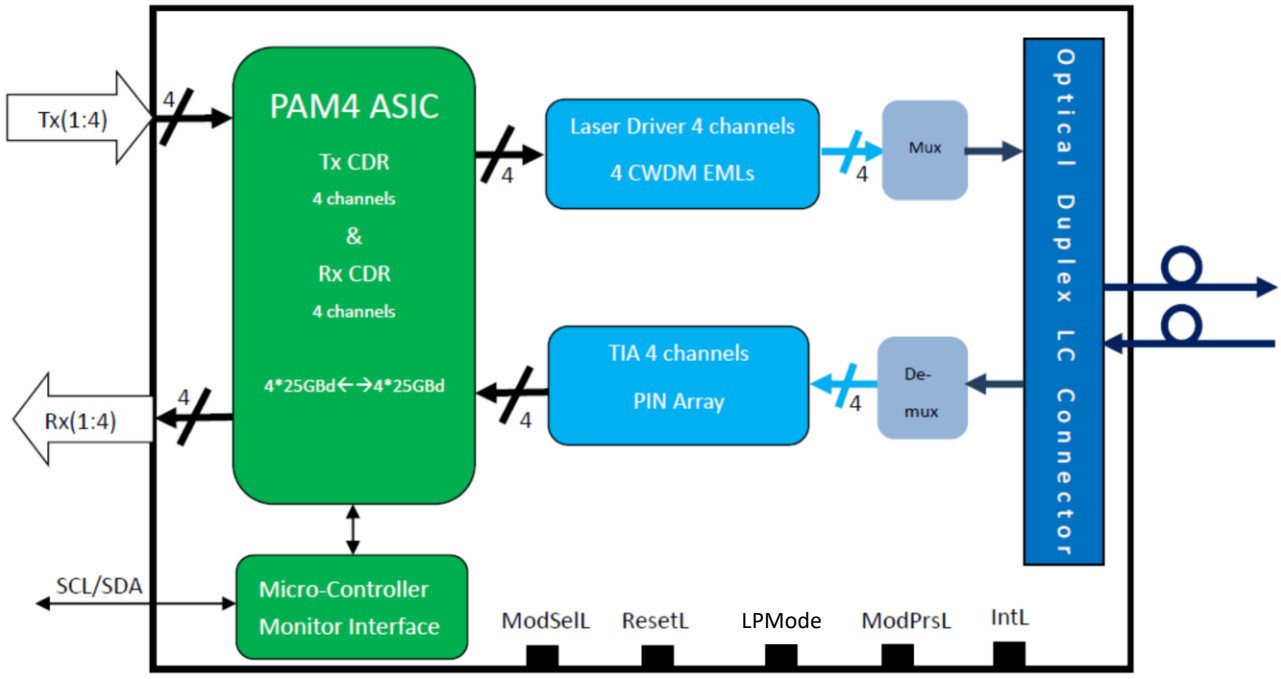


Figure 1. Transceiver Block Diagram

4. Pin Assignment and Description

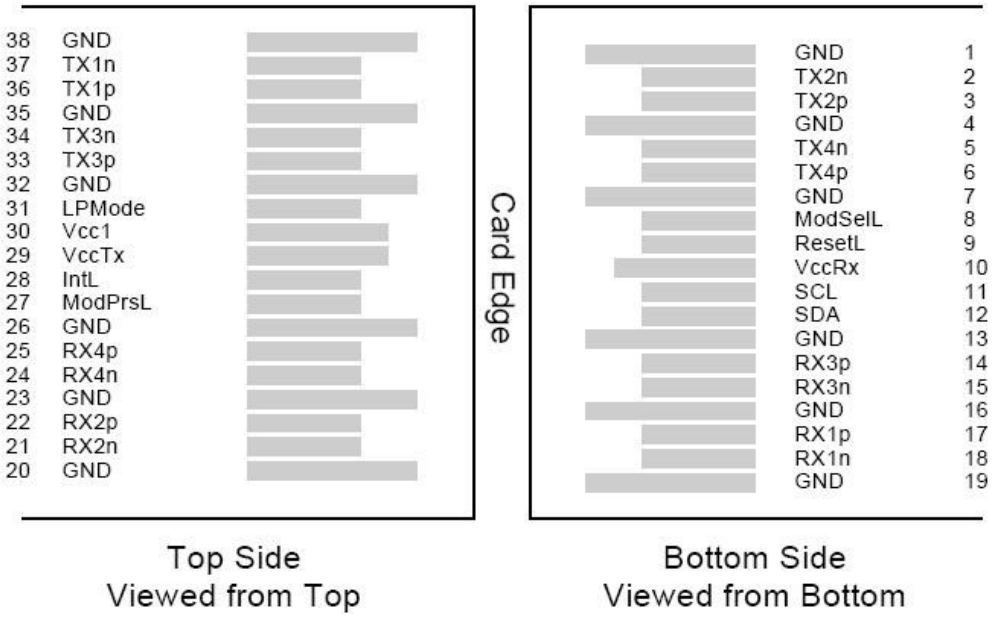


Figure 2. MSA compliant Connector

Pin Definition

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	

18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP56 modules. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

5. Recommended Power Supply Filter

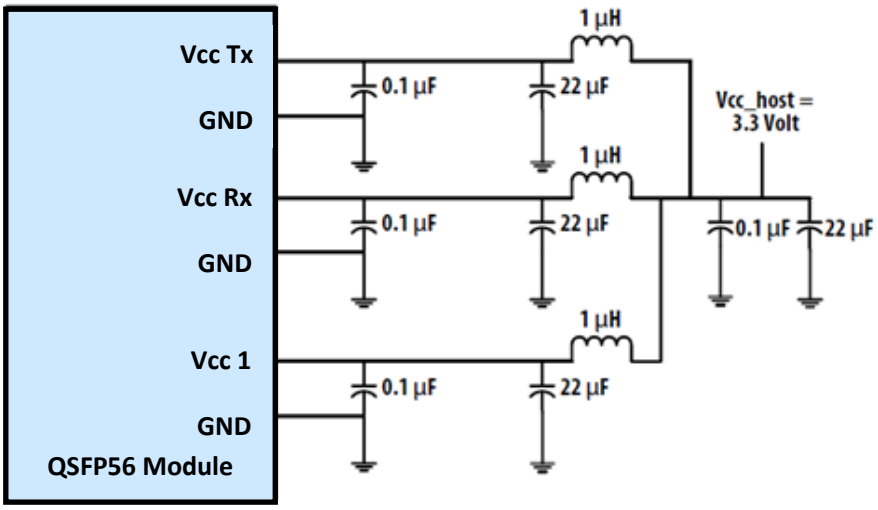


Figure 3. Recommended Power Supply Filter

6. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	15	65	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH_d		-5.7	dBm	

7. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	15		65	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Consumption				6.5	W	200G
				6.0	W	100G
Supply Current	Icc			1.96	A	200G
				1.80	A	100G
Data Rate, each Lane			26.5625		GBd	

Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance with G.652	D	0.002		3	km	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Power consumption	P			6.5	W	In 200G mode
				6.0	W	In 100G mode
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3

Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

9. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1265.25	1271	1276.75	nm	
	L1	1285.25	1291	1296.75	nm	
	L2	1305.25	1311	1316.75	nm	
	L3	1325.25	1331	1336.75	nm	
Transmitter						
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	Modulated
Total Average Launch Power	P_T			10.7	dBm	
Average Launch Power, each Lane	P_{AVG}	-5.2		4.7	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-2.2		4.5	dBm	2
Launch Power in OMAouter minus TDECQ, each Lane		-3.5			DB	
Transmitter and Dispersion Eye Clouser for PAM4, each Lane	TDECQ			3.3	DB	
Extinction Ratio	ER	3.5			DB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4	DB	
Rise and Fall time	Tr/tf			20	ps	3
Outer rail overshoot/undershoot				30	%	4
$RIN_{16.5}OMA$	RIN			-132	DB/Hz	5
Optical Return Loss Tolerance	TOL			16.5	DB	
Transmitter Reflectance	T_R			-26	DB	6
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-30	dBm	

Transmitter reflectance	ORL			17.1	dB	
Receiver						
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5.7			dBm	
Average Receive Power, each Lane		-9.2		4.7	dBm	7
Receive Power (OMA_{outer}), each Lane		-7		4.5	dBm	8
Difference in Receiver Power between any Two Lanes (OMA_{outer})				4.1	dB	
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.6	dBm	9
Bit Error Ratio Floor	BER_FL			3.4E-6		10
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-18	-15	-12	dBm	
LOS Hysteresis	LOSH	1	2	3	dB	
Stressed Conditions for Stress Receiver Sensitivity						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.3		dB	
OMA_{outer} of each Aggressor Lane			0.5		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) must exceed the minimum value specified here.

3. Between 20% and 80%. It can be measured by applying PRBS15 and search for pattern "00003333000" There is a built-in function in the keysight DCA-X to enable this measurement.
4. Measured based on cumulative distribution function (CDF) of vertical histogram of PAM4 eye.
5. RIN on OMA measured with 16.5dB return loss.
6. Transmitter reflectance is defined looking into the transmitter.
7. Average receive power, each lane(min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
8. Receiver sensitivity (OMA_{outer}), each lane is informative and is defined for a transmitter with SECQ of 0.9dB
9. Measured with conformance test signal at TP3 for the BER = 2.4E-4.
10. Measured with a reference transmitter to produce SECQ greater than or equal to 2dB. The BER at receiver must stay within the specified limit over an OMA range of -4.9dBm to 4.5dBm

10. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

11. Mechanical Dimensions

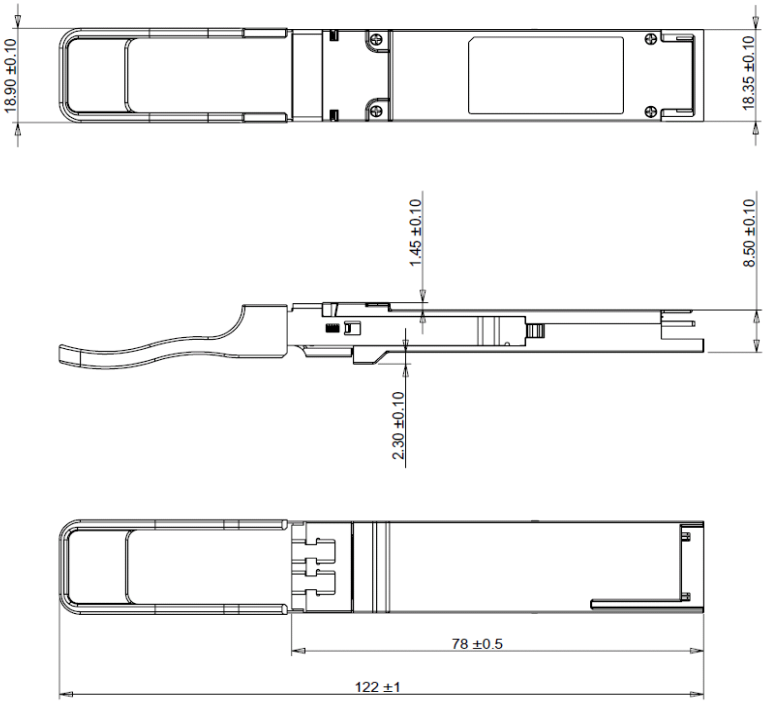


Figure 4. Mechanical Outline

12. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

13. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

USA	China
InnoLight Technology USA Inc. Tel: (408) 216-8889 Email: omok@innolight.com Address: 3235 Kifer Road, Suite 260 Santa Clara, CA 95051 USA	InnoLight Technology (Suzhou) Ltd. Tel: (0512) 8666-9288 Email: sales@innolight.com Address: 8 Xiasheng Road Suzhou Industrial Park, Suzhou, Jiangsu 215126, China

Contact Information