**INTREPID:** Developing Power Efficient Analog Coherent Interconnects to Transform Data Center Networks

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### Integration of Photonic Interfaces into Chip Packages

**Conventional Packaging:**
- Low integration level limits performance and efficiency

**INTREPID:** Energy-efficient coherent links for the datacenter
- Replace power-hungry electrical I/O with highly-efficient photonics and use the power saved to expand switch radix

**Analog Coherent WDM links**
- Expanded link budgets enable photonic routing/switching
- Low power: no/very little DSP
- Target: 800Gb/s/fiber = 4x@200Gb/s/λ (dual-pol QPSK, 50 Gbaud/s)

**Multimode VCSEL links**
- Server connections (30m)
- SOG → 100G

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### Analog Coherent Links: Maximizing Energy Efficiency

**Direct Detection**
- Detected power \( \propto (P_{\text{in}} \cdot A_{\text{det}}) \)
- \( P_{\text{in}} \): laser power, \( A_{\text{det}} \): total link attenuation
- RX sensitivity sets energy efficiency
- Sensitivity degrades with datarate
- Shrinking link budgets

**Coherent Detection**
- Detected power \( \propto (P_{\text{in}} \cdot A_{\text{det}}) \cdot P_{\text{LO}} \)
- \( P_{\text{LO}} \): Local Oscillator (LO) power
- ~20dB improvement in RX sensitivity
- Ability to compensate for insertion loss of optical routing/switching devices

### Optical Phase Locked Loop (OPLL) → Eliminating Power-Hungry DSP

OPLL locks phase and frequency of local oscillator allowing reception at low bit error-rate (BER) without forward error correction (FEC)

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### Integration And Scalability

**Table:**

<table>
<thead>
<tr>
<th>Switch ASIC</th>
<th>Integrated Photonic I/O</th>
<th>INTREPID Coherent Integration</th>
<th>25.6 Tb/s Switching Chip</th>
<th>L-Level Folded Clos</th>
<th>Adding One AWGR Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Rate per Integrated Port or per Fiber (Gb/s)</td>
<td>Chip Ports per Integrated Port</td>
<td>Number of Integrated Ports (RADIX)</td>
<td>Number of 50G Servers</td>
<td>2 (R/ρ) (N/2)</td>
<td>8 of 50G Servers</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>100</td>
<td>2</td>
<td>256</td>
<td>65,536</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>200</td>
<td>4</td>
<td>128</td>
<td>10,384</td>
</tr>
<tr>
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<td>100</td>
<td>400</td>
<td>8</td>
<td>64</td>
<td>8</td>
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<tr>
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<td>200</td>
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<td>16</td>
<td>32</td>
<td>4,096</td>
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<td>8</td>
<td>100</td>
<td>1,000</td>
<td>32</td>
<td>16</td>
<td>52,428</td>
</tr>
</tbody>
</table>

**INTREPID Integration Target:**
- \( R = 4 \) to \( 8 \)
- \( r = 200 \) Gb/s per \( \lambda \)
- \( R = 800 \) to 1,600 Gb/s per Fiber

**Same number of servers with current technology**

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**Future: Optical-switch-based architecture**

- Disaggregation
- Configurability to match workload
- High utilization
- Improved energy efficiency

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