OCP NIC 3.0 Card Design and Interoperability Testing

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Agenda

- OCP 3.0 NIC Design
- Interoperability Testing
  - Thermal
  - Electrical
- PCIe Conformance Testing for OCP platforms
- Future Work
Methodology

• Extend the success of OCP 2.0 by clearly specifying characteristics that allow ease of use across multiple systems.

• Thermal:
  - Standardize thermal requirements testing and details system requirements for airflow.

• Form Factor:
  - Clearly specify design limits and tolerances.
  - Industry standard SFF-TA-1002 (Rev 1.1)

• Systems Management:
  - Defines the minimum set of commands necessary to integrate any OCP 3.0 card into a compatible system.
Mechanical comparison to other Form Factors

Usable Space:
SFF to HHHL = 20% less
SFF to OCP2 = equivalent
LFF to FHFL = 50% less
LFF to FHHL = 13% less

Key difference for cooling is the topside keepout:
PCIe = 14.47 mm
OCP3 = 11.5 mm

Key difference for component placement
Bottom side Keepout:
PCIe = 2.67mm
OCP = ~1.75mm
Systems Management Overview

- **Power**
  - AUX mode and MAIN mode power requirements contained in the FRU. Allows system to determine if sufficient power is available prior to moving from ID mode to AUX mode.

- **Thermal**
  - FRU contains worst-case airflow requirements. Allows system to determine if sufficient airflow is possible prior to enabling the adapter.
  - Real-time temperature monitoring of ASIC and Optics (if installed) allow the system to adjust airflow to properly cool the adapter.
Thermal comparison to PCIe and OCP2.0

- OCP 3.0 has significantly less cooling capacity due to topside keepout restrictions.
  - 11.5 mm for OCP 3.0
  - 14.67 mm for PCIe CEM
- Tiers have been added to PCIe SIG to allow for ease of design-in and a placeholder table is in the draft OCP 3.0 specification pending further analysis.

<table>
<thead>
<tr>
<th>OCP PCIe 3.0 Local Inlet Temperature [°C]</th>
<th>Tier 1</th>
<th>Tier 2</th>
<th>Tier 3</th>
<th>Tier 4</th>
<th>Tier 5</th>
<th>Tier 6</th>
<th>Tier 7</th>
<th>Tier 8</th>
<th>Tier 9</th>
<th>Tier 10</th>
<th>Tier 11</th>
<th>Tier 12</th>
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</table>

Table 59: Hot Aisle Card Cooling Tier Definitions (LFM)

*Work in Progress*
SFF Hot Aisle Thermal restrictions

- Hot aisle simulations show 85°C optics required with 400 LFM for QSFP
- SFP simulations only require 250 LFM
Validation: Thermal
Goal: Standardize Thermal Validation for OCP

• Deterministic and standardize methodology across compute and storage platforms
  - Enabling both OCP Mezzanine v2.0 and v3.0
• Enable interoperability across Mezzanine add-in cards (NIC) and platforms
• Open sourced to OCP Community to enable independent qualification
  - System vendors
  - 3rd party labs
  - Mezzanine add-in card vendors.
• Design can be customized to adapt to different thermal test configurations.
Thermal Validation Test Fixture

- 3D Models released on Wiki
- Initial PCIe Gen4 capable schematic/layout/gerber package is posted for community feedback
- Allows validation of the OCP 3.0 card with/without the presence of a PCIe adapter immediately above the card.
- Correlation at the system level will allow a system designer to support 3rd party cards using FRU information.
Validation: Electrical: PCIe
Goal: Standardize PCIe Conformance for OCP

• Deterministic and standardize methodology across compute and storage platforms
• Enable interoperability across Mezzanine add-in cards (NIC) and platforms
• PCIe Gen3+ interoperability and conformance
• Open sourced to OCP Community to enable independent qualification
  – System vendors
  – 3rd party labs
  – Mezzanine add-in card vendors.
• Full integration with standard industry equipment
Methodology

• Road to formalize conformance guidelines for OCP 3.0
  - Use OCP 2.0 systems as enablement platform
  - Incorporate SI guidelines and requirements into OCP 3.0 specifications
  • Target v0.9

• Cross community collaboration
  - Platform developers
  - NIC Developers
  - Test equipment vendors

• Integrate test solution with test equipment for automation
OCP vs PCI-CEM (Gen3+) Conformance Testing

- OCP 2.0 vs PCI-CEM

<table>
<thead>
<tr>
<th>Attribute</th>
<th>OCP</th>
<th>PCI-SIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>1-3 Connectors</td>
<td>1-2 Connectors</td>
</tr>
<tr>
<td>Connector Z-height</td>
<td>3x versions (5mm, 8mm, 12mm)</td>
<td>1</td>
</tr>
<tr>
<td>System Loss</td>
<td>~14.5dB</td>
<td>~12dB</td>
</tr>
<tr>
<td>AIC Form-Factor</td>
<td>Mezzanine</td>
<td>CEM</td>
</tr>
</tbody>
</table>

*Source: Keysight*
OCP Conformance Guideline

- Key conformance parameters
  - Tx SQ at far-end (Rx pins)
  - Rx sensitivity and jitter tolerance
- Acceptance guideline
  - Meet PCI-SIG Rx requirements at far-end
  - BER with Stressed Jitter Eye

*Source: PCI Express® Base Specification Revision 3.0
OCP Conformance Testing

- Test fixtures
  - Base board
  - Load board
  - Calibration board
- Conformance Measurement setup
  - Calibration
  - Test
  - SigTest Processing for Tx
- Embed loss (pkg + worst channel)
OCP PCIe Test Fixtures

- OCP 2.0
  - Compute and Storage
  - 3x sets
    - Load Board
      - Type A
      - Type B
    - Base Board
      - Calibration
OCP3.0: Test Fixtures

Load Board (1 of 4)

Base Board

*Courtesy: Dell-EMC
Fixture Design

- Design
  - Material
    - OCP2.0
      - TU862 for BB and TU883 for LB
    - OCP3.0
      - TU863 for BB and TU883 for LB
  - Equal length channels
    - All Tx/Rx channels, including calibration
  - Clock trigger/power delivery similar to PCI-SIG CLB/CBB fixtures
OCP2.0 PCIe Test Fixtures: Loss Characteristics

<table>
<thead>
<tr>
<th>Test Fixture</th>
<th>Design Target (with Connectors)</th>
<th>Measured * (with Connectors)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseboard</td>
<td>-14.75dB</td>
<td>-14.5 dB</td>
</tr>
<tr>
<td>Load Board Type A</td>
<td>-3.45dB</td>
<td>-3.52 dB</td>
</tr>
<tr>
<td>Load Board Type B</td>
<td>-3.45dB</td>
<td>-3.24 dB</td>
</tr>
</tbody>
</table>

* Sample average
OCP2.0: Assessing Channel Margin

- Channel Margin
  - Per Simulation
    - AIC: -4.43dB
    - System: -14.93dB
  - Per Measurement
    - Under work

<table>
<thead>
<tr>
<th>Topology</th>
<th>EH(mV) BER@e-12 (CEM:34mv)</th>
<th>EW(ps) BER@e-12 (CEM:41.25ps)</th>
<th>Jitter PP/RMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT NIC + Mezz Connector + Baseboard + SMP + Rx pkg</td>
<td>48mv (TXEQ:P7)</td>
<td>66.88ps</td>
<td>46.88/7.37 (ps)</td>
</tr>
<tr>
<td>Yosemite V2 + Mezz Conn + LoadBoard + SMP + Rx pkg</td>
<td>39mv (TXEQ:P8)</td>
<td>61.87ps</td>
<td>46.88/7.63(ps)</td>
</tr>
</tbody>
</table>
Calibration Board

Characterize channel loss of test boards to enable AFR (Automatic Fixture Removal)

- Design replica channel of test fixture
  - 2-L philosophy
    - Board built on same panel as test board
    - Serialization with test board
    - Reference Channel
- Advantage
  - Characterize individual test board
  - Accurate loss embedding

Serialization of Test Board, Calibration and Coupons
Calibration Design and Configuration

- **Replica Channel**
  - 2-L measured insertion-loss
  - Divide by 2 to obtain loss for individual board
- **Single Differential channel**
  - All Tx/Rx channels equal length within < 1%
- **1:1 association with test board**
  - Same panel and serialized
OCP2.0: Fixtures and Platforms

Bryce Canyon with LB A

Yosemite V2 with LB B

Mezzanine NIC with BB
PCle Conformance Testing for OCP platforms: Rick Eads, Keysight
PCIe Physical Layer Compliance

• Focus is on the interoperability predictors
  − Signal quality
  − Receiver testing
• The PCIe Base Specification architecture
  − Transmitter (TX)
  − Receiver (RX)
  − Channel
• Three main PCIe Spec Documents
  − PCIe BASE Specification (BASE Spec)
  − PCIe Card Electromechanical Specification (CEM Spec)
  − PCIe Test Specification (Test Spec)
PCIe Channels Drive Spec Definition

Target Client Topology

10”, 1 connector
4-layer microstrip

<table>
<thead>
<tr>
<th>Seg</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>RC PKG (transmitter)</td>
</tr>
<tr>
<td>B</td>
<td>RC break-out ~1”</td>
</tr>
<tr>
<td>C</td>
<td>MB Main 3-7”</td>
</tr>
<tr>
<td>D</td>
<td>MB coupling cap</td>
</tr>
<tr>
<td>E</td>
<td>Add in card break in 3”</td>
</tr>
<tr>
<td>F</td>
<td>EP break-out</td>
</tr>
<tr>
<td>G</td>
<td>EP PKG (receiver)</td>
</tr>
</tbody>
</table>

Target Server Topology

Stripline with via stubs
6-8 layers, ””, 1 or 2 connectors

20” Length for RX-TX
PCle Transmitter Test

Post Processing S/W + Embed Package Model + Embed Reference Channel + Apply behavioral EQ

Oscilloscope

PCIe Connector

CBB 3.0

Motherboard

CLB 3.0

Ref Clk

TX

Post Processing S/W + Embed Package Model + Apply behavioral EQ

Oscilloscope
Conventional TX Test Setup

Add-in Card Test Example

Motherboard Test Example
PCle 3.0 Test Procedure

1. Setup DUT connection to Instrument
   - Calibrate and de-skew cables/connectors
2. Confirm Compliance Pattern at 8GT/s
3. Capture waveform on instrument
   - Differential TX signal for AIC test.
   - Differential TX and CLK signal for Motherboard test.
4. Post Process Data
   - Load data waveform in Sigtest (v3.2.0)
5. Change physical connection to next lane and repeat
PCIe Compliance Patterns

2.5GT/s Compliance Pattern

5GT/s Compliance Pattern

8GT/s Compliance Pattern

2.5GT/s Transition Eye

5GT/s Transition Eye

8GT/s Transition Eye
AIC Rx Test Setup

- RX Testing required for 8GT/s
- Measurement Method
- BERT Based stressed jitter test

Stressed Eye: 8G: 25mV, 16G 15mV EH
PCIe 3.0 Jitter Transfer Measurements

• Shows sensitivity of DUT TX output to Jitter on Reference Clock
• Requires the ability to drive a precision modulated, external reference clock

Recommended Equipment:
• Keysight 81150A, 81160A ARB or N4903B J-BERT
• Keysight 86100C DCA-J or N4877A CDR+DeMux
• Keysight 8108A Precision Waveform Analyzer (or 83496B Clock Recovery Module)
• Access to TX and Reference Clock of DUT

Steps:
• Calibrate Jitter Source to CDR module.
• Set target device into Gen2 Compliance mode
• Run Keysight 86100CU-400 PLL and jitter spectrum measurement software
• Record PLL Response

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<table>
<thead>
<tr>
<th>Standard</th>
<th>PLL BW</th>
<th>Peaking</th>
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</thead>
<tbody>
<tr>
<td>PCIe 1.1</td>
<td>1.5MHz-22MHz</td>
<td>3dB</td>
</tr>
<tr>
<td>PCIe 2.0 (5GT/s)</td>
<td>5MHz-16MHz</td>
<td>1dB-3dB</td>
</tr>
<tr>
<td>PCIe 3.0 (8GT/s)</td>
<td>2MHz-5MHz</td>
<td>2dB-1dB</td>
</tr>
</tbody>
</table>
PCIe 4.0 TX Measurement Test Setup - ASIC

- BASE Spec

PCIe 4.0 ASIC/IC Custom Breakout Board

- Keysight Z-Series Real Time Oscilloscope

S-Parameters of Replica Ch. Used to de-embed to pin or Ref CTLE can be used (12dB).
Keysight PCIe 4.0 (Gen4) TX N5393F Test Applications

- New Test Plan Setup
- Select Standard Version to Test
- Select Speeds of Gen4 Device to Test
- Automatic DUT control for toggle signal
PCIe 4.0 RX Stress Signal Calibration

- 16 GT/s Receiver Stress Signal Calibration Setup – 2

PCIe Base Specification 4.0 requires a CEM connector to part of the test channel!
PCIe 4.0 – 16 GT/s CEM Test Setup

- Calibration Setup for 16 GT/s RX

- CBB 4.0 as well as CLB 4.0 need to be combined with ISI trace boards
- CEM calibration procedure is very similar to base spec calibration but SIGTEST instead of SEASIM is mandatory
- J-BERT M8020A successfully tested most of the 16 GT/s AICs and systems at PCIe WS 101
- Many AICs and systems could be trained to loopback using the new LTSSM
RX-TX Test Summary

• PCIe Gen4 RX and TX test tools available today (BASE Spec)
• PCIe Gen4 CEM test fixtures still awaiting full release from PCISIG. Early previews available from Keysight.
PCle – Keysight Total Solution PCIe 3.0-4.0

**Physical layer – interconnect design**
- ADS design software
- 86100D DCA-J/TDR
- E5071C ENA option TDR
- Industry’s lowest scope noise floor/sensitivity and trigger jitter

**Physical layer-transmitter test**
- 90000 V-Series oscilloscope
- N593F PCIe electrical compliance software
- 86100CU-400 PLL and Jitter Spectrum Measurement SW
- DSA-X Series & V Series Real-Time Oscillosopes

**Physical layer-receiver test**
- M8020A J-BERT High Performance BERT
- N5990A automated compliance and device characterization test software
- Automated compliance software – accurate, efficient and consistent

**Data link/transaction layer**
- Digital Test Console
  - U4301A Protocol Analyzer
  - U4305A Exerciser
  - Protocol Test Card
  - Multiple probes with ESP technology
- X1 through x16 Analysis and Exerciser support, with industry’s only ESP probing technology
- Automated compliance software – accurate, efficient and consistent
For further information

You will find more information on PCIe 3.0 and Keysight solutions for PCI Express at:

<table>
<thead>
<tr>
<th>Website</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><a href="http://www.Keysight.com/find/pciexpress">www.Keysight.com/find/pciexpress</a></td>
<td>Keysight tools to help you succeed with your PCI Express design such as the N5393C Compliance application.</td>
</tr>
<tr>
<td><a href="http://www.Keysight.com/find/si">www.Keysight.com/find/si</a></td>
<td>Keysight tools to help you master signal integrity challenges.</td>
</tr>
<tr>
<td><a href="http://www.Keysight.com/find/PCIe_receiver_test">www.Keysight.com/find/PCIe_receiver_test</a></td>
<td>PCIe 3.0/4.0 Rx Test Information</td>
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Future Work
Future Work

- OCP 3.0 NIC Design
- Validation
  - Thermal
  - Electrical
- PCIe Conformance Testing for OCP 3.0
OCP 3.0 NIC Design

• Continue driving specification to 1.0 by EOY 2018 closing open items
  - Thermal correlation with the test fixture (SFF an LFF)
  - Electrical characterization of 3.0 PCIe test fixtures
• Formalize OCP 3.0 channel guidelines (Target v0.9)
  - Platforms
  - Add-in Cards
Validation: Electrical: OCP 3.0

• Release Conformance guidelines
  • Communicate plan by end of March 2018
  • Incorporate details as part of v0.9 (Target August 2018)
    - Including acceptance criteria
    - Fixture design and release

• Engage 3rd Party Lab
  - UNH-IOL

• Enable Test automation
  - Similar to conventional PCI-CEM
  - AFR, embedding models, test equipment setup etc.
Validation: Electrical: OCP 2.0

- Release guidelines
  - Target: 2Q18
  - Establish acceptance criteria
  - Finalize conformance guidelines
- Fixture design
  - Schematics, layout
  - Channel simulations
  - BOM
  - Component data sheets
  - Fixture validation reports
  - Supporting documentation (test reports, specifications, datasheet etc.)
- Schedule
  - OCP 2.0: 2Q18
PCIe Conformance for OCP 3.0

• Leverage CEM 4.0
  – Testing methodology
  – Test Fixture design, only modified for Form Factor
• Define testability features to simplify/automate testing
• Enable 3rd party conformance testing worldwide
• Follow PCIe Gen 5 roadmap for future inclusion if technically feasible
  – 0.9 Gen 5 PCIe spec estimated at Q3 2019
  – Signaling rate: 32 GT/s NRZ
  – Proposed channel loss target is: -36dB @ 16GHz
Keysight tools for PCIe 5.0

TX Testing and RX Testing

**DSA534A Z-Series Real Time Oscilloscope**
- Bandwidth up to 63GHz
- Low noise

**M8040A High Performance 64Gbaud BERT**
- Data rates up to 64GBaud
- NRZ and PAM4 capable
- 4 tap de-emphasis
- Integrated Jitter injection
Don’t miss the Demo