Data Analysis of Manufacturing Test Results for DRAM Module

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What Wiwynn Does?

- **Labs**
  - Optimize parameters of tests
  - Optimize pass criteria
  - Failure analysis

- **Factories**
  - Billions of test log entries every year

- **Datacenters**
  - Monitoring
  - Diagnosis
  - Auto-Healing
  - Wear prediction

- **Test Software**
  - Better design for good MTBF

- **Data Analytics**
  - Enhanced serviceability with diagnosis/healing knowledge

**Solid domain knowledge and experiences + data scientists**
# Failure Rates with Different DIMM Sizes

## 3 Million DIMMs

<table>
<thead>
<tr>
<th></th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>32GB</strong></td>
<td>Test Qty</td>
<td>1M-2M</td>
<td>0.1M-0.5M</td>
</tr>
<tr>
<td></td>
<td>Failure  rate</td>
<td>0.12%</td>
<td>0.15%</td>
</tr>
<tr>
<td><strong>16GB</strong></td>
<td>Test Qty</td>
<td>0.1M-0.5M</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>Failure  rate</td>
<td>0.07%</td>
<td>N/A</td>
</tr>
<tr>
<td><strong>8GB</strong></td>
<td>Test Qty</td>
<td>0.1M-0.5M</td>
<td>0.1M-0.5M</td>
</tr>
<tr>
<td></td>
<td>Failure  rate</td>
<td>0.06%</td>
<td>0.07%</td>
</tr>
</tbody>
</table>
# Failure Rates with Flash Storage

Over 770k Modules

<table>
<thead>
<tr>
<th>Test Qty</th>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;10K</td>
<td>0.08%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&gt;400K</td>
<td></td>
<td>0.11%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&gt;50K</td>
<td></td>
<td></td>
<td>0.10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&gt;50K</td>
<td></td>
<td></td>
<td></td>
<td>0.14%</td>
<td></td>
</tr>
<tr>
<td>&gt;100K</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.05%</td>
</tr>
</tbody>
</table>
# Failure Rates with Hard Disks

**Over 2 million Hard Disks**

<table>
<thead>
<tr>
<th>Test Qty</th>
<th>D1</th>
<th>D2</th>
<th>D2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Qty</td>
<td>0.5M-1M</td>
<td>1M-2M</td>
<td>&lt;0.1M</td>
</tr>
<tr>
<td>Failure rate</td>
<td>0.07%</td>
<td>0.042%</td>
<td>0.039%</td>
</tr>
</tbody>
</table>
Reliability Engineering of DIMMs

Great impact and difficult to control in production test:

- Difficult to define the golden testing time
- To define the error threshold in the testing time is an open problem
- Require several testing to confirm the defect DIMM modules.
The Stress Test Process for DIMMs

Software

• Run utility to test DIMMs and save logs to SEL (system event log) if any ECC error occurred.

• STRESSAPPTEST version 1.0.3_autoconf, 64 bit binary, Resource: opensource.google.com
Testing Model

Variables and Criteria

- Check error-correcting code (ECC) errors in system events log (SEL)

- Testing Time: $t_d$ (ex. 12 hours)
- Correctable ECC error threshold: $E_{max}$ (ex. 6)

- Not Defect DIMM
  - No uncorrectable ECC errors
  - Less than $E_{max}$ errors in total testing time $t_d$
Data Observation

Dataset

- We test over 80K DIMMs installed on 10K systems in a limit time period

Preliminary Observation of DIMMs Quality

- At least one ECC error occurred in testing

<table>
<thead>
<tr>
<th>Vendors</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC Error Rate</td>
<td>0.43%</td>
<td>0.50%</td>
<td>0.30%</td>
</tr>
</tbody>
</table>
**Data Observation**

**Time Distribution of The First ECC Error**

The $x$ axis is the normalized time and the $y$ axis is the count of DIMMs which have their first ECC error occur at that time.

The $x$ axis is the normalized time and the $y$ axis is the count of DIMMs which have their first ECC error occur at that time.
Data Observation

Dataset

- We normalized the total test time in field to 1000 time units for this analysis.
- At least one ECC error in testing
- In limit testing time data, Weibull distribution could predict the global coverage rate.
  - $\beta$: 80% coverage at 311 normalized time point
  - $\gamma$: 90% coverage at 444 normalized time point
The Overview of Recurrent ECC Errors

Time segment distribution between $1^{st}$ ECC and $E_{max}^{th}$ ECC errors (only show < 25 normalized time)
Error Types: Spike and Sparse

The Bucket

We used the average-linkage hierarchical clustering to analyze the error time segment.

A big portion of DIMMs reach their $E_{max}$th ECC error occurrence within 3.5 normalized time after their first ECC error occurrence.
Error Types: Spike and Sparse

The Spike Error Type DIMM

The Sparse Error Type DIMM

<table>
<thead>
<tr>
<th>ECC error type</th>
<th>Spike (&lt;=3.5)</th>
<th>Sparse (&gt;3.5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Percentage</td>
<td>52.55%</td>
<td>47.45%</td>
</tr>
</tbody>
</table>
Spike Assessment

Weibull Distribution with 1^{st} ECC Error Event Time Point of the Spike Type

$\alpha$: 50% coverage
$\beta$: 80% coverage
$\gamma$: 90% coverage
Sparse Assessment

The 1\textsuperscript{st} ECC Error Time Distribution

The $E_{max}$\textsuperscript{th} ECC Error Time Distribution

Weibull Distribution with 1\textsuperscript{st} ECC and $E_{max}$\textsuperscript{th} Error Event Time Point of the Sparse Type

$\alpha$: 50% coverage, $\beta$: 80% coverage, $\gamma$: 90% coverage
Our Purpose

Shorten the testing time but maintain quality

It is straightforward to just cut testing time and raise the threshold as compensation.

However, the benefits of less test time will be offset by less error coverage and increased false alarms.
Model Evaluation

Variables and Criteria

- Testing Time, ECC Error Threshold: \((t_d, E_{\text{max}})\)
- Defect DIMMs Judged by The Original Criteria \((t_d, E_{\text{max}})\): \(D_o\)
- Not Defect DIMMs Judged by The Original Criteria \((t_d, E_{\text{max}})\): \(N_o\)

Catch Rate

- \((\text{Defect DIMMs Judged by New Criteria and Existed in } D_o) / D_o\)

False Alarm Rate

- \((\text{Defect DIMMs Judged by New Criteria and Existed in } N_o) / N_o\)
Analysis of Different Testing Time and ECC error Threshold

Three steps analysis

1. Use trained data (80K) for direct data verification
2. Use the Weibull Distribution to predict criteria
3. Use new data (216K) to cross verify the criteria we predict.
Data Observation – Cross Verification Data

Preliminary Observation of DIMMs Quality

- At least one ECC error in testing (ECC Error Rate)
- More or equal than $E_{max}$ ECC error in the first stress testing (Defect Rate)

<table>
<thead>
<tr>
<th>Vendors</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC Error Rate</td>
<td>0.302%</td>
<td>0.302%</td>
<td>0.168%</td>
</tr>
<tr>
<td>Defect Rate</td>
<td>0.214%</td>
<td>0.23%</td>
<td>0.107%</td>
</tr>
</tbody>
</table>
## Summary

<table>
<thead>
<tr>
<th></th>
<th>Catch rate</th>
<th>Testing time</th>
<th>ECC Error threshold</th>
<th>False alarm rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct verification data</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90%</td>
<td>0.75 t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>0.5 E&lt;sub&gt;max&lt;/sub&gt;</td>
<td>0.016%</td>
<td></td>
</tr>
<tr>
<td>80%</td>
<td>0.5 t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>0.33 E&lt;sub&gt;max&lt;/sub&gt;</td>
<td>0.028%</td>
<td></td>
</tr>
<tr>
<td>Cross verification data</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90%</td>
<td>0.68 t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>0.5 E&lt;sub&gt;max&lt;/sub&gt;</td>
<td>0.036%</td>
<td></td>
</tr>
<tr>
<td>80%</td>
<td>0.51 t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>0.5 E&lt;sub&gt;max&lt;/sub&gt;</td>
<td>0.025%</td>
<td></td>
</tr>
<tr>
<td>Prediction based on Weibull distribution</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90%</td>
<td>0.7 t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>0.5 E&lt;sub&gt;max&lt;/sub&gt;</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>80%</td>
<td>0.49 t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>0.5 E&lt;sub&gt;max&lt;/sub&gt;</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>
The Cost-response Model

Elements of The Cost-response Model

1. **Cost with Catch Rate**
   - RMA Costs
   - Operation Loss for External Customer
   - Reputation

2. **Cost with False Alarm Rate**
   - Additional MoH of Testing Time

3. **MoH of Testing Time**
Conclusion

Implement predictive analytics by analyzing event logs generated from the manufacturing process.

Reduce the number of required test and find the best effective stress test time for different parts and brands.

With the optimized test process, we can improve cost and capacity but still keep high quality level.
How Do You Benefits from Data Analysis?
Smart Way to Improve Testing Time and Key Component Quality

Find out more about the manufacturing test results for DRAM Module

Download Whitepaper
White Paper

http://www.wiwynn.com/ usr_files/Wiwynn_Data_Analysis_Whit epaper.pdf