

vE-CPE – Denverton – Extra Small

Technical Specification of Extra Small vE-CPE

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1 Introduction

This document provides technical details on the platform

1.1 OEM specification

Feature:	
CPU:	C3558, 4 cores, Base Freq. 2.2GHz, 8MB, TDP 16W
BIOS:	UEFI
BIOS Flash:	
Operating System:	Vyatta OS
Memory	8GB Memory Down with ECC. (Platform supports up to 16GB memory down and an optional SODIMM that also supports up to 16GB)
Storage	64GB eMMC
Internal Switch	2x2.5Gb KR between CPU and Switch 1x1GbE between uBMC and Switch
External Switch	Marvell 88E6190X (X required for SFP) 4x1GbE 2x1GbE (POE+) 2xSFP
Host Mgmt.	1GbE RJ45 on Management Card. Shared with BMC. Intel i210. 1GbE Between uBMC and Switch
USB 3.0	2xFront, 2xInternal
Serial Console	RJ45 RS232 Console
LTE	M.2 Key-B, support 3042 Card. Externally accessible SIM card supported. Or Mini PCIe slot with externally accessible SIM card
WiFi	Mini PCIe Slot for WiFi.
M.2 Expansion	M.2 Key B with support up to 30x110mm. Currently used for M.2 Storage Note: There is a board population option to support USB to the card for the possible IoT card. The default build option is not to support this feature.
BMC	µBMC. See uBMC specification for additional details

TPM	TPM 2.0
Power	12V@60W External Power Adapter with locking connector. Dying Gasp supported on BMC. 54V@65W External Power Adapter with locking connector for POE+ ports
LED's	Management card support three tri-color configurable LED's (red, green, blue)
Other Hardware:	Configurable Recessed button (Recommend for Factory reset) Configurable Large button (Recommend for power) Optional Buzzer
Form Factor:	Desktop Form Factor (WxDxH) = 223x305x44mm Supports two side by side in 19" rack Rack Mount Option Wall Mount Option Branding Option
Display Port:	
Weight:	2.2kg (77.60oz) without optical modules
Input Power: Tolerances:	
Power Consumption:	Maximum Input 1: 110Vac / 1.8A ~ 240Vac / 0.8A, 50Hz to 60Hz Output 1: 12V / 5A Input 2: 110Vac / 1.8A ~ 240Vac / 1.2A, 50Hz to 60Hz Output 2: 54V / 1.2A Typical: Input 1: 110Vac / 0.47A ~ 240Vac / 0.3A, 50Hz to 60Hz Output 1: 12V / 2.12A Input 2: 110Vac / 1.2A ~ 240Vac / 0.8A, 50Hz to 60Hz Output 2: 54V / 1.1A

	The total power consumption of the card depends on user application
Cooling:	- 12VDC 40mmx40mmx20mm 10.1 CFM FAN. - Built-in thermal protection
Sensors/Monitors:	- Thermal monitors - Critical Error Detection - Voltage monitors - Current protection
Operating Temperature:	0°C – 40°C (32°F - 104°F)
Storage:	-40°C–65°C (-40°F–149°F)
Operating Altitude	10000 ft (3048 m)
Regulation:	CE EN 55032: 2012 + AC: 2013 Class B EN55024: 2010 IEC 61000-4-2: 2008 IEC 61000-4-3:2006 + A1: 2007; A2: 2010 IEC 61000-4-4: 2004 IEC 61000-4-5: 2005 IEC 61000-4-6: 2008 IEC 61000-4-11: 2004 FCC Subpart B Class B, ANSI C63.4-2014 CB Scheme IEC 60950-1:2005 (second Edition) + Am 1:2009 + Am 2:2013, EN 60950-1:2006+ A11:2009+ A12:2011+ A1:20010+ A2:2013 UL 60950-1 & CAN/CSA C22.2 No. 60950-1-07 – Information Technology Equipment – Safety – Part 1: General Requirement ROHS requirements
MTBF*:	143887.77 hours * According to Telcordia SR-332 Issue 4. Environmental condition – GB (Ground, Fixed, and Controlled). Ambient temperature 40°C

2 OEM Ordering Information

2.1 Ordering Information

P/N	Description	RMN	RTN	Notes:
80500-0150-G05	Shippable Kit: uCPE, Desktop, XS Module, Empty Right Slot, C3558 (4C), DDR4 8GB ECC, EMMC 64GB, including +12V, +54V Power supplies	IA3000	IA3000.01	Top level – Shippable kit, including packaging, GA

80500-0150-G07	Shippable Kit: uCPE, Desktop, XS Module, Empty Right Slot, C3758 (16C), DDR4 16GB ECC, M.2 SSD 256GB, including +12V, +54V Power supplies	IA3000	IA3000.02	Top level – Shippable kit, including packaging, GA
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2.2 Packing list

P/N	Item	Descriptions.
	1 x 80500-0150-G0x	vE-CPE, Desktop, VECPE-XS-SIL
EPS000014	1 x PoE Power supply	POWER SUPPLY: EXT DESKTOP, 54V POE, 65W, LATCHI
EPS000015	1 x 12V Power Supply	POWER SUPPLY: EXT DESKTOP, 12V, 60W, LATCHING AT
CPW000010	1 x Power Cord	POWER CORD, AC, 120V, 18AWG, 3COND, M/F, NEGA 5-15P
CBL000077	1 x USB to RS-232 adapter	Cable,USB2 to RS-232 Cisco pinout,RJ-45 console

2.3 Accessories - Optional items

P/N	Descriptions.
K#VE-CPE-MECH	Kit for rack mount brackets
K#VE-CPE-MECH-NO-PS	Kit for rack mount brackets without PS support
K#VE-CPE-MECH-WALL	Kit for wall mount bracket

System level Diagrams

2.4 Top level block Diagram

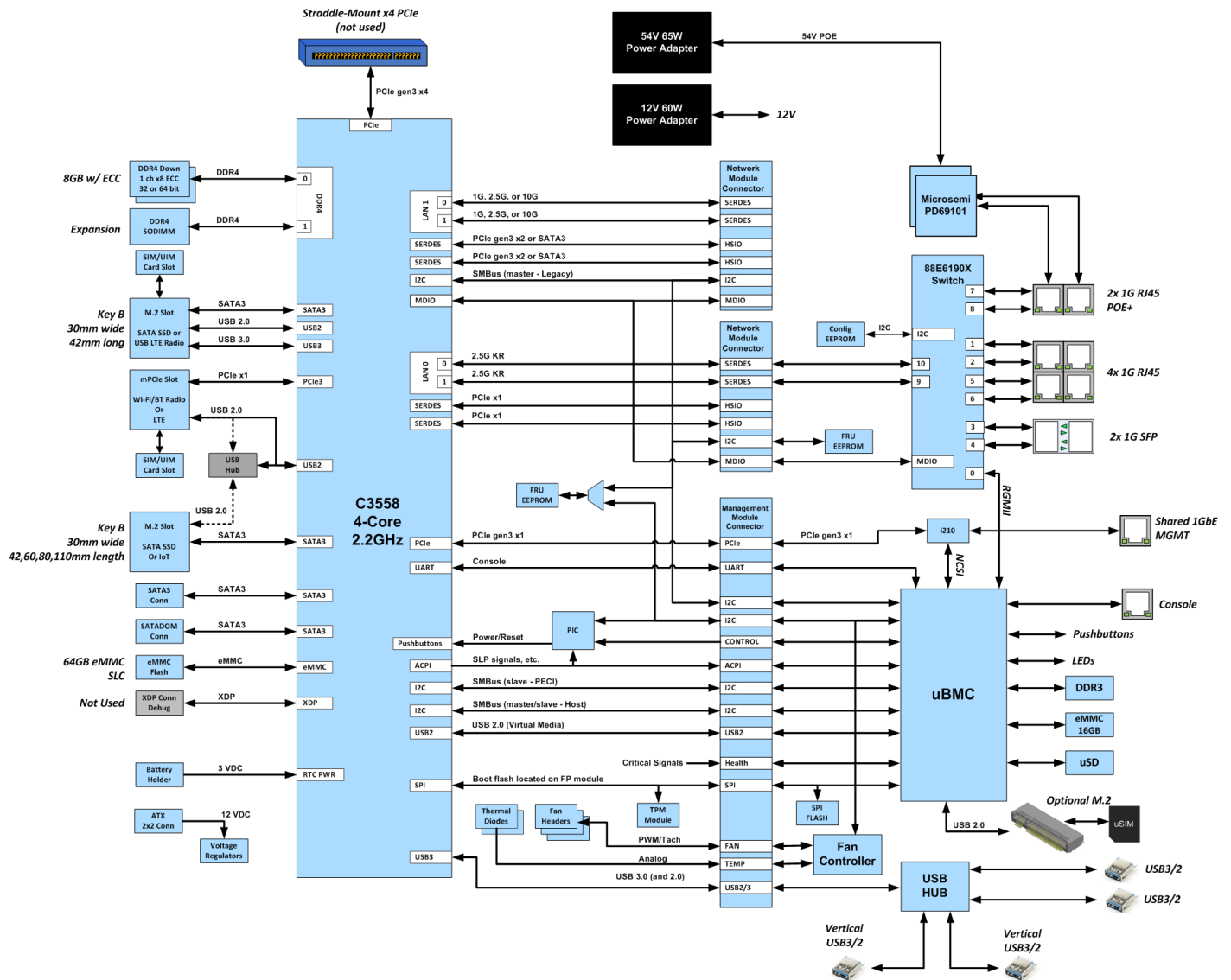


Figure 1 uCPE XS Block Diagram

2.5 Front IO

vE-CPE Enclosure
AT&T-XS Front Panel
Silkscreen Artwork
Silicom Connectivity Solutions
Scale 1:1

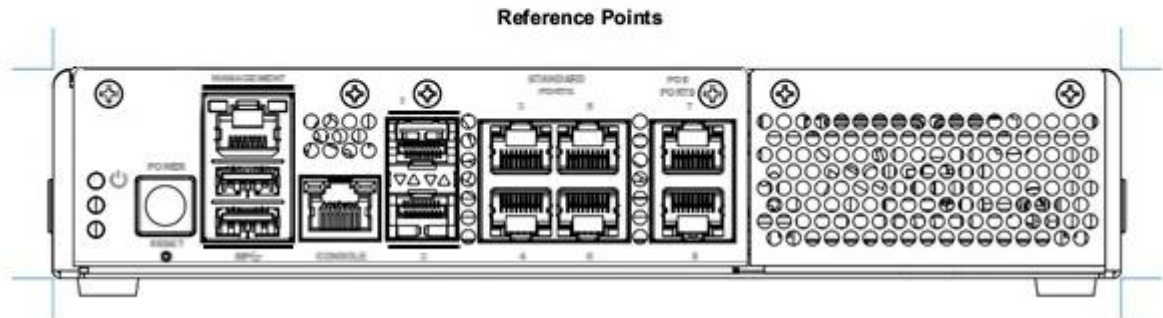


Figure 2 vE-CPE Front IO

3 Compute Board

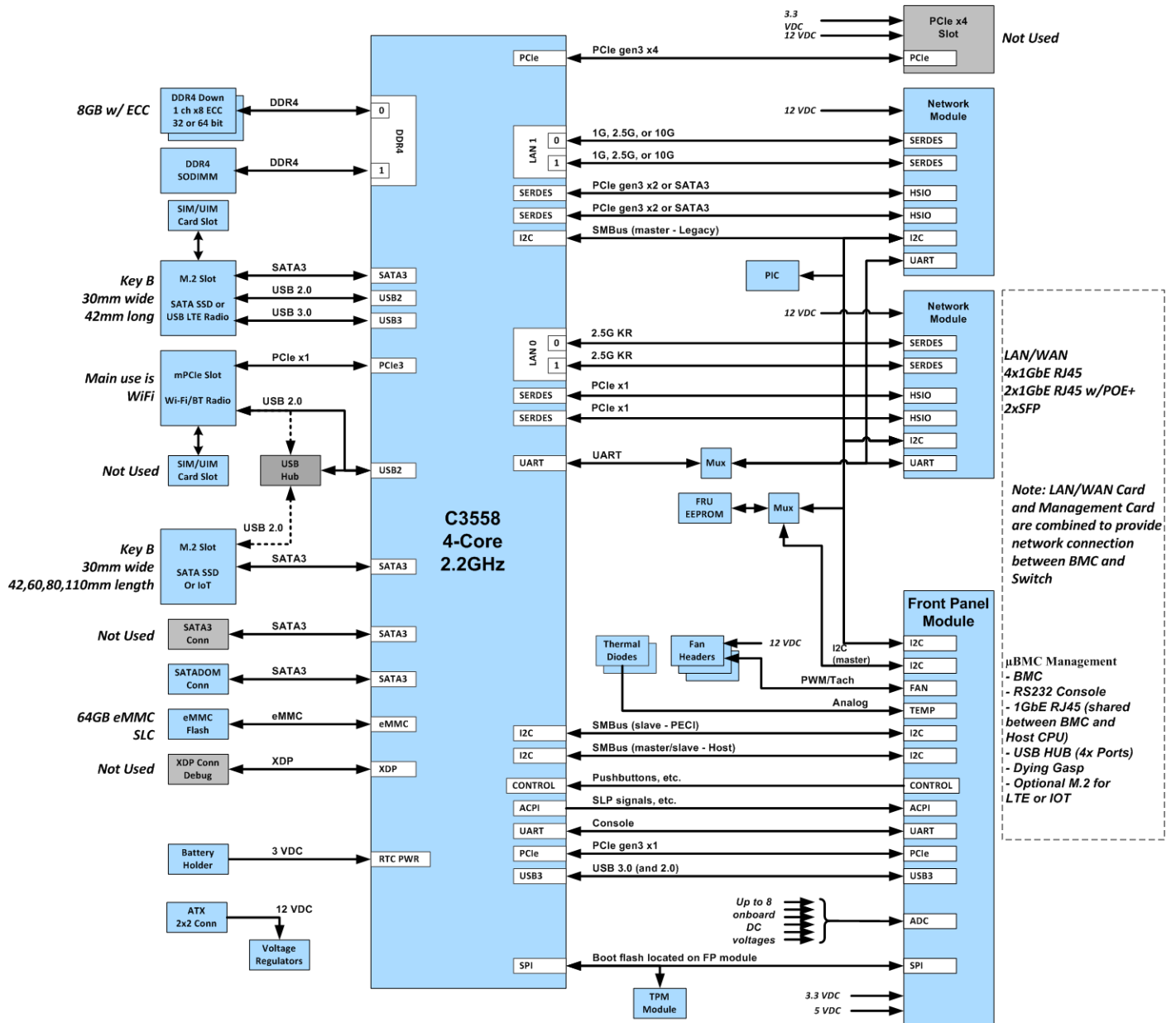


Figure 3 Compute Board Block Diagram

3.1 CPU

The compute boards support all SKU's of the Intel C3000 SoC. The XS uCPE will use the C3558 which is a 2.2Ghz, 4-core SoC with QAT.

3.2 CPU HSIO

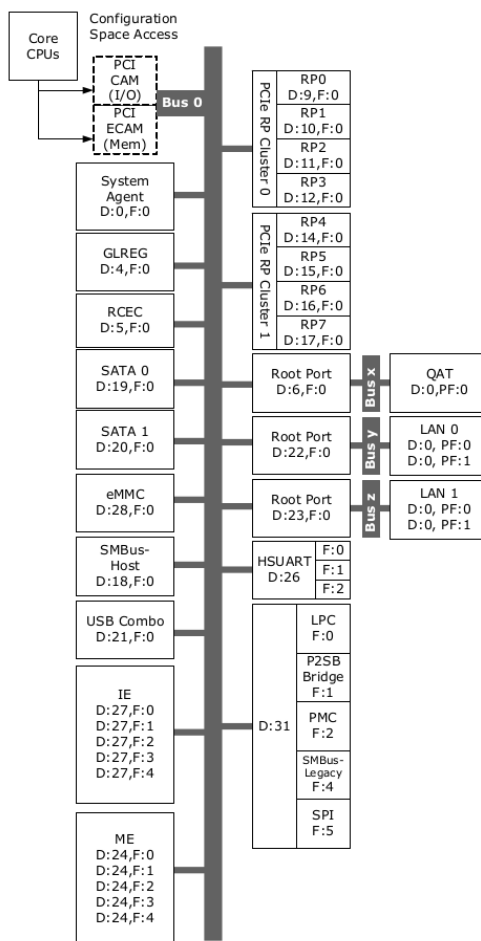
The Intel C3000 CPU supports HSIO which are I/O that can be configured as PCIe, SATA, or USB3.0. The C3558 CPU can support up to 12 HSIO. The options for HSIO are listed below along with how they will be configured on the XS uCPE. Note that the 12 selected can be changed if needed. This configuration is set by the CPU bootloader.

HSIO	PCleRoot ² Cluster ¹⁰	PCleRoot ² Cluster ¹¹	SATA Controller ¹⁰	SATA Controller ¹¹	USB3.0	Xsmall ¹⁰ uCPE	Description
0	0					PCle	
1	1					PCle	PCle ¹⁰ x4
2	2					PCle	Expansion
3	3					PCle	
4	4		0			PCle	
5	5		1			PCle	Network
6	6		2			PCle	Module ¹¹
7	7		3			PCle	
8		0	4			PCle	
9		1	5			PCle	Network
10		2	6			PCle	Module ¹⁰
11		3	7			PCle	
12		4		0		PCle	i210 ¹⁰ MGMT
13		5		1		SATA	M.2 ¹⁰ SSD
14		6		2		PCle	mPCle ¹⁰ WiFi
15		7		3		SATA	M.2 ¹⁰ LTE
16				4	0	USB3	USB ¹⁰ Hub
17				5	1	USB3	M.2 ¹⁰ LTE
18				6	2	SATA	SATADOM
19				7	3	SATA	SATA ¹⁰ Host
USB2.0							
0						USB2	M.2 ¹⁰ LTE
1						USB2	BMC
2						USB2	mPCle ¹⁰ WiFi
3						USB2	USB ¹⁰ Hub

Figure 4 XS uCPE HSIO and USB 2.0 Configuration

3.3 CPU Internal PCI devices

Denverton CPUs have fixed internal PCI devices on Bus 0. PCI/PCIe buses use a Bus/Device/Function triplet to uniquely identify the location of any device in the hierarchy of devices. The figure below shows the list of all possible devices. Throughout this document devices are referenced by their Bus/Device/Function address using the format BB:DD.F, where BB and DD are two digit hex numbers, and F is the function number between 0-7.



Note: Not all devices may be visible depending on SKU, bifurcation, and BIOS settings.

Figure 5 Internal Denverton PCI Devices

3.3.1 CPU GPIO Configuration

Several GPIO signals on the platform are connected directly to the Denverton. There is currently no Linux driver for Denverton GPIO. The GPIO registers are accessible by MMIO at the offsets specified in Figure relative to SBREG_BAR in BDF 00:31.1, see section 26 of the EDS[i] for more details.

GPIO#	Ball	Signal	Pad Config DW0	Pad Config DW1
0	BF70	GPIO_PIC	0xC204D8	0xC204DC
5	BL48	GPIO_FP_0	0xC50570	0xC50574
6	BE52	W_DISABLE_WWAN_N	0xC50578	0xC5057C
7	BH46	W_DISABLE_MPCIE_N	0xC50580	0xC50584
8	BY55	GPIO_FP_1	0xC505C8	0xC505CC
9	CA54	CPU_RSTBTN_PGIO_N	0xC505D0	0xC505D4
10	CA63	MFG_MODE	0xC50710	0xC50714
118	BR46	PIC_PRG_MCLR	0xC50540	0xC50544
150	BM38	SOC_UART1_MUX_SEL	0xC50620	0xC50624
151	BW27	GPIO_NM1	0xC50628	0xC5062C
152	CA37	GPIO_NM0	0xC50630	0xC50634

Figure 6 Denverton GPIO

3.4 Memory

3.4.1 Channel-0

Channel-0 is memory down and supports the following:

- x8 Devices
- Single or Dual Rank
- 32-bit or 64-bit bus
- ECC or non-ECC
- 2GB, 4GB, 8GB, or 16GB

The compute board has a SPD (Serial Presence Detect) EEPROM on the board which is read by the bootloader to get the memory down configuration. The SPD information will be used by the bootloader MRC (Memory Reference Code) to train the memory.

For the XS uCPE, the board will be configured with 8GB DDR4 with ECC in a dual rank (18x4Gb devices).

3.4.2 Channel-1

Channel-1 is an optional SODIMM which can support up to an additional 16GB of memory. If populated, it would support the following:

- x8 or x16 devices
- Single or Dual Rank
- 64-bit bus
- ECC or non-ECC
- 2GB, 4GB, 8GB, or 16GB

3.4.3 Channel-0 and Channel-1 Rules

- Both channels must be 32-bit or 64-bit
- At least 1 memory channel must be populated and enabled. Either channel-0 or channel-1 may be that 1 memory channel
- x8 and x16 devices can be mixed between channel-0 and channel-1
- Both channels must be ECC or non-ECC

3.5 eMMC Storage

The platform supports a soldered down eMMC. The following eMMC's are supported:

- 4GB, 8GB, 16GB, 32GB, 64GB, and 128GB
- eMMC 4.5 and 5.0

The XS uCPE will be populated with a 64GB eMMC.

The eMMC is connected to the native SDHCI in the SoC (BDF 00:1C.0). This device is covered by the standard sdhci-pci driver in Linux. A bug in the driver affecting this platform was fixed in the Linux kernel driver by commit eb701ce16a45ed9880897c48f05ee608d77c72e3 which is present in 4.14-rc4 and later kernels. Without this patch the controller does not retune the delay elements as temperature changes leading to eMMC failures as the board heats.

3.6 SATA Host Ports

The platform supports two 7-pin SATA host ports. One of the SATA host ports supports a SATADOM which is a standard 7-pin SATA host port with built-in 5V power

The platform also supports a 4-pin power connector that would be used to supply 12V or 5V to an offboard 2.5" disk drive.

The SoC contains two AHCI controllers, each of which can control up to 8 SATA lanes depending on the HSIO configuration. The two 7-pin SATA host ports are both connected to the controller located at BDF 00:14.0. Port 6 of the BDF 00:14.0 is connected to J17, and Port 7 is connected to J18. The standard Linux ahci driver works with the controller, and persistent device naming is available by reading the /dev/disk/by-path symlinks to see which /dev/sdx device corresponds to a port.

The udev rules for creating the persistent block device names can typically be found in: /usr/lib/udev/rules.d/60-persistent-storage.rules

3.7 M.2 Expansion

There are two M.2 connectors that are available for expansion options.

3.7.1 Large M.2 Slot

The platform supports a large SATA M.2 Key-B slot. The slot supports widths up to 30mm and supports lengths of 42mm, 60mm, 80mm, and 110mm.

In addition to SATA SSD's, there is a board population option for this slot to support USB 2.0. The USB 2.0 could be used to support a large 30mm x110mm IoT card w. **Currently, this USB 2.0 option is not planned for production.**

The large M.2 slot labelled J20 is connected to SATA controller 1 (BDF 00:14.0) port 1.

3.7.2 Small M.2

The platform supports a smaller M.2 Key-B slot which supports cards 30mm wide and 42mm long. This slot supports the following interfaces:

- SATA
- USB 2.0
- USB 3.0
- Externally accessible micro-SIM card

This slot will typically be reserved for LTE cards but could alternatively be used for SATA SSD.

The small M.2 slot labelled J10 is connected to SATA controller 1 (BDF 00:14.0) port 3.

3.8 Mini-PCIe Expansion

The platform support one mini-PCIe expansion slot. This slot supports the following interfaces:

- x1 PCIe Gen 3
- USB 2.0
- Externally accessible micro-SIM card

This slot will typically be reserved for WiFi/BT cards but could alternatively be used for LTE.

Electrically this slot is connected to root port 7 of PCIe root port cluster 1, any devices connected to this port will be on the secondary bus of BDF 00:11.0

3.9 x4 PCIe Expansion Slot

The platform supports a x4 PCIe Gen3 expansion slot off the side of the board. This slot will not be supported with the 4-core CPU because of HSIO limitations. The connector and power options for this slot **will not be populated in production**.

This slot is connected to root port 0 of PCIe root port cluster 0, any devices connected to this port will be on the secondary bus of BDF 00:09.0

3.10 TPM

The platform supports a soldered down Trusted Platform Module (TPM). The part currently used is an Infineon SLB 9670 which is TPM2.0 compatible. The exact part used is the Infineon SLB9670VQ20FW7.62. The board supports a population option to support an Atmel TPM if necessary.

The TPM is attached the SPI bus with a dedicated chip select, and logic in the SoC forwards any accessed to the TCG defined MMIO space to the TPM as SPI accesses without any additional software overhead. An ACPI device entry for device ID “SMO0768” tells the OS that a SPI TPM is attached, and provides the information needed for the OS to use device. On Linux the standard `tpm_tis_spi` driver will support this device. Section 19.10 of the EDS¹ contains more details of the addressing scheme.

3.11 Debug Port

The platform supports the 60-pin XDP debug connector. This can be used with a Lauterbach debugger. This connector will be available on the prototypes but **will not be populated in production**.

3.12 I2C/SMBus Architecture

The following is the I2C/SMBus architecture for the platform including the front-panel card.

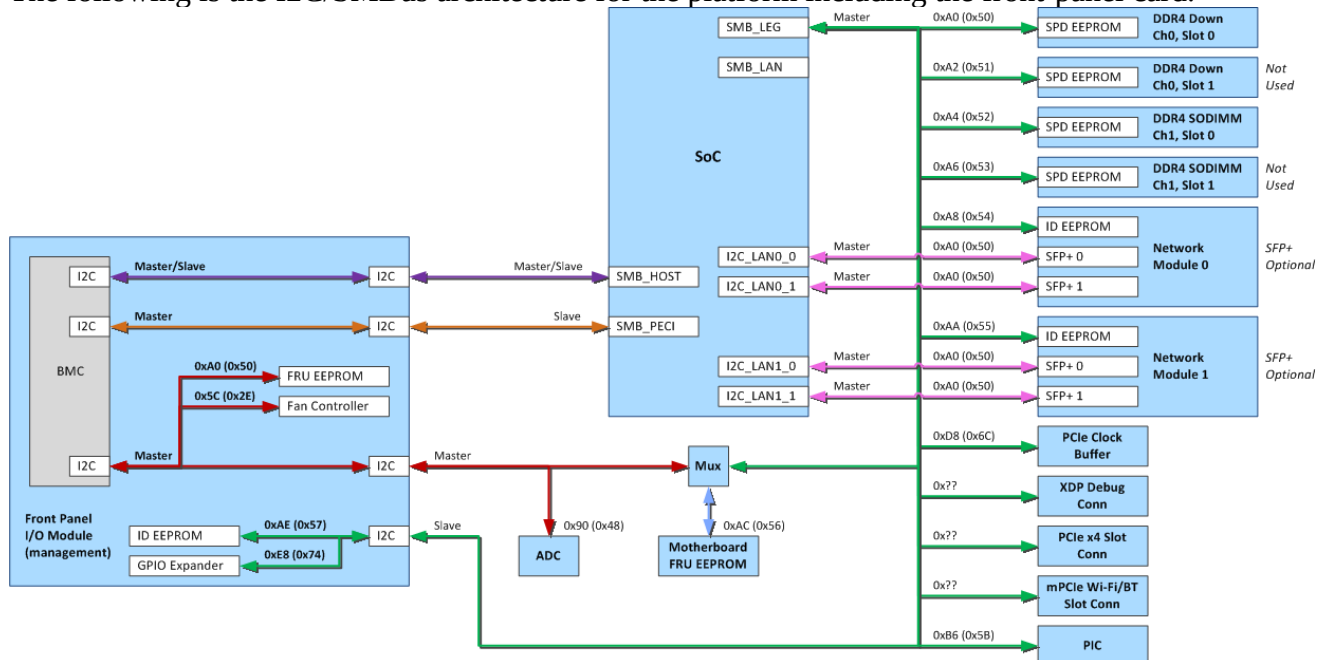


Figure 7 I2C/SMBus Architecture
Figure 8 Compute board i2C/Smbus Architecture

The SMB_LEG device referred to in Figure 8 corresponds to the legacy SMBus controller that is part of the multi-function legacy device known as the Platform Control Cluster (PCC) and can be found at BDF 00:1F.4, and is supported by the standard i2c_ismt driver found in Linux.

The SMB_HOST device referred to in Figure 8 can be found at BDF 00:12.0, and is supported by the standard i2c_i801 driver found in Linux.

The SMB_PECI bus is a SMB slave only interface to the Platform Environment Control Interface (PECI) that allows external devices like BMCs to read thermal status information from the processor without needing to interact with any software running on that processor.

The I2C_LANX_X links to the SFP+ ports are under direct control of the ixgbe driver, and must be accessed through that driver. The ixgbe driver provides ioctl and ethtool access to the information stored in these PROMS.

The various EEPROMs can be queried using tools like i2cdump from userspace, or the Linux at24 driver can be used.

The PCle clock buffer is a IDT 9DBU0531 device. It is not recommended that host software access this device, configuration will be done by the BIOS if needed.

TBD – Need an interface spec for the PIC.

The GPIO expander is a TCA9539, see section 4.7 for details of the GPIO connections. Linux driver support is available via the standard gpio-pca953x driver.

The fan controller is a Microchip EMC2300 part providing 3 PWM fan output with TACH feedback. The part also provides access to two remote thermal diodes as well as a temperature reading of the EMC2300's temperature. External diode 1 is connected to a sensor near the CPU, and external diode 2 is connected to a sensor near the air inlet to the unit. PWM1 is connected to J22, PWM2 is connected to J23, and PWM2 is connected to J24. Currently all 3 fans are 4pole fans. This part is under control of the BMC.

3.13 FRU EEPROM

COMPUTE BOARD FRU EEPROM IS TBD. ONIE STANDARD IS BEING CONSIDERED

3.14 Clock Architecture

The clock architecture for the compute board is shown below. All clocks are configured and enabled by the bootloader.

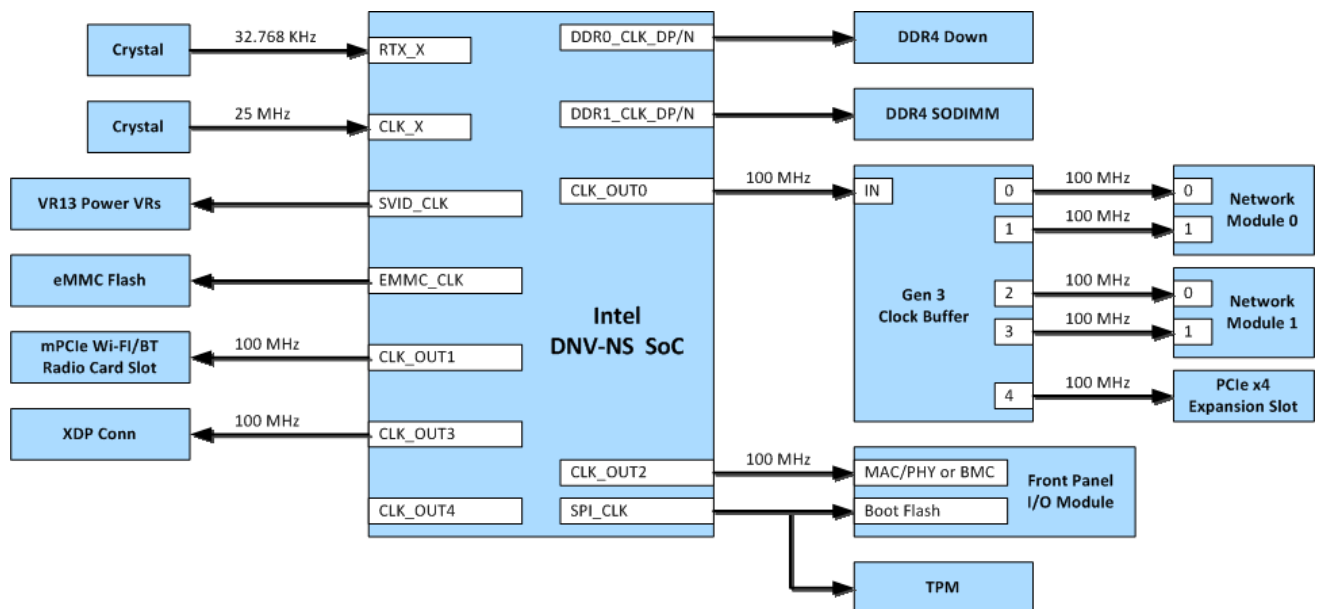


Figure 9 Internal Denverton PCI Devices

Figure 10 Clock Architecture

3.15 Analog-to-Digital Voltage Monitor

The compute board includes an analog-to-digital (A/D) voltage monitor IC. This IC is accessible over the I2C interface (Address 0x90 (0x48)) which is connected to the front panel module. It is intended to be configured and monitored by the uBMC. The A/D used is a TI ADS7830.

Note:

Internal 2.5V reference voltage must be enabled.

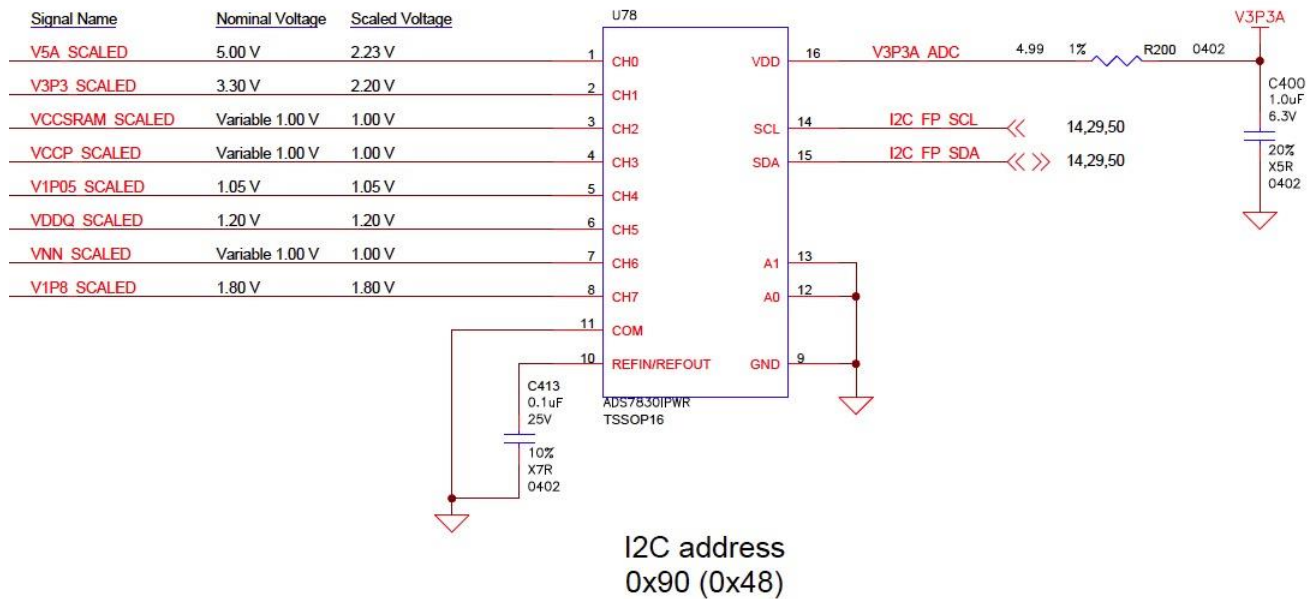


Figure 11 A/D Voltage Monitor

3.16 PIC Microcontroller

There is a low-cost PIC microcontroller on the compute board that is used for the following functions:

- Controls power up/down sequence: The PIC will power up CPU from a cold start. It will then respond to the sleep signals from CPU (S3/S4/S5) and set the power as requested. It will also shutdown the power if a CPU voltage regulator fault it determined. This is a major fault and requires cycling the external power to recover.
- Front Panel reset button control. Currently, the PIC passes the reset button to the host CPU reset button input (PMU_RESETBUTTON_N).
 - Short tap (<7 seconds) will cause platform reset. The PIC will assert reset to host CPU.
 - Long tap (>7 seconds) will be used for resetting to defaults. The PIC will assert an interrupt to the host CPU over GPIO0 (pin BF70 on C3000). The host can acknowledge the interrupt over SMBus interface to PIC.
- Front Panel power button control. Currently, the PIC passes the power button to the host CPU power button input (PMU_PWRBTN_N).
 - Very short tap filter (< 2 seconds) – tap shorter than 2 second will be filtered
 - Short tap (>2 seconds) – initiate graceful shutdown to host CPU
 - Long tap (>13 seconds) – hard shutdown for immediate power off
- Monitors the 12V power rail. When the power starts to drop, the PIC will negate the RSMRST_N to the host CPU.

- The PIC supports a SMB connection to the host CPU. The host CPU can read status and control certain functions through this interface. Register MAP is available upon request.

3.17 Power Architecture

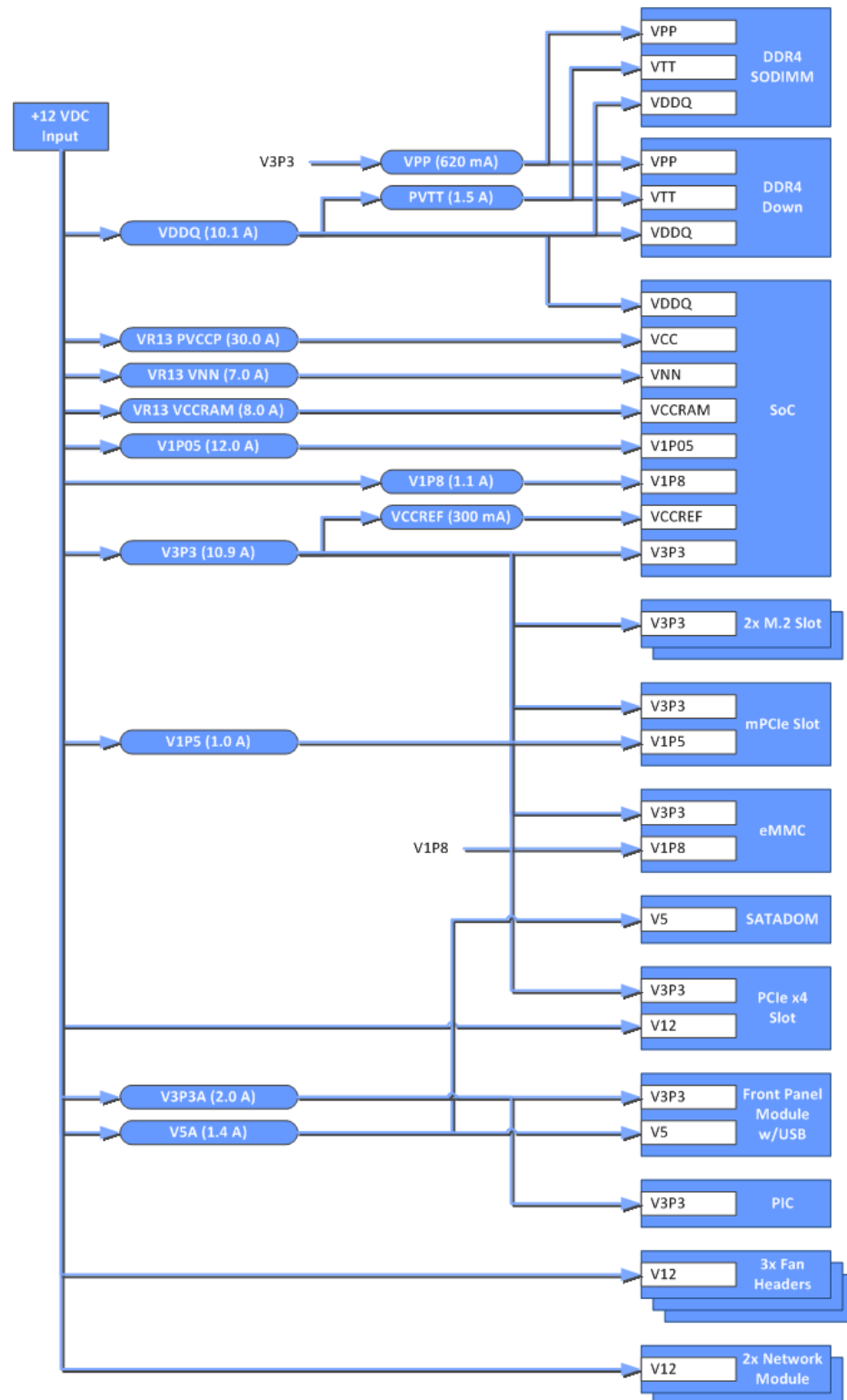


Figure 12 Power Architecture

3.18 Connector Pinouts

3.18.1 Network Module 0 (J4)

Dir	Signal	Pin	Pin	Signal	Dir
PWR	GND	B1	A1	+12 VDC	PWR
PWR	GND	B2	A2	+12 VDC	PWR
PWR	GND	B3	A3	+12 VDC	PWR
-	RFU	B4	A4	LAN0_PORT1_SFP_I2C_CLK	O
I/O	LAN0_PORT0_SFP_I2C_DATA	B5	A5	LAN0_PORT0_SFP_I2C_CLK	O
O	LAN0_PORT0_SFP_LED_SPEED	B6	A6	LAN0_PORT0_SFP_LED_LINKACT	O
O	LAN0_PORT1_SFP_LED_LINKACT	B7	A7	LAN0_PORT1_SFP_PRSENT_N	I
I/O	LAN0_PORT1_SFP_I2C_DATA	B8	A8	LAN0_PORT1_SFP_LED_SPEED	O
I	LAN0_PORT0_SFP_PRSENT_N	B9	A9	RFU	-
PWR	GND	B10	A10	RFU	-
-	RFU	B11	A11	SOC_WANE_N	I
O	RFU	B12	A12	GND	PWR
PWR	GND	B13	A13	HSIO_NM0_RX_1_DN1	I
PWR	GND	B14	A14	HSIO_NM0_RX_1_DP1	I
O	HSIO_NM0_TX_1_DN1	B15	A15	GND	PWR
O	HSIO_NM0_TX_1_DP1	B16	A16	GND	PWR
PWR	GND	B17	A17	HSIO_NM0_RX_1_DP0	I
PWR	GND	B18	A18	HSIO_NM0_RX_1_DN0	I
O	HSIO_NM0_TX_1_DN0	B19	A19	GND	PWR

Dir	Signal	Pin	Pin	Signal	Dir
O	HSIO_NM0_TX_1_DP0	B2 0	A2 0	GND	PW R
PW R	GND	B2 1	A2 1	HSIO_NM0_RX_0_DP1	I
PW R	GND	B2 2	A2 2	HSIO_NM0_RX_0_DN1	I
O	HSIO_NM0_TX_0_DN1	B2 3	A2 3	GND	PW R
O	HSIO_NM0_TX_0_DP1	B2 4	A2 4	GND	PW R
PW R	GND	B2 5	A2 5	HSIO_NM0_RX_0_DP0	I
PW R	GND	B2 6	A2 6	HSIO_NM0_RX_0_DN0	I
O	HSIO_NM0_TX_0_DN0	B2 7	A2 7	GND	PW R
O	HSIO_NM0_TX_0_DP0	B2 8	A2 8	GND	PW R
PW R	GND	B2 9	A2 9	CLK_100M_NM0_DP0	O
PW R	GND	B3 0	A3 0	CLK_100M_NM0_DN0	O
O	CLK_100M_NM0_DP1	B3 1	A3 1	GND	PW R
O	CLK_100M_NM0_DN1	B3 2	A3 2	GND	PW R
PW R	GND	B3 3	A3 3	LAN0_RX_DN1	I
PW R	GND	B3 4	A3 4	LAN0_RX_DP1	I
O	LAN0_TX_DP1	B3 5	A3 5	GND	PW R
O	LAN0_TX_DN1	B3 6	A3 6	GND	PW R
PW R	GND	B3 7	A3 7	LAN0_RX_DP0	I
PW R	GND	B3 8	A3 8	LAN0_RX_DN0	I

Dir	Signal	Pin	Pin	Signal	Dir
O	LAN0_TX_DP0	B3 9	A3 9	GND	PW R
I/O	LAN0_TX_DN0	B4 0	A4 0	GND	PW R
PW R	GND	B4 1	A4 1	SLOT_ADDR (Tied to GND)	O
I/O	GPIO_NM0_0	B4 2	A4 2	GND	PW R
I	SMB_LEG_ALRT_N	B4 3	A4 3	SMB_LEG_DATA	I/O
O	SMB_LEG_CLK	B4 4	A4 4	PLTRST_N	O
I	UART_RX_NM0	B4 5	A4 5	LAN_MDC	O
I/O	LAN_MDIO	B4 6	A4 6	UART_TX_NM0	O
PW R	GND	B4 7	A4 7	+12 VDC	PW R
PW R	GND	B4 8	A4 8	+12 VDC	PW R
PW R	GND	B4 9	A4 9	+12 VDC	PW R

Table 1 Network Module 0 Pinout (J4)

3.18.2 Network Module 1 (J3)

Dir	Signal	Pin	Pin	Signal	Dir
PW R	GND	B1	A1	+12 VDC	PW R
PW R	GND	B2	A2	+12 VDC	PW R
PW R	GND	B3	A3	+12 VDC	PW R
-	RFU	B4	A4	LAN1_PORT1_SFP_I2C_CLK	O
I/O	LAN1_PORT0_SFP_I2C_DATA	B5	A5	LAN1_PORT0_SFP_I2C_CLK	O
O	LAN1_PORT0_SFP_LED_SPEED	B6	A6	LAN1_PORT0_SFP_LED_LINKACT	O

Dir	Signal	Pin	Pin	Signal	Dir
O	LAN1_PORT1_SFP_LED_LINKACT	B7	A7	LAN1_PORT1_SFP_PRSENT_N	I
I/O	LAN1_PORT1_SFP_I2C_DATA	B8	A8	LAN1_PORT1_SFP_LED_SPEED	O
I	LAN1_PORT0_SFP_PRSENT_N	B9	A9	RFU	-
PWR	GND	B10	A10	RFU	-
-	RFU	B11	A11	SOC_WANE_N	I
O	RFU	B12	A12	GND	PWR
PWR	GND	B13	A13	HSIO_NM1_RX_1_DN1	I
PWR	GND	B14	A14	HSIO_NM1_RX_1_DP1	I
O	HSIO_NM1_TX_1_DN1	B15	A15	GND	PWR
O	HSIO_NM1_TX_1_DP1	B16	A16	GND	PWR
PWR	GND	B17	A17	HSIO_NM1_RX_1_DP0	I
PWR	GND	B18	A18	HSIO_NM1_RX_1_DN0	I
O	HSIO_NM1_TX_1_DN0	B19	A19	GND	PWR
O	HSIO_NM1_TX_1_DP0	B20	A20	GND	PWR
PWR	GND	B21	A21	HSIO_NM1_RX_0_DP1	I
PWR	GND	B22	A22	HSIO_NM1_RX_0_DN1	I
O	HSIO_NM1_TX_0_DN1	B23	A23	GND	PWR
O	HSIO_NM1_TX_0_DP1	B24	A24	GND	PWR
PWR	GND	B25	A25	HSIO_NM1_RX_0_DP0	I

Dir	Signal	Pin	Pin	Signal	Dir
PW R	GND	B2 6	A2 6	HSIO_NM1_RX_0_DN0	I
O	HSIO_NM1_TX_0_DN0	B2 7	A2 7	GND	PW R
O	HSIO_NM1_TX_0_DP0	B2 8	A2 8	GND	PW R
PW R	GND	B2 9	A2 9	CLK_100M_NM1_DP0	O
PW R	GND	B3 0	A3 0	CLK_100M_NM1_DN0	O
O	CLK_100M_NM1_DP1	B3 1	A3 1	GND	PW R
O	CLK_100M_NM1_DN1	B3 2	A3 2	GND	PW R
PW R	GND	B3 3	A3 3	LAN1_RX_DN1	I
PW R	GND	B3 4	A3 4	LAN1_RX_DP1	I
O	LAN1_TX_DP1	B3 5	A3 5	GND	PW R
O	LAN1_TX_DN1	B3 6	A3 6	GND	PW R
PW R	GND	B3 7	A3 7	LAN1_RX_DP0	I
PW R	GND	B3 8	A3 8	LAN1_RX_DN0	I
O	LAN1_TX_DP0	B3 9	A3 9	GND	PW R
I/O	LAN1_TX_DN0	B4 0	A4 0	GND	PW R
PW R	GND	B4 1	A4 1	SLOT_ADDR (Tied to GND)	O
I/O	GPIO_NM1_0	B4 2	A4 2	GND	PW R
I	SMB_LEG_ALRT_N	B4 3	A4 3	SMB_LEG_DATA	I/O
O	SMB_LEG_CLK	B4 4	A4 4	PLTRST_N	O

Dir	Signal	Pin	Pin	Signal	Dir
I	UART_RX_NM1	B4 5	A4 5	LAN_MDC	O
I/O	LAN_MDIO	B4 6	A4 6	UART_TX_NM1	O
PW R	GND	B4 7	A4 7	+12 VDC	PW R
PW R	GND	B4 8	A4 8	+12 VDC	PW R
PW R	GND	B4 9	A4 9	+12 VDC	PW R

Table 2 Network Module 1 Pinout (J3)

3.18.3 Front Panel Module (J7)

Dir	Signal	Pin	Pin	Signal	Dir
PWR	+12 VDC	B1	A1	GND	PWR
PWR	+12 VDC	B2	A2	GND	PWR
PWR	GND	B3	A3	USB3_FP_TX_DP	O
PWR	GND	B4	A4	USB3_FP_TX_DN	O
I	PCIE_FP_RX_DP	B5	A5	GND	PWR
I	PCIE_FP_RX_DN	B6	A6	GND	PWR
PWR	GND	B7	A7	USB3_FP_RX_DN	I
PWR	GND	B8	A8	USB3_FP_RX_DP	I
O	PCIE_FP_TX_DP	B9	A9	GND	PWR
O	PCIE_FP_TX_DN	B10	A10	GND	PWR
PWR	GND	B11	A11	RFU	-
PWR	+12 VDC	B12	A12	GND	PWR
PWR	+12 VDC	B13	A13	GND	PWR
PWR	GND	B14	A14	USB2_FP_DN	I/O
PWR	GND	B15	A15	USB2_FP_DP	I/O
O	CLK_100M_FP_DN	B16	A16	GND	PWR
O	CLK_100M_FP_DP	B17	A17	GND	PWR
PWR	GND	B18	A18	USB2_FP_VM_DN	I/O
PWR	GND	B19	A19	USB2_FP_VM_DP	I/O

Dir	Signal	Pin	Pin	Signal	Dir
O	PLTRST_N	B20	A20	GND	PWR
O	SMB_LEG_CLK	B21	A21	ISO_BUFFER_EN	O
I/O	SMB_LEG_DATA	B22	A22	NCSI_CRS_DV	O
I	FAN_RIGHT_PWM	B23	A23	NCSI_RXD1	O
O	FAN_RIGHT_TACK	B24	A24	NCSI_CLK_IN	I
I	FP_FRU_EEPROM_MUX_SEL	B25	A25	SPI_SOC_CS1_N	O
I	USB_OC_N	B26	A26	NCSI_RXD0	I
I	FP_PWRBTN_N	B27	A27	NCSI_TXD0	O
I	FP_BUTTON_OVERRIDE	B28	A28	NCSI_TX_EN	I
I	FP_RSTBTN_N	B29	A29	NCSI_TXD1	I
I	FAN_CENTER_PWM	B30	A30	TEMP_DIODE_CPU_DN	O
O	FAN_CENTER_TACH	B31	A31	TEMP_DIODE_CPU_DP	O
I	FAN_LEFT_PWM	B32	A32	I2C_FP_SCL	I
O	FAN_LEFT_TACH	B33	A33	I2C_FP_DATA	I/O
O	PSU_RIGHT_PWRGD	B34	A34	RFU	-
O	PSU_LEFT_PWRGD	B35	A35	RFU	-
I	SPI_SOC_MISO	B36	A36	SPI_SOC_MOSI	O
I/O	SPI_SOC_IO3	B37	A37	SPI_SOC_IO2	I/O
O	SPI_SOC_CLK	B38	A38	SPI_SOC_CS0_N	O
I	SOC_UART0_RXD	B39	A39	SOC_UART0_RTS	O
O	SOC_UART0_TXD	B40	A40	SOC_UART0_CTS	I
I/O	SMB_PECI_DATA	B41	A41	SMB_PECI_CLK	I
O	SOC_THERMTRIP_3P3_N	B42	A42	SLP_S45_N	O
O	SOC_PROCHOT_3P3_N	B43	A43	SLP_S3_N	O
O	CPU_ERROR_N	B44	A44	SMB_HOST_CLK	O
I/O	SMB_HOST_DATA	B45	A45	GPIO_FP_1	I/O
I/O	GPIO_FP_0	B46	A46	RFU	-
PWR	GND	B47	A47	+3.3 VDC	PWR
PWR	GND	B48	A48	+3.3 VDC	PWR
PWR	GND	B49	A49	+3.3 VDC	PWR

Table 3 Network Module 1 Pinout (J7)

3.18.4 Front Panel LED Header (J15)

Dir	Signal	Pin	Pin	Signal	Dir
O	LED_MPCIE_WWAN_N	1	2	+5 VDC	PWR
O	LED_MPCIE_WLAN_N	3	4	NC	-
O	LED_MPCIE_WPAN_N	5	6	LED_SATA_V5A	O
O	LED_M2_SSD_KEYB2_N	7	8	NC	-
O	LED_M2_SSD_KEB_N	9	10	GND	PWR

Table 4 PIC Programming Connector (J16)

3.18.5 SMBus Header (J16)

Pin	Signal	Dir
1	SMB_LEG_CLK	I
2	GND	PWR
3	SMB_LEG_DATA	I/O

Table 5 SMBus Header (J16)

3.18.6 Clear CMOS Header (J11)

Pin	Signal	Dir
1	SOC_RTEST_N	I
2	GND	PWR
3	SOC_SRTCST_N	I

Table 6 Clear CMOS Header (J11)

3.18.7 FAN Connectors (J22,J23,J24)

Pin	Signal	Dir
1	+12 VDC	PWR
2	FAN TACH	I
3	FAN PWM	O
4	GND	PWR

Table 7 Fan Connectors (J22, J23, J24)

3.18.8 HDD Power Connector (J10)

Pin	Signal	Dir
1	+12 VDC	PWR
2	GND	PWR
3	GND	PWR
4	+5 VDC	PWR

Table 8 HDD Power Connector (J10)

3.18.9 PIC Programming Cable (J13)

This connector will not be populated in production.

Pin	Signal	Dir
1	PIC_VPP	I
2	+3.3 VDC	PWR

3	GND	PWR
4	ICSPDAT	I/O
5	ICSPCLK	I

Table 9 PIC Programming Connector (J13)

3.18.10 SVID Connector (J5)

This connector will not be populated in production.

Pin	Signal	Dir
1	SVID_ALERT_N	-
2	SVID_DATA	-
3	SVID_CLK	-

Table 10 SVID Connector (J5)

4 uBMC/Switch Card

The front panel card for the XS uCPE is a double-wide card that connects to the compute board front-panel I/O slot and the network module-0 slot. The two block diagrams below represent the uBMC and networking sections of the card.

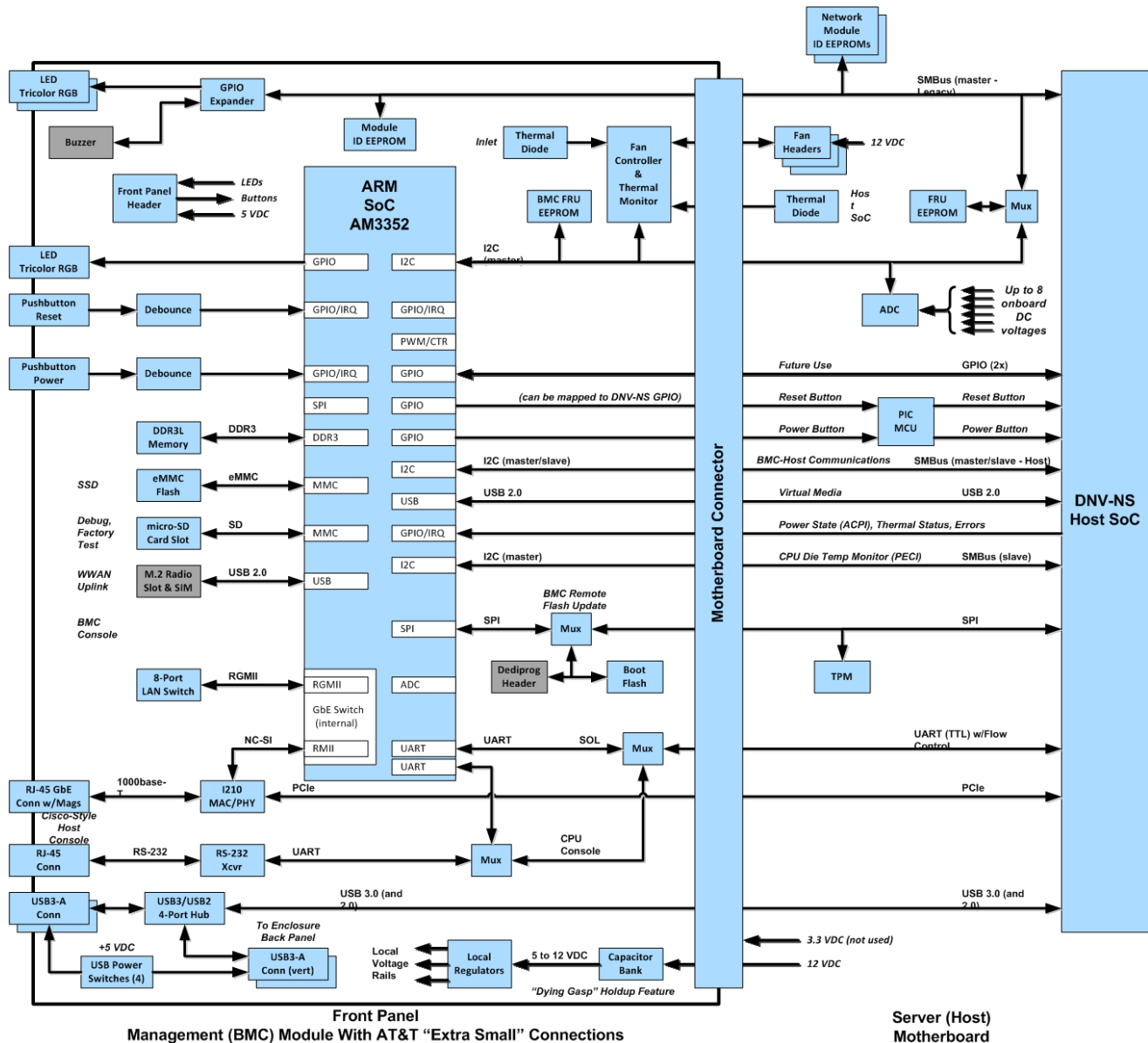


Figure 13 XS uCPE Management Block diagram

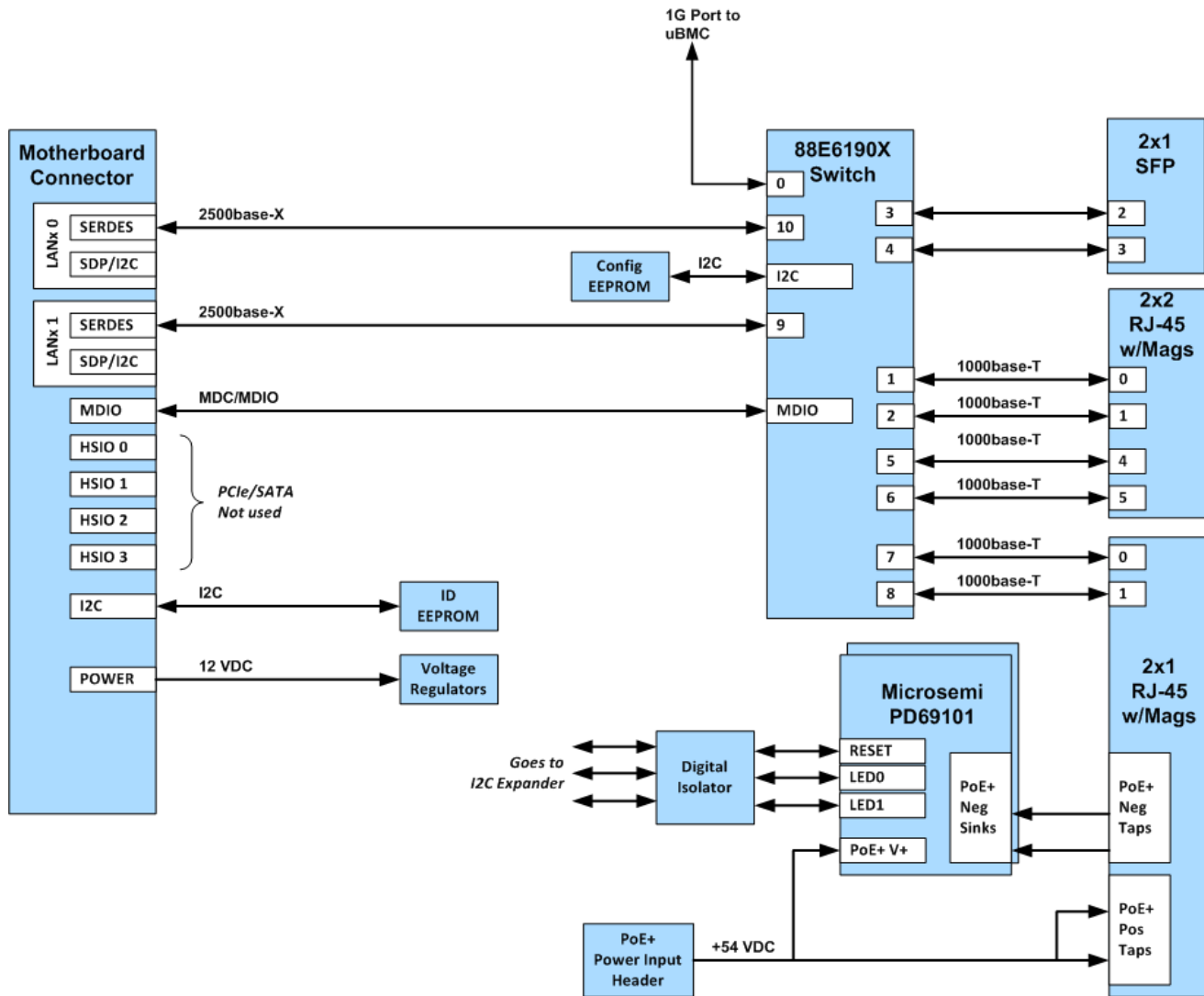


Figure 14 XS uCPE LAN/WAN Block Diagram

4.1 uBMC

The microcontroller used for the first generation uBMC is the TI AM3352ZCZ60 which has a 600MHz ARM Cortex –A8 32-bit RISC processor. The uBMC will be responsible for following:

- Supporting a secure connection over management port or WAN
- Supporting remote updates to host BIOS, OS, or BMC software.
- Controlling and monitoring thermals
- Monitoring critical error signals and on-board voltages
- Power and reset control
- Serial Console Over LAN (SOL)
- Virtual Media
- Dying Gasp

Refer to uBMC Software Functional Specification for additional details on the uBMC features.

4.1.1 Memory

The uBMC will have 512MB of DDR3 memory. This is implemented with a single 4Gb x16 memory IC.

4.1.2 eMMC

In production, the uBMC eMMC is planned to be an 8GB device. For prototypes, this may be larger to support development efforts.

4.1.3 Micro-SD Slot

The Micro-SD slot is used for factory test but can also be used for additional storage during the development process.

4.1.4 uBMC UARTs

The uBMC UART1 is connected to the host UART for Serial-Over-LAN (SOL) support and for capturing birth/death logs. The uBMC console port, UART0, is connected to the front panel RS232 console port.

At power on, the uBMC console will be displayed on the front port. After the uBMC is up, the user can select between the uBMC or host console by using the CNTL-X command.

During prototypes and before uBMC software is available, the host console port will be connected directly to the front panel port through a series of muxes. The mux can be controlled by the uBMC or through a jumper.

4.1.5 Ethernet

The uBMC supports two Ethernet connections. One connection is an RGMII connection to the onboard Ethernet switch. This gives the uBMC access to the WAN/LAN ports as well as a high-speed connection back to the host CPU.

The second Ethernet connection is a NC-SI (Network Controller Sideband Interface) to an Intel i210. This externally accessible port is shared with the host CPU. The NC-SI connection is limited to 100Mbps. Note that the NC-SI interface will continue to operate even if the host CPU PCIe, clock, and reset are in a power down state.

4.1.6 USB

The uBMC supports two USB2.0 ports. One is connected to the host CPU and is intended to be used as a virtual media port. This will provide a remote path for the uBMC to support OS installs or updates.

The second USB2.0 port is connected to a M.2 Key-B expansion slot.

4.1.7 M.2 Expansion

The uBMC is connected to a M.2 Key-B expansion slot over USB2.0. This slot is intended to provide a low bandwidth LTE connection to the uBMC. The card supports an externally accessible micro SIM card slot.

4.2 Front Panel 1GbE Port

There is front panel 1GbE port which is connected directly to the host CPU through an Intel i210 MAC/PHY. The i210 also supports a NC-SI interface to the uBMC. When the host CPU is powered down, the uBMC will still be able to use this port through the NC-SI interface.

4.3 Front Panel and Internal USB Ports

The host CPU does not support enough USB3.0 ports. A four-port hub will be used to expand the number of USB3.0 ports. The part used is a TI TUSB8041. Two of the USB3.0 ports will be connected to the front panel I/O. Two of the ports will be internal vertical ports. These can be used for internal connections such as flash drives or Bluetooth, or potentially LTE. Or they could be cabled to the back panel to be externally accessible. The default is to leave these ports as vertical ports inside the box. There is 20.1 mm between the top of the USB port and the top of the enclosure. Each USB3.0 port supports up to 1A. Power budget for all USB ports is assumed to be <2A (10W).

There is a population option available on the board that will connect the TUSB8041 to the host SMBus. When this option is used, the TUSB8041 is not operational until configured over the SMBus. This is why the first prototypes will not be populated with this option. Once support is added to the bootloader, this device will be connected to the SMBus. The main reason for adding this device to the SMBus is to give the host CPU control over each USB port's power. This is a desirable feature if a USB device needs to be power cycled (i.e. LTE modem).

4.4 Front Panel Power and Reset Buttons

The platform supports two front panel push button. One is a larger, easily accessible push button that is typically defined as the power button. The second is a recessed power button which is accessible through a small hole about the size of a paper clip. This button is typically defined for reset or reset to defaults.

Both push buttons go to the compute board and through a PIC microcontroller where their function can be defined. The PIC can route directly to the host CPU power and reset button inputs, or it can route to a GPIO. The PIC can also be programmed with timers to provide multifunction's to the push buttons.

The uBMC can also assert the power and reset buttons.

4.5 Front Panel Console Port

The front panel console port is a RJ45 port with RS232 Cisco pinout. It supports TX, RX, CTS, and RTS. DCD, DTR, and RI are not supported. The console will be connected directly to the uBMC. At power on, the uBMC console will be displayed on this port. After the uBMC is up, the user can to between the uBMC and host console by using the CNTL-X command.

During prototypes and before uBMC software is available, the host console port will be connected directly to the front panel port through a series of mixes. The mux can be controlled by the uBMC or through a jumper.

The RJ45 connector supports LED's which indicate the following:

- Right Yellow LED = RS232 Cable detected
- Left Green LED = Unused

4.6 Front Panel LED's

There are three tri-color (Red,Green,Blue) LED's on the front I/O panel.

	Default configuration
Top LED	When the platform is turned on, the default color will be AMBER (RED and GREEN). The bootloader will change the LED to BLUE. The host CPU has access to this LED so future definitions could be defined.
Center LED	Connected to I2C Expander. Controlled by the host CPU.
Bottom LED	This LED will only be controlled by the uBMC When platform is first powered on, this LED is off. The uBMC will change to BLUE once the kernel is loaded

Table 11 LED Description

4.7 I2C-to-GPIO Expander

There is a 16-bit I2C-to-GPIO Expander chip at SMBus address 0xE8 (0x74). The IC used is a NXP PCAL9539A.

Port#_bit	Signal	DIR	
P0_0	LED_BOT_RED_N	O	Bottom Red LED Control. 0=On, 1=Off
P0_1	LED_BOT_GRN_N	O	Bottom Green LED Control. 0=On, 1=Off
P0_2	LED_BOT_BLU_N	O	Bottom Blue LED Control. 0=On, 1=Off
P0_3	LED_CTR_RED_N	O	Center Red LED Control. 0=On, 1=Off
P0_4	LED_CTR_GRN_N	O	Center Green LED Control. 0=On, 1=Off
P0_5	LED_CTR_BLU_N	O	Center Blue LED Control. 0=On, 1=Off

P0_6	POE0_RST_N	O	Switch Port 7, POE+ Control. 0= Disable POE, 1= Enable POE.
P0_7	POE1_RST_N	O	Switch Port 8, POE+ Control. 0= Disable POE, 1= Enable POE.
P1_0	LED_TOP_RED_N	O	Top Red LED Control. 0=On, 1=Off
P1_1	LED_TOP_GRN_N	O	Top Green LED Control. 0=On, 1=Off
P1_2	LED_TOP_BLU_N	O	Top Blue LED Control. 0=On, 1=Off
P1_3	BUZZER	O	Buzzer Control. Not populated in production.
P1_4	POE0_LED0	I	Switch Port 7 POE Status. Refer to POE+ Ports section for details.
P1_5	POE0_LED1	I	Switch Port 7 POE Status. Refer to POE+ Ports section for details.
P1_6	POE1_LED0	I	Switch Port 8 POE Status. Refer to POE+ Ports section for details.
P1_7	POE1_LED1	I	Switch Port 8 POE Status. Refer to POE+ Ports section for details.

Table 12 I2C-to-GPIO Expander Description

4.8 LAN/WAN Ports and Network Switch

The WAN and LAN interfaces are through an internal Ethernet switch. The card will support 6x1GbE Copper ports and 2x1GbE Fiber ports. The connections between the switch and the host CPU will be 2x2.5Gb-X. There is also a 1GbE connection between the switch and uBMC.

The internal 10GbE controllers are always located on the secondary bus of an internal PCIe root port. Depending on the PCIe bifurcation, and what other PCIe cards are installed in the system the secondary bus numbering may change. For persistent device naming the udev rules can be changed to assign a fixed

network interface name to any device downstream of. As an example, the following udev rules rename the ixgbe interfaces according to network module and lane:

```
DEVPATH=="devices/pci0000:00/0000:00:16.0/0000:??:00.0/net/*", NAME="nm0ln0"
DEVPATH=="devices/pci0000:00/0000:00:16.0/0000:??:00.1/net/*", NAME="nm0ln1"
DEVPATH=="devices/pci0000:00/0000:00:17.0/0000:??:00.0/net/*", NAME="nm1ln0"
DEVPATH=="devices/pci0000:00/0000:00:17.0/0000:??:00.1/net/*", NAME="nm1ln1"
```

The network switch is a Marvell 88E6190X. The “X” version is used to get the required SFP ports. This switch supports managed functions and can be managed/configured in three possible ways:

1. Through the MDIO/MDC Interface
2. Through one of the upstream ports (9 or 10). Switch would need to be configured with EEPROM or through MDIO/MDC to allow this.
- 3.
4. External EEPROM. The external EEPROM is useful for a static configuration.

The switch port number does not match the front panel port numbering. The following table shows how the switch ports map to the front panel port numbering.

Switch Port Number	Front Panel
0	Internal to uBMC
1	4
2	3
3	1
4	2
5	6
6	5
7	8
8	7
9	Internal to host CPU
10	Internal to host CPU

Table 13 Switch port number to front panel markings

In Linux communication with MDIO devices typically takes place using the SIOCGMIIREG and SIOCMIIREG ioctl requests. Neither the mainline ixgbe nor the intel ixgbe driver supports MDIO accesses to any devices not associated with the autoprobe PHY. Silicom has a patch series that applies against the intel ixgbe source that changes this behavior.

Although each PCIe function associated with an ixgbe device has its own set of MSCA & MSRWD registers, there is a single MDIO controller in the SoC driving a single MDIO bus. To prevent contention between drivers, firmware, and hardware access to this shared resource. Both example Silicom ixgbe drivers handle access synchronization to the MDIO controller. If more advanced control is needed section 8.8.4 of the Denverton PRMⁱⁱ details the process for acquiring and releasing the lock on shared resources.

The Marvell switch has two addressing options. In the single-chip mode of operation that part claims multiple device addresses. Table 44 of the Switch Functional Specification^[iii] shows the device/register address layout. This board operates in multi-chip addressing mode and only 2 responds to 2 register addresses at a single device address (0x10). This indirection mechanism is described in Section 8.2 of the Switch Functional Specification^[iii].

Silicom has demo applications for accessing the switch in either mode, either with the modified mainline ixgbe driver, or with the modified dpdk driver.

Marvell also provides a software library called UMSD^[iv] that can be used as a HAL for interacting with the switch. Silicom has a demo application for accessing the EEPROM using this library.

4.9 POE+ Ports

The card will support two POE+ ports. Each port is controlled by a Microsemi PD69101 PSE controller. The controllers are configured to support 720mA of POE power.

The host CPU can enable/disable each port by controlling the PD69101 reset input. These are connected to the I2C expander on this card. Refer to I2C-to-GPIO Expander section for details. We reset is pulled low, the port is disabled.

The host CPU can monitor each port by looking at the PD69101 outputs LED0 and LED1. These are connected to the I2C expander on this card. Refer to I2C-to-GPIO Expander section for details. The follow table provides information on the LED0 and LED1 feedback signals.

By default, the POE+ ports will be enabled.

STATUS INDICATIONS	LED0	LED1	NOTES
AF Mode – Port “ON”	ON	OFF	Useful for Bicolor LED connected from LED0 to LED1
AT Mode (Class AT was detected) - Port “ON”	ON	ON	
AF Mode – Over-load or short	Blink 1Hz	OFF	Blinking continues for ~ 2 sec
AT Mode – Over-load or short	Blink 1Hz	Blink 1Hz	Blinking continues for ~ 2 sec
Vmain Voltage out of range or IC over-temperature	Blink 4Hz	OFF	Blinking continues as long as over-voltage or over-temperature state exists
AF Mode – Port “OFF”	OFF	ON	Useful for Bicolor LED connected from LED0 to LED1
AT Mode – Port “OFF”	OFF	OFF	

Table 14 POE+ LED0 and LED1 behavior

4.10 Network Switch / Host FRU EEPROM

FRU EEPROM is ID_info_vecpe_xs_r00x.docx

4.11 Host SPI Flash

The host CPU bootloader SPI Flash is located on this card. That SPI flash is currently a 16MB device. During the prototype stage, this device can be programmed in-circuit with a [Dediprog SF100](#) programmer and a [ISP-ADP-127](#) cable adapter. The header for this programmer will be removed for production.

The uBMC also has access to the SPI flash through a multiplexor which the uBMC controls. This allows the uBMC to perform updates and/or recover from bootloader failures.

4.12 BMC FRU EEPROM

BMC FRU per EEPROM is ID_info_vecpe_xs_r00x.docx

4.13 Thermal Management

The uBMC will be managing all thermals for the for the platform.

The uBMC has access to an on-board fan controller and temperature monitor. The device used is a Microchip EMC2300. The device supports the following:

- Control and monitor up to three fans (on compute board)
- Monitors two external temperature diodes.
 - One on the uBMC card for air intake temperatures
 - One on the compute board near the host CPU
- Internal temperature reading

The controller is programmed and polled by the uBMC though the uBMC sensor I2C bus.

The uBMC has access to the host CPU internal temperatures through the host CPU PECI I2C bus. The uBMC will poll this bus to monitor the CPU temperatures and adjust fans as needed and/or report failures as needed.

The uBMC has access to the PROCHOT_N signal on the compute board. This signal is asserted by the host CPU voltage regulators if they are too hot. This will tell the host-CPU to start throttling its performance to try and reduce the temperature. The uBMC can monitor this signal to know that the platform is in a degraded state and report as needed.

The uBMC has access to the THERMTRIP_N signal on the compute board. This signal is drive by the host CPU and is asserted if a catastrophic thermal event has occurred (temperate reached may damage the SOC). This signal causes the host CPU to go to a lower power state turning off most of the on-board power supplies. The uBMC can monitor this signal to know that the platform is in a powered down state and report as needed.

4.14 Dying Gasp

The uBMC will support sending out a dying gasp packet when the 12V power is going down. The following is the procedure for supporting this feature:

1. 12V Rails is detected to be falling and has passed a set threshold (10.4V)

2. The on-board 12V pass-through FET is disabled which will isolate 12V on the front panel card from the 12V on the compute board. This will prevent the front panel card from powering components on the compute board and draining the bulk capacitors
3. Non-essential circuits on the front panel card are disabled to reduce power draw. These include the USB hub/ports, Console, and GPIO Expander.
4. 12V bulk capacitors on the front panel card will slow down the 12V rail as it powers down. The on-board regulators on the front panel card can operate down to a lower voltage (6V).
5. A Non-Maskable Interrupt is sent to the uBMC which will tell the uBMC to send out the dying gasp packet.

Note that Intel i210 and the Marvell switch are both held up during this period, so the dying gasp packet could be sent out either.

4.15 Power Architecture

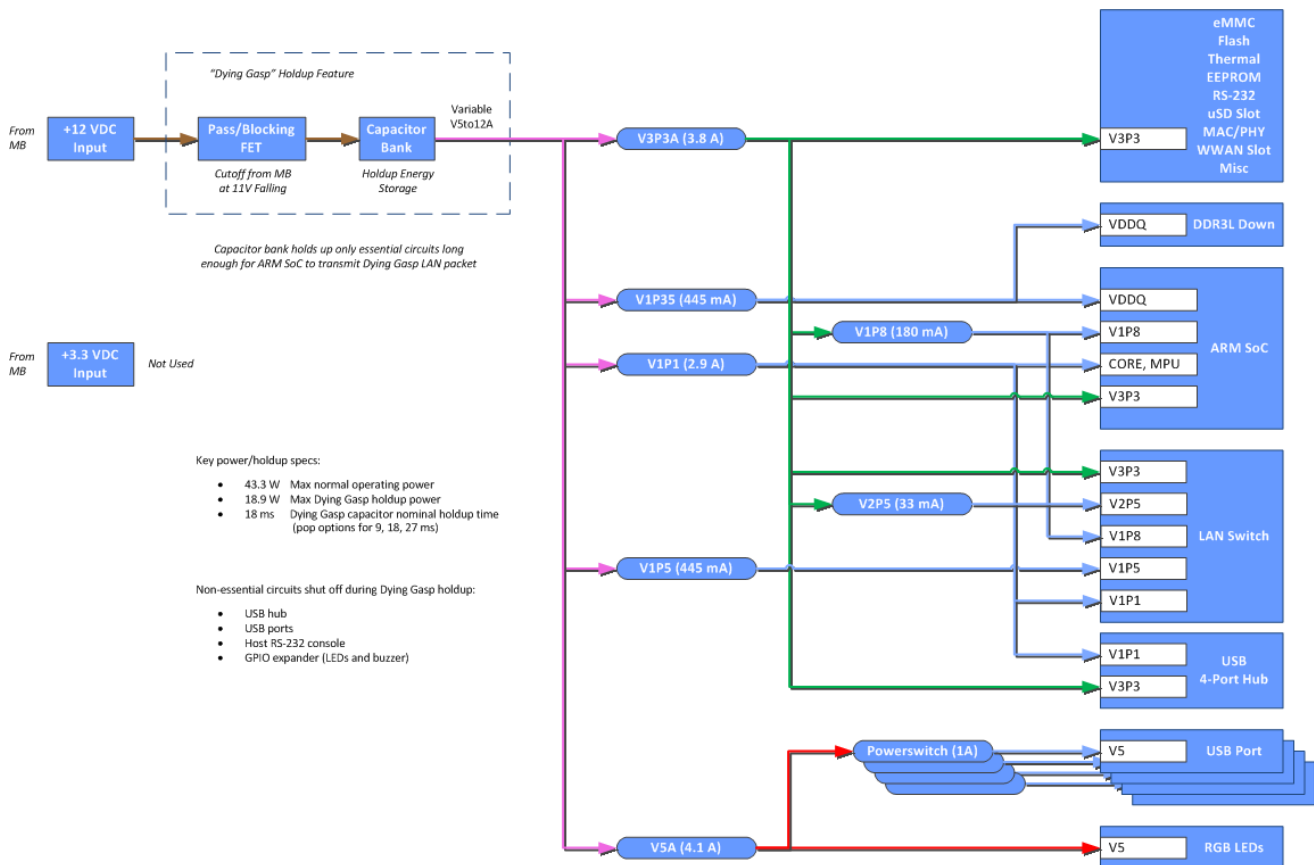


Figure 15 uBMC/Switch Card Power Architecture

4.16 Connector Pinouts

NEED TO COMPLETE

5 Bootloader

5.1 Boot Order

- SATA
- eMMC
- USB
- Virtual Media
- PXE

6 Mechanicals

`WILL CONTINUE TO ADD DETAILS

Front panel Lexan sticker per ECO-007089:

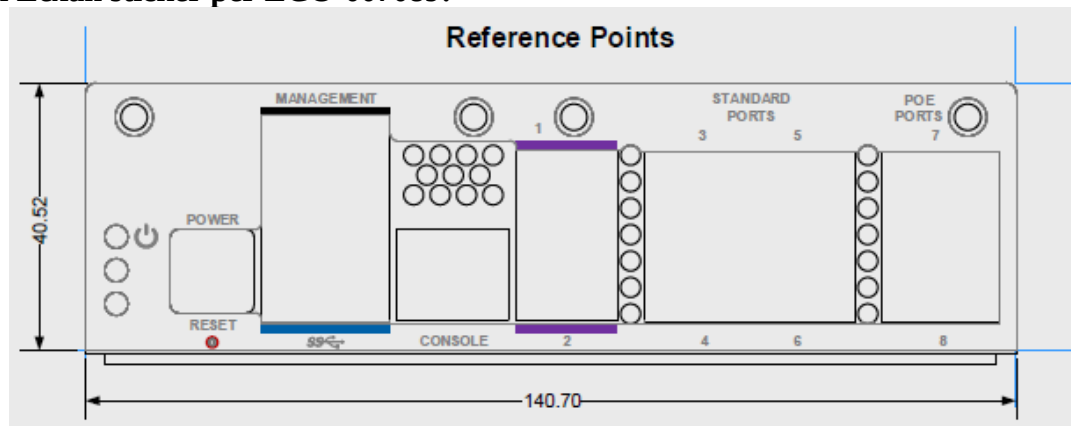


Figure 16 Front Panel Markings and I/O Configuration

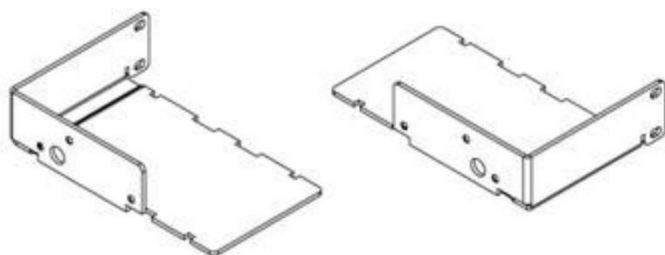
7 Power Estimates

NEED TO COMPLETE

8 Optional Accessories –

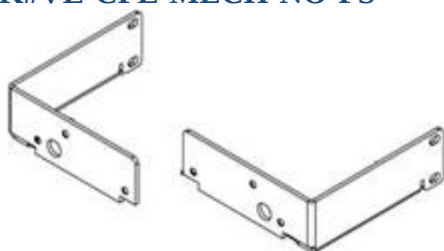
8.1 Rack mount brackets with power supplies support (2 items)

K#VE-CPE-MECH



8.2 Rack mount brackets without power supplies support (2 items)

K#VE-CPE-MECH-NO-PS



8.3 Wall mount bracket

K#VE-CPE-MECH-WALL



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- i Intel Atom Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4, Intel Document # 558579
 - ii Denverton SoC Product Family Integrated 10GbE LAN Controller Programmer's Reference Manual (PRM), Intel Document # 559023
 - iii Link Street® 88E6390X/88E6390/88E6190X/88E6190, Switch Functional Specification, Marvell Document # MV-S110642-00
 - iv Unified Marvell SOHO Driver Version 2.0.4, For SOHO Switch Family, User Manual, Marvell Document # MV-S800936-00