

vE-CPE FPM-ATT-XS

Front Panel Module - AT&T Extra Small

micro-BMC + 4x1GbE, 2xSFP, 2x1GbE w/ POE+

Revision	Date	Description
X100	Date	Alpha prototype release
X200	Date	Beta prototype release
R100	18.04.2018	GA#1 release
R101	06.05.2018	uBMC FW Update - Fan in Auto Mode
R102	09.05.2018	uBMC FW Update - See Release Notes for full detail
R103	10.05.2018	Update Assembly Changes
R200	12.05.2018	GA#2 release
R205	27.11.2018	1. Customer request: Update FP LED color to be Amber (RED and GREEN) . Before change it is green yellow 2. Unified FP LED Color - All three LEDs to the same color grade. 3. Bottom FP LED will be controlled only via the uBMC – eliminate potential contention between the x86 and uBMC.Functional Team(s):No Privilege
R206	04.12.2018	BOM Cleanup of ATT XS in order to reduce cost and improve logistics.

Feature	G00
Product SKU	AT&T XS
DDR3L RAM	512MB
eMMC SSD	8 GB
USB Ports (front)	2
USB Ports (back)	2
WWAN Slot	Yes
Dying Gasp Holdup	Yes
GbE Ports	4
SFP Ports	2
GbE w/ POE+ Ports	2

- Notes:
- 1. DNI (non-inserted) attributes displayed only through Variant Manager.
 - 2. Bootloader setting: ARM SoC must be configured for Operating Point OPP100

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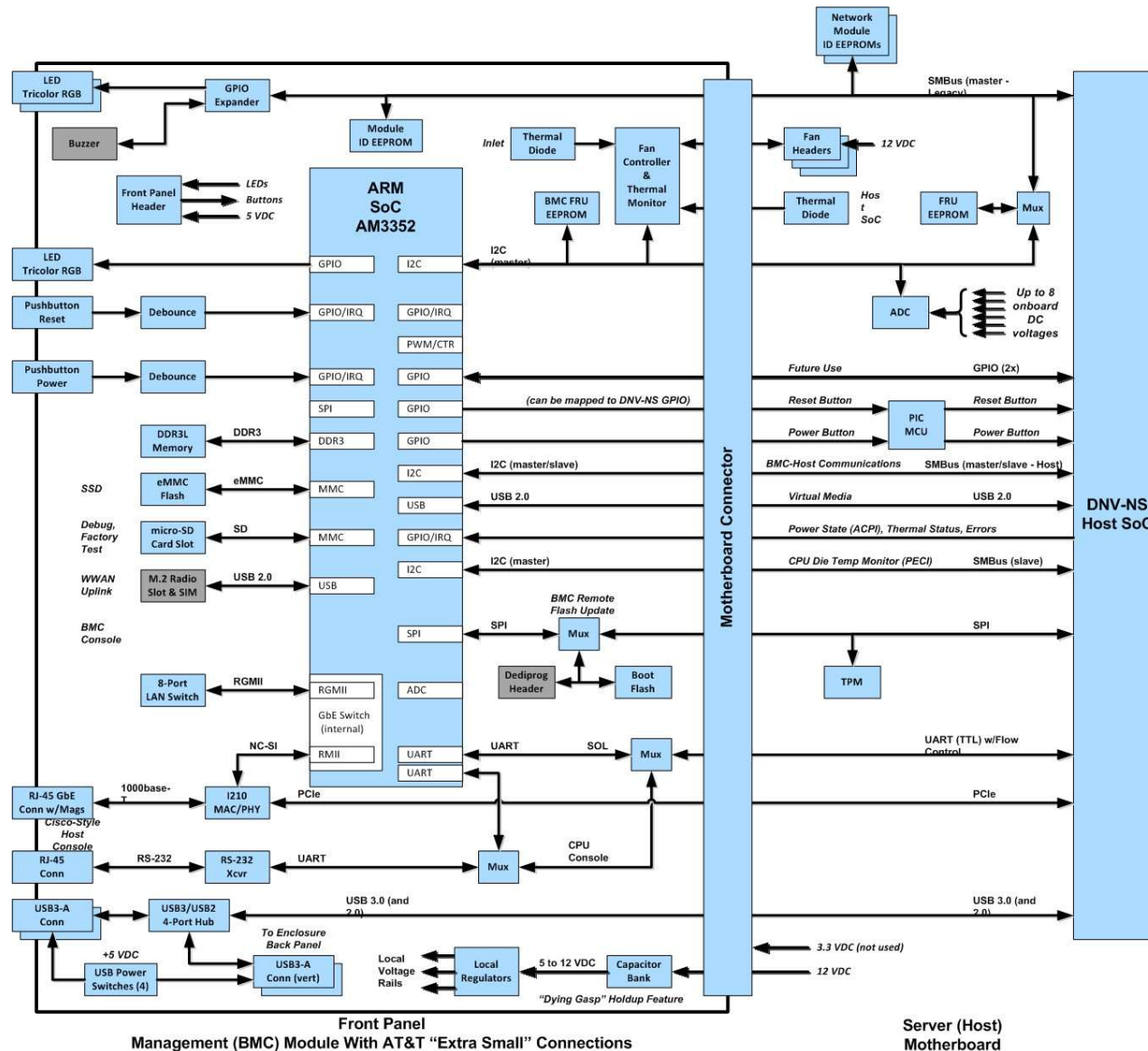
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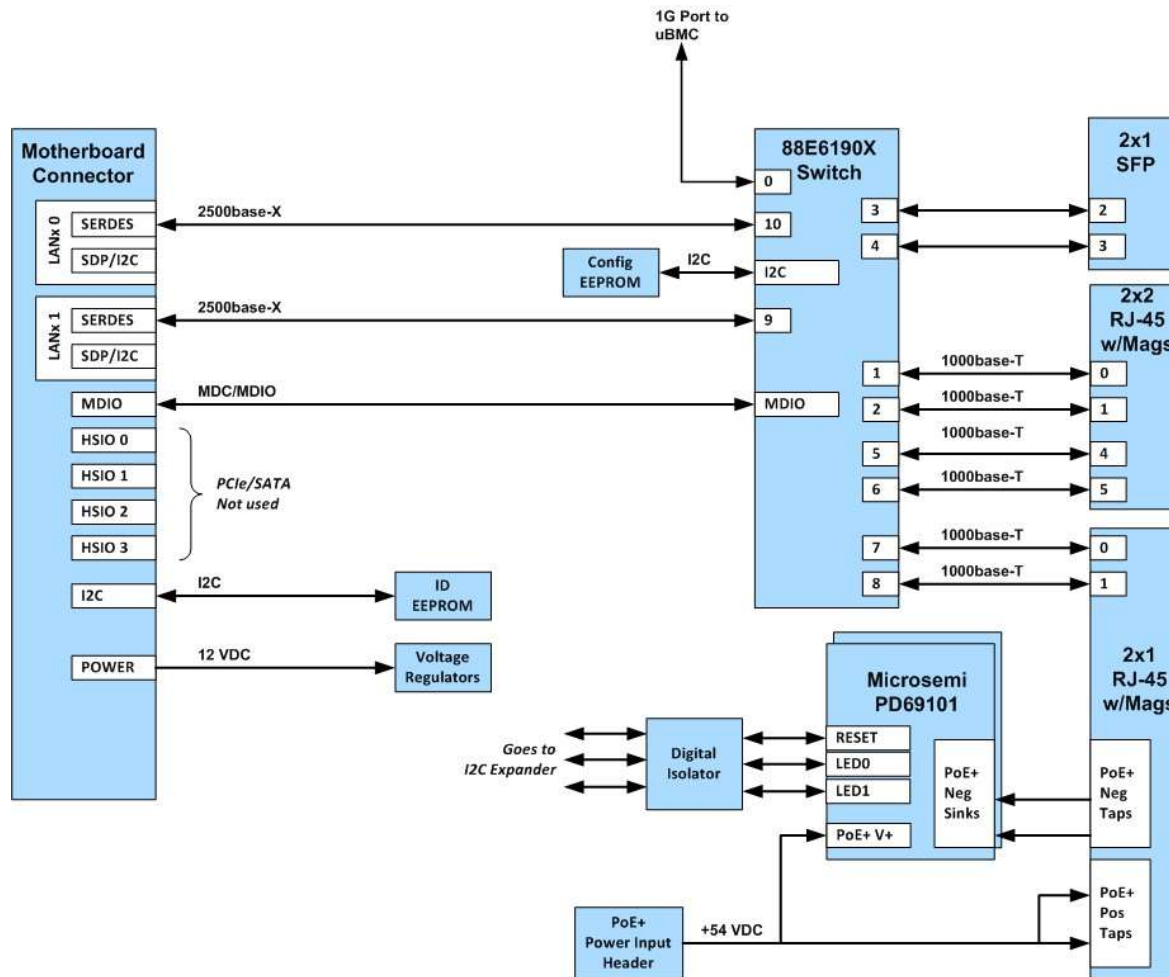
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DATE : Sunday, March 17, 2019		APPROV.	Nader Yaffe	N.Y.	17.03.19			
Monday, February 12, 2018		David C.	D.C.	17.03.19				
		Legal Disclaimer		SHEET : 3		of SHEETS : 35		





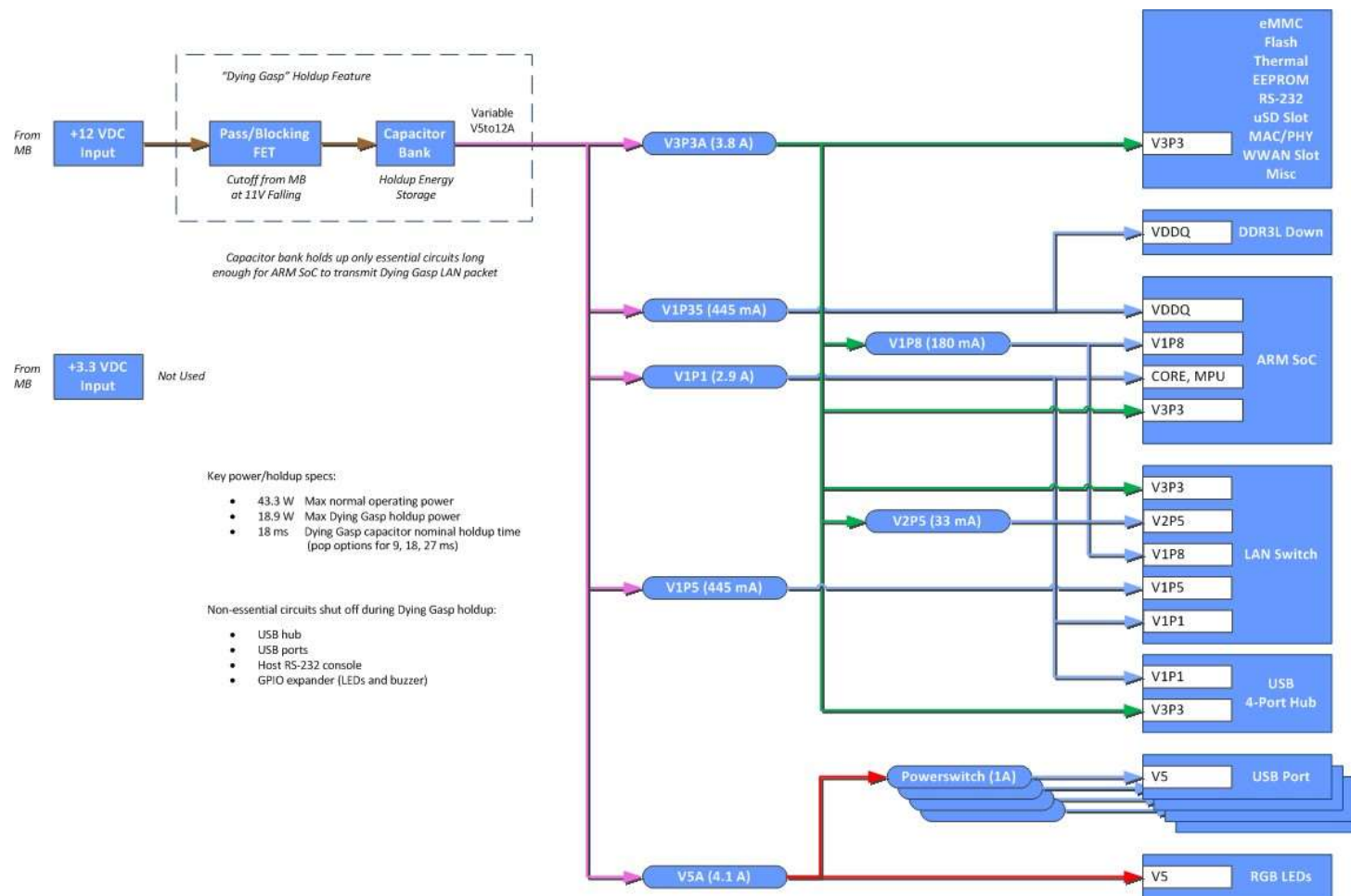
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80200-0175-G00

Block Diagram - LANWAN

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APPROV.	Nadav Yafe	N.Y.	17.03.19
	David C.	D.C.	17.03.19
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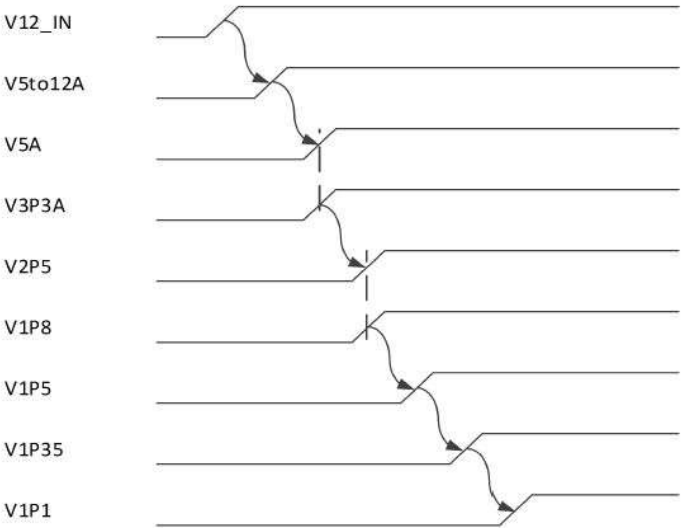
Power Architecture

APPROVALS			
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APPROV.	David C.	D.C.	17.03.19
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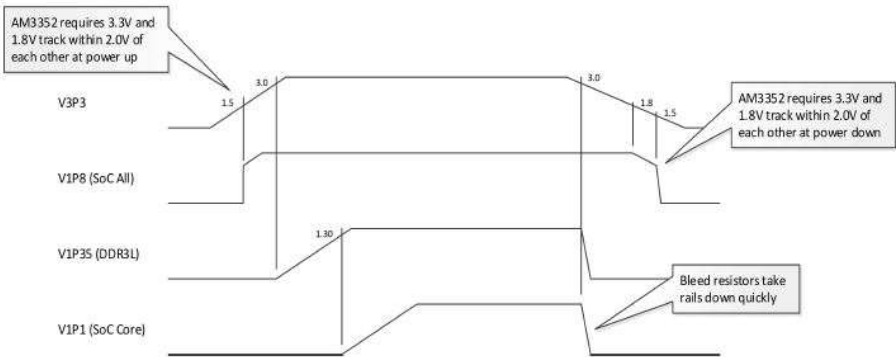
General Power Sequence



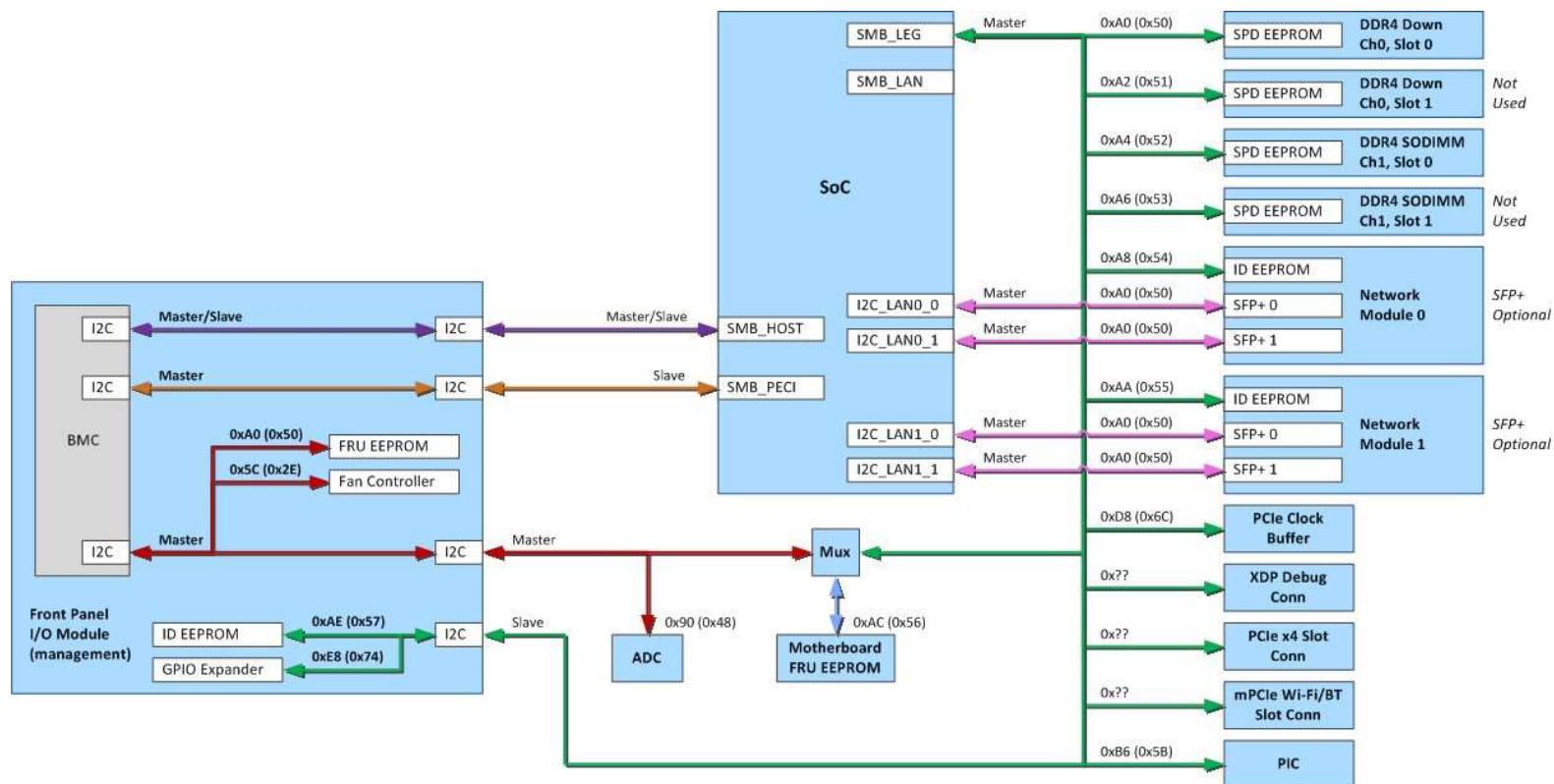
Note:

1. LAN switch sequence requires that each rail be brought up in sequence from highest-to-lowest or at the same time.
2. ARM SoC sequence is detailed in separate diagram below.
3. Other devices have no sequencing requirements.

SoC-Specific Power Sequence



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Power Sequence		APPROV.	David C.	D.C.	17.03.19
SHEET : 7		of SHEETS : 35			



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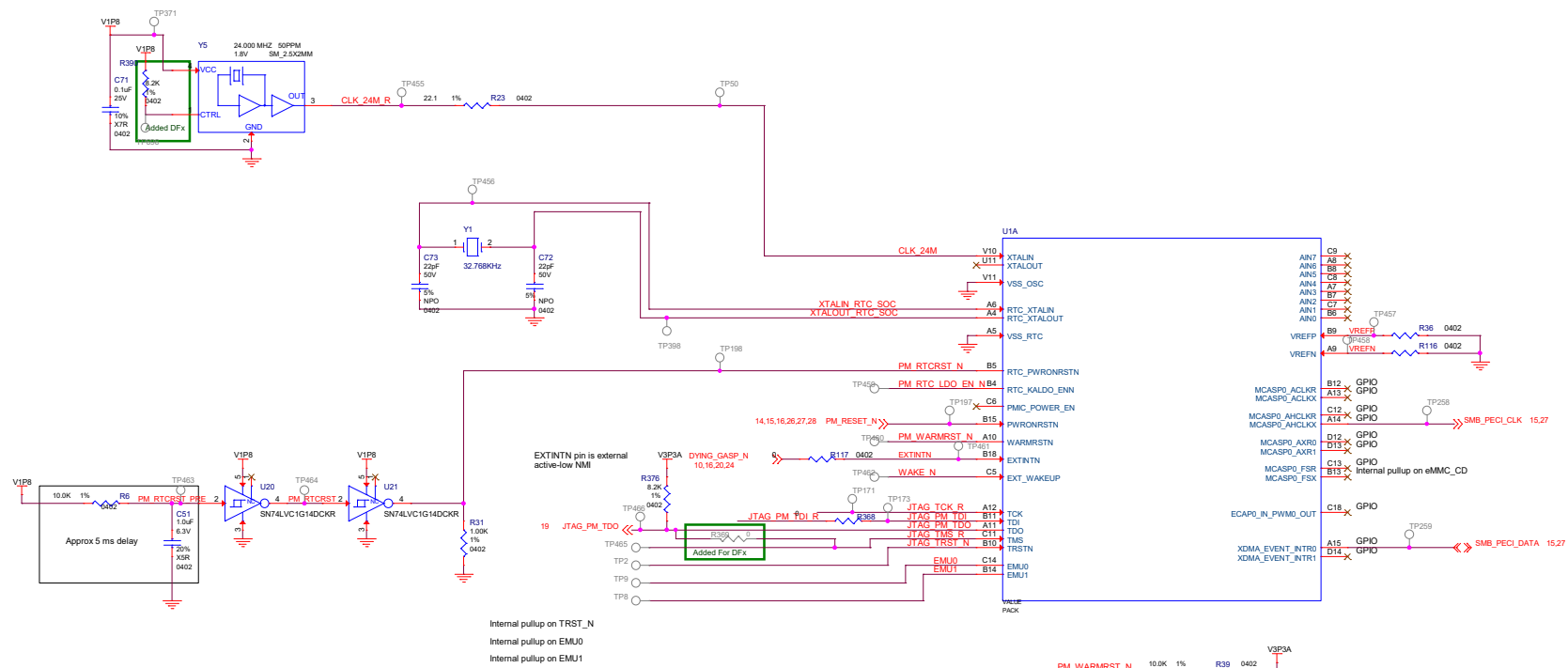
80200-0175-G00

I2C/SMBus Architecture

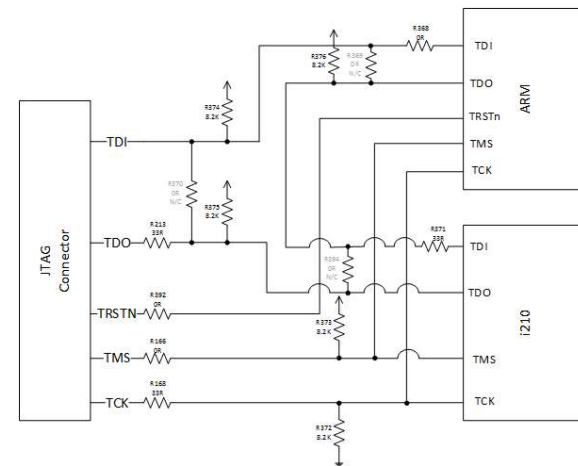
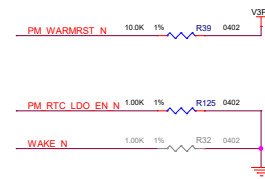
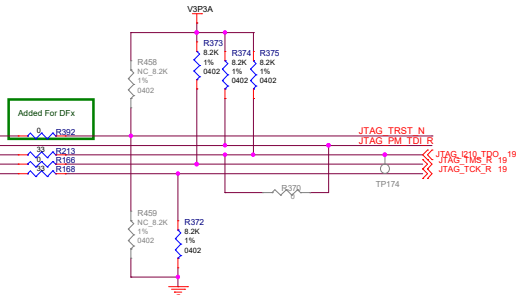
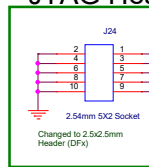
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JTAG Header

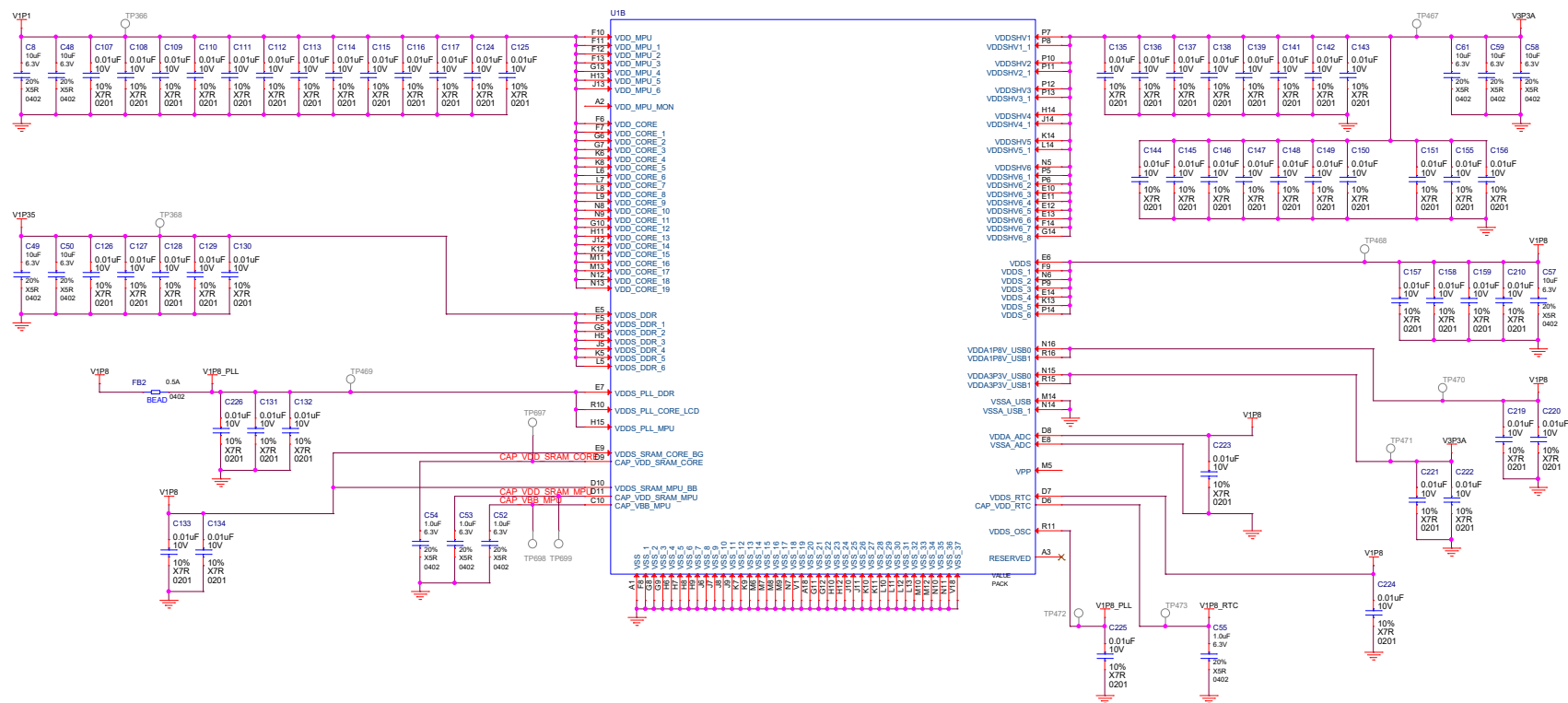


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NAME	SGN	DATE	
Nadar Yalo	N.Y.	17.03.19	
David C.	D.C.	17.03.19	

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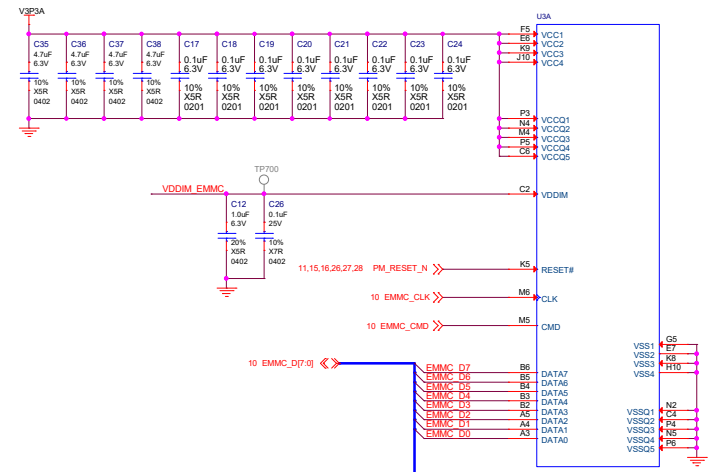
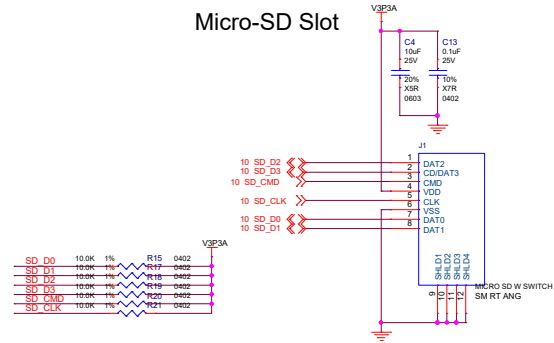
ARM SoC - Power, Ground

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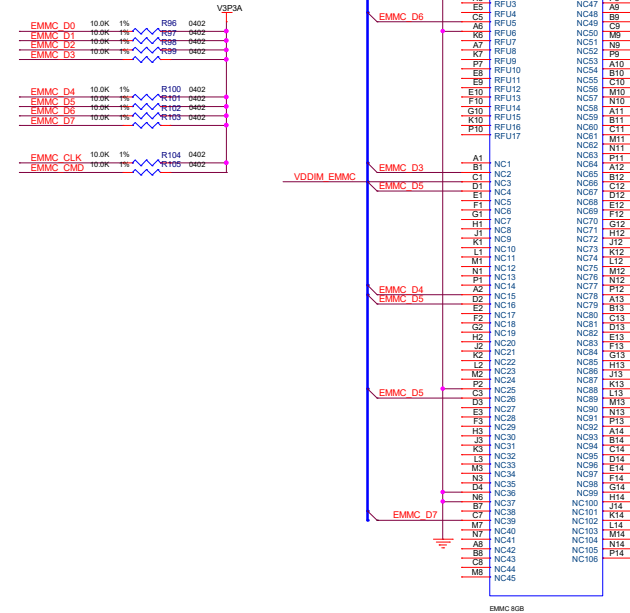
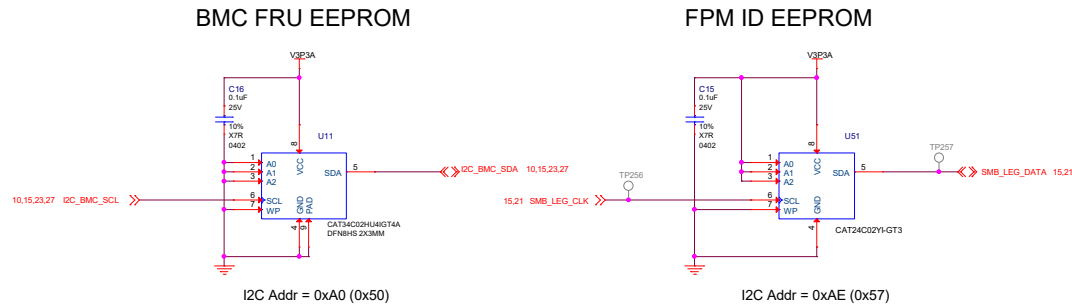
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		APPROV.	David C.	D.C.	17.03.19	
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eMMC Flash



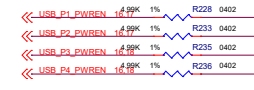
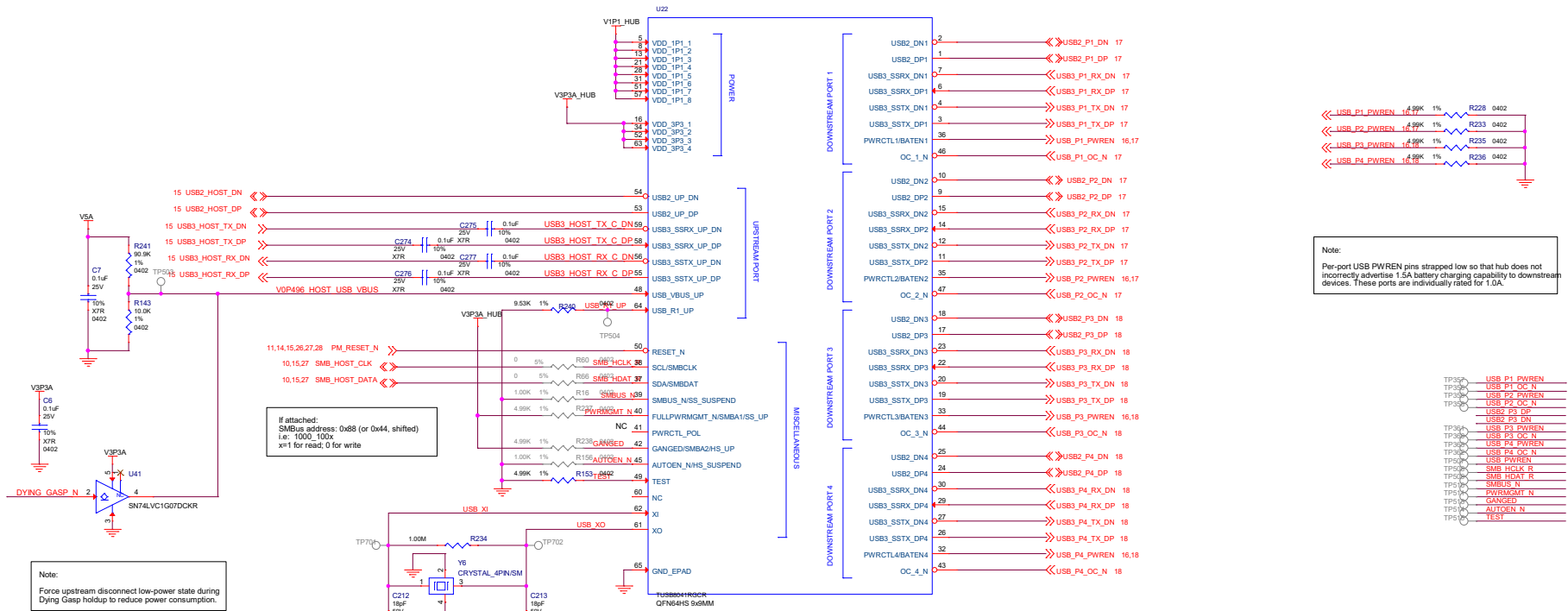
Route through NC pins to break out with standard TH vias (no micro vias). BGA153 is 0.5mm pitch.



EEPROMs, micro-SD, eMMC

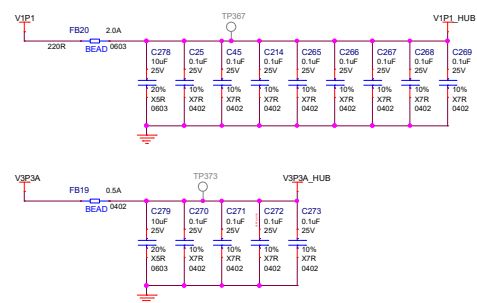
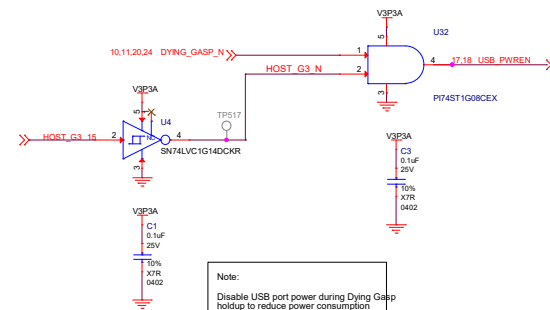
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USB 3.0/2.0 4-Port Hub

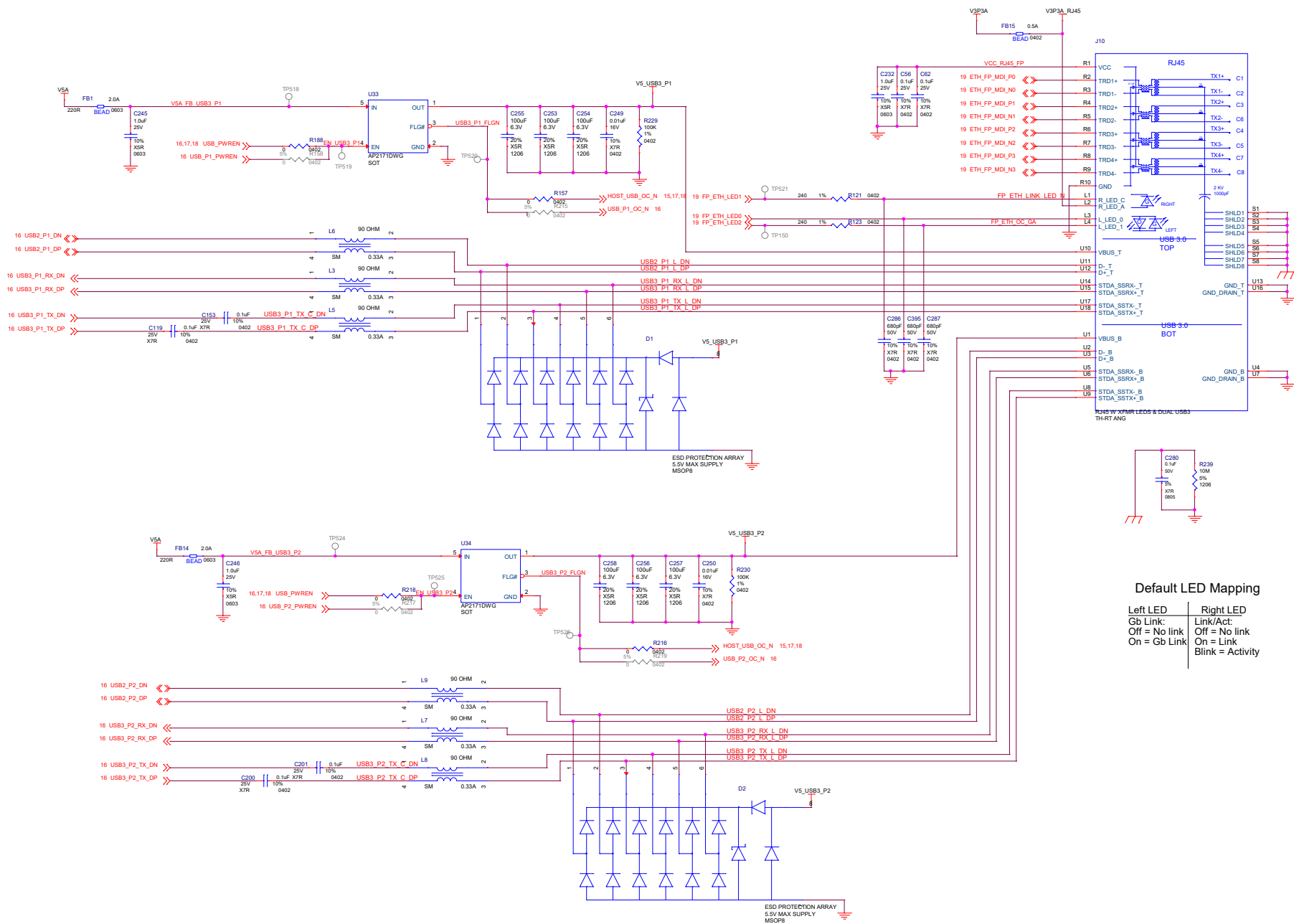


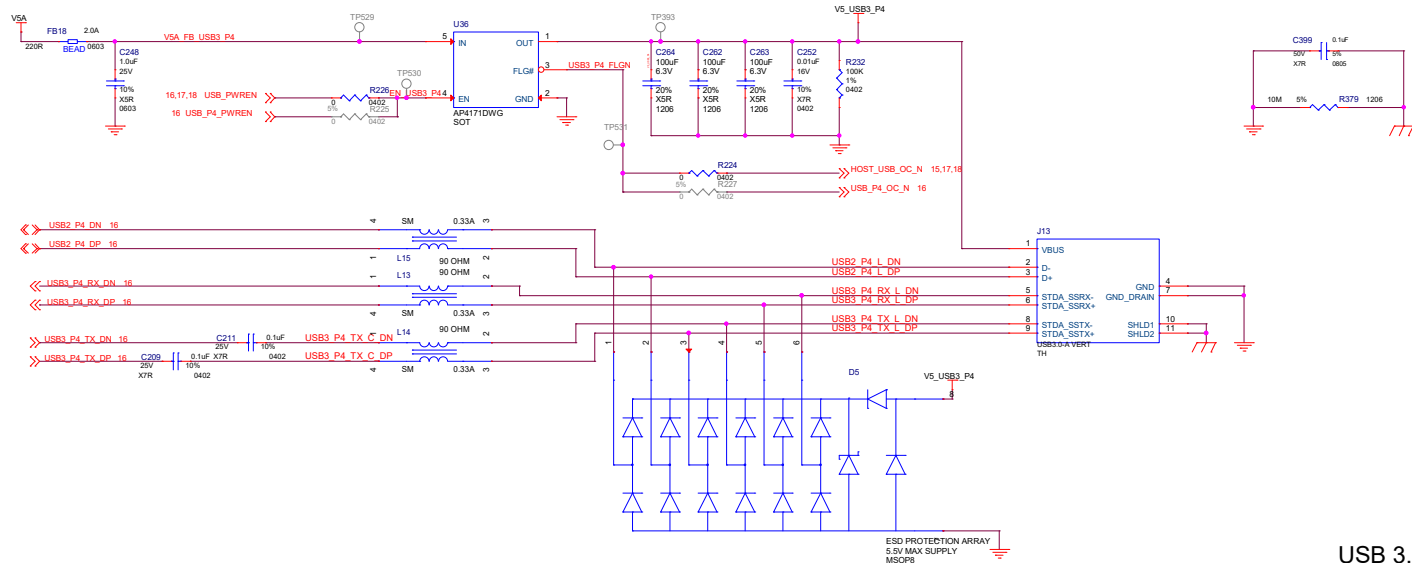
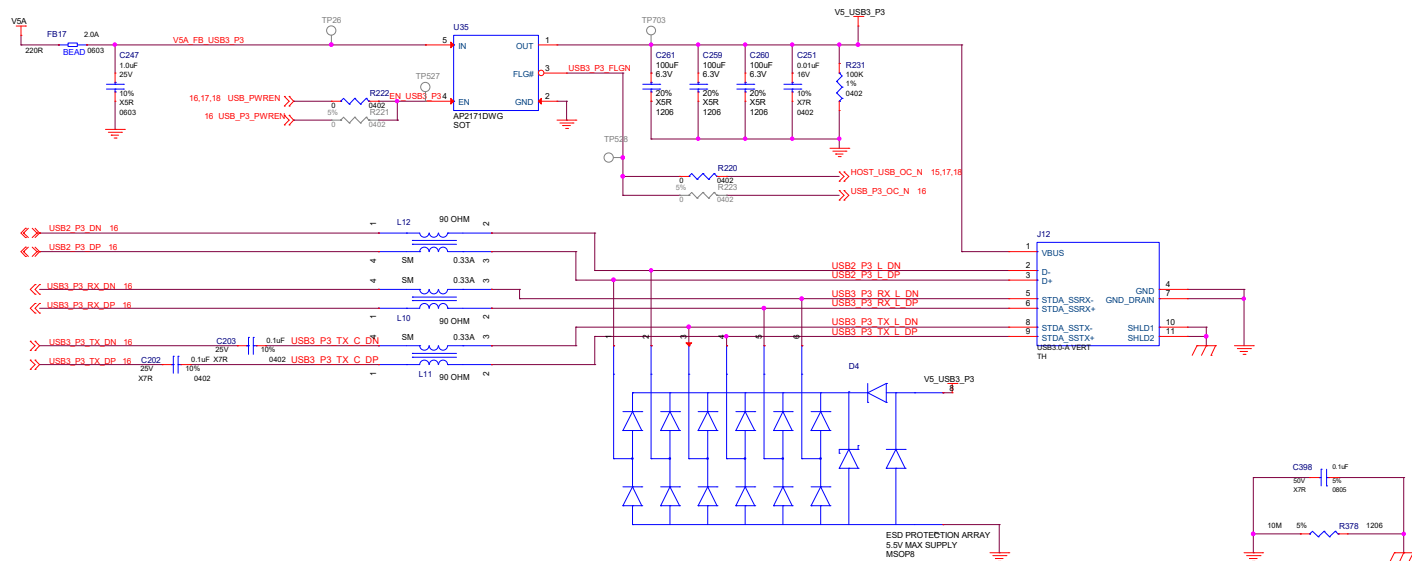
Note:
Per-port USB PWREN pins strapped low so that hub does not incorrectly advertise 1.5A battery charging capability to downstream devices. These ports are individually rated for 1.0A.

TP357	USB P1 PWREN
TP358	USB P1 OC_N
TP359	USB P2 PWREN
TP360	USB P2 OC_N
TP361	USB P3 PWREN
TP362	USB P3 OC_N
TP363	USB P4 PWREN
TP364	USB P4 OC_N
TP365	SMBUS_N
TP366	SMBUS_I
TP367	PWRMGMT_N
TP368	CHARGED
TP369	AUTOTEN_N
TP370	TEST



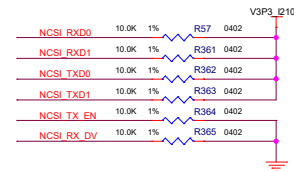
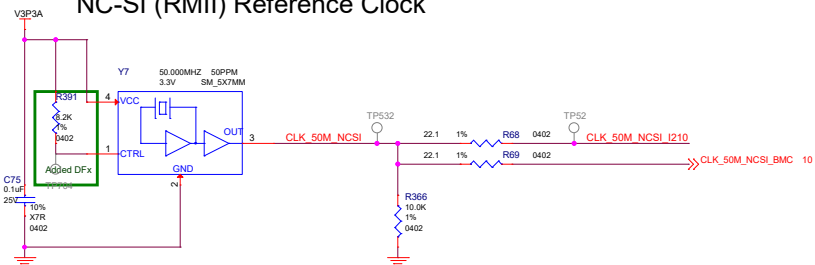
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				SHEET: 18	of SHEETS: 35	



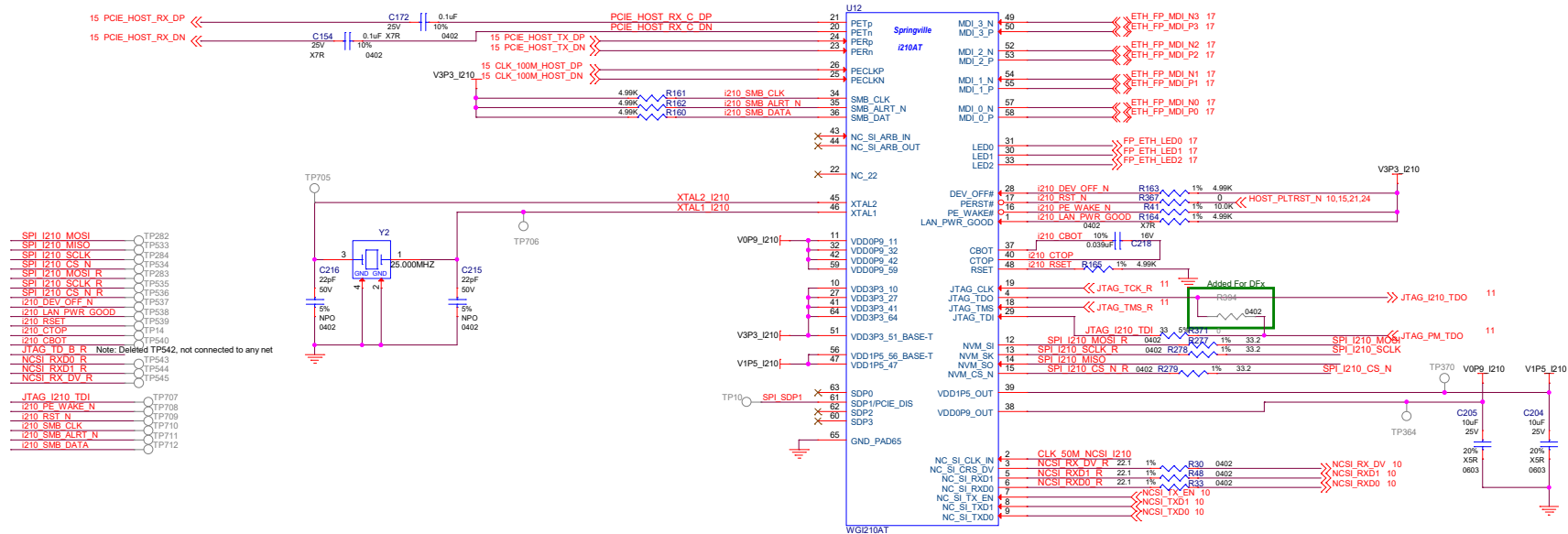


USB 3.0/2.0 Back Panel Ports

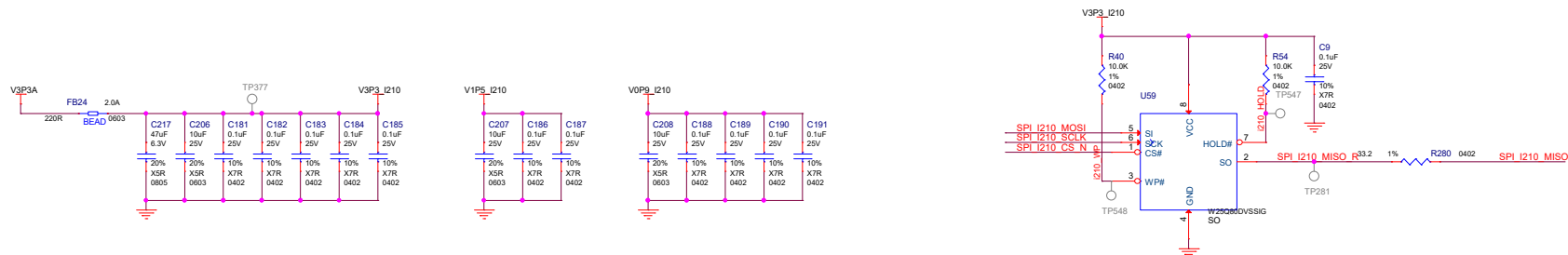
NC-SI (RMII) Reference Clock



Host GbE MAC/PHY With BMC NC-SI Sideband

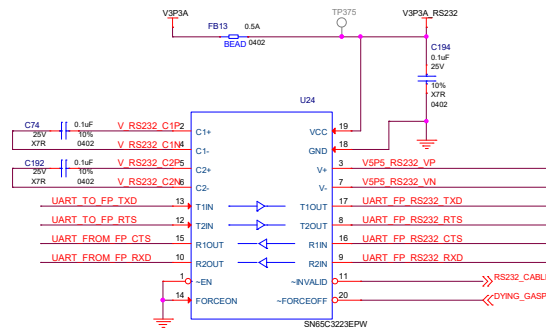
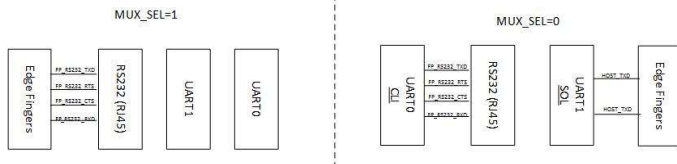
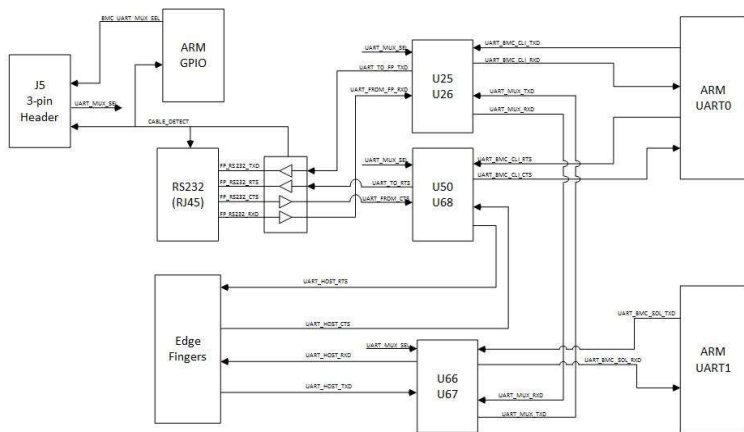


i210 NVM Flash



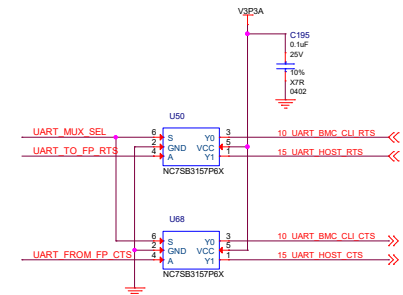
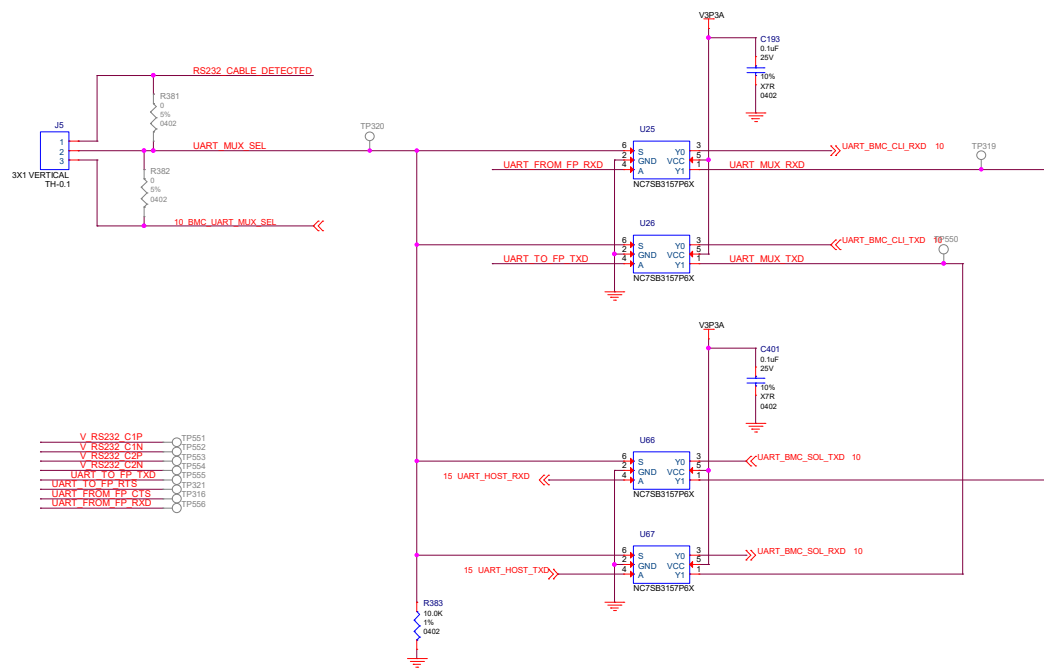
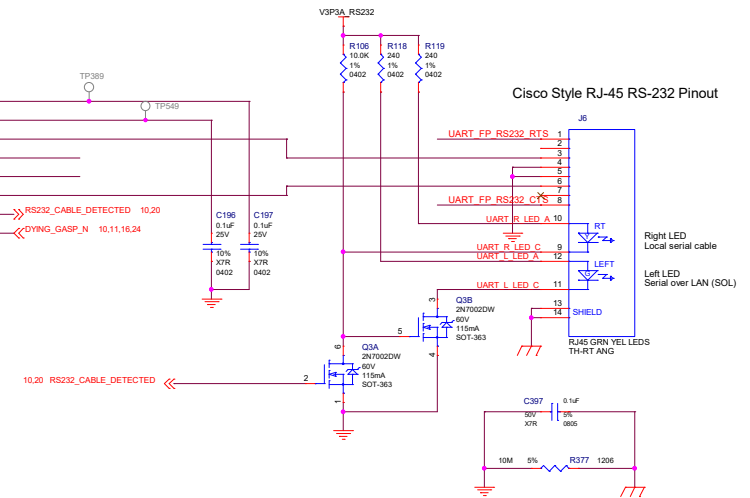
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				DATE :	David C.	D.C. 17.03.19
				SHEET : 19 of SHEETS : 38		

Host Console Port



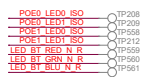
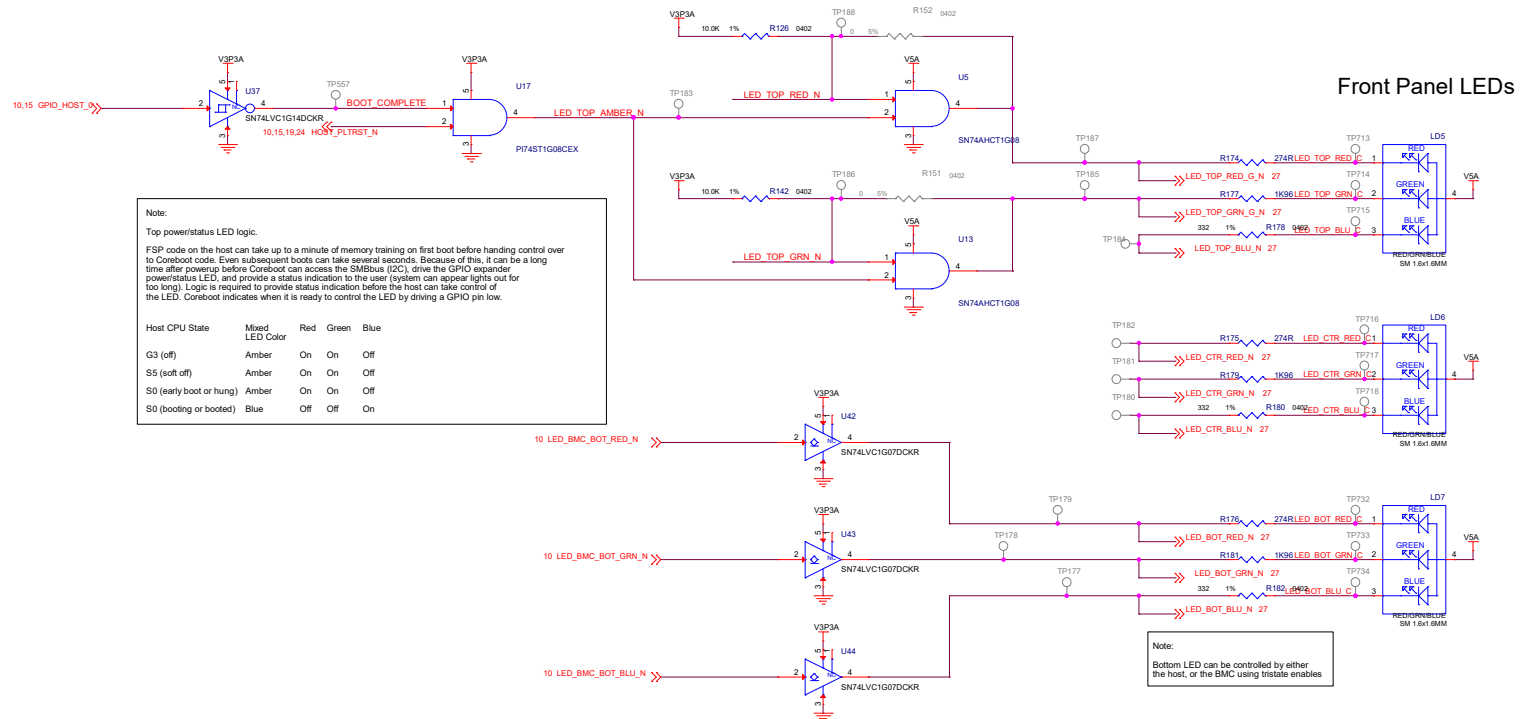
Note:
Disable console during Dying Gasp
holdup to reduce power consumption

Note:
RS-232 transceiver INVALID output is used to mux the host console
UART to either Serial over LAN (SOL) to the BMC, or to the local RJ-45
connector. LEDs on the RJ-45 indicate whether in SOL or local console mode.

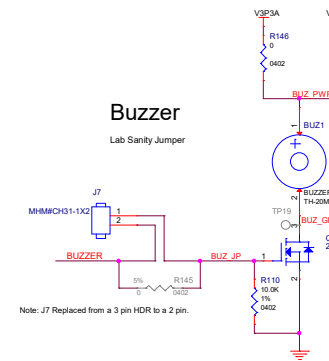
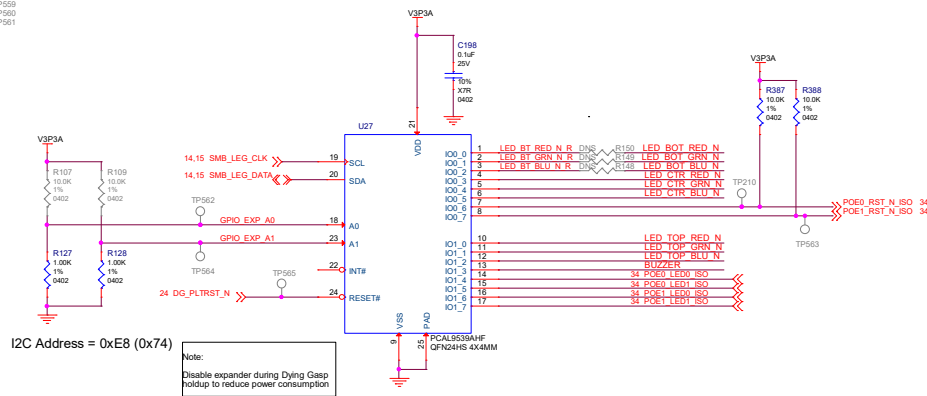


CPU Console, BMC Console

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DATE : Sunday, March 17, 2019	Monday, February 12, 2018	PROV	
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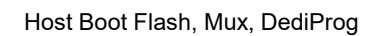


GPIO Expander

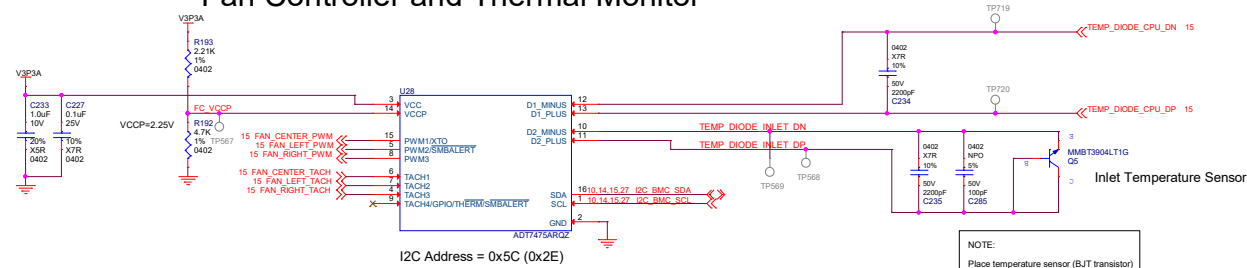


GPIO Expander, Front Panel LEDs, Buzzer

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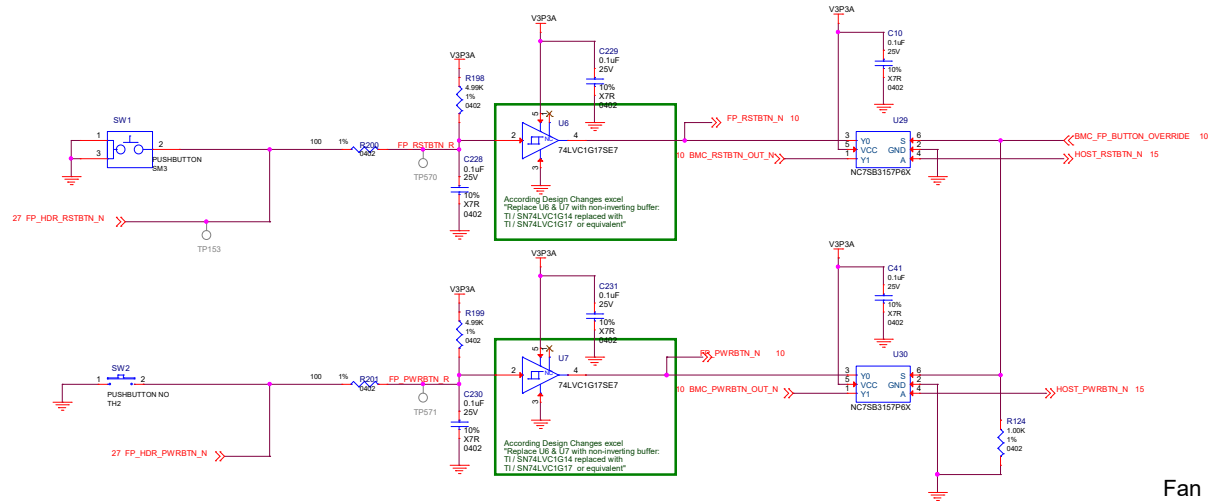


Fan Controller and Thermal Monitor



Fan Controller and Thermal Monitor

Power and Reset Pushbuttons



Fan Controller/Thermal Monitor, Buttons

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DATE: Sunday, March 17, 2019		Nadav Yule	N.Y.	17.03.19	
Monday, February 12, 2018		David C.	D.C.	17.03.19	
R208		SHEET: 23 of SHEETS: 35			

Diagram illustrating a 12V to 5V DC-DC converter circuit. The circuit includes a MOSFET (Q1, S8410N-14G6S), a diode (U48, 1N4001), and a capacitor (C281, 4700uF). The input is V12_IN (12V) and the output is V5012A (12V). The circuit is powered by a 12V source and includes a 5V output filter.

NOTE:

1. Reference threshold is 2.495V. Trip point (FET turn off) is set to 4.33 V.
2. Board normal max power consumption is 43.3 W.
3. With non-essential circuits disabled, board max power consumption is 18.3 W.
4. Capacitor bank provides 9, 18, or 27 ms holdup time at reduce (depends on how many caps populated)
5. Holdup gives BMC time to transmit Dump Gasp packet(s) on the close out filesystem, and shut down gracefully.

1. FET Reson will cause extra loss and associated heat generation.
2. Place FET on top layer to expose package to airflow.
3. Use large plane shapes for FET drain and source for heat dissipation, especially on the top layer where they are exposed to airflow and preferably duplicated on the bottom layer for additional exposure.
4. Bury FET drain and source pads in surface plane shapes (do not use them as relief spokes).
5. The outer layer plane shapes heavily into inner layer large plane shapes with large via arrays for additional heatsinking capability.

1. Reference threshold is 2.495V. Trip point (FET turn off) set to 10.4V.
2. Board normal max power consumption is 43.3 W.
3. With non-essential circuits disabled, board max power consumption is 18.9 W.
4. Capacitor bank provides 9, 18, or 27 ms holdup time at reduced 18.9 W power level.
(depends on how many caps populated)
5. Holdup gives BMC time to transmit Dying Gasp packet(s) on the LAN and/or WWAN, close out filesystem, and shut down gracefully.

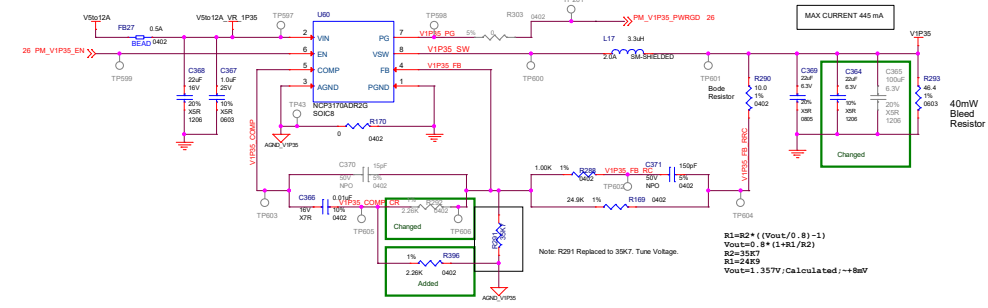
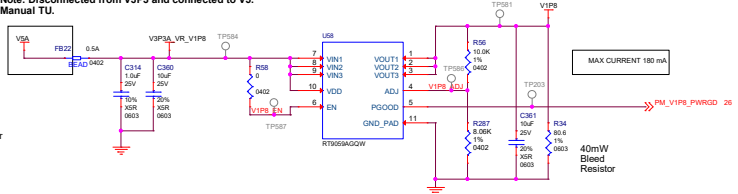
NOTE:

Sense threshold is 1.226V. Trip point set to 11V.
Monitor output is 5.5 u minimum pulse.
Output is open-drain; requires pullup.

Sense threshold is 1.226V. Trip point set to 11V.
Monitor output is 5.5 μ s minimum pulse.
Output is open-drain; requires pullup.



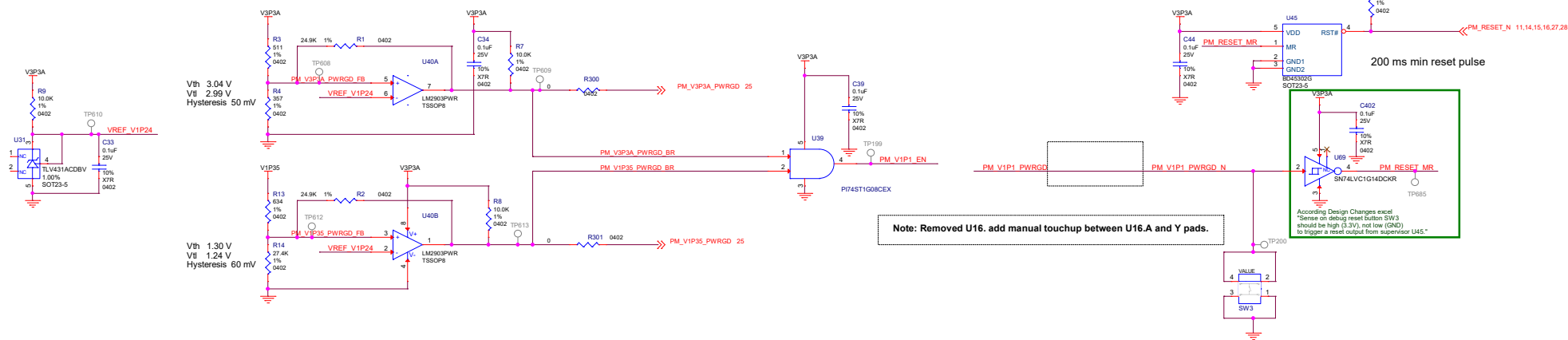
Note: Disconnected from V3P3 and connected to V5.
Manual TU.



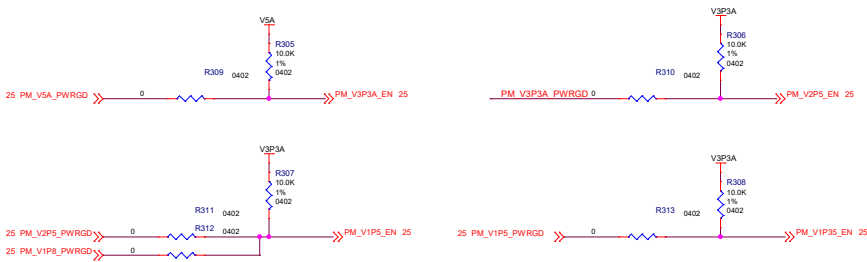
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NAME	SIGN	DATE																			
CHECK Nadia Yafe	N.Y.	17.03.19																			
APPROV. David C.	D.C.	17.03.19																			
SHEET: 25 OF SHEETS: 35																					
SIZE: Custom	REV No.: R208																				
DATE: Sunday, March 17, 2019 Monday, February 12, 2018																					

SoC Power Sequence Comparator

Voltage Supervisor / Reset Generation



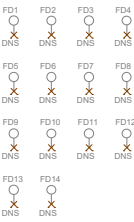
Power Sequence



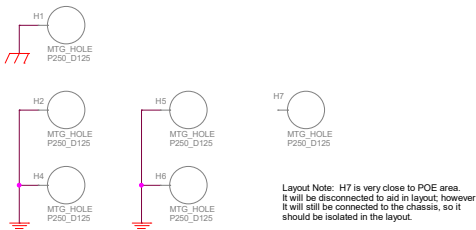
Power: Misc Regulators and Sequence

DRAWING No.: 80200-0175-G00		80200-0175-G00		APPROVALS		SILICONIC Ltd.
SIZE: Custom	REV No.: R208	Power: Misc Regulators		CHECK	NAME	DATE
DATE: Sunday, March 17, 2019		Monday, February 12, 2018		Nadev Yade	N.Y.	17.03.19
				David C.	D.C.	17.03.19
				SHEET: 26 of SHEETS: 35		

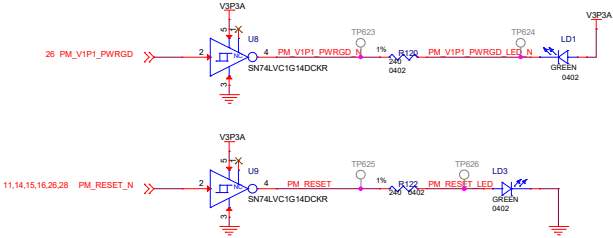
Fiducials



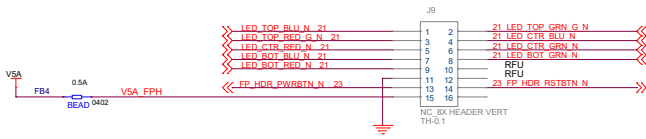
Mounting Holes



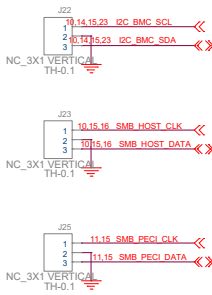
Debug LEDs



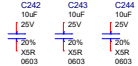
Front Panel Header



Debug Headers

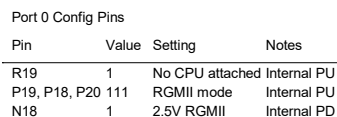


Light Blocking Caps For LED Lightpipe



Note
Light-blocking caps must be as tall as possible and still fit underneath the 1.40 mm lightpipe hood. Capacitor height must include both cap thickness and some tolerance for solder thickness. This cap was selected because the max height is 1.0 mm, allowing a little bit of tolerance for solder paste.

Misc, Debug LEDs

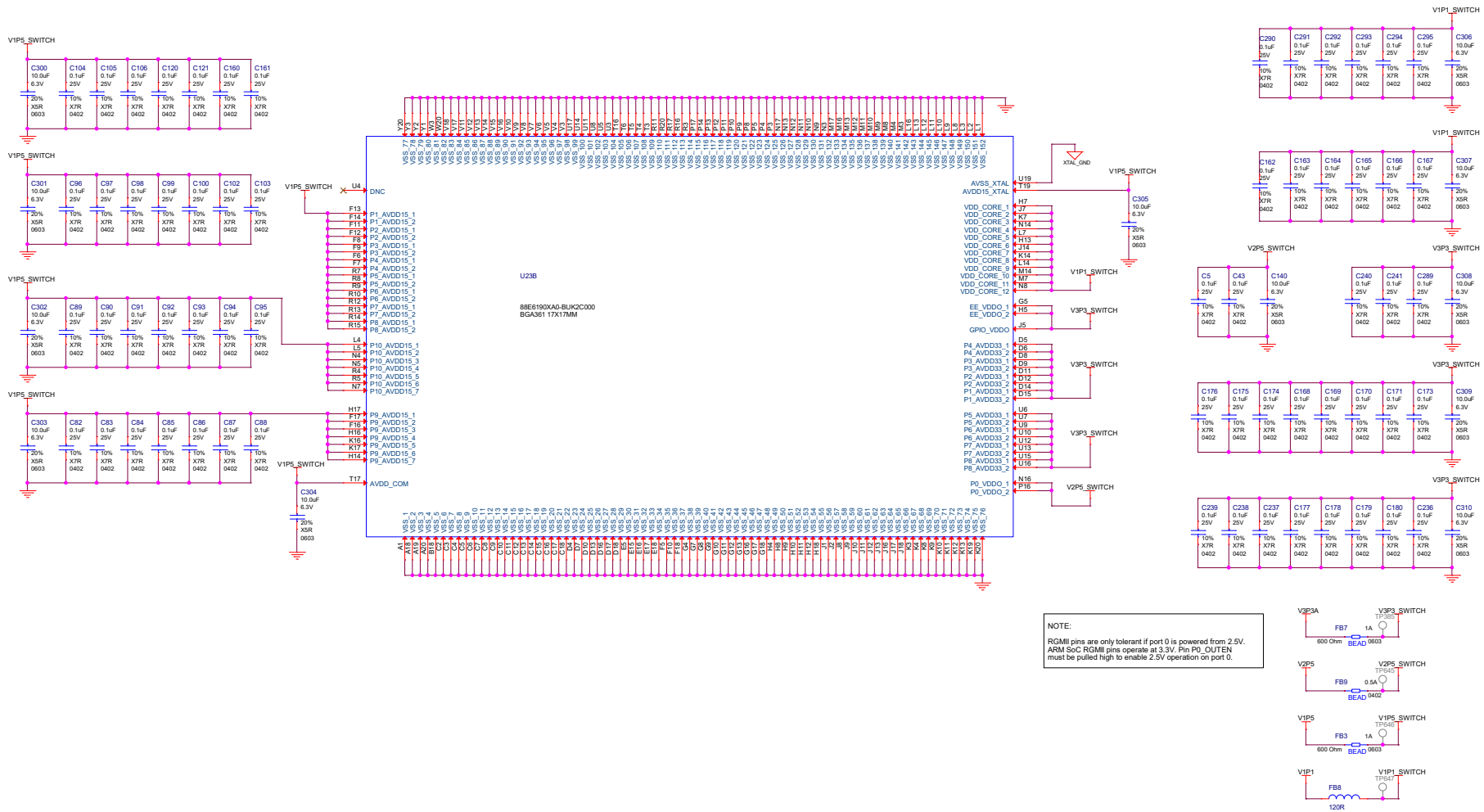


Signal	Value	Setting	Notes
C3_LED	1	Disable EEE	Internal PD
C2_LED	0	Separate LNK/ACT and SPD LEDs	Internal PD
C0_LED	1	Full-duplex flow control all ports	Internal PD
R4_LED	0	MDIO address = 0x10	Internal PU, value inverted
R3_LED	1	MDIO address = 0x10	Internal PU, value inverted
R2_LED	1	MDIO address = 0x10	Internal PU, value inverted
R1_LED	1	MDIO address = 0x10	Internal PU, value inverted
R0_LED	1	MDIO address = 0x10	Internal PU, value inverted
SW_24PN	1	Normal mode, no cross-chip cascading	Internal PU
SW_VDDOS	0	GPIO pins powered by 3.3V (not 2.5V)	Internal PU

1. Switch CPU MDIO is set for multi-cp address mode with address = 0x10.
2. The e-CPE system architecture requires that switches located on Network Modules (NMs) must have their MDIO addresses set to 0x10 when in NM slot 0 and 0x11 when in NM slot 1.
3. Set MDIO addresses to 0x10 for NM slot 0. This conflicts with the LAN NMs running on NerveoNet-NS1 CPU.
4. Due to the merging of the Front Panel IO Module (FPM) with BMC and a NM for the switch in this design, the switch is merged with the always active NM slot 0. Therefore, no dynamic MDIO addressing is required and the MDIO address can be hardwired to 0x10.
5. Note that the actual MDIO address for this switch is the inverse of the 0x10 pin. This is because there are internal pullups. So strap these pins to 0x0F inverts to an effective MDIO address of 0x10.



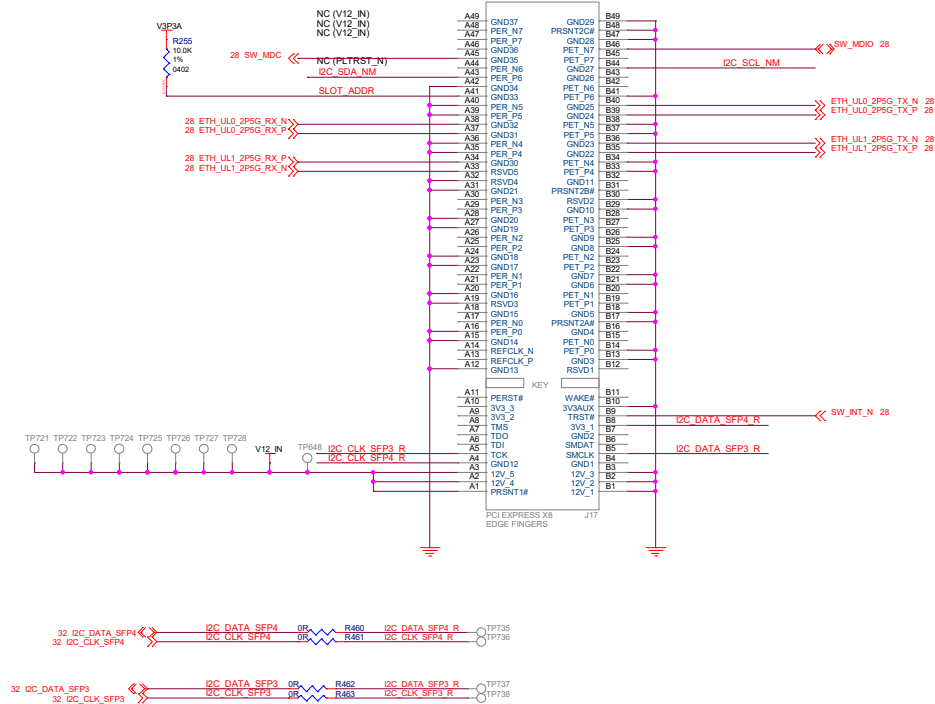
Front Panel Port #	Switch Port #
1	3
2	4
3	2
4	1
5	6
6	5
7	8
8	7



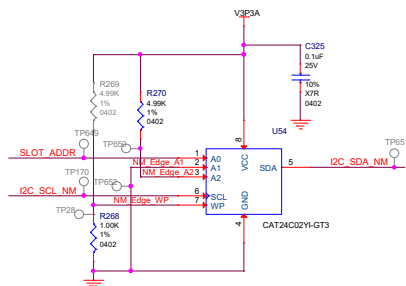
LAN Switch: Power

Blank Page

Motherboard NM Edge Fingers

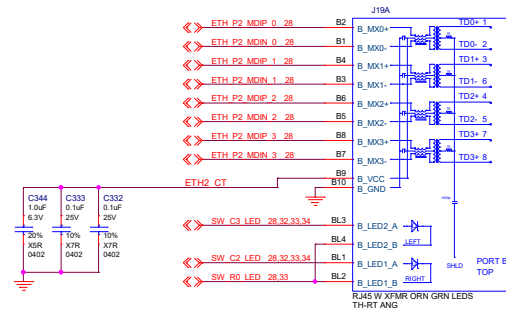


NM ID EEPROM

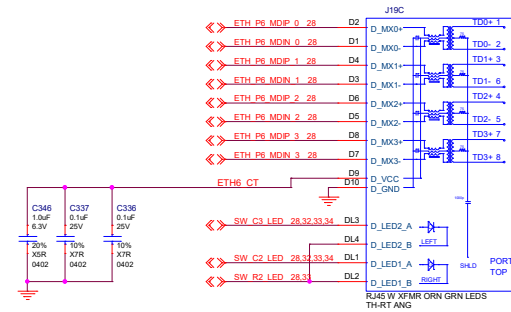


Network Module Edge Fingers

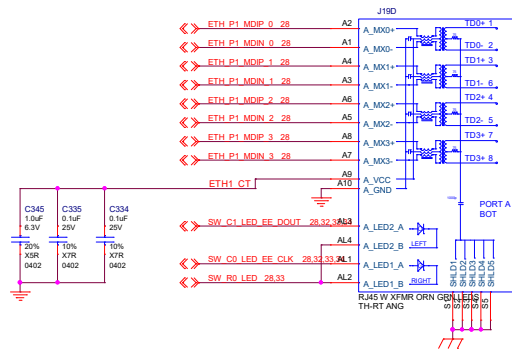
Port 3



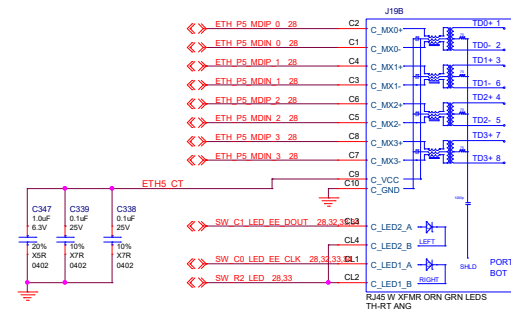
Port 5



Port 4



Port 6



Default LED Mapping

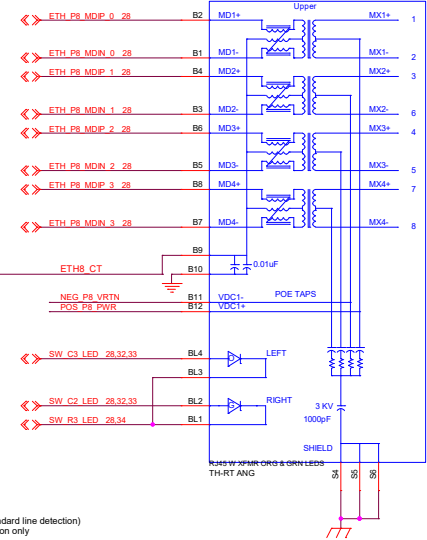
Left LED	Right LED
Gb Link:	Link/Act:
Off = No link	Off = No link
On = Gb Link	On = Link
	Blink = Activity



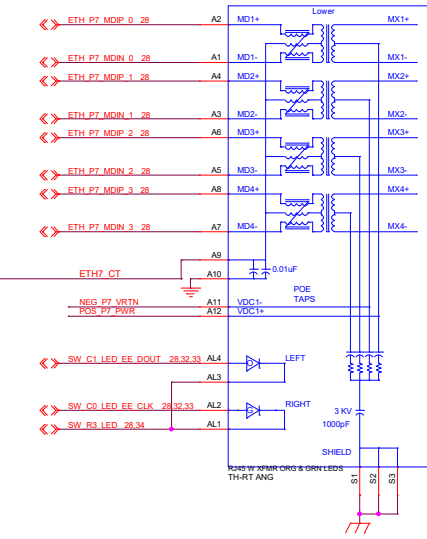
Ethernet RJ45 Connectors

DRAWING No.: 80204-0175-G00		80200-0175-300	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of R&D Group	
SIZE: Custom	REV No.: R208		CHECK	NAME	SIGN		DATE
			APPROV.	Nadav Yalo	N.Y.		17.03.19
DATE: Sunday, March 17, 2019				David C.	D.C.		17.03.19
Monday, February 12, 2018			SHEET: 33 of SHEETS: 35				

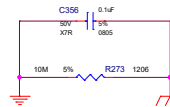
Port 7



PoE+ 54V input conn



Left LED	Right LED
Gb Link:	Link/Act:
Off = No link	Off = No link
On = Gb Link	On = Link
	Blink = Activity



Revision	Date	Description
X100	Date	Alpha prototype release
X200	Date	Beta prototype release
R100	18.04.2018	GA#1 release
R101	06.05.2018	uBMC FW Update - Fan in Auto Mode
R102	09.05.2018	uBMC FW Update - See Release Notes for full detail
R103	10.05.2018	Update Assembly Changes
R200	12.05.2018	GA#2 release
R205	27.11.2018	1. Customer request: Update FP LED color to be Amber (RED and GREEN) . Before change it is green yellow 2. Unified FP LED Color - All three LEDs to the same color grade. 3. Bottom FP LED will be controlled only via the uBMC – eliminate potential contention between the x86 and uBMC.Functional Team(s):No Privilege

R208	04.12.2018	Update of 80200-0150-G02 – XS Compute Board
		Name XDP Debug Port(COT000136ý) Power for offboard HDD/SSD SATA - A SATA/SATADOM - B Reference Designator J14 J10 J18 J17
		Update of 80200-0175-G00 – XS IO Board Name Buzzer (EBZ000001ý) Debug Headers Front Panel Header Reference Designator BUZ1 J22, J23, J25 J9

DRAWING No. : 80204-0175-G00		80200-0175-G00 Revision History	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group		
SIZE : A			REV No. : R208			NAME		SIGN	DATE
DATE : Sunday, March 17, 2019					CHECK	Nadav Yafe		N.Y.	17.03.19
Monday, February 12, 2018					APPROV.	David C.		D.C.	17.03.19
					SHEET : 35 of SHEETS : 35				