

vE-CPE Motherboard

Revision History

X100	7/12/17	Initial Alpha prototype release
X200	11/10/17	Beta prototype release
X202	11/10/17	Beta prototype release
R100	20/04/18	Beta prototype release
R200-02	15/05/18	DFx production release
R200-03	17/05/18	DFx production release 2
R202-00	06/12/18	BOM Cleanup for Mass prodcutcion

ADI PN	Intel SKU	Features				
		Cores	TDP (W)	QuickAssist	Temperature	Stepping
4460-0096	C3338	2	8.75	No	Standard	B0
4460-0102	C3558	4	16	Yes	Standard	B1
4460-0103	C3758	8	25	Yes	Standard	B1
4460-0107	C3858	12	25	Yes	Standard	B1
4460-0108	C3958	16	31	Yes	Standard	B1
4460-0106	C3308	2	9.5	Yes	Extended	B1
4460-0104	C3508	4	11.25	Yes	Extended	B1

Variants

Feature	G00	G01	G02	G03	G04
Product SKU	Intel Dev	Intel Dev	AT&T XS	Intel Dev	RAD
Configuration	Desktop	Desktop	Desktop	Desktop	Desktop
SoC SKU	C3758	C3958	C3558	C3758	C3758
# Cores	8	16	4	8	8
# HSIO Lanes Supported	20/20	20/20	12/20	20/20	20/20
DDR4 Down Total	16 GB	16 GB	8 GB	8 GB	16 GB
# DDR4 Ranks	2/2	2/2	1/2	1/2	2/2
DDR4 Bus Width	64 bit	64 bit	64 bit	64 bit	64 bit
DDR4 ECC	Yes	Yes	Yes	Yes	No
eMMC	16 GB	16 GB	64 GB	64 GB	No
M.2 WWAN/SATA SSD Slot 3042	Yes	Yes	Yes	Yes	Yes
M.2 WWAN/SATA SSD Slot 30110	Yes	Yes	Yes	Yes	Yes
mPCIe Wi-Fi/BT, WWAN Slot	Yes	Yes	Yes	Yes	Yes
SATA3 Connector	Yes	Yes	Yes	Yes	Yes
SATADOM Connector	Yes	Yes	Yes	Yes	Yes
PCIe x4 Slot	Yes	Yes	Yes	Yes	Yes
Power Connector	ATX 12V	ATX 12V	ATX 12V	ATX 12V	ATX 12V
Cooling	Chassis Fans	Chassis Fans	Chassis Fans	Chassis Fans	Chassis Fans
Proto/Debug Features	Yes	Yes	Yes	Yes	Yes
USB2.0 hub for long M.2 slot	No	No	No	No	No

Notes:

1. This is an EE7 variant design. DNI (non-inserted) and variable part number attributes displayed only through Variant Manager.

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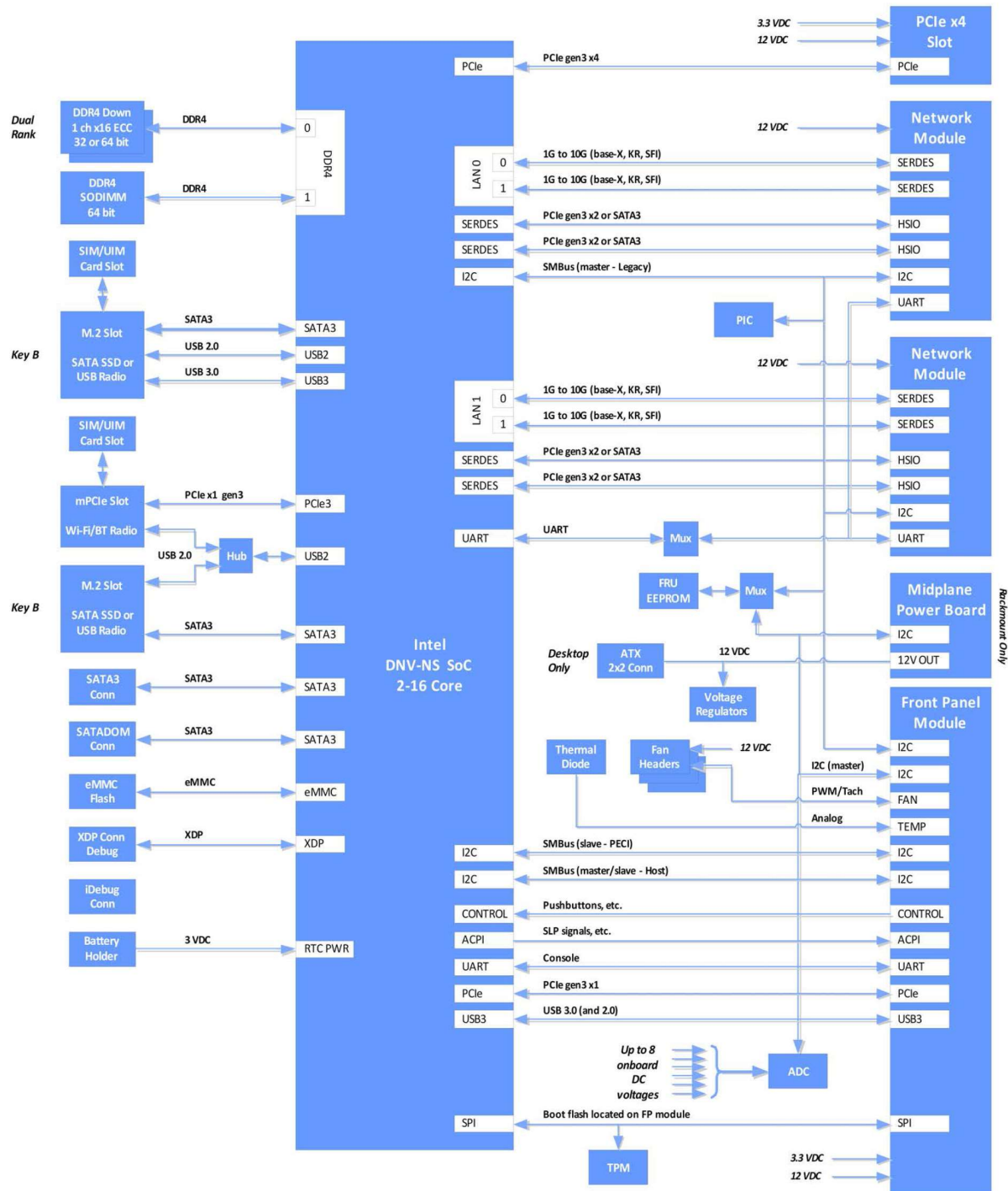
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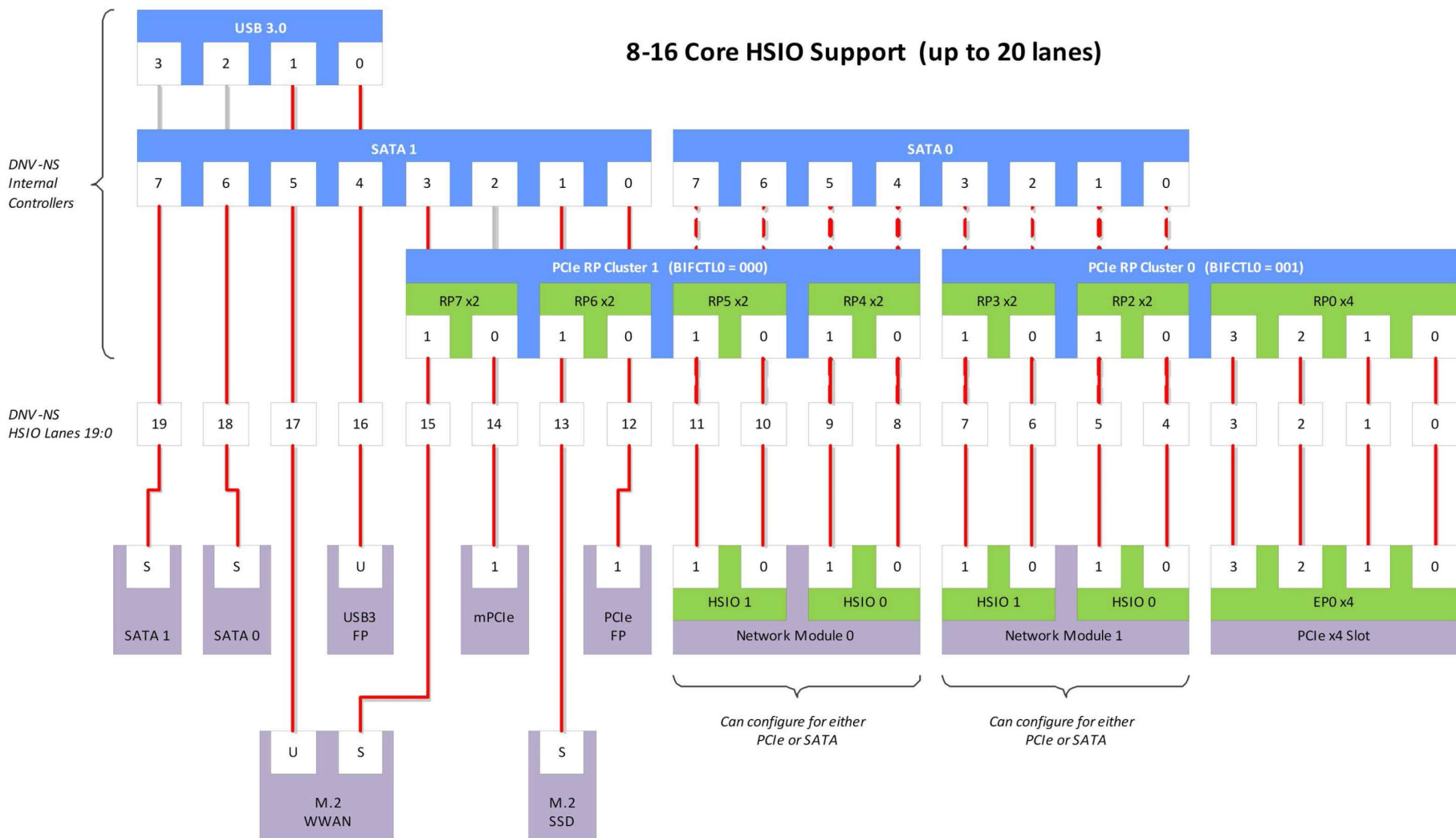
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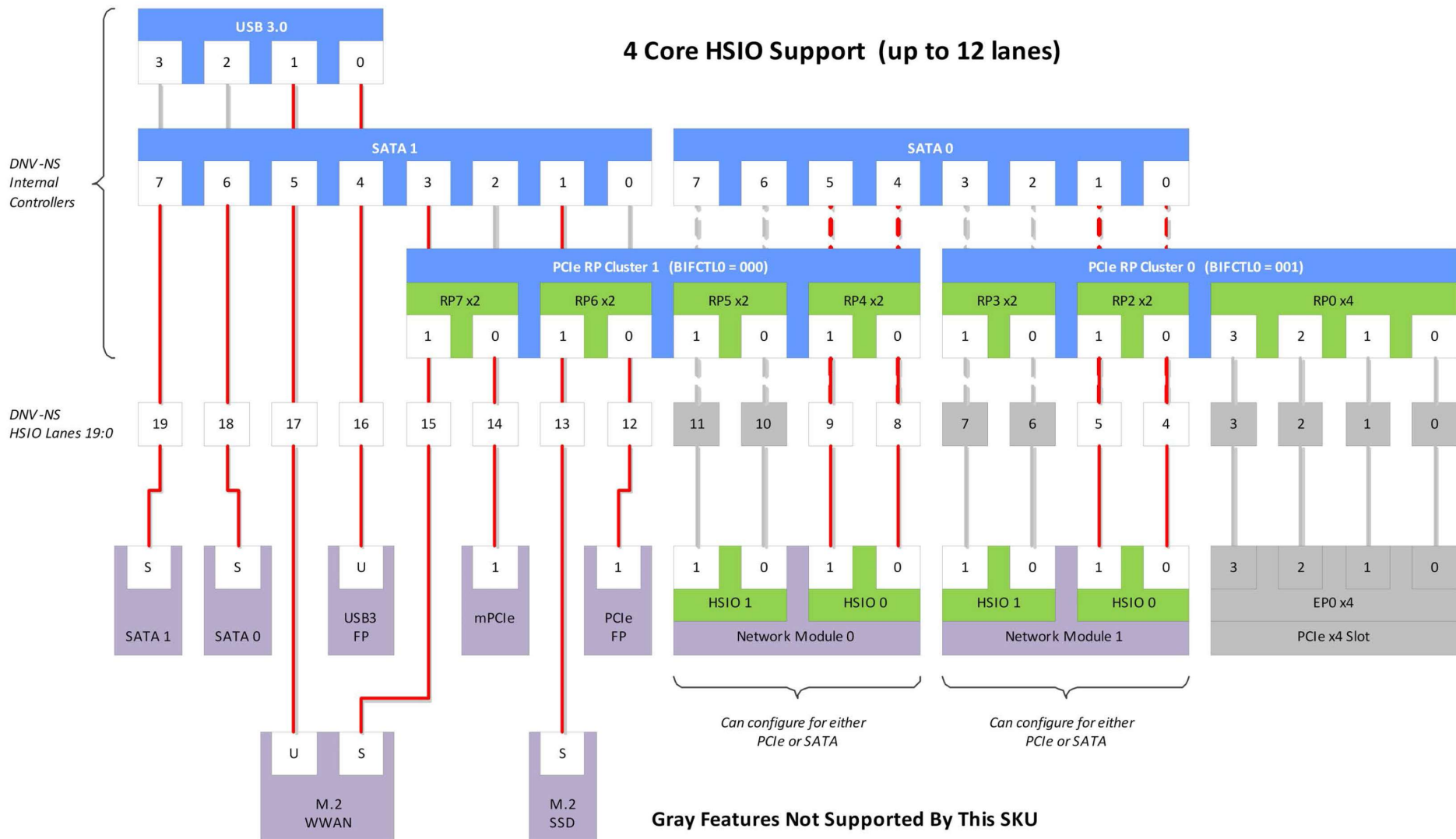
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PAGE	DESCRIPTION
1	TITLE PAGE
2	INTEL DISCLAIMER
3	ADI DISCLAIMER
4	BLOCK DIAGRAM
5	HSIO CONFIGURATION (8-16 CORES)
6	HSIO CONFIGURATION (4 CORES)
7	POWER SEQUENCING DIAGRAM
8	POWER BLOCK DIAGRAM
9	SMBUS/I2C DIAGRAM
10	CLOCKING DIAGRAM
11	SoC / DDR CH0
12	SoC/ DDR CH1
13	SoC / LAN, MISC
14	SoC / Debug, eMMC, USB, MISC
15	SoC / HSIO
16	SoC / POWER
17	SoC / Decoupling
18	SoC / GND
19	DDR4 MEMDOWN CH0-DQ[0-31]R0
20	DDR4 MEMDOWN CH0-DQ[32-63]R0
21	DDR4 MEMDOWN CH0-DQ[0-31]R1
22	DDR4 MEMDOWN CH0-DQ[31-63]R1
23	DDR4 MEMDOWN CH0 ECC & TERM
24	DDR4 SODIMM
25	TPM, DEBUG CONNECTORS
26	PCIe x4 EXPANSION SLOT
27	RADIO CARD SLOTS (WWAN, WI-FI)
28	SATA, SATADOM, M.2 SSD CARD SLOT, USB
29	FRONT PANEL INTERFACES
30	ADC, VOLTAGE DIVIDERS
31	3.3V ISOLATION
32	BLANK PAGE
33	BLANK PAGE
34	BLANK PAGE
35	eMMC
36	BLANK PAGE
37	BLANK PAGE
38	BLANK PAGE
39	POWER SEQUENCE
40	THERMAL CIRCUITRY, FAN CONNECTORS
41	BLANK PAGE
42	BLANK PAGE
43	POWER
44	POWER
45	POWER
46	POWER
47	POWER
48	POWER
49	POWER
50	LEDS, POWER ENTRY, MISC
51	CHANGE LOG

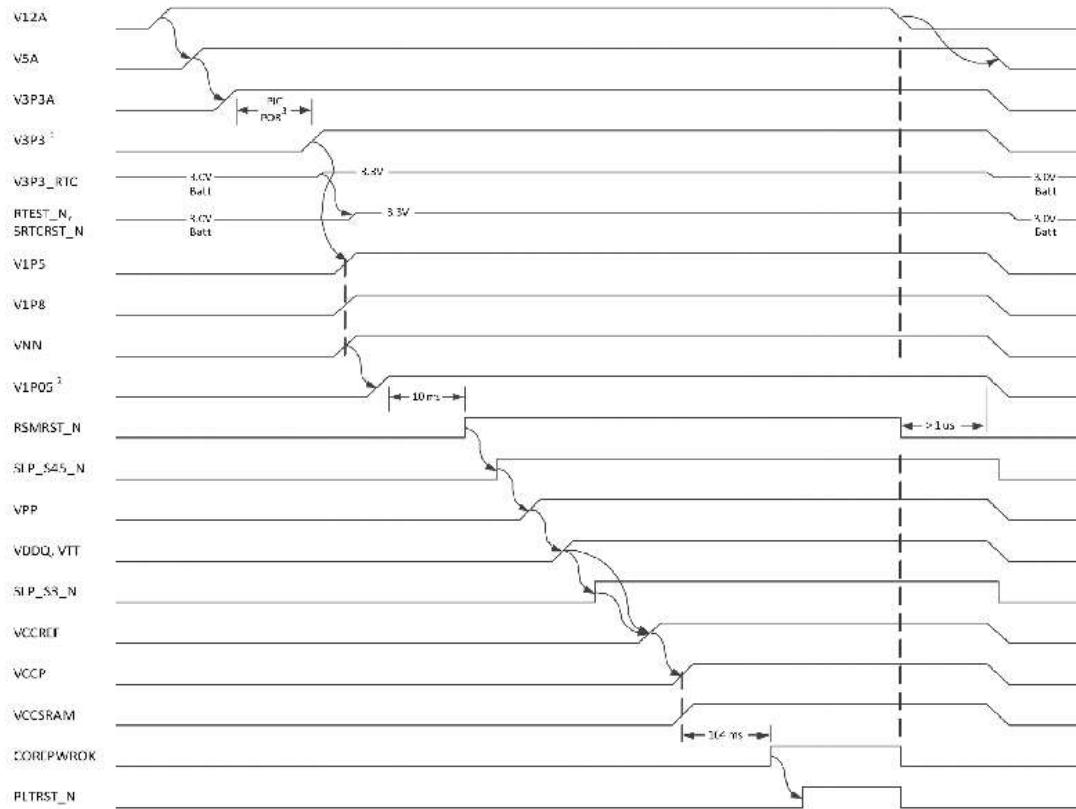


8-16 Core HSIO Support (up to 20 lanes)





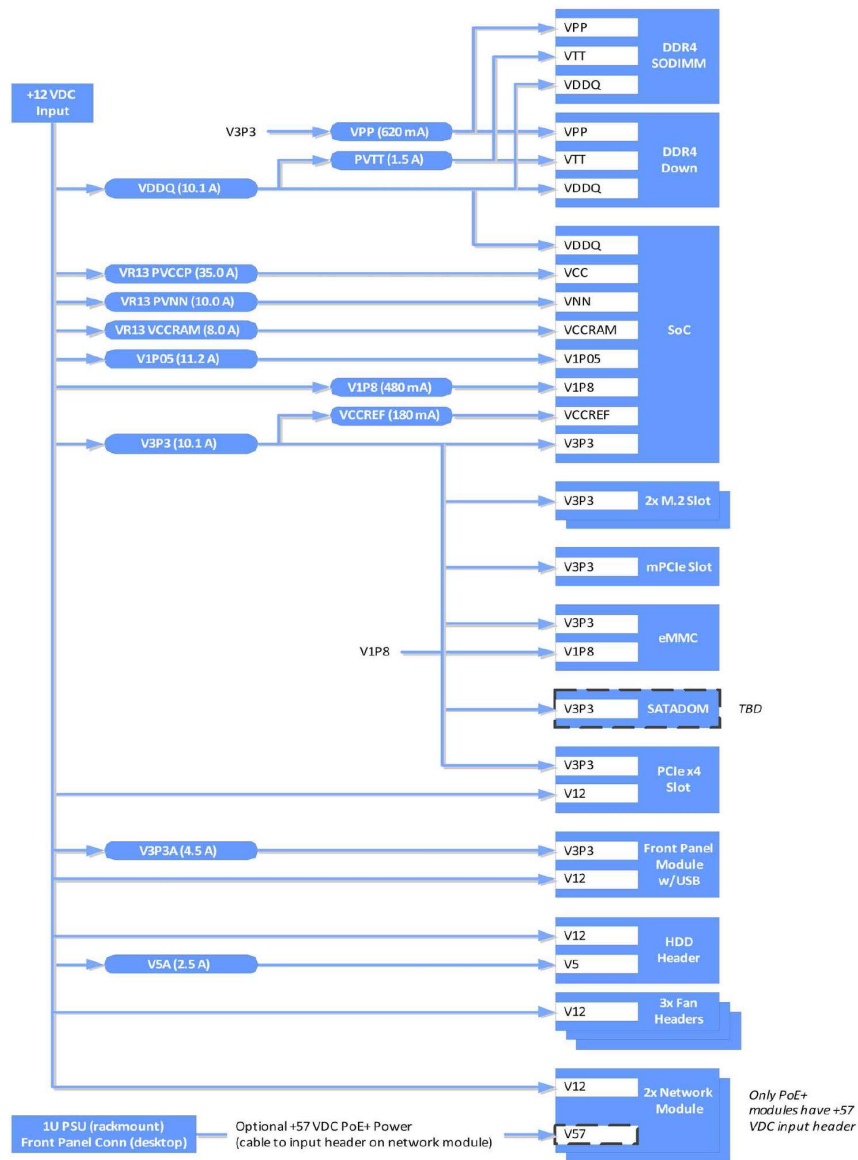
POWER SEQUENCING DIAGRAM



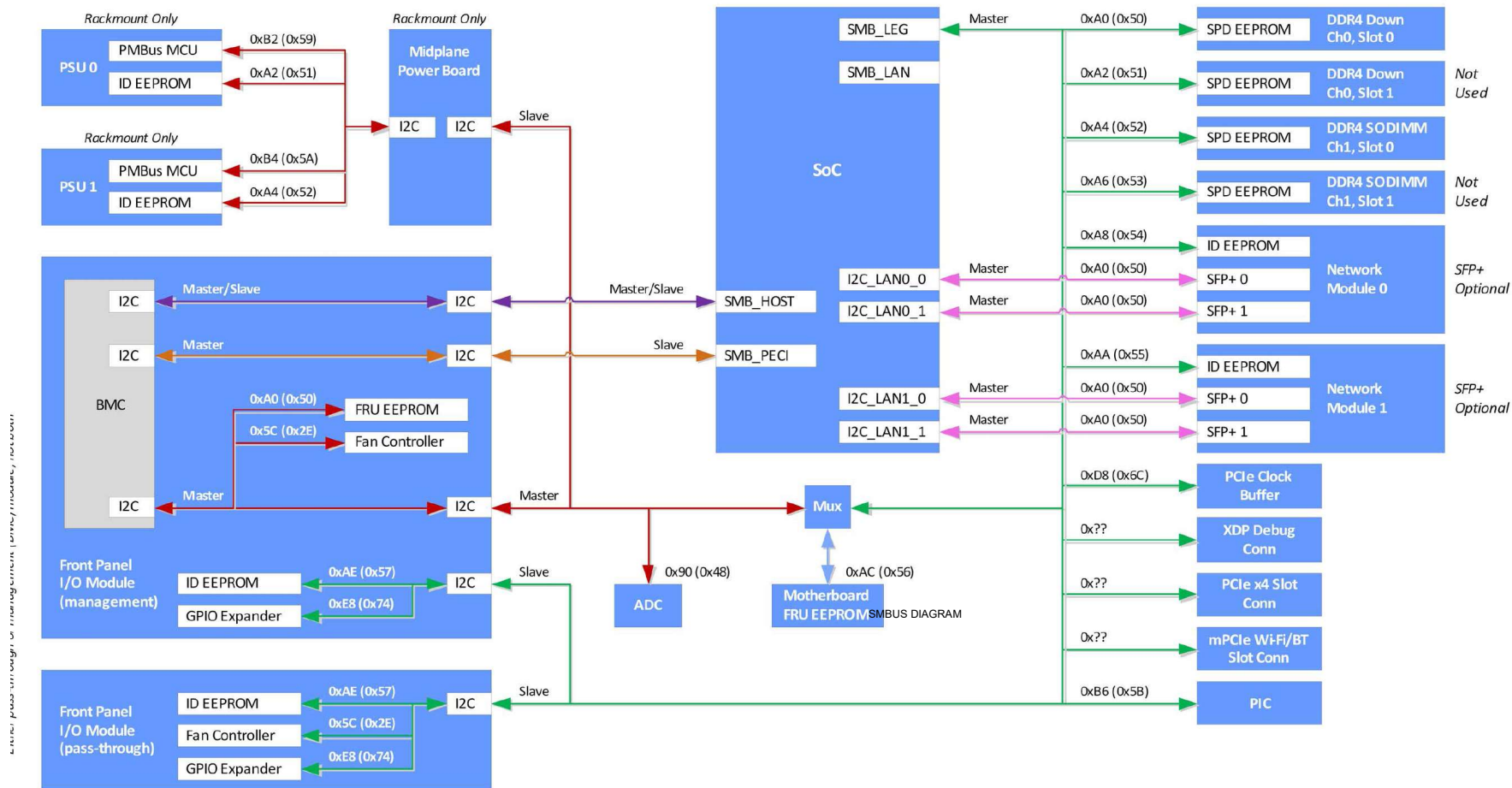
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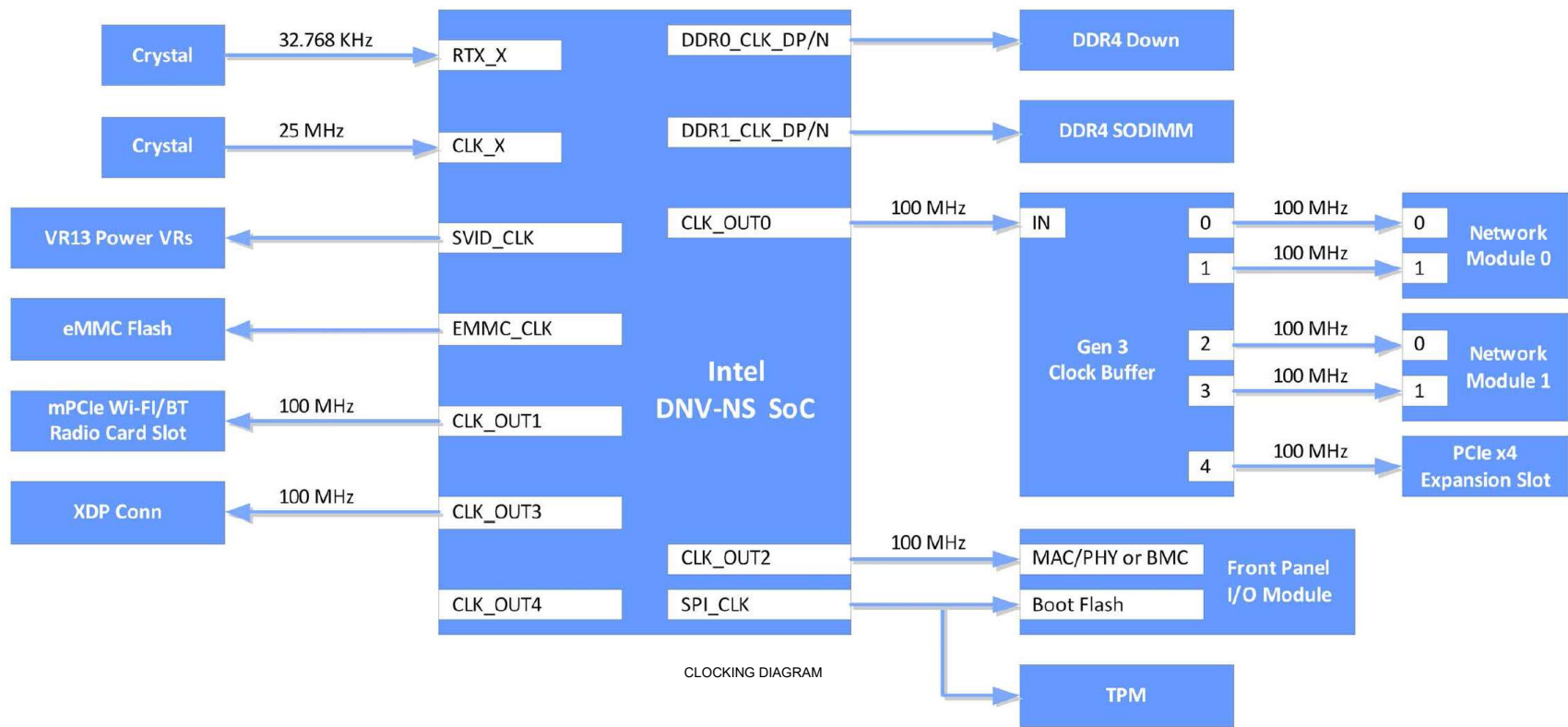
1. The following signals rise with V3P3: RSTBUTTON_N, PWRBUTTON_N, WAKE_N, SUS_STAT_N, SUSCLK (toggling), CLK_OUT[4:0] (toggling).
2. The following signals rise with V1P05: PROCHOT_N, THERMTRIP_N.
3. PIC power on reset 40 - 140 ms.

DRAWING No. : 80204-0150-G02		POWER SEQUENCING	APPROVALS				SILICOM Ltd. Conectivity Solutions A Member of RAD Group
AssyG02				NAME	SIGN	DATE	
SIZE : B	REV No. : R202-00		CHECK				
DATE : Thursday, November 29, 2018			APPROV.				
SHEET : 7		AT&T Compute Board	of SHEETS : 51				



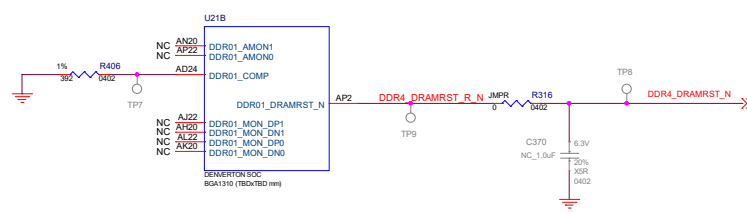
POWER BLOCK DIAGRAM



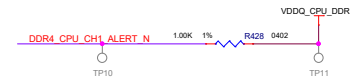
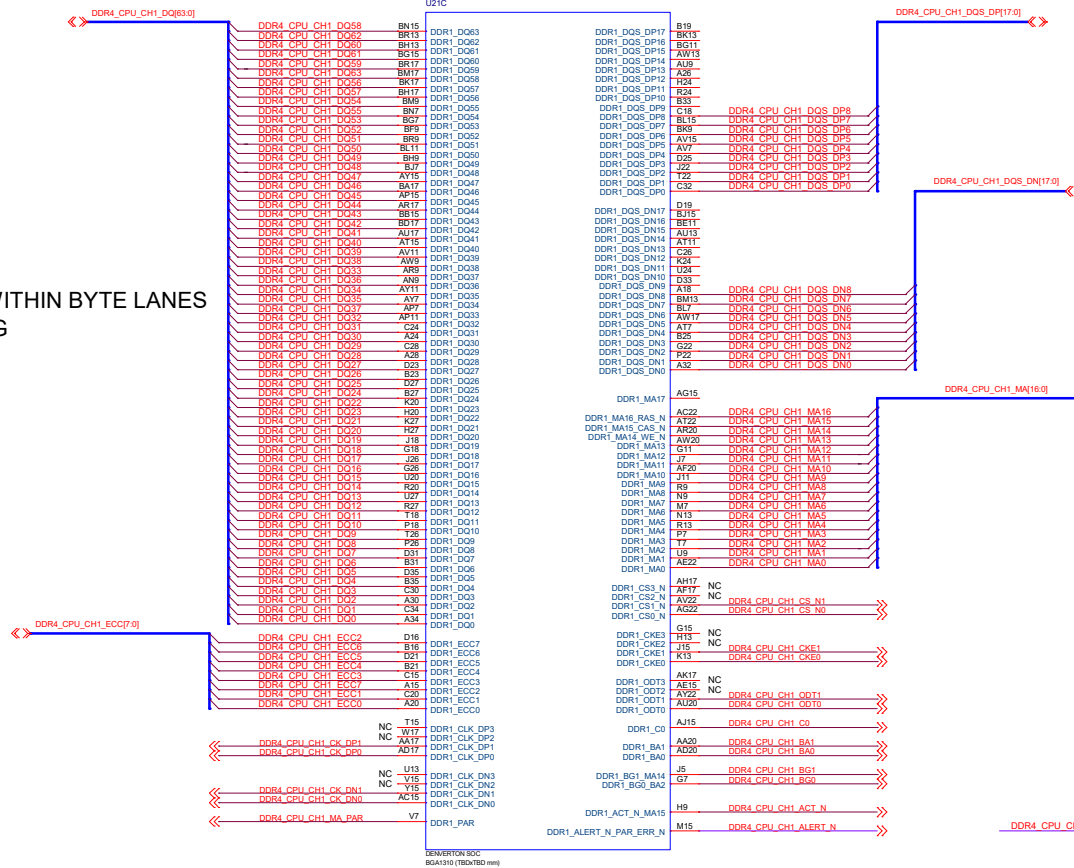


CLOCKING DIAGRAM

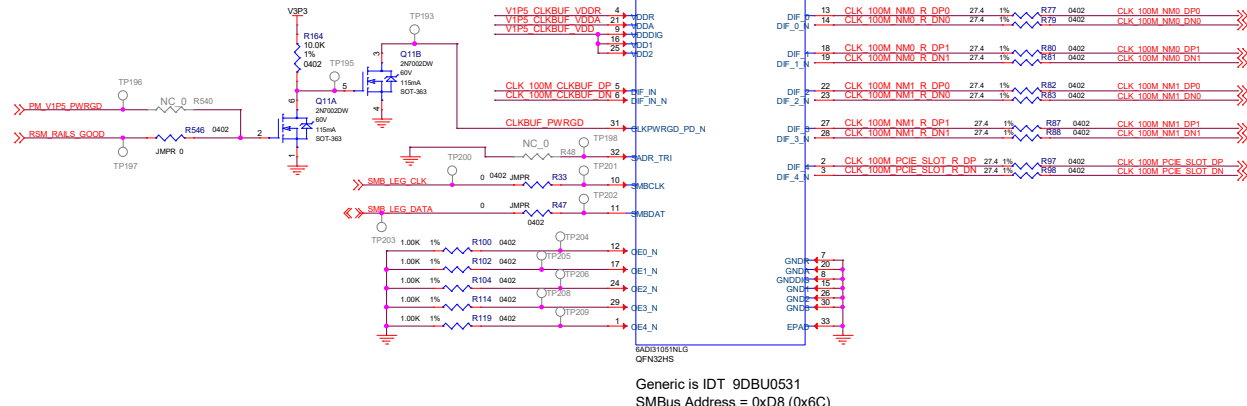
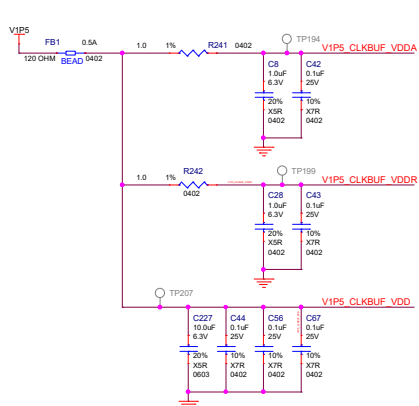
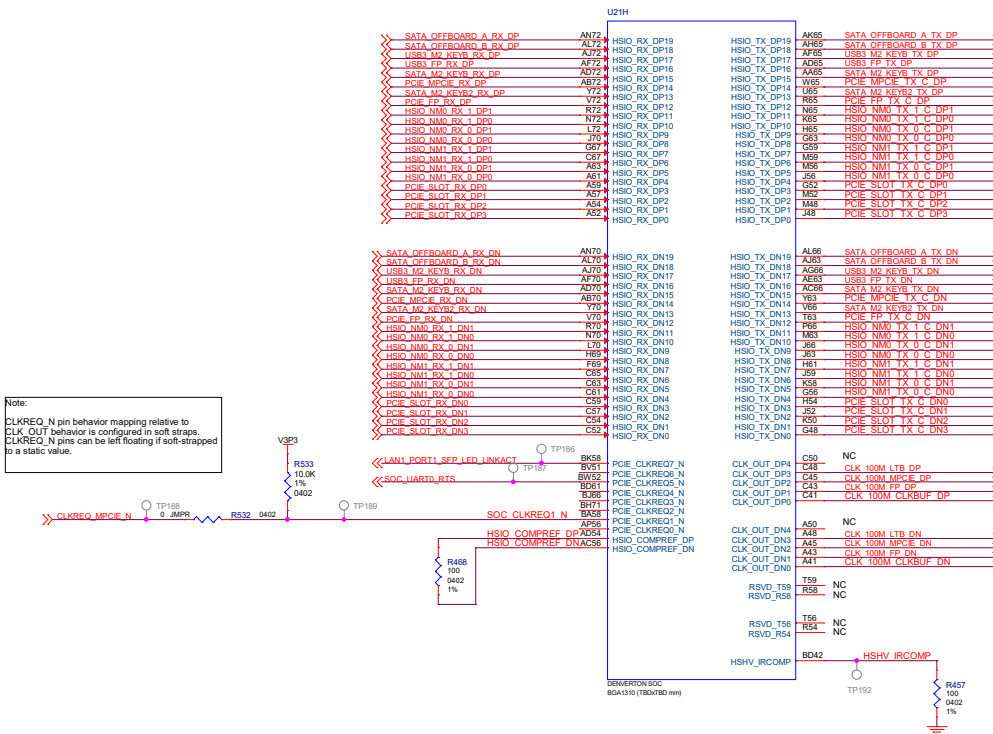
DRAWING No.: 8004-9159-002		CLOCKING DIAGRAM		APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
AssyG02				NAME	SIGN	DATE	
SIZE: Custom	REV No.: R202-00	AT&T Complete Board		CHECK			
DATE: Thursday, November 29, 2018				APPROV.			
				SHEET: 10	of 10	BT	

[illegible]

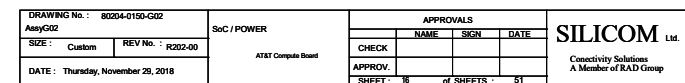
SIGNALS SWAPPED WITHIN BYTE LANES
TO IMPROVE ROUTING



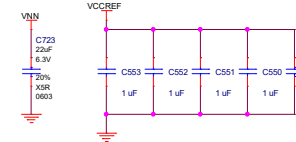
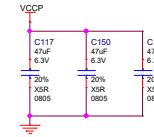
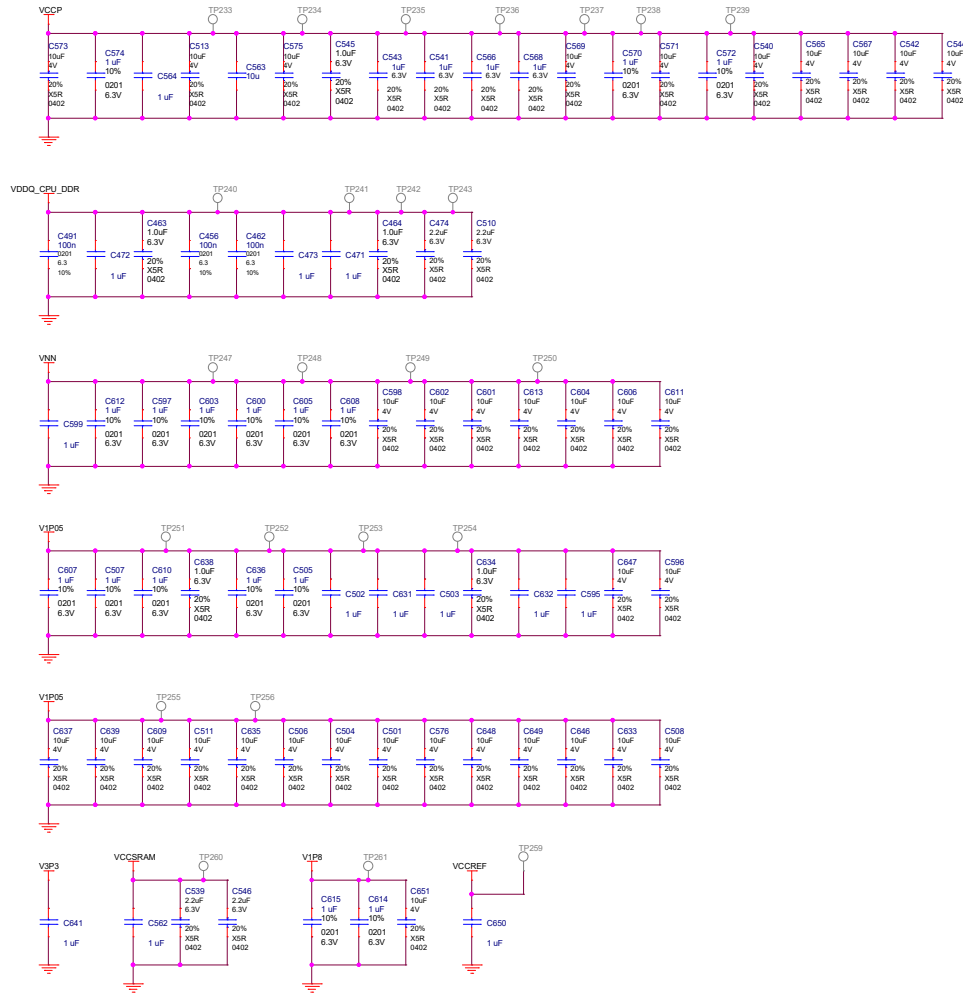
PCIE SLOT TX C D0	25V 0.1uF C733	0402 X7R 10%	25V 0.1uF C734	0402 X7R 10%	PCIE SLOT TX DP0
PCIE SLOT TX C DP1	25V 0.1uF C735	0402 X7R 10%	25V 0.1uF C736	0402 X7R 10%	PCIE SLOT TX DP1
PCIE SLOT TX C DP2	25V 0.1uF C698	0402 X7R 10%	25V 0.1uF C718	0402 X7R 10%	PCIE SLOT TX DP2
PCIE SLOT TX C DN3	25V 0.1uF C699	0402 X7R 10%	25V 0.1uF C717	0402 X7R 10%	PCIE SLOT TX DP3
PCIE SLOT TX C DP0	25V 0.1uF C729	0402 X7R 10%	25V 0.1uF C730	0402 X7R 10%	PCIE SLOT TX DN0
PCIE SLOT TX C DN1	25V 0.1uF C731	0402 X7R 10%	25V 0.1uF C732	0402 X7R 10%	PCIE SLOT TX DN1
PCIE SLOT TX C DN2	25V 0.1uF C697	0402 X7R 10%	25V 0.1uF C717	0402 X7R 10%	PCIE SLOT TX DN2
PCIE SLOT TX C DP3	25V 0.1uF C697	0402 X7R 10%	25V 0.1uF C717	0402 X7R 10%	PCIE SLOT TX DN3
PCIE MPCIe TX C DP	25V 0.1uF C696	0402 X7R 10%	25V 0.1uF C697	0402 X7R 10%	PCIE MPCIe TX DP
PCIE MPCIe TX C DN	25V 0.1uF C696	0402 X7R 10%	25V 0.1uF C697	0402 X7R 10%	PCIE MPCIe TX DN
PCIE FP TX C DP	25V 0.1uF C83	0402 X7R 10%	25V 0.1uF C81	0402 X7R 10%	PCIE FP TX DP
PCIE FP TX C DN	25V 0.1uF C83	0402 X7R 10%	25V 0.1uF C81	0402 X7R 10%	PCIE FP TX DN
HSIO NM0 TX 1 C DP1	25V 0.1uF C80	0402 X7R 10%	25V 0.1uF C69	0402 X7R 10%	HSIO NM0 TX 1 DP1
HSIO NM0 TX 1 C DP0	25V 0.1uF C80	0402 X7R 10%	25V 0.1uF C69	0402 X7R 10%	HSIO NM0 TX 1 DP0
HSIO NM0 TX 1 C DN1	25V 0.1uF C96	0402 X7R 10%	25V 0.1uF C84	0402 X7R 10%	HSIO NM0 TX 1 DN1
HSIO NM0 TX 1 C DNO	25V 0.1uF C102	0402 X7R 10%	25V 0.1uF C84	0402 X7R 10%	HSIO NM0 TX 1 DNO
HSIO NM0 TX 0 C DP1	25V 0.1uF C99	0402 X7R 10%	25V 0.1uF C97	0402 X7R 10%	HSIO NM0 TX 0 DP1
HSIO NM0 TX 0 C DP0	25V 0.1uF C99	0402 X7R 10%	25V 0.1uF C97	0402 X7R 10%	HSIO NM0 TX 0 DP0
HSIO NM0 TX 0 C DN1	25V 0.1uF C109	0402 X7R 10%	25V 0.1uF C101	0402 X7R 10%	HSIO NM0 TX 0 DN1
HSIO NM0 TX 0 C DNO	25V 0.1uF C102	0402 X7R 10%	25V 0.1uF C101	0402 X7R 10%	HSIO NM0 TX 0 DNO
HSIO NM1 TX 1 C DP1	25V 0.1uF C109	0402 X7R 10%	25V 0.1uF C104	0402 X7R 10%	HSIO NM1 TX 1 DP1
HSIO NM1 TX 1 C DP0	25V 0.1uF C109	0402 X7R 10%	25V 0.1uF C104	0402 X7R 10%	HSIO NM1 TX 1 DP0
HSIO NM1 TX 1 C DN1	25V 0.1uF C125	0402 X7R 10%	25V 0.1uF C122	0402 X7R 10%	HSIO NM1 TX 1 DN1
HSIO NM1 TX 1 C DNO	25V 0.1uF C125	0402 X7R 10%	25V 0.1uF C122	0402 X7R 10%	HSIO NM1 TX 1 DNO
HSIO NM1 TX 0 C DP1	25V 0.1uF C132	0402 X7R 10%	25V 0.1uF C126	0402 X7R 10%	HSIO NM1 TX 0 DP1
HSIO NM1 TX 0 C DP0	25V 0.1uF C132	0402 X7R 10%	25V 0.1uF C126	0402 X7R 10%	HSIO NM1 TX 0 DP0
HSIO NM1 TX 0 C DN1	25V 0.1uF C133	0402 X7R 10%	25V 0.1uF C133	0402 X7R 10%	HSIO NM1 TX 0 DN1
HSIO NM1 TX 0 C DNO	25V 0.1uF C133	0402 X7R 10%	25V 0.1uF C133	0402 X7R 10%	HSIO NM1 TX 0 DNO



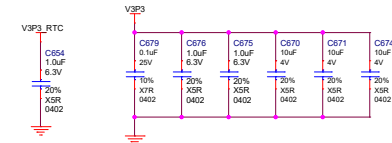
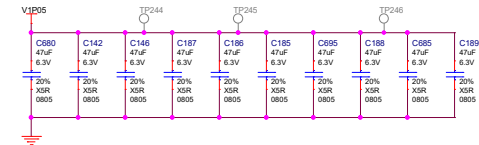
DRAWING No.: 80204-0150-G02		SoC / HSIO	APPROVALS				 Connectivity Solutions A Member of RAD Group		
AssyG02			AT&T Compute Board	CHECK	NAME	SIGN		DATE	
Custom	REV No.: R202-00				APPROV.	BY		DATE	BY
DATE: Thursday, November 29, 2018									



PLACE THESE CAPS AS BACKSIDE CAPS OF SoC



CAD NOTE: PLACE AT OUTPUT OF V1P05 VR



U21K		
A22	VSS_0	AM37
A37	VSS_1	AM43
AZ	VSS_2	VSS_85
AE5	VSS_3	VSS_86
AE6	VSS_4	VSS_87
AE7	VSS_5	AN1
AE8	VSS_6	AN13
AA13	VSS_7	VSS_90
AA14	VSS_8	VSS_91
AA39	VSS_9	VSS_92
AA48	VSS_10	VSS_93
AA24	VSS_11	VSS_94
AA58	VSS_12	VSS_95
AA61	VSS_13	VSS_96
AA69	VSS_14	VSS_97
AA71	VSS_15	VSS_98
AB5	VSS_16	VSS_99
AB6	VSS_17	VSS_100
AC29	VSS_18	VSS_101
AC37	VSS_19	VSS_102
AC32	VSS_20	VSS_103
AC63	VSS_21	VSS_104
AC69	VSS_22	VSS_105
AC71	VSS_23	VSS_106
AD13	VSS_24	VSS_107
AD5	VSS_25	VSS_108
AD60	VSS_26	VSS_109
AD61	VSS_27	VSS_110
AD88	VSS_28	VSS_111
AE2	VSS_29	VSS_112
AE29	VSS_30	VSS_113
AE4	VSS_31	VSS_114
AE48	VSS_32	VSS_115
AE52	VSS_33	VSS_116
AE53	VSS_34	VSS_117
AE6	VSS_35	VSS_118
AE69	VSS_36	VSS_119
AE71	VSS_37	VSS_120
AF11	VSS_38	VSS_121
AF24	VSS_39	VSS_122
AF5	VSS_40	VSS_123
AF54	VSS_41	VSS_124
AF58	VSS_42	VSS_125
AF61	VSS_43	VSS_126
AF58	VSS_44	VSS_127
AC29	VSS_45	VSS_128
AG37	VSS_46	VSS_129
AG41	VSS_47	VSS_130
AG48	VSS_48	VSS_131
AG63	VSS_49	VSS_132
AG69	VSS_50	VSS_133
AH13	VSS_51	VSS_134
AH61	VSS_52	VSS_135
AH69	VSS_53	VSS_136
AH71	VSS_54	VSS_137
AJ29	VSS_55	VSS_138
AJ37	VSS_56	VSS_139
AJ41	VSS_57	VSS_140
AJ48	VSS_58	VSS_141
AJ5	VSS_59	VSS_142
AJ52	VSS_60	VSS_143
AJ59	VSS_61	VSS_144
AJ68	VSS_62	VSS_145
AK13	VSS_63	VSS_146
AK29	VSS_64	VSS_147
AK37	VSS_65	VSS_148
AK41	VSS_66	VSS_149
AK48	VSS_67	VSS_150
AK54	VSS_68	VSS_151
AK58	VSS_69	VSS_152
AK61	VSS_70	VSS_153
AK69	VSS_71	VSS_154
AK71	VSS_72	VSS_155
AK8	VSS_73	VSS_156
AL11	VSS_74	VSS_157
AL15	VSS_75	VSS_158
AL5	VSS_76	VSS_159
AL52	VSS_77	VSS_160
AL59	VSS_78	VSS_161
AL68	VSS_79	VSS_162
AL7	VSS_80	VSS_163
AL72	VSS_81	VSS_164
AM29	VSS_82	VSS_165

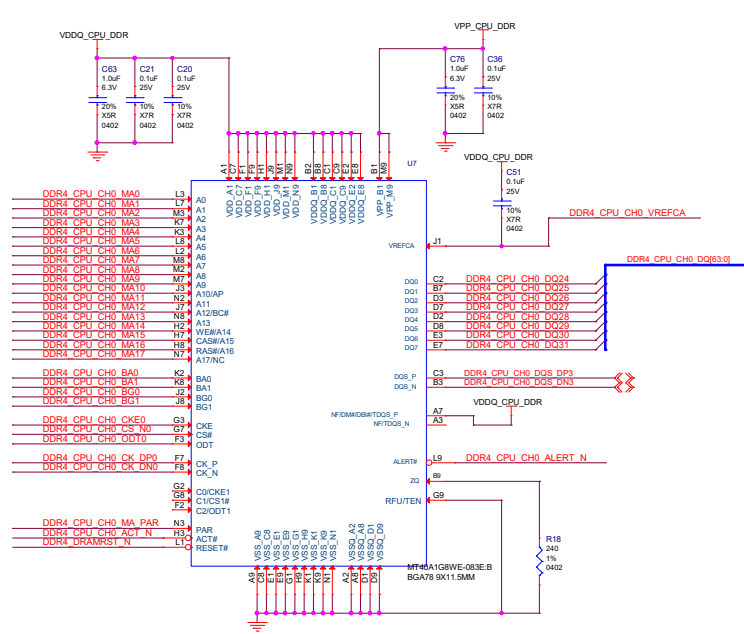
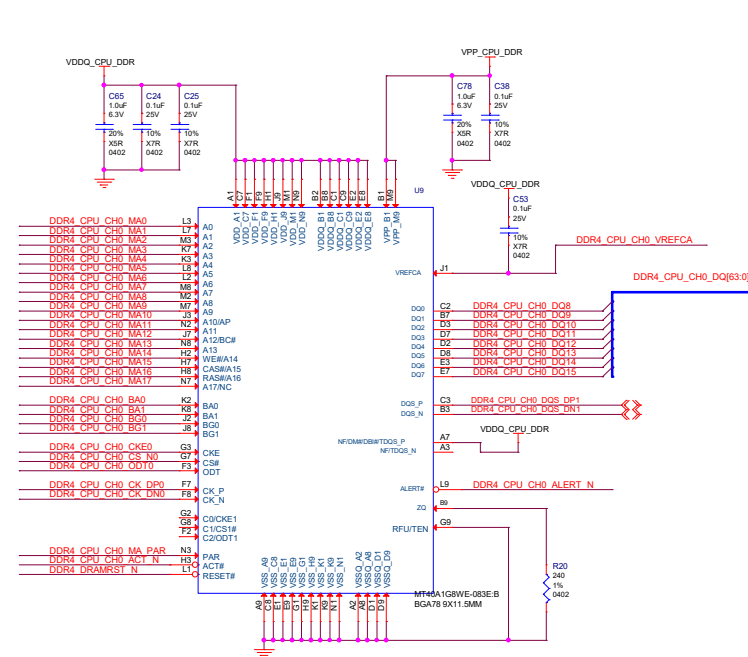
DEMERTON SOC
BGA1310 (7BDx7BD mm)

U21M		
BB29	VSS_195	BR38
BB37	VSS_196	BR6
BB41	VSS_197	BR70
BB44	VSS_198	VSS_251
BB48	VSS_199	VSS_252
BB5	VSS_170	VSS_253
BB52	VSS_171	VSS_254
BB53	VSS_172	VSS_255
BB59	VSS_173	VSS_256
BB61	VSS_174	VSS_257
BB68	VSS_175	VSS_258
BB7	VSS_176	VSS_259
BC71	VSS_177	VSS_260
BD13	VSS_178	VSS_261
BD37	VSS_179	VSS_262
BD27	VSS_180	VSS_263
BD27	VSS_181	VSS_264
BD31	VSS_182	VSS_265
BD5	VSS_183	VSS_266
BD6	VSS_184	VSS_267
BD7	VSS_185	VSS_268
BE13	VSS_186	VSS_269
BE19	VSS_187	VSS_270
BE37	VSS_188	VSS_271
BE7	VSS_189	VSS_272
BE77	VSS_190	VSS_273
BF13	VSS_191	VSS_274
BF17	VSS_192	VSS_275
BF37	VSS_193	VSS_276
BF42	VSS_194	VSS_277
BF48	VSS_195	VSS_278
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BF59	VSS_197	VSS_280
BF54	VSS_198	VSS_281
BF58	VSS_199	VSS_282
BF6	VSS_200	VSS_283
BF68	VSS_201	VSS_284
BF69	VSS_202	VSS_285
BG13	VSS_203	VSS_286
BG37	VSS_204	VSS_287
BG41	VSS_205	VSS_288
BG71	VSS_206	VSS_289
BT19	VSS_207	VSS_290
BT27	VSS_208	VSS_291
BT29	VSS_209	VSS_292
BT29	VSS_210	VSS_293
BT37	VSS_211	VSS_294
BT42	VSS_212	VSS_295
BT48	VSS_213	VSS_296
BT48	VSS_214	VSS_297
BT5	VSS_215	VSS_298
BT52	VSS_216	VSS_299
BT59	VSS_217	VSS_300
BT6	VSS_218	VSS_301
BT68	VSS_219	VSS_302
BT69	VSS_220	VSS_303
BT70	VSS_221	VSS_304
BT72	VSS_222	VSS_305
BT72	VSS_223	VSS_306
BT77	VSS_224	VSS_307
BT8	VSS_225	VSS_308
BT87	VSS_226	VSS_309
BT87	VSS_227	VSS_310
BT87	VSS_228	VSS_311
BT87	VSS_229	VSS_312
BT87	VSS_230	VSS_313
BT87	VSS_231	VSS_314
BT87	VSS_232	VSS_315
BT87	VSS_233	VSS_316
BT87	VSS_234	VSS_317
BT87	VSS_235	VSS_318
BT87	VSS_236	VSS_319
BT87	VSS_237	VSS_320
BT87	VSS_238	VSS_321
BT87	VSS_239	VSS_322
BT87	VSS_240	VSS_323
BT87	VSS_241	VSS_324
BT87	VSS_242	VSS_325
BT87	VSS_243	VSS_326
BT87	VSS_244	VSS_327
BT87	VSS_245	VSS_328
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BT87	VSS_247	VSS_330
BT87	VSS_248	VSS_331
BT87	VSS_249	VSS_332

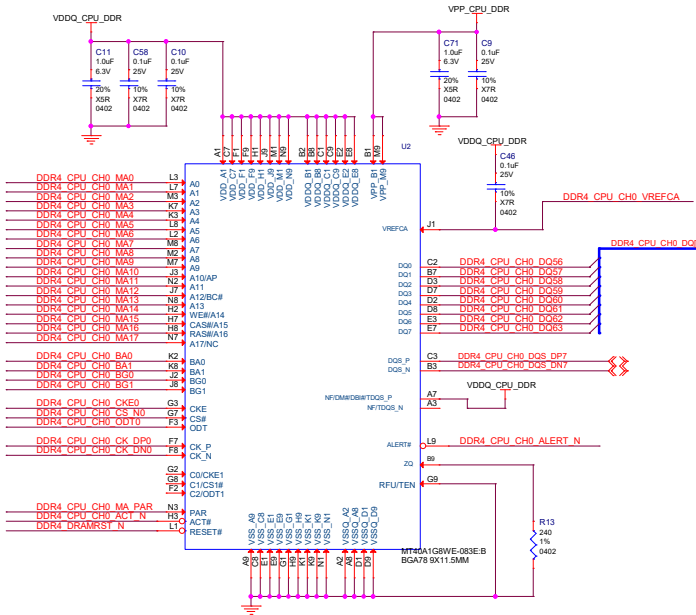
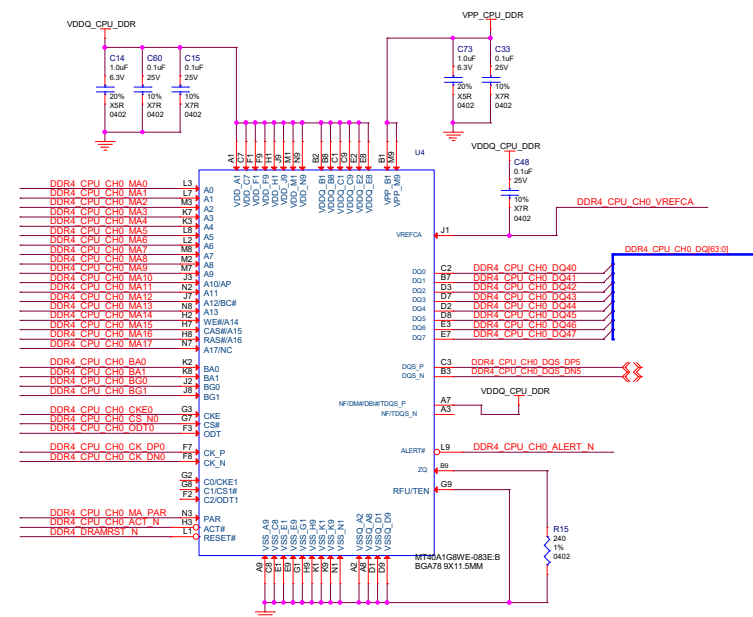
DEMERTON SOC
BGA1310 (7BDx7BD mm)

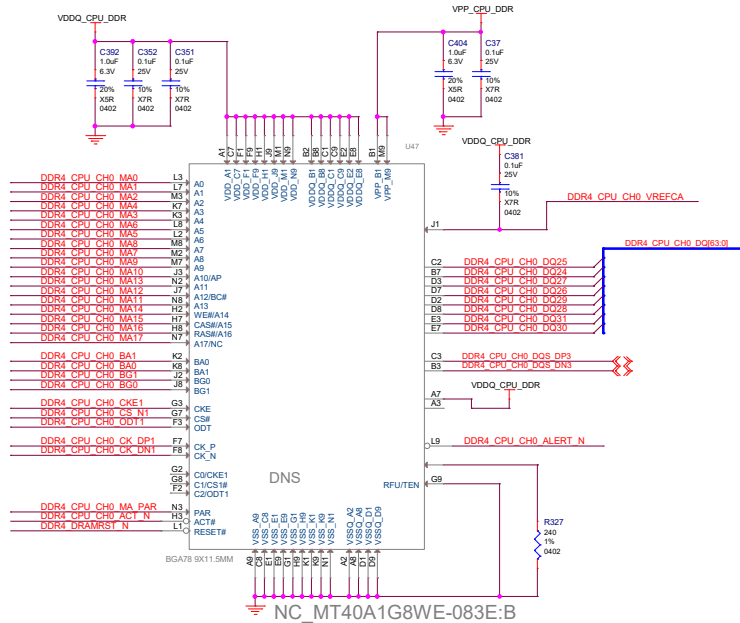
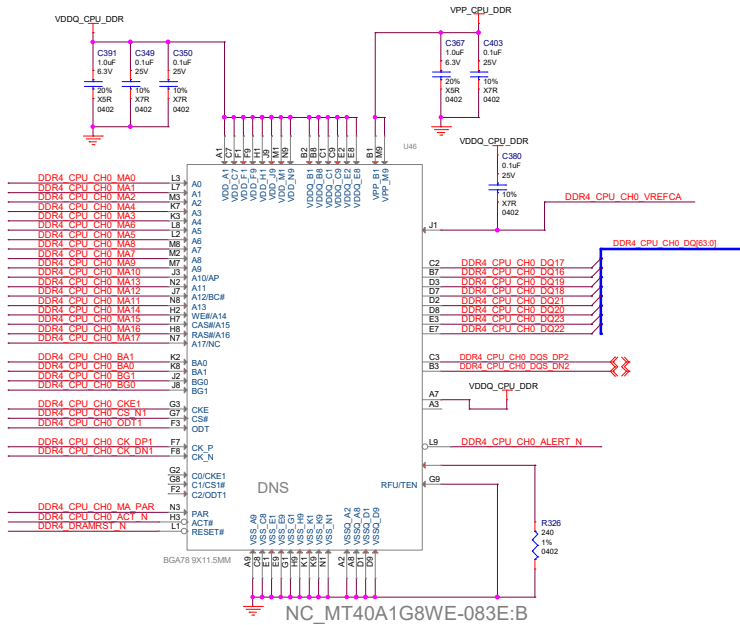
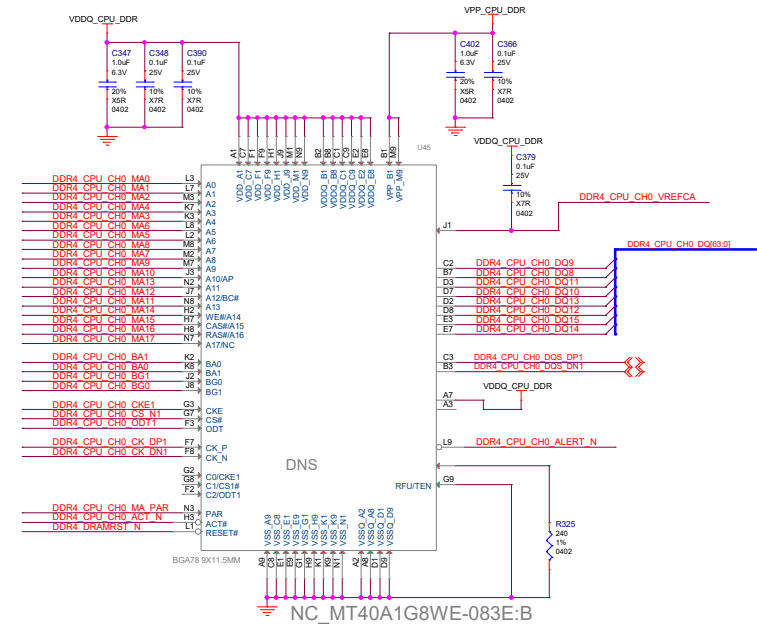
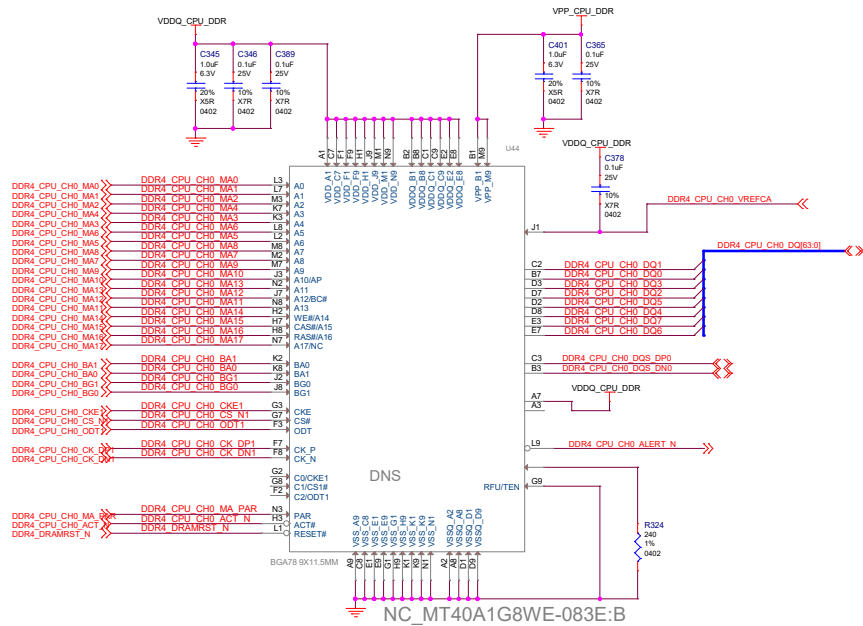
U21L		
E13	VSS_333	NC_ROT
E19	VSS_334	VSS_ROT
E29	VSS_335	
E32	VSS_336	
E37	VSS_337	VSS_416
E39	VSS_338	VSS_417
E39	VSS_339	VSS_418
E39	VSS_340	VSS_419
E39	VSS_341	VSS_420
E39	VSS_342	VSS_421
E39	VSS_343	VSS_422
E39	VSS_344	VSS_423
E39	VSS_345	VSS_424
E39	VSS_346	VSS_425
E39	VSS_347	VSS_426
E39	VSS_348	VSS_427
E39	VSS_349	VSS_428
E39	VSS_350	VSS_429
E39	VSS_351	VSS_430
E39	VSS_352	VSS_431
E39	VSS_353	VSS_432
E39	VSS_354	VSS_433
E39	VSS_355	VSS_434
E39	VSS_356	VSS_435
E39	VSS_357	VSS_436
E39	VSS_358	VSS_437
E39	VSS_359	VSS_438
E39	VSS_360	VSS_439
E39	VSS_361	VSS_440
E39	VSS_362	VSS_441
E39	VSS_363	VSS_442
E39	VSS_364	VSS_443
E39	VSS_365	VSS_444
E39	VSS_366	VSS_445
E39	VSS_367	VSS_446
E39	VSS_368	VSS_447
E39	VSS_369	VSS_448
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E39	VSS_373	VSS_452
E39	VSS_374	VSS_453
E39	VSS_375	VSS_454
E39	VSS_376	VSS_455
E39	VSS_377	VSS_456
E39	VSS_378	VSS_457
E39	VSS_379	VSS_458
E39	VSS_380	VSS_459
E39	VSS_381	VSS_460
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E39	VSS_393	VSS_472
E39	VSS_394	VSS_473
E39	VSS_395	VSS_474
E39	VSS_396	VSS_475
E39	VSS_397	VSS_476
E39	VSS_398	VSS_477
E39	VSS_399	VSS_478
E39	VSS_400	VSS_479
E39	VSS_401	VSS_480
E39	VSS_402	VSS_481
E39	VSS_403	VSS_482
E39	VSS_404	VSS_483
E39	VSS_405	VSS_484
E39	VSS_406	VSS_485
E39	VSS_407	VSS_486
E39	VSS_408	VSS_487
E39	VSS_409	VSS_488
E39	VSS_410	VSS_489
E39	VSS_411	VSS_490
E39	VSS_412	VSS_491
E39	VSS_413	VSS_492
E39	VSS_414	
E39	VSS_415	

DEMERTON SOC
BGA1310 (7BDx7BD mm)



Conectivity Solutions
A Member of RAD Group





DRAWING No.: 80204-0150-G02

AsayG02

SIZE: Custom REV No.: R202-00

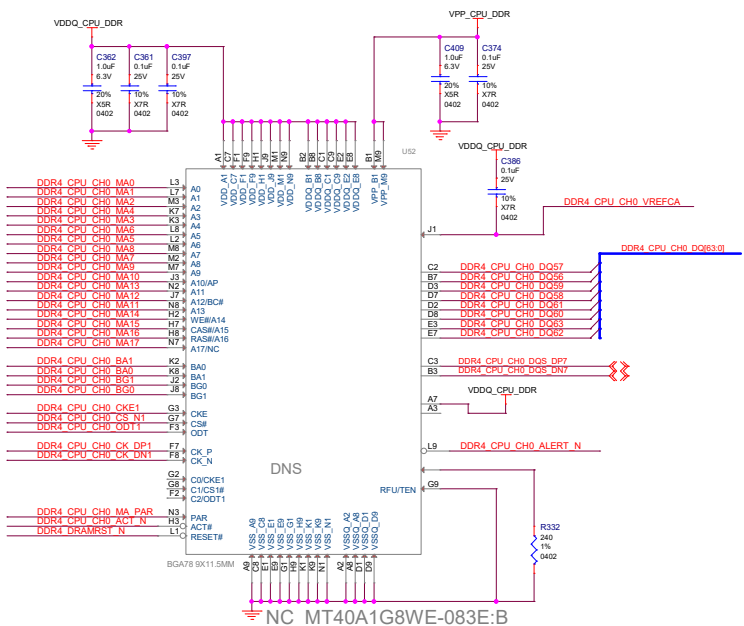
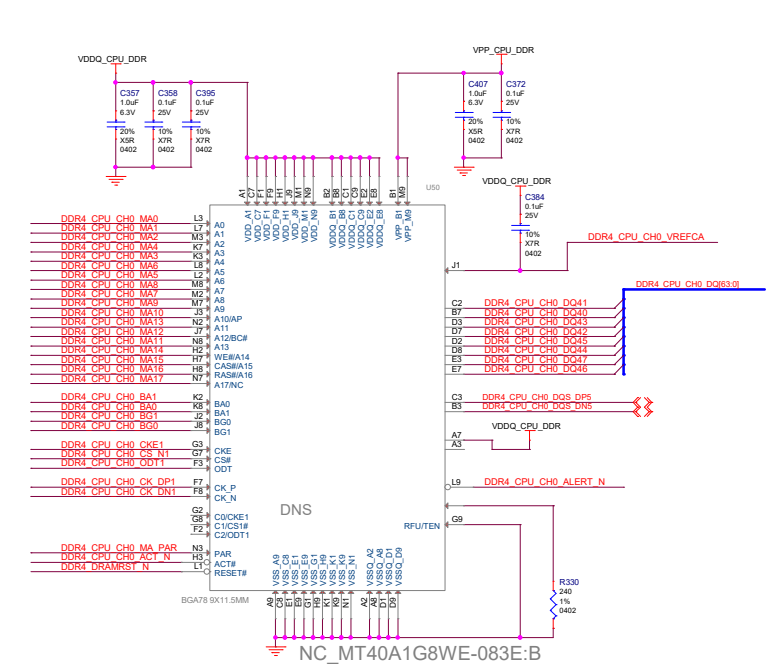
DATE: Thursday, November 29, 2018

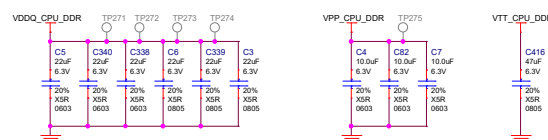
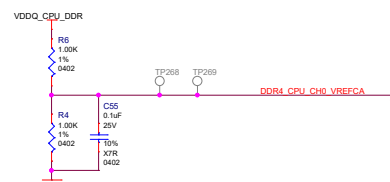
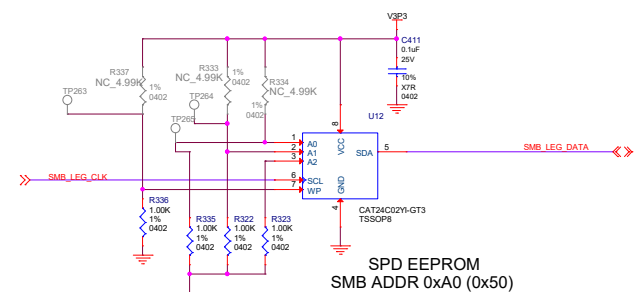
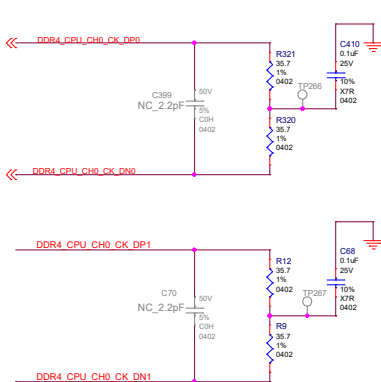
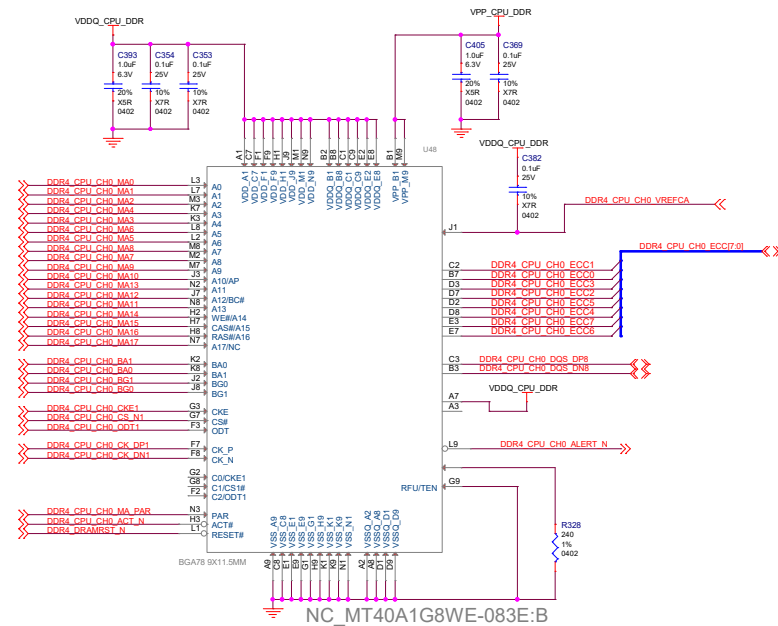
DDR4 MEMDOWN CH0-DQ0-31R1

AT&T Compaq Board

APPROVALS		
CHECK	NAME	DATE
APPROV.		
SHEET: 21	of SHEETS: 51	

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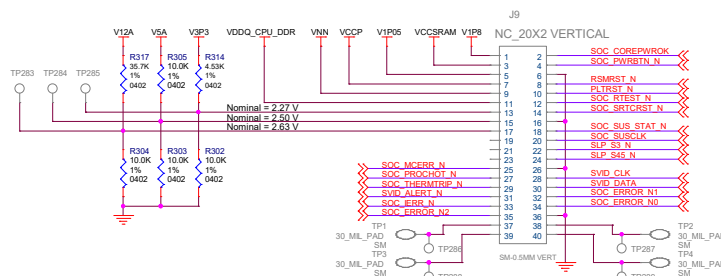
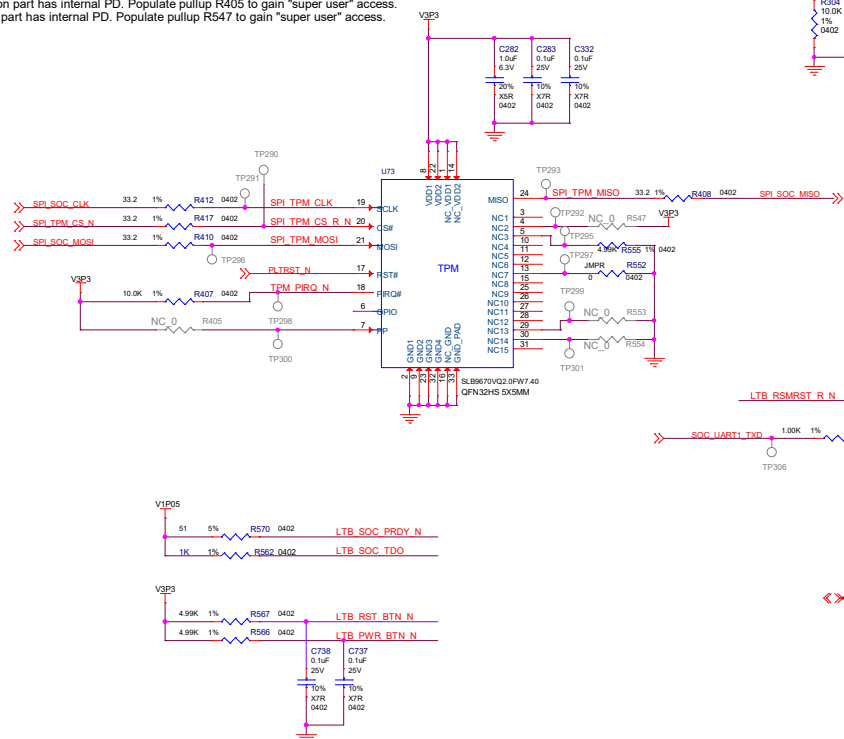


TPM Pin	Part	Populate Part	
		Infineon	Atmel
7	R405	note 1	
4	R547		note 2
29	R553		X
30	R554		X

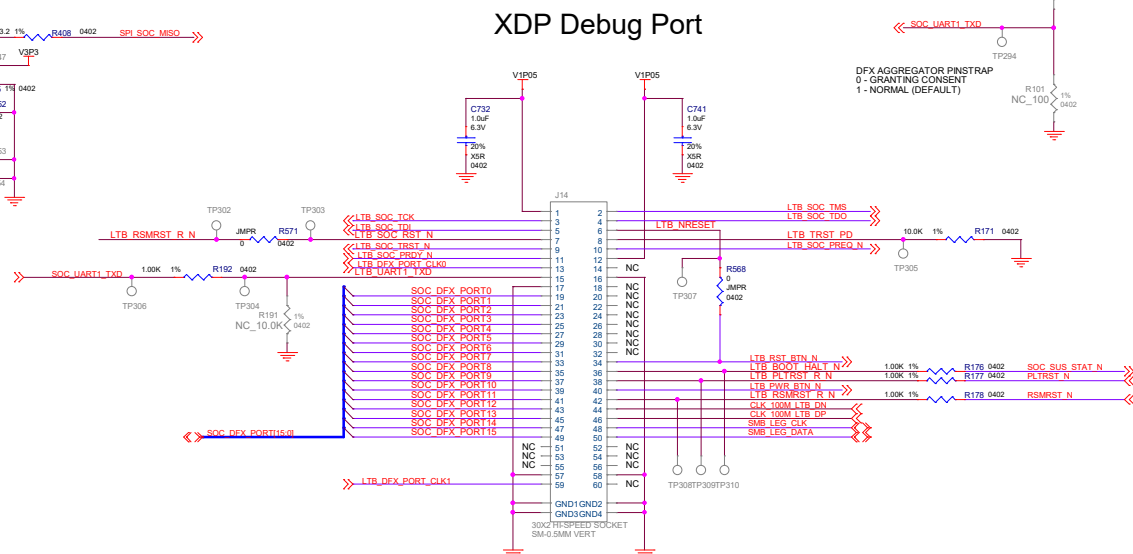
Trusted Platform Module (TPM)

Notes:

1. Pin on Infineon part has internal PD. Populate pullup R405 to gain "super user" access.
2. Pin on Atmel part has internal PD. Populate pullup R547 to gain "super user" access.



XDP Debug Port



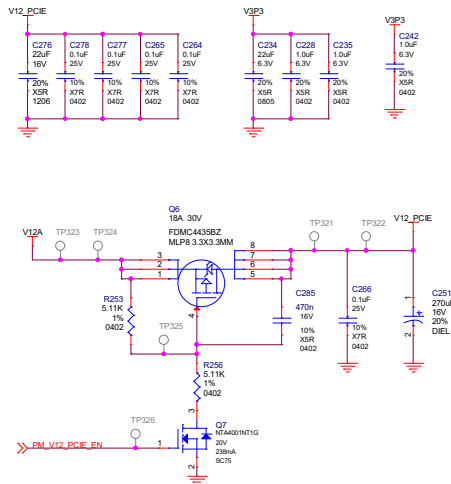
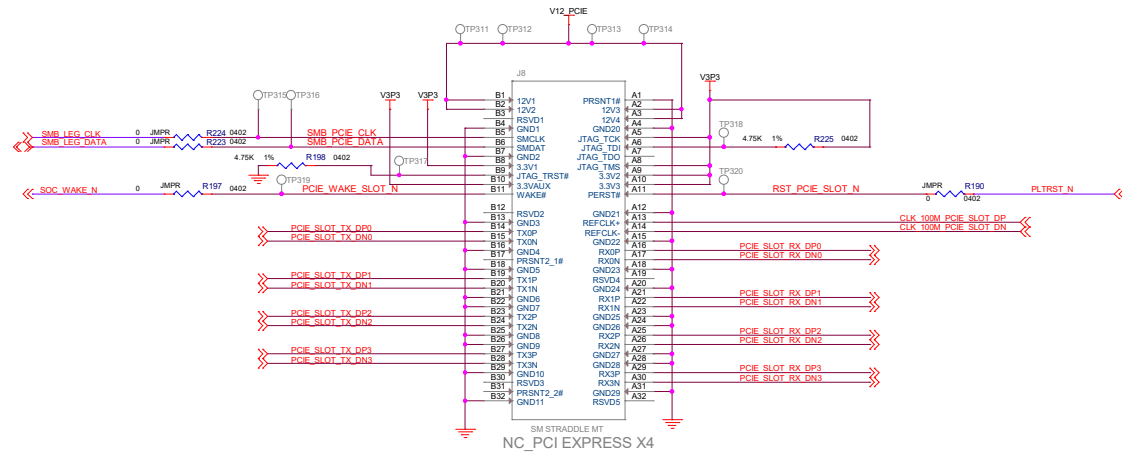
LAYOUT NOTE

All signals and voltages on pins 1-35 can be moved around to different pins in that range as needed to improve layout routing.

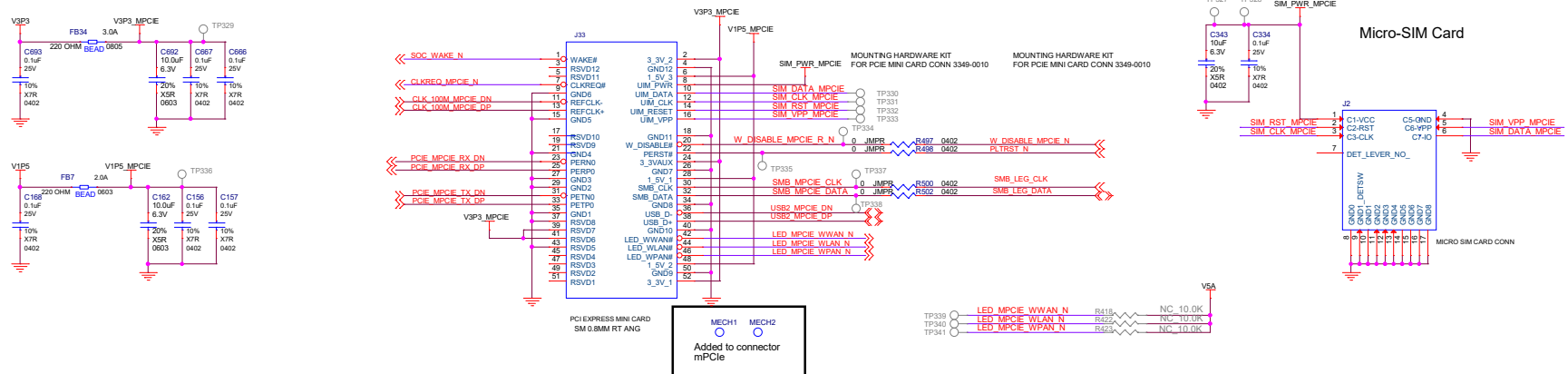
It is preferred that voltage rails on pins 1-35 be connected directly with dedicated traces. However if there are a few that impact routing, those can be brought out to test pads and mod wired from the voltage regulators on prototype boards.

Analog voltage in max is 3.0V.

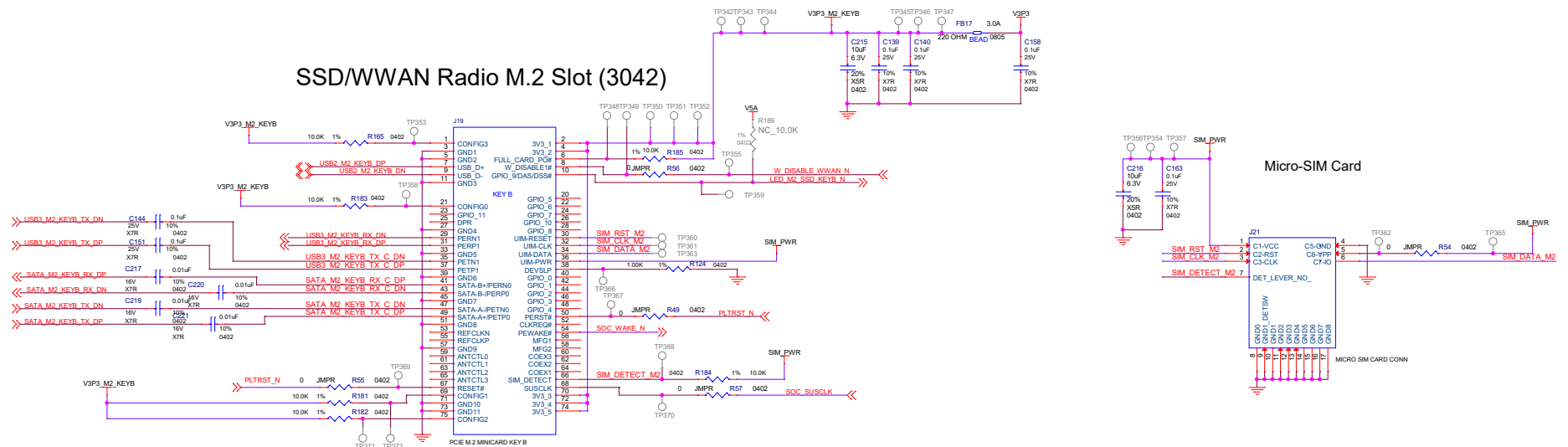
PCIe x4 Expansion Slot



mPCIe Wi-Fi/BT Radio Slot

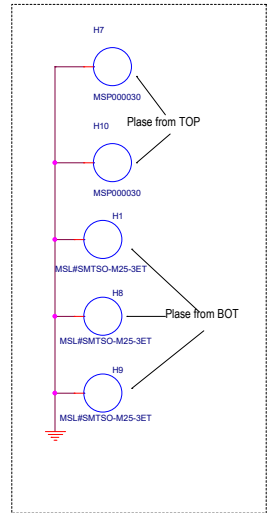
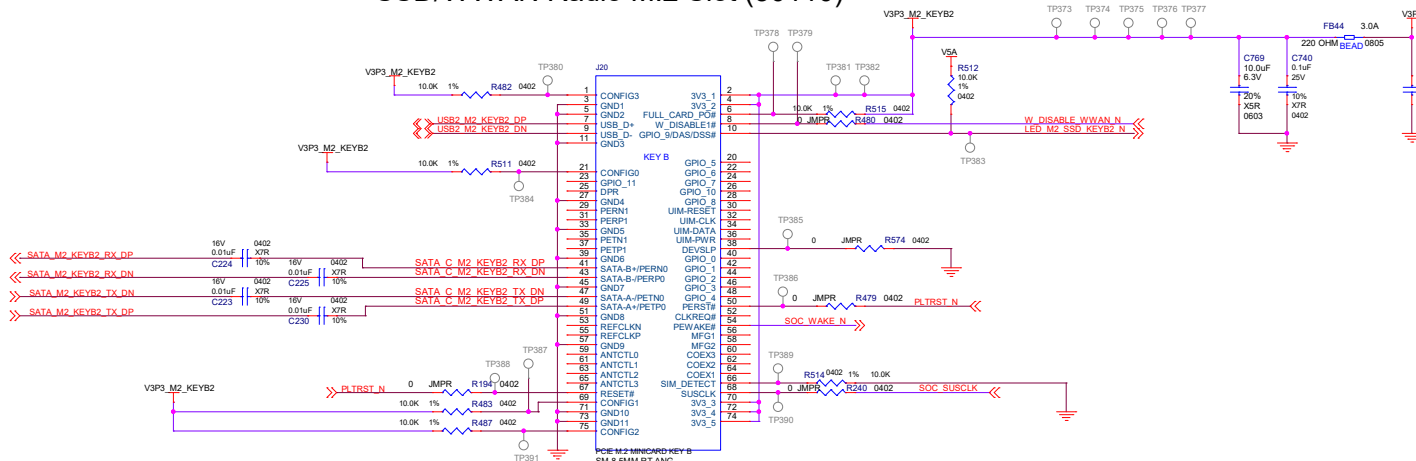


SSD/WWAN Radio M.2 Slot (3042)

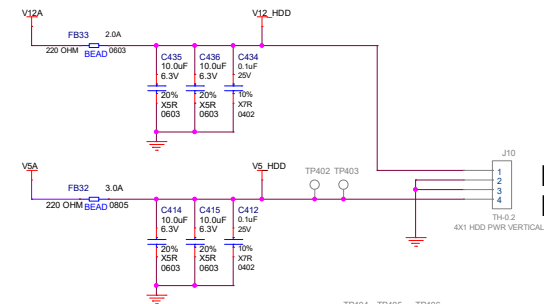
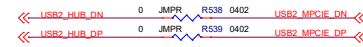
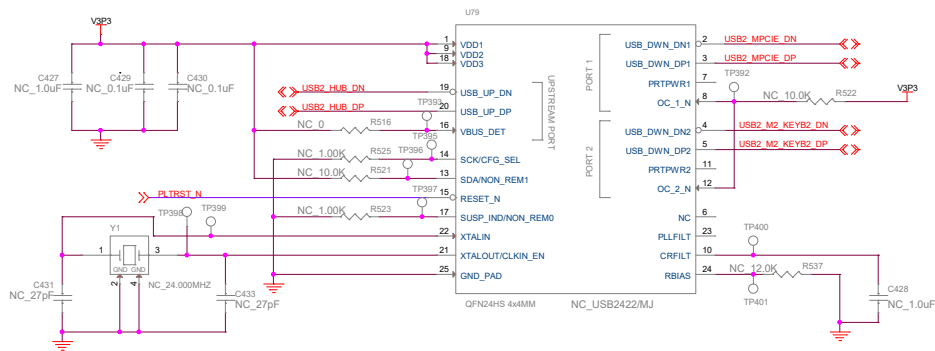


DRAWING No.: 80204-0150-G02		RADIO CARD SLOTS (WWAN/WI)	APPROVALS				 SILICOM Ltd. Connectivity Solutions A Member of RAD Group		
AsyG02									
SIZE: Custom	REV No.: R202-00		AT&T Compute Board		CHECK	NAME		SIGN	DATE
DATE: Thursday, November 28, 2018					APPROV:				
					OFFICE	W		U. S. J. 01/08/2019	ES

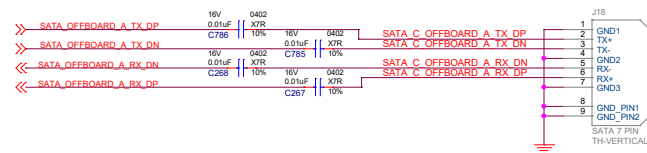
SSD/WWAN Radio M.2 Slot (30110)



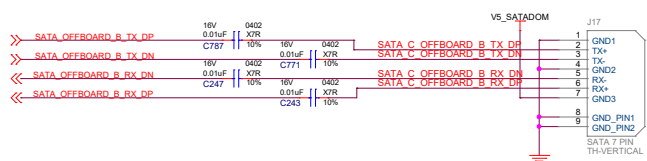
USB 2.0 Hub



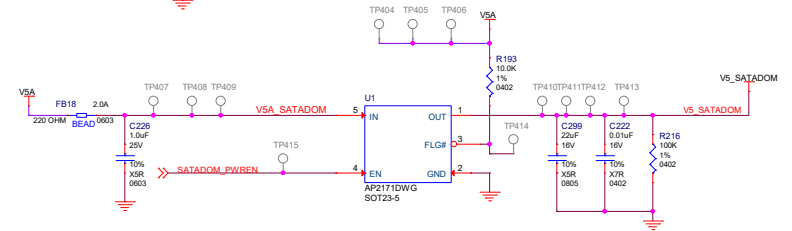
Power for offboard HDD/SSD



SATA - A

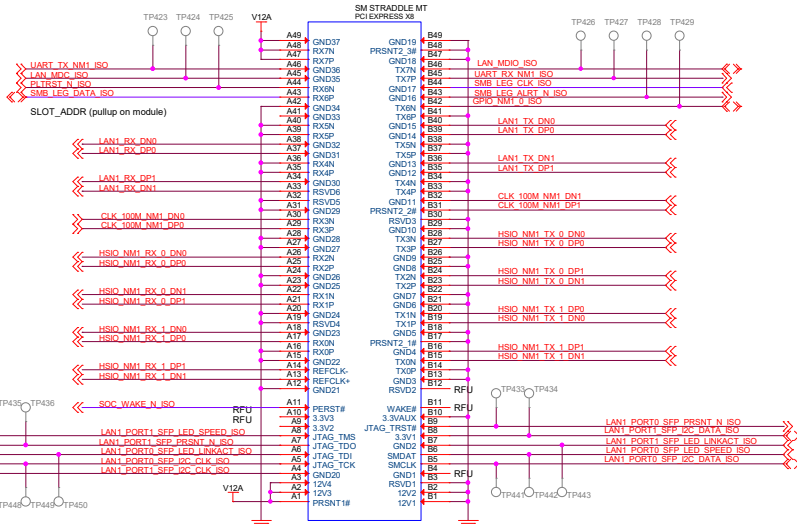
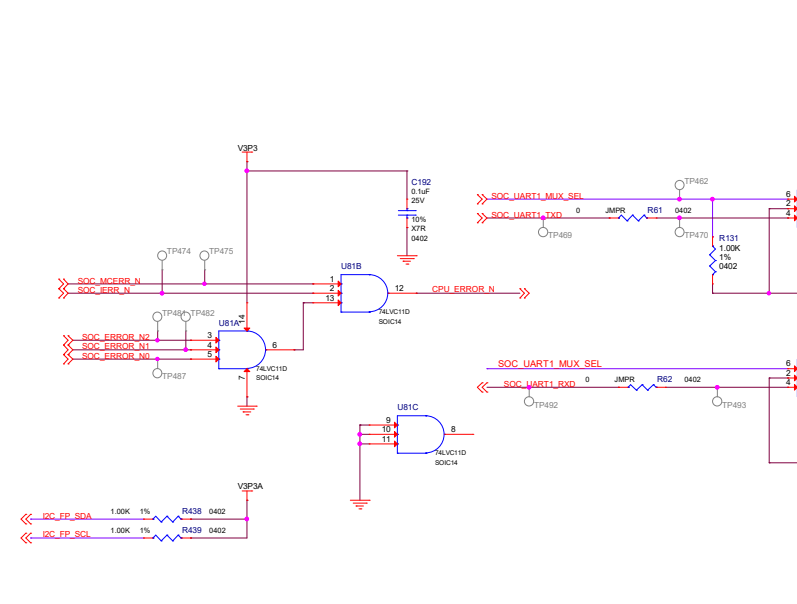


SATA/SATADOM - B
(supports powered modules)



DRAWING No.: 80204-0150-G02 AsyG02		SATA, SATADOM, M2 SSD, USB2		<table><tr><th colspan="3">APPROVALS</th></tr><tr><th>NAME</th><th>SIGN</th><th>DATE</th></tr><tr><td>CHECK</td><td></td><td></td></tr><tr><td>APPROV.</td><td></td><td></td></tr><tr><td>SUREV.</td><td>28</td><td>11/10/2019</td></tr></table>			APPROVALS			NAME	SIGN	DATE	CHECK			APPROV.			SUREV.	28	11/10/2019	 SILICOM Ltd. Connectivity Solutions A Member of RAD Group
APPROVALS																						
NAME	SIGN	DATE																				
CHECK																						
APPROV.																						
SUREV.	28	11/10/2019																				
SIZE: Custom	REV No.: R202-00	A18T Compact Board																				
DATE: Thursday, November 29, 2018																						

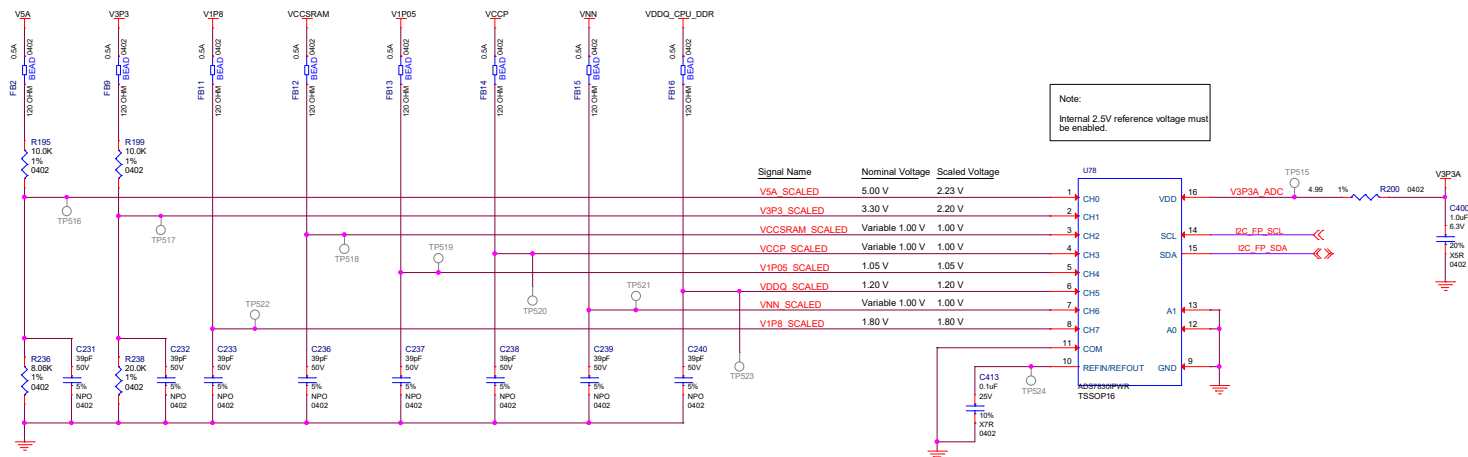
Network Module 1

[illegible]

V12A on pin A48/A49 is for monitoring power and for keeping a bank of holdup caps charged on BMC management versions of the front panel module. It allows the front panel module BMC to monitor state of V12A and take last-second actions if it detects V12A falling. The bank of capacitors and a local buck regulator keep the BMC alive long enough to do what it needs before power is completely lost - usually sending a notification packet out on the LAN.

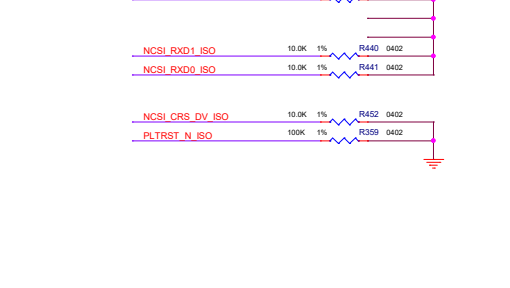
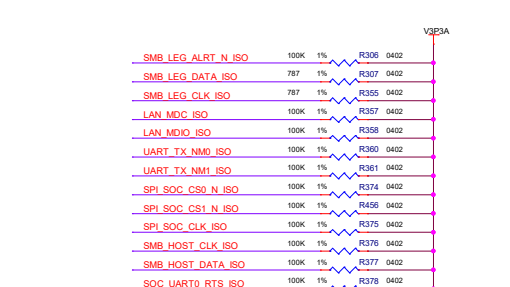
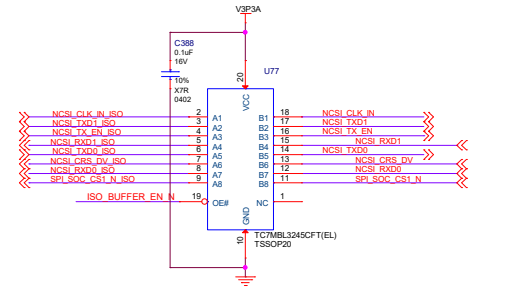
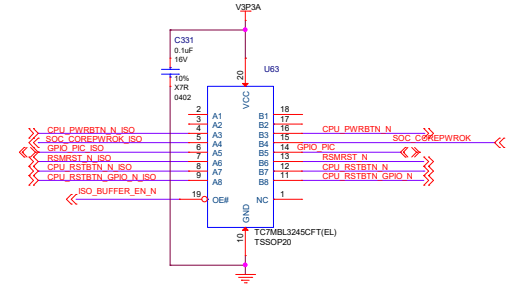
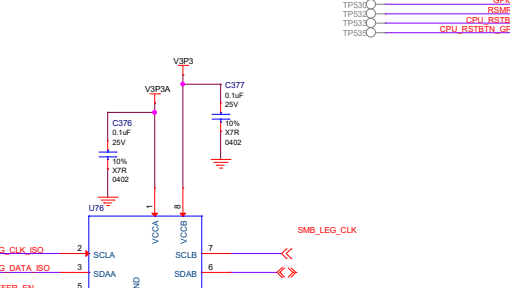
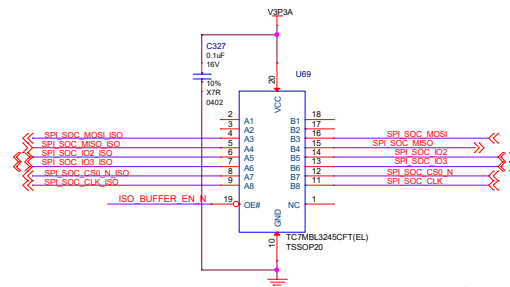
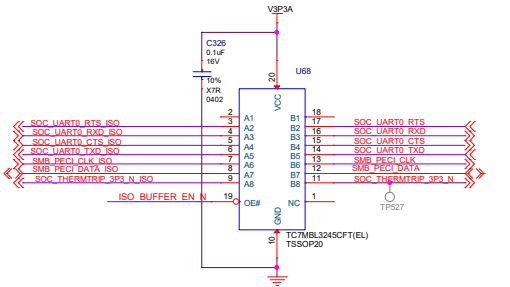
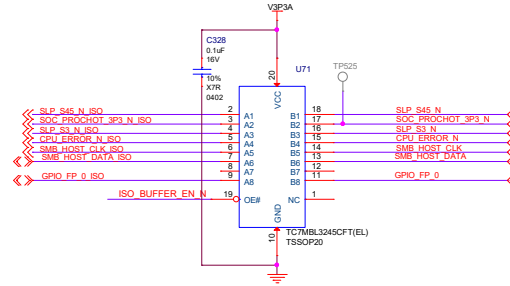
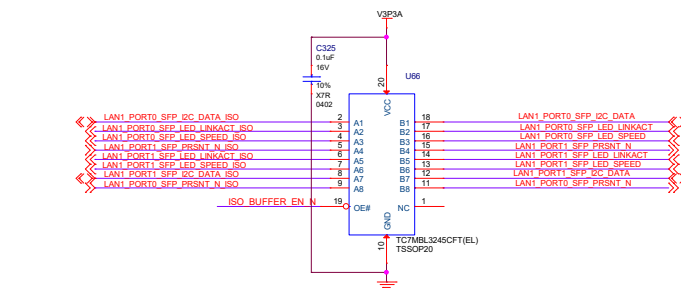
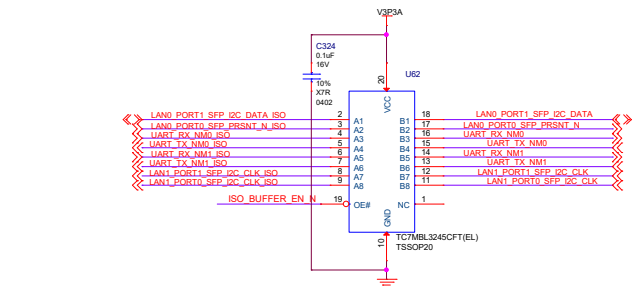
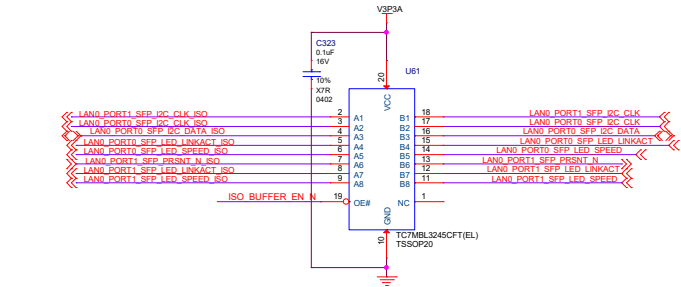
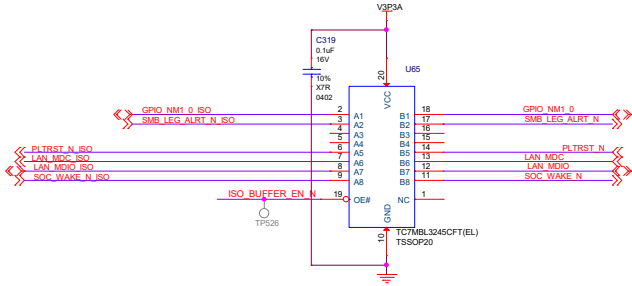
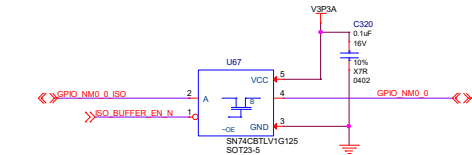
DRAWING No. : 80204-0150-G02		FRONT PANEL INTERACES		APPROVALS				 SILICOM Ltd. Connectivity Solutions A Member of RAD Group
AsyG02								
SIZE : Custom	REV No. : R202-00	AT&T Complete Board		CHECK	NAME	SIGN	DATE	
DATE : Thursday, November 29, 2018				APPROV.				
				SHEET : 26	of SHEETS : 51			

ADC Voltage Monitor (0 to +2.5 V Range)



I2C address
0x90 (0x48)

3.3V Isolation Buffers

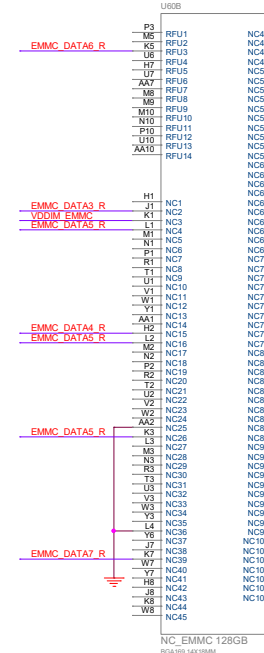
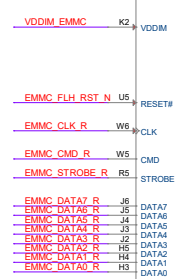
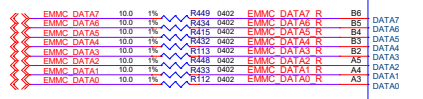
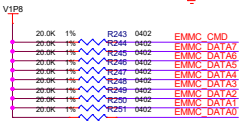


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AsyG02		AT&T Compute Board						
SIZE : Custom	REV No. : R202-00			CHECK	NAME	SIGN	DATE	
DATE : Thursday, November 29, 2018				APPROV.				
				SHEET : 33	of SHEETS : 51			

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4 - 64 GB eMMC

128 GB eMMC
(dual footprint)

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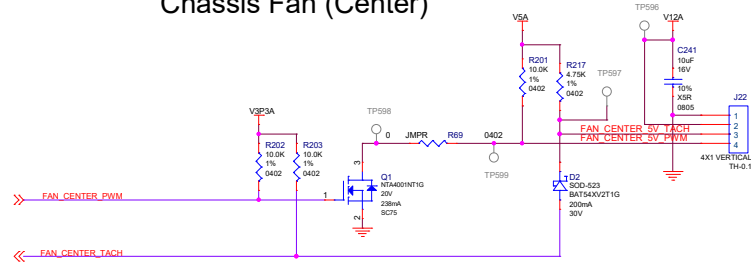
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AsyG02								
SIZE :	Custom	REV No. :	R202-00	CHECK	NAME	SIGN	DATE	
DATE : Thursday, November 29, 2018			AT&T Compute Board		APPROV.			
					SHEET : 31	of SHEETS : 51		

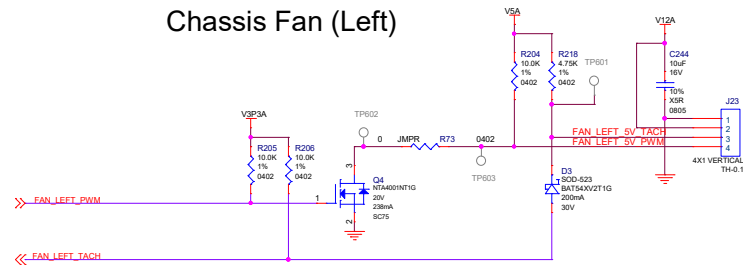
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CPU Negates SLP_S3_N > Enable VCCREF, V12_PCIE, V5_SATADOM	
VCCREF > Enable VCCP, VCCSRAM > 164mS Delay until SOC_COREPWROK	

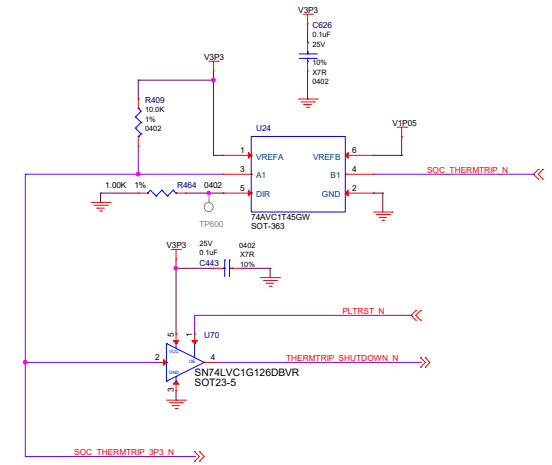
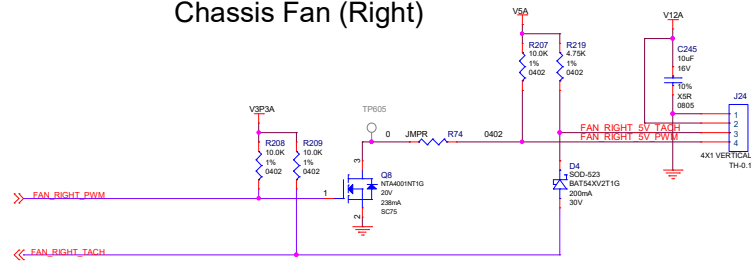
Chassis Fan (Center)



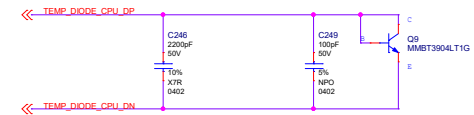
Chassis Fan (Left)



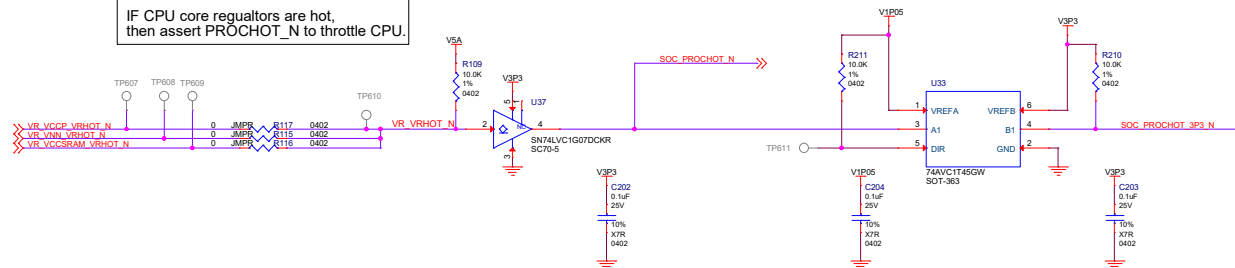
Chassis Fan (Right)



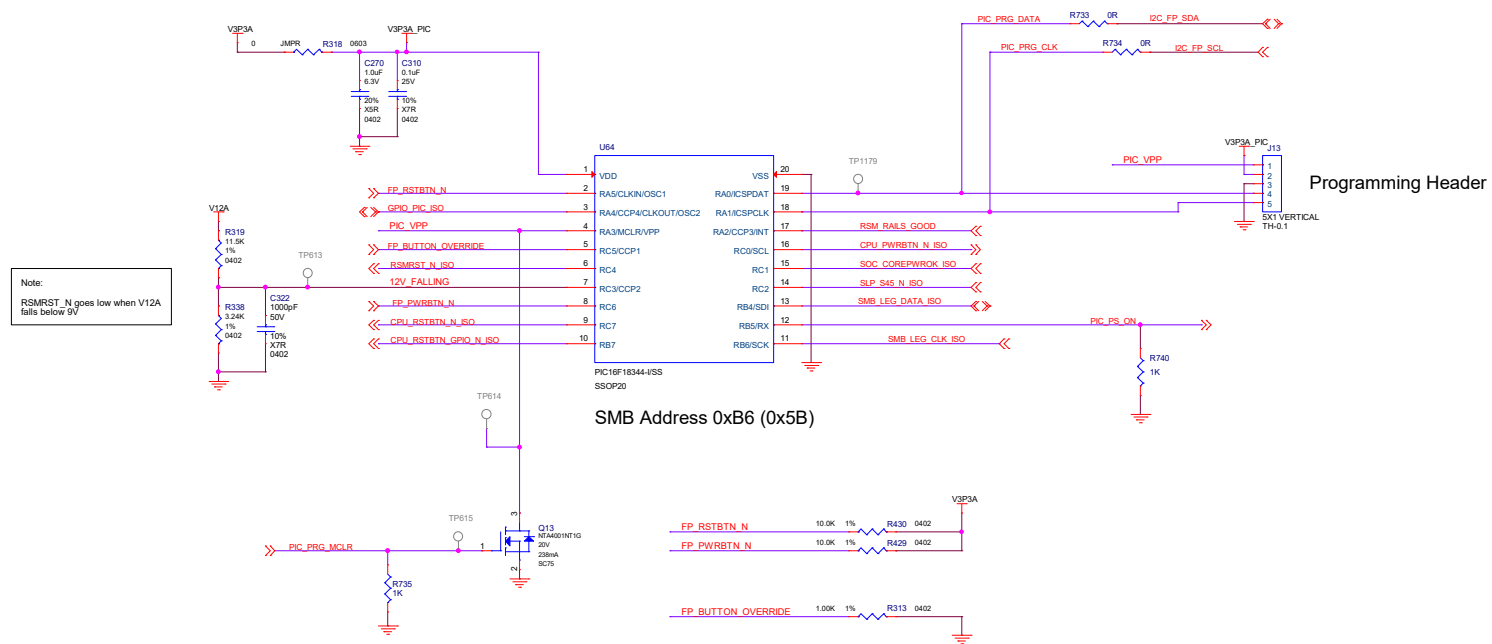
Thermal Diode (next to CPU)



IF CPU core regulators are hot,
then assert PROCHOT_N to throttle CPU.

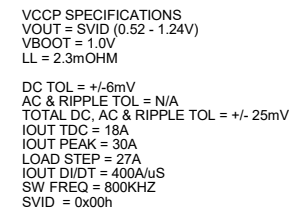


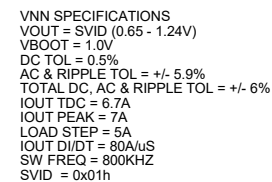
PIC Microcontroller

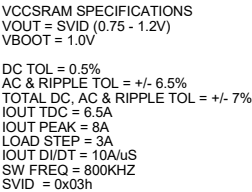


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DATE : Thursday, November 29, 2018								
		AT&T Compute Board						
			SHEET : 42 of SHEETS : 51					

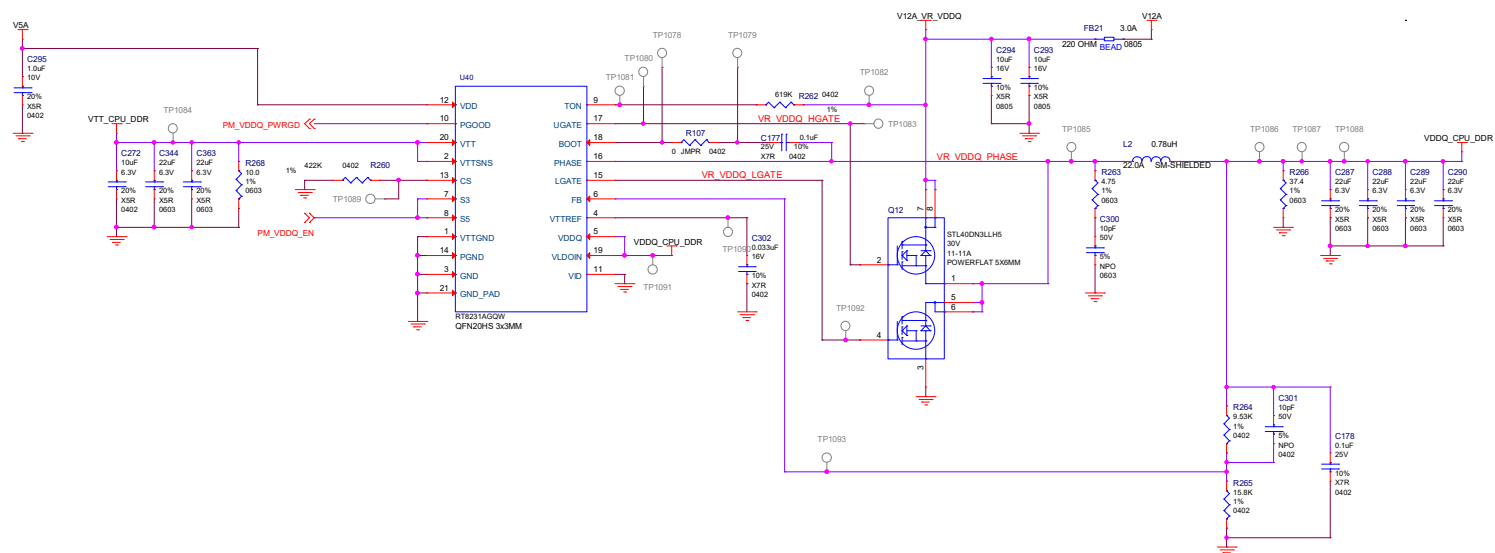






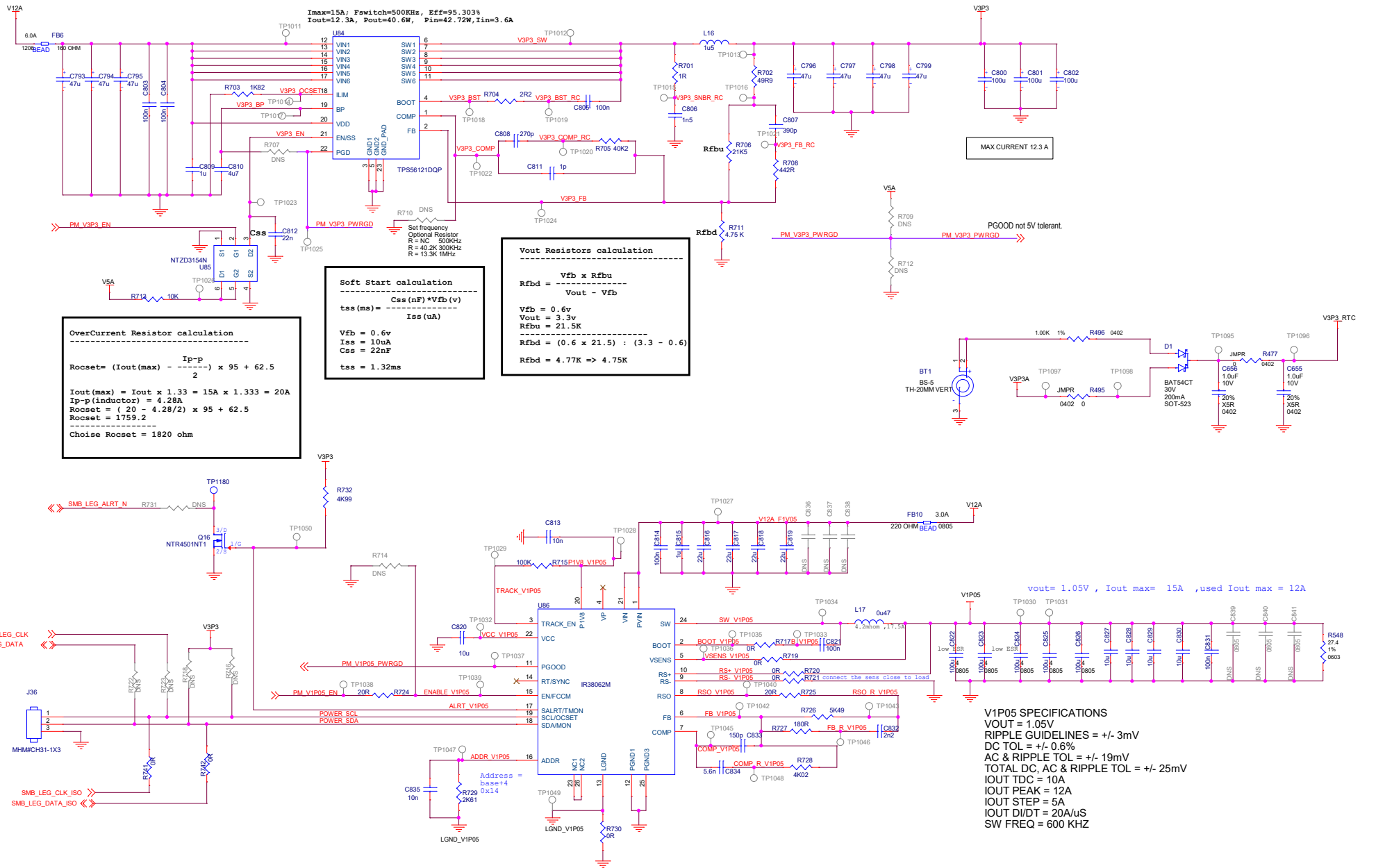
DRAWING No. : 80204-0150-G02			PO VCCSRM VRM SVID 0.75-1.2V								
AssyG02			AT&T Compute Board			APPROVALS			 SILICOM Ltd. Connectivity Solutions A Member of RAD Group		
SIZE : Custom		REV No. : R202-0				CHECK					
DATE : Thursday, November 29, 2018						APPROV.					
						SHEET : 45 of SHEETS : 51					

VDDQ SPECIFICATIONS
VOUT = 1.20V
RIPPLE GUIDELINES = +/- 4mV
DC TOL = +/- 8mV
AC & RIPPLE TOL = +42/-34mV @ SENSE POINT
TOTAL DC, AC & RIPPLE TOL = +50/-42mV @ SENSE POINT
IOUT TDC = 6.4A
IOUT PEAK = 10.1A
IOUT STEP = 3.5A
IOUT dV/dt = 18A/uS
SW FREQ = 400 KHZ

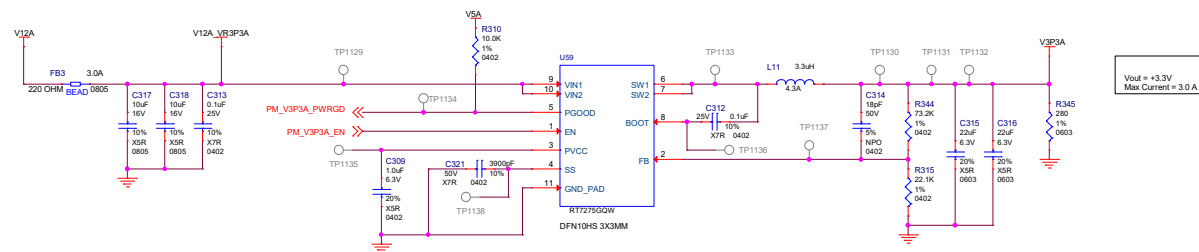
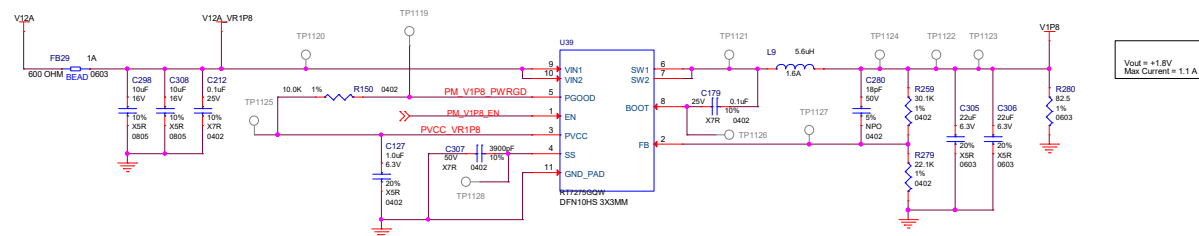
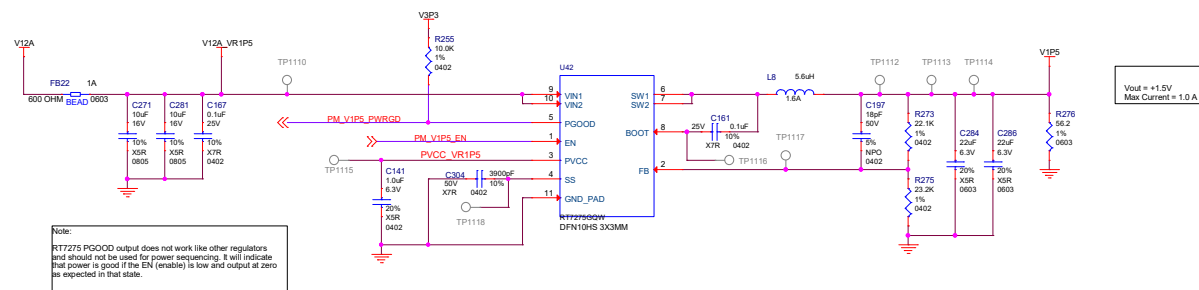
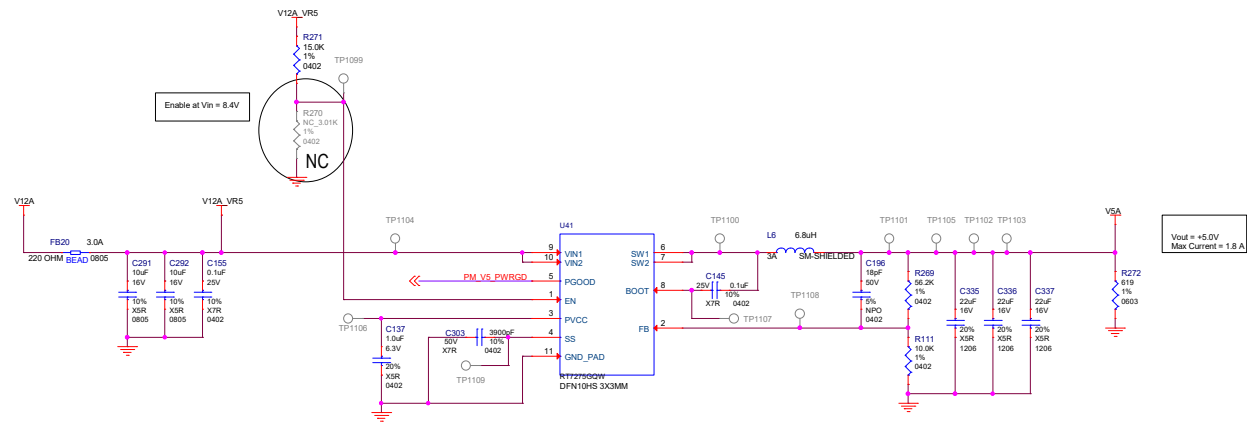


DRAWING No.: 80204-0150-G02		PO VDDQ_CPU_DDR	APPROVALS			 Connectivity Solutions A Member of RAD Group	
AssyG02				NAME	SIGN		DATE
SIZE: Custom	REV No.: R202-00		CHECK				
DATE: Thursday, November 29, 2018			APPROV.				
		AT&T Compute Board	CHECKED BY	DATE	BY		

PS - 3.3V



DRAWING No. : 80204-0150-G02		P P3V3, P1V05 SW	APPROVALS			 SILICOM Ltd. Connectivity Solutions A Member of RAD Group
AssyG02			NAME	SIGN	DATE	
CHECK						
APPROV						
SIZE : C	REV No. : R202-00	AT&T Computer Board	APPROV			
DATE : Thursday, November 29, 2018			APPROV			



DRAWING No. : 80204-0150-G02

AsayG02

SIZE : Custom REV No. : R202-00

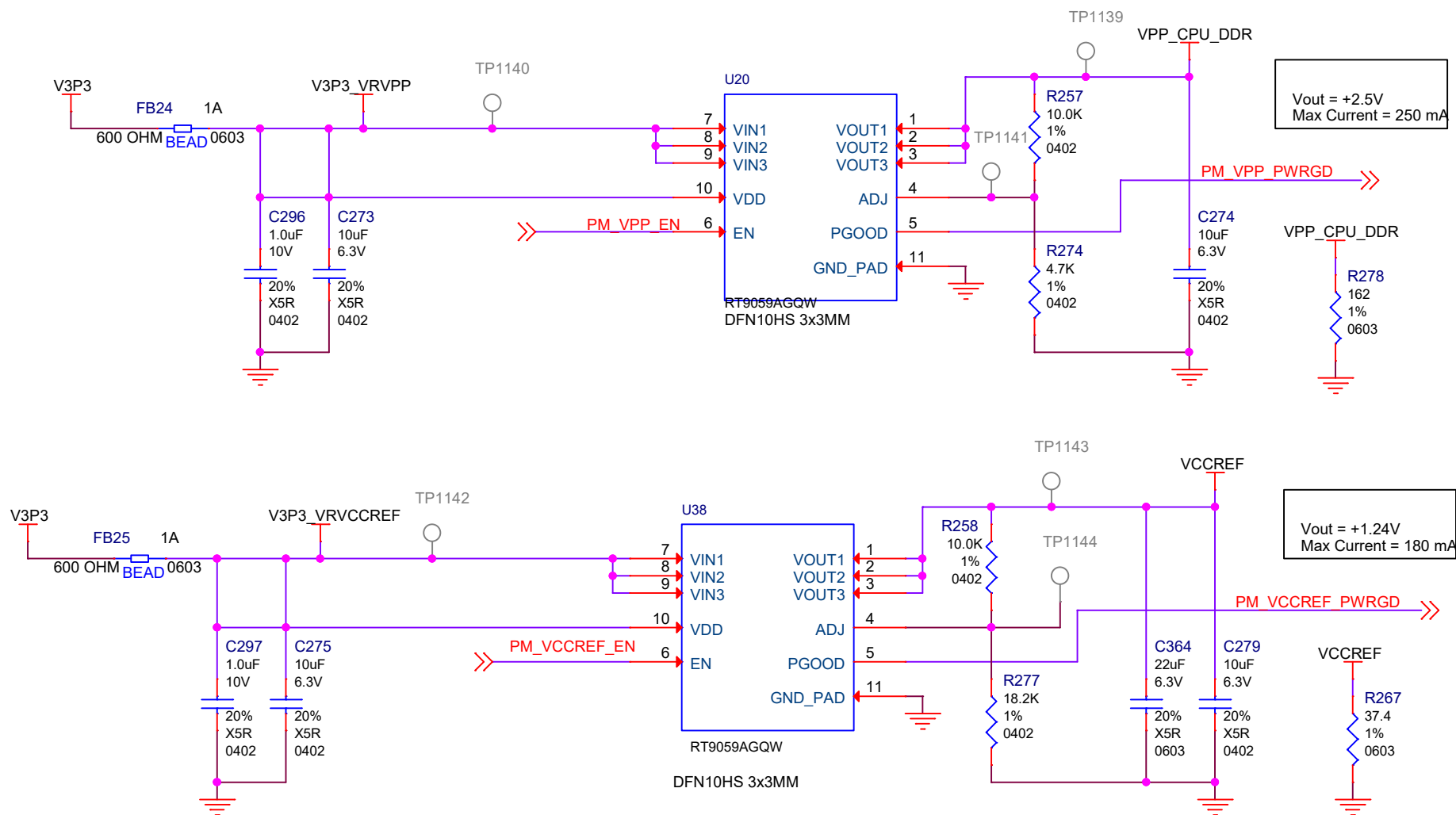
DATE : Thursday, November 29, 2018

PO V5A, V1P5, V1P8, V3P3A

AT&T Compute Board

APPROVALS		
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APPROV.		
SHEET : 48	of SHEETS : 51	

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DRAWING No. : 80204-0150-G02	
AssyG02	
SIZE : A	REV No. : R202-00
DATE : Thursday, November 29, 2018	

PO VPP_CPU_DDR, VCCREF

AT&T Compute Board

APPROVALS			
	NAME	SIGN	DATE
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APPROV.			
SHEET : 49	of SHEETS : 51		

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Revision	Sheet	Description														
X100	n/a	Initial Alpha prototype release.														
X200	29	Swap pinouts on 3 front panel module connectors to support flipped connector orientation in layout.														
	29, 30	Add I2C-based ADC for voltage monitoring. Removed voltage monitor signals from FPM connector.														
	13, 29, 31	Add NC-SI management interface and second SPI CS to FPM connector.														
	28	Add power connector for 2.5" and 3.5" drives.														
	13	Add clear CMOS header.														
	40, 30, 14	Rename PIC_XXX power button and reset button nets to match PIC code.														
	Layout	Replace L2 inductor footprint (was incorrect footprint and required mods).														
	Layout	Add heatsink fin direction notation to assembly drawing and silkscreen layer.														
	Layout	Move inductor L1 down and away from CPU heatsink.														
	Layout	Reset footprint for Q2 FET to default; one of the pads accidentally deleted on Alpha pass.														
	40, 29	Rename FAN_CPU_XXX signals to FAN_CENTER_XXX.														
	Layout	Move J22 fan connector to the right away from J23 fan connector by ~2 mm. The two connectors interfere with both cables plugged in.														
	48, 15	Change clock buffer enable to more reliable RSM_RAILS_GOOD signal. PM_V1P5_PWRGD signal does not operate correctly at powerup.														
	Layout	Misc silkscreen cleanup.														
	15	Replace clock buffer 27.4 kOhm series output resistors with correct 27.4 Ohm value.														
	39	Add SLP_S3_N controlled AND gate inline with COREPWROK signal. It was previously taking down the core rails and then deasserting COREPWROK.														
	28	Replace M.2 M-key slot with B-key slot to support additional WWAN card. Also add 110 mm card mounting hole for longer cards.														
	28, 14	Add USB 2.0 hub to allow simultaneous USB connections to mPCIe and new WWAN slots.														
	27, 28	Connect SOC_WAKE_N signal to all 3 radio cards.														
	29	Remove V5A connections from front panel module (FPM) connector (USB power now generated on FPM). Add more V12A connections.														
	25	Add dual vendor stuffing option resistors for Infineon and Atmel TPM devices.														
	29	Triple AND gate QFN package on CPU_ERROR_N signal no longer available. Change to SOIC package.														
	47	Change RTC power connection from V3P3 to V3P3A.														
	40, 29	Remove inlet thermal diode from motherboard. More appropriate location is on the front panel module closer to the intake vents.														
	40	Change fan signal pullup connections from V3P3 to V3P3A so fans stay active when CPU is down.														
	4, 8, 9	Update block diagrams.														
X201	n/a	Add G02, G03, G04 customer variants. No fab changes.														
	43	Per guidance from ST Micro, change VCCP FETs Q5, Q15 to different part numbers to eliminate issues with lower power CPU SKUs.														
	43	Change VCCP 12V input ferrite to 6.0A part. The 3.0A part did not have enough margin with high-power CPU SKUs and rating also dropped off at higher board temperatures.														
	44, 45	Change VNN, VCCSRAM 12V input ferrite to same 6.0A part as VCCP. Overrated for the application, but simplifies BOM.														
X202	n/a	Add ICT Test Points for all non high speed & DDR nets														
	13	Added U82 74AVCH4T245BQ level shifter for JTAG														
	13	Added J35 - JTAG 11491.1 2x5 male header														
	13,25	Changed SoC JTAG_PU resistors from 51 ohm to 1K ohm														
	47	V3P3 power supply replaced to TPS56121DQP, V1P05 replaced to IR38062M														
R100	39	Touch-up On PM_V3P3_EN signal 1K 0603 between R294.2 and GND VIA as shown below														
	47	Removed R731, Added R732 4.99K, to disconnect IR ALRTN_V1P05 from SMB_LEG_ALRT_N														
	48	Removed R270, pull-down from V5A enable voltage divider														
R200	27	J2 & J21 uSIM connector changed to COT000157														
	28	H7, H10 stand off ORCAD symbol changed and H7 moved from Page 27 to page 28														
	28	H1, H8 & H9 stand off holes changed to MSL#SMT50-M25-3ET														
	41	Added pull-down 1K resistor on PIC_PS_ON signal														
	43	C114 footprint changed														
	47	ALRTN_V1P05 renamed to ALRT_V1P05 consider with IR logic														
	47	Added Q16 open drain between IR ALRT_V1P05 and SMB_LEG_ALRT_N														
	47	Added R732 4.99K to IR ALRT_V1P05														
	47	Added 4 optional resistors for option IR I2C moving from SMB_LEG to SMB_LEG_ISO														
R200-02	13,25	JTAG PULL-UP resistors: R431, R446, R458 & R562 changed from ERS000297 (49.90hm) to ER#04021KFT (1Kohm)														
R200-03	27	Added two MECH parts COT000130 for mPCIe connector														
R202-00		BOM Cleanup for Mass production Update of 80200-0150-G02														
		<table><tr><th>Name</th><th>Reference Designator</th></tr><tr><td>XDP Debug Port(COT000136)</td><td>J14</td></tr><tr><td>Power for offboard HDD/SSD</td><td>J10</td></tr><tr><td>SATA - A</td><td>J18</td></tr><tr><td>SATA/SATADOM - B</td><td>J17</td></tr></table>	Name	Reference Designator	XDP Debug Port(COT000136)	J14	Power for offboard HDD/SSD	J10	SATA - A	J18	SATA/SATADOM - B	J17				
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