EP100-S1 (Wiwynn 1U openEDGE server)

Revision 0.3

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Revision history

Revision	Editor	Description
V0.1 (July, 2020)	Frank Ty Chen	First draft
V0.2 (August, 2020)	Frank Ty Chen	Revise author names
V0.3 (October, 2020)	Frank Ty Chen	Add appendix

Contents

2   Introduction

Wiwynn EP100 is designed based on the OpenEdge Server concept to fulfill various Edge computing requirements and use cases.

EP100 is a single-socket server that supports the Purley Platform Xeon-SP processors in combination with the Lewisburg PCH (PCH) to provide a balanced feature set between technology leadership and cost.

This specification defines the interfaces and connection topology of various buses and control signals in the compute node.

3   Product Architecture Overview

EP100-S1 Edge Server main characteristics and features are listed below:

Table 1: Server Feature List

| Item Name	Specifications
Form Factor	215mm x 421.8mm x 41mm (W x D x H), 1RU Height
Power Supply	DC 12V from Backplane
Fan	4x 4056 PWM Fan, Fans are controlled by the BMC in Sled.
MB	412.4mm x 205.8mm
CPU	1x Intel Skylake / Cascade Lake, U- (Design reserve) & N-type SKUs
System Chipset	1x Intel Lewisburg PCH C621 (C627 for QAT Option)
Memory	8x ECC DIMM Slots : Option 1 : 8x DDR4 R DIMM Option 2 : 6x DDR4 R DIMM + 2x DCPMM DIMM
Sled Management	ASPEED AST2500 with VGA
Boot/Data Drive	- Support two boot drive with M.2 PCIe Gen3 x4 port (support 2280/22110) - Support two U.2 7-mm drives with PCIe Gen3 x4 each, or two SATA 7mm SSD
Expansion Slots	- One PCIe Gen3 x16 OCP 3.0 Slot - One PCIe FHHL Gen3 x16 Slots
IO Ports	- OCP NIC 3.0, VGA port, USB, Debug port
Sled LED Indicators	- Power, UID,
Sled Button	- Power, UID, RST

3.1   Server Board Block Diagram
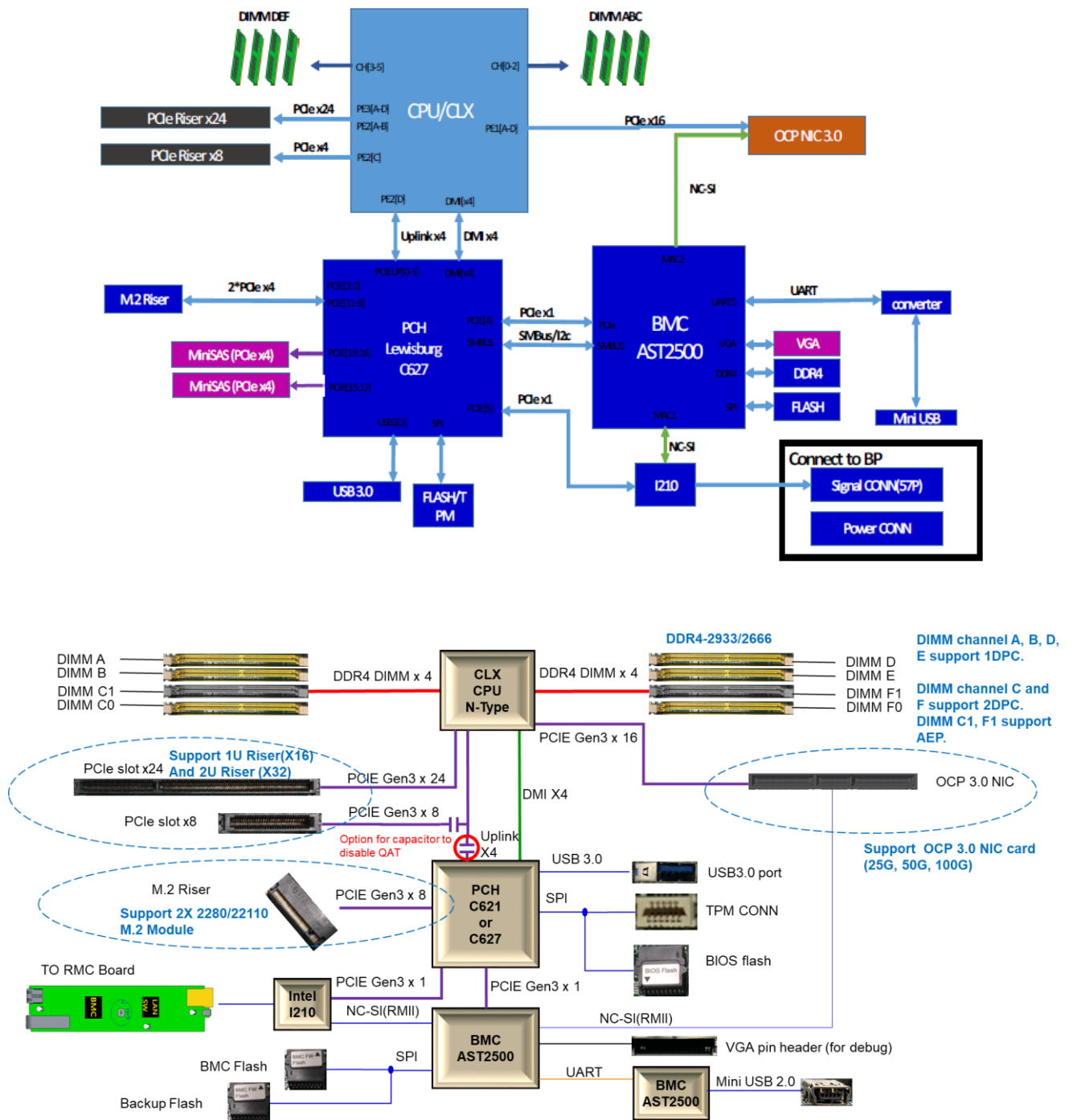
Figure 1: Server Board Block Diagram

3.2 Server Board

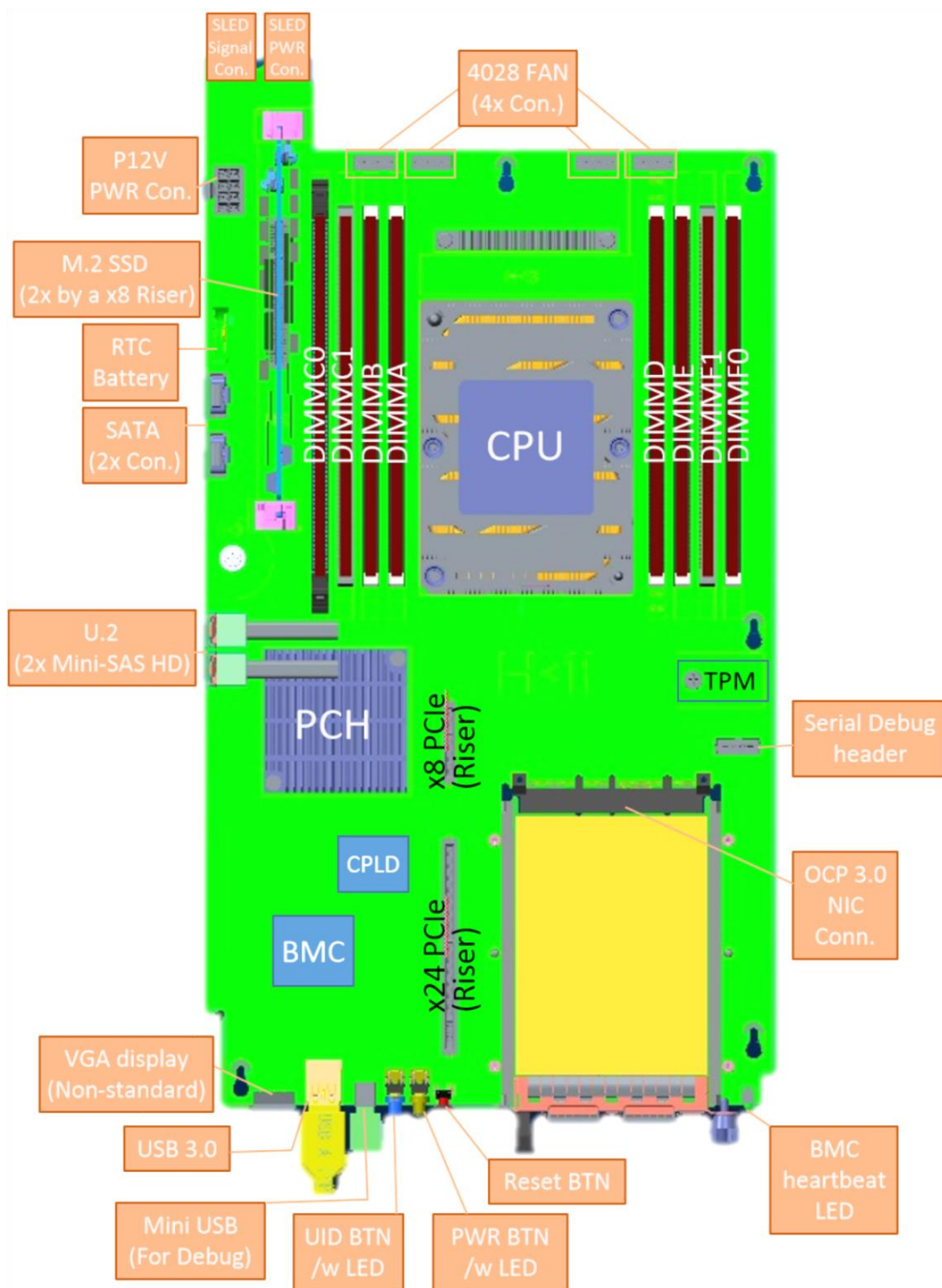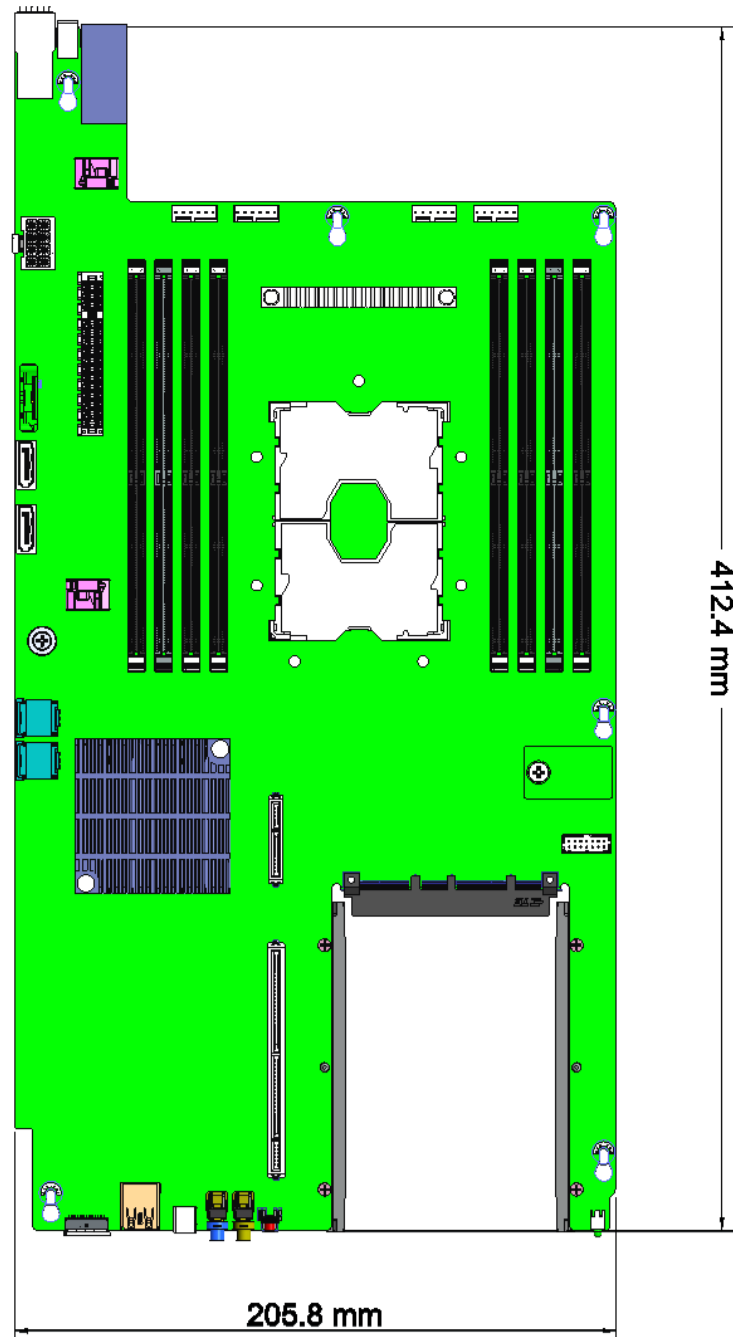### 3.2.1 Server Board Placement

Figure 2: Server Board Placement

3.2.2   Server Board Dimension

Server Board dimensions are 205.8 mm (W) x 412.4 mm (L).

Figure 3: Server Main Board Dimensions

3.2.3   Processor

The Cascade Lake SP is the next generation of Intel® Xeon® SP processor built on 14-nm process technology. The processor is designed for a platform consisting of at least one Cascade Lake SP processor and the Platform Controller Hub (PCH). Included in this family of processors are integrated memory controller (IMC) and an Integrated I/O (IIO) on a single silicon die.

All processor types support up to 48 lanes of PCI Express* 3.0 links capable of 8.0 GT/s. It features two Integrated Memory Controllers (IMC), each IMC supporting up to 3 channels of DDR4 DIMMs with up to two DIMMs per channel.

3.2.4   PCH

The PCH's core name of Purley platform is named "Lewisburg". It is an Intel C620 series chipset.

Lewisburg Key Features:

• ACPI Power Management Logic Support, Revision 4.0a

• PCI Express* Base Specification Revision 3.0

• Integrated Serial ATA host controller supports data transfer rates of up to 6 Gb/s on all ports.

• xHCI USB controller with SuperSpeed USB 3.0 ports

• Direct Media Interface

• Serial Peripheral Interface

• Enhanced Serial Peripheral Interface

• Flexible I/O—Allows some high speed I/O signals to be configured as PCIE root ports, PCIE uplink for use with certain PCH SKUs, SATA (and sSATA), or USB 3.0.

• General Purpose Input Output (GPIO)

• Low Pin Count interface, interrupt controller, and timer functions

• System Management Bus Specification, Version 2.0

• Integrated Clock Controller / Real Time Clock Controller

• Intel® High Definition Audio and Intel® Smart Sound Technology

• Integrated 10/1 Gb Ethernet

• Integrated 10/100/1000 Gigabit Ethernet MAC

• Supports Intel® Rapid Storage Technology Enterprise

• Supports Intel® Active Management Technology and Server Platform Services

• Supports Intel® Virtualization Technology for Directed I/O

• Supports Intel® Trusted Execution Technology

• JTAG Boundary Scan support

• Intel® QuickAssist Technology

• Intel® Trace Hub for debug.

• Innovation Engine

• ADR Support

3.2.5   Memory

There are six memory channels (A, B, C, D, E, F) in the server board design and it supports eight DIMM slots.

CH A, B, D and E are 1DPC. CH C and F are 2 DPC. CH C and F also support Intel AEP. Here is the population matrix.

	Channel A	Channel B	Channel C		Channel D	Channel E	Channel F	
	Slot 0	Slot 0	Slot 0	Slot1	Slot 0	Slot 0	Slot 0	Slot1
Config1	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
Config2	DRAM	DRAM	DRAM	Empty	DRAM	DRAM	DRAM	Empty
Config3	DRAM	DRAM	DRAM	AEP	DRAM	DRAM	DRAM	AEP
Config4	DRAM	DRAM	AEP	Empty	DRAM	DRAM	AEP	Empty

The DIMM identifiers on the silkscreen on the board provide information about the channel to which they belong. For example, DIMM_A0 is the first slot on Channel A of processor.
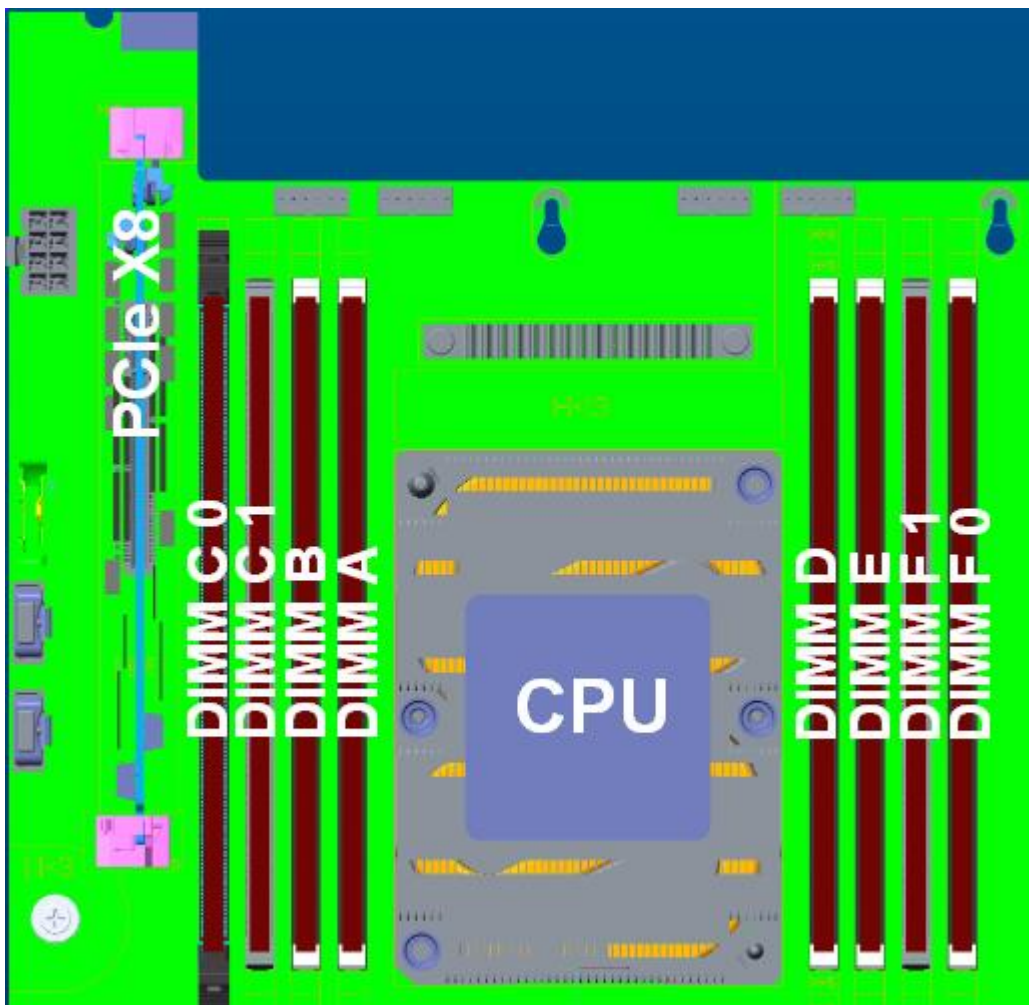

Figure 4: Server Sled DDR Physical Slots

3.2.6   PCIE Lanes

CPU PCIE Port2

The PCIE x8 lanes between CPU, PCH and X8 PCIe slot connector are in group of PCIE x 4 lanes.

Configuration 1:

PCH is C621.

CPU PCIE P2CD PCIE x 8 lanes are connecting to PCIe x8 Slot.

Configuration 2

PCH is C627 and supports PCIe x4(P2D) for QuickAssist.

CPU PCIE P2C PCIE x 4 lanes are connecting to PCIe x8 Slot.

3.2.7   SATA, U.2 and M.2

The PCH has two integrated SATA host controllers that support independent DMA operation.

EP100 has two M.2 (supporting NVMe M.2 2280 and 22110), two mini-SAS HD connectors (PCIe protocol) and two 7p SATA connectors. Mini-SAS HD connectors with connection to PCH PCIe Gen3 support two U.2 NVMe. Boot drive can choose from U.2 or M.2.

3.2.8   USB

The Lewisburg PCH supports total 14 USB ports, six USB 2.0 ports and eight USB 3.0 ports. The USB port distribution of EP100-S1 Edge Server is as follows:

- ASPEED BMC AST2500 consumes two USB 2.0 ports (one 1.1 and one 2.0)

- One USB3.0 port in front side

- One Mini USB port for debugging in front side

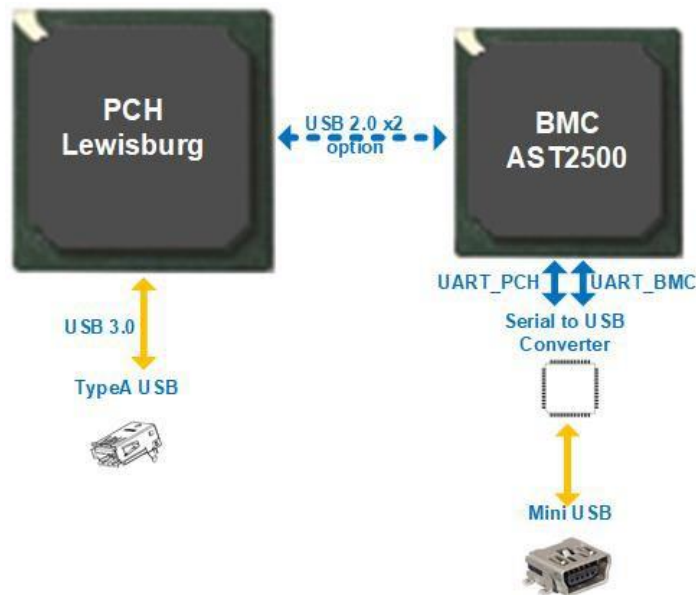The USB ports on the products are not required to be powered from STBY.

Figure 5: Server USB Ports

3.2.9   AST2500

The Server's Board Management Controller (**AST2500**) is a highly integrated single-chip solution, integrating several devices typically found on servers.

VGA Display Controller

- Fully IBM VGA compliant

- Maximum Display resolution: 1920x1200 32bpp@60Hz (reduced blanking)

- Support widescreen resolutions:

    – WXGA: 1280x800 32/16bpp @60Hz

    – WXGA+: 1440x900 32/16bpp @60Hz

    – WSXGA+ : 1680x1050 32/16bpp @60Hz

    – FullHD+ : 1920x1080 32/16bpp @60Hz

DDR3L/DDR4 SDRAM Controller

- Support external 16-bit DDR3L/DDR4 SDRAM data bus width

- Maximum memory clock frequency

    - DDR3L: 800MHz (DDR3-1600)

    - DDR4: 800MHz (DDR4-1600)

3.2.10 TPM

EP100-S1 Edge Server's PCH supports TPM specification 2.0 implemented with a TPM header on server sled. It supports SPI interface TPM 2.0 module.

3.2.11 UART

EP100-S1 Edge Server provides Host and BMC UART interfaces for development purpose. Both UARTs connect to a UART to USB converter on the server board. The USB connect to a mini-USB connector at the front IO. User can use an USB cable to link the USB port to laptop to access the UARTs.

3.2.12 LOM

The LOM solution in EP100-S1 Edge Server is Intel Ethernet controller I210-AT. I210-AT is a single port, compact, low power component that supports GbE designs. The I210 offers a fully-integrated GbE Media Access Control (MAC). The I210-AT enables 1000BASE-T implementations using an integrated PHY. Below are the features of I210-AT

- Operating Temperature: 0 to 70 °C.

- PCIE v2.1 (2.5 GT/s) x1 is used by the I210 as a host interface. In EP100-S1 Edge Server, the PCIE interface connects to PCH PCIE port.

- Network Interface: 1000 Base-T. In server sled, the 1000 Base-T is routing on the server sled towards the back plane.
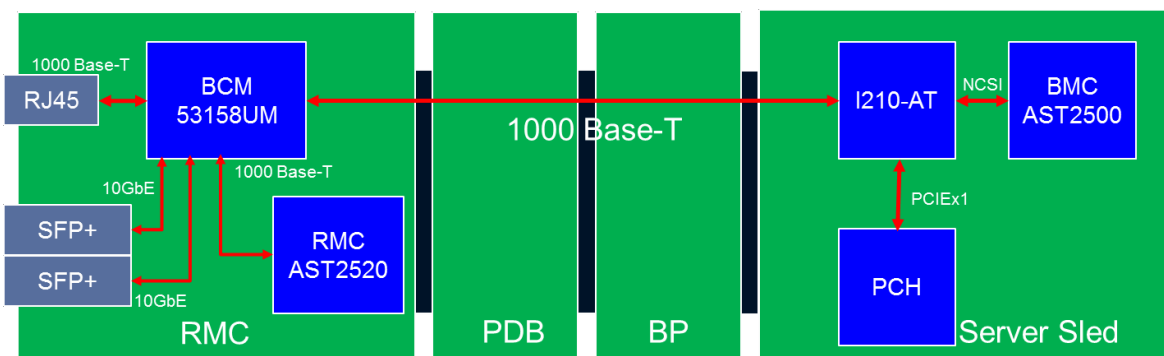
Figure 6: 1000 Base-T routing topology

 – It provides the following capabilities for the BMC on the server sled:

1. A dedicated 1000 BASE-T Ethernet port for hardware management. User can remote manage the server sled via this interface.

2. RMC can get the sled information via this interface.

- Manageability: NCSI interface. This is accomplished by providing mechanisms by which manageability network traffic is routed to and from BMC.

 – In EP100-S1 Edge Server, NCSI interface is connected to BMC. The usable bandwidth for either direction is up to 100 Mb/s for the NCSI interface.

3.2.13 Power Connector for Accelerator Card

EP100-S1 Edge Server can support FHHL accelerator card. The accelerator card needs the external 12V power feed via the cable. There is an 8-pin power connector on the server sled to offer the 12V power feed for accelerator.

3.2.14 Thermal Design

3.2.14.1 Thermal solution for 1U sled

CPU Heat Sink

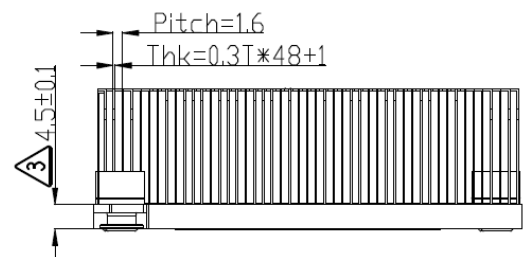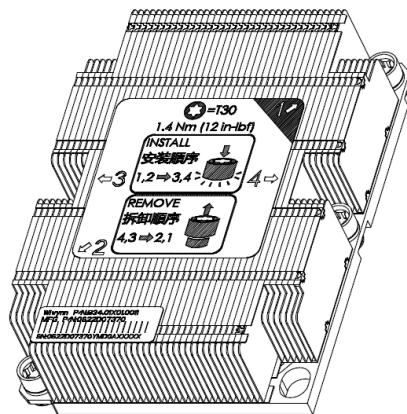- Dimensions=78*108*25.5 mm^3

- Material=Al base + Cu block + Al Fin

Figure 7: 1U CPU Heat Sink

System Fan x4

● Dimensions=4056 (dual rotor)

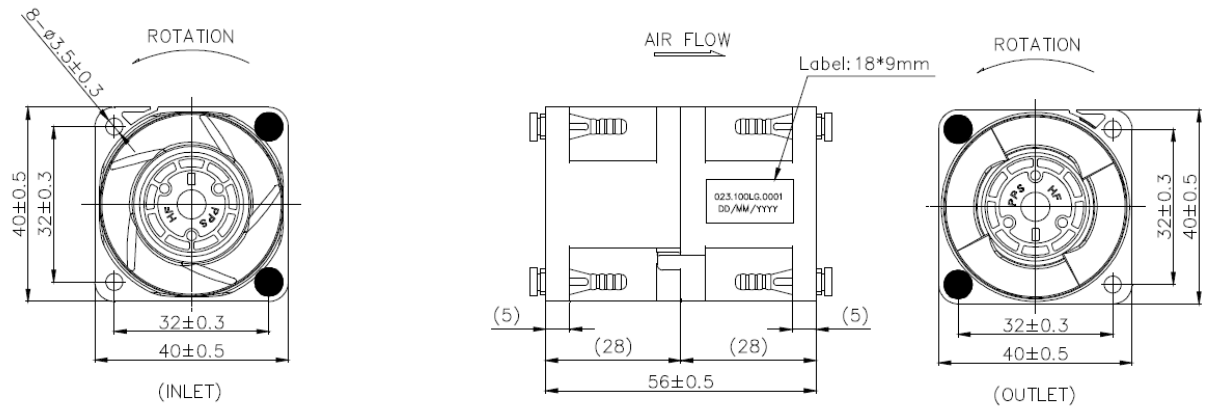● Voltage:12 V

Figure 8: 4056 Fan Drawing

4   Chassis Spec

4.1   1U Sled Overview

Dimensions are 475mm (D) x 215mm (W) x 4 mm (H).

2U chassis can support these configurations:

- Two M.2 cards

- One x16 FHHL PCIE card
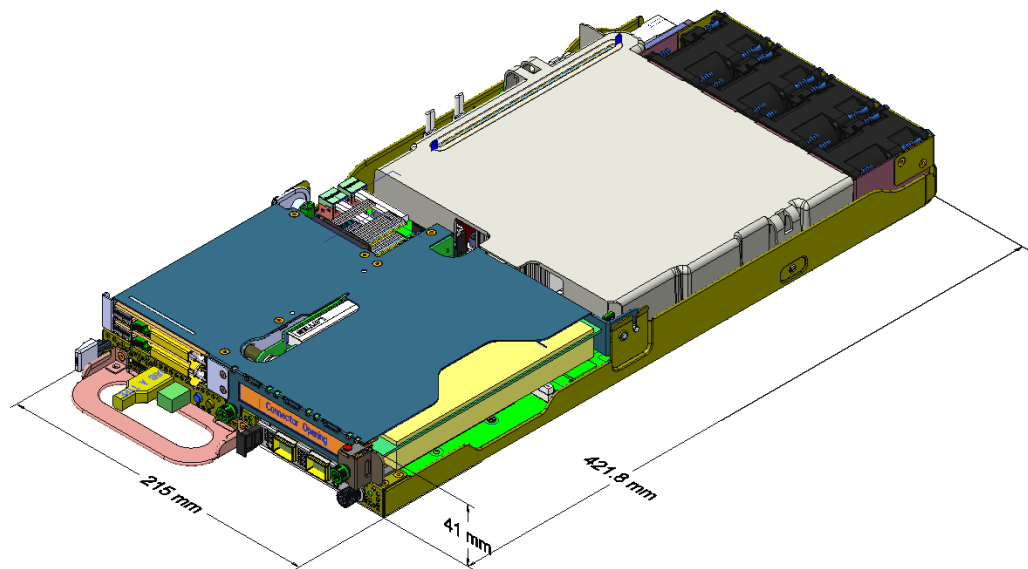
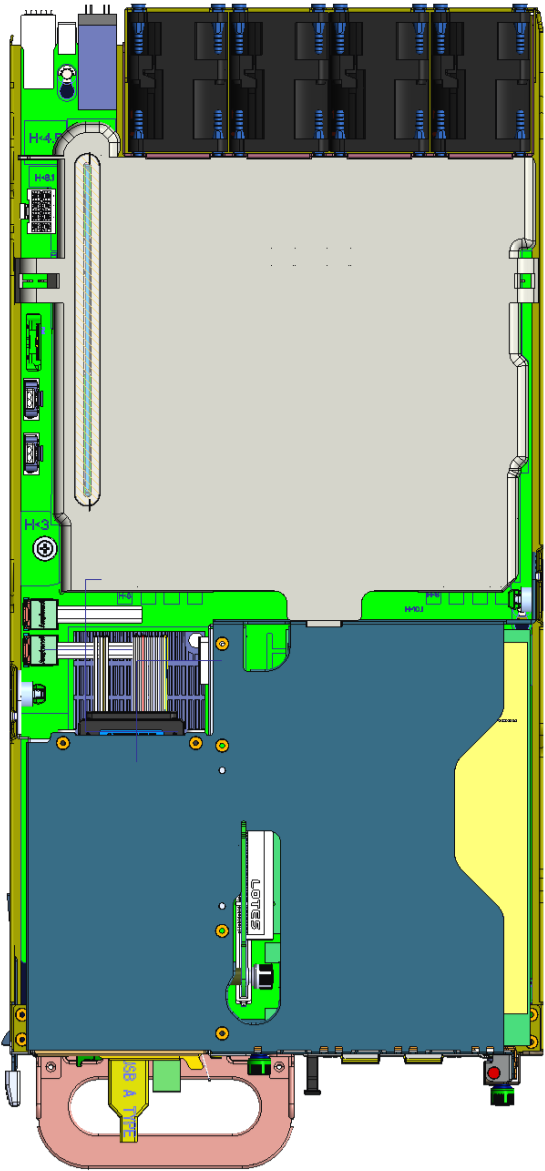- Two local 2.5" 7mm wide NVMe or SATA disks

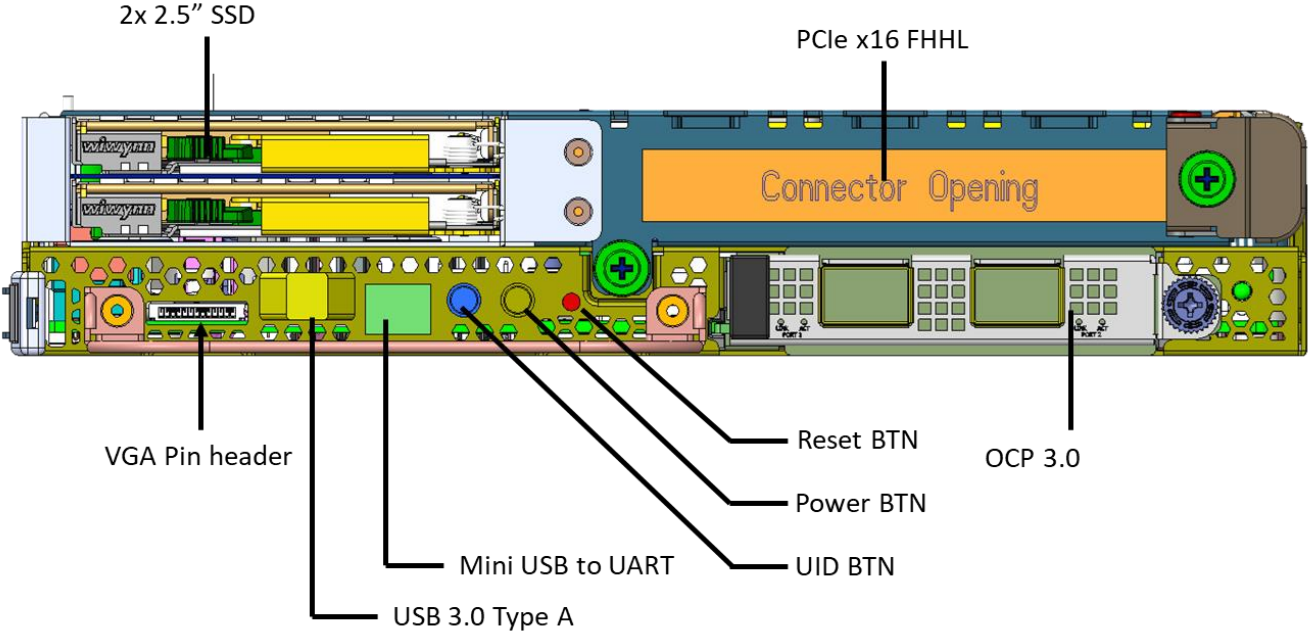**Figure 9: 1U Sled Overview**

Figure 10: 1U Sled Top View

Figure 11: 1U Sled Front View

5 Appendix

5.1 User Guidance

In the industry, there is a known vulnerability, CVE-2019-6260, when using ASPEED AST2500.
There are some approaches to mitigate:

    a.   Designers can refer to AST_usrGuide_QuickRef for CVE-2019-6260 to fine tune the firmware.

    b.   Designers can use another BMC chip to replace ASPEED AST2500 in the derivative designs.

1.1 Wiwynn actions to Aspeed QuickRef

According to CVE-2019-6260, ASPEED AST2400 and AST2500 Baseband Management Controller (BMC) hardware and firmware implement Advanced High-performance Bus (AHB) bridges, which allow arbitrary read and write access to the BMC's physical address space from the host.
The LPC, PCIe and UART AHB bridges are all explicitly features of ASPEED's designs for recovering BMC FW during firmware development or to allow the host to drive the BMC hardware even without any firmware on BMC.
The CVE applies to the Eight (8) specific cases of iLPC2AHB bridge Pt I, iLPC2AHB bridge Pt II, PCIe VGA P2A bridge, DMA from/to arbitrary BMC memory via X-DMA, UART-based SoC Debug interface, LPC2AHB bridge, PCIe BMC P2A bridge, and Watchdog setup.

- iLPC2AHB bridge Pt I

[Suggested Mitigation of CVE] Can be disabled by configuring a bit in the BMC's LPC controller.
Wiwynn would disable the AST2500 L2A bridge in the firmware.

- iLPC2AHB bridge Pt II

[Suggested Mitigation of CVE] Disable Super I/O decoding on the LPC bus (0x2E/0x4E decode).
Decoding is controlled via hardware strapping and can be turned off at runtime,
however disabling Super I/O decoding also removes the host's ability to configure SUARTs, System wakeups, GPIOs and the BMC/Host mailbox

After disabling Super I/O function, it would impact POSTCode, COM1/2 and SOL functions.
Wiwynn would disable L2A bridge and Super I/O function as the default setting, yet it will be configurable when needed.

- PCIe VGA P2A bridge

[Suggested Mitigation of CVE] Can be disabled or filter writes to coarse-grained regions of the AHB by configuring bits in the System Control Unit
Wiwynn would disable the AST2500 PCI2AHB bridge in the firmware.

- DMA from/to arbitrary BMC memory via X-DMA

[Suggested Mitigation of CVE] X-DMA accesses are configured to remap into VGA reserved memory in u-boot
Wiwynn would block the AST2500 X-DMA access in the firmware.

- UART-based SoC Debug interface

[Suggested Mitigation of CVE] Can be disabled by configuring a bit in the System Control Unit.
Wiwynn would disable the AST2500 U2A function in the firmware.

- LPC2AHB bridge

[Suggested Mitigation of CVE] Don't enable the feature.
Wiwynn would disable the AST2500 LPC_2_SPI function in the firmware.

- PCIe BMC P2A bridge

[Suggested Mitigation of CVE] Don't enable the feature.

Wiwynn would disable the AST2500 PCI BMC device in the firmware

- Watchdog setup

[Suggested Mitigation of CVE] State: Required system function, always available

Wiwynn would only trigger Watchdog Timer in the "SOC Reset" mode

- PCIe BMC P2A bridge

[Suggested Mitigation of CVE] Don't enable the feature.

Wiwynn would disable the AST2500 PCI BMC device in the firmware