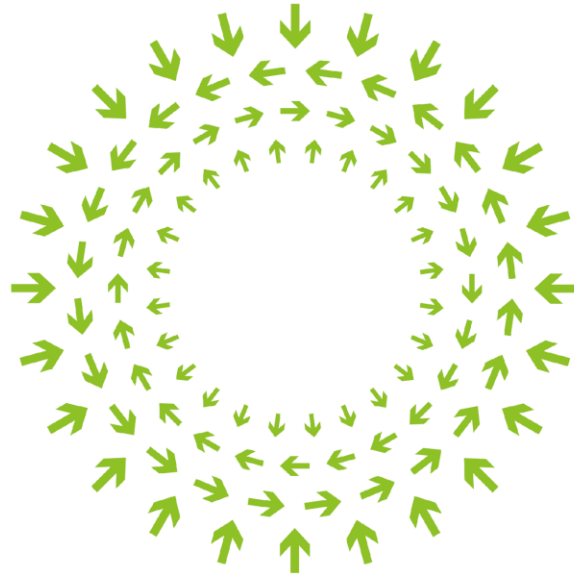




OPEN
Compute Project

Whitestone2 ORAN DU Hardware SPEC

Version 1.1

Author: Alex Chou

Version History

Date	Version #	Author	Description
01 Dec 24	1.0	Alex Chou	Initial release.
17 Dec24	1.1	Alex Chou	Removed & deleted instructions from template and make format consistent.

Current Template Version:

3 Layer (Base, Design and Product) Specification Template V1.1.0

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1. License

1.1. Open Web Foundation (OWF) CLA

Contributions to this Specification are made under the terms and conditions set forth in Modified OWF-CLA-1.0 (As of August 16, 2021) ("Contribution License") by:

MiTAC Computing Technology Corp.

Usage of this Specification is governed by the terms and conditions set forth in **Modified OWFa1.0 Final Specification Agreement (FSA) (As of August 16, 2021)** ("**Whitestone 2 ORAN DU hardware SPEC**").

You can review the applicable Specification License(s) referenced above by the contributors to this Specification on the OCP website at <http://www.opencompute.org/participate/legal-documents/>. For actual executed copies of either agreement, please contact OCP directly.

Notes: "None"

The above license does not apply to the Appendix or Appendices. The information in the Appendix or Appendices is for reference only and non-normative in nature.

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BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND EVEN IF OCP HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following for their feedback:

List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

3. Compliance with OCP Tenets

3.1. Openness

The Whitestone 2 ORAN DU is design for Open RAN for Telco subproject.

3.2. Efficiency

- 48V DC input to keep power efficiency by DC (but not AC to DC).
- Integrated FEC accelerator into Intel CPU.
- BMC for fan control.

3.3. Impact

ALL vDU, vCU features are integrated in an 1U compact server.

3.4. Scale

Chip down NIC for multiples use cases (FH/MH) and also daisy chain.

3.5. Sustainability

Low power design 400W ~ 800W for Telco cell site.

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4. **Scope**

This document defines the hardware specification for MiTAC Whitestone2 ORAN DU along with its FW for use it.

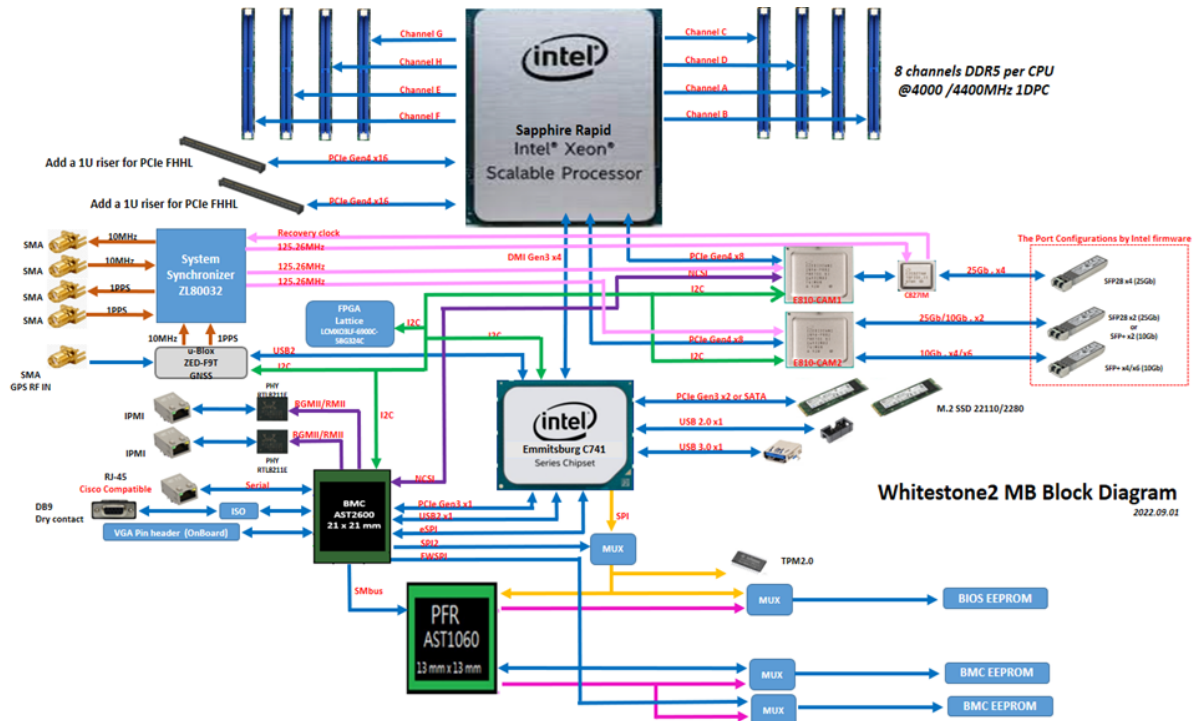
5. Overview

MiTAC Whitestone2 ORAN DU is designed for Open RAN DU at cell or tower site in an outdoor cabinet for data and control between RU (radio unit) & DU (distributed unit) and DU & CU (central unit) by x86 platform (Intel Xeon-SP) integrated hardware FEC accelerator and multiple networking options.

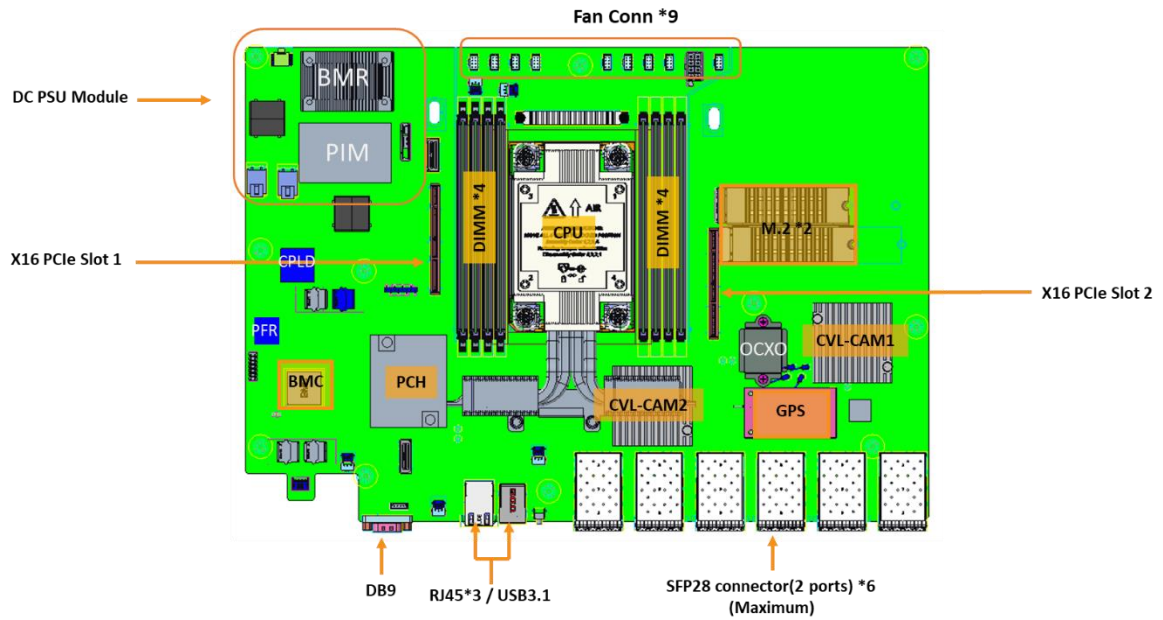
6. Base Specifications

6.1. Physical Specifications

6.1.1 Block Diagrams



6.1.2. Placement and Form Factor



6.1.3. Figures

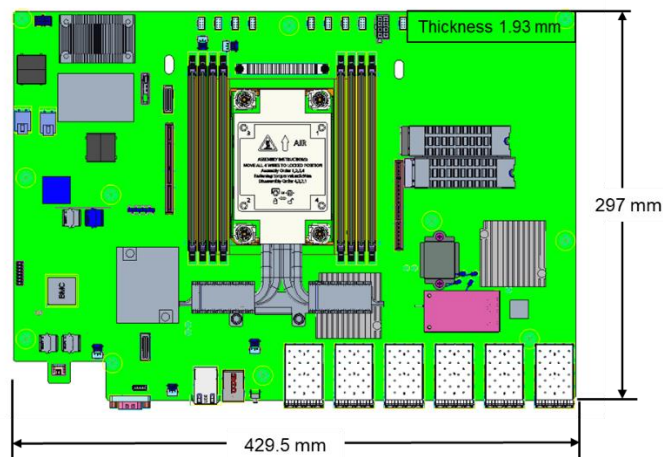
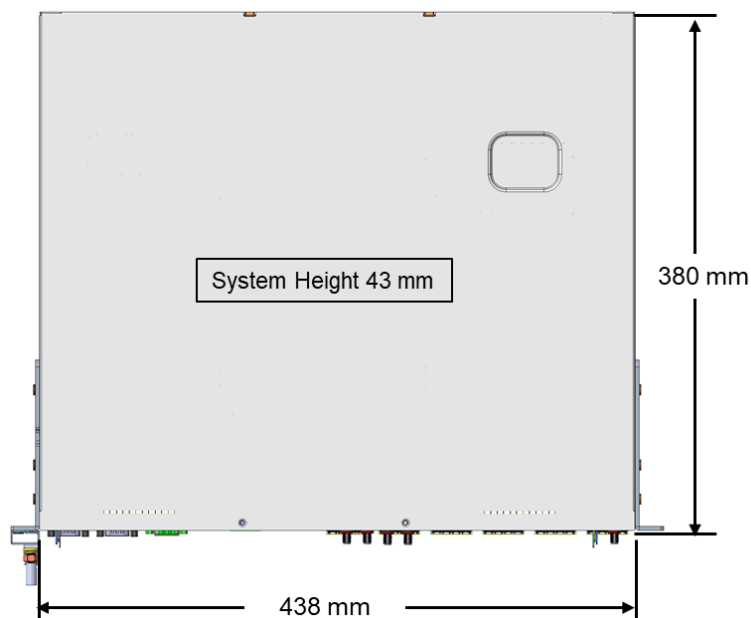


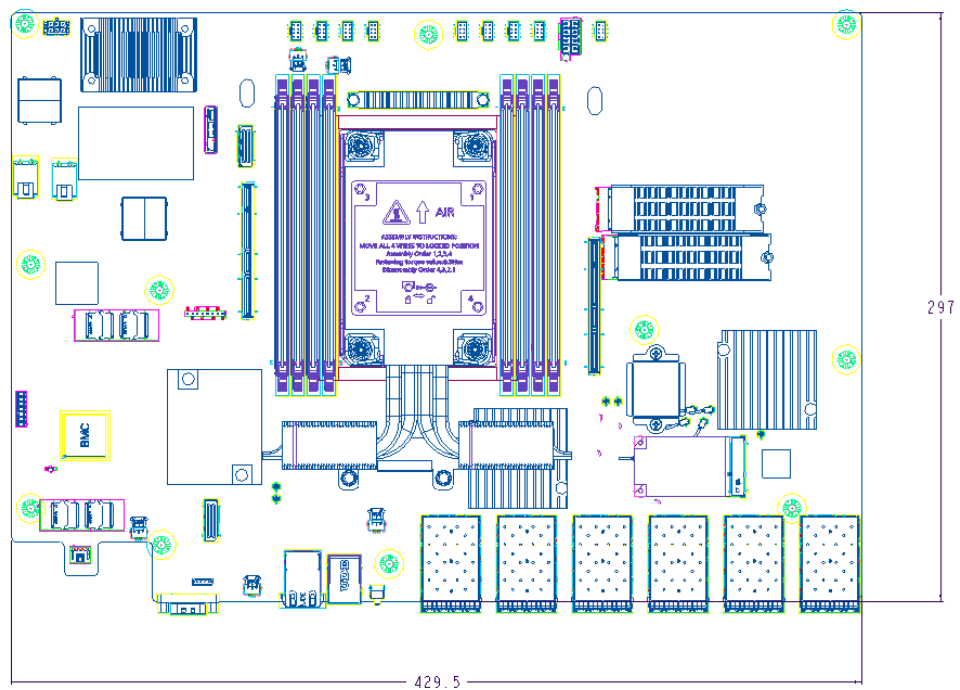
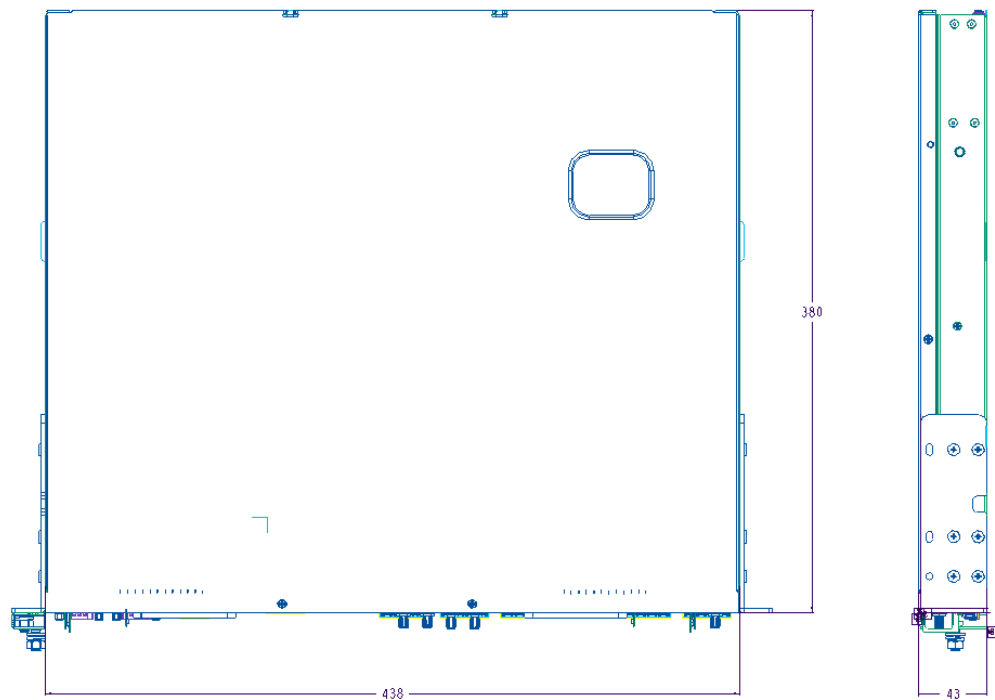
6.2. Mechanical

6.2.1. Rack Compatibility

MiTAC Whitestone2 ORAN DU is designed for EIA-19" rack and Telco-19" rack (600mm depth)

6.2.2. Dimensions

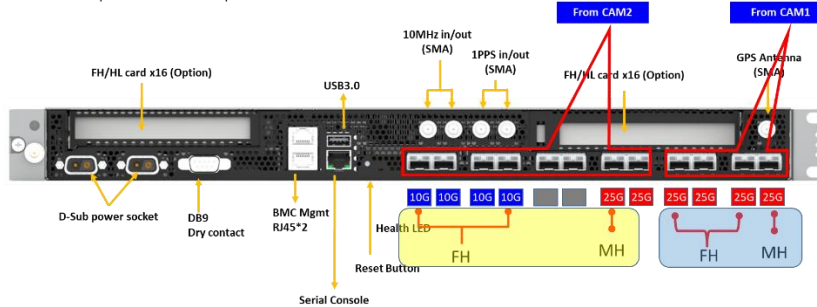




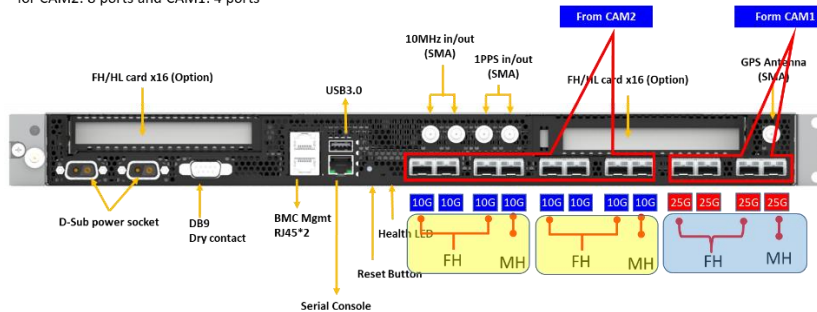
6.2.3. General Requirements

MiTAC Whitestone2 ORAN DU is 1U server with 380mm depth

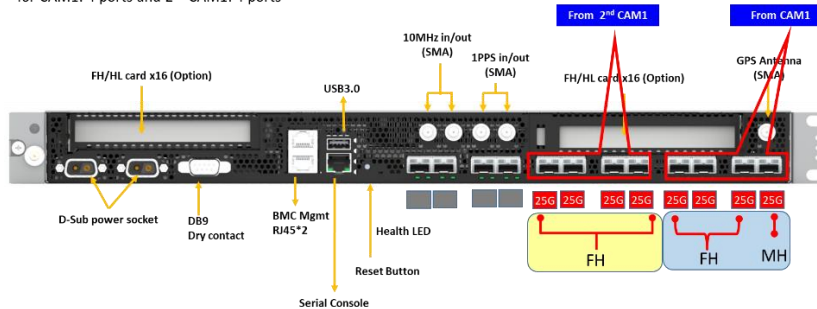
Config 1
for CAM2: 6 ports and CAM1: 4 ports



Config 2
for CAM2: 8 ports and CAM1: 4 ports



Config 3
for CAM1: 4 ports and 2nd CAM1: 4 ports



6.3. Electrical Requirements

Processor

Intel Sapphire Rapids

- 5433N SPR-EE-LCC, 20C 160W
- 6443N/6433N SPR EE-MCC, 32C 195W
- 6433NE SPR EE-MCC, 32C 205W (eTemp)

Chipset

- C741

Acceleration on board

- ACC200 integrated into SPR EE SKU
- Intel Columbiaville CAM1 NIC
- Intel Columbiaville CAM2 NIC

Memory

- 8x DDR5 DIMM (1DPC)
- SPR EE-LCC, 4000 MT/s DDR5
- SPR EE-MCC, 4400 MT/s DDR5

Local Storage

- 2x M.2 2280/22110 PCIe Gen.3/ SATA SSD

Expansion

- 2x PCIeG4 x16 FHHL

Synchronization

- IEEE1588 V2 PTP & SyncE support
- On board GPS module (Option)
- DPLL/OCXO design
- T-BC and T-TGM capabilities (C1, C2, C3)
- 8 hours hold-over time options

Management

- AST2600, Redfish, IPMI

Security

- PFR (Aspeed AST1060 RoT)

Physical

- Front-to-back airflow, 1RU, 380mm max depth

Power

- 800/600W Dual feeds -48VDC, front access

Cooling

- Rear fan set, 8+1 redundancy 4056 dual rotor fans

Operating temperature

- -40 °C to +55/65 °C (205/195W)

6.4. BIOS

MiTAC internal project BIOS specification addresses what features and configurations provided for a standard product. The information is intended to allow delivering whole native defined features and could eliminate the difference to other project.

Following sections will define the internal project (IP) features in detail and make all IP BIOS firmware with simultaneous functionalities and higher quality. The subjects are covered in implementing of BIOS Firmware Layout, Remote Control Management, Supported Software, Booting Device, BIOS/BMC Interaction, Event Log Handling, Error Handling, Board Information, BIOS Naming Convention etc. The implementation engineer shall refer this document to deliver IP BIOS firmware with fully understand of all technical concepts of features.

6.4.1. BIOS Requirement

6.4.1.1 Flash Image

A BIOS image resides in the SPI flash part which is along with other components such as Intel Management Engine firmware, platform descriptor, device expansion region, etc. The flash consists of several regions for storing these components.

BIOS (Required)

This region contains code and configuration data for the entire computer.

Platform Descriptor (Required)

This region contains information such as the space allocated for each region of the flash image, read-write permissions for each region, and a space which can be used for vendor-specific data. It takes up a fixed amount of space at the beginning of the flash memory.

Intel ME (Required)

This region contains code and configuration data for Intel® ME applications. It takes up a variable amount of space up to the BIOS region.

6.4.1.2 BIOS Update Requirement (PFR Not Supported)

BIOS shall provide proper utilities to support flash image update operations. In update progress, these utilities shall support the most frequently used scenarios listed as below.

- User can export current BIOS setting to a file.
- User can override BIOS SETUP settings with predefined configuration.
- Update partial image with user specified region of flash.
- Retain current setting while updating new BIOS.
- BIOS update utility shall support Command Line Interface (CLI) mode.

6.4.1.3 BIOS Update Requirement (PFR Supported)

BIOS update needs to be done through BMC. BMC provide proper utilities to support flash image update operations.

6.4.1.4 BIOS SUPPORTED UTILITIES

BIOS shall support to use proper utilities to achieve some functions. Listed the tools must be supported as below.

Need License Fee

- AMI AFU in Linux/EFI/Windows.
- AMI DMI in EFI/Windows.
- AMI SCE in Linux/EFI/Windows.
- AMI Change Logo in Windows.
- AMI AMISLP in Windows.

Free

- Tyan SMBIOS reading tool.
- Intel MEInfo/SpsInfo.

6.4.2. BIOS Features

6.4.2.1 Boot Logo

While BIOS booting, if there is a graphic display supported in the system, user can see the defined logo screen when enabling boot logo present feature. BIOS shall provide a selection option in SETUP for user to choose boot logo presented or not at the boot time. If this feature is enabled, it could be scale to full screen with sufficient image resolution and keep a while of seconds on screen.

If user set boot logo presented option to be disabled, BIOS shall switch to IBV native defined mode on display. The message must include platform information which is defined in section “3.2 Information Displayed during POST Time” to let user can properly to know system summary information.

Need to take care of logo resolution when it's in full screen scale. The MiTAC logo file and the minimum format requirement are defined as,

- BMP format
- 8bits color depths
- 800x600 pixels dimension

Consistency of Early POST and BIOS POST

In system with BMC implemented, the boot logo could be displayed from BMC first and then BIOS to deliver seamless full screen boot logo experience.

However, it shall consider three scenarios for consistency issues.

- When Quiet Boot is disabled. (Default)

During the period of BIOS POST, BIOS doesn't display brand logo.

- When Quiet Boot is enabled.

During the period of BIOS POST, BIOS displays brand logo. (e.g. TYAN Logo)

- Customized

When customized boot logo was installed, BIOS shall notify BMC that the BMC early post logo shall be enabled or disabled to have a great consistency display.

E.g. If BMC early post logo is brand logo but BIOS post logo was customized. In order to avoid inconsistency display between BIOS and BMC, BIOS shall automatically change Quiet Boot to “enabled” and notify BMC to disable its early post logo.

6.4.2.2 Information Displayed During POST Time

During BIOS POST, the text message will be showed on the host display or redirected to remote console connection for user to examine the summary information about the whole system without entering BIOS setup. The screen contents shall hold and keep around 1 second so as to view the information easily. The contents would cover below information.

- BIOS Version
- BIOS Banner String2
- BIOS Build Date
- BMC Version
- SDR Version
- IPMI IP Address
- Total Installed Memory Size
- Processor Type and Speed1
- USB Devices Information1,2
- POST Error Information3

Information of POST Error Code

In some failed conditions such as chassis cover was opened, BMC self-test was failed etc. The following descriptions could be displayed on screen.

- [BMC is not responding!!]

BIOS will display messaged when,

- KCS self-test result is 0x55.
- KCS I/O communicating result is 0xFF.
- [Chassis intrusion detected!!] (Optional)

- BIOS shall provide for user a SETUP option to enable/disable Chassis Intrusion detection function.
- BIOS shall conserve the intrusion state and send to BMC after BMC finished its initialization stage.
- [CMOS or NVRAM was Cleared!! Restored setup defaults!!]

This message indicates that the BIOS settings will return to default settings
BIOS will display message when,

- RTCRST is asserted.
- Battery is in low voltage or battery is removed.
- The BIOS NVRAM region is updated.
- (E.g. Performed AFU tool with /N parameter)
- After updating the BIOS, the NVRAM of the old BIOS version is not compatible with the new version.
- [WARNING: P0_MC0_DIM_CH_A0 has failed. It has been disabled.]

BIOS will display message when,

- The failure DIMM during POST time is detected.
- The system shall not hang and keep POST. The amounts of total memory size will exclude the failed memory module.

6.4.2.3 BIOS Hotkeys

Support to use specified single key or combination keys to enter BIOS Setup Menu, the default setting is or <F2> during boot time when prompt information is displayed on screen or remote console. The following instructional message would be displayed on the screen.

- 1Press or <F2> to enter setup.
- Press <F11> to prompt boot popup menu.
- Press <F12> to PXE Boot.

Furthermore, the prompt presented time on the screen would be a selection in BIOS setup menu. User can define a specified value with seconds scale to wait for input actions.

- The default setup prompt timeout is 1 seconds.

6.4.2.4 Remote Combination Hotkeys

BIOS provides serial redirection feature in various remote management console. Here is the combination key supported list for different kind of terminal setting.

Standard ANSI Sequences

Key or Function	Sequence
Right	<ESC> [, C
Left	<ESC> [, D
Up	<ESC> [, A
Down	<ESC> [, B
Home	<ESC> [, H
End	<ESC> [, K
F1	<ESC> O , P
F2	<ESC> O , Q
F3	<ESC> O , R
F4	<ESC> O , S
System Reset	<ESC>R<ESC>r<ESC>R

Putty VT100 Keypad	
Key or Function	Sequence
F1	<ESC> O , P
F2	<ESC> O , Q
F3	<ESC> O , R
F4	<ESC> O , S
F5	<ESC> O , T
F6	<ESC> O , U
F7	<ESC> O , V
F8	<ESC> O , W
F9	<ESC> O , X
F10	<ESC> O , Y
F11	<ESC> O , Z
F12	<ESC> O , [
Home	<ESC> [, 1, ~
Ins	<ESC> [, 2, ~
Del	<ESC> [, 3, ~
End	<ESC> [, 4, ~
Page Up	<ESC> [, 5, ~
Page Dn	<ESC> [, 6, ~

6.4.2.5 BIOS POST Code

The POST codes are composed of two or four HEX codes according to Intel or AMD platform. During the period of POST time, BIOS shall output these HEX codes to specified interfaces or media to let user realize the system POST status. E.g. BMC SoL.

POST Code for OPROM Entry and Exit

It's a special pair of BIOS post codes to indicate the entry and exit of option ROM. Two consecutive bytes are assigned for the entry and exit to avoid the same sequence used on another BIOS POST code. The definition is,

- Use [AA][C0] to indicate entering Option ROM.
- Use [BB][C1] to indicate exiting Option ROM.

6.4.2.6 BMC FRB2 Watch Dog Timer

The default setting of watch dog function is DISABLED and only be enabled when customer requests this feature. The default timeout setting is 6 minutes and then RESET the system when the timer expired. The watchdog timer is always disabled after POST.

6.4.2.7 Altitude

The default altitude setting of the platform location above the sea level is 300 meters with hexadecimal format '0x12C'. Be aware that the scale is meters and expressed in hex format.

6.4.2.8 PROTECTED PROCESSOR INVENTORY NUMBER

BIOS shall support PPIN and set default to [Unlock and Enable]. There are two ways for user to access PPIN.

BIOS shall map PPIN of each CPU0 and CPU1 to SMBIOS OEM Strings (Type 11) String 5 and String 6. User can view PPIN value from Linux' s "dmidecode" command.

6.4.2.9 START OF POST AND END OF POST INFORMATION

BIOS shall assert specified GPIO pin status to inform BMC about BIOS start of POST and end of POST events.

6.4.2.10 MANUFACTURE MODE

BMC will provide an IPMI command to enter manufacture mode. It is a special BIOS mode designed to decrease the time which systems spend on the assembly line.

This is done by skipping non-essential boot functions/tests and by prioritizing pre-defined boot devices ordering. These changes decrease the boot time significantly which allows more systems to complete the factory processes in less time.

BIOS shall replace AMI boot logo with a manufacture mode picture like below and set Quiet Mode to disabled to show up on the screen during BIOS POST Time to indicate user that the system is booting on manufacture status.



Prerequisites

For example, BIOS could implement below listed items,

- Set “Onboard LAN” to be the first bootable device, if it presents.
- System console redirection would be always enabled.
- Do not launch onboard storage and add-on card, if it appears in system.
- Launch onboard storage and add-on card, if it doesn’t appear in system.

6.4.2.11 WHEA ID

Beginning with Windows Server 2008 and Windows Vista SP1, when a hardware error occurs, the operating system creates an error record that describes the error condition and sends an event tracing for Windows (ETW) event that contains the error record to user mode. The format of the error record is based on the Common Platform Error Record as described in Appendix N of version 2.2 of the Unified Extensible Firmware Interface (UEFI) Specification. The following table describes each of the WHEA error-specific hardware error events that are defined for Windows Server 2008, Windows Vista SP1, and later versions of Windows.

Event	Event ID
WHEALOGR_DEFAULT_ERROR	1
WHEALOGR_DEFAULT_WARNING	2
WHEALOGR_DEFAULT_INFO	3
WHEALOGR_PCIE_ERROR	16
WHEALOGR_PCIE_WARNING	17
WHEALOGR_XPF_MCA_ERROR	18
WHEALOGR_XPF_MCA_WARNING	19
WHEALOGR_XPF_AMD64NB_MCA_ERROR	20
WHEALOGR_XPF_AMD64NB_MCA_WARNING	21
WHEALOGR_PLATFORM_MEMORY_ERROR	22
WHEALOGR_PLATFORM_MEMORY_WARNING	23
WHEALOGR_PCIXBUS_ERROR	24
WHEALOGR_PCIXBUS_WARNING	25
WHEALOGR_PCIXDEVICE_ERROR	26
WHEALOGR_PCIXDEVICE_WARNING	27
WHEALOGR_IPF_MCA_ERROR	38
WHEALOGR_IPF_MCA_WARNING	39
WHEALOGR_PCIE_NODEVICEID_ERROR	40
WHEALOGR_PCIE_NODEVICEID_WARNING	41
WHEALOGR_PCIXBUS_NODEVICEID_ERROR	42
WHEALOGR_PCIXBUS_NODEVICEID_WARNING	43
WHEALOGR_PCIXDEVICE_NODEVICEID_ERROR	44
WHEALOGR_PCIXDEVICE_NODEVICEID_WARNING	45
WHEALOGR_PLATFORM_MEMORY_NOTYPE_ERROR	46
WHEALOGR_PLATFORM_MEMORY_NOTYPE_WARNING	47

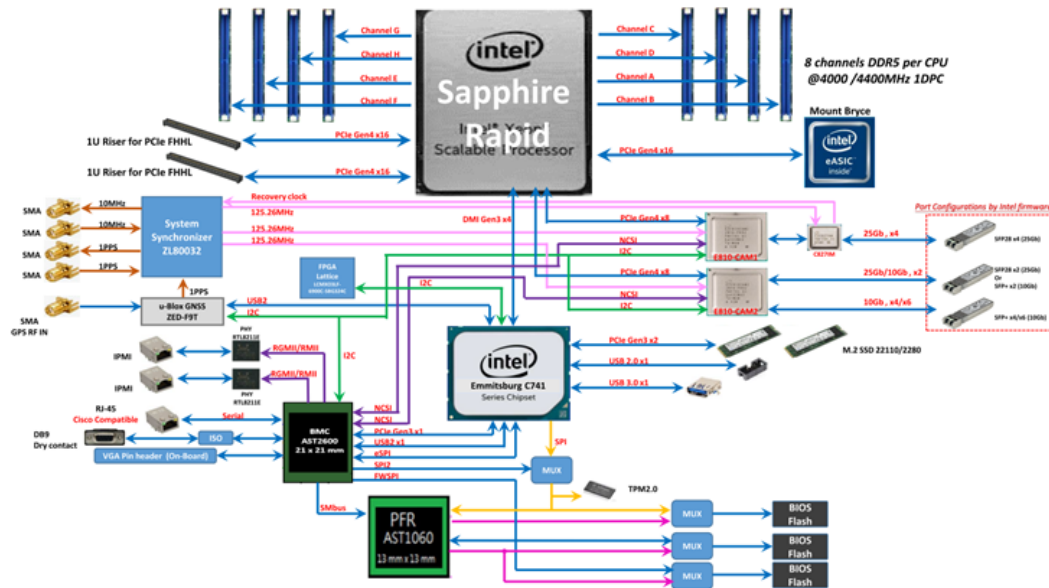
6.5 BMC

6.5.1 BMC Overview

This document specifies the BMC firmware features on Whitestone2 platform. The BMC firmware implements IPMI 2.0 based on AST2600 service processor. It performs all the BMC management tasks defined by IPMI 2.0 and, as a Service Processor, allows for remote monitoring using Serial Over LAN.

6.5.2 HW Block Diagram

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6.5.3 BMC Hardware Component

Component	Size	Usage
Aspeed AST2600	NA	It's a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms.
DDR4 SDRAM	512MB	BMC memory
SPI flash	128MB x2	BMC Flash part includes BMC FW, user configuration, SEL and SDR.
EEPROM	128KB	FRU information

6.5.4 AST2600 BMC GPIO Table

No.	Pin_Name	SCH_Pin_Name	Pin Function
GPIOA0	GPIOA0/MDC3/SCL11	SMB11_SMLINK2_STBY_LVC3_SCL_R	I2C
GPIOA1	GPIOA1/MDIO3/SDA11	SMB11_SMLINK2_STBY_LVC3_SDA_R	I2C
GPIOA2	GPIOA2/MDC4/SCL12	BMC_GPIOA2_R_SCL12	GPI => I2C
GPIOA3	GPIOA3/MDIO4/SDA12	BMC_GPIOA3_R_SDA12	GPI => I2C

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GPIOA4	GPIOA4/MAC1LINK/SCL13/SGPS2CK/SGPM2CK	GPS_SCL2	GPI => I2C
GPIOA5	GPIOA5/MAC2LINK/SDA13/SGPS2LD/SPGM2LD	GPS_SDA2	GPI => I2C
GPIOA6	GPIOA6/MAC3LINK/SCL14/SGPS2IO/SGPM2O	SMB14_CPU_PiROM_SCL_R	I2C
GPIOA7	GPIOA7/MAC4LINK/SDA14/SGPS2I1/SGPM2I	SMB14_CPU_PiROM_SDA_R	I2C
GPIOB0	GPIOB0/SALT1/LHAD0	FM_BMC_DBP_PRESENT_R_N	GPO => GPI
GPIOB1	GPIOB1/SALT2/LHAD1	FM_BOARD_REV_ID0	GPI
GPIOB2	GPIOB2/SALT3/LHAD2	FM_CPU1_PROCHOT_LVT3_BMC_N	GPI
GPIOB3	GPIOB3/SALT4/LHAD3	DBP_SYSPWROK_R	TBC => GPI
GPIOB4	GPIOB4/MDC2/LHCLK	RST_BMC_SMBUS_MUX_NX1	GPO => GPI
GPIOB5	GPIOB5/MDIO2/LHFRAME#	TP_FM_BMC_NMI_N	GPI
GPIOB6	GPIOB6/TXD4/LHSIRQ#	FM_BMC_BMCINIT_R	GPO
GPIOB7	GPIOB7/RXD4/LHRST#	BMC_SYS_READY	GPO, H
GPIOC0	RGMII3TXCK/RMII3RCLK0/GPIOC0	VSP_BMC_O_HBLED_R	GPO
GPIOC1	RGMII3TXCTL/RMII3TXEN/GPIOC1	RMII_BMC_I350_TX_EN_R	RMII, MAC3
GPIOC2	RGMII3TXD0/RMII3TXD0/GPIOC2	RMII_BMC_I350_TXD0_R	RMII, MAC3
GPIOC3	RGMII3TXD1/RMII3TXD1/GPIOC3	RMII_BMC_I350_TXD1_R	RMII, MAC3
GPIOC4	RGMII3TXD2/GPIOC4	MOUNTBRYCE_TEMP_CRITN	GPI
GPIOC5	RGMII3TXD3/GPIOC5	MOUNTBRYCE__TEMP_ALERT_N	GPI
GPIOC6	RGMII3RXCK/RMII3RCLKI/GPIOC6	CLK_50M_BMC_RMII_3	RMII, MAC3
GPIOC7	RGMII3RXCTL/GPIOC7	PD_BMC_GPIOC7	GPI
GPIOD0	RGMII3RXD0/RMII3RXD0/GPIOD0	RMII_BMC_I350_RXD0	RMII, MAC3
GPIOD1	RGMII3RXD1/RMII3RXD1/GPIOD1	RMII_BMC_I350_RXD1	RMII, MAC3
GPIOD2	RGMII3RXD2/RMII3CRSDV/GPIOD2	RMII_BMC_I350_CRSDV	RMII, MAC3
GPIOD3	RGMII3RXD3/RMII3RXER/GPIOD3	PD_RMII_BMC_I350_RXER	GPI => RMII, MAC3

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GPIOD4	RGMII4TXCK/RMII4RCLKO/NCTS3/GPIOD4	FM_CPU_ERR0_LVT3_N	GPI => RMII, MAC4
GPIOD5	RGMII4TXCTL/RMII4TXEN/ND3CD3/GPIOD5	RMII_BMC_TX_EN_R	GPI
GPIOD6	RGMII4TXD0/RMII4TXD0/ND3SR3/GPIOD6	RMII_BMC_R_TXD<0>	GPI
GPIOD7	RGMII4TXD1/RMII4TXD1/NRI3/GPIOD7	RMII_BMC_R_TXD<1>	GPI
GPIOE0	RGMII4TXD2/NDTR3/GPIOE0	M2_SSD1_PRSENT_N	GPI
GPIOE1	RGMII4TXD3/NRTS3/GPIOE1	M2_SSD2_PRSENT_N	GPI
GPIOE2	RGMII4RXCK/RMII4RCLKI/NCTS4/GPIOE2	CLK_50M_BMC_RMII_4	GPI
GPIOE3	RGMII4RXCTL/ND3CD4/GPIOE3	PD_BMC_GPIOE3	GPI
GPIOE4	RGMII4RXD0/RMII4RXD0/ND3SR4/GPIOE4	RMII_BMC_RXD<0>	GPI
GPIOE5	RGMII4RXD1/RMII4RXD1/NRI4/GPIOE5	RMII_BMC_RXD<1>	GPI
GPIOE6	RGMII4RXD2/RMII4CRSDV/NDTR4/GPIOE6	RMII_BMC_CRSDV	GPI
GPIOE7	RGMII4RXD3/RMII4RXER/NRTS4/GPIOE7	PD_RMII_BMC_RX_ER	GPI
GPIOF0	GPIOF0/SD1CLK/PWM8	GND	GPI
GPIOF1	GPIOF1/SD1CMD/PWM9	GND	GPI
GPIOF2	GPIOF2/SD1DAT0/PWM10	GND	GPI
GPIOF3	GPIOF3/SD1DAT1/PWM11	GND	GPI
GPIOF4	GPIOF4/SD1DAT2/PWM12	GND	GPI
GPIOF5	GPIOF5/SD1DAT3/PWM13	GND	GPI
GPIOF6	GPIOF6/SD1CD#/PWM14	GND	GPI
GPIOF7	GPIOF7/SD1WP#/PWM15	GND	GPI
GPIOG0	GPIOG0/TXD6/SD2CLK/SALT9	MAIN_I2C_BUS_SEL1	GPO
GPIOG1	GPIOG1/RXD6/SD2CMD/SALT10	FP_LED_STATUS_GREEN	GPO
GPIOG2	GPIOG2/TXD7/SD2DAT0/SALT11	FP_LED_STATUS_BLUE	GPO
GPIOG3	GPIOG3/RXD7/SD2DAT1/SALT12	FP_LED_STATUS_AMBER	GPO
GPIOG4	GPIOG4/TXD8/SD2DAT2/SALT13	TP_FP_ID_BTN_N	GPO => GPI

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GPIOG5	GPIOG5/RXD8/SD2DAT3/SALT14	PWRGD_P12V_0_SW_R	GPI
GPIOG6	GPIOG6/TXD9/SD2CD#/SALT15	FM_BMC_CPU_PWR_DEBUG_R_N	TBC => GPI
GPIOG7	GPIOG7/RXD9/SD2WP#/SALT16	DBP_PRESENT_R2_N	TBC => GPI
GPIOH0	GPIOH0/SGPM1CK	SGPIO_BMC_CLK_R	SGPIO
GPIOH1	GPIOH1/SGPM1LD	SGPIO_BMC_LD_R_N	SGPIO
GPIOH2	GPIOH2/SGPM1O	SGPIO_BMC_DOUT_R	SGPIO
GPIOH3	GPIOH3/SGPM1I	SGPIO_BMC_DIN_R	SGPIO
GPIOH4	GPIOH4/SGPS1CK/SCL15	RST_PLTRST_BMC_N	GPI
GPIOH5	GPIOH5/SGPS1LD/SDA15	FM_CPU_MSMTI_CATERR_LVT3_N	GPI
GPIOH6	GPIOH6/SGPS1IO/SCL16	FM_PCH_BMC_THERMTRIP_N	GPI
GPIOH7	GPIOH7/SGPS1I1/SDA16	FM_THROTTLE_R2_N	GPI
GPIOI0	GPIOI0/MNTRST2/TXD12	JTAG_BMC_NTRST_R_N	JTAG
GPIOI1	GPIOI1/MTDI2/RXD12	JTAG_BMC_TDI_R	JTAG
GPIOI2	GPIOI2/MTCK2/TXD13	JTAG_BMC_TCK_R	JTAG
GPIOI3	GPIOI3/MTMS2/RXD13	JTAG_BMC_TMS_R	JTAG
GPIOI4	GPIOI4/MTDO2	JTAG_BMC_TDO	JTAG
GPIOI5	GPIOI5/SIOPBO#	FM_BMC_PWRBTN_OUT_R_N	GPO or SIOPBO# => ACPI
GPIOI6	GPIOI6/SIOPBI#	FM_BMC_PWR_BTN_N	GPI or SIOPBI# => ACPI
GPIOI7	GPIOI7/SIOSCI#	FM_BMC_PCH_SCI_LPC_R_N	GPI => LPC
GPIOJ0	GPIOJ0/SCL1/HVI3C3SCL	SMB1_SLED_BUF_BMC_SCL_R	I2C
GPIOJ1	GPIOJ1/SDA1/HVI3C3SDA	SMB1_SLED_BUF_BMC_SDA_R	I2C
GPIOJ2	GPIOJ2/SCL2/HVI3C4SCL	SMB2_CVL_STBY_LVC3_SCL_R	I2C
GPIOJ3	GPIOJ3/SDA2/HVI3C4SDA	SMB2_CVL_STBY_LVC3_SDA_R	I2C

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GPIOK4	GPIOK4/SCL3/HVI3C5SCL	SMB3_RISER_STBY_LVC3_SCL_R	I2C
GPIOK5	GPIOK5/SDA3/HVI3C5SDA	SMB3_RISER_STBY_LVC3_SDA_R	I2C
GPIOK6	GPIOK6/SCL4/HVI3C6SCL	SMB4_HOST_STBY_BMC_LVC3_SCL_R	I2C
GPIOK7	GPIOK7/SDA4/HVI3C6SDA	SMB4_HOST_STBY_BMC_LVC3_SDA_R	I2C
GPIOK0	GPIOK0/SCL5	SMB5_TIMESYNC_SCL_R	I2C
GPIOK1	GPIOK1/SDA5	SMB5_TIMESYNC_SDA_R	I2C
GPIOK2	GPIOK2/SCL6	SMB6_SMLINK0_STBY_LVC3_SCL_R	I2C
GPIOK3	GPIOK3/SDA6	SMB6_SMLINK0_STBY_LVC3_SDA_R	I2C
GPIOK4	GPIOK4/SCL7	SMB7_TEMPSENSOR_STBY_LVC3_SCL_R	I2C
GPIOK5	GPIOK5/SDA7	SMB7_TEMPSENSOR_STBY_LVC3_SDA_R	I2C
GPIOK6	GPIOK6/SCL8	SMB8_PMBUS_SML1_STBY_LVC3_SCL_R	I2C
GPIOK7	GPIOK7/SDA8	SMB8_PMBUS_SML1_STBY_LVC3_SDA_R	I2C
GPIOL0	GPIOL0/SCL9	SMB9_HSBP_STBY_LVC3_SCL_R	I2C
GPIOL1	GPIOL1/SDA9	SMB9_HSBP_STBY_LVC3_SDA_R	I2C
GPIOL2	GPIOL2/SCL10	SMB10_BMC_SPD_ACCESS_STBY_LVC_3_SCL	I2C
GPIOL3	GPIOL3/SDA10	SMB10_BMC_SPD_ACCESS_STBY_LVC_3_SDA	I2C
GPIOL4	GPIOL4/TXD3	DBP_CPU_PREQ_R_N	TBC => GPI
GPIOL5	GPIOL5/RXD3	FM_JTAG_TCK_MUX_SEL_R	GPO
GPIOL6	GPIOL6/VGAHS	V_BMC_GFX_HSYNC	VGA
GPIOL7	GPIOL7/VGAVS	V_BMC_GFX_VSYNC	VGA
GPIOM0	GPIOM0/NCTS1	VSP_BMC_COM1_CTS	UART
GPIOM1	GPIOM1/NDCD1	VSP_BMC_COM1_DCD	UART
GPIOM2	GPIOM2/NDSR1	VSP_BMC_COM1_DSR	UART
GPIOM3	GPIOM3/NRI1	VSP_BMC_COM1_NRI	UART

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GPION4	GPION4/NDTR1	VSP_BMC_COM1_DTR	UART
GPION5	GPION5/NRTS1	VSP_BMC_COM1_RTS	UART
GPION6	GPION6/TXD1	VSP_BMC_COM1_TXD	UART
GPION7	GPION7/RXD1	VSP_BMC_COM1_RXD	UART
GPION0	GPION0/NCTS2	FM_BOARD_SKU_ID5	GPI
GPION1	GPION1/NDCD2	FM_BOARD_SKU_ID4	GPI
GPION2	GPION2/NDSR2	FM_BOARD_SKU_ID3	GPI
GPION3	GPION3/NRI2	FM_BOARD_SKU_ID2	GPI
GPION4	GPION4/NDTR2	FM_BOARD_SKU_ID1	GPI
GPION5	GPION5/NRTS2	FM_BOARD_SKU_ID0	GPI
GPION6	GPION6/TXD2	FM_CPU_ERR1_LVT3_N	GPI
GPION7	GPION7/RXD2	TP_BMC_GPION7	GPO => GPI
GPIO00	GPIO00/PWM0	FAN_BMC_PWM0	PWM
GPIO01	GPIO01/PWM1	FAN_BMC_PWM1	PWM
GPIO02	GPIO02/PWM2	FAN_BMC_PWM2	PWM
GPIO03	GPIO03/PWM3	FAN_BMC_PWM3	PWM
GPIO04	GPIO04/PWM4	FM_PCIE_SLOT3_PRSENT_N	GPI
GPIO05	GPIO05/PWM5	FM_PCIE_SLOT2_PRSENT_N	GPI
GPIO06	GPIO06/PWM6	FM_PCIE_SLOT1_PRSENT_N	GPI
GPIO07	GPIO07/PWM7	TP_GPIO07	GPI
GIOP0	GIOP0/PWM8/THRUIN0	FP_BMC_RST_BTN_N	THRUIN0
GIOP1	GIOP1/PWM9/THRUOUT0	RST_BMC_RSTBTN_OUT_R_N	THRUOUT0
GIOP2	GIOP2/PWM10/THRUIN1	FP_BMC_PWR_BTN_R_N	THRUIN1
GIOP3	GIOP3/PWM11/THRUOUT1	FM_BMC_PWR_BTN_N	THRUOUT1

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GPIOP4	GPIOP4/PWM12/THRUIN2	TP_GPIOP4	GPO => THRIN
GPIOP5	GPIOP5/PWM13/THRUOUT2	TP_GPIOP5	GPI => THROUT
GPIOP6	GPIOP6/PWM14	TP_GPIOP6	GPI
GPIOP7	GPIOP7/HBLED#/PWM15	LED_BMC_HB_LED_N	HBLED#
GPIOQ0	GPIOQ0/TACH0	FAN_BMC_TACH0	TACH
GPIOQ1	GPIOQ1/TACH1	FAN_BMC_TACH1	TACH
GPIOQ2	GPIOQ2/TACH2	FAN_BMC_TACH2	TACH
GPIOQ3	GPIOQ3/TACH3	FAN_BMC_TACH3	TACH
GPIOQ4	GPIOQ4/TACH4	FAN_BMC_TACH4	TACH
GPIOQ5	GPIOQ5/TACH5	FAN_BMC_TACH5	TACH
GPIOQ6	GPIOQ6/TACH6	FAN_BMC_TACH6	TACH
GPIOQ7	GPIOQ7/TACH7	FAN_BMC_TACH7	TACH
GPIOR0	GPIOR0/TACH8	NI	GPI
GPIOR1	GPIOR1/TACH9	FM_PASSWORD_CLEAR_R_N	GPO
GPIOR2	GPIOR2/TACH10	FM_CPU1_MEMHOT_OUT_LV3_N	GPI
GPIOR3	GPIOR3/TACH11	NI	GPI
GPIOR4	GPIOR4/TACH12	NI	GPI
GPIOR5	GPIOR5/TACH13	NI	GPI
GPIOR6	GPIOR6/TACH14	IRQ_SMB_M2_ALERT_NX1	GPI
GPIOR7	GPIOR7/TACH15	IRQ_NMI_EVENT_R_N	GPI
GPIOS0	GPIOS0/MDC1	IRQ_BMC_PCH_NMI_R	GPI => GPO
GPIOS1	GPIOS1/MDIO1	FM_PCIE_SLOT4_PRSENT_N	GPI
GPIOS2	GPIOS2/PEWAKE#	PU_BMC_PEWAKE_N	GPO => GPI
GPIOS3	GPIOS3/OSCCLK	RST_RSMRST_BMC_N	GPI

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GPIOS4	GPIOS4/TXD10	FM_FORCE_ADR_N	GPO => GPI
GPIOS5	GPIOS5/RXD10	A_P3V_BAT_SCALED_EN	GPO
GPIOS6	GPIOS6/TXD11	FM_REMOTE_DEBUG_EN_DET_R	GPI
GPIOS7	GPIOS7/RXD11	FM_HSC_TIMER_EXP_N	GPI
GPIOT0	ADC0/GPIT0	A_P12V_STBY_SCALED	ADC
GPIOT1	ADC1/GPIT1	A_P5V_AUX_SCALED	ADC
GPIOT2	ADC2/GPIT2	A_P3V3_AUX_SCALED	ADC
GPIOT3	ADC3/GPIT3	A_P12V_RISER_SCALED	ADC
GPIOT4	ADC4/GPIT4	A_P5V_SCALED	ADC
GPIOT5	ADC5/GPIT5	A_P3V3_SCALED	ADC
GPIOT6	ADC6/GPIT6	A_P1V8_PCH_AUX_SCALED	ADC
GPIOT7	ADC7/GPIT7	A_P1V05_PCH_AUX_SCALED	ADC
GPIOU0	ADC8/GPIU0/SALT9	A_PVNN_PCH_AUX_SCALED	ADC
GPIOU1	ADC9/GPIU1/SALT10	A_PVDDQ_CPU1_ABCD_SCALED	ADC
GPIOU2	ADC10/GPIU2/SALT11	A_PVDDQ_CPU1_EFGH_SCALED	ADC
GPIOU3	ADC11/GPIU3/SALT12	A_P1V8_CPU1_SCALED	ADC
GPIOU4	ADC12/GPIU4/SALT13	A_PVCCIO_CPU1_SCALED	ADC
GPIOU5	ADC13/GPIU5/SALT14	A_PVCCIN_CPU1_SCALED	ADC
GPIOU6	ADC14/GPIU6/SALT15	A_PVCCANA_CPU1_SCALED	ADC
GPIOU7	ADC15/GPIU7/SALT16	A_P3V_BAT_SCALED	ADC
GPIOV0	GPIOV0/SIOS3#	FM_SLPS3_R_N	GPI => ACPI
GPIOV1	GPIOV1/SIOS5#	FM_SLPS4_R_N	GPI => ACPI
GPIOV2	GPIOV2/SIOPWREQ#	TP_BMC_SIO_PWREQ_N	GPO => ACPI
GPIOV3	GPIOV3/SIOONCTRL#	FM_BMC_ONCTL_R_N	GPO => ACPI

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GPIOV4	GPIOV4/SIOPWRGD	PWRGD_CPU1_LVC3_R	GPI => ACPI
GPIOV5	GPIOV5/LPCPD#/LHPD#	IRQ_OC_DETECT_N	GPI
GPIOV6	GPIOV6/LPCPME#	FM_CPU_ERR2_LVT3_N	GPI
GPIOV7	GPIOV7/LPCSMI#	IRQ_BMC_PCH_SMI_LPC_R_N	GPI => GPO
GPIW0	GPIOW0/LAD0/ESPID0	ESPI_IO0_BMC_R	ESPI
GPIW1	GPIOW1/LAD1/ESPID1	ESPI_IO1_BMC_R	ESPI
GPIW2	GPIOW2/LAD2/ESPID2	ESPI_IO2_BMC_R	ESPI
GPIW3	GPIOW3/LAD3/ESPID3	ESPI_IO3_BMC_R	ESPI
GPIW4	GPIOW4/LCLK/ESPICK	ESPI_CLK_BMC_R	ESPI
GPIW5	GPIOW5/LFRAME#/ESPICS#	ESPI_CS0_BMC_R_N	ESPI
GPIW6	GPIOW6/LSIRQ#/ESPIALT#	IRQ_ESPI_ALERT0_BMC_N	ESPI
GPIW7	GPIOW7/LPCRST#/ESPIRST#	RST_ESPI_RESET_BMC_N	ESPI
GPIX0	GPIOX0/SPI2CS0#	FM_EDSFF0_PRSNT_N	GPI
GPIX1	GPIOX1/SPI2CS1#	IRQ_SMI_ACTIVE_BMC_N	GPI
GPIX2	GPIOX2/SPI2CS2#	FM_BIOS_POST_CMPLT_R_N	GPI
GPIX3	GPIOX3/SPI2CK	NI	GPI
GPIX4	GPIOX4/SPI2MOSI	NI	GPI
GPIX5	GPIOX5/SPI2MISO	NI	GPI
GPIX6	GPIOX6/SPI2DQ2/TXD12	FM_BIOS_POST_START_R_N	GPI
GPIX7	GPIOX7/SPI2DQ3/RXD12	FM_BIOS_ENTER_SETUP_R_N	GPI
GPIYO0	GPIYO0/SALT5/WDTRST1#	H_BMC_PRDY_R_N	TBC => GPI
GPIYO1	GPIYO1/SALT6/WDTRST2#	IRQ_SML0_ALERT_BMC_N	GPI
GPIYO2	GPIYO2/SALT7/WDTRST3#	TP_SMB_HOST_STBY_BMC_LVC3_RST_N	GPI
GPIYO3	GPIYO3/SALT8/WDTRST4#	IRQ_SML1_PMBUS_BMC_ALERT_N	GPI

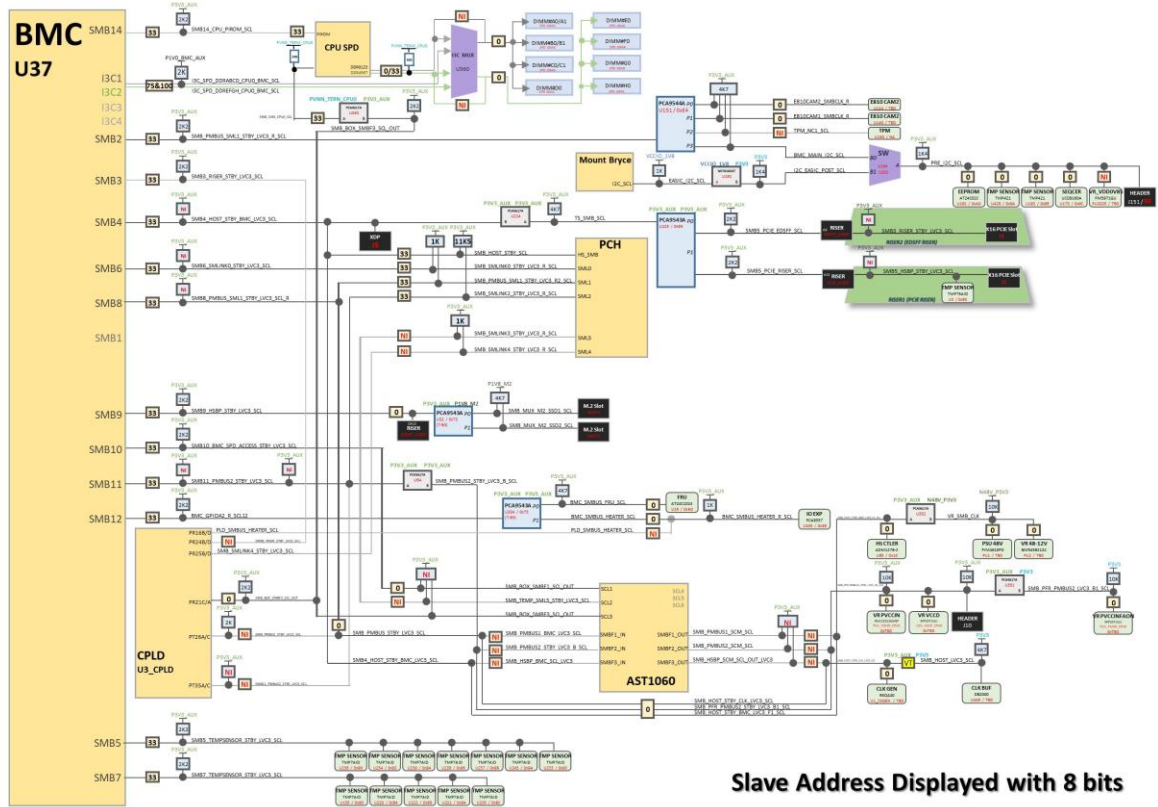
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GPIOY4	GPIOY4/FWSPIDQ2	SPI_BMC_BOOT_IO2_R	SPI
GPIOY5	GPIOY5/FWSPIDQ3	SPI_BMC_BOOT_IO3_R	SPI
GPIOY6	GPIOY6/FWSPiABR	PU_SPI_BMC_BOOT_ABR	GPO
GPIOY7	GPIOY7/FWSPiWP#	PU_SPI_BMC_BOOT_WP_N	GPO
GPIOZ0	GPIOZ0/SPI1CS1#	PWRGD_SYS_PWROK_BMC	GPO
GPIOZ1	GPIOZ1/SPI1ABR	FM_BOARD_REV_ID2	GPI
GPIOZ2	GPIOZ2/SPI1WP#	FM_BOARD_REV_ID1	GPI
GPIOZ3	GPIOZ3/SPI1CK	PD_BMC_GPIOZ3	GPI
GPIOZ4	GPIOZ4/SPI1MOSI	PD_BMC_GPIOZ4	GPI
GPIOZ5	GPIOZ5/SPI1MISO	PD_BMC_GPIOZ5	GPI
GPIOZ6	GPIOZ6/SPI1DQ2/TXD13	TOD_SERIAL_PORT_RXD1	UART
GPIOZ7	GPIOZ7/SPI1DQ3/RXD13	TOD_SERIAL_PORT_TXD1	UART
GPIO18A0	RGMII1TXCK/RMII1RCLKO/GPIO18A0	GND	GPI
GPIO18A1	RGMII1TXCTL/RMII1TXEN/GPIO18A1	GND	GPI
GPIO18A2	RGMII1TXD0/RMII1TXD0/GPIO18A2	GND	GPI
GPIO18A3	RGMII1TXD1/RMII1TXD1/GPIO18A3	GND	GPI
GPIO18A4	RGMII1TXD2/GPIO18A4	GND	GPI
GPIO18A5	RGMII1TXD3/GPIO18A5	GND	GPI
GPIO18A6	RGMII1RXCK/RMII1RCLKI/GPIO18A6	GND	GPI
GPIO18A7	RGMII1RXCTL/GPIO18A7	GND	GPI
GPIO18B0	RGMII1RXD0/RMII1RXD0/GPIO18B0	GND	GPI
GPIO18B1	RGMII1RXD1/RMII1RXD1/GPIO18B1	GND	GPI
GPIO18B2	RGMII1RXD2/RMII1CRSDV/GPIO18B2	GND	GPI
GPIO18B3	RGMII1RXD3/RMII1RXER/GPIO18B3	GND	GPI
GPIO18B4	RGMII2TXCK/RMII2RCLKO/GPIO18B4	GND	GPI
GPIO18B5	RGMII2TXCTL/RMII2TXEN/GPIO18B5	GND	GPI

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GPIO18B6	RGMII2TXD0/RMII2TXD0/GPIO18B6	GND	GPI
GPIO18B7	RGMII2TXD1/RMII2TXD1/GPIOU18B7	GND	GPI
GPIO18C0	RGMII2TXD2/GPIO18C0	GND	GPI
GPIO18C1	RGMII2TXD3/GPIO18C1	GND	GPI
GPIO18C2	RGMII2RXCK/RMII2RCLKI/GPIO18C2	GND	GPI
GPIO18C3	RGMII2RXCTL/GPIO18C3	GND	GPI
GPIO18C4	RGMII2RXD0/RMII2RXD0/GPIO18C4	GND	GPI
GPIO18C5	RGMII2RXD1/RMII2RXD1/GPIO18C5	GND	GPI
GPIO18C6	RGMII2RXD2/RMII2CRSDV/GPIO18C6	GND	GPI
GPIO18C7	RGMII2RXD3/RMII2RXER/GPIO18C7	GND	GPI
GPIO18D0	GPIO18D0/EMMCCLK	BMC_EMMC_CLK	EMMC
GPIO18D1	GPIO18D1/EMMCCMD	BMC_EMMC_CMD	EMMC
GPIO18D2	GPIO18D2/EMMCDAT0	BMC_EMMC_DATA<0>	EMMC
GPIO18D3	GPIO18D3/EMMCDAT1	BMC_EMMC_DATA<1>	EMMC
GPIO18D4	GPIO18D4/EMMCDAT2	BMC_EMMC_DATA<2>	EMMC
GPIO18D5	GPIO18D5/EMMCDAT3	BMC_EMMC_DATA<3>	EMMC
GPIO18D6	GPIO18D6/EMMCDD#	BMC_EMMC_CD_N	EMMC
GPIO18D7	GPIO18D7/EMMCWP#	BMC_EMMC_WP_N	EMMC
GPIO18E0	GPIO18E0/EMMCDAT4/VBCS#	BMC_EMMC_DATA<4>	EMMC
GPIO18E1	GPIO18E1/EMMCDAT5/VBCK	BMC_EMMC_DATA<5>	EMMC
GPIO18E2	GPIO18E2/EMMCDAT6/VBMOSI	BMC_EMMC_DATA<6>	EMMC
GPIO18E3	GPIO18E3/EMMCDAT7/VBMISO	BMC_EMMC_DATA<7>	EMMC

6.5.5 BMC I2C Definition Table



6.5.6 BMC Main Features

Feature		Description
IPMI 2.0 Standard Features	System Interface support	- KCS - LAN(RMCP/RMCP+)
	Text Console Redirection: SOL	Support in IPMI stack for SOL to remotely access BIOS and text console before OS booting.
	IPMI 2.0 based Management	- BMC stack with a full IPMI 2.0 implementation - Optional commands supported(refer to section 4.1.1) - OEM commands supported(refer to section 4.1.2 and section 5)
	System Management	- System health monitoring. - System Power management - Fan speed monitor and control

Feature		Description
	Event Log and Alerting	- Read Log events - Sensor readings - SNMP traps
	Remote Server Power Control	- Server's power status report - Support for remotely power-cycle, power-down, power-up, reset the server
	Watchdog Timer Support	Watchdog function that can generate interrupt or reset after zero count down
	Sophisticated User Management	- IPMI based user management - Multiple user permission level - Extended security algorithms and cipher suites support
OEM features	Management Network Interface	BMC should has Shared-NIC uses RMII/NCSI interface for Out-of-Band access.
	Port 80 POST	- BMC to support port 80 POST code display to drive 8 bit HEX GPIO and SOL - BMC should have access to POST code and record up to 256 POST codes.
	FSC in BMC (Not ready)	- BMC should support FSC in both PID and step mode. BMC should support both In-Band and Out-of-Band FSC configuration update; updates should take effect immediately without reboot required. BMC should support FAN boost during fan failure. - Default fan PWM setting is 100% when power on by HW.
	Control Power and System Identification LED (Power LED no define)	
	YAFU BMC/BIOS remote update(Not ready)	
	BMC web GUI	

6.5.7 BMC Main Features

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	Feature	Description
IPMI 2.0 Standard Features	System Interface support	• KCS • LAN(RMCP/RMCP+)
	Text Console Redirection: SOL	• Support in IPMI stack for SOL to remotely access BIOS and text console before OS booting.
	IPMI 2.0 based Management	• BMC stack with a full IPMI 2.0 implementation • Optional commands supported(refer to section 4.1.1) • OEM commands supported(refer to section 4.1.2 and section 5)
	System Management	• System health monitoring. • System Power management • Fan speed monitor and control
	Event Log and Alerting	• Read Log events • Sensor readings • SNMP traps
	Remote Server Power Control	• Server's power status report • Support for remotely power-cycle, power-down, power-up, reset the server
	Watchdog Timer Support	• Watchdog function that can generate interrupt or reset after zero count down
	Sophisticated User Management	• IPMI based user management • Multiple user permission level • Extended security algorithms and cipher suites support
OEM features	Management Network Interface	• BMC should has Shared-NIC uses RMII/NCSI interface for Out-of-Band access.
	Port 80 POST	• BMC to support port 80 POST code display to drive 8 bit HEX GPIO and SOL • BMC should have access to POST code and record up to 256 POST codes.
	FSC in BMC (Not ready)	• BMC should support FSC in both PID and step mode. BMC should support both In-Band and Out-of-Band FSC configuration update; updates should take effect immediately without reboot required. BMC should support FAN boost during fan failure. • Default fan PWM setting is 100% when power on by HW.
	Control Power and System Identification LED (Power LED no define)	•
	YAFU BMC/BIOS remote update(Not ready)	•
	BMC web GUI	•

6.5.8 Messaging interfaces

The BMC messaging interfaces comply with the IPMI 2.0 specification. The following interfaces are supported.

- Keyboard Controller Style (KCS) Host Interface – Chapter 9 of the IPMI 2.0 specification.
- LAN Interface – Chapter 13 of the IPMI 2.0 specification.
- IPMI Serial/Modem Interface – Chapter 14 of the IPMI 2.0 specification.

Channel	Interface
0h	IPMB
1h	RMII Sideband NIC
3h	KCS
Fh	Host/SMS

6.5.9 Text console redirection – SOL (Serial over LAN)

Whitestone2 BMC FW provides the support for text console redirection (SOL) to remotely access BIOS setup or text consoles that are available on the serial console of host system.

The firmware includes support for IPMI based SOL where the standard IPMI client like IPMITOOL can be used to establish a SOL session with the service processor.

The SOL default baud rate is setup by BMC flash part as 115200. BMC and uEFI will synch at the system booting POST stage.

6.5.10 Commands Support

Whitestone2 BMC FW provides a fully-compliant IPMI 2.0 based management of the service processor.

All the mandatory requirements and commands in IPMI 2.0 are supported

IPMI commands support

In addition to the mandatory criteria in IPMI 2.0 specification, Whitestone2 BMC FW also supports many optional commands.

The following is a list of commands that currently support to the Whitestone2 BMC firmware.

IPMI Global Commands

IPMI Global Commands
Get Device ID
Cold Reset
Warm Reset

Get Self Test Results
Set ACPI Power State
Get ACPI Power State
Get Device GUID
Get NetFn Support
Get Command Support
Get Command Sub-function Support
Get Configurable
Get Configurable Command Sub-functions

BMC Watchdog Timer Commands

BMC Watchdog Timer Commands
Reset Watchdog Timer
Set Watchdog Timer
Get Watchdog Timer

IPMI Messaging Support Commands

IPMI Messaging Support Commands
Set BMC Global Enables
Get BMC Global Enables
Clear Message Flags
Get Message Flags
Enable Message Channel Receive
Get Message
Send Message
Read Event Message Buffer
Get System GUID
Get Channel Authentication Capabilities
Get Session Challenge
Activate Session
Set Session Privilege Level
Close Session
Get Session Info
Get AuthCode
Set Channel Access
Get Channel Access
Get Channel Info
Set Channel Security Keys
Set User Access
Get User Access
Set User Name
Get User Name
Set User Password
Master Write-Read
Get Channel Cipher Suites
Get System Interface Capabilities
Set System Info Parameters
Get System Info Parameters

RMCP+ Support and Payload Commands

RMCP+ Support and Payload Commands
Activate Payload
Deactivate Payload
Get Payload Activation Status
Get Payload Instance Info
Set User Payload Access
Get User Payload Access
Get Channel Payload Support
Get Channel Payload Version
Get Channel OEM Payload Info
Suspend/Resume Payload Encryption

Chassis Device Commands

Chassis Device Commands
Get Chassis Capabilities
Get Chassis Status
Chassis Control
Chassis Identify
Set Chassis Capabilities
Set Power Restore Policy – disable by default
Get System Restart Cause
Set System Boot Options
Get System Boot Options
Get POH Counter

Event Commands

Event Commands
Set Event Receiver
Get Event Receiver
Platform Event

PEF and Alerting Commands

PEF and Alerting Commands
Get PEF Capabilities
Arm PEF Postpone Timer
Set PEF Configuration Parameters
Get PEF Configuration Parameters
Set Last Processed Event ID
Get Last Processed Event ID
Alert Immediate
PET Acknowledge

Sensor Device Commands

Sensor Device Commands
Get Device SDR Info
Get Sensor Reading Factors
Set Sensor Hysteresis
Get Sensor Hysteresis
Set Sensor Threshold
Get Sensor Threshold
Set Sensor Event Enable
Get Sensor Event Enable
Re-arm Sensor Events
Get Sensor Event Status
Get Sensor Reading
Set Sensor Reading And Event Status
Set Sensor Type

FRU Inventory Area Info

FRU Device Commands
Get FRU Inventory Area Info
Read FRU Data
Write FRU Data

SDR Repository Device Commands

SDR Repository Device Commands
Get SDR Repository Info
Get SDR Repository Allocation Info
Reserve SDR Repository
Get SDR
Add SDR
Partial Add SDR
Delete SDR
Clear SDR Repository
Get SDR Repository Time
Enter SDR Repository Update Mode
Exit SDR Repository Update Mode
Run Initialization Agent

SEL Device Commands

SEL Device Commands
Get SEL Info
Get SEL Allocation Info
Reserve SEL
Get SEL Entry
Add SEL Entry
Partial Add SEL Entry
Clear SEL
Get SEL Time
Set SEL Time
Get SEL Time UTC Offset
Set SEL Time UTC Offset

IPMI LAN Commands

IPMI LAN Commands
Set LAN Configuration Parameters
Get LAN Configuration Parameters
Suspend BMC ARPs

SOL Commands

SOL Commands
Set Serial/Modem Configuration
Get Serial/Modem Configuration
SOL Activating
Set SOL Configuration Parameters
Get SOL Configuration Parameters

OEM command support

Except the Standard and optional commands, provide the system specific OEM commands that dedicated for Whitestone2 system, below are all the OEM commands that available for Whitestone2.

The following is a list of OEM commands that planning to support on the Whitestone2 BMC firmware.

Table 0-1: OEM Commands Synopsis

Command Set	Sub command	NetFn	CMD Code
FSC Command Set	Enter FSC Update Mode Command	30h	61h
	Exit FSC Update Mode Command	30h	62h
	Read FSC Profile Header Command	30h	63h
	Write FSC Profile Header Command	30h	64h
	Read FSC Profile Command	30h	65h
	Write FSC Profile Command	30h	66h
	Read Zone Control Setting Command	30h	67h
	Write Zone Control Setting Command	30h	68h
	Get the total number of PWM IDs Command	30h	71h
	Restore FSC Command	30h	72h
	Set PWM value Command	3Ch	01h
	Get PWM value Command	3Ch	02h
	Set FAN Mode Switch Command	3Ch	03h
Other OEM Command Set	Restore Factory Default Command	32h	66h
	Get Board ID Command	3Ch	06h
	Get FAB Revision ID Command	3Ch	07h
	Global Reset to ME Command	3Ch	0Bh

	PFR Provision Command	3Ch	53h
	LED Control Command	3Ch	54h
	Get Alarm Event Severity Command	3Ch	55h

6.5.11 Monitoring

Sensors

The Table below shows the IPMI sensors monitored on the Whitestone2 by the AST2600 BMC.

Details of these sensor connections are described in the following sections.

The following thresholds are defined by the IPMI2.0 specification

Sensor List

Table 0-2: Whitestone2 BMC Sensor List

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
		[[Threshold Sensors]]									
SYS_Air_Inlet	30h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
CPU_Area	32h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
ENV_BMC_Area	35h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
M.2_NVME_Area	36h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
SYS_Air_Outlet	37h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCH_Area	38h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
CAM2_Area	39h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
C827_Area	3Ah	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
GPS_Area_1	3Bh	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
GPS_Area_2	3Ch	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
CPLD_Area	3Dh	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
CAM1_Area	3Eh	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
P12V_PSU	50h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P5V_AUX	51h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P3V3_AUX	52h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P12V	53h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P5V	54h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
P3V3	55h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P1V8_PCH_AUX	56h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P1V05_PCH_AUX	57h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVNN_PCH_AUX	58h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVCCFA_EHV	59h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVNN_MAIN	5Ah	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVCCD_HV	5Bh	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVCCIN	5Ch	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVCCFA_EHV_FIVRA	5Dh	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
PVCCINFAON	5Eh	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
P3V_BAT	5Fh	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[DC]
HSC_TEMP	0Fh	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
HSC_PIN	90h	Power Supply 08H	Threshold 01H	01H	BMC 20H	07H	00H	Watts 6	As and De	09h – UC	[AC]
HSC_VIN	91h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[AC]
HSC_IOUT	92h	Current 03H	Threshold 01H	01H	BMC 20H	07H	00H	Amps 5	As and De	09h – UC	[AC]
SYS_FAN0	61h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	00H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN1	62h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	00H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN2	63h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	01H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN3	64h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	01H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN4	65h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	02H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN5	66h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	02H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN6	67h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	03H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
SYS_FAN7	68h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	03H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN8	69h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	04H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN9	6Ah	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	04H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN10	6Bh	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	05H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN11	6Ch	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	05H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN12	6Dh	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	06H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN13	6Eh	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	06H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN14	6Fh	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	07H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN15	70h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	07H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
SYS_FAN16	71h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	08H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
SYS_FAN17	72h	Fan 04H	Threshold 01H	01H	BMC 20H	1DH	08H	RPM 12H	As and De	04h – LNR 02h – LC 00h – LNC	[DC]
P0_TEMP_T	01h	Temperature 01H	Threshold 01H	01H	BMC 20H	03H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_DTS_Margin_T	02h	Temperature 01H	Threshold 01H	01H	BMC 20H	03H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH1_DIM_T	10h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH2_DIM_T	11h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH3_DIM_T	12h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH4_DIM_T	13h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH5_DIM_T	14h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH6_DIM_T	15h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH7_DIM_T	16h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
P0_CH8_DIM_T	17h	Temperature 01H	Threshold 01H	01H	BMC 20H	08H	00H	Degree C 1	As and De	09h – UC	[DC]
PCH_T	05h	Temperature 01H	Threshold 01H	01H	BMC 20H	03H	00H	Degree C 1	As and De	09h – UC	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
VR48_TEMP	45h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
VR48_IOUT	93h	Current 03H	Threshold 01H	01H	BMC 20H	07H	00H	Amps 5	As and De	09h – UC	[AC]
VR48_VIN_A	94h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[AC]
VR48_VIN_B	95h	Voltage 02H	Threshold 01H	01H	BMC 20H	07H	00H	Volts 4	As and De	09h – UC 02h – LC	[AC]
VR_MOS1_TEMP	3Fh	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
VR_VCCIN_TEMP	40h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
VR_VCCFA_TEMP	41h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
VR_EHV_TEMP	44h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
VR_PVCCD_TEMP	42h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]
VR_FAON_TEMP	43h	Temperature 01H	Threshold 01H	01H	BMC 20H	07H	00H	Degree C 1	As and De	09h – UC	[AC]

[end]

Table 0-3: Whitestone2 BMC Discrete/Event only Sensor List

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
			[[Discrete Sensor]]								
System Event	80h	System Event 12H	Sensor Specific 6FH	03H	BMC 20H	07H	00H	Unspecified 0	As	01h – OEM System Boot Event 04h – PEF action 05h – Timestamp Clock Synch	[DC]
SEL Status	BBh	Event Logging Disabled 10H	Sensor Specific 6FH	02H	BMC 20H	06H	02H	Unspecified 0	As	02h – Log Area Reset/Cleared	[DC]
HSC_Status_Low	C1h	Other 0BH	Sensor Specific 6FH	02H	BMC 20H	14H	00H	Unspecified 0	As	[0]=1b, NONEABOVE_STATUS [1]=1b, CML_FAULT [2]=1b, TEMP_FAULT [3]=1b, VIN UV FAULT [4]=1b, IOUT OC FAULT [5]=1b, VOUT OV FAULT [6]=1b, HOTSWAP_OFF [7]=1b, BUSY	[AC]
HSC_Status_High	C2h	Other 0BH	Sensor Specific 6FH	02H	BMC 20H	14H	01H	Unspecified 0	As	[0]=1b, Unknown [1]=1b, Other [2]=1b, Fans [3]=1b, Power Good [4]=1b, MFR Specific [5]=1b, Input [6]=1b, Iout/Pout [7]=1b, Vout	[AC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
POST Error	2Bh	System Firmware Progress 0FH	Sensor Specific 6FH	03H	BIOS 01H	22H	00H	Unspecified 0	As	Event Data1: [7:6] 10b or 11b [5:4] 10b [3:0] Offset 0x00 (System Firmware Error) Event Data2: ED1[7:6]= 10b, LSB of POST Error Code. ED1[7:6]= 11b, Per IPMI Spec. Event Data3: MSB of POST Error Code	[AC]
DCMI Watchdog	60h	Watchdog2 23H	Sensor Specific 6FH	02H	BMC 20H	D0H	01H	Unspecified 0	As	[0]=1b, Timer expired [1]=1b, Hard Reset [2]=1b, Power Down [3]=1b, Power Cycle [8]=1b, Timer interrupt	[AC]
Power Unit State	ACh	Power Unit 09H	Sensor Specific 6FH	03H	BMC 20H	0AH	00H	Unspecified 0	As	04h – AC lost.	[AC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
Sys restart	82h	System Boot/ Restart Cause 1Dh	Sensor Specific 6FH	03H	BMC 20H	07H	00H	Unspecified 0	As	07h – System Restart. Event Data 2 and Event Data 3 must follow IPMI specification with the following Get System Restart Cause offsets	[DC]
ACPI_Power_State	ABh	System ACPI Power State 22h	Sensor Specific 6FH	03H	BMC 20H	07H	00H	Unspecified 0	As	Event Data1: [7:4]=0000b [3:0]= 0h – S0/G0 “working” 5h – S5/G2 “soft-off”	[DC]
Critical IRQ	EAh	Critical Interrupt 13h	Sensor Specific 6FH	03H	BMC 20H	07H	00H	Unspecified 0	As	00h - Diagnostic Interrupt	[DC]
Clear_CMOS	C7h	OEM RESERVED C0H	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: [7:0] 01h – Assert Event Data2: 0xFF Event Data3: 0xFF	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCleErr_Slot1	00h	Critical Interrupt 13h	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: A4h – PCI PERR A5h – PCI SERR A7h – Bus Correctable Error A8h – Bus Uncorrectable Error AAh – Bus Fatal Error AFh – Last Boot PCI Error Event Data2: [7:0] – PCIe Bus Number Event Data3: [7:3] – PCIe Device Number [2:0] – PCIe Function Number	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCleErr_Slot2	01h	Critical Interrupt 13h	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: A4h – PCI PERR A5h – PCI SERR A7h – Bus Correctable Error A8h – Bus Uncorrectable Error AAh – Bus Fatal Error AFh – Last Boot PCI Error Event Data2: [7:0] – PCIe Bus Number Event Data3: [7:3] – PCIe Device Number [2:0] – PCIe Function Number	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCleErr_CAM1	02h	Critical Interrupt 13h	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: A4h – PCI PERR A5h – PCI SERR A7h – Bus Correctable Error A8h – Bus Uncorrectable Error AAh – Bus Fatal Error AFh – Last Boot PCI Error Event Data2: [7:0] – PCIe Bus Number Event Data3: [7:3] – PCIe Device Number [2:0] – PCIe Function Number	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCleErr_CAM2	03h	Critical Interrupt 13h	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: A4h – PCI PERR A5h – PCI SERR A7h – Bus Correctable Error A8h – Bus Uncorrectable Error AAh – Bus Fatal Error AFh – Last Boot PCI Error Event Data2: [7:0] – PCIe Bus Number Event Data3: [7:3] – PCIe Device Number [2:0] – PCIe Function Number	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCleErr_M2_Slot1	81h	Critical Interrupt 13h	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: A4h – PCI PERR A5h – PCI SERR A7h – Bus Correctable Error A8h – Bus Uncorrectable Error AAh – Bus Fatal Error AFh – Last Boot PCI Error Event Data2: [7:0] – PCIe Bus Number Event Data3: [7:3] – PCIe Device Number [2:0] – PCIe Function Number	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PCleErr_M2_Slot2	82h	Critical Interrupt 13h	Sensor Specific 6FH	03H	BIOS 01H	07H	00H	Unspecified 0	As	Event Data1: A4h – PCI PERR A5h – PCI SERR A7h – Bus Correctable Error A8h – Bus Uncorrectable Error AAh – Bus Fatal Error AFh – Last Boot PCI Error Event Data2: [7:0] – PCIe Bus Number Event Data3: [7:3] – PCIe Device Number [2:0] – PCIe Function Number	[DC]
CPU_STATUS	03h	Processor 07H	Sensor Specific 6FH	03H	BMC 20H	03H	00H	Unspecified 0	As	Event Data1: 01h - Thermal Trip	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
PFR_Status	ADh	Other 0BH	Sensor Specific 6FH	02H	BMC 20H	21H	00H	Unspecified 0	As	Event Data1: 00h: AC cycle 01h: PCH update intent 02h: BMC update intent 03h: BMC reset detected 04h: BMC WDT expired 05h: Intel® ME WDT expired Event Data2: 01h: BMC authentication failure 02h: PCH/CPU authentication failure 04h: Intel® PFR CPLD authentication failure Event Data3: BMC or PCH authentication failure 01h: Active region authentication failure 02h: Recovery region authentication failure 06h: FW update capsule failed authentication	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_1_ECC_Error	01h	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_2_ECC_Error	03h	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_3_ECC_Error	05h	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_4_ECC_Error	07h	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_5_ECC_Error	09h	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_6_ECC_Error	0Bh	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_7_ECC_Error	0Dh	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

[Sensor Name]	Sensor Number	Sensor Type	Event/Reading Type	Sensor Record Type	Sensor Owner ID	Entity ID	Entity / Instance	Sensor Unit Type	Assert/Dassert	Event Offset Trigger	Monitor during AC/DC on
DIMM_8_ECC_Error	0Fh	Memory 0Ch	Sensor Specific 6FH	03H	BIOS 3FH	08H	00H	Unspecified 0	As	Event Data1: 0xA0 : Correctable ECC. 0xA1 : Uncorrectable ECC. Event Data2: If ED1 = 0xA0 , 0xA1 ,0xA5 ED2 [7:4] : Reserved ED2 [3] : Dimm valid bit ED2 [2] : Channel valid bit ED2 [1] : Socket valid bit ED2 [0] : 0 =Current , 1= Last Boot If ED1 = 0xA4 ED2 [7:0] : Reserved Event Data3: Reserved	[DC]

6.7 Thermal Design

MiTAC Whitestone2 ORAN DU is designed for the use at cell or tower site in an outdoor cabinet and defined the operating temperature at -40C to 65C.

For operating at high temperature, need to consider below thermal solution:

- EVAC heatsink for CPU
- Heatsink for hot components such as: Intel PCH, NIC, M.2.
- Dual rotor fan with fan control to support one fan fail



For operating at low temperature, need to consider below thermal solution:

- Select industrial level components (operating at -40C) or add heaters for cold boot circuits so the DU can be power on at -40C.
- Temperature sensors for heater enable.

Appendix A - Checklist for Steering Committee (SC) approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes	
Was it approved in the OCP Contribution Portal?	No	In Process
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	MiTAC
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	

Appendix B-__ <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist

(to be provided by each supplier seeking OCP recognition for a Hardware Product based on this specification)

Company: [MiTAC Computing Technology](#)

Contact Info: [Alex Chou \(alex.chou@mic.com.tw\)](mailto:alex.chou@mic.com.tw)

Product Name: [Whitestone2 5G CU/DU Edge Server](#)

Product SKU#: [WS1S11](#)

Link to Product Landing Page:

https://www.mitaccomputing.com/5GEdgeComputing_WS1S11_WS1S11_EN~Spec

The following is needed for OCP hardware product recognition:

For OCP Inspired™

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Declare product is 100% compliant with specification
- Complete the [OCP Inspired™ Product Recognition Checklist](#), which includes hardware management conformance checks and security profile.

For OCP Accepted™

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Complete the [OCP Accepted™ Product Recognition Checklist](#), which includes hardware management conformance checks, security profile and open system firmware conformance checks.
- Submit a design package meeting [OCP Hardware Design Guideline Contribution Checklist](#) (if not already submitted by the contributor). If already submitted, declare the product is 100% compliant with the design package.
- Submit a firmware package including a firmware image, build scripts, documentation, test results and a tool that verifies modifications
- Submit the BMC source code, if applicable to product type

Please complete the OCP Inspired™ Product Recognition Submission Checklist or OCP Accepted™ Product Recognition Checklist and the following table.

Item	Details	Links
Which product recognition?	OCP Accepted™ or OCP Inspired™	Provide link for the appropriate Product Checklist
If OCP Accepted™, who provided the Design Package?		Link to OCP Contribution Database
Where can a potential adopter purchase the product?		Link to OCP Marketplace