OPEN

Compute Project

Wedge 400 Design Specification

V0.3

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1. License

1.1 Open Web Foundation (OWF) CLA

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Notes:

1) The following clarifications, which distinguish technology licensed in the Contribution License and/or Specification License from those technologies merely referenced (but not licensed), were accepted by the Incubation Committee of the OCP: None

2) The above license does not apply to the Appendix or Appendices. The information in the Appendix or Appendices is for reference only and non-normative in nature.

1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback: List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

2. OCP Tenets Compliance

Note: The ideals behind open sourcing stipulate that everyone benefits when we share and work together. Any open source project is designed to promote sharing of design elements with peers and to help them understand and adopt those contributions. There is no purpose in sharing if all parties aren't aligned with that philosophy. The IC will look beyond the contribution for evidence that the contributor is aligned with this philosophy. The contributor actions, past and present, are evidence of alignment and conviction to all the tenets.

2.1 Openness

The measure of openness is the ability of a third party to build, modify, or personalize the device or platform from the contribution. OCP strives to achieve completely open platforms, inclusive of all programmable devices, firmware, software, and all mechanical and electrical design elements. Any software utilities necessary to modify or use design contributions should also be open sourced. Barriers to achieving this goal should be constantly addressed and actions taken to remove anything that prevents an open platform. Openness can also be demonstrated through collaboration and willingness to share, seek feedback, and accept changes to design and specification contributions under consideration.
W400: The electrical design and mechanical design of W400 is fully open, and all the PCB and chassis design files have been included in the design package.

2.2 Efficiency

Continuous improvement has been a fundamental value of the industry. New contributions (and updates to existing contributions) shall be more efficient than existing or prior generation contributions. Efficiency can be measured in many ways - OpEx and CapEx reduction, performance, capacity, power or water consumption, raw materials, utilization, size or floorspace are some examples. The goal is to express efficiency with clear metrics, valued by end-users, when the contribution is proposed.
W400: The system comes in a 2RU form factor, slightly larger than W100S, its 32 x 100G predecessor, while quadrupling the switching throughput both in terms of bandwidth and packets per second. The SCM is FRU-able in W400, which increases the efficiency in fleet maintenance.

2.3 Impact

OCP contributions should have a transformative impact on the industry. This impact can come from introducing new technology, time-to-market advantage of technology, and/or enabling technology through supply chains that deliver to many customers in many regions of the world. New technologies are impactful when such technology is enabled through a global supply channel. (W400 Switch System Generic Specification http://opencompute.org) One example is the NIC 3.0 specification which achieved global impact by having over 12 companies author, adopt, and supply products that conformed to the specification. Another example is emerging and open security features that establish and verify trust of a product.
W400 leverages the latest generation of switch ASIC, utilizes the 50G PAM4 SerDes technology at scale, and achieves efficiency gains outlined above.

2.4 Scale

OCP contributions must have sufficient enabling, distribution and sales support (pre and post) to scale to Fortune 100 as well as large hyperscale customers. Demonstration of this tenet can be accomplished by providing sales data or by providing go-to-market plans that involve either platform/component providers or systems integrator/VAR (direct and/or channel). Platform/component providers or systems integrators/VARs that can use this contribution to obtain product recognition (OCP Accepted™ or OCP Inspired™) and create Integrated Solutions which would also demonstrate scale. Software projects can also demonstrate this tenet when software is adopted across business segments or geographies, when software is a key factor in accelerating new technology, or when software provides scale of new hardware which meets OCP tenets.

W400: It is designed with FRU-able switch control module (microserver), fan, and PSU for easy field maintenance. There are multiple hardware sensors built-in, and OpenBMC has necessary utilities for hardware monitoring. It has been and will continue to be deployed as a top of rack switch in large quantities.

3. Revision Table

Date	Revision #	Author	Description
8/1/2020	V0.1	Lingjun Wu	Initialized the draft version.
2/1/2022	V0.2	Lingjun Wu	Added license and tenets sections. Added the link of supplier info.
2/16/2022	V0.3	Lingjun Wu	Fixed the editing issue for the tenet chapter according to OCP review feedbacks.

4. Introduction

4.1. Scope

The purpose of this document is to provide a system description of the Meta Wedge400 platform.

This document also introduces Wedge400's software accessible interfaces, and required software actions to properly manage the hardware at the system level.

4.2. System Description

Wedge400 is Meta's new generation Top of Rack switch. It can be used as rack (OpenRack v2) switch of data center network of Meta.
The main attributes are:

- Box Size
  - 87.5mm(H) x 440mm(W) x 558.8 mm(D)
- Traffic Ports
  - 16 x QSFP-DD: 400G/200G/100G ports
  - 32 x QSFP56: 200GE/100GE ports or 2*50GE/4*25GE/4*10GE breakout ports
- Management Ports
  - one RJ45 as RS232 console port to BMC.
  - One RJ45 as OOB GE management port, it supports 1000M/100M/10M Base-T.
  - USB 2.0 compatible, supports OCP debug card.
  - Rackmon: 3 x RJ45 as RS485 ports, 1 x RJ45 as GPIO.
- Switch Main Board (SMB)
  - Switch Main Board has Switch ASIC, BMC, and front panel ports.
  - Data plane:
    - Switching ASIC: Broadcom's BCM56980 a.k.a. Tomahawk 3, 12.8Tbps, 256*50G PAM4 SERDES.
  - Management Plane:
    - BMC: Aspeed AST2520
      - Located on SMB board
      - UART mux for supporting sol.sh
      - I2C system management bus
      - JTAG controller for programming CPLDs
      - 128MB flashes and 8G eMMC for BMC, located on SCM, a.k.a. BMC Storage Module (BSM).
    - GbE Switch: for all COM-e, BMC, and front RJ45 OOB port (one of the SGMII interfaces reserved to Rackmon connector for future use to replace the GPIO port)
- System Controller Module (SCM)

    - Minilake, developed for Meta, as industrial standard COM-Express CPU module, Type 7.
    - SCM is pluggable on rear side.
    - One M.2 SSD slot:
        - NMVe PCIe 3.0 x4;
    - One M.2 BSM slot:
        - BMC Storage Module, it includes 2 flashes and 1 eMMC;
- Power Plane
    - AC/DC modules or DC/DC (PEM) modules;
    - AC/DC PSU 1+1:
        - 90Vac to 305Vac input
    - DC/DC PEM for single 12V inputs:
        - Hot-swap / slow powerup controller
        - 3.3V Standby (always on) @0.5A; ORing/LDO on 3.3V;
        - PSU_ON signal to enable/disable 12V output;
        - Top of Rack installation will go with one DC/DC PEM module (There is NO dual 12V inputs supporting);
- Fan System
    - Four 80mm x 80mm x 80mm counter-rotating fan-trays, which shares the same part from Meta Minipack/Backpack systems;

4.3. Common Terms

The following terms are used in Wedge400 project:

- 100GE – 100 Gigabit Ethernet
- 200GE – 200 Gigabit Ethernet
- 400GE – 400 Gigabit Ethernet
- SMB – Switch Main Board
- SCM – System Controller Module
- FCM – Fan Controller Module
- PDB –Power Distribution board
    - PDB-T – Power Distribution board, this is for top PSU/PEM plugged in.
    - PDB-B – Power Distribution board, this is for bottom PSU/PEM plugged in.
- COM-E – COM-Express CPU module
- PSU – Power Supply Unit
- PEM – Power Extension Module
- QSFP28 –Quad Small Form-factor Pluggable (QSFP) at 4 x 28Gbps, used for 100GBE
- QSFP56 –Quad Small Form-factor Pluggable (QSFP) at 4 x 56Gbps, used for 200GBE
- QSFP-DD –Quad Small Form-factor Pluggable Double Density at 8 x 56Gbps, used for 400GBE
- BMC -- Baseboard Management Controller
- BSM -- BMC Storage Module
- Rackmon – Rack Monitor Interface

5. System Architecture

5.1. System Architecture

Wedge400 is a single switch ASIC modular system, it only has one 12.8T switch ASIC, one System Control Module (SCM) and one BMC. It has four 80mm x 80mm x 80mm CR fan trays to cool the system. The following picture shows the system diagram of Wedge400 switch:

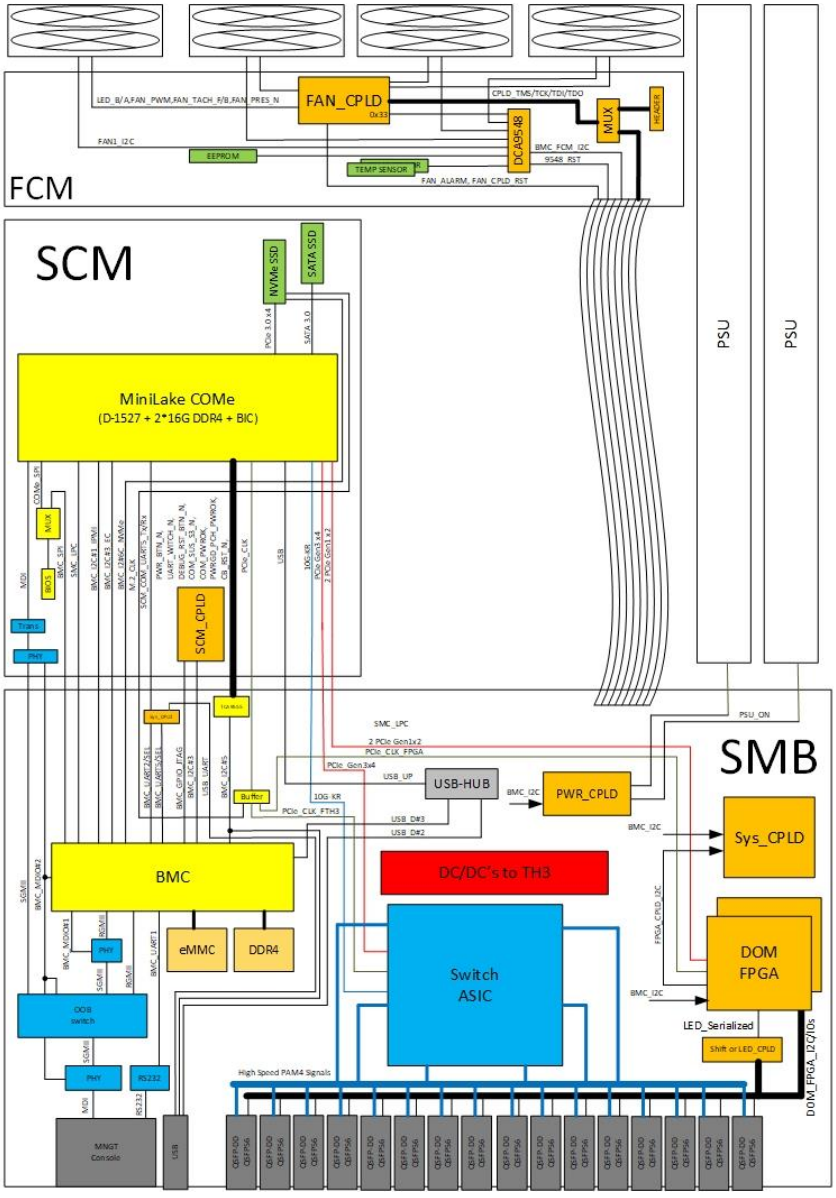


Figure 1:System architecture of Wedge400

The System Control Module (SCM) carries one COM-e Broadwell-DE CPU module, and can be plugged into the chassis from rear side. The Broadwell-DE CPU module provides the control function of Wedge400.
Switch Main Board (SMB) is fixed to the chassis, it consists of switch ASIC, BMC system, and connectors to SCM. The switch ASIC is controlled by Broadwell-DE CPU of SCM through PCIe Gen3 interface.

5.2. Chassis Design

Wedge400 is standard 19” wide, 2-RU height modular switch.

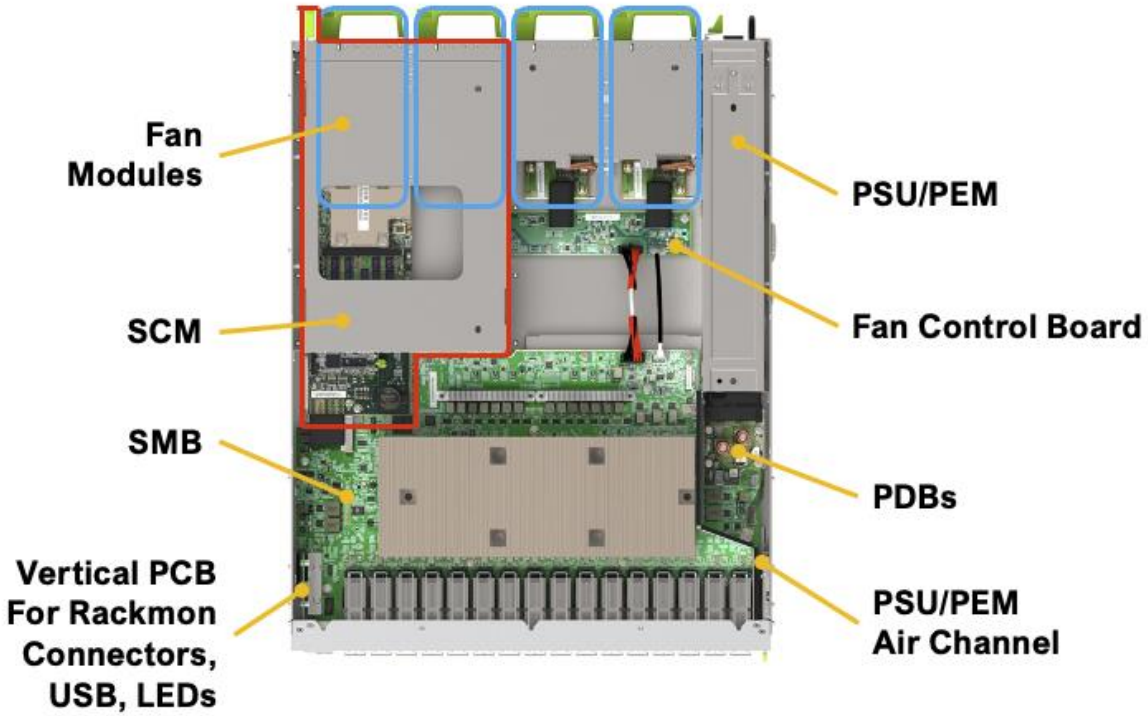


Figure 2:Wedge400 Chassis top View

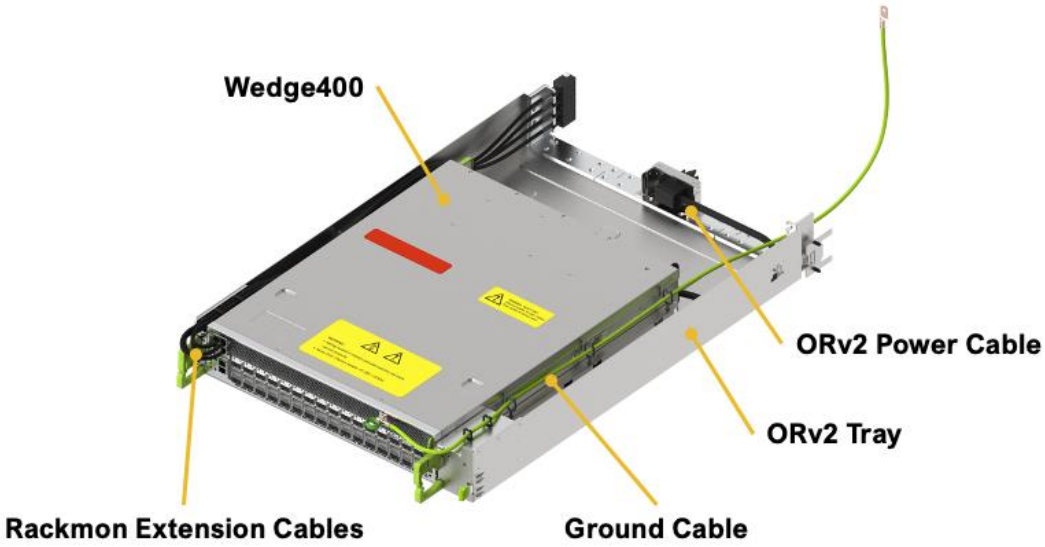


Figure 3: Wedge400 with ORv2 Tray

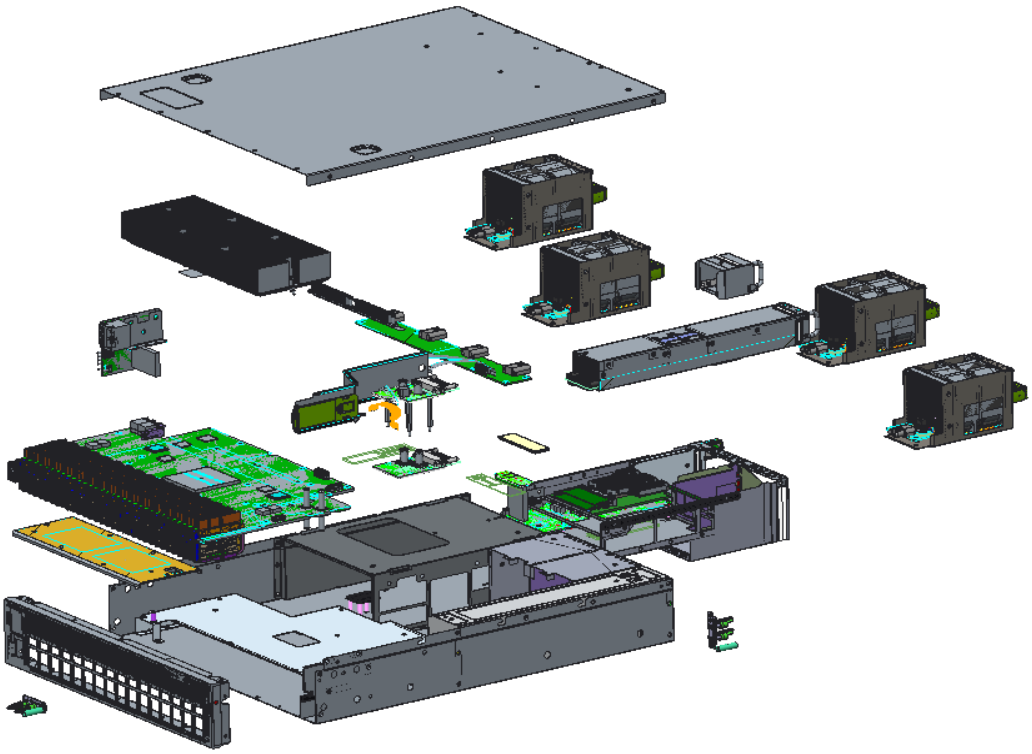


Figure 4: Wedge400 explosion overview

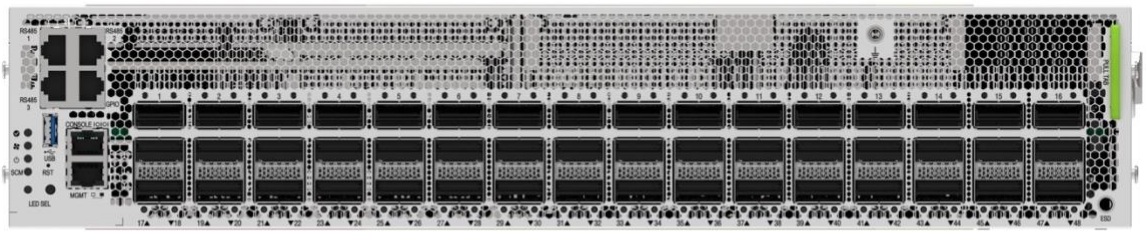


Figure 5:Wedge400 Front View

Figure 6:Wedge400 Rear View

5.3. Data Plane

Wedge400 has 12.8T switch ASIC as the main data plane chip. The switch ASIC supports 32 x 400G port configuration, or 64 x 200G port configuration, or 128 x 100G port configuration.

5.3.1. Switch Element

Wedge400 uses the Meta unique switch element to form the fabric. One switch element has one BMC, one CPU module and one switch ASIC. This unique switch element architecture makes our data center network disaggregated, easily managed and easy to scale.
Wedge400 is one switch element which can support 16 x 400/200/100G + 32 x 200/100G. It's designed to be used as the Top of Rack switch for ORv2 in Meta data centers.

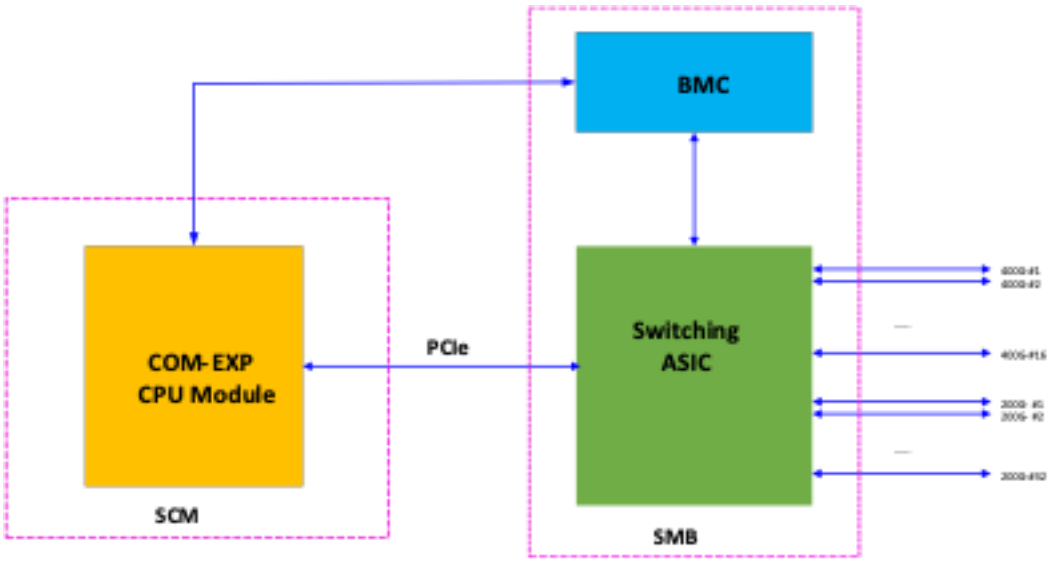


Figure 7:Switch Element

5.3.2. Switch ASIC Port-mapping

There are 16 QSFP-DD ports and 32 QSFP56 ports on Wedge400. The front panel placement is shown as below.

QDD_P1	QDD_P2	QDD_P3	QDD_P4	QDD_P5	QDD_P6	QDD_P7	QDD_P8	QDD_P9	QDD_P10	QDD_P11	QDD_P12	QDD_P13	QDD_P14	QDD_P15	QDD_P16
Q56_P17	Q56_P19	Q56_P21	Q56_P23	Q56_P25	Q56_P27	Q56_P29	Q56_P31	Q56_P33	Q56_P35	Q56_P37	Q56_P39	Q56_P41	Q56_P43	Q56_P45	Q56_P47
Q56_P18	Q56_P20	Q56_P22	Q56_P24	Q56_P26	Q56_P28	Q56_P30	Q56_P32	Q56_P34	Q56_P36	Q56_P38	Q56_P40	Q56_P42	Q56_P44	Q56_P46	Q56_P48

Figure 8:Wedge400 Faceplate Port Numbering

5.4. Control Plane

Main control plane features are listed below:

- COM-Express BW-DE CPU module
  - 8mm mating distance.
  - Implemented on SCM
- BMC as management entity to control Switch ASIC and COM-E CPU module
  - Enable/disable power of switch ASIC or COM-e
  - OOB ethernet to front port
  - Console port to front port

    - SMB bus and I2C bus to SCM COM-E CPU module
- Front panel management and debug interface
- Meta 2nd generation debug connector
- PCIe Interface
- Switch ASIC: PCIe x4 gen3
- 2 pcs of DOM FPGAs: PCIe x 1/2 gen1/2
- NVMe: PCIe x4 gen3
- PCIe clock is from COM-E module
- LPC bus
- SCM COMe LPC bus control the following device
- BMC on SMB
- OOB Ethernet (BCM5389)
- 8-port OOB switch on SMB
- BMC GBE ethernet interface
- BMC RGMII interface
- SCM COM-E ethernet interface
- Switch ASIC management GBE port(SGMII)
- Front RJ45 OOB ethernet interface
- Two ports reserved for RackMon
- USB
- COM-E is root-complex port
- 3-port USB hub on SMB
- BMC USB slave port
- Meta OCP debug USB from the USB HUB

5.4.1. Clock Tree

The following diagram shows the clock design in the system:

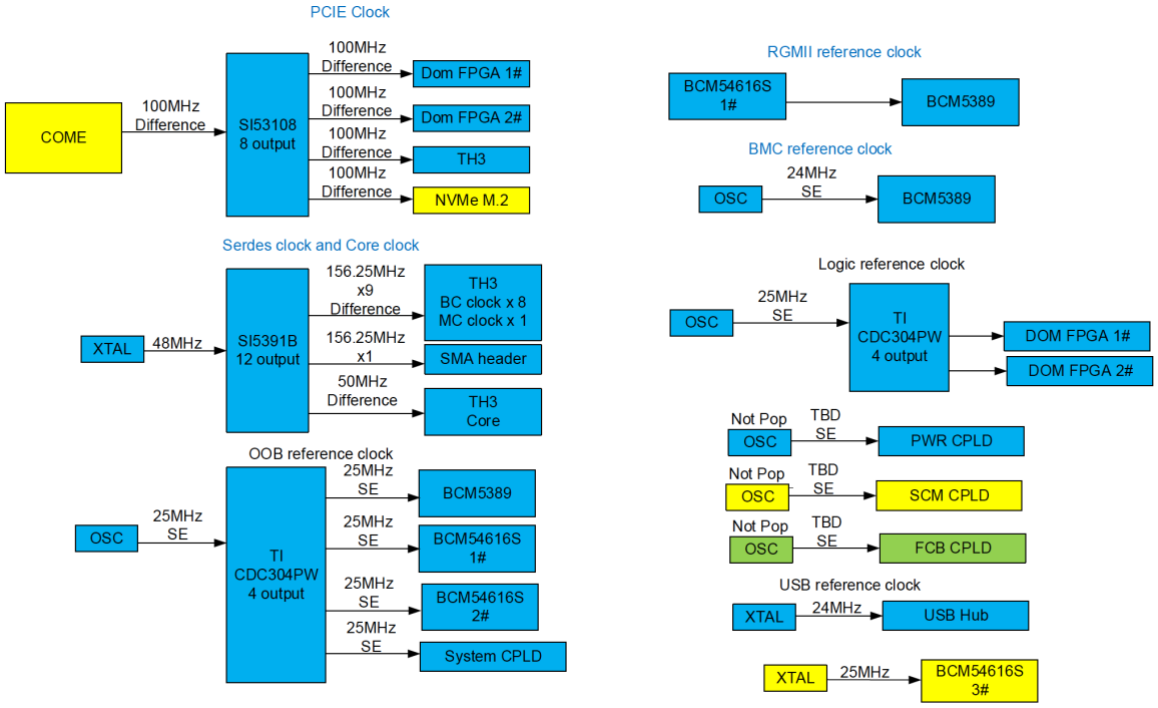


Figure 9:Clock Tree

5.4.2. PCIe Assignments

The following diagram shows the PCIe port assignments from Broadwell-DE to TH3, DOM FPGAs and NVMe SSD.

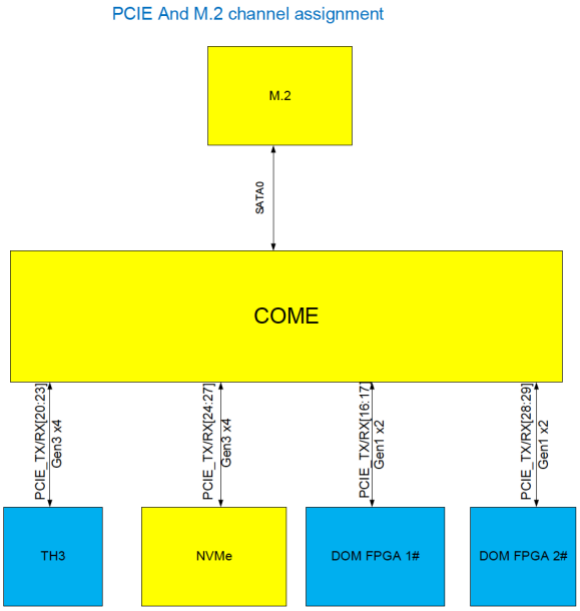


Figure 10:PCIe Diagram

5.5. Chassis management Plane

BMC on SMB works as the chassis management module, Chassis management bus is I2C, and the management bus can access the following modules/components:

- System Management Module (SCM)
- FCM/FAN
- PSU/PEM
- Temperature sensors and power monitoring.

5.5.1. BSM (BMC Storage Module)

The BSM module was introduced to support META security requirement. It contains NOR flashes (primary and secondary) and eMMC on a daughter card for easily removing and shredding by ERAD team when the unit goes through RMA. This daughter card is based on M.2 form factor and connector. Here is the diagram of BSM module:

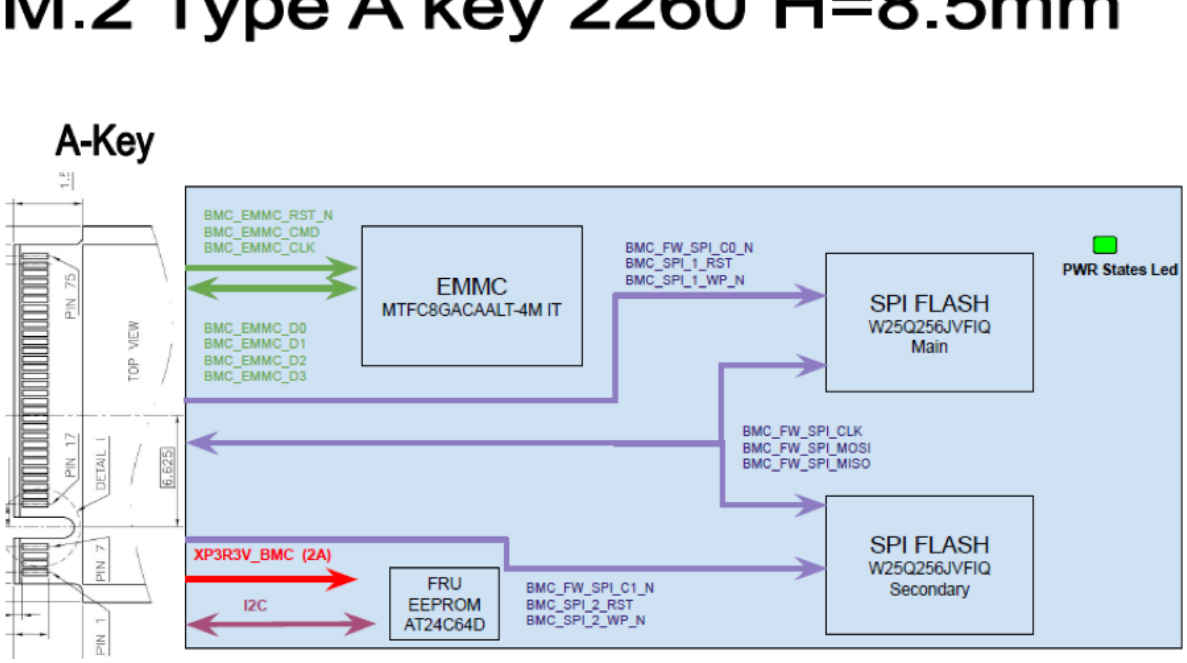


Figure 11:BSM Diagram

The components are all placed on top side to simplify the manufacturing process. Based on the placement, 2260 formfactor is selected. The I2C interface is routed to the M.2 connector on SCM. An EEPROM is used for FRU info, located on M.2 card, accessible from BMC.

Figure 12:BSM PCB Design

Pinout definition (Based on A-key):
Table 1:M.2 Pin Definition

74	BMC_+3.3V	75	GND
72	BMC_+3.3V	73	NC
70	NC	71	BMC_EMMC_D0
68	NC	69	GND
66	BMC_EMMC_RST_N	67	BMC_EMMC_D1
		65	BMC_EMMC_D2

64	NC		
		63	GND
62	NC		
		61	BMC_EMMC_D3
60	NC		
		59	BMC_EMMC_CMD
58	BMC_EMMC_D4 (Reserved)		
		57	GND
56	BMC_EMMC_D5 (Reserved)		
		55	BMC_EMMC_CLK
54	BMC_EMMC_D6 (Reserved)		
		53	NC
52	BMC_EMMC_D7 (Reserved)		
		51	GND
50	NC		
		49	PERp0 (Reserved)
48	NC		
		47	PERn0 (Reserved)
46	EEPROM_WP		
		45	GND
44	ALERT# (Reserved)		
		43	PETp0 (Reserved)
42	SMB_DATA (3.3V)		
		41	PETn0 (Reserved)
40	SMB_CLK (3.3V)		
		39	GND
38	FRU_EEPROM_ADDR (Floating on MB: 0xAC; GND on MB: 0xA8)		
		37	BMC_FW_SPI_CS0_N
36	GND		
		35	BMC_FW_SPI_CS1_N
34	REFCLKp (Reserved)		
		33	GND
32	REFCLKn (Reserved)		
		31	BMC_FW_SPI_CLK

30	GND		
		29	GND
28	BMC_SPI_0_HOLD_N		
		27	BMC_FW_SPI_MOSI
26	BMC_SPI_1_HOLD_N		
		25	BMC_FW_SPI_MISO
24	GND		
		23	GND
22	USB_D+ (Reserved)		
		21	BMC_SPI_1_RST
20	USB_D- (Reserved)		
		19	BMC_SPI_2_RST
18	GND		
		17	NC
16	EMMC_PRESENT_N		
		15	A-Key
14	A-Key		
		13	A-Key
12	A-Key		
		11	A-Key
10	A-Key		
		9	A-Key
8	A-Key		
		7	GND
6	NC		
		5	BMC_SPI_1_WP_N
4	BMC_+3.3V		
		3	BMC_SPI_2_WP_N
2	BMC_+3.3V		
		1	GND

As BMC is on SMB and it's not easy to access if BMC flash and eMMC were located on SMB, so physically this daughter card (BSM, BMC Storage Module) is located on SCM as SCM is a FRU, and users can easily pull out the SCM card, and then take the BSM module out for ERAD/replacement. Here is the picture of W400 BSM module:

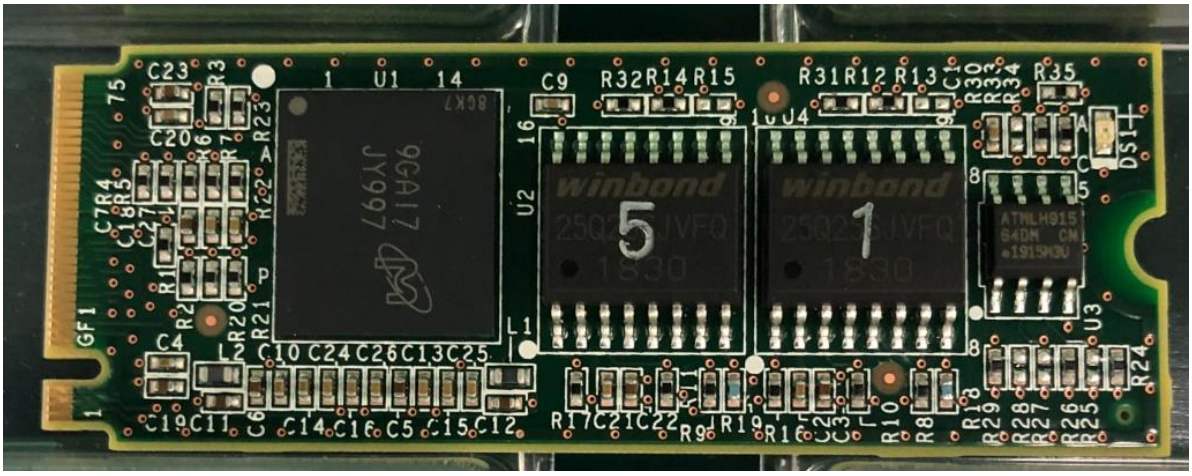
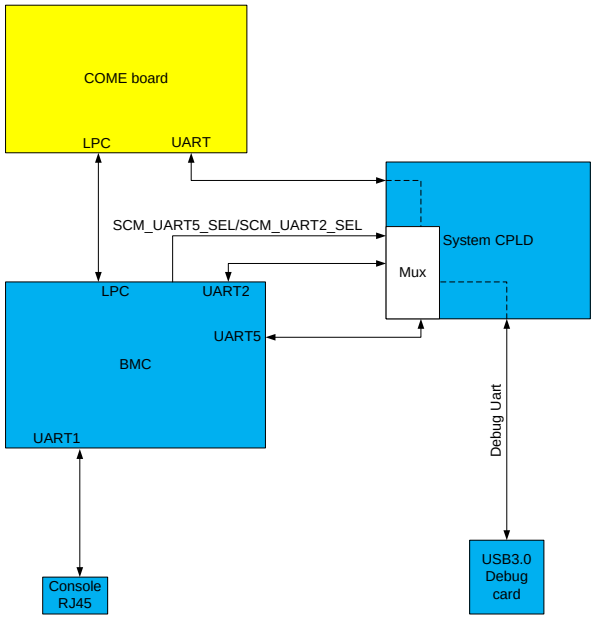


Figure 13:BSM proto picture

5.5.2. UART Connection

The following diagram shows UART connections of front console port, uS and BMC's UART ports.



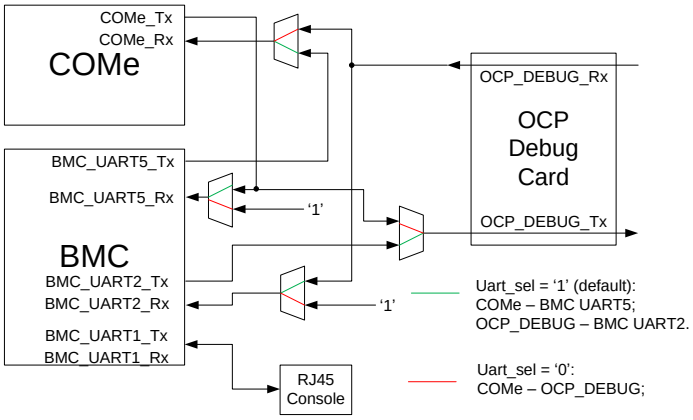


Figure 14:UART Diagram

5.5.3. OOB Switch

The following diagram shows the OOB switch connections.

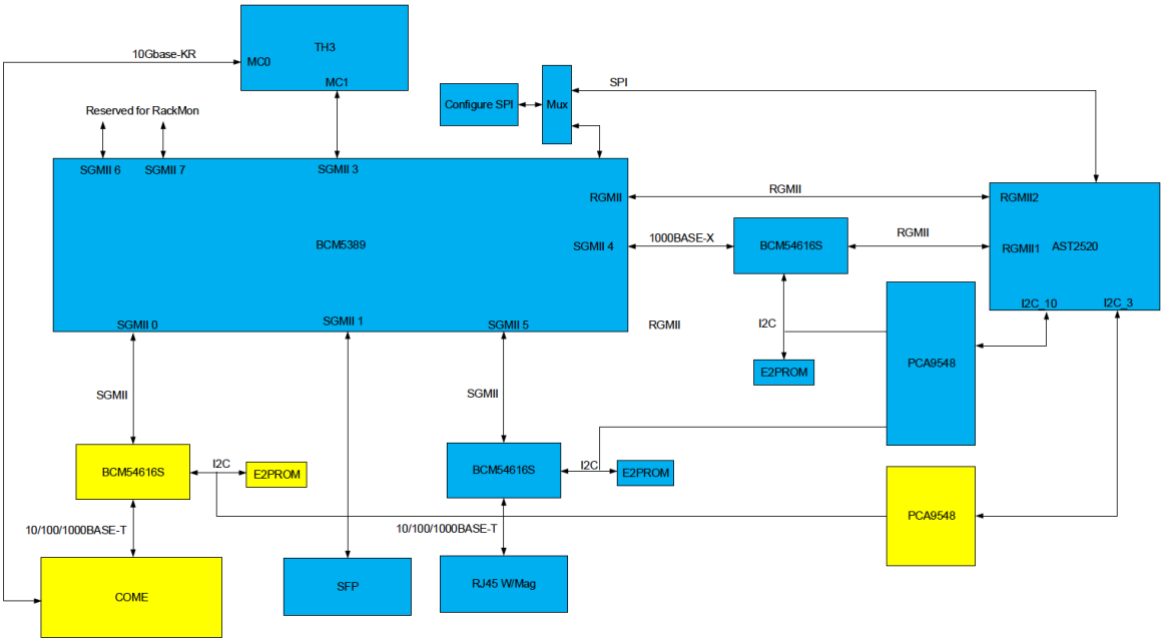


Figure 15:OOB Diagram

5.5.4. RackMon Interface

The following diagram shows the RackMon interface in system.

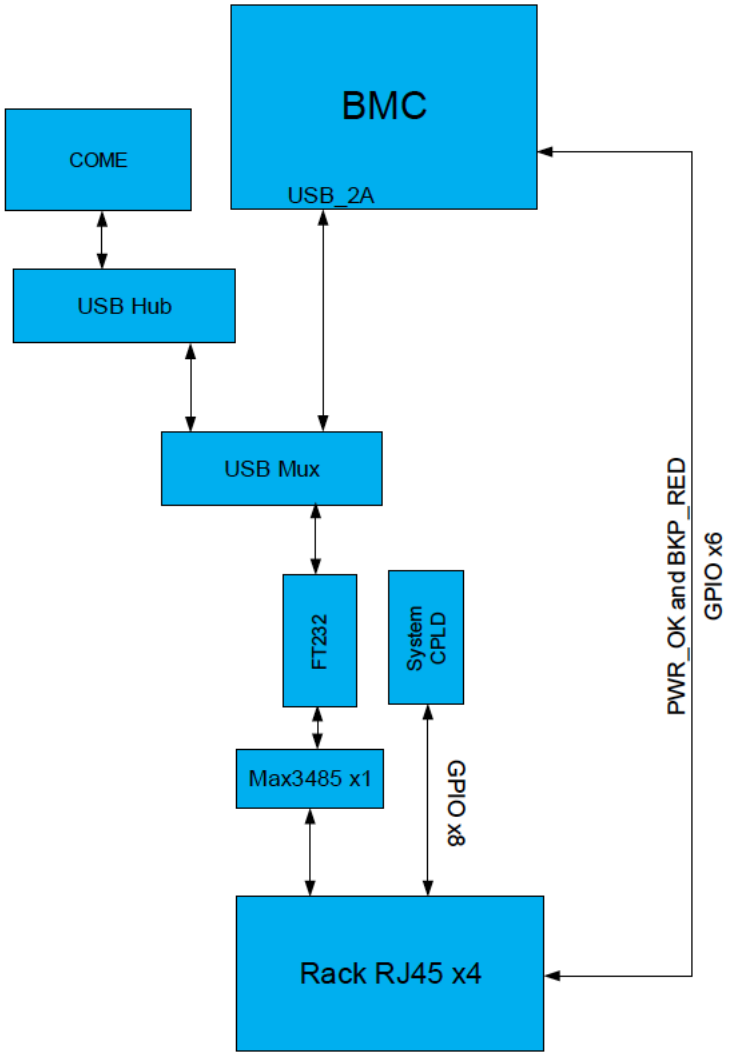


Figure 16:Rackmon Diagram

5.6. System Powerup Sequence

Wedge400 has a PWR CPLD design to enable remotely power cycling the whole system. The powerup sequencer controls the major power rails coming up in the right sequence. The hot swap controller is designed for FRUs like SCM. Here is the diagram showing the detailed HW design:

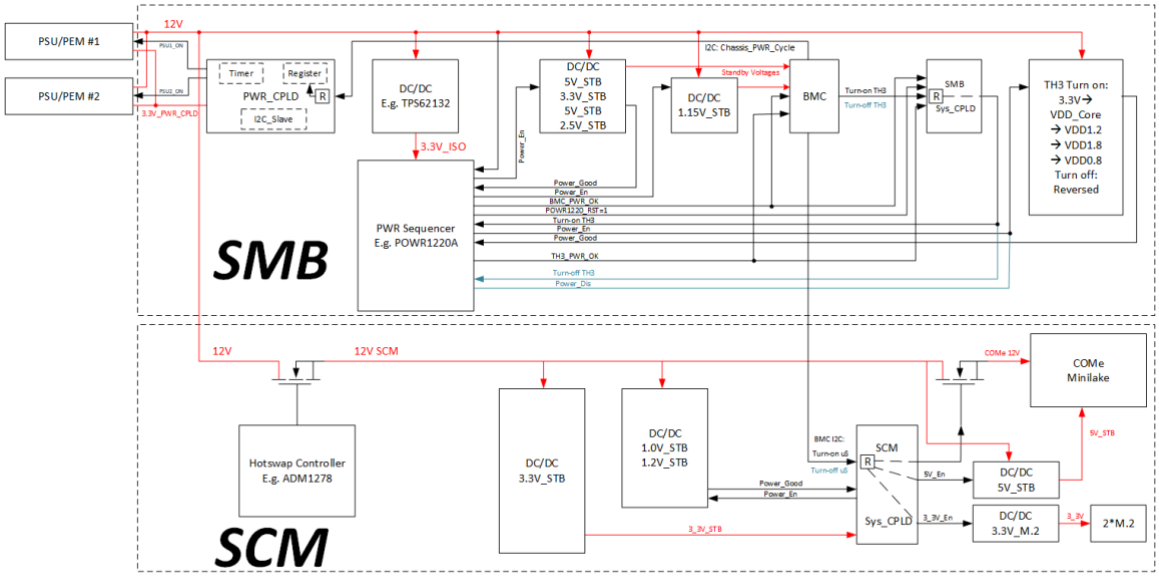


Figure 17:Wedge400 power control/sequence diagram

5.7. Switch Main Board (SMB)

Switch Main Board has two major function blocks:

- Data plane function with 12.8T Switch ASIC;
- Management plane function with BMC AST2520 system;
    - BMC supports TPM 2.0 through I2C device SLB 9670VQ2.0.

SMB also provides DOM FPGA function for SCM CPU to access QSFP modules through PCIe. Here is high level DOM FPGA diagram:

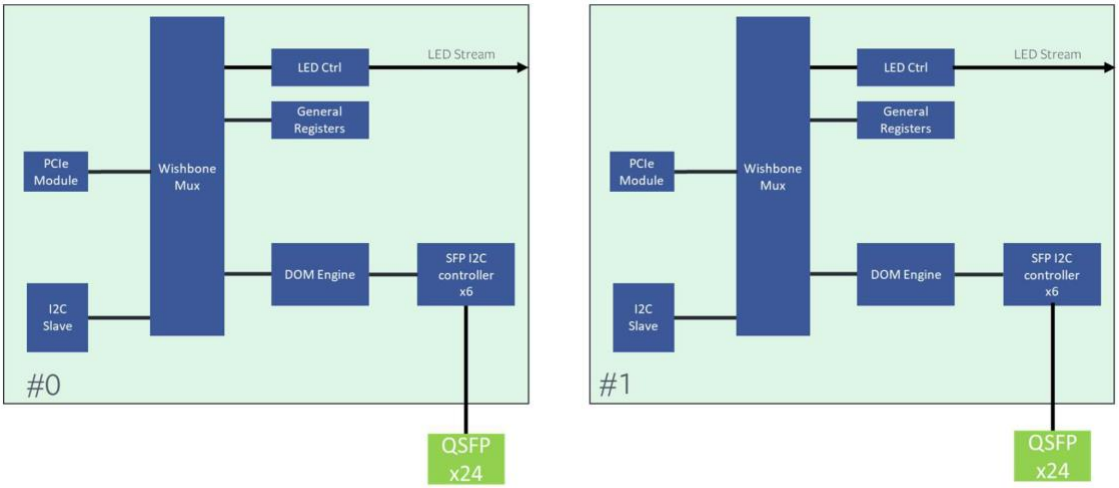


Figure 18:DOM FPGA Diagram

5.7.1. Block Diagram of SMB

The following diagram shows the diagram of Switch Main Board (SMB).

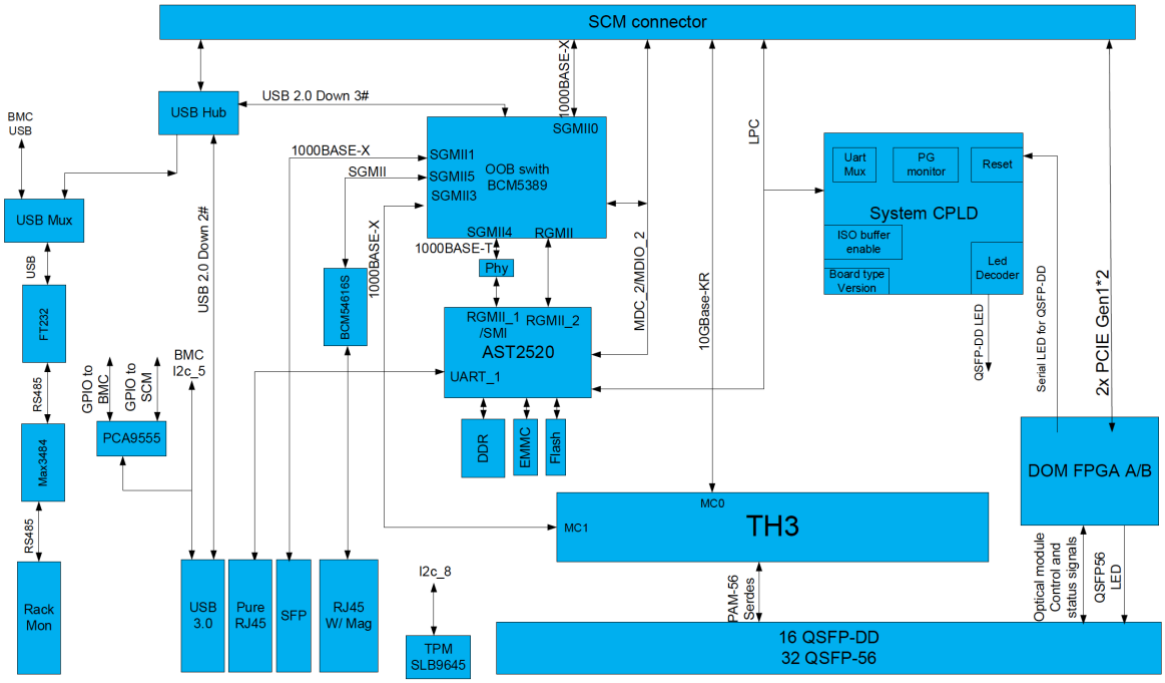


Figure 19:Switch Main Board Diagram

5.7.2. BMC I2C diagram

The following table shows the I2C topology of BMC.

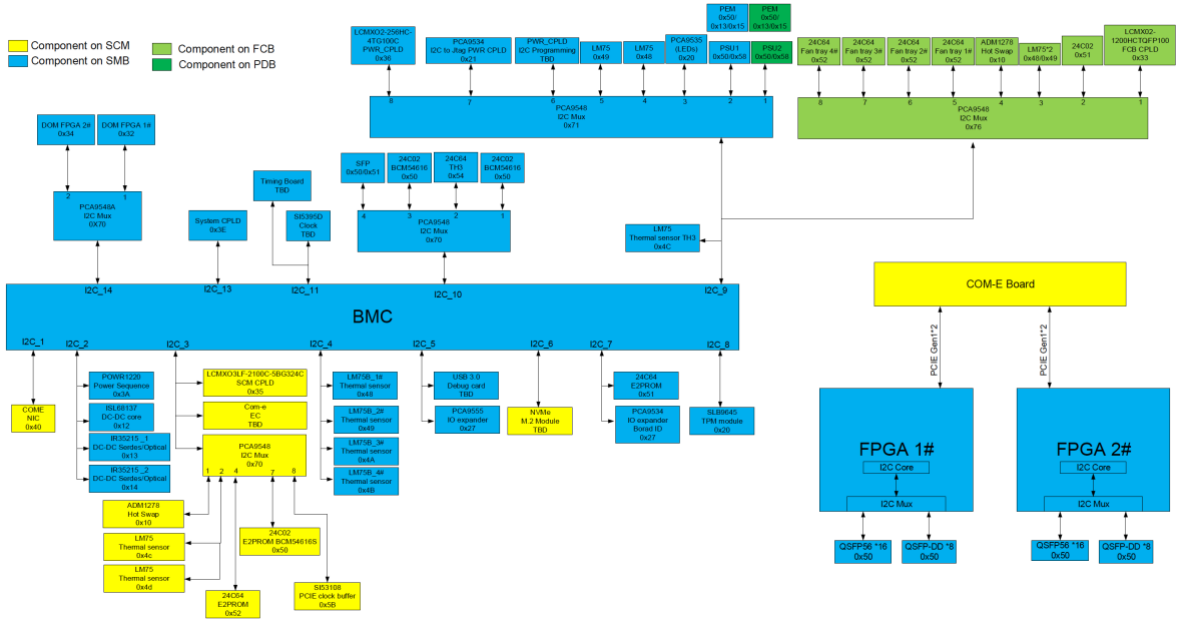


Figure 20:SMB I2C Diagram

5.7.3. BMC I2C mapping

Table 2:BMC I2C address table

HW Bus	SW Bus	Address	Component	Board
I2c_1		0x20	Com-e EC	SCM
I2c_2		0x2F	IR3595 (XP3R3V & Serdes) I2C	SMB
		0x47	IR3595 (XP3R3V & Serdes) PMBus	
		0x35	IR3595 (XP3R3V & 0.8 Voltage) I2C	
		0x4D	IR3595 (XP3R3V & 0.8 Voltage) PMbus	
		0x60	ISL68137 (TH3 Core Voltage)	
		0x3A	POWR1220	
I2c_3		0x3e	SCM CPLD	SCM
		0x70	PCA9548	SCM
I2c_3 0x70 I2C Switch	Channel1, 0x01	0x10	ADM1278	SCM
	Channel2, 0x02	0x4C	TMP75#1	
		0x4D	TMP75#2	
	Channel4, 0x08	0x52	24C64 (SCM_Inv)	
	Channel5, 0x10	0x50	24C02 (BCM54616S EEPROM)	
	Channel6, 0x20		NVME	
	Channel7,TBD	0x56	BSM EEPROM	
	Channel8, 0x80	0x6c	SI53108(Clock buffer)	
I2c_4		0x48	TMP75#1	SMB
		0x49	TMP75#2	
		0x4A	TMP75#3	
		0x4B	TMP75#4	
		0x4C	TMP421 for intake air	
		0x4E	TMP421 for intake air	
		0x4F	TMP422/ TH3 remote temp	
I2c_5		0x54	OCP debug card	SMB
		0X27	TCA9555	SMB
I2C_6		0x60	DOM_FPGA_2	SMB
I2c_7		0x21	PCA9534 (8-bit Borad ID)	SMB
		0x20	PCA9535 (LEDs)	RackMon
		0x51	24C64 (SMB_Inv)	SMB

I2c_8		0x20	SLB9645 (TPM)	SMB
I2c_9		0x70	PCA9548	SMB
I2c_9 0x70 I2C Switch	Channel1, 0x01	0x58	AC PSU1 MCU/DC PSU 1 Hot swap	SMB
		0x50	EEPROM	
		0x18	PEM 1 Thermal sensor	
	Channel2, 0x02	0x58	AC PSU2 MCU/DC PSU 2 Hot swap	
		0x50	EEPROM	
		0x18	PEM 1 Thermal sensor	
	Channel3, 0x4	0x50	24c02 (BMC RGMII PHY BCM54616S EEPROM)	
	Channel4, 0x8	0x50	24c02 (BMC MDI PHY BCM54616S EEPROM)	
	Channel5, 0x10	0x54	24c64 (TH3 EEPROM IP_BSC0)	
	Channel6, 0x20		Reserved PWR_CPLD_I2C_Programming	
	Channel8, 0x80	0x3e	PWR_CPLD	
I2c_10		0x74	SI5391 (TH3 156.25MHz Clock)	
I2c_11			PTP (Reserved)	PTP
I2c_12		0x70	PCA9548	FCM
I2c_12 0x70 I2C Switch	Channel1, 0x01	0x3e	FAN CPLD	FCM
	Channel2, 0x02	0x51	24c02 (FCB Inv)	
	Channel3, 0x04	0x48	TMP75	
		0x49	TMP75	
	Channel4, 0x08	0x10	ADM1278	
	Channel5, 0x10	0x52	24c64 (Fan#1)	FAN-Trays
	Channel6, 0x20	0x52	24c64 (Fan#2)	
	Channel7, 0x40	0x52	24c64 (Fan#3)	
	Channel8, 0x80	0x52	24c64 (Fan#4)	
I2c_13		0x3E	SMB SYS CPLD	SMB
I2c_14		0x60	DOM_FPGA_1	SMB

5.7.4. BMC SPI diagram

BMC's SPI#0 is used to upgrade FWs/images. Here are the SPI devices connected to BMC's SPI#0 and the chip select functionality implemented in SMB sys_CPLD.
SPI devices on SMB:

- 2 pcs of FPGA flash W25Q128
- Switching ASIC flash W25Q257
- BCM5396's SPI EEPROM 93C46
- BMC's SPI EEPROM 93C46
- SPI device on SCM:
- Backup BIOS flash W25Q128

The following diagram shows SPI connections in W400:

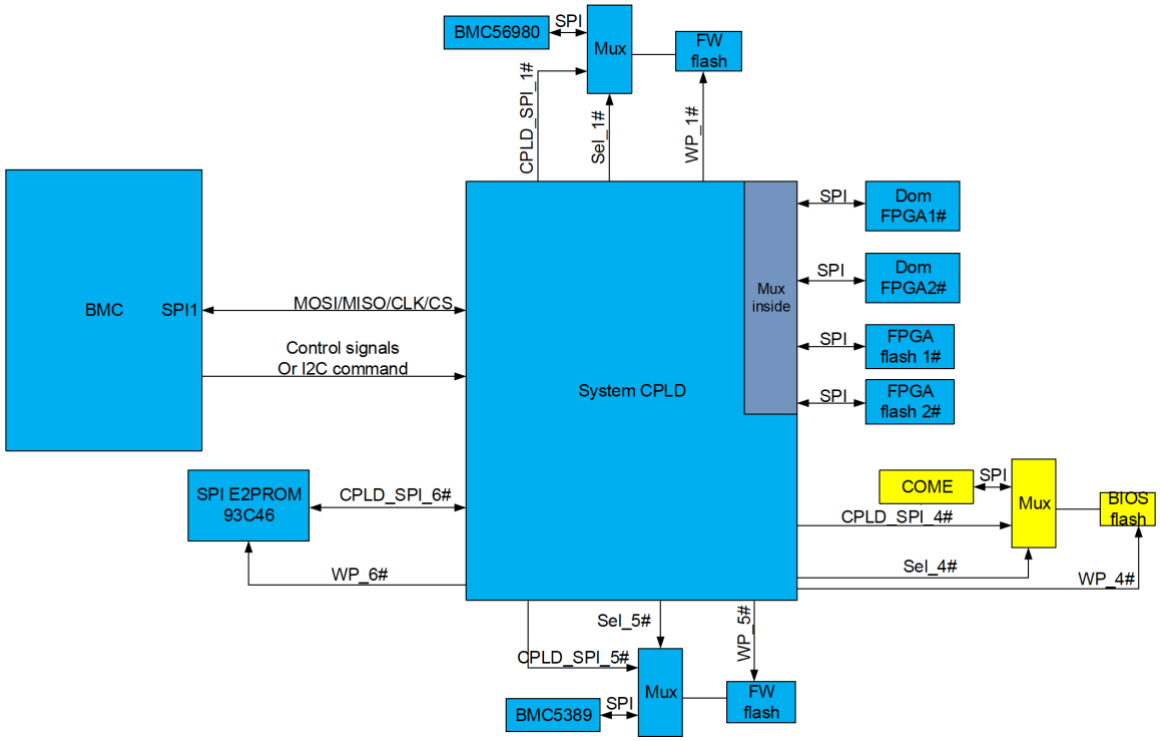


Figure 21:SPI Diagram

5.7.5. PWR_CPLD Registers

PWR_CPLD is a dedicated CPLD to implement the functionality of power cycling the whole system. BMC configures the registers of PWR_CPLD and the system will be powered off for a certain period and then powered on automatically. Here is an example of CPLD diagram:

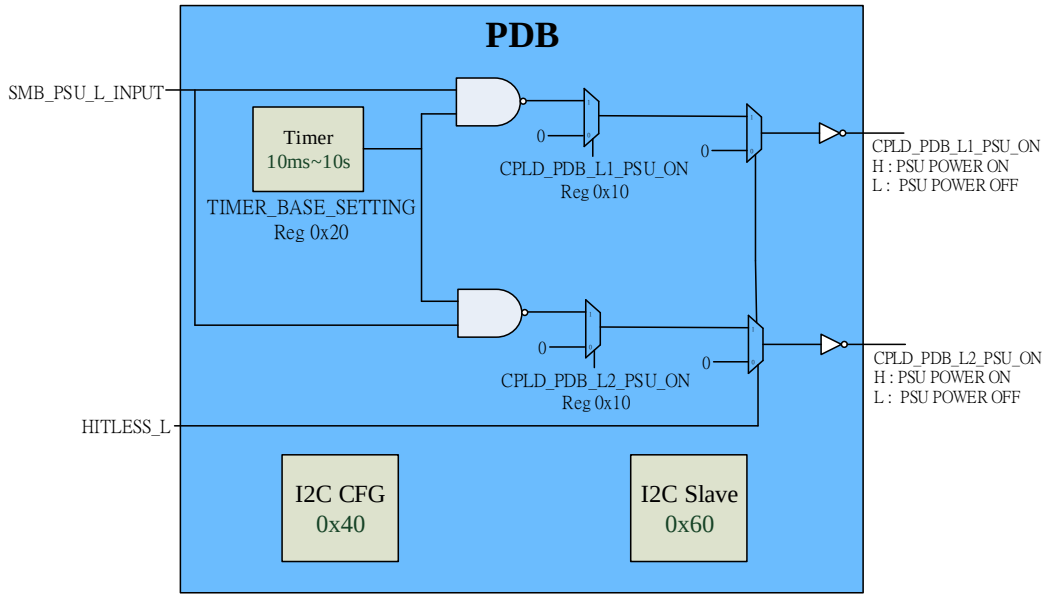


Figure 22:SPI Diagram

CPLD Registers		
Offset	Name	Description
0x01	CPLD_VERSION	CPLD Version Register
0x02	CPLD_SUB_VERSION	CPLD Sub Version Register
0x10	SYSTEM_MISC_1	System Misc 1 Register
0x11	SYSTEM_MISC_2	System Misc 2 Register
0x20	TIMER_BASE_SETTING	Timer Base Setting Register
0x21	TIMER_COUNTER_SETTING	Timer Counter setting Register
0x22	TIMER_COUNTER_STATE	Timer Counter State Register
0x23	TIMER_MISC	Timer Misc Register

Register 0x01: CPLD_VERSION – CPLD Version Register

Table 3 – CPLD Version Register

Bit #	Name	R/W	Reset Value	Description
[7]	Reserved	R		
[6]	RELEASE_STA	R		Released Bit 0= not released, 1= Released version after PVT
[5:0]	CPLD_VER	R		CPLD Revision[5:0]

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register

Table 4 – CPLD Sub Version Register

Bit #	Name	R/W	Reset Value	Description
[7:0]	CPLD_SUB_VERSION	R		CPLD sub-version, used for HW debug only

Register 0x10 SYSTEM_MISC_1 – System Misc 1 Register

Table 5 – System Misc 1 Register

Bit #	Name	R/W	Default Value	Description
[7:2]	Reseved			
[1]	CPLD_PSU2_ON	R/W	1	0: L2/R2 PSU2 POWER OFF 1: L2/R2 PSU2 POWER ON
[0]	CPLD_PSU1_ON	R/W	1	0: L1/R1 PSU1 POWER OFF 1: L1/R1 PSU1 POWER ON

Register 0x11 SYSTEM_MISC_2 – System Misc 2 Register

Table 6 – System Misc 2 Register

Bit #	Name	R/W	Default Value	Description
[7:4]	Reserved			
[3]	CPLD_PSU2_PG	R	1	1: Normal 0:Fail
[2]	CPLD_PSU1_PG	R	1	1: Normal 0:Fail
[1:0]	Reserved	R	0x3	

Register 0x20 TIMER_BASE_SETTING – Timer Base Setting Register

Table 7 – Timer Base Setting Register

Bit #	Name	R/W	Default Value	Description
[7:4]	Reserved			
[3]	TIMER_BASE_10s	R/W	0	Timer base 10s, (Note: This value needs 0x23[1] to update)
[2]	TIMER_BASE_1s	R/W	0	Timer base 1s, (Note: This value needs 0x23[1] to update)
[1]	TIMER_BASE_100ms	R/W	1	Timer base 100ms, (Note: This value needs 0x23[1] to update)
[0]	TIMER_BASE_10ms	R/W	0	Timer base 10ms, (Note: This value needs 0x23[1] to update)

Register 0x21: TIMER_COUNTER_SETTING – Timer Counter setting Register

Table 8 – Timer Counter Setting Register

Bit #	Name	R/W	Default Value	Description
[7:0]	TIMER_COUNTER_SETTING	R/W	0xFF	This timer is used for power up automatically, When counter down to zero, the power will repower up.

				(Note: This value needs 0x23[1] to update)

Register 0x22 TIMER_COUNTER_STATE – Timer Counter State Register

Table 9 – Timer Counter State Register

Bit #	Name	R/W	Default Value	Description
[7:0]	TIMER_COUNTER_STATE	R		The counter state

Register 0x23: TIMER_MISC – Timer Misc Register

Table 10 – Timer Misc Register

Bit #	Name	R/W	Reset Value	Description
[7:2]	Reserved			
[1]	TIMER_COUNTER_SETTING_UPDATE	R/W	0	0: No Update 1: Update the 0x21 and 0x20 TIMER_BASE_SETTING TIMER_COUNTER_SETTING
[0]	POWER_CYCLE_GO	R/W	0	0: No power cycle 1: Start the power cycle

5.7.6. SMB sys_CPLD Registers

Here are the main functionalities of system CPLD on SMB:

- All the major components power/reset sequence and controlling through reset registers;
- SCM/PSU/FCM present status access through registers;
- Control I/O signals on SMB board through register reads/writes, like Write protection pins, enable/disable pins, Programming pins, UART selection pins, SPI chip selection pins, etc;
- Control FPGA init and CPU reset sequence;
- Interrupt status/masks controlling through registers;
- SFP/SFP+ of OOB status controlling;
- UART selections;
- Support hitless programming; (This is general requirement for all the CPLDs.)
- Other clue logics.

Two identical FPGA share the same image to shorten programming time, so this CPLD needs to take care of this unique requirement. CPLD needs to allow the FPGA to be initialized one by one, from the same SPI flash, then reset release CPU, so both FPGA can get their PCI enumerated properly.

CPLD Registers		
Offset	Name	Description
0x00	SYSPLD_REG_BOARD_INFO	

0x01	SYSPLD_REG_PLD_VERSION	
0x02	SYSPLD_REG_PLD_SUB_VERSION	
0x03	SYSPLD_REG_PSU_STATUS	
0x05	SYSPLD_REG_SYSTEM_RST_1	
0x06	SYSPLD_REG_SYSTEM_RST_2	
0x07	SYSPLD_REG_SYSTEM_RST_3	
0x10	SYSPLD_REG_SYSTEM_INT_1	
0x11	SYSPLD_REG_SYSTEM_INT_2	
0x12	SYSPLD_REG_SYSTEM_INT_3	
0x20	SYSPLD_REG_SYSTEM_INT_MASK_1	
0x21	SYSPLD_REG_SYSTEM_INT_MASK_2	
0x22	SYSPLD_REG_SYSTEM_INT_MASK_3	
0x30	SYSPLD_REG_SYSTEM_INT_STA_1	
0x31	SYSPLD_REG_SYSTEM_INT_STA_2	
0x32	SYSPLD_REG_SYSTEM_INT_STA_3	
0x39	SYSPLD_REG_PORT_LED_TEST	
0x3A	SYSPLD_REG_UART_MUX	
0x40	SYSPLD_REG_MISC_BMC	
0x41	SYSPLD_REG_MISC_1	
0x42	SYSPLD_REG_MISC_2	
0x43	SYSPLD_REG_MISC_PWR_1	
0x44	SYSPLD_REG_MISC_PWR_2	
0x45	SYSPLD_REG_MISC_PWR_3	
0x46	SYSPLD_REG_MAC_ROV	
0x47	SYSPLD_REG_FPGA_INITIAL	
0x48	SYSPLD_REG_SPI_MUX_1	
0x4A	REG_BMC_RESERVE_1	
0x4B	REG_BMC_RESERVE_2	
0x4C	REG_BMC_RESERVE_3	
0x4D	Rack_Mon IO control_1	
0x4E	Rack_Mon IO control_2	
0x4F	Rack_Mon IO control_3	
0x50	CPLD_FPGA IO control_1	
0x51	CPLD_FPGA IO control_2	
0x52	CPLD_FPGA IO control_3	

Register 0x01: Board_VERSION – Board Version Register

Table 11 – CPLD Board Version Register

Bit #	Name	R/W	Reset Value	Description
[7-2]	Reserved	R		
[1:0]	Board_Version	R		Board Version[1:0]

Register 0x01: CPLD_VERSION – CPLD Version Register

Table 12 – CPLD Version Register

Bit #	Name	R/W	Reset Value	Description
[7]	Reserved	R		
[6]	RELEASE_STA	R		Released Bit 0= not released, 1= Released version after PVT
[5:0]	CPLD_VER	R		CPLD Revision[5:0]

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register

Table 13 – CPLD Sub Version Register

Bit #	Name	R/W	Reset Value	Description
[7:0]	CPLD_SUB_VERSION	R		CPLD sub-version, used for HW debug only

Register 0x03 SYSPLD_REG_PSU_STATUS

Table 14 – SYSPLD_REG_PSU_STATUS Register

Bit #	Name	R/W	Default Value	Description
[7:4]	Reseved	R		
[3]	PSU2_ACOK	R		1: PSU input OK. When AC PSU, means AC input, when PEM, means 12V input. 0: PSU input Not OK.
[2]	PSU1_ACOK	R		1: PSU input OK. When AC PSU, means AC input, when PEM, means 12V input. 0: PSU input Not OK.
[1]	PSU2_PWROK	R		1: PSU DC output OK. 0: PSU DC output Not OK.
[0]	PSU1_PWROK	R		1: PSU DC output OK. 0: PSU DC output Not OK.

Register 0x5 SYSPLD_REG_SYSTEM_RST_1

Table 15 – SYSPLD_REG_SYSTEM_RST_1 Register

Bit #	Name	R/W	Default Value	Description

[7]	SI5391B_RST_N	R/W	1	CLK buffer reset. Low active.
[6]	USBHUB_RST_N	R/W	1	USB bridge reset. Low active.
[5]	BMC_LPCRST_N	R/W	1	BMC_LPC reset. Low active.
[4]	BMC_PHY_2_RST_N	R/W	1	OOB front panel Phy reset. Low active.
[3]	BMC_PHY_1_RST_N	R/W	1	OOB RGMII Phy reset. Low active.
[2]	BCM5389_RESETB_N	R/W	1	OOB switch reset. Low active.
[1]	MAC_PCIE_PERST_L	R/W	1	TH3 PCIE reset. Low active.
[0]	MAC_RESET_N	R/W	1	TH3 reset. Low active.

Register 0x6 SYSPLD_REG_SYSTEM_RST_2

Table 16 – SYSPLD_REG_SYSTEM_RST_2 Register

Bit #	Name	R/W	Default Value	Description
[7]	FT232_RESET_N	R/W	1	FT232_RESET. Low active.
[6]	TPM_RST_N	R/W	1	TPM module reset. Low active.
[5]	SCM_CPLD_RESET	R/W	1	SCM CPLD reset. Low active.
[4]	FCM_CPLD_RST	R/W	1	FCB board reset. Low active.
[3]	FCM_PCA9548_RST	R/W	1	FCB board 9548 reset. BMC I2C bus 9. Low active.
[2]	PCA9534_RST_N	R/W	1	SMB board 9548 reset. BMC I2C bus 14. Low active.
[1]	PCA9535_RST_N	R/W	1	SMB board 9548 reset. BMC I2C bus 10. Low active.
[0]	PCA9548A_2_RESET_N	R/W	1	SMB board 9548 reset. BMC I2C bus 9. Low active.

Register 0x7 SYSPLD_REG_SYSTEM_RST_3

Table 17 – SYSPLD_REG_SYSTEM_RST_3 Register

Bit #	Name	R/W	Default Value	Description
[7:2]	Reseved			
[1]	DOM_FPGA2_RST_IN	R/W	1	DOM_FPGA2_RST. Low active.
[0]	DOM_FPGA1_RST_IN	R/W	1	DOM_FPGA1_RST. Low active.

Register 0x10 SYSPLD_REG_SYSTEM_INT_1

Table 18 – SYSPLD_REG_SYSTEM_INT_1 Register

Bit #	Name	R/W	Default Value	Description
[7]	PSU_ALERT_2_L	RC	1	SCM_CPLD Interrupt 0: Status changed from last read 1: Status not changed
[6]	PSU_ALERT_1_L	RC	1	FCB_CPLD Interrupt 0: Status changed from last read 1: Status not changed
[5]	SCM_CPLD_Int	RC	1	SCM_CPLD Interrupt 0: Status changed from last read 1: Status not changed
[4]	FCB_CPLD_Int	RC	1	FCB_CPLD Interrupt 0: Status changed from last read 1: Status not changed
[3]	TEMP_SENSOR_CPLD_ALERT4	RC	1	Thermal sensor int_4 0: Status changed from last read 1: Status not changed
[2]	TEMP_SENSOR_CPLD_ALERT3	RC	1	Thermal sensor int_3 0: Status changed from last read 1: Status not changed
[1]	TEMP_SENSOR_CPLD_ALERT2	RC	1	Thermal sensor int_2 0: Status changed from last read 1: Status not changed
[0]	TEMP_SENSOR_CPLD_ALERT1	RC	1	Thermal sensor int_1 0: Status changed from last read 1: Status not changed

Register 0x11 SYSPLD_REG_SYSTEM_INT_2

Table 19 – SYSPLD_REG_SYSTEM_INT_2

Bit #	Name	R/W	Default Value	Description
[7]	PSU_PRNST_2_N	RC	1	PSU 2 present interrupts.
[6]	PSU_PRNST_1_N	RC	1	PSU 1 present interrupts.
[5]	SCM_PRESET	RC	1	SCM present interrupts.
[4]	DEBUG_PRESENT_N	RC	1	DEBUG card present interrupts.
[3]	MAC_CPLD_PCIE_WAKE_L	RC	1	PCIE Wake interrupt
[2]	SMB_TPM_INT_N	RC	1	TPM I2C INTR
[1]	MAC_CPLD_PCIE_INTR_L	RC	1	PCIE_INTR
[0]	TPM_PP	RC	1	TPM PP interrupt

Register 0x12 SYSPLD_REG_SYSTEM_INT_3

Table 20 – SYSPLD_REG_SYSTEM_INT_3 Register

Bit #	Name	R/W	Default Value	Description
[7]	FAULT_R_XP5R0V_USB	RC	1	USB XP5R0V fault interrupts
[6]	XP5R0V_PG	RC	1	XP5R0V power good interrupts.
[5]	BMC_POWER_OK	RC	1	BMC all power rails power ok interrupts.
[4]	TH3_POWER_OK	RC	1	TH3 all power rails power ok interrupts.
[3]	PSU_ACOK_2	RC	1	PSU2 AC Input power ok interrupts.
[2]	PSU_ACOK_1	RC	1	PSU1 AC Input power ok interrupts.
[1]	PSU_PWROK_2	RC	1	PSU2 DC output power ok interrupts.
[0]	PSU_PWROK_1	RC	1	PSU1 DC output power ok interrupts.

Register 0x20 SYSPLD_REG_SYSTEM_INT_Mask_1

Table 21 – SYSPLD_REG_SYSTEM_INT_Mask_1 Register

Bit #	Name	R/W	Default Value	Description
[7]	PSU_ALERT_2_L mask	R/W	1	SCM_CPLD Interrupt mask 1: mask 0: Don't mask
[6]	PSU_ALERT_1_L mask	R/W	1	FCB_CPLD Interrupt mask 1: mask 0: Don't mask
[5]	SCM_CPLD_Int mask	R/W	1	SCM_CPLD Interrupt mask 1: mask 0: Don't mask
[4]	FCB_CPLD_Int mask	R/W	1	FCB_CPLD Interrupt mask 1: mask 0: Don't mask
[3]	TEMP_SENSOR_CPLD_ALERT4 mask	R/W	1	Thermal sensor int_4 mask 1: mask 0: Don't mask
[2]	TEMP_SENSOR_CPLD_ALERT3 mask	R/W	1	Thermal sensor int_3 mask 1: mask 0: Don't mask
[1]	TEMP_SENSOR_CPLD_ALERT2 mask	R/W	1	Thermal sensor int_2 mask 1: mask 0: Don't mask
[0]	TEMP_SENSOR_CPLD_ALERT1 mask	R/W	1	Thermal sensor int_1 mask 1: mask 0: Don't mask

Register 0x21 SYSPLD_REG_SYSTEM_INT_Mask_2

Table 22 – SYSPLD_REG_SYSTEM_INT_Mask_2 Register

Bit #	Name	R/W	Default Value	Description
[7]	PSU_PRNST_2_N mask	R/W	1	PSU 2 present interrupts mask
[6]	PSU_PRNST_1_N mask	R/W	1	PSU 1 present interrupts mask
[5]	SCM_PRESET mask	R/W	1	SCM present interrupts mask
[4]	DEBUG_PRESENT_N mask	R/W	1	DEBUG card present interrupts mask
[3]	MAC_CPLD_PCIE_WAKE_L mask	R/W	1	PCIE Wake interrupt mask
[2]	SMB_TPM_INT_N mask	R/W	1	TPM I2C INTR mask
[1]	MAC_CPLD_PCIE_INTR_L mask	R/W	1	PCIE_INTR mask
[0]	TPM_PP mask	R/W	1	TPM PP interrupt mask

Register 0x22 SYSPLD_REG_SYSTEM_INT_Mask_3

Table 23 – SYSPLD_REG_SYSTEM_INT_Mask_3 Register

Bit #	Name	R/W	Default Value	Description
[7]	FAULT_R_XP5R0V_USB mask	R/W	1	USB XP5R0V fault interrupts mask
[6]	XP5R0V_PG mask	R/W	1	XP5R0V power good interrupts mask
[5]	BMC_POWER_OK mask	R/W	1	BMC all power rails power ok interrupts mask
[4]	TH3_POWER_OK mask	R/W	1	TH3 all power rails power ok interrupts mask
[3]	PSU_ACOK_2 mask	R/W	1	PSU2 AC Input power ok interrupts mask
[2]	PSU_ACOK_1 mask	R/W	1	PSU1 AC Input power ok interrupts mask
[1]	PSU_PWROK_2 mask	R/W	1	PSU2 DC output power ok interrupts mask
[0]	PSU_PWROK_1 mask	R/W	1	PSU1 DC output power ok interrupts mask

Register 0x30 SYSPLD_REG_SYSTEM_INT_Status_1

Table 24 – SYSPLD_REG_SYSTEM_INT_Status_1 Register

Bit #	Name	R/W	Default Value	Description
[7]	PSU_ALERT_2_L Status	R	1	SCM_CPLD Interrupt Status 0: PSU has interrupts 1: Not interrupts
[6]	PSU_ALERT_1_L Status	R	1	FCB_CPLD Interrupt Status 0: PSU has interrupts 1: Not interrupts
[5]	SCM_CPLD_Int Status	R	1	SCM_CPLD Interupt Status 0: SCM has interrupts 1: Not interrupts
[4]	FCB_CPLD_Int Status	R	1	FCB_CPLD Interupt Status 0: FCB has interrupts 1: Not interrupts
[3]	TEMP_SENSOR_ CPLD_ALERT4 Status	R	1	Thermal sensor int_4 Status 0: Sensor has interrupts 1: Not interrupts
[2]	TEMP_SENSOR_ CPLD_ALERT3 Status	R	1	Thermal sensor int_3 Status 0: Sensor has interrupts 1: Not interrupts
[1]	TEMP_SENSOR_ CPLD_ALERT2 Status	R	1	Thermal sensor int_2 Status 0: Sensor has interrupts 1: Not interrupts
[0]	TEMP_SENSOR_ CPLD_ALERT1 Status	R	1	Thermal sensor int_1 Status 0: Sensor has interrupts 1: Not interrupts

Register 0x31 SYSPLD_REG_SYSTEM_INT_ Status _2

Table 25 – SYSPLD_REG_SYSTEM_INT_ Status _2 Register

Bit #	Name	R/W	Default Value	Description
[7]	PSU_PRNST_2_N Status	R	1	PSU 2 present interrupts Status 0: PSU present 1: PSU not present
[6]	PSU_PRNST_1_N Status	R	1	PSU 1 present interrupts Status 0: PSU present 1: PSU not present
[5]	SCM_PRESET Status	R	1	SCM present interrupts Status 0: SCM present 1: SCM not present
[4]	DEBUG_PRESEN T_N Status	R	1	DEBUG card present interrupts Status 0: Debug card present 1: Debug card not present

[3]	MAC_CPLD_PCIE_WAKE_L Status	R	1	PCIE Wake interrupt Status 0: PCIE Wake status 1: PCIE Not Wake status
[2]	SMB_TPM_INT_N Status	R	1	TPM I2C INTR Status 0: TPM I2C has interrupt 1: TPM I2C has not interrupt
[1]	MAC_CPLD_PCIE_INTR_L Status	R	1	PCIE_INTR Status 0: TH3 PCIE has interrupt 1: TH3 PCIE has not interrupt
[0]	TPM_PP Status	R	1	TPM PP interrupt Status 0: TPM PP has interrupt 1: TPM PP has not interrupt

Register 0x32 SYSPLD_REG_SYSTEM_INT_ Status_3

Table 26 – SYSPLD_REG_SYSTEM_INT_ Status_3 Register

Bit #	Name	R/W	Default Value	Description
[7]	FAULT_R_XP5R0V_USB Status	R	1	USB XP5R0V fault interrupts Status
[6]	XP5R0V_PG Status	R	1	XP5R0V power good interrupts Status
[5]	BMC_POWER_OK Status	R	1	BMC all power rails power ok interrupts Status
[4]	TH3_POWER_OK Status	R	1	TH3 all power rails power ok interrupts Status
[3]	PSU_ACOK_2 Status	R	1	PSU2 AC Input power ok interrupts Status
[2]	PSU_ACOK_1 Status	R	1	PSU1 AC Input power ok interrupts Status
[1]	PSU_PWROK_2 Status	R	1	PSU2 DC output power ok interrupts Status
[0]	PSU_PWROK_1 Status	R	1	PSU1 DC output power ok interrupts Status

Register 0x39 SYSPLD_REG_PORT_LED_TEST

Table 27 – SYSPLD_REG_PORT_LED_TEST Register

Bit #	Name	R/W	Default Value	Description
[7:4]	Reserved			
[3]	LED Test enable	R/W	0	1: Test mode, LED manual control. 0: LED control by FPGA LED stream.
[2]	LED_Green	R/W	0	1: All Led Green on. 0: All Led Green off.
[1]	LED_Blue	R/W	0	1: All Led Blue on.

				0: All Led Blue off.
[0]	LED_Red	R/W	0	1: All Led Red on. 0: All Led Red off.

Register 0x3A SYSPLD_UART selection

Table 28 – SYSPLD_UART selection Register

Bit #	Name	R/W	Default Value	Description
[7:6]	Debug UART Selection	R/W	0	REAR_DBG_UART selection 00: Tomahawk UART-0 01: Tomahawk UART-2 10: Tomahawk UART-3 11: reserved
[5:2]	Reserved	R/W	0	1: All Led Blue on. 0: All Led Blue off.
[1:0]	UART Selection	R/W	10	00: UART_SELECT_BMC (BMC_UART_SEL5 signal controls UART selection) 01: UART_SELECT_DBG (USB_UART_SEL from META USB Debug controls UART selection) 10: force to select 0 11: force to select 1 UART_SEL 1: UART port of COMe connect to BMC UART-5, and META USB Debug UART connect to BMC UART-2 0: UART port of COMe connect to META USB Debug UART,

Register 0x40 SYSPLD_REG_MISC_BMC

Table 29 – SYSPLD_REG_MISC_BMC Register

Bit #	Name	R/W	Default Value	Description
[7]	CPLD_56980_QSPI_WP_N	R/W	1	TH3 PCIE FW E2PROM WP
[6]	CPLD_BMC_SPI_1_WP_N	R/W	1	BMC SPI 1 Flash WP
[5]	CPLD_BMC_PHY1_WP	R/W	1	PHY1 E2 WP
[4]	CPLD_BMC_SPI_2_WP_N	R/W	1	BMC SPI 2 Flash WP

[3]	CPLD_BMC_PHY2_WP	R/W	1	PHY1 E2 WP
[2]	SCM_SPI_WP_N	R/W	1	COME BIOS WP
[1]	FPGA1_SPI_WP_N	R/W	1	FPGA SPI E2PROM WP
[0]	FPGA2_SPI_WP_N	R/W	1	FPGA SPI E2PROM WP

Register 0x41 SYSPLD_REG_MISC_1

Table 30 – SYSPLD_REG_MISC_1 Register

Bit #	Name	R/W	Default Value	Description
[7:5]	Reserved	R/W	0	
[4]	CPLD_USB_MUX_SEL1	R/W	0	
[3]	CPLD_USB_MUX_SEL0	R/W	0	
[2]	USB_EN3	R/W	1	
[1]	USB_EN2	R/W	1	
[0]	USB_EN1	R/W	1	

Register 0x42 SYSPLD_REG_MISC_2

Table 31 – SYSPLD_REG_MISC_2 Register

Bit #	Name	R/W	Default Value	Description
[7:4]	Reserved		1	
[3]	XP5R0V_USB_EN	R/W	1	
[2]	SCM_POWER_ENABLE	R/W	1	
[1]	FCM_3R3V_EN	R/W	1	
[0]	TH3_TURN_ON	R/W	0	

Register 0x43 SYSPLD_REG_MISC_PWR_1

Table 32 – SYSPLD_REG_MISC_PWR_1 Register

Bit #	Name	R/W	Default Value	Description
[7:6]	Reserved	R		
[5]	XP1R15V_BMC_PG	R		1: Power good. 2. Power off or power failure
[4]	XP3R3V_BMC_PG	R		1: Power good. 2. Power off or power failure
[3]	XP2R5V_BMC_PG	R		1: Power good. 2. Power off or power failure

[2]	XP1R2V_BMC_PG	R		1: Power good. 2. Power off or power failure
[1]	XP5R0V_PG	R		1: Power good. 2. Power off or power failure
[0]	XP3R3V_1220_PG	R		1: Power good. 2. Power off or power failure

Register 0x44 SYSPLD_REG_MISC_PWR_2

Table 33 – SYSPLD_REG_MISC_PWR_2 Register

Bit #	Name	R/W	Default Value	Description
[7:6]	Reserved	R		
[5]	XP3R3V_Optical_Right_PG	R		1: Power good. 2. Power off or power failure
[4]	XP3R3V_Optical_Left_PG	R		1: Power good. 2. Power off or power failure
[3]	USB_OC_PG	R		1: Power good. 2. Power off or power failure
[2]	XP1R0V_FPGA_PG	R		1: Power good. 2. Power off or power failure
[1]	XP1R8V_FPGA_PG	R		1: Power good. 2. Power off or power failure
[0]	XP3R3V_FPGA_PG	R		1: Power good. 2. Power off or power failure

Register 0x45 SYSPLD_REG_MISC_PWR_3

Table 34 – SYSPLD_REG_MISC_PWR_3 Register

Bit #	Name	R/W	Default Value	Description
[7]	Reserved	R		
[6]	Reserved	R		
[5]	Reserved	R		
[4]	XP3R3V_TH3_PG	R		1: Power good. 2. Power off or power failure
[3]	TRVDD_TH3_PG	R		1: Power good. 2. Power off or power failure
[2]	VDDCore_TH3_PG	R		1: Power good. 2. Power off or power failure
[1]	XP1R8V_TH3_PG	R		1: Power good. 2. Power off or power failure
[0]	XP1R2V_TH3_PG	R		1: Power good. 2. Power off or power failure

Register 0x46 SYSPLD_REG_MAC_ROV

Table 35 – SYSPLD_REG_MAC_ROV Register

Bit #	Name	R/W	Default Value	Description
[7]	ROV_7	R		TH3 ROV_7 Value
[6]	ROV_6	R		TH3 ROV_6 Value
[5]	ROV_5	R		TH3 ROV_5 Value
[4]	ROV_4	R		TH3 ROV_4 Value
[3]	ROV_3	R		TH3 ROV_3 Value
[2]	ROV_2	R		TH3 ROV_2 Value
[1]	ROV_1	R		TH3 ROV_1 Value
[0]	ROV_0	R		TH3 ROV_0 Value

Register 0x47 SYSPLD_REG_FPGA_Initial

Table 36 – SYSPLD_REG_FPGA_Initial Register

Bit #	Name	R/W	Default Value	Description
[7]	Reserved			
[6]	Reserved			
[5]	DOM_FPGA2_PROGRAM	R/W	1	TBD
[4]	DOM_FPGA1_PROGRAM	R/W	1	TBD
[3]	DOM_FPGA2_Initial	R/W	1	TBD
[2]	DOM_FPGA1_Initial	R/W	1	TBD
[1]	DOM_FPGA2_Done	R		1: DOM_FPGA2 load image finished. 0: DOM_FPGA load image not finished.
[0]	DOM_FPGA1_Done	R		1: DOM_FPGA2 load image finished. 0: DOM_FPGA load image not finished.

Register 0x48 SYSPLD_REG_SPI_MUX_1

Table 37 – SYSPLD_REG_SPI_MUX_1 Register

Bit #	Name	R/W	Default Value	Description
[7:3]	Reserved	R	0	
[2:0]	BIOS_Sel	R/W	0	00h: BMC Select the System_E2. 01h: BMC Select the BIOS. 02h: BMC Select the BCM5389 E2. 03h: BMC Select the TH3 PCIE E2. 04h: BMC Select the FPGA1 flash. 05h: BMC Select the FPGA2 flash. Others: Reserved

Register 0x4A REG_BMC_RESERVE_1

Table 38 – REG_BMC_RESERVE_1 Register

Bit #	Name	R/W	Default Value	Description
[7:0]	RacK_Mon_R[8:1]	R		Rack_Mon value input value

Register 0x4B REG_BMC_RESERVE_2

Table 39 – REG_BMC_RESERVE_2 Register

Bit #	Name	R/W	Default Value	Description
[7:0]	RacK_Mon_W[8:1]	R/W		Rack_Mon value Output value

Register 0x4C REG_BMC_RESERVE_3

Table 40 – REG_BMC_RESERVE_3 Register

Bit #	Name	R/W	Default Value	Description
[7:0]	RacK_Mon_EN[8:1]	R/W	0	Rack_Mon value Output enables. 0: Output disables. 1: Output enables.

Register 0x4D Rack_Mon IO control_1

Table 41 – Rack_Mon IO control_1 Register

Bit #	Name	R/W	Default Value	Description
[7]	Reserved			
[6]	Reserved			
[5]	RMON_RF_3_input	R		RF/PF input value
[4]	RMON_PF_3_input	R		RF/PF input value
[3]	RMON_RF_2_input	R		RF/PF input value
[2]	RMON_PF_2_input	R		RF/PF input value
[1]	RMON_RF_1_input	R		RF/PF input value
[0]	RMON_PF_1_input	R		RF/PF input value

Register 0x4E Rack_Mon IO control_2

Table 42 – Rack_Mon IO control_2 Register

Bit #	Name	R/W	Default Value	Description
[7]	Reserved			
[6]	Reserved			

[5]	RMON_RF_3_output	R/W	0	RF/PF output value
[4]	RMON_PF_3_output	R/W	0	RF/PF output value
[3]	RMON_RF_2_output	R/W	0	RF/PF output value
[2]	RMON_PF_2_output	R/W	0	RF/PF output value
[1]	RMON_RF_1_output	R/W	0	RF/PF output value
[0]	RMON_PF_1_output	R/W	0	RF/PF output value

Register 0x4F Rack_Mon IO control_3

Table 43 – Rack_Mon IO control_3 Register

Bit #	Name	R/W	Default Value	Description
[7]	Reserved			
[6]	Reserved			
[5]	RMON_RF_3_output_en	R/W	0	RF/PF output enable 0: Output disables. 1: Output enables.
[4]	RMON_PF_3_output_en	R/W	0	
[3]	RMON_RF_2_output_en	R/W	0	
[2]	RMON_PF_2_output_en	R/W	0	
[1]	RMON_RF_1_output_en	R/W	0	
[0]	RMON_PF_1_output	R/W	0	

Register 0x50 CPLD_FPGA IO control_1

Table 44 – CPLD_FPGA IO control_1Register

Bit #	Name	R/W	Default Value	Description
[7]	FPGA2_CPLD_RESERED_4	R		FPGA_CPLD input value
[6]	FPGA2_CPLD_RESERED_3	R		FPGA_CPLD input value
[5]	FPGA2_CPLD_RESERED_2	R		FPGA_CPLD input value

[4]	FPGA2_CPLD_RESERED_1	R		FPGA_CPLD input value
[3]	FPGA1_CPLD_RESERED_4	R		FPGA_CPLD input value
[2]	FPGA1_CPLD_RESERED_3	R		FPGA_CPLD input value
[1]	FPGA1_CPLD_RESERED_2	R		FPGA_CPLD input value
[0]	FPGA1_CPLD_RESERED_1	R		FPGA_CPLD input value

Register 0x51 CPLD_FPGA IO control_2

Table 45 – CPLD_FPGA IO control_2Register

Bit #	Name	R/W	Default Value	Description
[7]	FPGA2_CPLD_RESERED_4_output	R/W	0	FPGA_CPLD output value
[6]	FPGA2_CPLD_RESERED_3_output	R/W	0	FPGA_CPLD output value
[5]	FPGA2_CPLD_RESERED_2_output	R/W	0	FPGA_CPLD output value
[4]	FPGA2_CPLD_RESERED_1_output	R/W	0	FPGA_CPLD output value
[3]	FPGA1_CPLD_RESERED_4_output	R/W	0	FPGA_CPLD output value
[2]	FPGA1_CPLD_RESERED_3_output	R/W	0	FPGA_CPLD output value
[1]	FPGA1_CPLD_RESERED_2_output	R/W	0	FPGA_CPLD output value
[0]	FPGA1_CPLD_RESERED_1_output	R/W	0	FPGA_CPLD output value

Register 0x52 CPLD_FPGA IO control_3

Table 46 – CPLD_FPGA IO control_3 Register

Bit #	Name	R/W	Default Value	Description
[7]	FPGA2_CPLD_RESERED_4_en	R/W	0	FPGA_CPLD output enable 0: Output disables. 1: Output enables.
[6]	FPGA2_CPLD_RESERED_3_en	R/W	0	
[5]	FPGA2_CPLD_RESERED_2_en	R/W	0	

[4]	FPGA2_CPLD_RESERED_1_en	R/W	0	
[3]	FPGA1_CPLD_RESERED_4_en	R/W	0	
[2]	FPGA1_CPLD_RESERED_3_en	R/W	0	
[1]	FPGA1_CPLD_RESERED_2_en	R/W	0	
[0]	FPGA1_CPLD_RESERED_1_en	R/W	0	

5.8. System Control Module (SCM)

The System Control Module (SCM) has the host COM-E CPU for Switching ASIC. The SCM support one Broadwell-DE COM-E CPU module.

5.8.1. System Control Module Block Diagram

The SCM has the following components:

- BW-DE COM-E CPU modules (a.k.a Minilake)
- one M.2 256GB NVMe SSD
- CPLD is used to provide control and management function for SCM
- One dedicated I2C management bus for SMB BMC to access SCM
- I2C bus to SMB

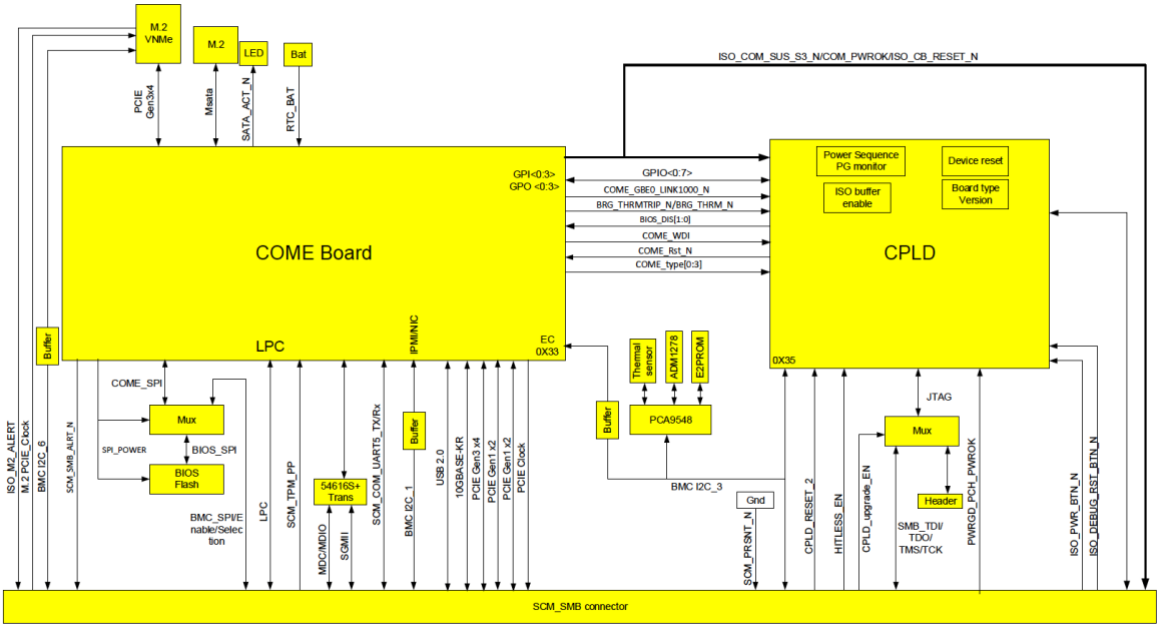


Figure 23:System Controller Module (SCM) block diagram

Figure 24:System Controller Module (SCM) top view

5.8.2. 10G KR interface

SCM reserves one pair of 10G KR signals to SMB. BW-DE COM-e CPU module supports extra 10G KR ethernet interface.

5.8.3. SCM LPC bus

The LPC bus of SCM COM-e CPU is extended across the high speed connector to access the LPC slave devices on SMB. The LPC is connected to BMC on SMB.

5.8.4. COM-Express CPU Module

COM-E CPU module is Meta MiniLake Type-7 COM-e CPU module. It has the following features:

- Processor
  - Intel® Broadwell-DW processor D1527, 14nm process node
  - Four-core, 2.2Ghz Base, 2.5Ghz Turbo, TDP 35W
  - Cache: L1(32K data,32K instruction/core), L2 256K/core, L3 1.5MB/core
  - 24x PCIe3, 6x SATA3, 4x USB3.0, 4x USB2.0
  - Support Intel® TXT technology
  - Up to DDR4-2133; SODIMM, UDIMM, RDIMM with ECC and non-ECC.
- BIOS
  - AMI BIOS
- Memory
  - Supports two SODIMM slots, each slot installs 16GB DDR4 SODIMM, up to 2133MT/s
- Storage Devices
  - One NVMe PCIe gen3 x4, M.2 SSD
- Watchdog Timer
  - Programmable by embedded controller
- Expansion Interface
  - Supports up to 8 PCI Express gen2 lanes, and up to 16 PCIe Gen3 lanes.
  - 1 SPI interface for BIOS on carrier board
  - 1 SM bus interface
  - 1 I2C interface
  - 1 LPC interface
- I/O Interface
  - 1 Ethernet - Onboard Intel I210IT
  - At least 1 serial port supported by onboard EC (Embedded Controller)
- USB
  - One USB2.0
- Mechanic and Environment
  - Dimension - 95mm(L) x 125mm(W) x 2.0mm(H)
- Power Supply - DC 12V only
- Wedge400 uses the following configuration:
  - Boot SPI Flash: 8Mbyte, secondary on SCM main board
  - M.2 PCIe NVMe SSD: 256Gbyte, physically located at SCM main board
  - Memory: 2*16Gbyte DDR4 ECC 1600 with thermal sensor, 240-pin SODIMM
  - BIOS: AMI UEFI
  - Ethernet: 1000GbaseT, BCM PHY on SCM main board to provide SGMII interface
  - PCIe: PCIe Gen3, x4 lanes are used for Switch ASIC PCIe access
  - PCIe: 2 ports PCIe Gen1/2 x2 lanes are used from SCM to SMB, will be used for the two DOM FPGAs access

- PCIe: PCIe Gen3, x4 lanes are used for M.2 NVMe SSD access
- USB port: USB 2.0 port is used for SMB USB interface
- WDT: programmable via SW from 1s to 255min
- LPC: LPC bus at 33.33Mhz

The following is the block diagram of COM-E module:

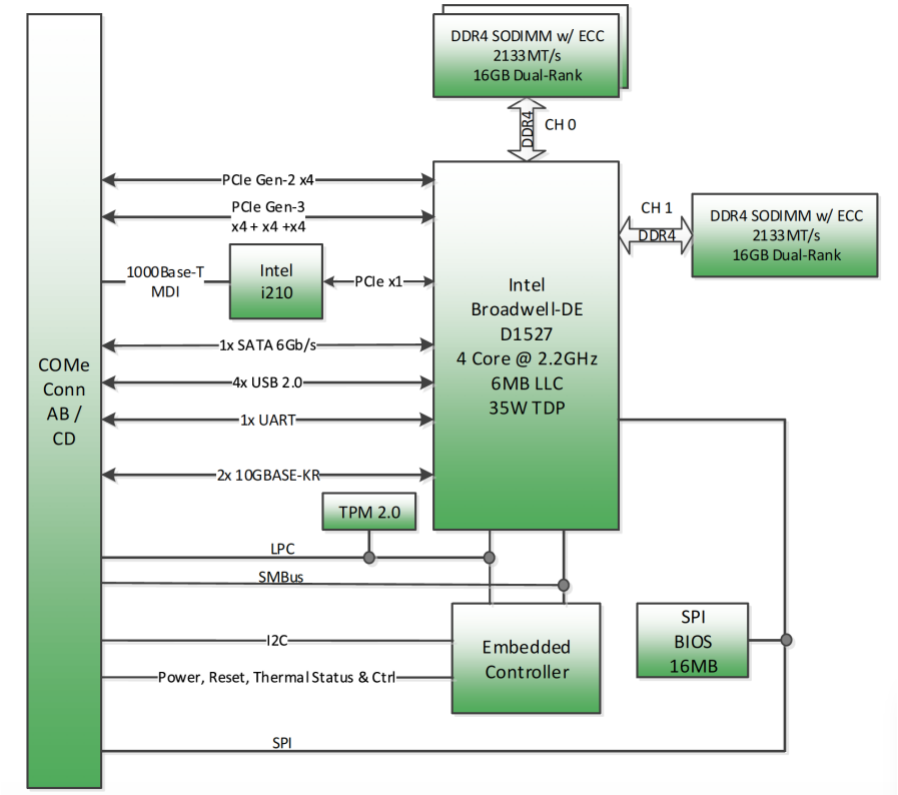


Figure 25:Meta MiniLake CPU Module Block Diagram

5.8.5. SCM Sys_CPLD Registers

Registers in SCM CPLD are accessed by BMC through I2C interface. Here are the definitions of the registers which should be in SCM Sys_CPLD.

CPLD Registers		
Offset	Name	Description
0x00	BOARD_INFO	Board Info Register
0x01	CPLD_VERSION	CPLD Version Register
0x02	CPLD_SUB_VERSION	CPLD Sub Version Register
0x0C	Watch Dog	Watch Dog Register
0x10	SCM_RST_CTRL	SCM Reset Control Register
0x11	COME_STA	COMe Status Register
0x12	COME_BIOS_DIS_CTRL	COMe Bios DIS Control Register
0x14	COME_PWR_CTRL_REG	COMe Power Control Register

0x21	SYSTEM_INTERRUPT	System Interrupt Register
0x28	SYSTEM_INTERRUPT_MASK	System Interrupt Mask Register
0x29	SYSTEM_INTERRUPT_STA	System Interrupt Status Register
0x30	SYSTEM_POWER_STUTS	System Power Status Register
0x31	SYSTEM_POWER_ENABLE	System Power Enable Register
0x32	SYSTEM_ISO	System ISO Register
0x34	THERMAL	Thermal Register
0x35	SYSTEM_MISC_1	System Misc_1 Register
0x36	SYSTEM_MISC_2	System Misc_2 Register
0x37	SYSTEM_MISC_3	System Misc_3 Register
0x38	SYSTEM_MISC_4	System Misc_4 Register
0x39	SYSTEM_MISC_5	System Misc_5 Register
0x3A	SYSTEM_MISC_6	System Misc_6 Register

Register 0x00: BOARD_INFO – Board Info Register

Table 47 – Board Version Register

Bit #	Name	R/W	Reset Value	Description
[7:3]	Reserved	NA		
[2:0]	PCB_Version	RO		000: R0A 001: R0B 010: R0C 011: R01 100: R02 101: R03 110: PVT1 110: PVT2 Others: Reserved

Register 0x01: CPLD_VERSION – CPLD Version Register

Table 48 – CPLD Version Register

Bit #	Name	R/W	Reset Value	Description
[7]	Reserved	RO	0	
[6]	RELEASE_STA	RO	0	Released Bit 0= not released, 1= Released version after PVT
[5:0]	CPLD_VER	RO	0	CPLD Revision[5:0]

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register

Table 49 – CPLD Sub Version Register

Bit #	Name	R/W	Reset Value	Description

[7:0]	CPLD sub-version	RO	0	used for HW debug only

Register 0x0C: Watch Dog – Watch Dog Register

Table 50 – Watch Dog Register

Bit #	Name	R/W	Default Value	Description
[7:1]	Reserved	NA	DA	Reserved
[0]	ISO_COM_BRG_WDT	RO		

Register 0x10: SCM_RST_CTRL – SCM Reset Control Register

Table 51 –SCM Reset Control Register

Bit #	Name	R/W	Default Value	Description
[7:5]	Reserved	NA	NA	Reserved
[4]	ISO_SMB_CB_RESET_N	R/W	1	0: write 0 to trigger System PCIE reset 1: normal
[3]	NVME_SSD_PERST	R/W	1	0: write 0 to trigger M.2 reset 1: normal
[2]	PCA9548_RST_N	R/W	1	0: write 0 to trigger PCA9548 reset 1: normal
[1]	CPLD_COM_PHY_RST_N	R/W	1	0: write 0 to trigger BCM54616S reset 1: normal
[0]	SYS_RESET_N	R/W	1	0: write 0 to trigger COMe reset 1: normal

Register 0x11: COME_STA – COMe Status Register

Table 52 – COMe Status Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved	NA		Reserved
[3]	ISO_COM_SUS_STAT_N	RO		COMe Module SUS_STAT_N Status
[2]	ISO_COM_SUS_S5_N	RO		COMe Module SUS_S5_N Status
[1]	ISO_COM_SUS_S4_N	RO		COMe Module SUS_S4_N Status
[0]	ISO_COM_SUS_S3_N	RO		COMe Module SUS_S3_N Status

Register 0x12: COME_BIOS_DIS_CTRL – COMe Bios DIS Control Register

Table 53 – COMe Bios DIS Control Register

Bit #	Name	R/W	Default Value	Description
[7:2]	Reserved	R/W		Reserved
[1]	COM_BIOS_DIS1_N	R/W	0	Control COMe BIOS DIS1
[0]	COM_BIOS_DIS0_N	R/W	0	Control COMe BIOS DIS0

Register 0x14: COME_PWR_CTRL_REG – COMe Power Control Register

Table 54 – COMe Power Control Register

Bit #	Name	R/W	Default Value	Description
[7:3]	Reserved		0	Reserved
[2]	come_pwr_ctrl_reg[2]	R/W	1	PWR_CYC_N Write 0 to this bit will trigger CPLD power cycling the COMe Module, This bit will auto set to 1 after Power Cycle finish.
[1]	come_pwr_ctrl_reg[1]	R/W	1	PWR_Force_off 0: COMe power is OFF 1: COMe power is ON
[0]	Come_pwr_ctrl_reg[0]	R/W	1	PWR_COME_EN 0: COMe power is OFF 1: COMe power is ON

Register 0x21: SYSTEM_INTERRUPT – System Interrupt Register

Table 55 – System Interrupt Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			
[5]	BCM54616S_INT_N	RC		1:No interrupt 0: Interrupt
[4]	LM75B_INT_N	RC		1:No interrupt 0: Interrupt
[3]	HOTSWAP_PG	RC		1:No interrupt 0: Interrupt
[2]	HS_ALERT2	RC		1:No interrupt 0: Interrupt
[1]	HS_ALERT1	RC		1:No interrupt 0: Interrupt
[0]	HS_FAULT_N	RC		1:No interrupt 0: Interrupt

Register 0x28: SYSTEM_INTERRUPT_MASK – System Interrupt Mask Register

Table 56 – System Interrupt Mask Register

Bit #	Name	R/W	Reset Value	Description

[7:6]	Reserved			Reserved
[5]	BCM54616S_INT_N_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
[4]	LM75B_INT_N_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
[3]	HOTSWAP_PG_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
[2]	HS_ALERT2_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
[1]	HS_ALERT1_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
[0]	HS_FAULT_N_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

Register 0x29: SYSTEM_INTERRUPT_Stauts – System Interrupt Stauts Register

Table 57 – System Interrupt Status Register

Bit #	Name	R/W	Reset Value	Description
[7:6]	Reserved			Reserved
[5]	BCM54616S_INT_N	R		
[4]	LM75B_INT_N	R		
[3]	HOTSWAP_PG_status	R		
[2]	HS_ALERT2_status	R		
[1]	HS_ALERT1_status	R		
[0]	HS_FAULT_N_status	R		

Register 0x30: SYSTEM_POWER_STUTS – System Power Status Register

Table 58 – System Power Status Register

Bit #	Name	R/W	Reset Value	Description
[7]	Reserved			Reserved
[6]	Reserved			Reserved
[5]	COM_PWROK	RO		1: Normal 0: Fail
[4]	PWRGD_PCH_PWROK	RO		1: Normal 0: Fail
[3]	XP12R0V_COME_PG	RO		1: Normal 0: Fail
[2]	XP5R0V_COME_PG	RO		1: Normal 0: Fail
[1]	XP1R8V_PG	RO		1: Normal 0: Fail
[0]	XP3R3V_SSD_PG	RO		1: Normal

				0: Fail

Register 0x31: SYSTEM_POWER_ENABLE – System Power Enable Register

Table 59 – System Power Enable Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			Reserved
[3]	XP12R0V_COME_EN	R/W	1	1: Enable 0: disable
[2]	XP5R0V_COME_EN	R/W	1	1: Enable 0: disable
[1]	XP1R8V_EN	R/W	1	1: Enable 0: disable
[0]	XP3R3V_SSD_EN	R/W	1	1: Enable 0: disable

Register 0x32: SYSTEM_ISO_1 – System ISO 1 Register

Table 60 – System ISO 1 Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			Reserved
[3]	I2C1_BUF_EN	R/W	0	0: Enable 1: Disable
[2]	COME_USB_BUF_OE_N	R/W	0	0: Enable 1: Disable
[1]	IO_BUF_3V3_SCM_SMB_OE_N	R/W	0	0: Enable 1: Disable
[0]	IO_BUF_COME_3V3_OE_N	R/W	0	0: Enable 1: Disable

Register 0x34: THERMAL – Thermal Register

Table 61 – Thermal Register

Bit #	Name	R/W	Reset Value	Description
[7:1]	Reserved			
[0]	CB_THRMTRIP_N	RO		Indicating that the CPU has entered thermal shutdown.

Register 0x35: SYSTEM_MISC_1 – System Misc 1 Register

Table 62 – System Misc 1 Register

Bit #	Name	R/W	Reset Value	Description
[7:2]	Reserved			
[1]	COME_GPI0	RW	1	TBD

[0]	RTC_CLEAR	R/W	1	0: Clear CMOS 1: Normal work

Register 0x36: SYSTEM_MISC_2 – System Misc 2 Register

Table 63 – System Misc 2 Register

Bit #	Name	R/W	Reset Value	Description
[7:5]	Reserved			
[4]	ISO_HITLESS_EN	RO		1: Hitless on going. 0: Normal operation.
[3]	NVME_SSD_CLKREQ_N	RO		1: Normal operation. 0: NVME SSD Req.
[2]	Reserved	RO		
[1]	Reserved	RO		
[0]	BATLOW_N	RO		1: Battery is normal 0: Battery is low

Register 0x37: SYSTEM_MISC_3 – System Misc 3 Register

Table 64 – System Misc 3 Register

Bit #	Name	R/W	Reset Value	Description
[7]	PWR_BTN_N	RO		OCP debug card used
[6]	DEBUG_RST_BTN_N	RO		OCP debug card used When negative edge detect, The bit will flag
[5]	UART_SWITCH_N	RO		OCP debug card used When negative edge detect, The bit will flag
[4]	COME_TYPE2	RO		Module Type Descriptions
[3]	COME_TYPE1	RO		Module Type Descriptions
[2]	COME_TYPE0	RO		Module Type Descriptions
[1]	Reserved			
[0]	COME_GPO_0	RO		

Register 0x38: SYSTEM_MISC_4 – System Misc 4 Register

Table 65 – System Misc 4 Register

Bit #	Name	R/W	Reset Value	Description
[7:3]	Reserved			
[1]	SCM_EEPROM_WP	RW	1	1: Write protect 0: Write enable

[0]	BCM54616_PHY_EEPROM_WP	RW	1	1: Write protect 0: Write enable

Register 0x39: SYSTEM_MISC_5 – System Misc 5 Register

Table 66 – System Misc 5 Register

Bit #	Name	R/W	Reset Value	Description
[7:5]	Reserved			
[4]	SUS_S3_N_CLK_BUFFER_PWRD_N	RW	1	1: Power on 0: Power down
[3]	PCIE_CLK_BUFFER_DIF3_OE_N	RW	1	1: Buffer disable 0: Buffer enable
[2]	PCIE_CLK_BUFFER_DIF2_OE_N	RW	1	1: Buffer disable 0: Buffer enable
[1]	PCIE_CLK_BUFFER_DIF1_OE_N	RW	1	1: Buffer disable 0: Buffer enable
[0]	PCIE_CLK_BUFFER_DIF0_OE_N	RW	1	1: Buffer disable 0: Buffer enable

Register 0x3A: SYSTEM_MISC_6 – System Misc 6 Register

Table 67 – System Misc 6 Register

Bit #	Name	R/W	Reset Value	Description
[7:3]	Reserved			
[2]	CB_GBE0_ACT_N	RO		Link Active.
[1]	CB_GBE0_LINK1000_N	RO		Link speed on 1G.
[0]	CB_GBE0_LINK100_N	RO		Link speed on 100M.

5.9. Fan Control Module(FCM) and Fan-tray

Wedge400 uses four 80mm x 80mm x 80mm CR fans to provide forced air cooling to the chassis. There is one Fan Control Module (FCM) inside Wedge400 chassis. The FCM has one CPLD used for fan controlling and fan status monitoring. The BMC on SMB can access the fan control CPLD via a system management I2C bus.

FAN CPLD's JTAG goes directly from BMC's GPIOs to make the CPLD re-programming fast. The following diagram shows the functional blocks of fan control module:

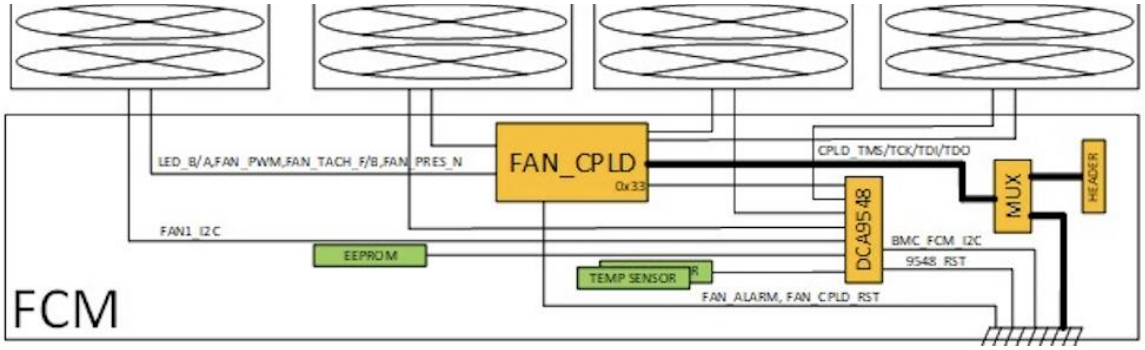


Figure 26:FAN Control Module (FCM)

5.9.1. Fan_CPLD Registers

There is a FAN_CPLD located on FCM board. Here are the functionalities of the CPLD:

- CPU can access FAN CPLD via I2C interface to get fan status.
- Register to control Fan PWM signal for fan speed control and detect fan direction, and the counter for fan speed reporting.
- Fan power control to enable/ disable Fan power rail.
- Detect fan speed to check fan status if there is any issue.
- Inform CPU by fan interrupt signal if any fan failure occurs, or temp sensor alerts or watchdog times out.
- The fan LED will report the fan status via Blue/Amber LEDs.

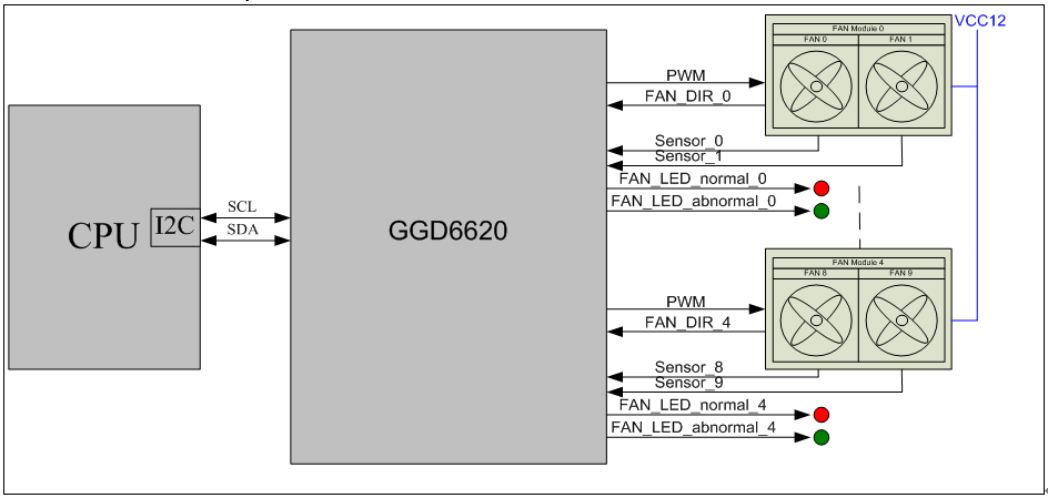


Figure 27:FAN Control Circuits

Here is the Fan_CPLD diagram:

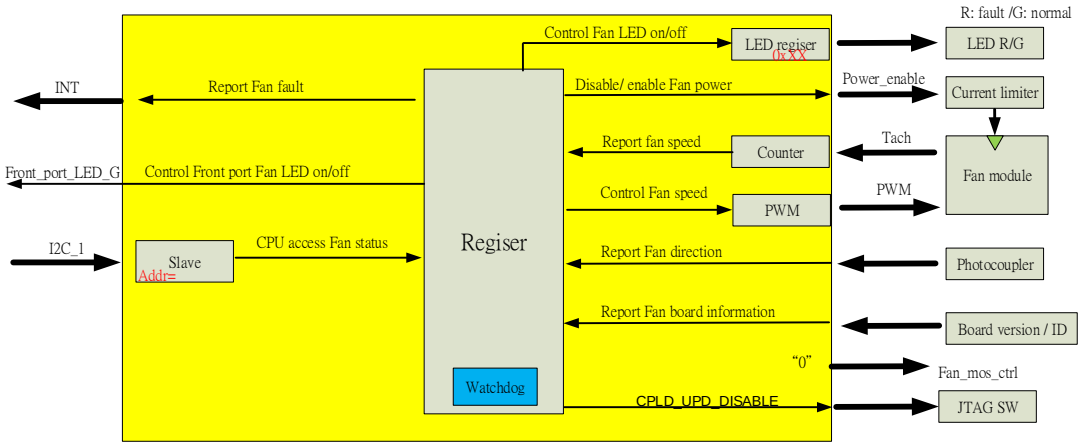


Figure 28:FAN CPLD Diagram

5.9.2. Fan Control Mechanism

Front fan max speed is 13400RPM, and rear fan max speed is 13700RPM.Period time is 200ms, CPLD counts negative waveform and records it at 0x20~0x23.

200ms / T ms = m (times / sec)

200ms / (1/2 * TS) = m (times / sec)

200ms/m (times / sec) = 1/2 * TS

TS = 60/N

N = 60/TS = 60/0.4*m=150*m (times / sec)

SW must multiple 150 and show it as RPM (Revolutions per minute).

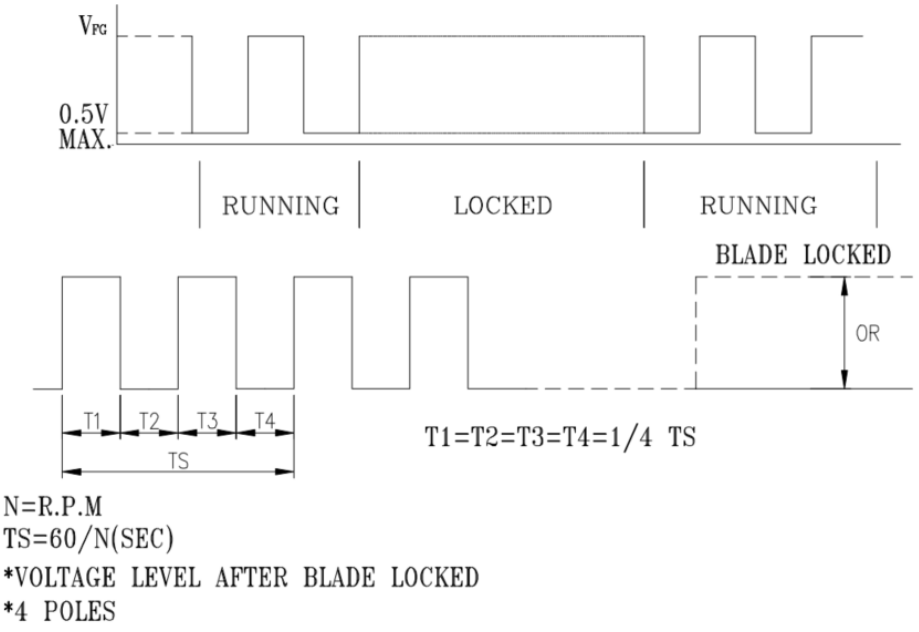


Figure 29:FAN PWM Calculation

Fan PWM setting duty cycle table shown in below table

Table 68 – FAN PWM Setting

FAN_PWM[4:0]	
00_0000	0/63 or 0% duty cycle
00_0001	1/63 or 1.549% duty cycle
00_0010	2/63 or 3.116% duty cycle
00_0011	3/63 or 4.671% duty cycle
00_0100	4/63 or 6.235% duty cycle
00_0101	5/63 or 7.804% duty cycle
00_0110	6/63 or 9.358% duty cycle
00_0111	7/63 or 10.923% duty cycle
00_1000	8/63 or 12.485% duty cycle
00_1001	9/63 or 14.047% duty cycle
00_1010	10/63 or 15.611% duty cycle
00_1011	11/63 or 17.174% duty cycle
00_1100	12/63 or 18.732% duty cycle
00_1101	13/63 or 20.295% duty cycle
00_1110	14/63 or 21.864% duty cycle
00_1111	15/63 or 23.414% duty cycle
01_0000	16/63 or 24.987% duty cycle
01_0001	17/63 or 26.553% duty cycle
01_0010	18/63 or 28.121% duty cycle
01_0011	19/63 or 29.678% duty cycle
01_0100	20/63 or 31.234% duty cycle
01_0101	21/63 or 32.795% duty cycle
01_0110	22/63 or 34.375% duty cycle
01_0111	23/63 or 35.923% duty cycle
01_1000	24/63 or 37.482% duty cycle
01_1001	25/63 or 39.048% duty cycle
01_1010	26/63 or 40.617% duty cycle
01_1011	27/63 or 42.177% duty cycle
01_1100	28/63 or 43.732% duty cycle
01_1101	29/63 or 45.303% duty cycle
01_1110	30/63 or 46.863% duty cycle
01_1111	31/63 or 49.900% duty cycle
10_0000	32/63 or 51.546% duty cycle
10_0001	33/63 or 53.109% duty cycle
10_0010	34/63 or 54.669% duty cycle
10_0011	35/63 or 56.234% duty cycle
10_0100	36/63 or 57.789% duty cycle
10_0101	37/63 or 59.369% duty cycle

10_0110	38/63 or 60.932% duty cycle
10_0111	39/63 or 62.495% duty cycle
10_1000	40/63 or 64.041% duty cycle
10_1001	41/63 or 65.613% duty cycle
10_1010	42/63 or 67.177% duty cycle
10_1011	43/63 or 68.745% duty cycle
10_1100	44/63 or 70.295% duty cycle
10_1101	45/63 or 71.863% duty cycle
10_1110	46/63 or 73.419% duty cycle
10_1111	47/63 or 74.975% duty cycle
11_0000	48/63 or 76.553% duty cycle
11_0001	49/63 or 78.106% duty cycle
11_0010	50/63 or 79.671% duty cycle
11_0011	51/63 or 81.234% duty cycle
11_0100	52/63 or 82.796% duty cycle
11_0101	53/63 or 84.349% duty cycle
11_0110	54/63 or 85.925% duty cycle
11_0111	55/63 or 87.482% duty cycle
11_1000	56/63 or 89.039% duty cycle
11_1001	57/63 or 90.606% duty cycle MAX
11_1010	58/63 or 92.169% duty cycle
11_1011	59/63 or 93.736% duty cycle
11_1100	60/63 or 95.297% duty cycle
11_1101	61/63 or 96.861% duty cycle
11_1110	62/63 or 98.424% duty cycle
11_1111	63/63 or 100.00% duty cycle

In order to reduce the inrush current after Fan present, CPLD will auto control the Fan PWM value after Fan presented. By default, the Fan PWM target value will set to 50% (This might be changed based on thermal testing results). CPLD will take 8S to increase the PWM duty cycle from 0% to 50%. Every 500mS increase a duty cycle level.
Below figure shows out the Fan present status and the PWM Duty Cycle output status.

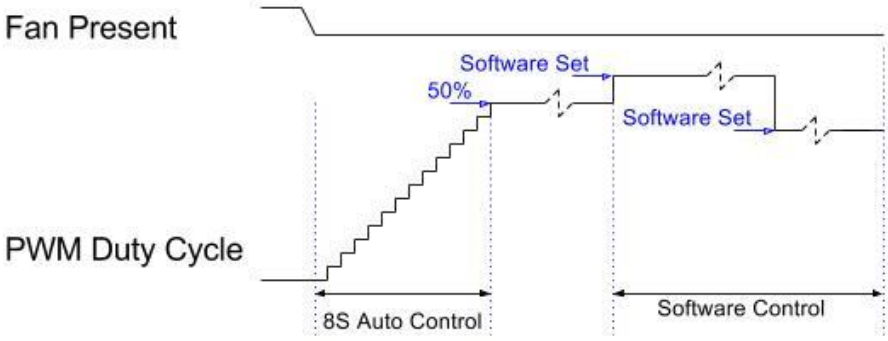


Figure 30:FAN Turn-on Slowly

Fan CPLD Register mapping:

Address	Register	R/W	Default value	Description
0x00	BOARD_VERSION	Read Only	0x00	Board Version Register
0x01	CPLD_VERSION	Read Only		CPLD Version Register
0x02	CPLD_SUB_VERSION	Read Only	0x01	CPLD Sub Version Register
0x04	INT_RPT	Read clear	0xFF	Interrupt Report Register
0x7	LM75 Alert Status	Read Only		
0x8	LM75 Alert Mask	Read & Write	0x3	
0x0F	FCB_EEPROM_WP	Read & Write	0x00	Fan Control Board EEPROM Write Protect Register
0x10	FAN_ENABLE-REG	Read & Write	0x0F	Fan Enable Register
0x11	FCB_ADM1278_REG	Read Only		ADM1278 Alert Register
0X12	FCB_ADM1278_MASK_REG	Read & Write	0x00	ADM1278 Alert Mask Register
0x13	FCB_Efuse_REG	Read Only		FCB_Efuse Alert Register
0x14	FCB_Efuse_Mask_REG	Read & Write		FCB_Efuse Alert Mask Register
0x20	FAN1_TACH_F_N	Read Only	0x00	Fan1 Front Fan Speed Register
0x21	FAN1_TACH_B_N	Read Only	0x00	Fan1 Back Fan Speed Register
0x22	FAN1_PWM	Read & Write	0x10	Fan1 PWM Control Register
0x24	FAN1_LED	Read & Write	0x00	Fan1 LED Control Register
0x25	FAN1_EEPROM_WP	Read & Write	0x00	Fan1 EEPOM Write Protect Register
0x28	FAN1_PRESENT	Read Only	0x00	Fan1 Status Register
0x29	FAN1_INT_MASK	Read & Write	0xFF	Fan1 Interrupt Mask Register
0x30-0x3A	FAN2 control register			The same as Fan1 control register from 0x20-0x2A
0x40_0x4A	FAN3 control register			The same as Fan1 control register from 0x20-0x2A
0x50-0x5A	FAN4 control register			The same as Fan1 control register from 0x20-0x2A

Register 0x00: BOARD_VERSION – Board Version Register

Table 69 – Board Version Register

Bit #	Name	R/W	Reset Value	Description
7	Reserved			Reserved
[6:4]	Version_ID[3:0]	R		000: R0A

				Others: Reserved
[3:2]	Reserved			Reserved
[1:0]	Board_ID[1:0]	R		00: Wedge 400 FCB board. Others: Reserved

Register 0x01: CPLD_VERSION – CPLD Version Register

Table 70 – CPLD Version Register

Bit #	Name	R/W	Reset Value	Description
[7]	Reserved	R		Reserved
[6]	Released Bit	R		0=not released 1=Released version after PVT
[5:0]	CPLD_ver[5:0]	R		CPLD version

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register

Table 71 – CPLD Sub Version Register

Bit #	Name	R/W	Reset Value	Description
[7:0]	CPLD_SUB_VERSION	R		CPLD sub-version, used for HW debug only

Register 0x04: INT_RPT – Fan Interrupt Report Register

Table 72 – Fan Interrupt Report Register

Bit #	Name	R/W	Reset Value	Description
[7]	HS_INT	RC	1	Hot swap interrupt status.
[6]	Efuse_INT	RC	1	Efuse interrupt status.
[1]	LM75_INT_1	RC	1	LM75 interrupt status.
[0]	LM75_INT_1	RC	1	LM75 interrupt status.
[3]	FAN4_INT	RC	1	FanTray-4 Interrupt 0: No interrupt 1: Fan4 interrupt is active
[2]	FAN3_INT	RC	1	FanTray-3 Interrupt 0: No interrupt 1: Fan3 interrupt is active
[1]	FAN2_INT	RC	1	FanTray-2 Interrupt 0: No interrupt 1: Fan2 interrupt is active
[0]	FAN1_INT	RC	1	FanTray-1 Interrupt 0: No interrupt 1: Fan1 interrupt is active

Register 0x7: LM75 Alert Register

Table 73 – LM75 Alert Register

Bit #	Name	R/W	Reset Value	Description
[7:2]	Reserved			
[1]	LM75_2	R		LM75 interrupt status
[0]	LM75_1	R		LM75 interrupt status

Register 0x8: LM75 Alert Mask Register

Table 74 – LM75 Alert Mask Register

Bit #	Name	R/W	Reset Value	Description
[7:1]	Reserved			
[1]	LM75_2 MASK	R/W	1	0: not mask 1: mask
[0]	LM75_1 MASK	R/W	1	0: not mask 1: mask

Register 0x0F: FCB_EEPROM_WP – Fan Control Board EEPROM Write Protect Register

Table 75 – Fan Control Board EEPROM Write Protect Register

Bit #	Name	R/W	Reset Value	Description
[7:1]	Reserved			
[0]	FCM_EEPROM_WP	R/W	1	AN Control Board EERPOM Write Protect 1:Not protect 0:Protect

Register 0x10 FAN_ENALBE_REG – Fan Enable Register

Table 76 – Fan Enable Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			
[3]	FAN4_ENALBE_REG	R/W	1	FAN4 Power Supply Enable 1: Enable the fan Power 2: Disable the fan Power
[2]	FAN3_ENALBE_REG	R/W	1	FAN3 Power Supply Enable 1: Enable the fan Power 2: Disable the fan Power
[1]	FAN2_ENALBE_REG	R/W	1	FAN2 Power Supply Enable 1: Enable the fan Power 2: Disable the fan Power
[1]	FAN1_ENALBE_REG	R/W	1	FAN1 Power Supply Enable 1: Enable the fan Power 2: Disable the fan Power

Register 0x11: ADM1278 Alert Register

Table 77 – ADM1278 Alert Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			
[3]	HS_FAULT	R	1	HS_FAULT status
[2]	HS_ALERT2	R	1	HS_FAULT2 status
[1]	HS_ALERT1	R	1	HS_FAULT1 status
[0]	HOTSWAP_PG	R	1	HOTSWAP_PG status

Register 0x12: ADM1278 Alert Mask Register

Table 78 – ADM1278 Alert Mask Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			
[3]	HS_FAULT_MASK	R/W	1	0: not mask 1: mask
[2]	HS_ALERT2_MASK	R/W	1	0: not mask 1: mask
[1]	HS_ALERT1_MASK	R/W	1	0: not mask 1: mask
[0]	HOTSWAP_PG_MASK	R/W	1	0: not mask 1: mask

Register 0x13: FCB_Efuse Alert Register

Table 79 – FCB_Efuse Alert Register

Bit #	Name	R/W	Reset Value	Description
[7]	PG_FAN4	R	0	Fan4 Efuse PG status
[6]	PG_FAN3	R	0	Fan3 Efuse PG status
[5]	PG_FAN2	R	0	Fan2 Efuse PG status
[4]	PG_FAN1	R	0	Fan1 Efuse PG status
[3]	FLTB_FAN4	R	0	Fan4 FLTB status
[2]	FLTB_FAN3	R	0	Fan4 FLTB status
[1]	FLTB_FAN2	R	0	Fan4 FLTB status
[0]	FLTB_FAN1	R	0	Fan4 FLTB status

Register 0x13: FCB_Efuse Alert Mask Register

Table 80 – FCB_Efuse Alert Mask Register

Bit #	Name	R/W	Reset Value	Description
[7]	PG_FAN4_MASK	R/W	1	0: not mask 1: mask
[6]	PG_FAN3_MASK	R/W	1	0: not mask 1: mask
[5]	PG_FAN2_MASK	R/W	1	0: not mask

				1: mask
[4]	PG_FAN1_MASK	R/W	1	0: not mask 1: mask
[3]	FLTB_FAN4_MASK	R/W	1	0: not mask 1: mask
[2]	FLTB_FAN3_MASK	R/W	1	0: not mask 1: mask
[1]	FLTB_FAN2_MASK	R/W	1	0: not mask 1: mask
[0]	FLTB_FAN1_MASK	R/W	1	0: not mask 1: mask

Below register definition is the same for all Fans. Fan1 control register range is 0x20-0x2F. Fan2 register range is 0x30-0x3F. Fan3 register range is 0x40-0x4F. Fan4 register range is 0x50-0x5F.

Register 0x10*(i-1) +20: FANi_TACH_F_N – Fan1 Front Fan Speed Register, (i=1,2,3,4)

Table 81 – Fani Front Fan Speed Register

Bit #	Name	R/W	Reset Value	Description
[7:0]	FANi_TACH_F_N	RO		Fani Front Fan Speed

Register 0x10*(i-1) +21: FANi_RFAN_B_N – Fan1 Back Fan Speed Register, (i=1,2,3,4)

Table 82 – Fani Back Fan Speed Register

Bit #	Name	R/W	Reset Value	Description
[7:0]	FANi_TACH_B_N	RO		Fani Back Fan Speed

Register 0x10*(i-1) +22: FANi_PWM – Fan1 PWM Control Register

Table 83 – Fani PWM Control Register

Bit #	Name	R/W	Reset Value	Description
[7]	Reserved	RO		
[6:0]	FANi_PWM	R/W		FANi_PWM[5:0] FanTray i PWM control signal Please refer to Table3 for the mapping to fan duty cycle.

Register 0x10*(i-1) +24: FANi_LED – Fani LED Control Register

Table 84– Fani LED Control Register

Bit #	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W		
[1:0]	FANi_LED	R/W	00	FANi_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON

				10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF

Register 0x10*(i-1) +25: FANi_EEPROM_WP – Fan1 EEPOM Write Protect Register

Table 85– Fani EEPROM Write Protect Register

Bit #	Name	R/W	Reset Value	Description
[7:1]	Reserved	R/W		
[0]	FANi_EEPROM_WP	R/W		FANi EERPOM Write Protect 1:Protect 0:Not protect

Register 0x10*(i-1) +28: FAN1_PRESENT – Fan1 Status Register

Table 86– Fani Status Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved	RO		
[3]	FFANi_ALIVE	RO		Front Fani Alive Status 0: alive 1: bad
[2]	RFANi_ALIVE	RO		Rear Fani Alive Status 0: alive 1: bad
[1]	FANi_ALIVE	RO		Fani Alive Status 0: alive 1: bad
[0]	FANi_PRESENT	RO		FanTray i Present 0: alive 1: bad

Register 0x10*(i-1) +29: FANi_INT_MASK – Fan1 Interrupt Mask Register

Table 87– Fani Interrupt Mask Register

Bit #	Name	R/W	Reset Value	Description
[7:4]	Reserved			
[3]	FFANi_ALIVE_MASK	R/W	1	Front Fani Alive Status Interrupt

				Mask 0: not mask 1: mask
[2]	RFANi_ALIVE_MASK	R/W	1	Rear Fani Alive Status Interrupt Mask 0: not mask 1: mask
[1]	FANi_ALIVE_MASK	R/W	1	Fani Alive Status Interrupt Mask 0: not mask 1: mask
[0]	FANi_PRE_MASK	R/W	1	FanTray i Present Interrupt Mask 0: not mask 1: mask

5.10. LED

Wedge400 chassis and module cards have status LED to display the information of the system.

5.10.1. LED Controlling

The following diagram shows the LED controlling in system.

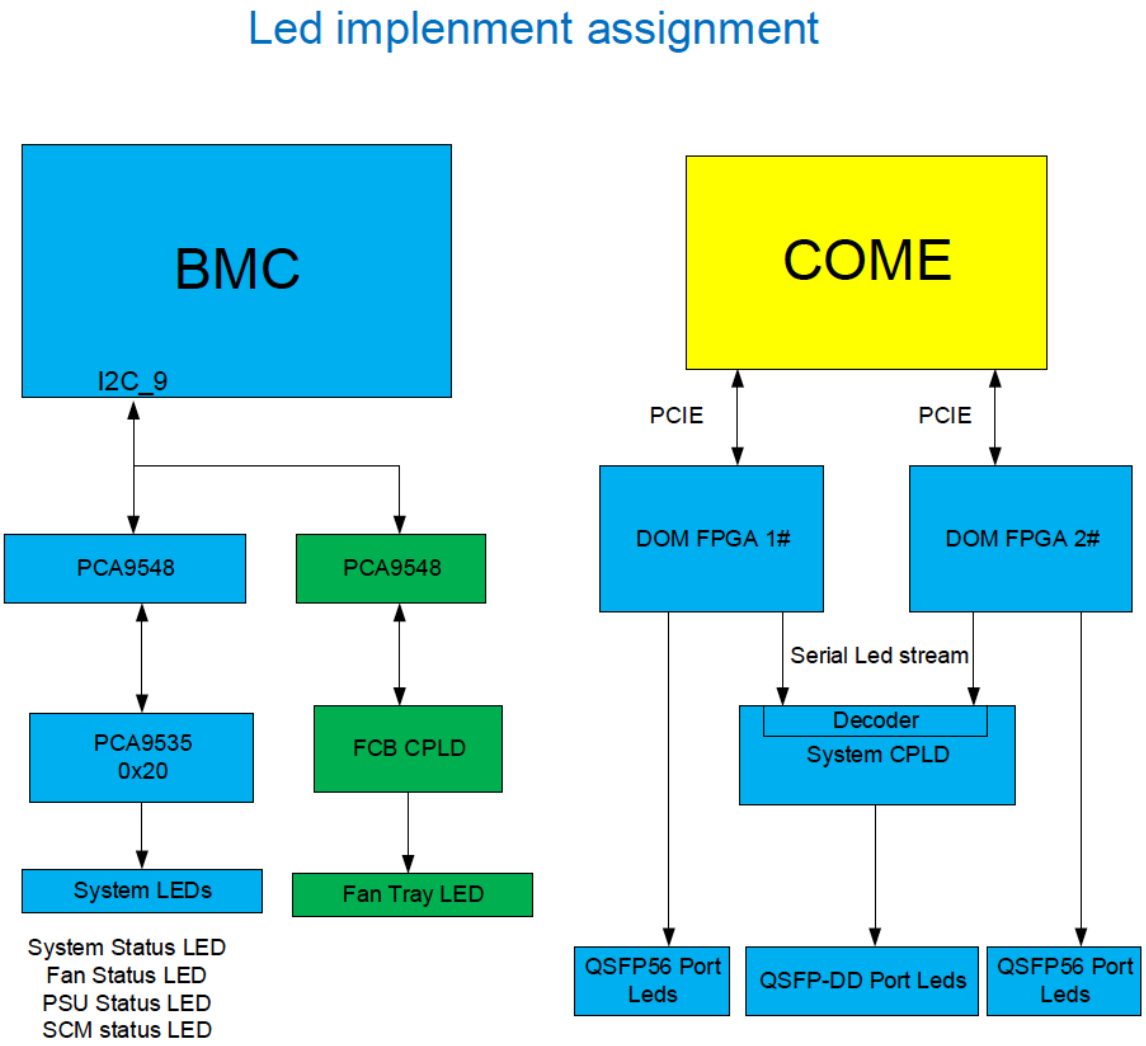


Figure 31:LED Diagram

5.10.2. System Information LED (SIM)

There are four tri-color LED on the top left corner of Wedge400 front panel to display information of the system:

- STS: System Status LED
- FAN: Fan Status LED
- PSU: PSU Status LED
- SCM: System Control Module Status LED

BMC controls the SIM LED through an I2C IO expander on SMB. SIM PCA9535 Bit Mapping:

Bit	Name	R/W	Reset Value	Description

15:14	Reserve		1	NA
13	SCM_BLU_L	R/W	1	SMB LED Blue 0: SMB LED Blue is ON 1: SMB LED Blue is OFF
12	SCM_GRN_L	R/W	1	SMB LED Green 0: SMB LED Green is ON 1: SMB LED Green is OFF
11	SCM_RED_L	R/W	1	SMB LED Red 0: SMB LED Red is ON 1: SMB LED Red is OFF
10	PSU_BLU_L	R/W	1	PSU LED Blue 0: PSU LED Blue is ON 1: PSU LED Blue is OFF
9	PSU_GRN_L	R/W	1	PSU LED Green 0: PSU LED Green is ON 1: PSU LED Green is OFF
8	PSU_RED_L	R/W	1	PSU LED Red 0: PSU LED Red is ON 1: PSU LED Red is OFF
7:6	Reserve		1	NA
5	FAN_BLU_L	R/W	1	FAN LED Blue 0: FAN LED Blue is ON 1: FAN LED Blue is OFF
4	FAN_GRN_L	R/W	1	FAN LED Green 0: FAN LED Green is ON 1: FAN LED Green is OFF
3	FAN_RED_L	R/W	1	FAN LED Red 0: FAN LED Red is ON 1: FAN LED Red is OFF
2	SYS_BLU_L	R/W	1	SYS LED Blue 0: SYS LED Blue is ON 1: SYS LED Blue is OFF
1	SYS_GRN_L	R/W	1	SYS LED Green 0: SYS LED Green is ON 1: SYS LED Green is OFF
0	SYS_RED_L	R/W	1	SYS LED Red 0: SYS LED Red is ON 1: SYS LED Red is OFF

OpenBMC software controls the system information LED per OCP Panel Indication Specification, and the following is the specific behavior in Minipack. Please note that Amber is generated by turning on both Red and Green.

LED	Default Power-On State	Color	Condition
SYS LED	Off	Blue	All FRUs are present, and no FRU-level alarms
		Amber	One or more FRUs are not present; One or more FRUs have alarms
		Blue / Amber flashing (0.5s Blue and 0.5s Amber alternating)	Firmware upgrade in process (BIOS, EEPROM, CPLD, FPGA, etc.)
		Amber flashing	Attention from service technician required
Fan LED	Off	Blue	All fans are present, and are within the normal RPM range
		Amber	One or more fans are not present; One or more fans have out-of-range RPM
PSU LED	Off	Blue	All PSUs are present, and both INPUT OK and PWR OK are asserted for every PSU (accessible through SMB Sys CPLD by BMC)
		Amber	One or more PSUs are not present; One or more PSUs have INPUT OK or PWR OK de-asserted
SCM LED	Off	Blue	No out-of-range voltage and temperature sensors
		Amber	One or more sensors out-of-range

Table 88: System Information LED Definition

5.10.3. Management OOB port LEDs

The OOB RJ45 port on SMB front panel also have typical Active LED and Link status LED to indicate the status of OOB Ethernet:
Link Speed LED, Left of OOB RJ45 port, Green/Amber

- Solid Green: 1Gbps
- Solid Amber: 100Mbps
- OFF: No link/10Mbps

Activity LED, right of OOB RJ45 port

- Blinking Green: TX or RX activity
- OFF: no activity

5.10.4. QSFP Port LEDs

There is one LED per QSFP56 port, and two LEDs per QSFP-DD port. The microserver / CPU accesses the port LED control registers in DOM FPGA through PCIe, and DOM FPGA lights up the port LEDs on front panel.

Following is the port LED control design diagram. This design uses time-division-multiplex concept to drive external logic with a serial interface. The external logic could be discrete shifters, or external CPLD, or simply FPGA user logic.

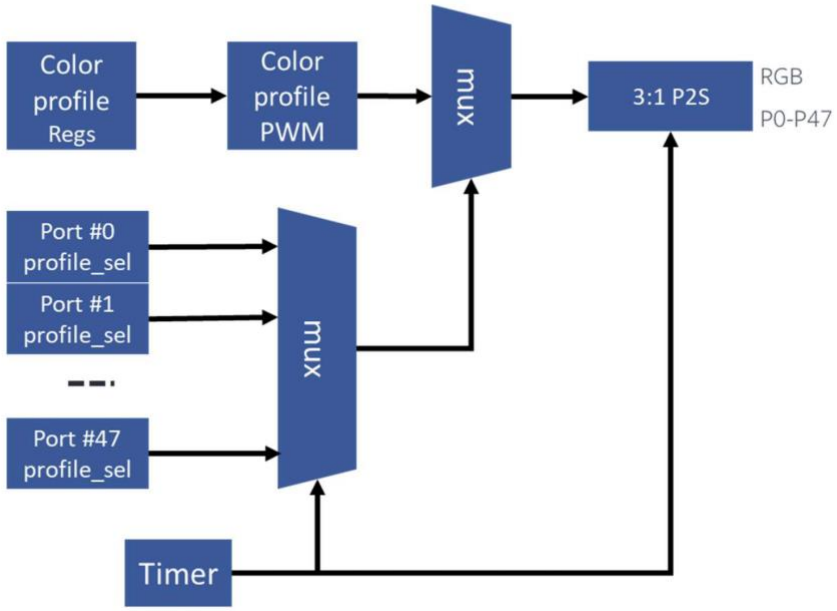


Figure 32:Port LED Control Path

Here is the expected port LED behavior under micro-server/DOM FPGA's control.

LED	Default Power-On State	Color	Condition
Port LED	Rotating colors	Blue	Link up
		Amber	Optic transceiver present but link down
		Amber flashing	Attention from service technician required
		Off	Optic transceiver not present

Table 89: Port LED Behavior

5.10.4.1. Background of Adding LED button

W400 is designed with 2 LEDs per QSFP-DD port, and 1 LED per QSFP port on the front panel.

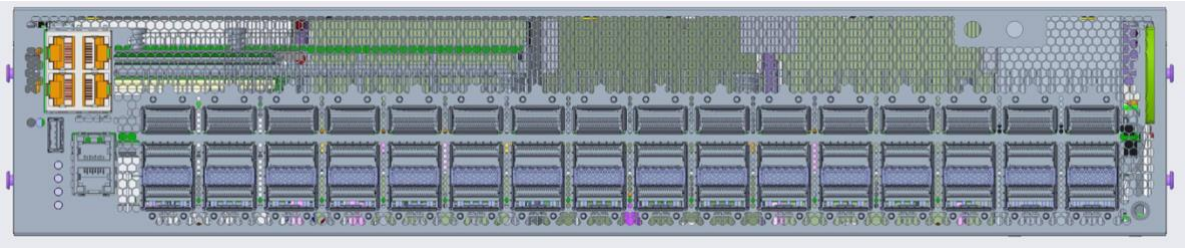


Figure 33:Front Port View

5.10.4.2. LED button

There is an LED Select buttom and LED indicating the LED modes.

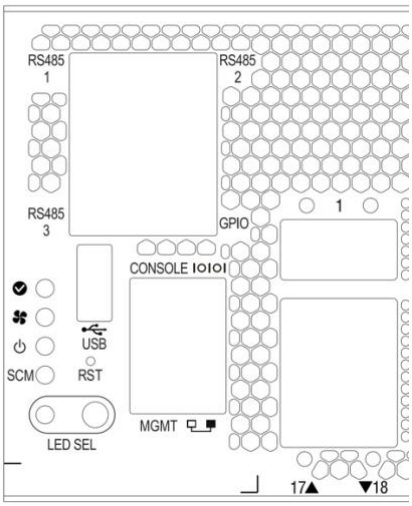


Figure 34:Silkscreen on LED SEL and LED button

6. Modules Interfaces

Wedge400 has the following components:

- Switch Main Board (SMB)
- System Controller Module (SCM)
- Fan Control Module (FCM)
- Power Distribution Board(PDB)
    - Power Distribution Board Top (PDB-T)
    - Power Distribution Board Bottom (PDB-B)
- Power Supply Unit (PSU)
    - AC/DC: AC PSU
    - DC/DC: DC PEM
- Fan Tray Unit(FAN)
    - 80mm x 80mm x80mm Fan tray FRU

Here are the descriptions of the interfaces between modules.

6.1. Interfaces between SCM and SMB

Signal definitions/mappings:

	MPN	Vendor						
SCM	10124308-101LF	FCI						
SMB	10128415-101LF	FCI						
Guide pin	TBD	FCI						
For SCM								
	8	7	6	5	4	3	2	1
K	CPLD_RESET	Gnd	(ISO_M2_ALERT)-BMC_SPI_2_WP_N	Gnd	ISO_PWR_BTN_N	Gnd	BMC_FW_SPI_CS1_N	Gnd
J	Gnd	SCM_PCIE_FPGA1_RX_1_P	Gnd	DOM_FPGA1_PCIE_CLK_N	Gnd	SCM_SGMII_TX_P	Gnd	SCM_PCIE_FPGA1_TX_1_P
I	SCM_10G_RX_P	SCM_PCIE_FPGA1_RX_1_N	SCM_PCIE_FPGA1_RX_0_P	DOM_FPGA1_PCIE_CLK_P	SCM_PCIE_FPGA2_TX_0_N	SCM_SGMII_TX_N	SCM_PCIE_FPGA1_TX_0_P	SCM_PCIE_FPGA1_TX_1_N
H	SCM_10G_RX_N	Gnd	SCM_PCIE_FPGA1_RX_0_N	Gnd	SCM_PCIE_FPGA2_TX_0_P	Gnd	SCM_PCIE_FPGA1_TX_0_N	Gnd
G	Gnd	SCM_PCIE_FPGA2_RX_1_P	Gnd	DOM_FPGA2_PCIE_CLK_N	Gnd	SCM_PCIE_TH3_TX_1_N	Gnd	SCM_PCIE_TH3_TX_2_N
F	SCM_SGMII_RX_P	SCM_PCIE_FPGA2_RX_1_N	SCM_PCIE_FPGA2_RX_0_P	DOM_FPGA2_PCIE_CLK_P	SCM_USB_DN	SCM_PCIE_TH3_TX_1_P	SCM_10G_TX_N	SCM_PCIE_TH3_TX_2_P
E	SCM_SGMII_RX_N	Gnd	SCM_PCIE_FPGA2_RX_0_N	Gnd	SCM_USB_DP	Gnd	SCM_10G_TX_P	Gnd
D	Gnd	SCM_PCIE_TH3_RX_2_N	Gnd	SCM_PCIE_TH3_RX_0_N	Gnd	SCM_PCIE_FPGA2_TX_1_N	Gnd	SCM_PCIE_TH3_TX_0_N
C	SCM_PCIE_TH3_RX_3_P	SCM_PCIE_TH3_RX_2_P	SCM_PCIE_TH3_RX_1_N	SCM_PCIE_TH3_RX_0_P	SW_TH3_PCIE_CLK_N	SCM_PCIE_FPGA2_TX_1_P	SCM_PCIE_TH3_TX_3_N	SCM_PCIE_TH3_TX_0_P
B	SCM_PCIE_TH3_RX_3_N	Gnd	SCM_PCIE_TH3_RX_1_P	Gnd	SW_TH3_PCIE_CLK_P	Gnd	SCM_PCIE_TH3_TX_3_P	Gnd
A	Gnd	(SCM_Preset) BMC_SPI_1_WP_N	Gnd	ISO_DEBUG_RST_BTN_N	Gnd	ISO_COM_SUS_S3_N	Gnd	BMC_FW_SPI_CLK
	8	7	6	5	4	3	2	1
K	COM_PWROK	Gnd	SCM_LPC_SERIRQ_N	Gnd	(NC)BMC_EMMC_CLK	Gnd	(GND)SCM_SPI_WP_N	12V
J	Gnd	SCM_LPC_AD_0	Gnd	SCM_SPI_MOSI	Gnd	(SCM_SPI_Sel_N)BMC_EMMC_D0	Gnd	12V
I	(CPLD_RESET_1)BMC_FW_SPI_MISO	SCM_LPC_AD_1	(ISO_UART_SWITCH_N)SCM_SPI_Sel_N	SCM_SPI_MISO	SCM_I2C_SCL	(SCM_SPI_WP_N)BMC_EMMC_D1	(GND)DOM_FPGA_SCM_CPLD_SCL	12V
H	(SCM_power_enable)BMC_FW_SPI_CS0_N	Gnd	SCM_LPC_CLK	Gnd	SCM_I2C_SDA	Gnd	(GND)DOM_FPGA_SCM_CPLD_SDA	12V
G	Gnd	(NC)BMC_SPI_1_RST	Gnd	SCM_SPI_CLK	Gnd	SCM_COM_MDC	Gnd	12V
F	(SCM_SMB_ALRT_N)BMC_FW_SPI_MOSI	(HITLESS_EN)BMC_SPI_2_RST	SCM_LPC_AD_2	SCM_SPI_CS	(ISO_M2_SMB_CLK)BMC_EMMC_D2	SCM_COM_MDIO	(GND)SCM_Preset	12V
E	ISO_CB_RESET_N	Gnd	SCM_LPC_AD_3	Gnd	(ISO_M2_SMB_SDA)BMC_EMMC_D3	Gnd	(GND)SCM_power_enable	12V
D	Gnd	SCM_COM_UART5_TX	Gnd	SMB_TCK	Gnd	(DOM_FPGA_SCM-CPLD_SCL)(X)P3R3V_BMC	Gnd	12V
C	SCM_SMBus_SCL	SCM_COM_UART5_RX	SCM_LPC_FRAME_N	SMB_TMS	SMB_TDI	(DOM_FPGA_SCM-CPLD_SDA)(X)P3R3V_BMC	(GND)HITLESS_EN	12V
B	SCM_SMBus_SDA	Gnd	(SCM_TPM_PP)BMC_EMMC_RST_N	Gnd	SMB_TDO	Gnd	(GND)ISO_M2_ALERT	12V
A	Gnd	PWRGD_PCH_PWROK	Gnd	BMC_SCM_CPLD_EN	Gnd	(NC)BMC_EMMC_CMD	Gnd	12V

6.2. Interfaces between FMC and SMB

Signal definitions:

	MPN	Vendor								
FCB signal	501190-2017	Molex								
FCB power	449141201	Molex								
Signal										
Pin number	1	3	5	7	9	11	13	15	17	19
Signal name	Gnd	FCM_SCL	FAN_ALARM	CARD_PRESENT	Gnd	FCM_SEL	FCM_TCK	FCM_TDO	3R3V_EN	NC
Signal name	Gnd	FCM_SDA	FCM_PCA9548_RST	FCM_CPLD_RST	Gnd	FCM_TMS	FCM_TDI	Gnd	FCM_Hitless	NC
Pin number	2	4	6	8	10	12	14	16	18	20
Power										
Pin number	1	2	3	4	5	6				
Signal name	12V	12V	12V	GND	GND	GND				
Signal name	12V	12V	12V	GND	GND	GND				
Pin number	7	8	9	10	11	12				

6.3. Interfaces between PDB and SMB

Signal definitions:

	MPN	Vendor
PDB_T signal	501190-2017	Molex
PDB_T power	C10-761044-000	AMPHENOL
SMB signal to PDB_T	501190-2017	Molex
SMB signal to PDB_B	501190-3017	Molex
SMB power	C10-760262-000	AMPHENOL
PDB_B signal	501190-3017	Molex
PDB_B power	C10-760246-000	AMPHENOL

Pin number	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29
Signal name	PSU_I2C_SCL	PSU_ALERT_L	PSU_ACOK	PSU_L1_ON	V_SENSE	ISHARE	Gnd	Gnd	3.3V_SBY	3.3V_SBY	NC	NC	NC	NC	NC
Signal name	PSU_I2C_SDA	PSU_PWROK	PSU_PRNST_N	Gnd	V_SENSE_R	Gnd	Gnd	Gnd	3.3V_SBY	3.3V_SBY	NC	NC	NC	NC	NC
Pin number	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30

6.4. Interfaces between Rackmon board and SMB

Signal definitions:

Rack Mon connector	NA	NA
SMB connector	HSEC8-125-01-L-DV-A-K-TR	Samtec
RackMon RJ45 2*2	RMR4JZ-Z6B3-3ED-0R	Luxshare
USB 3.0	484040004	Molex
Led(4)		

Pin number	1	3	5	7	9	11	13	15	17	19
Signal name	RMON_PF_1	RMON_PF_2	RMON_PF_3	PCA9535_LED_SCL	RACK_GPIO_1	RACK_GPIO_3	RACK_GPIO_5	RACK_GPIO_7	FT232_Reset_N	XP3R3V
Signal name	RMON_RF_1	RMON_RF_2	RMON_RF_3	PCA9535_LED_SDA	RACK_GPIO_2	RACK_GPIO_4	RACK_GPIO_6	RACK_GPIO_8	Debug_Present_N	XP3R3V
Pin number	2	4	6	8	10	12	14	16	18	20

Pin number	21	23	25	27	29	31	33	35	37	39
Signal name	Gnd	OOB_SW_SMIIA_TX_P	OOB_SW_SMIIA_TX_N	Gnd	USB_FT232_P	USB_FT232_N	Gnd	OOB_SW_SMIIA_RX_P	OOB_SW_SMIIA_RX_N	Gnd
Signal name	Gnd	OOB_SW_SMIIB_TX_P	OOB_SW_SMIIB_TX_N	Gnd	MGMT_BRD_USB_P	MGMT_BRD_USB_N	Gnd	OOB_SW_SMIIB_RX_P	OOB_SW_SMIIB_RX_N	Gnd
Pin number	22	24	26	28	30	32	34	36	38	40

Pin number	41	43	45	47	49	51	53	55	57	59
Signal name	XP5R0V	Debug_SCL	Gnd	Debug_UART_TX	RACK_MON_GE_MDC	Gnd	RACK_BUTTON_LED_G	RACK_BUTTON_LED_B	XP12R0V	RACK_RESET_BUTTON
Signal name	XP5R0V	Debug_SDA	PCA9535_reset_N	Debug_UART_RX	RACK_MON_GE_MDIO	Gnd	RACK_BUTTON_LED_R	RACK_LED_BUTTON	XP12R0V	Gnd
Pin number	42	44	46	48	50	52	54	56	58	60

6.5. Interfaces between Timing board and SMB

Signal definitions:

	MPN	Vendor	
SMB	61082-042422LF	FCI	
Timing board	TBD	FCI	

Signal name	Pin number		Signal name
XP12R0V	1	2	XP12R0V
GND	3	4	GND
XP3R3V	5	6	XP3R3V
XP3R3V	7	8	XP3R3V
GND	9	10	GND
PTP_BMC_SCL	11	12	PTP_SPI_CS1
PTP_BMC_SDA	13	14	PTP_SPI_CS2
GND	15	16	GND
PTP_RESET	17	18	PTP_SPI_MISO
PTP_PRESENT	19	20	PTP_SPI_MOSI
GND	21	22	PTP_SPI_SCK
DPLL_REF_CLK_P	23	24	GND
DPLL_REF_CLK_N	25	26	PTP_FPGA_CLK_4K
GND	27	28	PTP_FPGA_CLK_1PPS
NC	29	30	GND
NC	31	32	GND
GND	33	34	PTP_FPGA_CLK_25M
L1_RCVRD_CLK	35	36	NC
GND	37	38	GND
L1_RCVRD_CLK_BKUP	39	40	NC

7. Transceivers and cables

100G optic

- QSFP28 CWDM4 100G transceiver (MSA)
- QSFP28 LR4/LR4-lite 100G transceiver (IEEE)
- QSFP28 SR4 100G transceiver (IEEE)
- 100G DAC Cable
- QSFP28 100GE to QSFP28 100GE cable, 1M, 2M, 3M, 3.5M
- QSFP28 100GE to 2 QSFP28 50GE split cable, aka Y-cable, 1M, 2M, 3M, 3.5M
- QSFP28 100GE to 4 SFP28 25GE fanout cable, 1M, 2M, 3M, 3.5M

200G optic

- QSFP56 FR4 200G transceiver
- QSFP56 200G to QSFP56 200G cable, 1M, 1.5M, 2M

400G optic

- QSFP-DD FR4 400G transceiver

8. Wedge400 Power and Mechanical

Wedge400 has AC version and DC version. The DC version is based on 12V ORv2 power supply.

8.1. DC/DC Power Extension Module (PEM)

Wedge400 has 12V DC PEM to support ORv2 rack installation.

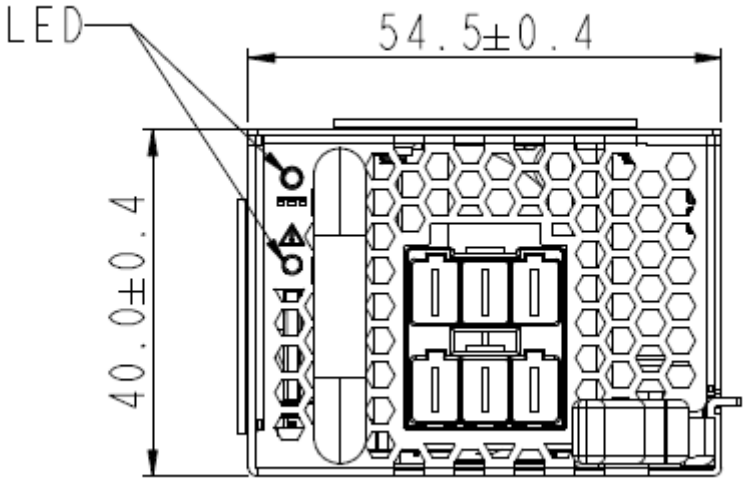
Hot-swappable	Yes
Load-sharing	No
Efficiency Requirement	90+% across full load range
Input characteristics	DC: 11.8 – 12.8 Vdc
Input connector	MiniELCON PN 2204535-1
Output characteristics	Primary 12 Vdc, at rated power output Rated power for primary 12 Vdc shall be follow SKU(Shelf rack power Unit) Standby 3.3 Vdc, +/- 5%, 2A
Hold up time	N/A
LED	Blue Amber Error/Failure/Bad
Air flow	Front to back
Output control	Need provide a mechanism for primary 12 Vdc shutdown by the host software. The 3.3 Vdc standby power shall always be present
Status report	output indicating status of the 12 Vdc output
Monitor and control	I2C / PMBus interface for software monitoring and control Need support following parametric data : Main DC output voltage, current, and power Auxiliary DC output voltage, current, and power PEM temperature sensor(s)

Here is the signal definition on the DC PEM connector:

Pin	Signal Name	Type	Vlow_max	Vhigh_min	Function	comments
Power						
1-5	GND					
6-10	+12V					
Signal						
A1	3.3VSB					
B1	3.3VSB					
C1	3.3VSB					
D1	3.3VSB					
E1	3.3VSB					
A2	SGND					
B2	SGND					
C2	N/C	-	-	-	-	-
D2	N/C	-	-	-	-	-
E2	N/C	-	-	-	-	-

A3	N/C	-	-	-	-	-
B3	N/C					
C3	SDA	Bi-directional	0.4V	2.1V	I2C data	Pull up resistor is 10Kohm
D3	N/C	-	-	-	-	-
E3	N/C	-	-	-	-	-
A4	SCL	Input	0.4V	2.1V	I2C clock	Pull up resistor is 10Kohm
B4	PSON_L	Input / Active low	0.8V	2.0V	Enable / Disable Main Output	Logic “Low” – turn ON Logic “High” – turn Off Pull up resistor is 10kohm
C4	SMB_ALERT_L	Output / Active low	0.4	2.4	SM Alert	Logic “Low” – Fault or Warning Logic “High” – OK
D4	N/C					
E4	VINOK_H(ACOK_H)	Output / Active high	0.4V	2.4V	Input Power OK	Logic “High” – Output is OK Logic “Low” – Output is not OK Pull up resistor is 10Kohm
A5	PSKILL_H	Input/ Active low	0.8V	2.0V	Control the PSU	Logic “Low” – PSU OK Logic “High” – PSU shut down Pull up resistor is 10Kohm
B5	N/C	-	-	-	-	-
C5	PWOK_H	Output / Active high	0.4V	2.4V	Output Power OK	Logic “High” – Output is OK Logic “Low” – Output is not OK Pull up resistor is 10kohm
D5	N/C					
E5	SGND					

LED definition:



DCPEM CONDITION	BLUE (OK) LED STATUS	AMBER (FAIL) LED STATUS
12V Input and output OK	ON	OFF
No 12V input	OFF	OFF
DCPEM failure (no 12V output)	OFF	ON

8.2. AC/DC PSU

Wedge400 uses Delta DDM1500BH12A3F AC power supply unit (PSU) to provide power to the chassis. There are 2 PSU in the chassis. Each PSU is rated at 1500W with 12V output. The power system of Wedge400 is load sharing of two PSU, usually it is used as 1+1 PSU redundancy, one PSU connect to one AC feed and the other PSU connect to redundant feed, providing feed redundancy. The following Figure shows the AC PSU from Delta.

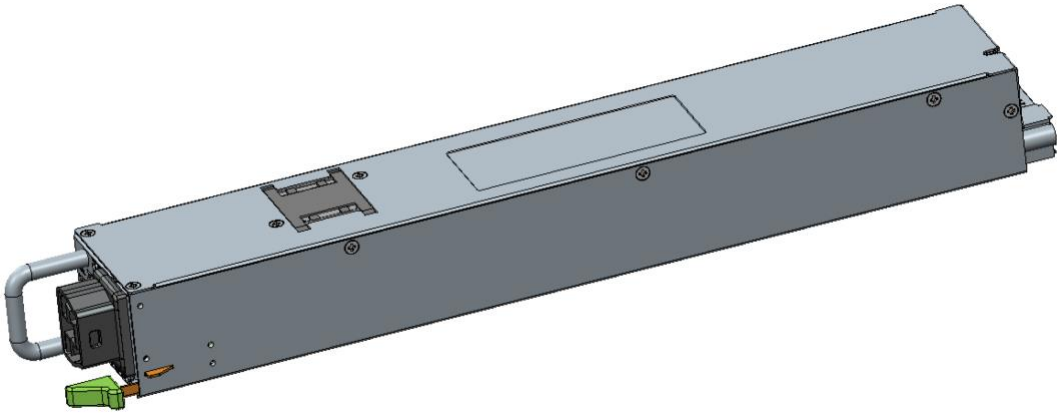


Figure 35:DDM1500BH12A3F 1.5KW PSU

Power Supply Connector: Tyco Electronics P/N 2-1926736-3 (NOTE: Column 5 is recessed (short pins))
Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

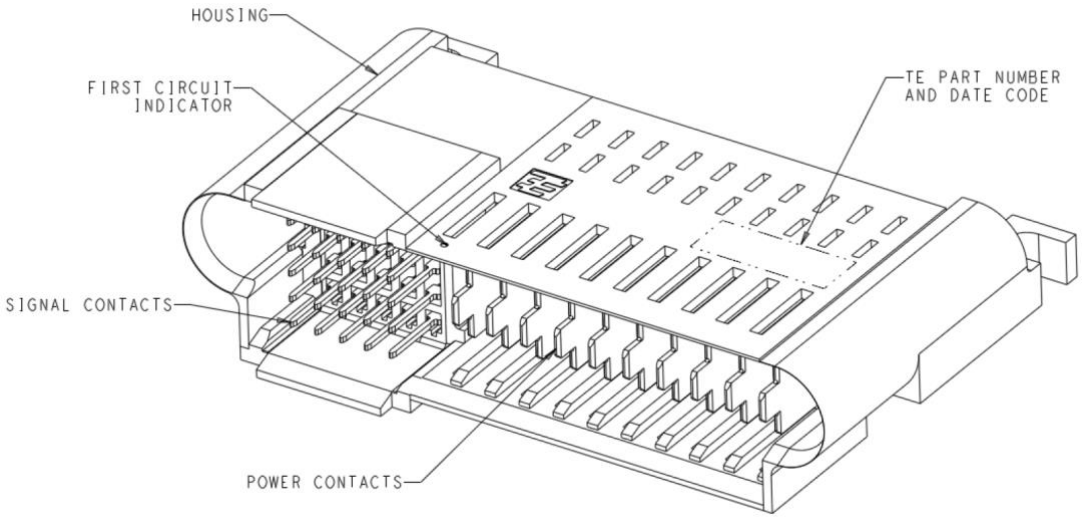


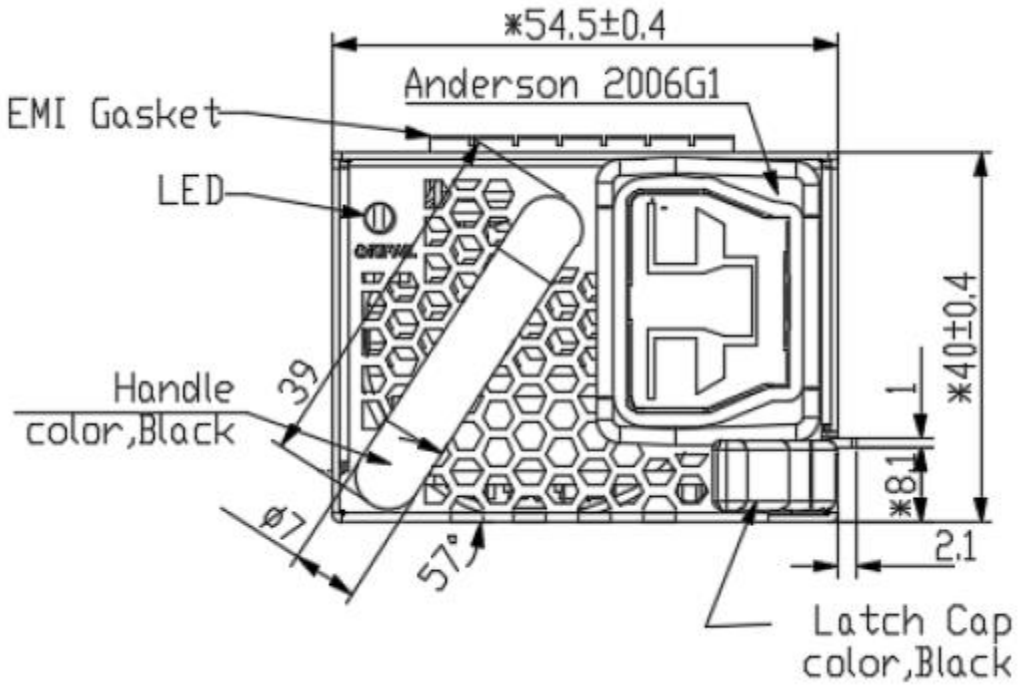
Figure 36:PSU power output connector

	1	2	3	4	5	PGND	V1
A	VSB	SGND	APS	SCL	PSKILL_H	1, 2, 3, 4, 5	6, 7, 8, 9, 10
B	VSB	SGND	N/C	PSON_L	ISHARE		
C	VSB	HOTSTANDBYEN_H	SDA	SMB_ALERT_L	PWOK_H		
D	VSB	VSB_SENSE_R	V1_SENSE_R	N/C	VSB_SEL		
E	VSB	VSB_SENSE	V1_SENSE	ACOK_H	PRESENT_L		

Signal definition:

Pin	Signal Name	Type	Vlow_max	Vhigh_min	Function	comments
Power						
1-5	GND					
6-10	+12V					
Signal						
A1	3.3VSB					
B1	3.3VSB					
C1	3.3VSB					
D1	3.3VSB					
E1	3.3VSB					
A2	SGND					
B2	SGND					
C2	HOTSTANDBYEN_H	Input/ Active low	0.8V	2.0V	Control the Smart standby mode	Logic “Low” – normal redundancy mode Logic “High” – Smart standby mode Pull up resistor is 10kohm
D2	Analog	-	-	Standby output remote positive sense line	Analog	
E2	VSB_SENSE	Analog	-	-	Standby output remote positive sense line	
A3	APS	Input	-	-	The I2C address	It is connected with resistor to select the address Pull up resistor is 12.1kohm
B3	N/C					
C3	SDA	Bi-directional	0.4V	2.1V	I2C data	Pull down resistor is 47.5ohm
D3	V1_SENSE_R	Analog	-	-	Main output remote negative sense line	
E3	V1_SENSE	Analog	-	-	Main output remote positive sense line	
A4	SCL	Input	0.4V	2.1V	I2C clock	Pull down resistor is 47.5ohm
B4	PSON_L	Input / Active low	0.8V	2.0V	Enable / Disable Main Output	Logic “Low” – turn ON Logic “High” – turn Off Pull up resistor is 10kohm
C4	SMB_ALERT_L	Output / Active low	0.4	2.4	SM Alert	Logic “Low” – Fault or Warning Logic “High” – OK
D4	N/C					
E4	ACOK_H	Output / Active high	0.4V	2.4V	Input Power OK	Logic “High” – Output is OK Logic “Low” – Output is not OK Pull up resistor is 10kohm
A5	PSKILL_H	Input/ Active low	0.8V	2.0V	Control the PSU	Logic “Low” – PSU OK Logic “High” – PSU shut down Pull up resistor is 47.5kohm
B5	ISHARE	Analog	-	-	Main output current share bus	
C5	PWOK_H	Output / Active high	0.4V	2.4V	Output Power OK	Logic “High” – Output is OK Logic “Low” – Output is not OK Pull up resistor is 10kohm
D5	VSB_SEL	Input	-	-	Select the standby output	NA
E5	PRESENT_L	Output / Active low	0.4V	-	PSU present	Connected to SGND inside PSU

LED definition:



Event	Blue LED Status	Amber LED Status
12V main on and in voltage regulation band (Active mode)	Solid Blue	OFF
12V main off (Standby mode)	1HZ Blinking	OFF
No AC input power to any of the system power supplies	OFF	OFF
No AC input power, but other PSU in the system operating	OFF	1HZ Blinking
F Warning event (Output OCW/ OTW/ Fan fail)	OFF	1HZ Blinking
Fault event (Input OVP/ Output OVP, UVP, OCP/ OTP/ Other internal fault)	OFF	Solid Amber
FW update	OFF	2HZ Blinking

8.3. Power Circuits Design Target

Here is the power estimation which is for DC/DC design to support worst case. It's target for board DC/DC design, not for thermal design.

	Component	Qty	Voltage			
			12	5	3.3	1.2
SCM board	COME module	1.00	5.00	2		
	CPLD	1.00	0.00		0.15	
	M.2	2.00	0.00		2.5	
	Phy BCM54616S	1.00	0.00		0.35	0.24
	Other	1.00	0.00		0.5	
	Total(W)	90.09	5	2	6	0.24

	Component	Qty	Voltage							
			5	3.3	2.5	1.8	1.2	1.15	1	0.8	0.8
(include Rack M	TH3	1		0.74		0.38	5.8			397	79
	Aspeed 2520	1		0.5			0.7	0.8			
	DDR 4	1			0.02		0.31				
	DOM FPGA	2		0.37		0.2	0.1		3		
	QSFP-DD	16		4.24							
	QSFP56	32		2.12							
	SFP GE	1		0.5							
	PWR CPLD	1		0.1							
	System CPLD	1		0.2							
	BCM54616S	2		0.35			0.24				
	EMMC	1		0.1							
	BCM5389	1			0.04		0.812				
	USB hub	1		0.11							
	USB	1	1								
	Other	1		1							
	Total(W)	867.46	1	140.37	0.06	0.78	8.302	0.8	6	397	79

	Component	Qty	Voltage
			3.3
FCB board	FCB CPLD	1	0.15
	FAN	4	23.6
	Others	1	1
	Total(W)	81.68	24.75

System Total Power Consumtion	1154.69

8.4. Power Tree

Here is the power tree estimated from 12V main input to low voltage power rails:

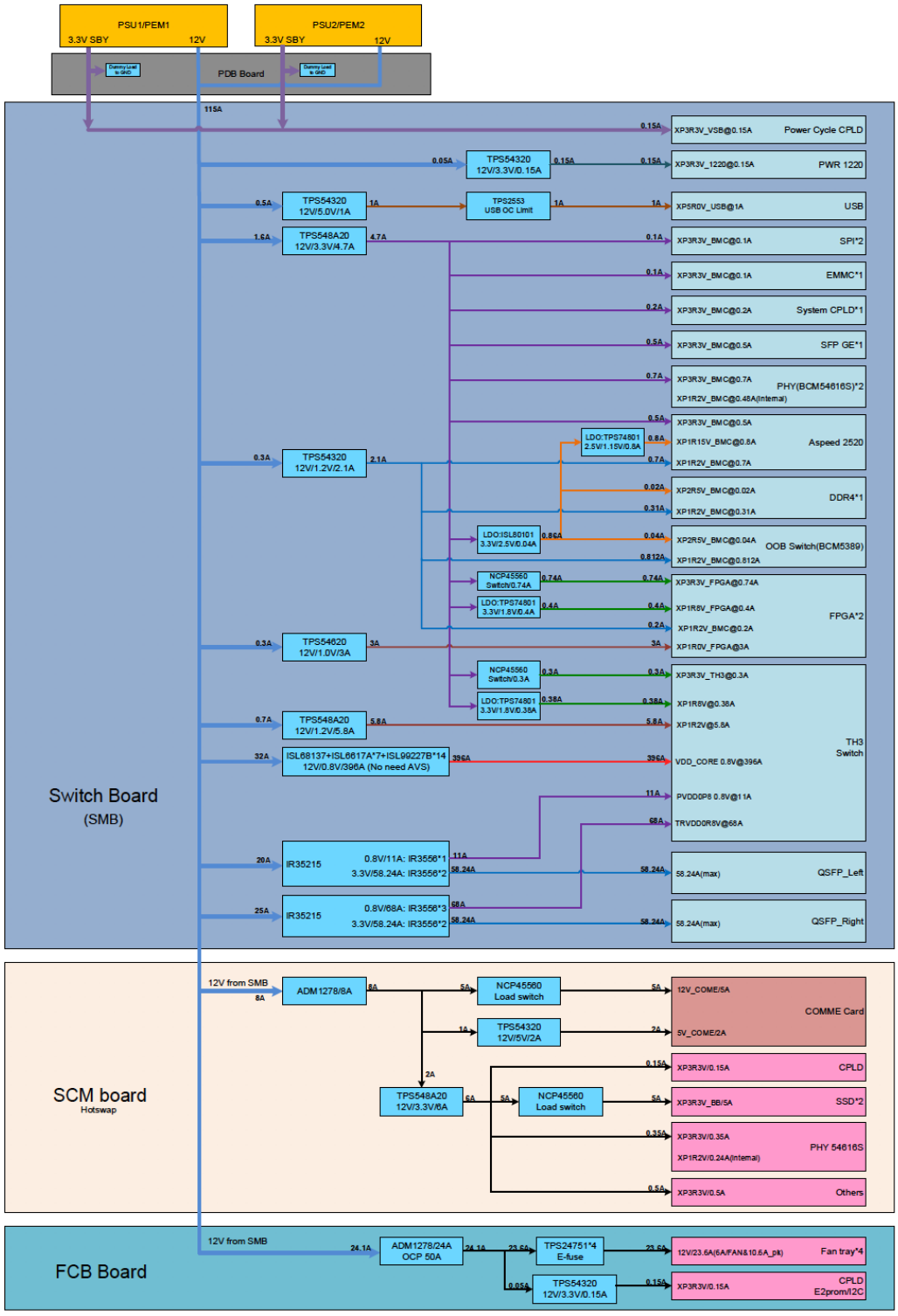


Figure 37:Power Tree Diagram

6.5. Voltage Detection Sensors

There are 9 Low Voltage Monitor Inputs which can accept voltage range between 0.075V and 5.734V and 1 High Voltage Monitor Inputs which can accept voltage range between 0.3V and 13.2V.
There are 8 power rails on board and 2 power rails from PSU. The detail channel mapping is shown below.
Table 90 ispPAC_POWR1220AT8 IO Assignment

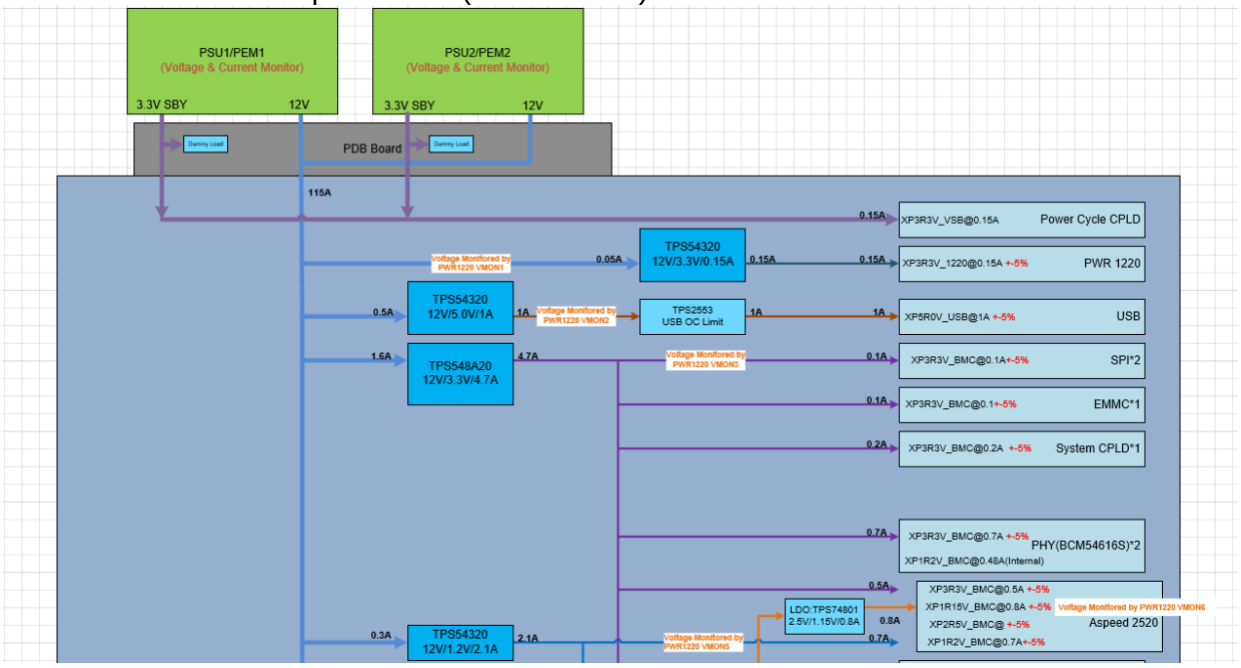
IO#	IO	Signal Name	Function Description
VMON1	IN	PWR12R0V_MON	Detect POWR 1220A self voltage is good or not
VMON2	IN	XP5R0V	Detect USB XP5R0V is good or not
VMON3	IN	XP3R3V_BMC	Detect BMC XP3R3V is good or not
VMON4	IN	XP2R5V_BMC	Detect BMC XP2R5V is good or not
VMON5	IN	XP1R2V_BMC	Detect BMC XP1R2V is good or not
VMON6	IN	XP1R15V_BMC	Detect BMC XP1R8V is good or not
VMON7	IN	XP1R8V_FPGA	Detect FPGA XP1R8V is good or not
VMON8	IN	PVDD0P8	Detect TH3 QSFP 0.8V is good or not
VMON9	IN	XP3R3V_TH3	Detect TH3 XP3R3V is good or not
VMON10	IN	VDD_CORE	Detect TH3 CORE 0.8V is good or not
VMON11	IN	TRVDD0R8V	Detect TH3 TRVDD0R8V is good or not
VMON12	IN	XP3R3V_RIGHT	Detect QSFP XP3R3V is good or not
OUT 1	OUT	XP5R0V_USB_EN	Enable signal for USB XP5R0V regulator, high active
OUT 2	OUT	PWR1220_RESET_PRST	RESET POWR1220
OUT 3	OUT	BMC_P1220_SYS_OK	Power good signal – POWR1220_SYS
OUT 4	OUT	N/A	
OUT 5	OUT	XP3R3V_BMC_EN	Enable signal for BMC XP3R3V regulator, high active
OUT 6	OUT	XP1R0V_FPGA_EN	Enable signal for FPGA XP1R0V regulator, high active
OUT 7	OUT	XP2R5V_BMC_EN	Enable signal for BMC XP2R5V regulator, high active
OUT 8	OUT	XP1R2V_BMC_EN	Enable signal for BMC XP1R2V regulator, high active
OUT 9	OUT	XP1R8V_FPGA_EN	Enable signal for FPGA XP1R8V regulator, high active
OUT 10	OUT	XP1R15V_BMC_EN	Enable signal for BMC XP1R5V regulator, high active
OUT 11	OUT	BMC_POWER_OK	Power good signal - BMC
OUT 12	OUT	XP3R3V_FPGA_EN	Enable signal for FPGA XP3R3V regulator, high active

OUT 13	OUT	XP3R3V_RL_EN	Enable signal for QSFP XP3R3V regulator, high active
OUT 14	OUT	XP3R3V_TH3_EN	Enable signal for TH3 XP3R3V regulator, high active
OUT 15	OUT	VDD_TH3_EN	Enable signal for TH3 VDD_CORE regulator, high active
OUT 16	OUT	XP1R2V_TH3_EN	Enable signal for TH3 XP1R2V regulator, high active
OUT 17	OUT	XP1R8V_TH3_EN	Enable signal for TH3 XP1R8V regulator, high active
OUT 18	OUT	XP0R8V_PVDD_EN	Enable signal for QSFP PVDD0P8V regulator, high active
OUT 19	OUT	XP0R8V_TRVDD_EN	Enable signal for TH3 TRVDD0R8V regulator, high active
OUT 20	OUT	TH3_POWER_OK	Power good signal – TH3

6.6. Current Detection Sensors

The current detection on Wedge400 will be categorized as follows.

- Current of 12V primary power can be read from PSU through I2C
- Currents of switch core/analogy power rails (high current) can be read from PWM controllers through I2C
- Current of QSFP-DD 3.3V can be read from PWM controller through I2C
- Current of other power rails (small current) will NOT be monitored



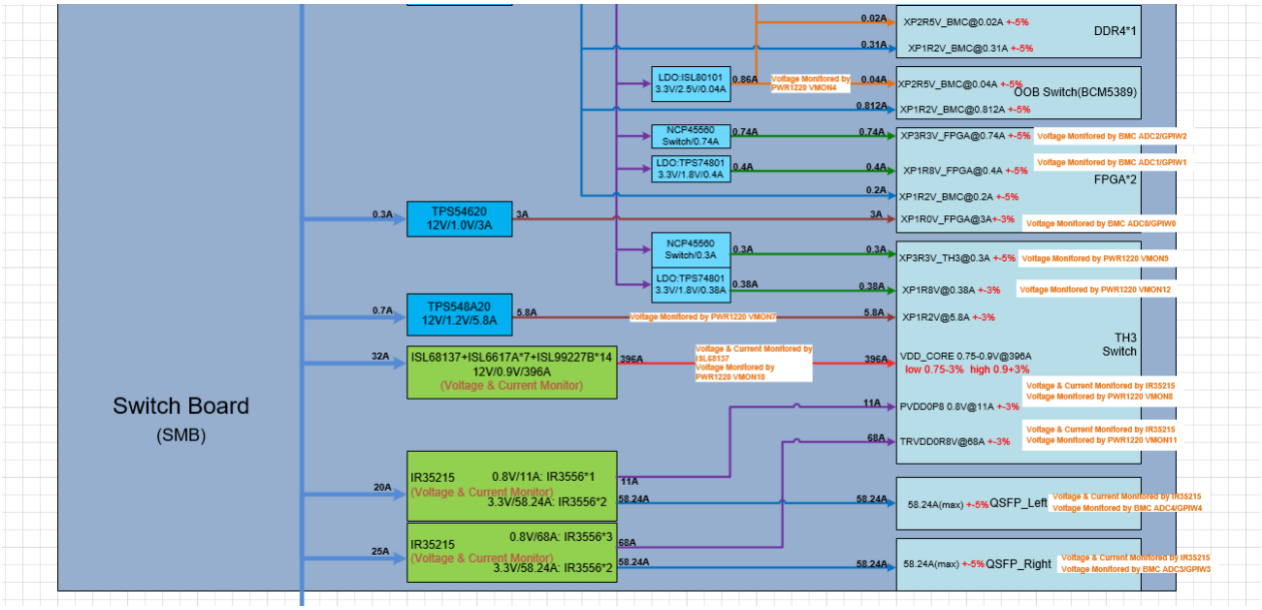


Figure 38:Power Monitor Diagram

9. Thermal design

The thermal design of Wedge400 is optimized for better thermal performance to support 55C CWDM4 100G optics, 65C FR4 200G optics and 65C FR4 400G optics, which are specified by Meta.
Totally there are 4 fan-tray in Wedge400 chassis, each fan-tray has one 80mm x 80mm x 80mm CR fan. The FCM (Fan Control Module) supports 4 fan-tray.

9.1. Fan tray

Wedge400 chassis supports four fan-tray with 3+1 redundancy.

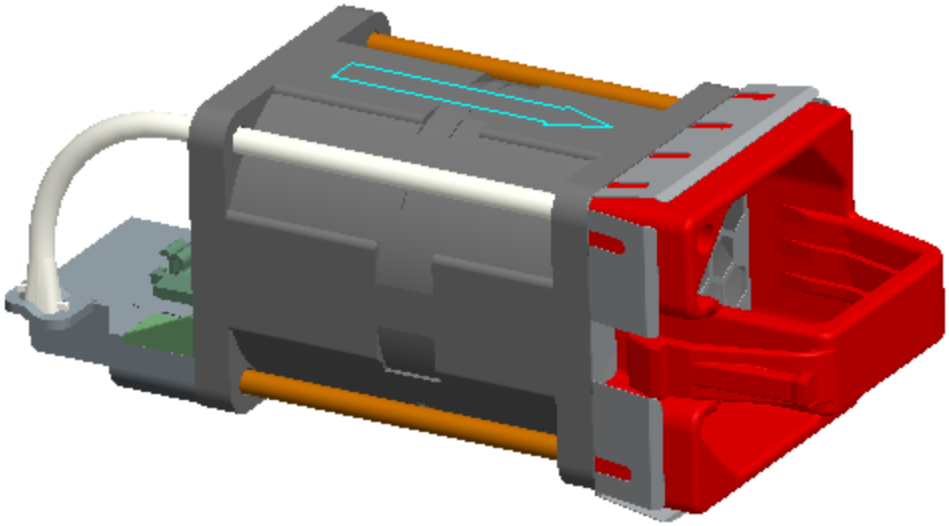


Figure 39:Wedge400 Fan-tray

The following Sanyo Denki CR fan is recommended.

- Sanyo Denki: 9CRA0812P8G001 (80mm x 80mm x 80mm)
- 63.6W Max
- Rated speed: 12000 inlet, 11300 outlet
- Max Airflow: 4.5 M3/min, or 158.9CFM
- Max Static Pressure: 4.62 inchH2O

Figure 40:Wedge400 fan

80mm CR fan 9CRA0812P8G001 from Sanyo Denki has the following technical parameters

9CRA0812P8G001	
Item	Description
Rated voltage	12 VDC
Operating voltage	7.0 ~ 13.2 VDC
Input current	5.30A
Input power	63.6W
speed	Front 12000, Rear 11300 RPM +/-10%
Max Air flow at zero static	4.50m3/min, or 158.9CFM
Max Air Pressure	4.62 in-H2O
acoustic	76 dB-A
Lead Wire	

Table 3: Sanyo Denki fan 9CRA0812P8G001

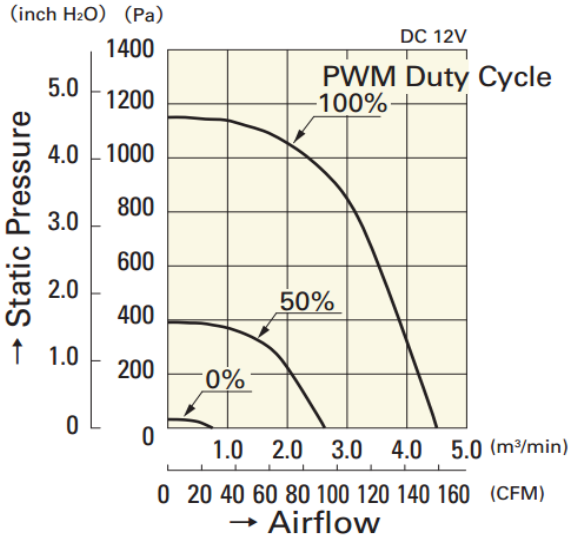


Figure 41:PQ Curve of CR Fan 9CRA0812P8G001

9.2. Temperature Sensors

Each module card can have multiple temperature sensors to monitor temperature. Temperature information needs to be reported to the BMC via system management I2C bus.
Additionally, over-temperature thresholds are configurable, and an alert mechanism is provided to enable thermal shutdown and / or an increase in airflow. The sensors are accurate to +/-2C. The ambient temperature sensor can be a TMP75 from Texas Instruments or an equivalent part from other vendors. Its I2C address can be set to 0x98 to 0x9F. 8 TMP75 temperature sensors can share one i2c bus.

BMC Channel	I2C switch address	witch cha	Device type and Address	Description
I2c_3	0x70	2	LM75, 0x4c	Sensor on SCM. Not need for FSC at this moment
I2c_3	0x70	2	LM75, 0x4d	Sensor on SCM. Not need for FSC at this moment
I2c_4	NA	NA	LM75, 0x48	system inlet sensor(left)
I2c_4	NA	NA	LM75, 0x49	TH3 outlet sensor
I2c_4	NA	NA	LM75, 0x4A	SMB outlet sensor
I2c_4	NA	NA	LM75, 0x4B	system inlet sensor(right)
I2c_4	NA	NA	TPM421, 0x4C	System left side.Not need for FSC at this moment
I2c_4	NA	NA	TPM421, 0x4D	System right side.Not need for FSC at this moment
I2c_4	NA	NA	TPM422, 0x4F	TH3 internel sensor.
I2c_12	0x76	3	LM75, 0x48	system outlet sensor(left)
I2c_12	0x76	3	LM75, 0x49	system outlet sensor(left)

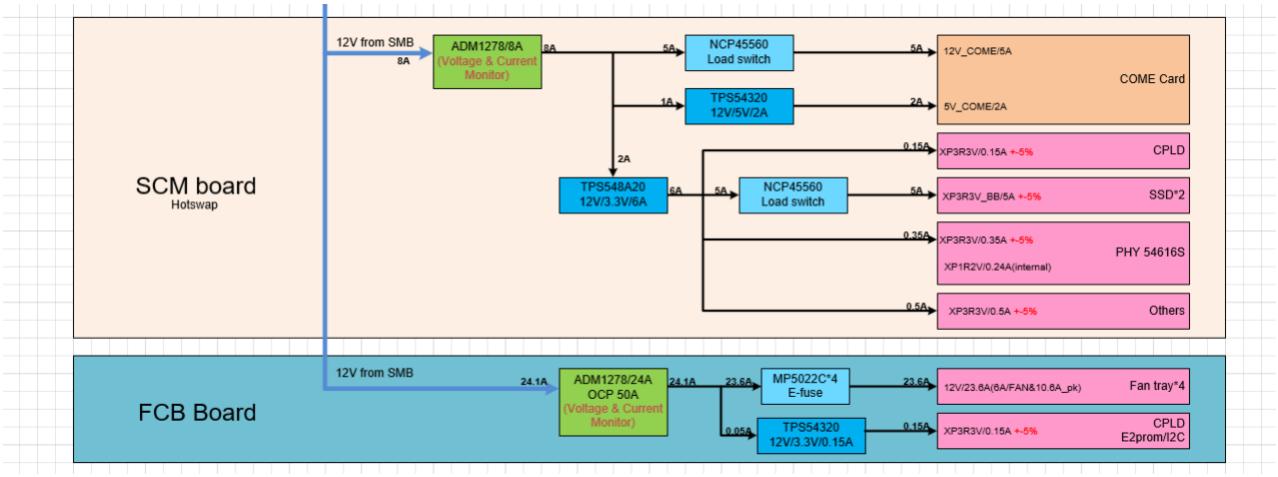


Figure 42:Temperature I2C Access

10. Regulatory Compliance Requirements

Every ODM engaged with Meta to develop a L10 product to be used in our Data Center's infrastructure must meet the following regulatory compliance requirements. Reports must be from labs accredited to a current version of IEC 17025. The reports and certificates must name the ODM as the applicant.

10.1. CE Declaration to the following Regulatory Directives by ODMs

EMC Directive 2014/30/EU
Low Voltage (LVD) Directive 2014/35/EU

10.2. Safety Certification

CB certificate/report to IEC 62368-1 including all national deviations
CB certificate/report to IEC/EN 60950-1 including all national deviations
UL/CSA/IEC/EN 60950-1 with all latest amendments
UL/IEC 62368-1 with all latest amendments
CNS14336 Taiwan BSMI safety regulation
EN 60825-1 Safety of Laser products – part 1
UL 94-V0 Flammability rating

10.3. EMC Certification

Every ODM engaged with Meta to develop a L10 product to be used in our Data Center's infrastructure must meet the following regulatory compliance requirements. Reports must be from labs accredited to a current version of IEC 17025. The reports and certificates must name the ODM as the applicant. EMC certification and report:
FCC Part 15 (Class A)
ICES-003 (Canada) Class A
EN55032 (Europe) Class A
CISPR32 (International) Class A
AS/NZS CISPR32 (Australia and New Zealand) Class A
VCCI CISPR 32 (Japan) Class A
CNS 13438 (Taiwan) Class A
EN61000-3-2
EN61000-3-3
EN55024
EN 61000-4-2 ESD
EN 61000-4-3 Radiated Immunity
EN 61000-4-4 EFT
EN 61000-4-5 Surge
EN 61000-4-6 Low Frequency Conducted Immunity
EN 61000-4-11 Voltage Variations and Dips

10.4. Immunity Levels

The ODM must strive to design to the META Goal at the start and during the project. The design team will decide if levels below the goal are acceptable. Off the shelf power supplies must meet the required level at a minimum.

Network Equipment						
Immunity Standard	Description	Standard Criteria (Required)	FB Criteria (Goal)	Standard Level (Required)	FB Level (Goal)	Remarks
IEC 61000-4-2	Electrostatic Discharge (ESD)	B	A	4 kV Cont. / 8 kV Air	8 kV Cont. / 15 kV Air	Criteria A (FB Goal) is highly desirable for any level
IEC 61000-4-3	Radiated Immunity	A	A	3 V/m	10 V/m	For communication cables >3 meters
IEC 61000-4-4	EFT	B	B	0.5 kV		Ports: Signal &Telecom (>3 meters), DC power input
		B	B	1 kV		Ports: AC power input & AC/DC Converter
IEC 61000-4-5	Surges	C	A	1 kV		Ports: Signal and Telecom connected to outdoor cables
		B	A	0.5 kV		Ports: DC power input
				1 kV L-L / 2 kV L-GND		Ports: AC power input & AC/DC Converter
IEC 61000-4-6	Conducted Immunity	A	A	3 V	10 V	Ports: Signal &Telecom (>3 meters), AC and DC power input
IEC 61000-4-8	Magnetic Field	A	A	1 A/m		Only EUT containing devices susceptible to magnetic fields
IEC 61000-4-11	Voltage Dips	B	B	>95% Reduction		Ports: AC power input & AC/DC Converter (0.5 Period)
		C	C	30% Reduction		Ports: AC power input & AC/DC Converter (25 Periods)
	Voltage Interruptions	C	C	>95% Reduction		Ports: AC power input & AC/DC Converter (250 Periods)

10.5. Sound

The ODM must strive to design to the META Goal at the start and during the project. The design team will decide if levels above the goal are acceptable. The sound power level limits apply to the normal operating conditions where the system is configured and equipped in its deployed state with the worst case configuration to produce the loudest noise. Maintenance conditions, open covers, are not considered normal conditions and do not need to be measured. Sound from alarms does not need to be measured. Maximum fan speed expected under normal operation should be measured.

Network Equipment				
	OHSA (Required)	Directive 2003/10/EC (Goal)	FB Design Goal	Remarks
Sound Limit	85	80	78	Under normal operation at 25 ˚C, the system must not produce a A-weighted sound power level above the required limit. The FB design goal should be targeted during development of the product. The Directive goal represents the limit that requires hearing protection to be provided to our Data Center Staff in Europe. The ODM must provide the result of the formal testing.

10.6. Environmental Compliance

Every ODM engaged with Meta to develop a L10 product to be used in our Data Center's infrastructure must meet the following environmental compliance requirements. Reports must be from labs accredited to a current version of IEC 17025. Environmental Compliance reports:
RoHS 2
REACH (SVHC & Annex 17)
WEEE
POP Regulation
Prop 65
Batteries Directive
Halogen-free IEC/EN 61249-2-21 (900 ppm Br or Cl, 1500 ppm combined)
Phthalate (DEHP, DBP, DiBP, BBP)-free (1000 ppm)
Arsenic-free (1000 ppm)
The Packaging and Packaging Waste Directive 94/62/EC
CE Declaration to the following environmental Directives by ODM:
RoHS Directive 2011/65/EU

11. Labels and Markings

11.1. PCBA Labels and Markings

Wedge400 PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

Table 91 PCBA Label Requirements

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Meta P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

11.2. Chassis Labels and Markings

TBD

12. References (OPTIONAL)

[1] “Title”, publication year, publication journal/conference/standard, volume, pages, link to publication if available
[2] OCP Profiles - https://github.com/opencomputeproject/OCP-Profiles
[3] Redfish Interop Validator - https://github.com/DMTF/Redfish-Interop-Validator
[4] Redfish Service Validator - https://github.com/DMTF/Redfish-Service-Validator
[5] Redfish Service Conformance Check - https://github.com/DMTF/Redfish-Service-Conformance-Check

13. References (OPTIONAL)

[1] “Title”, publication year, publication journal/conference/standard, volume, pages, link to publication if available
[2] OCP Profiles - https://github.com/opencomputeproject/OCP-Profiles
[3] Redfish Interop Validator - https://github.com/DMTF/Redfish-Interop-Validator
[4] Redfish Service Validator - https://github.com/DMTF/Redfish-Service-Validator
[5] Redfish Service Conformance Check - https://github.com/DMTF/Redfish-Service-Conformance-Check

Appendix A - Requirements for IC Approval

[Note to author: appendix A must be completed by the Contributor of Baseline Specification]

List all the requirements in one summary table with links from the sections.

Requirements	**Details**	**Link to which Section in Spec**
Contribution License Agreement	Which one?	Link to Sec 1
If OWF CLA, please provide link to OWFa 1.0 Final Spec Agreement. If OCP CLA, please provide link to OCP Hardware Licence of choice.		
Tenets	Which ones? Openness Efficiency Impact Scale	Link to Sec 2
Supplier Requirements:		
Supplier must be an OCP Member.		
Supplier must become an OCP Solution Provider.		
Supplier must provide product based on this spec within 120 days		
Supplier must make product available to the PUBLIC		
Name of Supplier(s)		

Appendix B _ - OCP Supplier Information (to be provided by the Supplier of Product within 120 days)

Your product must apply for OCP Product Recognition within 120 days.

Company: Celestica
Contact Info: William Zhang
Section 701~801, Building 1, 3000 Long dong Ave., Shanghai, 201203, China.

Product Name:
Product SKU#: R1149-F0002-07

Description: Wedge400

OCP Product Recognition:
Please have your supplier complete the following 2021 Supplier Requirements before seeking OCP Product Recognition. Insert the completed spreadsheet link in the table below.

For Server Products ONLY:
For OCP Inspired™ Product Recognition, complete the following tabs:

- Supplier Details
- Security - bronze level
- HW Mgmt
- BMC (binary)

For OCP Accepted™ Product Recognition:

- Supplier Details
- Open System Firmware
- Security - silver/gold level
- HW Mgmt
- BMC (source + binary blobs)

For all other Products:

- Supplier Details
- Security (Bronze for OCP Inspired™ or Silver/Gold for OCP Accepted™)
- BMC if applicable

List all the requirements in one summary table with links from the sections.

Requirements	Details	Links
Which Product recognition?	OCP Accepted™ or OCP Inspired™	
If OCP Accepted™, who provided the Design Package?	Meta	

2021 Supplier Requirements for your product(s)		W400 Supplier