UfiSpace Distributed Disaggregated Chassis (DDC) Routing System

S9700-53DX Line Card White Box Specification

Revision 1.0

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2 Revision History

Date	Rev	Author	Summary of Change
Jan 20, 2020	R1.0	Ken Chen	First Draft Release.

3 Overview

This document describes the technical specifications of the S9700-53DX designed for Distributed Disaggregated Chassis (DDC) Routing System for telco service application.

The S9700-53DX is the best of breed robust, flexible and carrier-grade Distributed Disaggregated Chassis (DDC) line card white box router that can be deployed in the core or edge to transport services over a scalable next-gen service provider network. Equipped with 100GE service supports and 400GE fabric ports, the S9700-53DX enables fault and performance monitoring, non-stop routing support for control and data plane, and comprehensive high-availability networks.

The S9700-53DX can be positioned as standalone or coupled with the S9705-48D fabric white box router in small, medium, and large clusters enabling 4Tb to 192Tb switching capacity. By connecting to the S9705-48D (fabric white box), it scales out not only economically and rapidly, but it also brings down the total cost of ownership.

The DDC Routing System adopts the innovated discrete Network Cloud Processor (NCP or line card white box) and Network Cloud Fabric (NCF or fabric white box) building blocks providing flexibility to core router needs in the industry, integral to Ethernet switching performance and intelligence to networks while minimizing the network complexity.

Front View:

Rear View:

4 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9700-53DX DDC white box router.

4.1 Feature Summary

- Ethernet I/O ports:
  - 40 x 100GE QSFP28 ports
  - 13 x 400GE QSFPDD ports
- Front/Real panel LED indicators:
  - 2 x power status LED
  - 1 x FAN status LED
  - 1 x system status LED
  - Per port link status LED
  - Beaconing LED (2-digits 7 segment)
  - Per port FAN status LED (Rear panel on each FRU)
  - Per port PSU status LED (Rear panel on each FRU)
- Management interfaces:
  - 1 x GE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x tact switch for system reset/reload default configuration
  - 2 x 10G SFP+ management ports

4.2 Component Summary

- PCBA:
  - 1 x Switch board
  - 1 x CPU card
  - 1 x BMC card
  - 1 x FAN card
  - 1 x PSU card
  - 1 x OOB card
  - 1 x Micro-USB card
  - 1 x Beaconing LED card
- On board key components:
  - Switch Board
    - 1 x MAC Jericho2 Broadcom BCM88690
    - 1 x KBP Broadcom BCM16K
    - 10 x Gearbox Broadcom BCM81724
    - 5 x Re-timer Broadcom BCM81358
    - 1 x PCIe switch Broadcom PEX8724
    - 1 x 10GE PHY Inphi CS4227
    - 1 x BMC AST2400
    - 1 x PCIe NIC controller I210-IT for CPU
  - CPU Card
    - 1 x CPU Broadwell-DE D-1548 with 8-core @ 2.0GHz
    - 4 x DDR4 RDIMM with ECC module support up to 4 x 32GB (Alpha : 2 x 32GB)
    - 2 x M.2 2280 SATA3 SSD module support up to 2 x 128GB (Alpha : 1 x 128GB)
- PSU & FAN:
  - 2x 2000W slim PSUs with redundancy support

- 4x 8038 FAN tray modules with redundancy support

4.3 Switch Board Functional Block Diagram

The S9700-53DX system functional block diagram is shown as below:

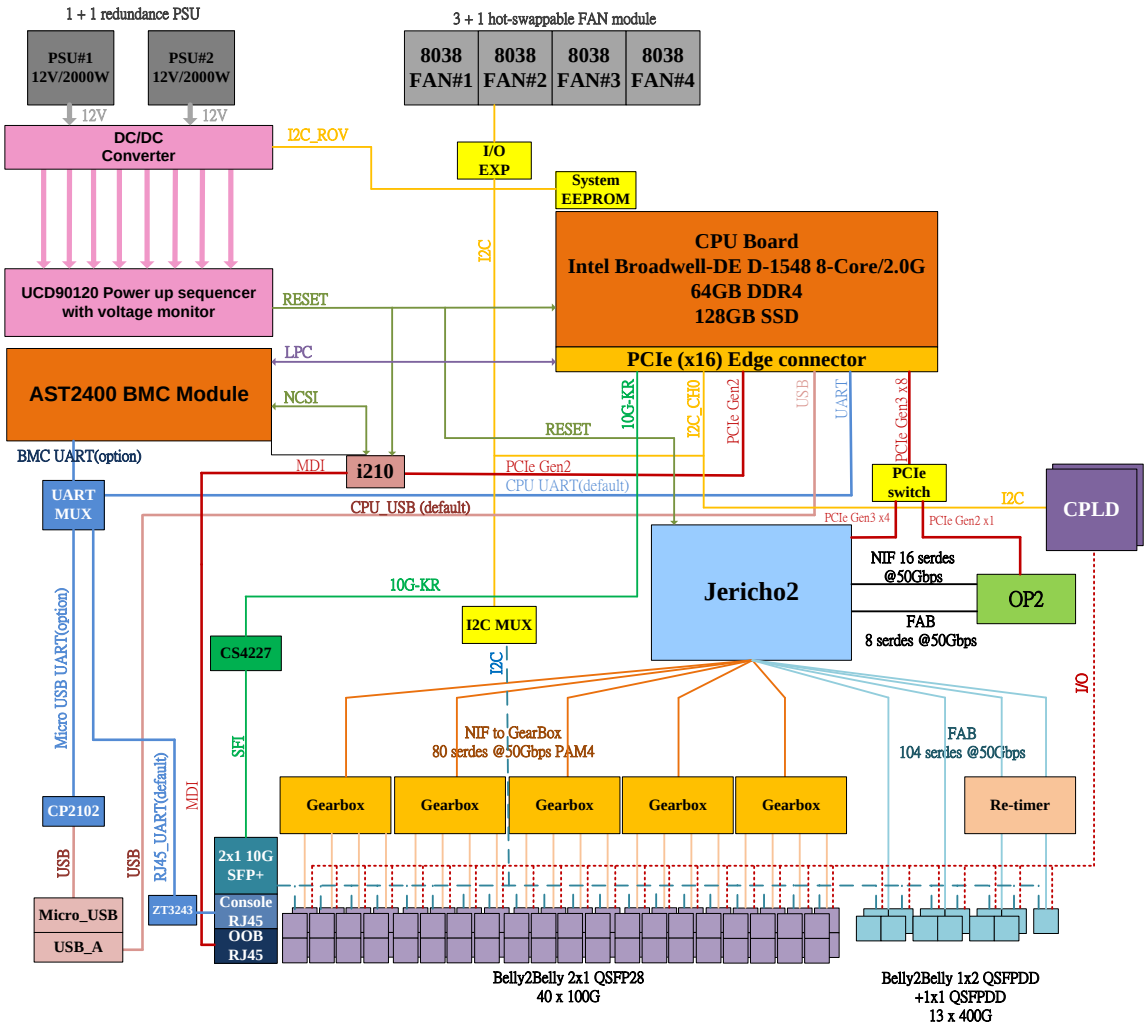


Figure 4-1 Switch Board Block Diagram

The S9700-53DX main board placement is shown as below:

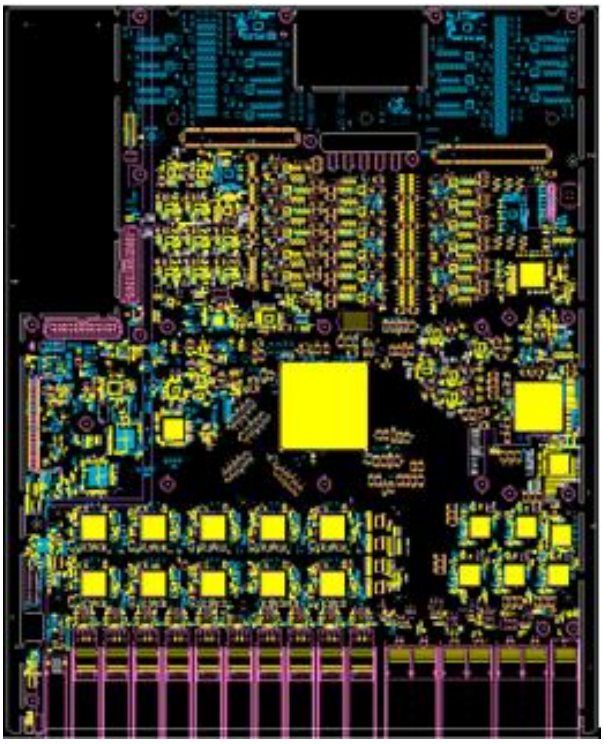


Figure 4-2 Switch Board PCB Layout

4.4 CPU Card Functional Block Diagram

The S9700-53DX CPU card block diagram is shown as below:

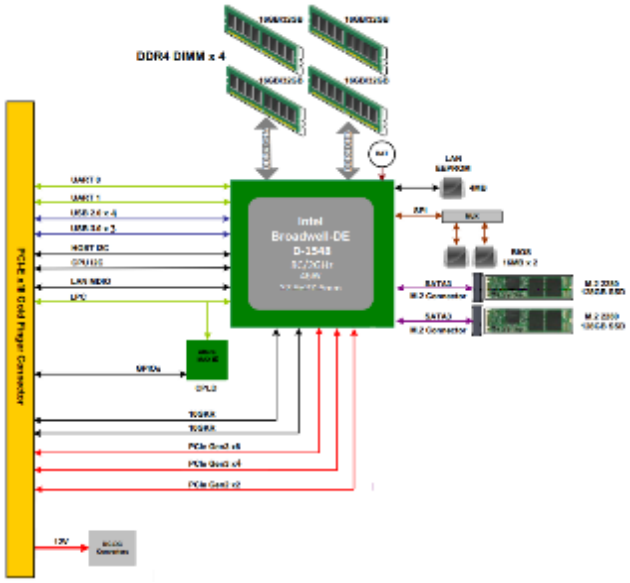


Figure 4-3 CPU Board Functional Block Diagram

CPU card placement is shown as below:

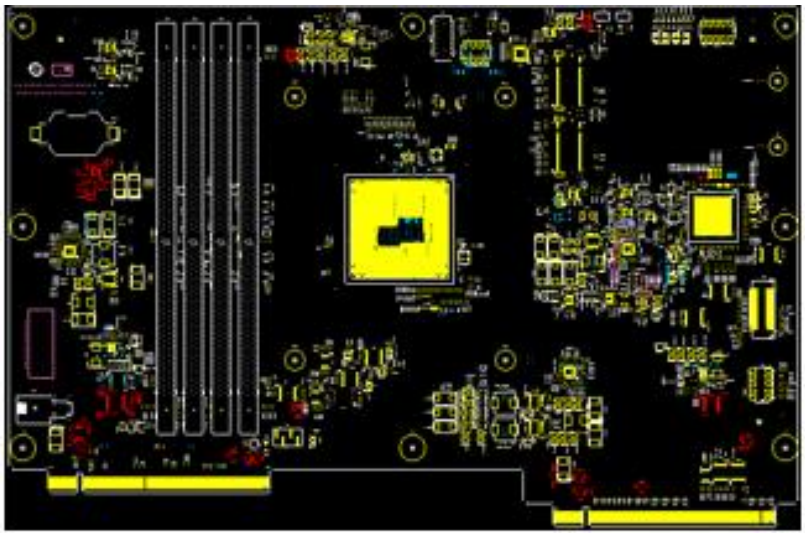


Figure 4-4 CPU Board PCB Layout

4.5 Mechanical Outline

The S9700-53DX is designed to meet cabinet with 19’’ depth installation requirement. This 2RU systemmechanical dimension is: 436mmx762mmx87.7mm (WxDxH).

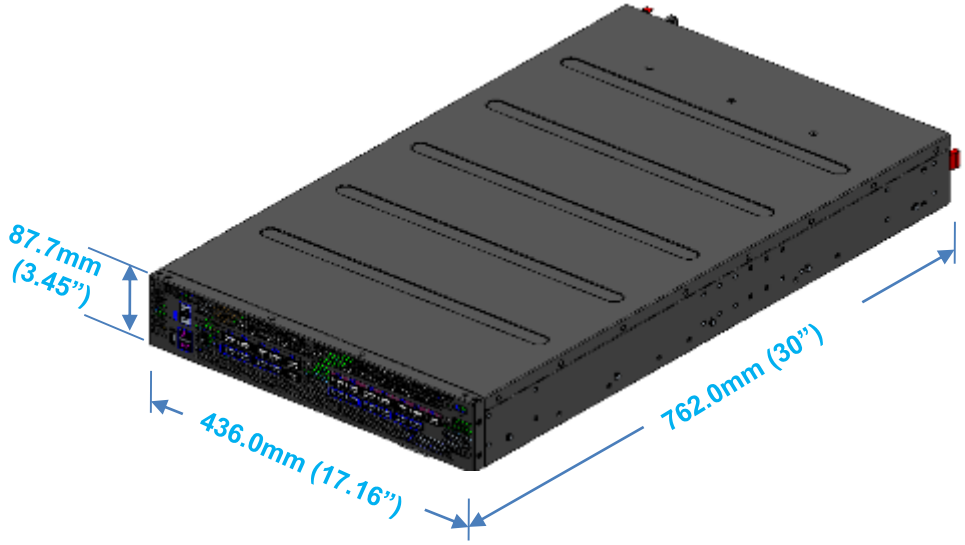


Figure 4-5 S9700-53DX Mechanical Outline

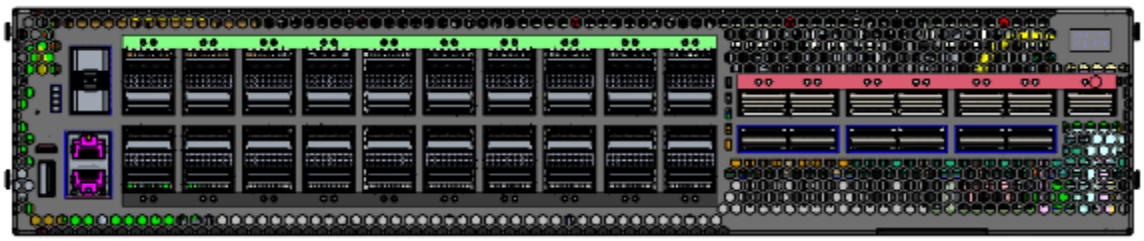


Figure 4-6 S9700-53DX Front View

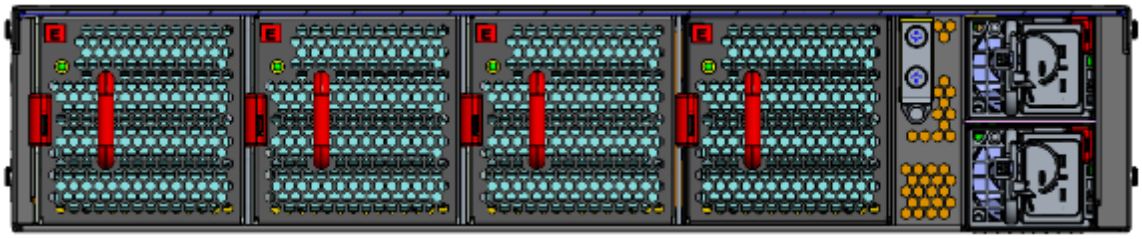


Figure 4-7 S9700-53DX Rear View

The S9700-53DX system top view without top cover is shown as below:

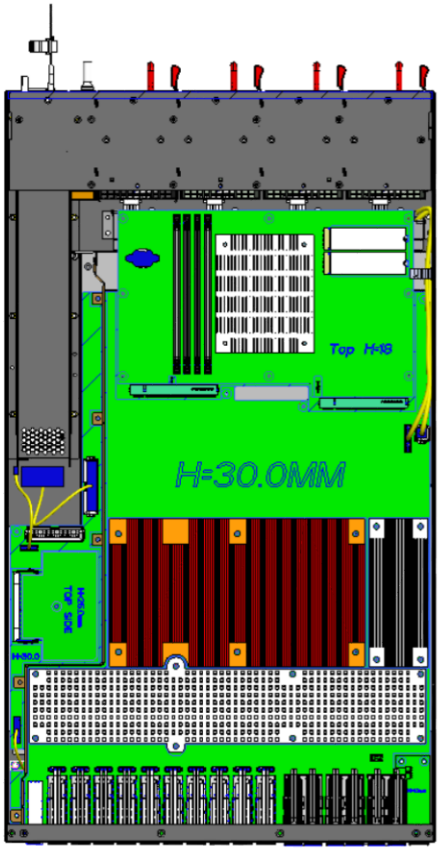


Figure 4-8 S9700-53DX System Top View

5 Hardware Architecture

This section will focus on detailed description of each major component used on the S9700-53DX.

5.1 CPU Subsystem

Intel's x86 embedded SoC processor Broadwell-DE D-1548 is equipped on S9700-53DX CPU board. The major onboard components and interfaces to switch board are listed as below:

- Intel's Broadwell-DE Processor
  - ✓ Capable of supporting up to 16-core processor
  - ✓ Four DDR4 ECC RDIMMs, up to 128GB
  - ✓ Two M.2 22*80mm SSD module up to 256GB
  - ✓ Dual 16MB SPI boot/BIOS flash components
- Two PCIe gold fingers to switch board
  - ✓ Single x8 PCIe Gen3 interface
  - ✓ Single x4 PCIe Gen3 interface
  - ✓ Single x2 PCIe Gen2 interface
  - ✓ Single SATA Gen3 interface
  - ✓ Two 10G-KR Ethernet interfaces
  - ✓ Two UART interfaces
  - ✓ Three USB3 interfaces
  - ✓ Single LAN MDC/MDIO interface
  - ✓ Two SM Bus interfaces

5.1.1 CPU Broadwell-DE

The key features of processor D-1548 product family are shown as below:

- The max base frequency running at 2.2GHz.
- 3 levels caching for the processor
  - ✓ Instruction Cache Unit (ICU) and Data Cache Unit (DCU): 32 KB each (64 KB total)
  - ✓ Mid-Level Cache (MLC) per core: 256 KB (instructions and data)
  - ✓ Last Level Cache (LLC) per socket: Up to 1.5 MB per Cbo (instructions and data)
- Two channels Integrated Memory Controller (IMC) for DDR3/DDR4 DIMMs
  - ✓ Supports 2 Gb and 4 Gb DRAM technologies with DDR3 (DDR3L only at 1.35V)
  - ✓ Supports 4 Gb and 8 Gb DRAM technologies with DDR4
- The Integrated I/O module provides PCIe interface
  - ✓ PCIe Gen3 speeds at 8 GT/s (no 8b/10b encoding)
  - ✓ X16 interface bifurcated down to two x8 or four x4 (or combinations)
  - ✓ X8 interface bifurcated down to two x4
- Two Integrated 10 GE Controllers (MAC)
  - ✓ KX4 PHY supports:
    - – XAUI for XGMII extension (clause 47 of 802.3)
    - – 10GBASE-KX4 for gigabit backplane applications (IEEE802.3 clause 71)
    - – 2500BASE-KX for gigabit backplane applications
    - – 1000BASE-KX for gigabit backplane applications (IEEE802.3 clause 70)
  - ✓ KR PHY supports:
    - – 10GBASE-KR for gigabit backplane applications (IEEE802.3 clause 72)
    - – 1000BASE-KX for gigabit backplane applications (IEEE802.3 clause 70)
    - – 10GBASE SFP+ through a XFI compatible interface
    - – 10GBASE-T through a XFI compatible interface
- The Integrated PCH Logic provides extensive I/O support.
  - ✓ Eight ports PCIe GEN2 speeds up to 5 GT/s

- ✓ ACPI Power Management Logic Support, Revision 4.0a
- ✓ Enhanced DMA controller, interrupt controller, and timer functions
- ✓ Integrated SATA host controllers with independent DMA operation on up to six ports
- ✓ xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
- ✓ One legacy EHCI USB controller provides a USB debug port.
- ✓ Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- ✓ Version 2.0 SMBus with additional support for I2C devices
- ✓ Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- ✓ Supports Intel® Trusted Execution Technology (Intel® TXT)
- ✓ Integrated Clock Controller
- ✓ Low Pin Count (LPC) interface
- ✓ Firmware Hub (FWH) interface support
- ✓ Serial Peripheral Interface (SPI) support
- ✓ JTAG Boundary Scan support

5.1.2 DDR4 RDIMM

Four DDR4 RDIMM slots are designed in, up to 2400 MT/s are supported with both DIMMs populated. 8GB, 16GB and 32GB single rank (“1R”) and dual rank (“2R”).

Two 16GB R-DIMM modules are populated on the S9700-53DX CPU card by default.

5.1.3 SPI Boot Flash

There are two SPI boot flashes for Broadwell-DE BIOS storage. In manufacture, both of these two components store the same BIOS image. By default, system boots from primary SPI flash (#0). It will swap to backup SPI flash (#1) when system boot up fail from primary flash.

Dual boot flash design is also useful for system BIOS upgrade, in the case of the flash is crash during firmware upgrade, it will be recovered by the original image stored in the backup flash.

These two BIOS flashes are connected to the same SPI bus with two dedicated chip select (CS#) signals see figure below for SPI connection.

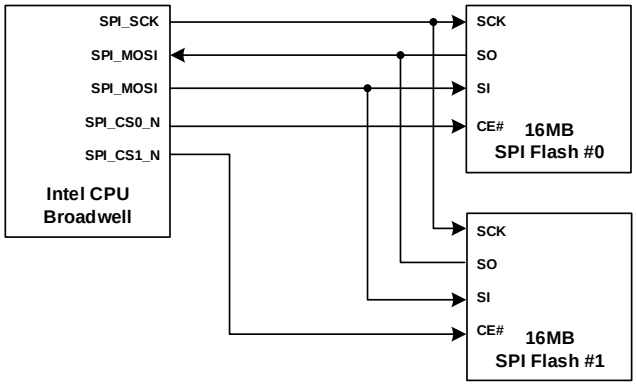


Figure 5-1 Intel Broadwell-DE BIOS Flash Connection

5.1.4 SATA M.2 SSD

The Broadwell-DE SoC contains Gen3 serial ATA ports capable of independent DMA operation. The SATA controllers are completely software transparent with an IDE Interface. Two M.2 connectors withM.2 22*80mm 128GBSSD are populated on CPU card.

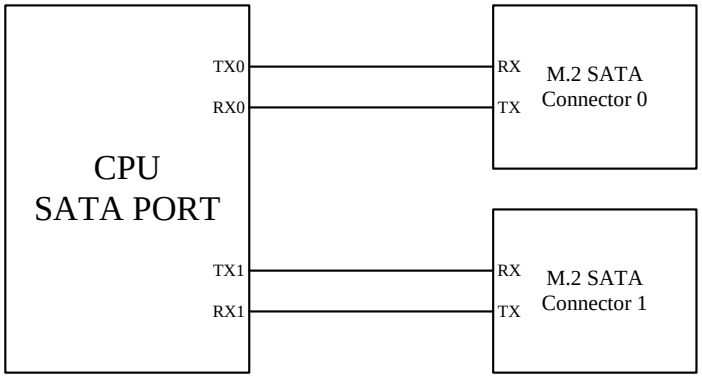


Figure 5-2 Intel Broadwell-DE SATA SSD Connection

5.1.5 USB

The SoC supports up to 4 USB 3.0 cable ports to provide support for SuperSpeed USB devices. In addition, the SoC supports up to 4 USB 2.0 ports that can be used to connect to high-speed, full-speed and low-speed USB devices. The SoC incorporates an XHCI controller and another EHCI controller. The four USB 3.0 ports are mapped to 4 of the existing USB 2.0 ports in the controller. USB 2.0 allows data transfers up to 480 Mb/s, and USB 3.0 up to 5 Gb/s. All USB interfaces are connected to PCIe golden finger.

USB Controller	Port Number	Net Name	Function description
PCI Device 29 Function 0(TBU)	1	USB2_PCH_P0_DN USB2_PCH_P0_DP	USB 2.0
	2	USB2_PCH_P1_DN USB2_PCH_P1_DP	USB 2.0
	3	USB2_PCH_P2_DN USB2_PCH_P2_DP	USB 2.0
PCI Device 20 Function 0(TBU)	1	USB3_RX_P0_N USB3_RX_P0_P USB3_TX_P0_N USB3_TX_P0_P	USB 3.0
	2	USB3_RX_P1_N USB3_RX_P1_P USB3_TX_P1_N USB3_TX_P1_P	USB 3.0
	3	USB3_RX_P2_N USB3_RX_P2_P USB3_TX_P2_N USB3_TX_P2_P	USB 3.0

Table 5-1 Broadwell-DE USB connection

5.1.6 DC/DC Power

CPU card is sourced by 12V DC power, which is delivered from switch board. All power rails for CPU, R-DIMM & SSD etc. components are converted by onboard DC/DC regulators. DC/DC power convertor design is shown as below:

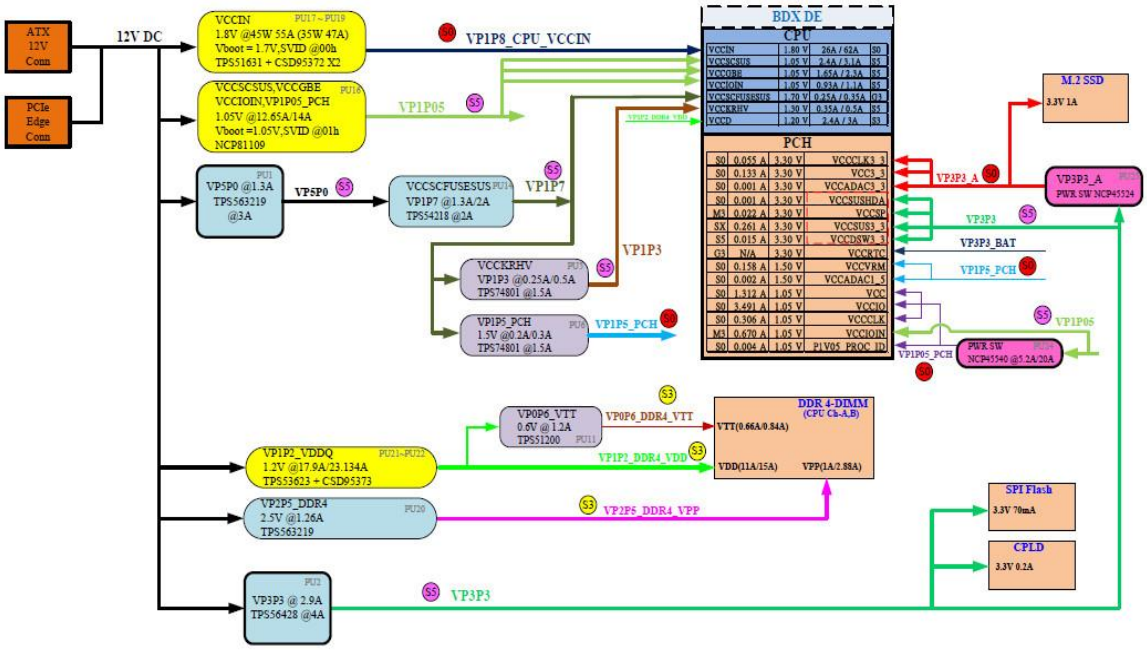


Figure 5-3 CPU Card DC/DC Power Distribution Diagram

5.1.7 Clock Distribution

The integrated clock generator of Broadwell-DE provides 33MHz and 100MHz clock outputs to PCI and PCIe components, all other clocks for core, memory controllers, SDRAMs, SPI flash and SMBus are also generated by internal clock controller. No external clock generator is needed.

Only two 25MHz XTALs and one 32.768 KHz XTAL are populated on CPU card.

Figure below shows CPU card clock distribution design.

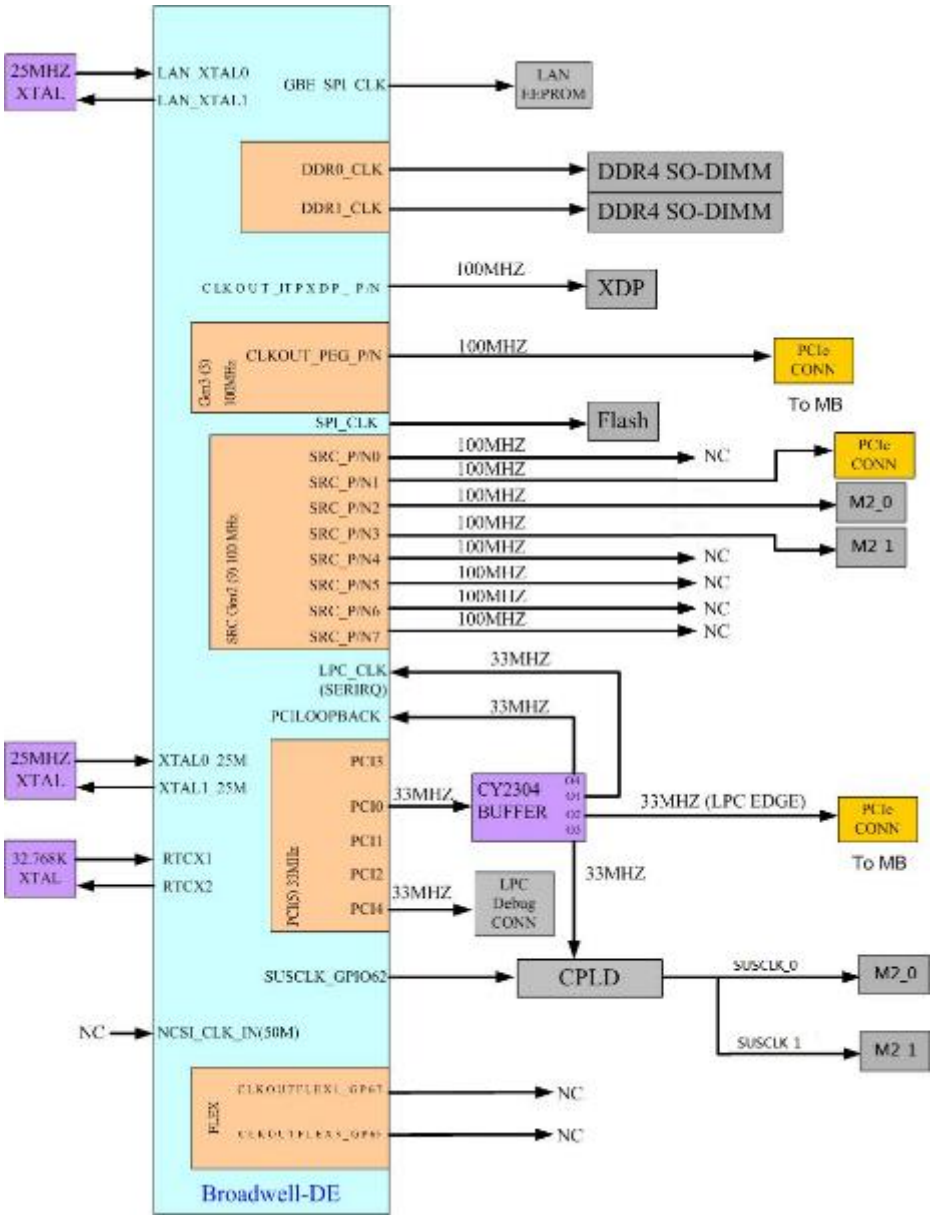


Figure 5-4 CPU Card Clock Distribution Diagram

5.1.8 Reset Control

CPU reset is controlled by onboard CPLD, reset pin will be de-asserted once all DC/DC power rails are converted by expected. CPU can also be reset by tact switch button located on the left of front panel.

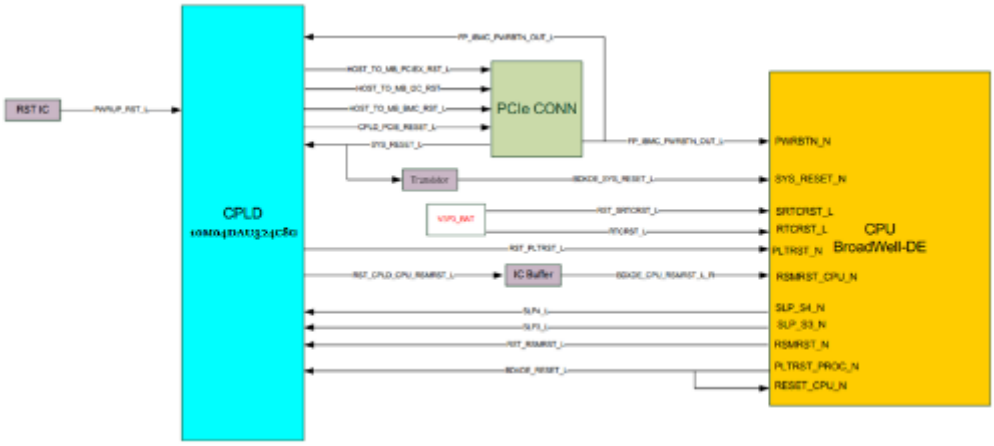


Figure 5-5 CPU Card Reset Diagram

5.1.9 SMBus/I2C Interface

There are two SMBus/I2C interfaces for CPU card and switch board components management.

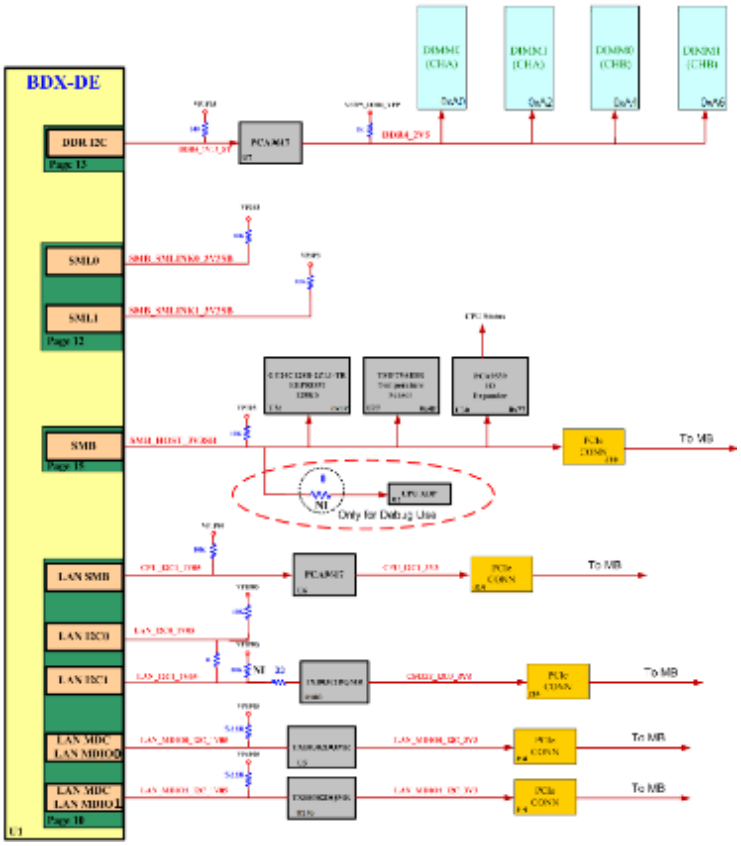


Figure 5-6 CPU Card SMBus/I2C Interfaces Diagram

5.1.10 CPU Straps

STRAP NAME	DEFAULT	DESCRIPTION
BOOT BIOS STRAPS (GP19, GP51)	1,1	BOOT BIOS DESTINATION 0 1 RESERVED 1 0 RESERVED 1 1 SPI (DEFAULT) 0 0 LPC
DMI_TERMINATION	0	DMI TX TERMINATION WHEN DCCOUPLED MODE. 0 = DMI TX IS TERMINATED TO VSS. 1 = DMI TX IS TERMINATED TO VCC/2.
BIOS_ADV_FUNCTIONS	0	DMI RX TERMINATION WHEN AC-COUPLED MODE: 0 = DMI RX IS TERMINATED TO VSS.(DEFAULT) 1 = DMI RX IS TERMINATED TO VCC/2.
GSXDIN	0	DMI AC OR DC COUPLING? 0 = DMI IS IN AC-COUPLING MODE (SERVER/WORKSTATION ONLY, NOT MEANT FOR DESKTOP/MOBILE) 1 = DMI IS IN DC-COUPLING MODE (DESKTOP, MOBILE OR SERVER/WORKSTATION).
ADR_TRIGGER	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
SUSCLK	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
NCSI_TRI_EN CPU2PCH_THROT SPARE[0]	0,0,0	STRAPS HERE TO IDENTIFY WHICH SOCKET IS WHICH IN ORDER FOR PECI TO WORK
SPARE[1]	0	THIS IS THE DISABLE TO THE SC PCU RESET FSM 0 = PMC FSB BRINGS UP SOUTH COMPLEX 1 = PCODE BRINGS UP SOUTH COMPLEX OF PMC
SPARE[2]	0	BYPASSES THE CRYSTAL CLOCK TO THE SCPLL 0 = PICKS THE 25MHZ KR CRYSTAL CLOCK AS THE REFERENCE TO SCPLL (DEFAULT) 1 = FORCES THE TEST CLOCK FROM TSTCLK_SC PINS
SPARE[3]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NO TEST CLOCK OVERRIDE (DEFAULT) 1 = TEST CLOCK OVERRIDE
SPARE[4]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NORMAL REFERENCE CLOCK PATH WITH CR BASED REFERENCE CLOCK SELECTION (DEFAULT) 1 = FORCE "REGULAR" REFERENCE CLOCKS TO BE SENT TO THE KX4 PLLS
UART_TXD[0]	0	JTAG PORT FOR NORTH COMPLEX TAP 0 = GB#_SDP* PINS ARE USED AS FUNCTIONAL PIN OR CAN BE USED FOR SC TAPS THROUGH TAP PROGRAMMING. (DEFAULT) 1 = PINS ARE USED AS JTAG PORT FOR NC TAP
UART_TXD[1]	0	CONTROLS THE SECURITY ATTRIBUTES ON THE NVM – FOR PRE-PRODUCTION USAGE 0 = DISABLES NVM SECURITY (DEFAULT) 1 = SECURITY ENABLED

STRAP NAME	DEFAULT	DESCRIPTION
NCSI_ARB_OUT	1	USING COMBINED P1V05
DSWODVREN	1	0 = DISABLE INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR. THIS MODE IS ONLY SUPPORTED FOR TESTING ENVIRONMENTS. 1 = ENABLE DSW 3.3V-TO-1.05V INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR.
NCSI_RXD_1	0	ENABLE/DISABLE MANAGEBILITY TRAFFIC 0 = LAN AVAILABLE IN S5 FOR WOL (DEFAULT) 1 = LAN NOT AVAILABLE IN S5. MANAGEBILITY DISABLED.
INTVRMEN	1	INTEGRATED VRMS 0 = DCPSUS1, DCPSUS2 AND DCPSUS3 ARE POWERED FROM AN EXTERNAL POWER SOURCE. SERVERS SHOULD NOT PULL THE STRAP LOW. 1 = INTEGRATED VRMS ENABLED.
10GBE_MDIO_DIR_CTL_0 10GBE_MDIO_DIR_CTL_1	1,1	00 = BOTH LAN PORTS ARE DISABLED. 01 = PORT 1 IS DISABLED. PORT 0 IS ENABLED. 10 = RESERVED 11 = BOTH PORT0 & 1 ARE ENABLED. (DEFAULT)
DDR3_4_STRAP	1	1 = DDR4 0 = DDR3
TXT_PLTEN	1	(INTEL? TXT) PLATFORM ENABLE STRAP. 0 = THE PLATFORM IS NOT INTEL TXT ENABLED. 1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED
TXT_AGENT	1	TXT AGENT (DRIVES TXT TRANSANCTIONS): 1 = CPU IS TXT_AGENT 0 = CPU IS NOT TXT_AGENT
BIST_ENABLE	1	BUILT-IN SELF TEST (BIST): 1 = BIST ENABLED 0 = BIST DISABLED
SAFE_MODE_BOOT	0	SAFE MODE BOOT (DISABLE CLOCK GATING): 1 = SAFE MODE BOOT ENABLED 0 = SAFE MODE BOOT DISABLED

5.1.11 Memory and I/O Mapping

Fixed I/O ranges decoded by Broadwell-DE:

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA

0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA

92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Fixed I/O ranges decoded by Broadwell-DE:

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	64	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	16	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	32	SMB unit
TCO	96 bytes above ACPI base	32	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	32	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Memory decode ranges from processor perspective:

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set

FFC8 0000h-FFCF FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh FF90	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh FF98	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh FFA0	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh	LPC or SPI (or PCI)	Always enabled.
FF70 0000h–FF7F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0
1 KB anywhere in 4 GB range	USB EHCI Controller #1	Enable using standard PCI mechanism
64 KB anywhere in 4 GB range	USB xHCI Controller	Enable using standard PCI mechanism
FED0 X000h–FED0 X3FFh	High Precision Event	BIOS determines “fixed” location which is
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere	PCI Bridge	Enable using standard PCI mechanism
Prefetchable Memory	PCI Bridge	Enable using standard PCI mechanism
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic
32 Bytes anywhere in 64-bit	SMBus	Enable using standard PCI mechanism
2 KB anywhere above 64 KB to	SATA Host Controller #1	AHCI memory-mapped registers. Enable
Memory Base/Limit anywhere	PCI Express* Root Ports 1-8	Enable using standard PCI mechanism
Prefetchable Memory	PCI Express Root Ports 1-8	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
16 Bytes anywhere in 64-bit	Intel® MEI #1, #2	Enable using standard PCI mechanism
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism
16 KB anywhere in 4 GB range	Root Complex Register	Enable using setting bit[0] of the Root

5.2 BMC Subsystem

In the S9700-53DX, the base board management controller (BMC) autonomously monitors system’s health including temperature, voltage, fan speed, etc. We use the DDR4 SO-DIMM connector as the BMC module connector. The BMC module connector is on the main board PCBA:

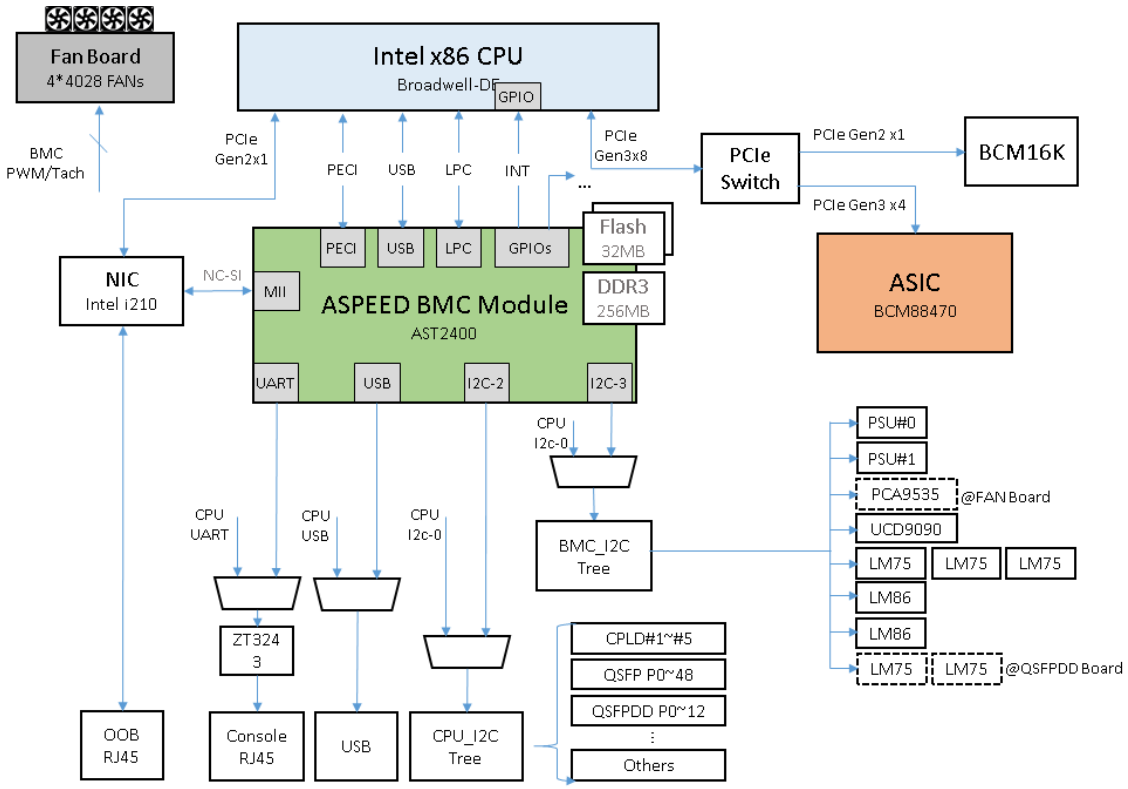


Figure 5-7 BMC Block Diagram

5.2.1 Key Interfaces and Configurations

5.2.1.1 LPC

Low-Pin-Count interface is an important interface for communication among Broadwell-DE, CPLD on CPU Board and BMC. The OS running in x86 use this interface to communicate with BMC's IPMI message handler.

5.2.1.2 USB

AST2400 provides three USB interfaces for different functional objectives. All USB controllers of AST2400 meet USB specification revision 2.0 and 1.1 and also compliant with EHCI and UHCI specification. USB MUX is controlled by BMC and IOExp (U105) on main board.

5.2.1.3 UART

AST2400 supports up to 5 sets UART IO interface with full flow control pins, and 1 set with Tx/Rx only for BMC console. The administrator can switch x86 and BMC console easily and choose to connect to front panel console RJ45 or micro-USB connector. Also the BMC console could be disabled by command. It also supports SOL, host console is able to be decoded by Super I/O integrated in AST2400 via LPC interface. UART MUX is controlled by BMC and IOExp(U105) on main board.

5.2.1.4 I2C

AST2400 integrates up to 14 sets of multi-function I2C/SMBus bus controllers used to collect voltage, temperature, FRU and manufacture information. The S9700-53DX implements two I2C trees for

management: CPU_I2C tree and BMC_I2C tree. Both two I2C trees could be accessed by CPU or BMC, but in default configuration BMC only accesses the BMC_I2C tree. The CPLD on main switch board will take the arbitration.

It monitors system's health continuously after it boots up. BMC should record and handle the event when sensor's values are out of reasonable range.

5.2.1.5 PWM/Tacho

AST2400 integrates up to 8 sets of PWM outputs and 16 tachometer inputs. In the S9700-53DX, the BMC implements 4 Fans in 3+1 redundancy.

5.3 Switching Subsystem

This section details switch board component features/functionalities summary and hardware system design.

5.3.1 Network Ports Design

This section describes the data path for each Ethernet fiber port and the management path for each PHY.

5.3.1.1 MIIM Interface Block Diagram

There are ten reverse gearboxes (BCM81724) for 100G ports and five re-timers (BCM81358) for last five 400GE ports, they are connected to dedicated MIIM interface and are directly managed by MAC, controlled by CPU.

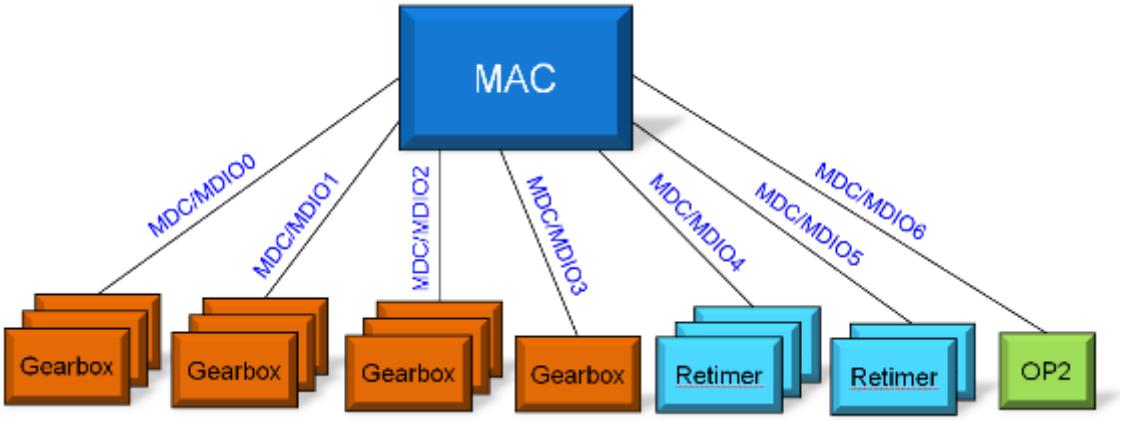


Figure 5-8 Physical Ports Assignment

5.3.1.2 Network Port Path Configuration

This section shows the physical port location assignment and Ethernet data path.

5.3.1.2.1 Physical Port Location Assignments

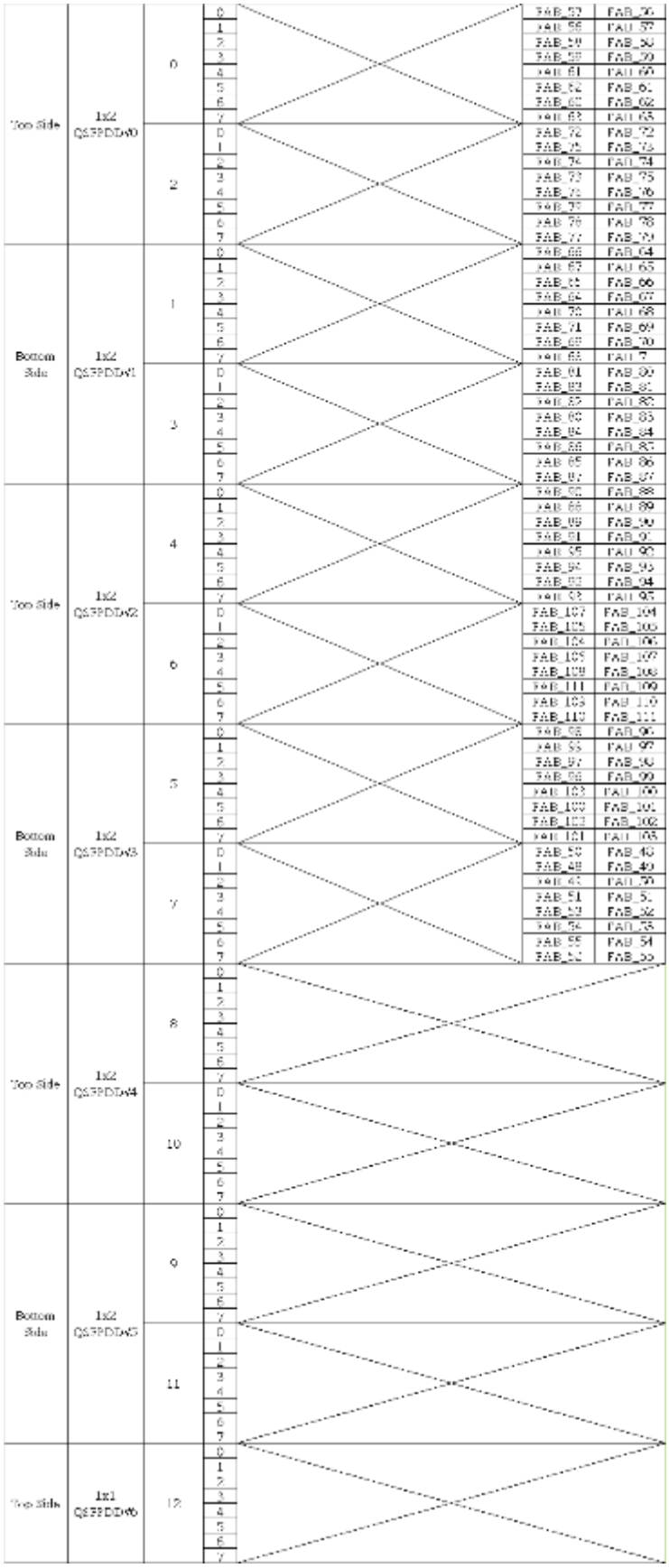
Figure 5-9 Physical Ports Assignment

5.3.1.2.2 Optical Ports Data, Management Path

Please find the following table for detail. The port mapping includes MAC, Gearbox, Re-timer, and KBP connection.

Port Panel				Reverse Gearbox mode					
				PHY				MAC	
						Line side		Host side	
Connector		Physical port	Lane	MDIO Bus [7:5]	MDIO Address [4:2]	TX Lane	RX Lane	TX Lane (OIF/FAR)	RX Lane (OIF/FAR)
Top Side	Port QSFP28#0	0	0	0	001	0	0	NL2_02	NL2_02
			1			1	1		
			2			2	2	NL2_03	NL2_01
			3			3	3		
		1	0			8	8	NL2_04	NL2_04
			1			9	9		
			2			10	10	NL2_05	NL2_06
			3			11	11		
Bottom Side	Port QSFP28#1	20	0			12	12	NL2_06	NL2_07
			1			13	13		
			2			14	14	NL2_07	NL2_05
			3			15	15		
		21	0			4	4	NL2_01	NL2_00
			1			5	5		
			2			6	6	NL2_00	NL2_03
			3			7	7		
Top Side	Port QSFP28#2	2	0		010	0	0	NL2_08	NL2_09
			1			1	1		
			2			2	2	NL2_09	NL2_08
			3			3	3		
		1	0			8	8	NL2_12	NL2_14
			1			9	9		
			2			10	10	NL2_13	NL2_12
			3			11	11		
Bottom Side	Port QSFP28#3	22	0			12	12	NL2_14	NL2_13
			1			13	13		
			2			14	14	NL2_15	NL2_15
			3			15	15		
		23	0			4	4	NL2_10	NL2_10
			1			5	5		
			2			6	6	NL2_11	NL2_11
			3			7	7		
Top Side	Port QSFP28#4	4	0		011	0	0	NL2_16	NL2_19
			1			1	1		
			2			2	2	NL2_17	NL2_18
			3			3	3		
		5	0			8	8	NL2_20	NL2_20
			1			9	9		
			2			10	10	NL2_21	NL2_22
			3			11	11		
Bottom Side	Port QSFP28#5	24	0			12	12	NL2_22	NL2_21
			1			13	13		
			2			14	14	NL2_23	NL2_23
			3			15	15		
		25	0			4	4	NL2_18	NL2_17
			1			5	5		
			2			6	6	NL2_19	NL2_16
			3			7	7		

Top Side	2x1 QSFP28#6	6	0	1	100	0	0	XIF_24	XIF_27
			1			1	1		
			2			2	2	XIF_25	XIF_25
			3			3	3		
		7	0			8	8	XIF_28	XIF_28
			1			9	9		
			2			10	10	XIF_29	XIF_29
			3			11	11		
Bottom Side	2x1 QSFP28#7	36	0			12	12	XIF_30	XIF_30
			1			13	13		
			2			14	14	XIF_31	XIF_31
			3			15	15		
		37	0			4	4	XIF_26	XIF_26
			1			5	5		
			2			6	6	XIF_27	XIF_24
			3			7	7		
Top Side	2x1 QSFP28#8	8	0			0	0	XIF_32	XIF_35
			1			1	1		
			2			2	2	XIF_34	XIF_33
			3			3	3		
		9	0			8	8	XIF_36	XIF_36
			1			9	9		
			2			10	10	XIF_37	XIF_37
			3		10	11	11		
Bottom Side	2x1 QSFP28#9	38	0	1		12	12	XIF_38	XIF_38
			1			13	13		
			2			14	14	XIF_39	XIF_39
			3			15	15		
		39	0			4	4	XIF_38	XIF_39
			1			5	5		
			2			6	6	XIF_35	XIF_34
			3			7	7		
Top Side	2x1 QSFP28#10	10	0			0	0	XIF_40	XIF_41
			1			1	1		
			2			2	2	XIF_41	XIF_40
			3			3	3		
		11	0			8	8	XIF_44	XIF_44
			1			9	9		
			2			10	10	XIF_45	XIF_47
			3			11	11		
Bottom Side	2x1 QSFP28#11	30	0		00	12	12	XIF_46	XIF_46
			1			13	13		
			2			14	14	XIF_47	XIF_45	
			3			15	15		
		31	0			4	4	XIF_43	XIF_43
			1			5	5		
			2			6	6	XIF_42	XIF_42
			3			7	7		
Top Side	2x1 QSFP28#12	12	0			0	0	XIF_80	XIF_88
			1			1	1		
			2			2	2	XIF_81	XIF_89	
			3			3	3		
		13	0			8	8	XIF_82	XIF_82
			1			9	9		
			2			10	10	XIF_83	XIF_83
			3		010	11	11		
Bottom Side	2x1 QSFP28#13	32	0			12	12	XIF_92	XIF_92
			1			13	13		
			2			14	14	XIF_93	XIF_93	
			3			15	15		
		33	0			4	4	XIF_90	XIF_90
			1			5	5		
			2			6	6	XIF_91	XIF_91
			3			7	7		
Top Side	2x1 QSFP28#14	14	0			0	0	XIF_81	XIF_81
			1			1	1		
			2			2	2	XIF_80	XIF_80	
			3			3	3		
		15	0			8	8	XIF_87	XIF_85
			1			9	9		
			2			10	10	XIF_86	XIF_86
			3	2	011	11	11		
Bottom Side	2x1 QSFP28#15	34	0			12	12	XIF_85	XIF_87
			1			13	13		
			2			14	14	XIF_84	XIF_84	
			3			15	15		
		35	0			4	4	XIF_80	XIF_82
			1			5	5		
			2			6	6	XIF_83	XIF_83
			3			7	7		
Top Side	2x1 QSFP28#16	16	0			0	0	XIF_74	XIF_72
			1			1	1		
			2			2	2	XIF_73	XIF_73
			3			3	3		
		17	0			8	8	XIF_79	XIF_77
			1			9	9		
			2			10	10	XIF_78	XIF_78
			3		100	11	11		
Bottom Side	2x1 QSFP28#17	36	0			12	12	XIF_77	XIF_76
			1			13	13		
			2			14	14	XIF_76	XIF_76
			3			15	15		
		37	0			4	4	XIF_75	XIF_74
			1			5	5		
			2			6	6	XIF_72	XIF_75
			3			7	7		
Top Side	2x1 QSFP28#18	18	0			0	0	XIF_66	XIF_64
			1			1	1		
			2			2	2	XIF_65	XIF_65
			3			3	3		
		19	0			8	8	XIF_70	XIF_71
			1			9	9		
			2			10	10	XIF_71	XIF_70
			3	3	101	11	11		
Bottom Side	2x1 QSFP28#19	38	0			12	12	XIF_68	XIF_69
			1			13	13		
			2			14	14	XIF_69	XIF_68
			3			15	15		
		39	0			4	4	XIF_67	XIF_66
			1			5	5		
			2			6	6	XIF_64	XIF_67
			3			7	7		



5.3.2 DC/DC Power Design

Power distribution diagram is shown as below :

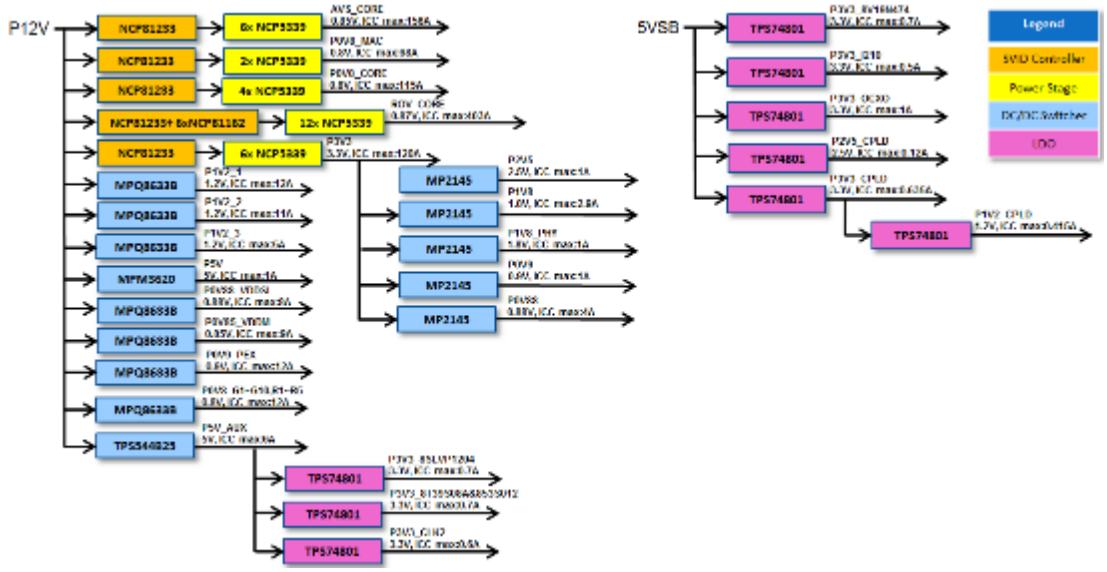


Figure 5-10 S9700-53DX System Power Distribution Diagram

System clock diagram is shown as below:

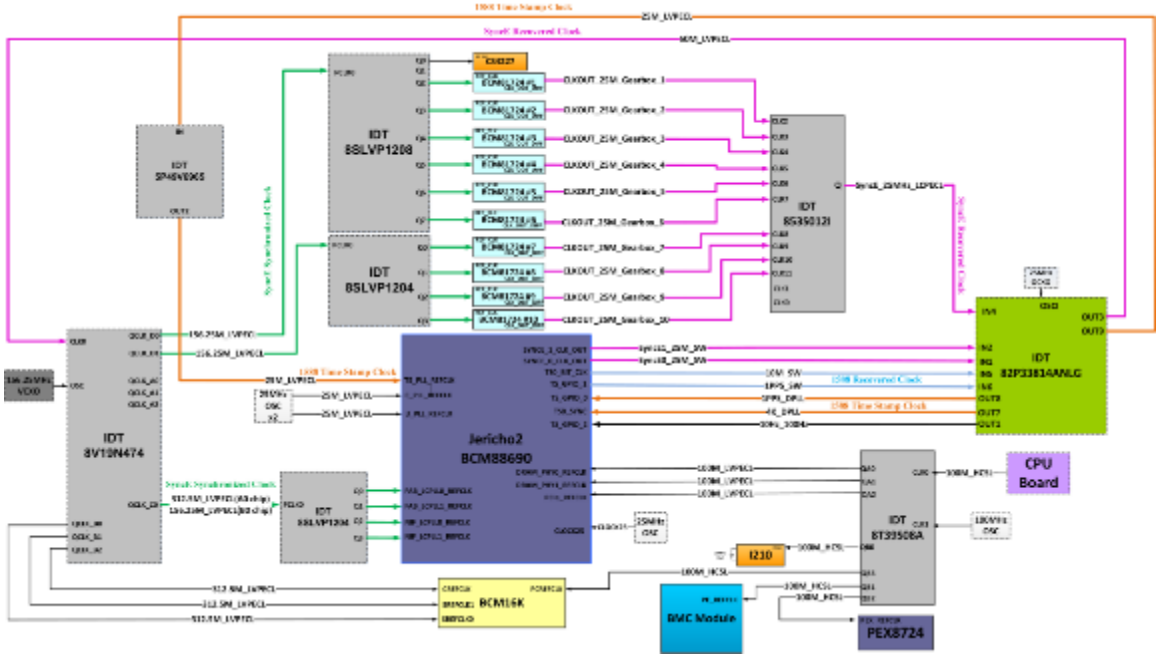


Figure 5-11 S9700-53DX Switch Board Clock Diagram

5.4 System Management

5.4.1 System I²C Interface

There are two major I2C buses on S9700-53DX card, one is CPU_I2C bus, and another one is BMC_I2C. Both CPU and BMC can access the buses but they need to negotiation to each other and always only one host can access the buses. The features of these two buses:

- CPU_I2C: Access to I2C devices including CPLDs, I/O Ports, peripherals.
- BMC_I2C: Access to I2C devices including PSU, FAN, thermal sensors.

There is one dedicated CS4227_I2C bus from CPU and this bus is used for controlling 10G PHY and SFP+ LED control.

I2C block diagram is shown as below:

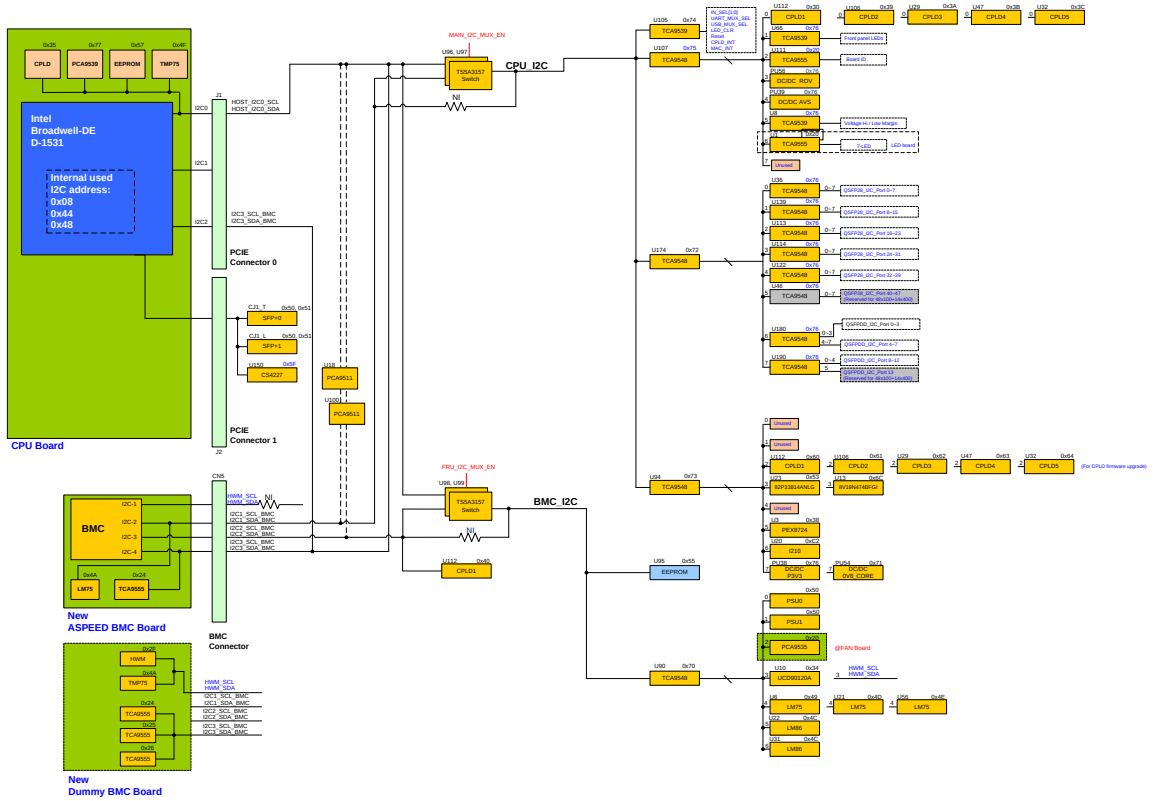


Figure 5-12 I²C Bus Connection Diagram

CPU_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
CPU_I2C	I/O EXP	111-0100	0x74	TCA9539	0.7	8V19N474_INT
					0.6	UART_MUX1_SEL
					0.5	UART_MUX2_SEL
					0.4	USB_MUX_SEL

I2C Bus	Name	Address		Device	Bit #	Function
					0.3	HOST_TO_BMC_I2C_GPIO
					0.2	LED_CLR
					0.1	EXP_J2_PCIE_RST_L
					0.0	9539_J2_RST_L
					1.7	I210_RST_L
					1.6	I210_PE_RST_L
					1.5	OP2_INT_L
					1.4	CPLD01_TO_CPU_INT_L
					1.3	CPLD2_TO_CPU_INT_L
					1.2	CPLD3_TO_CPU_INT_L
					1.1	CPLD4_TO_CPU_INT_L
					1.0	J2_INT_L
	I2C MUX	111-0001	0x75	TCA9548	--	CPLDs, System LEDs, Board ID, CPLDs DC/DC ROV, DC/DC AVS, Voltage Margin
	I2C MUX	111-0010	0x72	TCA9548	--	I2C of QSFP28 Port 1~40 I2C of QSFPDD Port 1 ~13
	I2C MUX	111-0011	0x73	TCA9548	--	CPLD upgrade Clock Gens. PCIE switch, PEX8716 Ethernet controller, I210 DC/DC P3V3, DC/DC 0V8_CORE
	Device				**Ch #**	**Function**
	TCA9548 0x75				Ch0	CPLD1~CPLD5 , 0x40, 0x39 ~ 0x3C
					Ch1	TCA9539, 0x76 Ch1.7: Unused Ch1.6: Unused Ch1.5: Unused Ch1.4: Unused Ch1.3: Unused Ch1.2: Unused Ch1.1: PSU0_PWROK Ch1.0: PSU1_PWROK Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: PSU0_LED_Y Ch0.3: PSU1_LED_Y Ch0.2: FAN_LED_Y Ch0.1: FAN_LED_EN Ch0.0: PSU0_LED_Y
					Ch2	TCA9555, 0x20 Ch1.7: Board_ID_3 Ch1.6: Board_ID_2

I2C Bus	Name	Address		Device	Bit #	Function
						Ch1.5: Board_ID_1 Ch1.4: Board_ID_0 Ch1.3: HW_REV_1 Ch1.2: HW_REV_0 Ch1.1: Build_REV_1 Ch1.0: Build_REV_0 Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: Unused Ch0.3: Unused Ch0.2: Unused Ch0.1: Unused Ch0.0: Unused
					Ch3	DC/DC ROV, 0x76
					Ch4	DC/DC AVS, 0x76
					Ch5	TCA9539, 0x76 Voltage High/Low margin test
					Ch6	TCA9548, 0x20 Beacon LED
					Ch7	Unused
	Device				**Ch #**	**Function**
	TCA9548 0x72				Ch0	TCA9548, 0x76 Ch0: QSFP28 Port 0 I2C Ch1: QSFP28 Port 1 I2C Ch2: QSFP28 Port 2 I2C Ch3: QSFP28 Port 3 I2C Ch4: QSFP28 Port 4 I2C Ch5: QSFP28 Port 5 I2C Ch6: QSFP28 Port 6 I2C Ch7: QSFP28 Port 7 I2C
					Ch1	TCA9548, 0x76 Ch0: QSFP28 Port 8 I2C Ch1: QSFP28 Port 9 I2C Ch2: QSFP28 Port 10 I2C Ch3: QSFP28 Port 11 I2C Ch4: QSFP28 Port 12 I2C Ch5: QSFP28 Port 13 I2C Ch6: QSFP28 Port 14 I2C Ch7: QSFP28 Port 15 I2C
					Ch2	TCA9548, 0x76 Ch0: QSFP28 Port 16 I2C Ch1: QSFP28 Port 17 I2C Ch2: QSFP28 Port 18 I2C Ch3: QSFP28 Port 19 I2C Ch4: QSFP28 Port 20 I2C Ch5: QSFP28 Port 21 I2C Ch6: QSFP28 Port 22 I2C Ch7: QSFP28 Port 23 I2C
					Ch3	TCA9548, 0x76 Ch0: QSFP28 Port 24 I2C Ch1: QSFP28 Port 25 I2C

I2C Bus	Name	Address		Device	Bit #	Function
						Ch2: QSFP28 Port 26 I2C Ch3: QSFP28 Port 27 I2C Ch4: QSFP28 Port 28 I2C Ch5: QSFP28 Port 29 I2C Ch6: QSFP28 Port 30 I2C Ch7: QSFP28 Port 31 I2C
					Ch4	TCA9548, 0x76 Ch0: QSFP28 Port 32 I2C Ch1: QSFP28 Port 33 I2C Ch2: QSFP28 Port 34 I2C Ch3: QSFP28 Port 35 I2C Ch4: QSFP28 Port 36 I2C Ch5: QSFP28 Port 37 I2C Ch6: QSFP28 Port 38 I2C Ch7: QSFP28 Port 39 I2C
					Ch5	TCA9548, 0x76 Ch0: Reserved for QSFP28 Port 40 I2C Ch1: Reserved for QSFP28 Port 41 I2C Ch2: Reserved for QSFP28 Port 42 I2C Ch3: Reserved for QSFP28 Port 43 I2C Ch4: Reserved for QSFP28 Port 44 I2C Ch5: Reserved for QSFP28 Port 45 I2C Ch6: Reserved for QSFP28 Port 46 I2C Ch7: Reserved for QSFP28 Port 47 I2C
					Ch6	TCA9548, 0x76 Ch0: QSFPDD Port 0 I2C Ch1: QSFPDD Port 1 I2C Ch2: QSFPDD Port 2 I2C Ch3: QSFPDD Port 3 I2C Ch4: QSFPDD Port 4 I2C Ch5: QSFPDD Port 5 I2C Ch6: QSFPDD Port 6 I2C Ch7: QSFPDD Port 7 I2C
					Ch7	TCA9548, 0x76 Ch0: QSFPDD Port 8 I2C Ch1: QSFPDD Port 9 I2C Ch2: QSFPDD Port 10 I2C Ch3: QSFPDD Port 11 I2C Ch4: QSFPDD Port 12 I2C Ch5: Reserved for QSFPDD 13 Ch6: Unused Ch7: Unused
	Device				**Ch #**	**Function**
	TCA9548 0x73				Ch0	Unused
					Ch1	Unused
					Ch2	CPLD1~CPLD5, 0x60~0x64 For CPLD firmware upgrade
					Ch3	Clock generators 82P33814ANLG, 0x53 8V19N474BFGI, 0x6C
					Ch4	Unused
					Ch5	PCIE Switch PEX8724, 0x38

I2C Bus	Name	Address		Device	Bit #	Function
					Ch6	Ethernet Controller I210, 0xC2
					Ch7	DC/DC P3V3, 0x76 DC/DC 0V8_CORE, 0x71

BMC_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
BMC_I2C	EEPROM	101-0101	0x55	M24128	--	Main Board EEPROM
	CPLD1	000-0100	0x40	CPLD	--	CPLD1
	I2C MUX	111-0000	0x70	TCA9548	--	FRU units, thermal sensors
	Device				**Ch #**	**Function**
	TCA9548 0x74				Ch0	PSU0, 0x50
					Ch1	PSU1, 0x50
					Ch2	PCA9535, 0x20 (at Fan board) Ch1.7: FAN4_DIR Ch1.6: FAN4_ABS Ch1.5: FAN4_LED_Y Ch1.4: FAN4_LED_G Ch1.3: FAN3_DIR Ch1.2: FAN3_ABS Ch1.1: FAN3_LED_Y Ch1.0: FAN3_LED_G Ch0.7: FAN2_DIR Ch0.6: FAN2_ABS Ch0.5: FAN2_LED_Y Ch0.4: FAN2_LED_G Ch0.3: FAN1_ABS Ch0.2: FAN1_ABS Ch0.1: FAN1_LED_Y Ch0.0: FAN1_LED_G
					Ch3	Voltage monitor UCD90120A, 0x34 HWM W83795, 0x2F (Reserved for dummy BMC board)
					Ch4	Thermal sensor LM75, 0x49 Thermal sensor LM75, 0x4D Thermal sensor LM75, 0x4E
					Ch5	Thermal sensor LM86, 0x4C
					Ch6	Thermal sensor LM86, 0x4C
					Ch7	Unused

CS4227_I2C Map:

I2C Bus	Name	Address	Device	Bit #	Function

I2C Bus	Name	Address		Device	Bit #	Function
CS4227_I2C	SFP+0	101-0000 101-0001	0x50 0x51	SFP+	--	SFP+ Port 0
	SFP+1	101-0000 101-0001	0x50 0x51	SFP+	--	SFP+ Port 1

Table 5-2 IO Expander in I²C Bus Description Table

5.4.2 System PCIe Interface

PCIe Gen 2, 3 interfaces are used to manage the slave devices by host CPU. PCIe slave component includes MAC BCM88690, BCM16K, and I210.

Both 1x PCIe Gen2, 4x PCIe Gen3, and 8x PCIe Gen3 interfaces on CPU card are switched by PEX8724.

PCIe interrupt from these components are wired together and connected to CPU card. CPU should scan PCIe devices one by one to check where the interrupt event comes from.

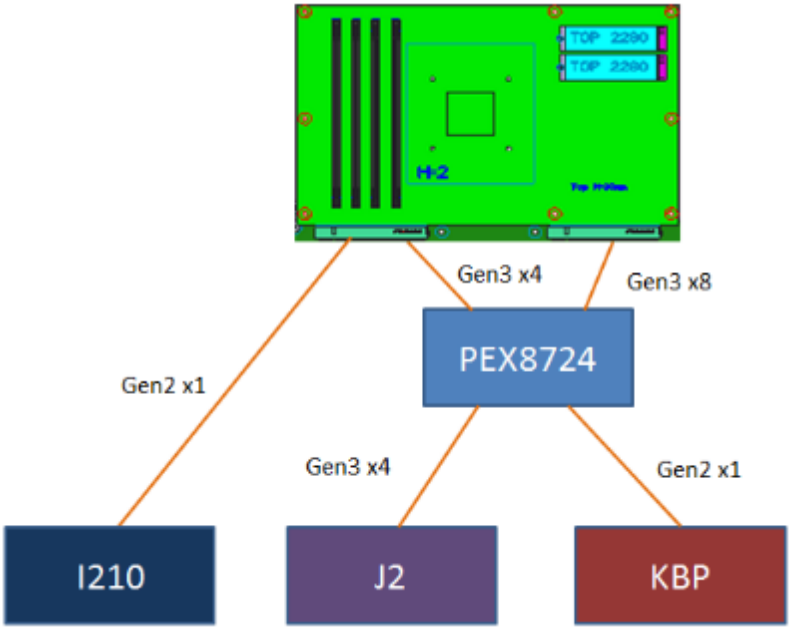


Figure 5-13 PCIe Connection Diagram

5.5 Other Daughter Boards

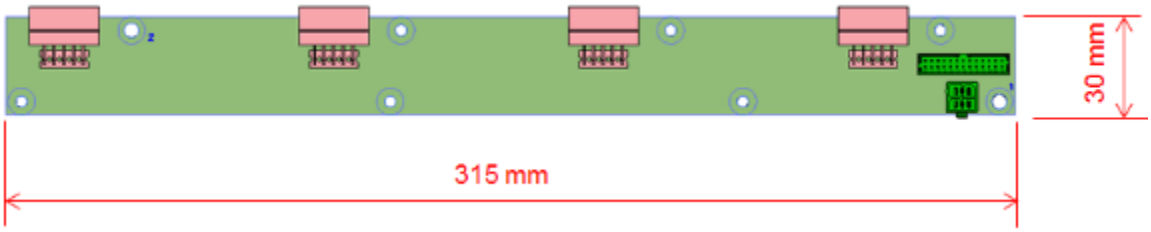
There are five daughter boards on the S9700-53DX system. It includes FAN board, PSU Board, OOB, Micro-USB, and Beacon LED board. The description detial show as below.

5.5.1 FAN Board

The Fan expander board is a passive board that bridges 12V power and control I/O to the Fan modules. The fan's I/O is controlled by BMC.

5.5.1.1 PCB Dimensions

S9700-53DX FAN board PCB Dimension.



5.5.1.2 PCB Layout

The PCB layout shows as below.

Figure 5-14 FAN Board PCB Layout

5.5.1.3 Connector Pin Definition

The following table is the pin definition of connectors on the FAN board.

Pin	1	3	5	7	9	11	13	15	17	19	21	23	25
Description	FAN0_F_DET	Reserve	FAN1_F_DET	Reserve	FAN2_F_DET	FAN_STATUS_INT_L	FAN_BOARD_SCL	FAN_BOARD_SDA	P12V	P12V	P12V	P12V	P12V
Pin	2	4	6	8	10	12	14	16	18	20	22	24	26
Description	Reserve	FAN3_F_DET	Reserve	FAN0_1_PWM	FAN2_3_PWM	P3V3	GND	GND	GND	GND	GND	GND	P12V

Table 5-3 2x13 connector Pin Definition (mates with MB)

Pin	1	2	3	4	5
Description	GND	P12V	FAN_PWM	P12V	FAN_LED_G
Pin	6	7	8	9	10
Description	FAN_LED_Y	FAN_F_DET	GND	FAN_DIR#	FAN_ABS#

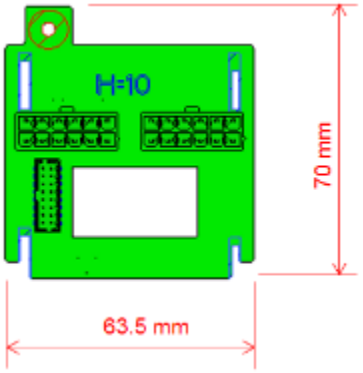
Table 5-4 2x5 connector Pin Definition (mates with FAN)

5.5.2 PSU Board

The PSU board is a passive board that bridges 12V power and control signals to the PSU.

5.5.2.1 PCB Dimensions

S9700-53DX PSU board PCB Dimension.



5.5.2.2 PCB Layout

The PCB layout shows as below.

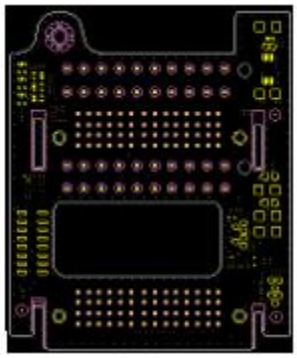


Figure 5-15 PSB Board PCB Layout

5.5.2.3 Connector Pin Definition

The following table is the pin definition of connectors on the PSB board.

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
A1	PSU_PRESENT	B1	PSU_PDB_FAULT	C1	GND	D1	P12V	P1_1	GND	P2_1	GND	P3_1	P12V	P4_1	P12V
A2	PSU_PDB_ALERT	B2	PSU_A0	C2	PSU_INT	D2	PSU_SHARE_PIN	P1_2	GND	P2_2	GND	P3_2	P12V	P4_2	P12V
A3	RESERVED	B3	AC_OK	C3	PSU_STATUS_SCL	D3	PSU_STATUS_SDA	P1_3	GND	P2_3	GND	P3_3	P12V	P4_3	P12V
A4	RESERVED	B4	RESERVED	C4	PSU_PWRON#	D4	GND	P1_4	GND	P2_4	GND	P3_4	P12V	P4_4	P12V
A5	RESERVED	B5	RESERVED	C5	PSU_A1	D5	PSU_PWROK								
A6	+5VSB	B6	+5VSB	C6	+5VSB	D6	+5VSB								

Table 5-5 Power Edge Connector Pin Definition (mates with PSU)

Pin	1	3	5	7	9	11	13	15
Description	PSU0_STATUS_SDA	PSU1_INT	PSU1_STATUS_SDA	PSU1_PRSNT	PSU1_PWROK	PSU1_PWRON	+5VSB	+5VSB
Pin	2	4	6	8	10	12	14	16
Description	PSU0_STATUS_SCL	PSU0_INT	PSU1_STATUS_SCL	PSU0_PRSNT	PSU0_PWROK	PSU0_PWRON	P3V3	GND

Table 5-6 2x8 signal connector Pin Definition (mates with MB)

Pin	1	3	5	7	9	11	13	15	17	19
Description	GND	GND	GND	GND	GND	P12V	P12V	P12V	P12V	P12V
Pin	2	4	6	8	10	12	14	16	18	20
Description	GND	GND	GND	GND	GND	P12V	P12V	P12V	P12V	P12V

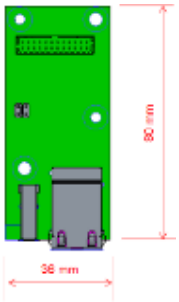
Table 5-7 Power connector Pin Definition (mates with MB)

5.5.3 OOB Board

The management board has a console port and a management port. It also connects power outputs to the main board and fan expander board.

5.5.3.1 PCB Dimensions

S9700-53DX OOB board PCB Dimension.



5.5.3.2 PCB Layout

The PCB layout shows as below.

Figure 5-16 OOB Board PCB Layout

5.5.3.3 Connector Pin Definition

The following table is the pin definition of connectors on the OOB board.

Pin Name	PIN NO.		Pin Name
P5V	1	2	GND
USB_UART_PN	3	4	USB_UART_DN

Table 5-8 2x2 Connector Pin Definition (mates with Micro-USB Board)

Pin Name	PIN	PIN	Pin Name
P5V_SB	1	2	P3V3
GND	3	4	OOB_SPD_1G
OOB_MDI_N0	5	6	OOB_LINK_ACT
OOB_MDI_P0	7	8	GND
OOB_MDI_N1	9	10	UART_TX
OOB_MDI_P1	11	12	UART_RX
OOB_MDI_N2	13	14	GND
OOB_MDI_P2	15	16	USB_N
OOB_MDI_N3	17	18	USB_P
OOB_MDI_P3	19	20	GND
NVCC_3V1	21	22	P5V
NC	23	24	NC

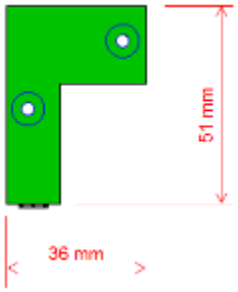
Table 5-9 2x12 signal connector Pin Definition (mates with MB)

5.5.4 Micro-USB Board

The USB board is a board that bridges 5V power and signals to the USB connector, it also provides the UART signals to USB console port for configuration.

5.5.4.1 PCB Dimensions

S9700-53DX Micro-USB board PCB Dimension.



5.5.4.2 PCB Layout

The PCB layout shows as below.

Figure 5-17 Micro-USB Board PCB Layout

5.5.4.3 Connector Pin Definition

The following table is the pin definition of connectors on Micro-USB board.

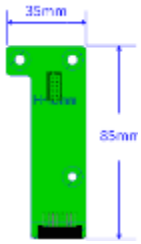
Pin	Signal
1	5V_USB
2	UART_M_RXD
3	UART_M_TXD
4	Reserve
5	GND

Table 5-10 Micro-USB Pin Definition

5.5.5 Beacon LED board

5.5.5.1 PCB Dimensions

S9700-53DX Beacon LED board PCB Dimension.



5.5.5.2 PCB Layout

The PCB layout shows as below.

Figure 5-18 Beacon LED Board PCB Layout

5.5.5.3 Connector Pin Definition

The following table is the pin definition of connectors on Beacon LED board.

Pin Name	PIN	PIN	Pin Name
P3V3	1	2	P3V3
P3V3	3	4	Beacon_LED_SCL
NC	5	6	Beacon_LED_SDA
NC	7	8	GND
GND	9	10	GND

Table 5-11 Micro-USB Pin Definition

5.6 Front Panel Design

The S9700-53DX front panel IO ports includes the functionalities below:

- System status LED
  - ✓ Power status LED
  - ✓ FAN status LED
  - ✓ Beacon LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port

✓ 1x console port in RJ45
✓ 1x console port in Micro-USB

● Ethernet data ports
✓ 40x 100GE QSFP28 ports
✓ 13x 400GE QSFPDD ports

Detailed IO arrangement is shown as below :

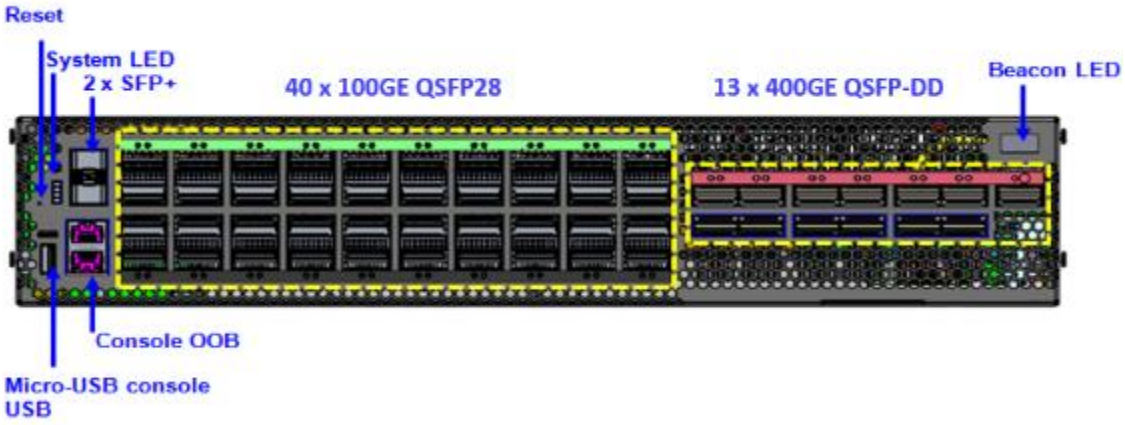


Figure 5-19 Front Panel IO Arrangement

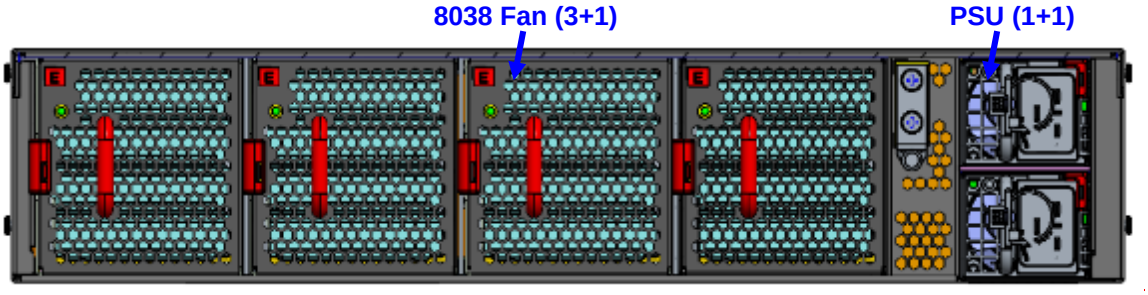


Figure 5-20 Rear Panel IO Arrangement

5.6.1 System LED Indicators

The system status and stacking LED are placed on main board and controlled by I/O expender U66 address 0x75.

Items	LED Indication	Behavior	Description
1	SYS	OFF	No power
		Solid Green	Host CPU/BMC is up
		Solid Amber	Power is up but Host CPU/BMC is not up
2	FAN	OFF	Fans are not initialized
		Solid Green	All Fans are work normal
		Solid Amber	Fan fail : one or more Fans need service
3	PS1	OFF	No power

		Solid Green	PSU1 is work normal
		Solid Amber	PSU1 fail (PSU1 need service)
4	PS2	OFF	No power
		Solid Green	PSU2 is work normal
		Solid Amber	PSU2 fail (PSU2 need service)

Table 5-12 System LED Descriptions

5.6.2 Management Port LED Indicators

The platform will have 2 green LEDs integrated in the front panel management RJ45 port.

Left LED:
- Off: no link
- Green-solid: Link-up

Right LED:
- Off: no activity
- Amber-blinking: TX/RX activity

5.6.3 SFP+ port LED Indicators

Each front panel SFP+ port will have one bi-color (Green/Amber) LED, and LED status is controlled by CPLD.

The following table shows the 1GE/10GE LED definitions:

Location	LED Indication	Color	Behavior	Description
E0 & E1 SFP+ ports	Link/Act/Speed of 10GE	Green	Solid	Link up
			Blinking	Packet transmitting or receiving
			Off	No link or port disable
	Link/Act/Speed of 1GE	Amber	Solid	Link up
			Blinking	Packet transmitting or receiving
			Off	No link or port disable

Table 5-13 SFP+ port LED Descriptions

5.6.4 QSFP28/QSFPDD Port LED Indicators

The BCM88690 provides five serial LED output interfaces and allows the user to select any of the bit steam outputs to control LED status of Ethernet ports. On the S9700-53DX, bit stream 0 is designed for QSFP28 port 1 to QSFP28 port 40. QSFPDD port 1 to port 13 are controlled by CPLD register directly.

For QSFP28 is controlled by serial LED interface of MAC, the bit stream0 sequencing from start bit to end bit is shown as below. For QSFPDD is controlled by CPLD register directly.

Bit stream0 for QSFP28

Front Panel Port Number	Bit Number	Function	Bit Value	Color	Bit Value	Color
P39	0	25G Link/ACT	1	Yellow	0	Off
	1	100G Link/ACT	1	Green	0	Off
P38	2	25G Link/ACT	1	Yellow	0	Off

	3	100G Link/ACT	1	Green	0	Off
P37	4	25G Link/ACT	1	Yellow	0	Off
	5	100G Link/ACT	1	Green	0	Off
P36	6	25G Link/ACT	1	Yellow	0	Off
	7	100G Link/ACT	1	Green	0	Off
P35	8	25G Link/ACT	1	Yellow	0	Off
	9	100G Link/ACT	1	Green	0	Off
P34	10	25G Link/ACT	1	Yellow	0	Off
	11	100G Link/ACT	1	Green	0	Off
P33	12	25G Link/ACT	1	Yellow	0	Off
	13	100G Link/ACT	1	Green	0	Off
P32	14	25G Link/ACT	1	Yellow	0	Off
	15	100G Link/ACT	1	Green	0	Off
P31	16	25G Link/ACT	1	Yellow	0	Off
	17	100G Link/ACT	1	Green	0	Off
P30	18	25G Link/ACT	1	Yellow	0	Off
	19	100G Link/ACT	1	Green	0	Off
P29	20	25G Link/ACT	1	Yellow	0	Off
	21	100G Link/ACT	1	Green	0	Off
P28	22	25G Link/ACT	1	Yellow	0	Off
	23	100G Link/ACT	1	Green	0	Off
P27	24	25G Link/ACT	1	Yellow	0	Off
	25	100G Link/ACT	1	Green	0	Off
P26	26	25G Link/ACT	1	Yellow	0	Off
	27	100G Link/ACT	1	Green	0	Off
P25	28	25G Link/ACT	1	Yellow	0	Off
	29	100G Link/ACT	1	Green	0	Off
P24	30	25G Link/ACT	1	Yellow	0	Off
	31	100G Link/ACT	1	Green	0	Off
P23	32	25G Link/ACT	1	Yellow	0	Off
	33	100G Link/ACT	1	Green	0	Off
P22	34	25G Link/ACT	1	Yellow	0	Off
	35	100G Link/ACT	1	Green	0	Off
P21	36	25G Link/ACT	1	Yellow	0	Off
	37	100G Link/ACT	1	Green	0	Off
P20	38	25G Link/ACT	1	Yellow	0	Off
	39	100G Link/ACT	1	Green	0	Off
P19	40	25G Link/ACT	1	Yellow	0	Off
	41	100G Link/ACT	1	Green	0	Off
P18	42	25G Link/ACT	1	Yellow	0	Off
	43	100G Link/ACT	1	Green	0	Off
P17	44	25G Link/ACT	1	Yellow	0	Off
	45	100G Link/ACT	1	Green	0	Off
P16	46	25G Link/ACT	1	Yellow	0	Off
	47	100G Link/ACT	1	Green	0	Off
P15	48	25G Link/ACT	1	Yellow	0	Off
	49	100G Link/ACT	1	Green	0	Off
P14	50	25G Link/ACT	1	Yellow	0	Off
	51	100G Link/ACT	1	Green	0	Off
P13	52	25G Link/ACT	1	Yellow	0	Off
	53	100G Link/ACT	1	Green	0	Off
P12	54	25G Link/ACT	1	Yellow	0	Off
	55	100G Link/ACT	1	Green	0	Off
P11	56	25G Link/ACT	1	Yellow	0	Off
	57	100G Link/ACT	1	Green	0	Off
P10	58	25G Link/ACT	1	Yellow	0	Off
	59	100G Link/ACT	1	Green	0	Off
P9	60	25G Link/ACT	1	Yellow	0	Off
	61	100G Link/ACT	1	Green	0	Off
P8	62	25G Link/ACT	1	Yellow	0	Off
	63	100G Link/ACT	1	Green	0	Off
P7	64	25G Link/ACT	1	Yellow	0	Off
	65	100G Link/ACT	1	Green	0	Off

P6	66	25G Link/ACT	1	Yellow	0	Off
	67	100G Link/ACT	1	Green	0	Off
P5	68	25G Link/ACT	1	Yellow	0	Off
	69	100G Link/ACT	1	Green	0	Off
P4	70	25G Link/ACT	1	Yellow	0	Off
	71	100G Link/ACT	1	Green	0	Off
P3	72	25G Link/ACT	1	Yellow	0	Off
	73	100G Link/ACT	1	Green	0	Off
P2	74	25G Link/ACT	1	Yellow	0	Off
	75	100G Link/ACT	1	Green	0	Off
P1	76	25G Link/ACT	1	Yellow	0	Off
	77	100G Link/ACT	1	Green	0	Off
P0	78	25G Link/ACT	1	Yellow	0	Off
	79	100G Link/ACT	1	Green	0	Off

Table 5-14 S9700-53DX QSFP28 Port LED Bit-Stream Table

5.6.5 OOB Port

The S9700-53DX includes 1 standard GE RJ45 port for out of band (OOB) management, share by CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

5.6.6 Console Port

Two console ports available for S9700-53DX systems access, both of them can be used for CPU or BMC access. The pin definition of the RS232 console port is shown as below. Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor. The default baud rate is 115200 bps.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

Table 5-15 Pin Definition of RJ45 Console Connector

5.6.7 USB2.0 Port

The S9700-53DX integrates a USB 2.0 host controller that supports a single port operating at high speed (HS) at 480 Mbps (USB 2.0).

USB 5V power will be enabled during system initialization, software should de-assert ‘PWR_EN’ by pulling this pin low once over current event (USB device consumes >0.5A current more than 20mS) is received. ‘PWR_EN’ need set as ‘HIGH’ to re-enable USB port.

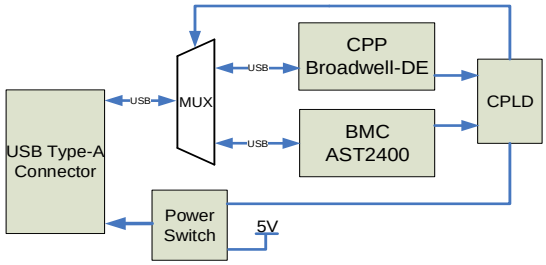


Figure 5-21 USB Interface Diagram

6 FAN Control and Thermal Policy

The FAN tray with 80x80x38mm FAN is adopted on the S9700-53DX system to meet chassis depth requirement.

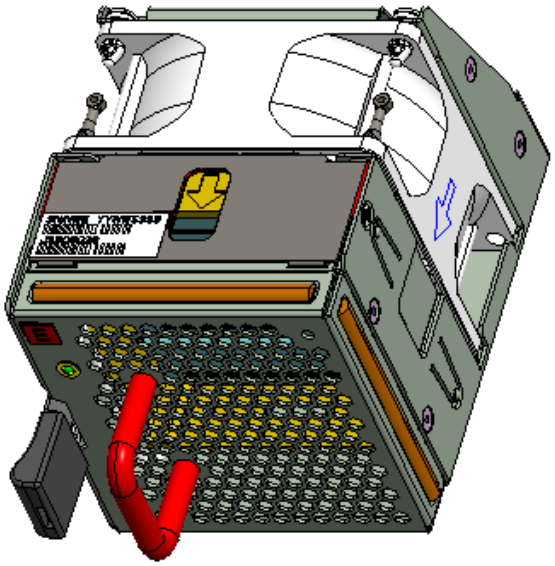


Figure 6-1 8038 FAN Module

6.1 Electrical Specifications

Rated voltage	12VDC
Rated current	3.5A MAX
Rated power consumption	48W MAX
Operating voltage range	10.8VDC ~ 13.2VDC
Operating temperature	-20 ~ +70
Rated speed	16100 +/- 1610 min-1
Acoustic noise	73dB MAX

7 Power Supply

The S9700-53DX adopts two kinds of 2000W hot swappable power supplies. The PSU modules supported: One is 220Vac input to +12.2Vdc output AC/DC PSU, the other is -48Vdc input to +12.2Vdc output DC/DC PSU.

7.1 Physical Size

The physical size of the power supply enclosure is intended to accommodate the power range of up to 2000W. The physical size is 40mm x 50.5mm x 360mm (height x width x length).

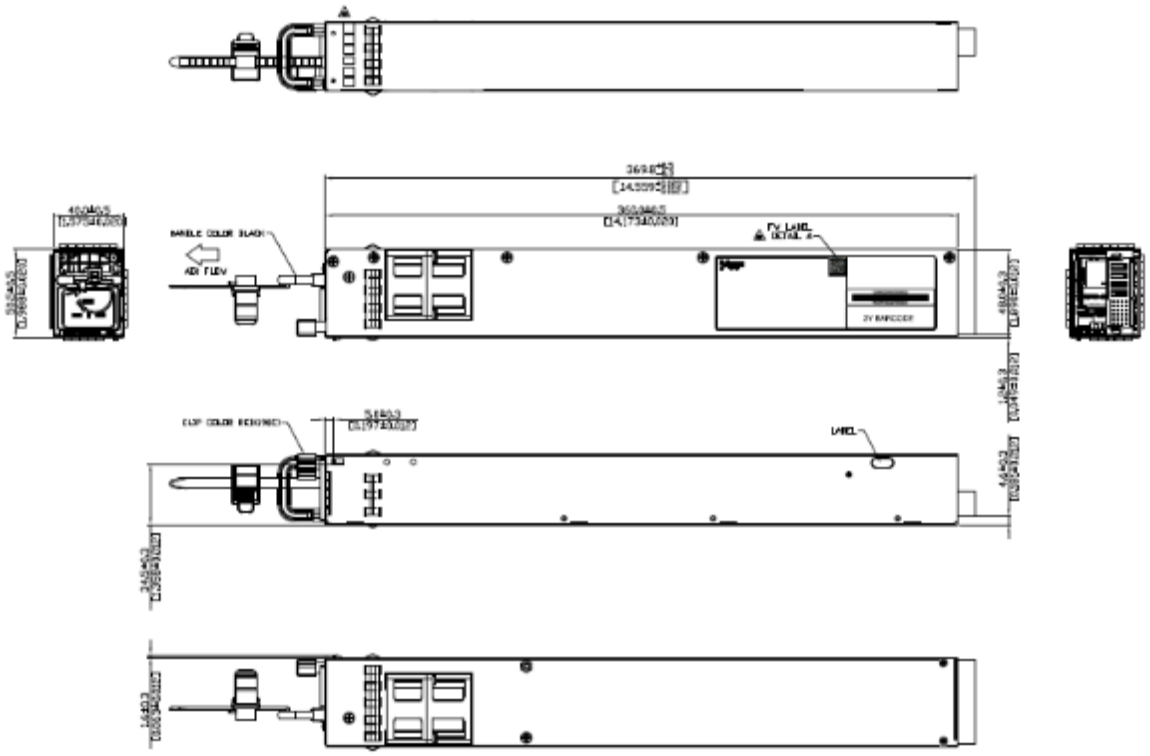


Figure 7-1 2000W AC/DC Power Supply Dimension

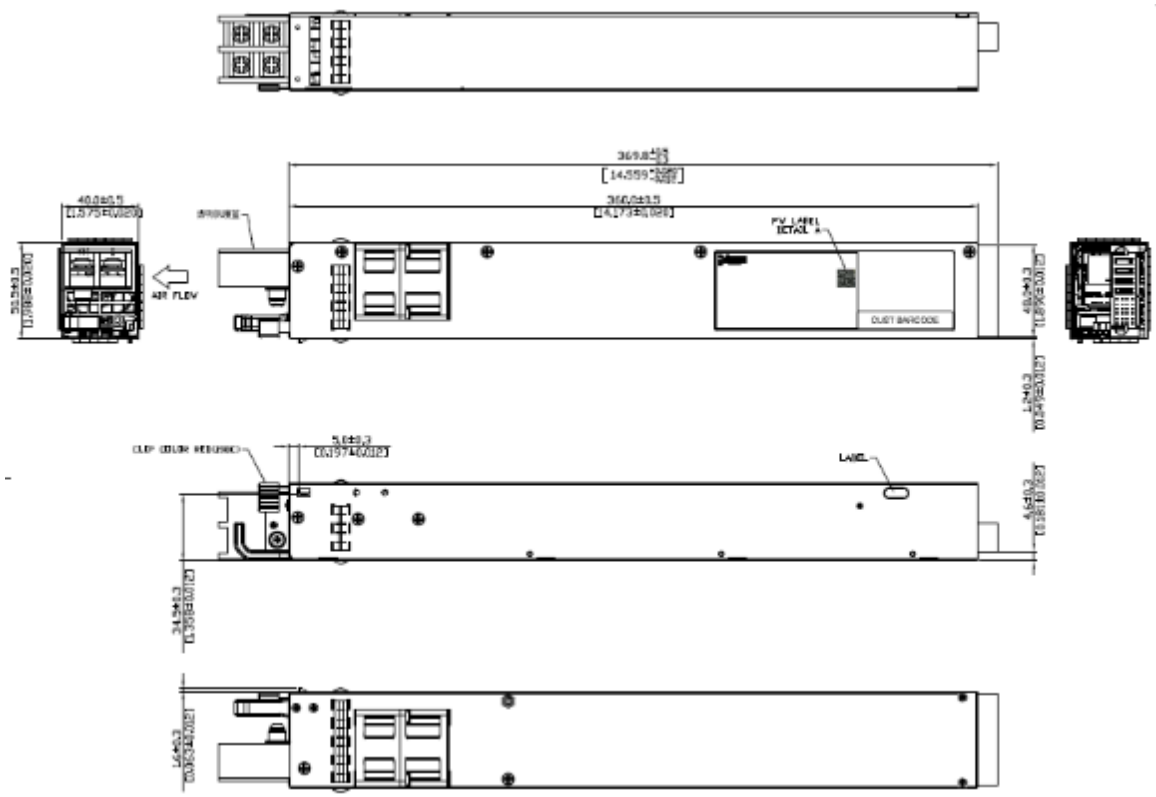


Figure 7-2 2000W DC/DC Power Supply Dimension

7.2 Electrical Specifications

Protection circuits inside the PSU shall cause only the main output to shutdown (latch off). If the PSU latches off due to a protection circuit assert, an Input power cycle off for 15sec or a PSON pin cycle high for 1sec shall be able to reset the PSU.

The detailed electrical specifications of AC/DC PSU are shown below:

INPUT SPECIFICATIONS	
Input Voltage Range	90~264VAC
Input Frequency	47-63 Hz
Input Current	13A max.
Inrush Current	100A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12.2V
Output Current (Amps)	90~264VAC:82A(+12.2V), 180~264VAC:164A(+12.2V)
Max Power (Watt)	2000W
Output Voltage (Volts)	+5VSB
Output Current (Amps)	5A (+5VSB)
Efficiency	80Plus Platinum >90% @20% load, >94 @50% load, >91% @100% load
Ripple P-P (mV) (max.)	+12.2V:200, +5VSB:50

Total Regulation	+12.2V:±5%, +5VSB:±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	4msec
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Latch off
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes
Load Sharing	Yes
Hi-pot	1800VAC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–5°C to 50°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	0 to 90% RH
EMI	Meets FCC/CISPR 22 Class A(under 6dB) Specification

Table 7-1 AC/DC Power Supply Specification

The detailed electrical specifications of DC/DC PSU are shown below:

INPUT SPECIFICATIONS	
Input Voltage Range	-40 ~ -72VDC
Input Current	60A max.
Inrush Current	100A
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12.2V
Output Current (Amps)	164A(+12.2V)
Max Power (Watt)	2000W@-40~-72VDC
STB Output Voltage (Volts)	+5VSB
STB Output Current (Amps)	5A (+5VSB)
Efficiency	>88% @20% load, >92 @50% load, >91% @100% load
Ripple P-P (mV) (max.)	+12.2V:120, +5VSB:50
Total Regulation	+12.2V:±5%, +5VSB:±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	1msec
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Latch off
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes
Load Sharing	Yes
Hi-pot	1500VDC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–5°C to 50°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	0 to 90% RH
EMI	Meets FCC/CISPR 22 Class A(under 6dB) Specification

Table 7-2 DC/DC Power Supply Specification

Power supply condition	Power supply LED
Output ON and OK.	Green
No AC power to all power supplies.	Off
PSU standby state AC present / Only +5VSB on.	1Hz Flashing Green
AC cord unplugged or AC power lost with a second power supply in parallel still with AC input power.	1Hz Flashing Red
Power supply critical event causing a shutdown, failure, over current, short circuit, over voltage, fan failure, over temperature.	Red
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	Flashing 1sec Red and 1sec Green

Table 7-3 LED Status Information

Module	Module Pin Out	Dir.	BMC Pinout	Functionality Description
PSU #0	PSU0_PWROK	→	GPIOK7	PSU0 power OK signal generated by PSU
	PSU0_PRESENT_L	→	GPIOK6	PSU0 Slot. (0 : Present, 1 : Empty)
	PSU0_PSON_N	←	GPIOP2	PSU0 main power enable control by BMC
	PSU0_I2C	←	I2C2	PSU0 EEPROM access via I2C bus
	PSU0_INT_N	→	GPIOP3	PSU0 interrupt signal generated by PSU
PSU #1	PSU1_PWROK	→	GPIOP5	PSU1 power OK signal generated by PSU
	PSU1_PRESENT_L	→	GPIOP4	PSU1 Slot. (0 : Present, 1 : Empty)
	PSU1_PSON_N	←	GPIOE2	PSU1 main power enable control by BMC
	PSU1_I2C	←	I2C2	PSU1 EEPROM access via I2C bus
	PSU1_INT_N	→	GPIOP7	PSU1 interrupt signal generated by PSU

Table 7-4 PSU Management Pin Definition

7.3 System Power Consumption

Power consumption of the S9700-53DX:

Table 7-5 Power consumption of switch main board

Item	Sheet	Function / Subset	Qty	Power Consumption (W)
1	NCP1-1 MB	Switch Main Board	1	1458
2	BMC	BMC module	1	14
3	CPU	CPU module	1	83
4	FAN	FAN module	4	192
PSU 12V total current(A)				145.6
Total Power consumption (W)				1746.6
AC/DC De-rating, 10%				1
Mini PSU Power Budget (W)				1746.63

Table 7-6 Power consumption of S9700-53DX system

8 Software Support

The S9700-53DX supports a base software package composed of the following components:

BIOS

The S9700-53DX Supports AMI AptioV BIOS version xx or greater with the x86 CPU module

BMC

The S9700-53DX Supports AMI MegaRAC SP-X BMC firmware for Aspeed AST2400 platform.

ONIE

See http://onie.org/ for the latest supported version

9 Compliance

Environmental	
Operating temperature	0 ~ 45°C (at sea level with Fan Failure condition)
Storage temperature	-40~70°C (–40°F to 158°F)
Altitude	0~10,000ft at 45°C
Operating relative humidity	0%-85% RH (non-condensing)
Storage relative humidity	0%-85% RH (non-condensing)
Acoustic	76dB at 27°C
Dimensions (height x width x depth)	436.0 mm (W) x 762.0 mm (D) x 87.7 mm (H)
Weight	26.66kg

Regulatory Compliances	
Category	ATT-TP-76200 ESR-003 (Carrier Grade Level 3)
Safety	NEBS Level 3 UL 62368-1 IEC/EN 60950-1 IEC/EN 62368-1 BSMI CNS 14336-1 UL 60960
EMC	NEBS Level 3 FCC Part 15, Subpart B, Class A; EN55032, Class A EN 300 386 EN 55024 EN 301 489-1 EN 301 489-19 EN 303413 BSMI (CNS 13438), Class A