OPEN Compute Project

Time Card Base Address via PCIe

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1.0

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1.2 Acknowledgements

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2. Change Log

Date	Version #	Author	Description
07AUG23	1.0	Thomas Schaub	Initial Version
05SEP23	2.0	ADVA/Oscilloquartz	Added AXI Address and MSI Mapping for Ethernet Support

3. AXI Address Mapping

AXI Slave interface	Slave	Offset Address	High Address
S_AXI_CTL	AXI PCIe Control	0x0001_0000	0x0001_0FFF
axi4l_slave	Version	0x0002_0000	0x0002_0FFF
S_AXI	AXI GPIO Ext	0x0010_0000	0x0010_0FFF
S_AXI	AXI GPIO GPS/MAC	0x0011_0000	0x0011_0FFF
S_AXI	AXI GPIO SEL	0x0013_0000	0x0013_0FFF
S_AXI	AXI GPIO SMA MAP1	0x0014_0000	0x0014_0FFF
S_AXI	AXI GPIO SMA STATUS	0x0014_2000	0x0014_2FFF
S_AXI	AXI I2C	0x0015_0000	0x0015_FFFF
S_AXI	AXI UART 16550 GPS	0x0016_0000	0x0016_FFFF
S_AXI	AXI UART 16550 GPS2	0x0017_0000	0x0017_FFFF
S_AXI	AXI UART 16550 MAC	0x0018_0000	0x0018_FFFF
S_AXI	AXI UART 16550 NMEA	0x0019_0000	0x0019_FFFF
S_AXI	AXI GPIO SMA MAP2	0x0022_0000	0x0022_0FFF
S_AXI_LITE	AXI HWICAP	0x0030_0000	0x0030_FFFF
AXI_LITE	AXI Quad SPI Flash	0x0031_0000	0x0031_FFFF
AXI_LITE	AXI DMA	0x0080_0000	0x0080_FFFF
AXI_LITE	AXI Eth Port 1	0x0084_0000	0x0087_FFFF
AXI_LITE	AXI Eth Port 2	0x0088_0000	0x008B_FFFF
axi4l_slave	Adj. Clock	0x0100_0000	0x0100_FFFF
axi4l_slave	Signal TS0 (GNSS)	0x0101_0000	0x0101_FFFF
axi4l_slave	Signal TS1	0x0102_0000	0x0102_FFFF
axi4l_slave	PPS Master	0x0103_0000	0x0103_FFFF
axi4l_slave	PPS Slave	0x0104_0000	0x0104_FFFF
axi4l_slave	TOD Slave	0x0105_0000	0x0105_FFFF
axi4l_slave	Signal TS2	0x0106_0000	0x0106_FFFF
axi4l_slave	IRIG Slave	0x0107_0000	0x0107_FFFF
axi4l_slave	IRIG Master	0x0108_0000	0x0108_FFFF
axi4l_slave	DCF Slave	0x0109_0000	0x0109_FFFF

axi4l_slave	DCF Master	0x010A_0000	0x010A_FFFF
axi4l_slave	TOD Master	0x010B_0000	0x010B_FFFF
axi4l_slave	Signal TS PPS	0x010C_0000	0x010C_FFFF
axi4l_slave	Signal Generator1	0x010D_0000	0x010D_FFFF
axi4l_slave	Signal Generator2	0x010E_0000	0x010E_FFFF
axi4l_slave	Signal Generator3	0x010F_0000	0x010F_FFFF
axi4l_slave	Signal Generator4	0x0110_0000	0x0110_FFFF
axi4l_slave	Signal TS3	0x0111_0000	0x0111_FFFF
axi4l_slave	Signal TS4	0x0112_0000	0x0112_FFFF
axi4l_slave	Frequency Counter 1	0x0120_0000	0x0120_FFFF
axi4l_slave	Frequency Counter 2	0x0121_0000	0x0121_FFFF
axi4l_slave	Frequency Counter 3	0x0122_0000	0x0122_FFFF
axi4l_slave	Frequency Counter 4	0x0123_0000	0x0123_FFFF

The AXI interconnect can have multi masters which all have access to the slaves. One is the AXI PCIe interface and another one for the static configuration which does only a basic configuration after reset.

4. Message-Signaled Interrupt Mapping

The interrupts in the design are connected in a the MSI(-X) Vector to the PCI Express Core. The Interrupts have following mapping:

MSI Number	Interrupt Source
0	NTL Signal TS PPS
1	NTL Signal TS0
2	NTL Signal TS1
3	AXI UART 16550 GPS
4	AXI UART 16550 GPS2
5	AXI UART 16550 MAC
6	NTL Signal TS2
7	AXI I2C
8	AXI HWICAP
9	AXI Quad SPI Flash
10	AXI UART 16550 NMEA
11	NTL Signal Generator1
12	NTL Signal Generator2
13	NTL Signal Generator3
14	NTL Signal Generator4
15	NTL Signal TS3
16	NTL Signal TS4
17	AXI DMA CH1
18	AXI DMA CH1
19	AXI DMA CH2
20	AXI DMA CH2
21	AXI ETH 1
22	AXI ETH 2
23	AXI ETH 1 MDIO
24	AXI ETH 2 MDIO