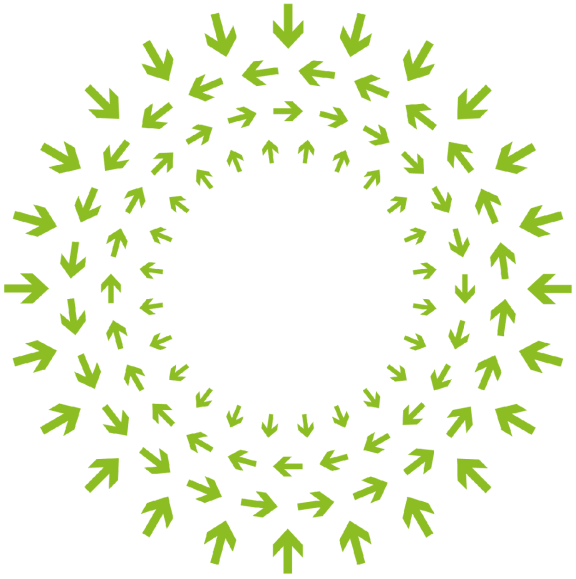

OPEN
Compute Project

Server Project: OCE Link Layer

Universal D2D Transaction and Link Layer Specification, with Profiles and Variants Specifications

for BoW and UCIe Interfaces

1.3.0
05 June 2025

Modular (Base, Design and Product) Specification
Effective June 05, 2025

Author: David Kruckemyer, Jeff Maguire

Version History

Note, refer to the OCP Contribution Versions, Revisions and Errata best practices documentation. Generally speaking, Versions and revisions are made to this document and logged here. Errata is a separate document such that the contribution specification document it refers to was not revised. Ex: Version 1, Errata E1

Date	Version #	Author	Description
18 APR 23	A.1.0	David Kruckmeyer	Initial Release
tbd	1.2.0	Brian Murray	Sideband addition release
05 JUN 25	1.3.0	David Kruckmeyer Jeff Maguire	Incremental UCIe interfacing with reference to Variants and Profiles

Current Template Version:

3 Layer (Base, Design and Product) Specification Template V1.6.0

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1. Acknowledgements

The Contributors of this Specification would like to acknowledge the following for their feedback:

Brian Murray, VeriSilicon, who made a significant contribution to help review/refine the OCP/ODSA framework, formalize the ODSA D2D Transaction and Link Layer specification and make several AMBA Protocol Variant contributions.

2. Compliance with OCP Tenets

Please describe how this Specification complies with the OCP tenets.

A full explanation of the OCP core tenets can be seen here.

1.1. Openness

These specifications are an open multi-layered community driven chiplet interfacing framework capable of mapping any protocol to any parallel PHY transport. There are no associated licensing costs or vendor lock-in scenarios.

1.2. Efficiency

The framework enables market-leading ultra low-latency, low-overhead and robust transport of internal chiplet native IP interfacing protocols. This removes the need for expensive protocol bridges, NoC integrations, and UCIe CRC/Retry mechanism.

1.3. Impact

Extending the ODSA TLL specification to support UCIe capitalizes on the recent market traction and addresses gaps in the UCIe specification to AMBA-based protocols. The semiconductor industry will greatly benefit from protocol interoperability being defined within an open chiplet ecosystem to support a wide range of applications.

1.4. Scale

The low-overhead framework provides the flexibility to transport a wide range and mix of native IP protocols over chiplet interfaces, which can scale from cost-effective to very high-performance chiplet integrations.

1.5. Sustainability

The framework enables the disaggregation of monolithic SoCs into highly reusable chiplet element functions, which improves degrees of freedom for system composability, while minimizing the overhead to utilize the underlying native interfacing IP protocols over chiplet connections. This enables the development of domain specific acceleration design IP, which can be quickly productized as chiplets at a lower cost, to accelerate the realization of dramatic improvements to performance per watt.

3. Scope

The contribution has been broken into the OCP Base, Design and Product layer specifications. While these chiplet specifications might not precisely fit the OCP layered specification model, there seemed to be a reasonable and helpful association. The entire scope of this work is being developed within the OCP/OCE Link Layer workstream which is tracked within the following Wiki page:

OCE Link Layer Wiki

3.1. Base Specification Layer

In-Scope:
Transaction and Link Layer packetization
Link Layer Packet (LLP) to UCIe mainband interfacing
Protocol Variant mappings to the Transaction Layer Packet (TLP)
Chiplet Profiles comprising a collection of Protocol Variant mappings

Out-of-Scope:
UCIe specification features including Adapter Layer, Sideband, and Management

3.2. Design Specification Layer

All possible Protocol Variant to TLP mappings are in-scope.

3.3. Product Specification Layer

All possible Profiles mixes of Protocol Variants are in-scope.

4. Overview

This specification describes the extension of the OCP/ODSA Transaction and Link Layer (TLL) specification to UCIe. This ushers in the new OCP/OCE “Universal” D2D TLL specification which combines supporting bindings to several physical layer standards, with a low-latency low-overhead packetization of a wide range of protocols between chiplets. The overall D2D layered architecture maps a set of design IP protocols (Protocol Variants) on a chiplet interface (Profiles) through the Universal TLL Transaction Layer Packet (TLP) and Link Layer Packet (LLP) formats to a particular physical layer interface.

Table 1 summarizes the proposed Universal OCP/OCE D2D layered architecture which overlays the UCIe architecture over the prior OCP/ODSA layered architecture. While the UCIe specification makes references to the PCIe/CXL protocol specifications, these protocols are viewed out-of-scope for this die disaggregation approach which primarily focuses on low-latency AMBA-based protocols. This Profile and Protocol Variant protocol mappings of the OCP/OCE Universal D2D layered architecture addresses the gap in the UCIe specification to an open, flexible and low-latency protocol mapping to the UCIe FDI Streaming interface.

<table>
<tr><th>OCE Universal D2D</th><th>ODSA D2D (BoW)</th><th>UCIe</th></tr>
<tr><td>System Interface</td><td>Profiles/Variants</td><td>N/A (PCIe/CXL out-of-scope)</td></tr>
<tr><td rowspan="2">Packetization Layer</td><td>Transaction Layer</td><td rowspan="2">Protocol Layer Operation Formats</td></tr>
<tr><td>Upper Link Layer</td></tr>
<tr><td>Bitstream Interface</td><td>LLP</td><td>FDI Streaming</td></tr>
<tr><td>Adapter Layer</td><td>Lower Link Layer</td><td>D2D Adapter Layer</td></tr>
<tr><td>Physical Interface</td><td>BoW Interface</td><td>RDI</td></tr>
<tr><td>Physical Layer</td><td>Physical Layer</td><td>Physical Layer</td></tr>
</table>

Table 1- *Universal D2D Layered Architecture*

5. Base Specifications

5.1. Description

The Transaction and Link Layer (TLL) specification provides the base specification for a low-overhead packetization of protocols used within a chiplet to a Die-to-Die (D2D) physical transport layer (PHY).

5.2. Goals and Vision

The aim is to minimize the overall latency across chiplets while leveraging existing design IP protocols used within chiplets. This latency focus narrows the scope of the physical layers to a class of low-latency parallel PHYs. The original physical layer was based on the Bunch of Wires (BoW) which was defined within the OCP/ODSA workstream. This is now being extended to UCIe which ushers in the concept of a Universal D2D TLL which can support a linkage to any PHY technology.

5.3. Solution Architecture

The base specification is composed of the Transaction and Link Layers (TLL) under the system interface boundary shown in Figure 1. The Protocol layer in the figure is addressed by the Protocol Variants (design specification) and Profiles (product specifications) which are covered in following chapters. Figure 2 provides an overview of the OCP/ODSA TLL TLP and LLP packet formats, which remain unchanged in the proposed Universal OCP/OCE TLL specification.

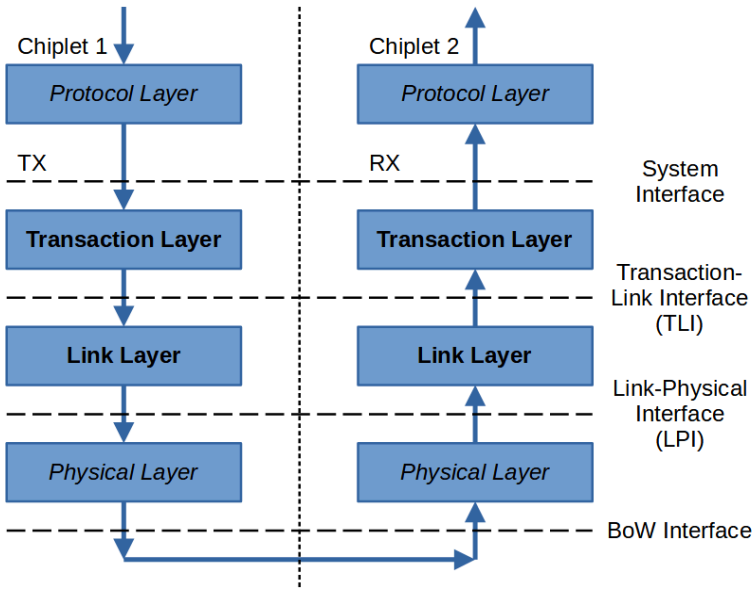

Figure 1- *ODSA D2D Layered Architecture*

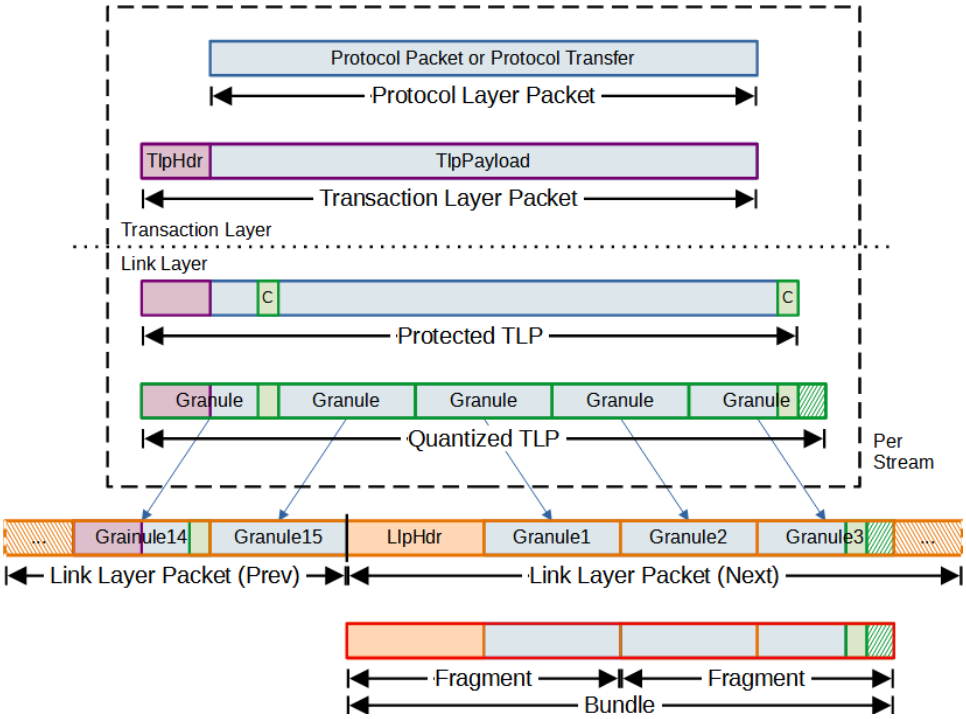

Figure *2 - Packet Formats*

5.4. Functional Requirements

Flit-Aware D2D Interface

The D2D interface communicates with the UCIe D2D Adapter via the Flit-Aware D2D Interface, or FDI. The protocol layer uses the Streaming protocol interface with the Raw format, which bypasses the CRC/Retry mechanisms in the UCIe Adapter Layer. By convention, a single 64B LLP corresponds to a flit on the FDI, and the protocol layer always communicates in full flits.

This specification assumes the UCIe Adapter has brought the chiplet interface into an Active state and is maintained in that Active state during operation.

Transmit

LLP Ordering

LLPs are presented to the UCIe FDI in ascending granule order, i.e. HDR (or G00) is presented before G01, and G01 is presented before G12, etc. This order corresponds to the transfer order of the LLP.

For UCIe, an LLP represents a protocol layer *flit*.

Assignment

Once an LLP is packed, the granules in the LLP are assigned in data width chunks (NBYTES) of the UCIe flit-aware D2D interface (FDI), i.e. a chunk equals one cycle of data on the FDI interface.

The protocol layer supports the following parameter values for NBYTES: 8, 16, 32, and 64; and the TX interface and the RX interface may support different values of NBYTES to accommodate different process technologies and implementation methodologies. The assignment of granules to data width chunks is such that the LlpHdr (i.e. HDR) is always bits [31:0] of a data width chunk.

Implementation Note: To support a variety of data rates and possible implementations of a Hub SoC, the protocol layer *must* support all of these chunk sizes. The chunk size is boot-time configurable.

The transmit order for an LLP is described below.

LLP Transfer Order

The following diagrams illustrate the LLP transmit and receive order for different values of NBYTES equal to the UCIe FDI data width. Each row represents the transmit or receive data signal name for each sequential cycle T.

When NBYTES=8, an LLP is transmitted or received as follows:

T	NBYTES=8 [63:0]	
0	G01	HDR
1	G03	G02
2	G05	G04
3	G07	G06
4	G09	G08
5	G11	G10
6	G13	G12
7	G15	G14

8B Data Width

For a 16B data width, an LLP is transmitted or received as follows:

T	NBYTES=16 [127:0]			
0	G03	G02	G01	HDR
1	G07	G06	G05	G04
2	G11	G10	G09	G08
3	G15	G14	G13	G12

16B Data Width

For a 32B data width, an LLP is transmitted or received as follows:

T	NBYTES=32 [255:0]							
0	G07	G06	G05	G04	G03	G02	G01	HDR
1	G15	G14	G13	G12	G11	G10	G09	G08

32B Data Width

For a 64B data width, an LLP is transmitted or received as follows:

T	NBYTES=64 [511:0]															
0	G15	G14	G13	G12	G11	G10	G09	G08	G07	G06	G05	G04	G03	G02	G01	HDR

64B Data Width

Receive

Alignment

Unlike BoW, data on the UCIe FDI does *not* require alignment, and the receive order for LLPs is described above.

For each LLP, the RX interface link layer first decodes the LlpHdr to determine where the granules containing a TlpHdr are located in the LLP, based on the TlpStart bits. Any errors in the LlpHdr *must* be corrected in order to determine the proper location of the TlpHdr granules.

Error Correction

Within the TLP processing pipeline, the large codewords are gathered and are corrected, as necessary. Once all the granules are gathered, a compressed TLP is expanded into a standard TLP as required, and a TLP is presented to the transaction layer.

The UCIe Adapter could potentially enable a CRC/Retry mechanism for FDI Streaming Flit format other than the Raw format. If enabled, the CRC/Retry mechanism would scrub errors before they would be corrected by the TLP processing pipeline.

5.5. Repository Location

The OCP/OCE Transaction and Link Layer specification can be found in the following repository:

Transaction and Link Layer Repository

5.6. References

Ventana Contribution References:

[1] “ODSA Transaction and Link Layer Specification”, 2023, OCP specification, Revision A, Version 1.0: https://www.opencompute.org/documents/transaction-and-link-layer-specification-for-bunch-of-wires-bow-interfaces-pdf-pdf

[2] “UCIe Specifications”, 2025, https://www.uciexpress.org/specifications

6. Design Specifications

6.1. Description

While the TLL is defined as the base specification layer, it also serves as a design specification for the base D2D Controller TLP to LLP framework that would be integrated into a chiplet. That said, the TLP packet format does not correspond to design IP protocol interfaces found within chiplet integration. Therefore, the TLL is not considered a complete design specification.

In order to bridge to design IP protocols, Protocol Variant specifications have been created to map protocols to the TLP packet format. AMBA-based protocols were the natural starting point as they are industry standard protocols over which a monolithic SoC integration of IP blocks could be disaggregated into a chiplets. While AMBA protocols are the natural starting point, there is nothing in the framework that would prevent protocols other than AMBA to be addressed.

Each protocol can be broken down into Protocol Variants which can comprise different sets of protocol features and parameterization. Interoperable subsets of these Variants should naturally align with the underlying IP blocks integrated within chiplets.

6.2. Goals and Vision

Ventana intends to help foster a large and broad OCE community to help define/refine Protocol Variants in an effort to create more interoperability within the OCP Chiplet Marketplace.

6.3. Repository Location

Protocol Variant specifications can be found in the following repository:

Variant Repository

6.4. References

Ventana Contribution References:

[1] “ODSA CHI-E RN-256 Bus Protocol Variant”, 2023, OCP specification, revision A, version 0.8.1: https://github.com/opencomputeproject/ODSA-Link-Layer/blob/main/Profiles%20and%20Variants/ODSA%20CHI-E%20RN-256%20Bus%20Protocol%20Variant%20Rev%20A%20-%20v0.8.1.pdf

[2] “ODSA AXI5-Lite D-64 Interface Profile”, 2023, OCP specification, revision A, version 0.7.0::
https://github.com/opencomputeproject/ODSA-Link-Layer/blob/main/Profiles%20and%20Variants/ODSA%20AXI5-Lite%20D-64%20Interface%20Profile.pdf

7. Product Specifications

7.1. Description

The TLL specification supports the ability to concurrently run multiple Protocol Variants over a common chiplet interface. Profile specifications serve as the product specification layer that captures the set of Protocol Variants that define the chiplet mainband interface.

7.2. Goals and Vision

Ventana intends to help foster a large and broad OCE community to help define Profile Classes in an effort to create more interoperability within the OCP Chiplet Marketplace. Some possible examples of Profile Classes could be compute, memory, IO, or NoC-NoC chiplet interfaces that could be fully coherent, IO-coherent or non-coherent in nature.

7.3. Repository Location

Profile specifications can be found in the following repository:

Profile Repository

7.4. References

Ventana Contribution References:

[1] “Veyron V1 Interface Profile”, 2023, OCP specification, revision A, version 0.9.1: https://github.com/opencomputeproject/ODSA-Link-Layer/blob/main/Profiles%20and%20Variants/Ventana%20Veyron%20V1%20Interface%20Profile%20Rev%20A%20-%20v0.9.1.pdf

Appendix A - Checklist for Steering Committee (SC) approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes	If no, please state the reason.
Was it approved in the OCP Contribution Portal?	Yes	If no, please state the reason.
Is there a Supplier(s) that is building a product based on this Spec?	Yes	List Supplier Name(s) Ventana offers a CPX D2D Controller design IP product. Other suppliers will arise who follow this open specification
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	Ventana has a D2D Controller design IP product for interfacing to Veyron compute chiplets