

Revision History

Rev	Group	Date	Description
X100	G00/G02/G03	Nov, 2018	Initial Release
R100	G00/G02/G03	Dec, 2018	Beta0 Release
R101	G00/G02/G03	Dec27, 2018	Beta1 Release
R200	G00/G02/G03	Jan 27, 2019	Beta2 Release

Variants

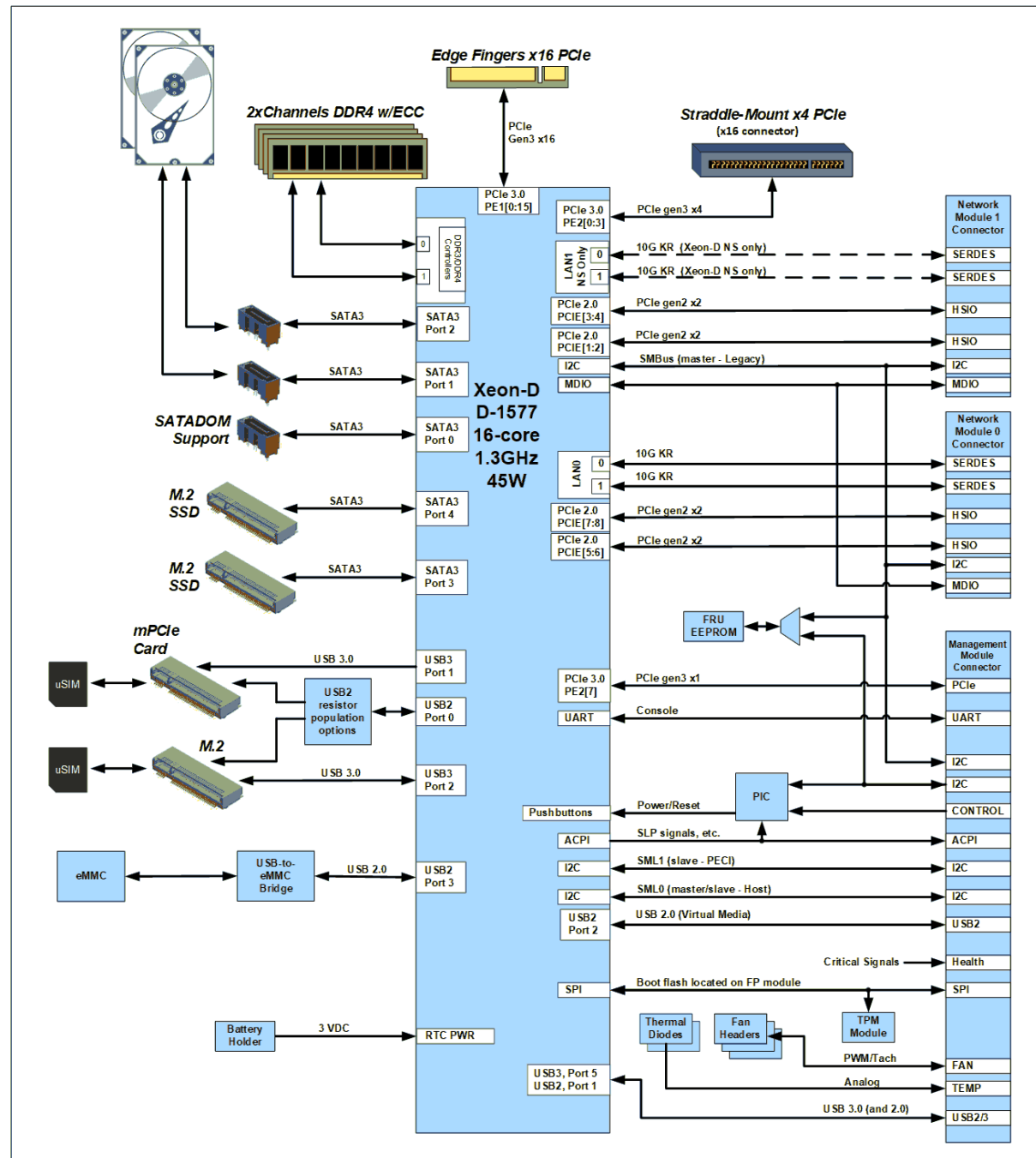
Feature	G00	G02	G03
PCB	-0189	-0190	-0190
SoC SKU	D-1577	D-1541	D-1517
Cores	16	8	4
DIMM Slots	4	2	2
EMMC	Yes	No	No
PCIe x16 Side Ex.Slot	V.T.H	Straddle	Straddle
PCIe x8 Side Ex.Slot	V.T.H	Straddle	Straddle

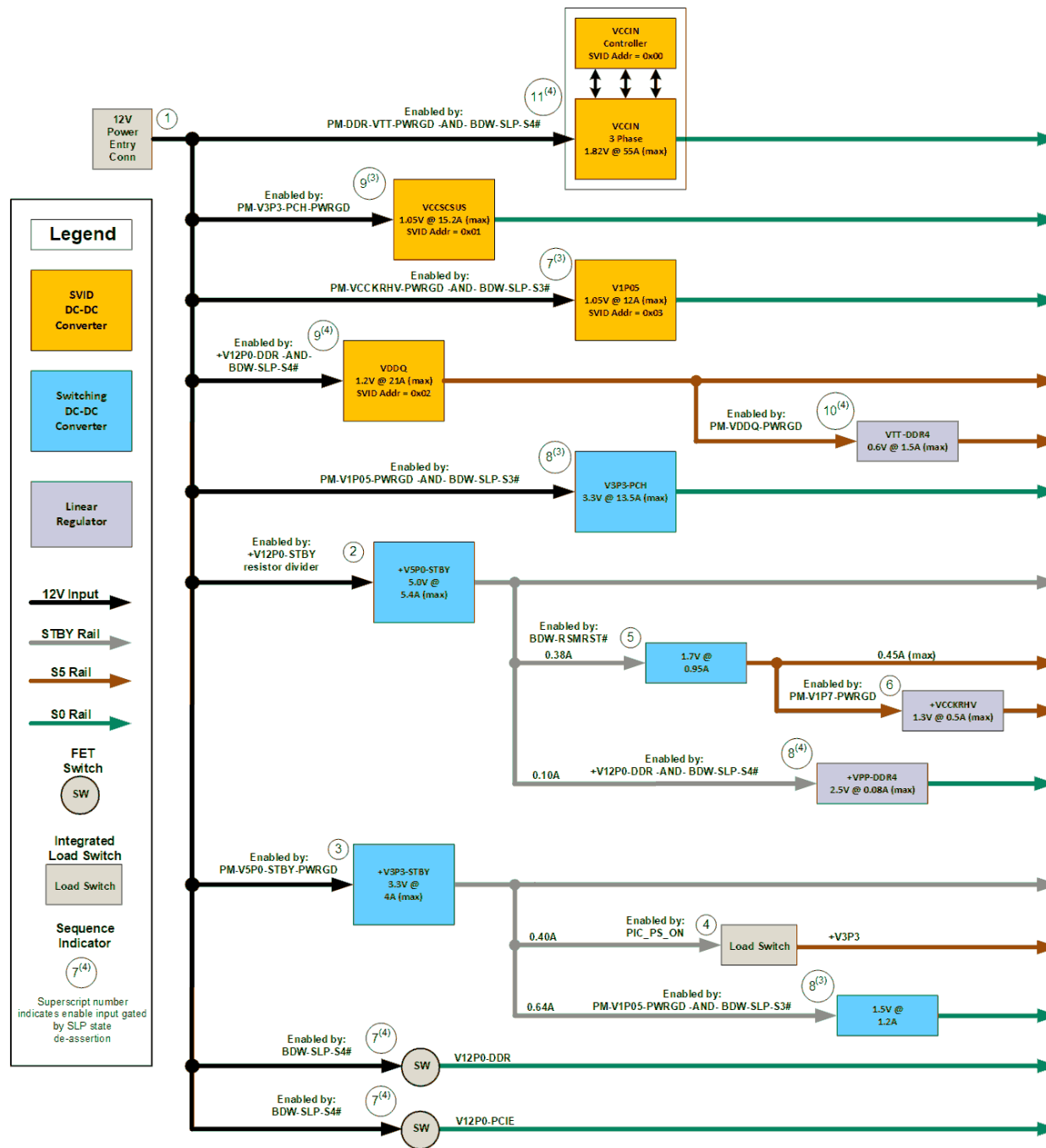
Notes

- * Schematic prepared for two PCB boards in three variants:
PCB1 80204-0189-G00 for Compute Large
PCB2 80204-0190-G02 for Compute Medium
PCB2 80204-0190-G03 for Compute Small
- * Schematic supports V2 and Y0 CPU (none -NS) steppings only
In order support -NS chip, need change layout as following:
- Remove SHRT1
- connect U1 pins T40, T42 & V40 to +VCCSCSUS
- * PCB boards difference
-0189 Side Expansion Slots True Holes mount
-0190 Side Expansion Slots Straddle mount
- * To see variant:
1. Open View menu
2. Choose Variant View Mode menu
3. Choose one of the variants
4. Press OK

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50	Power Entry / Downstream Regulators





DRAWING No. : 80304

SIZE : Custom REV No. : R200

DATE : Sunday, April 07, 2019
Monday, June 11, 2018

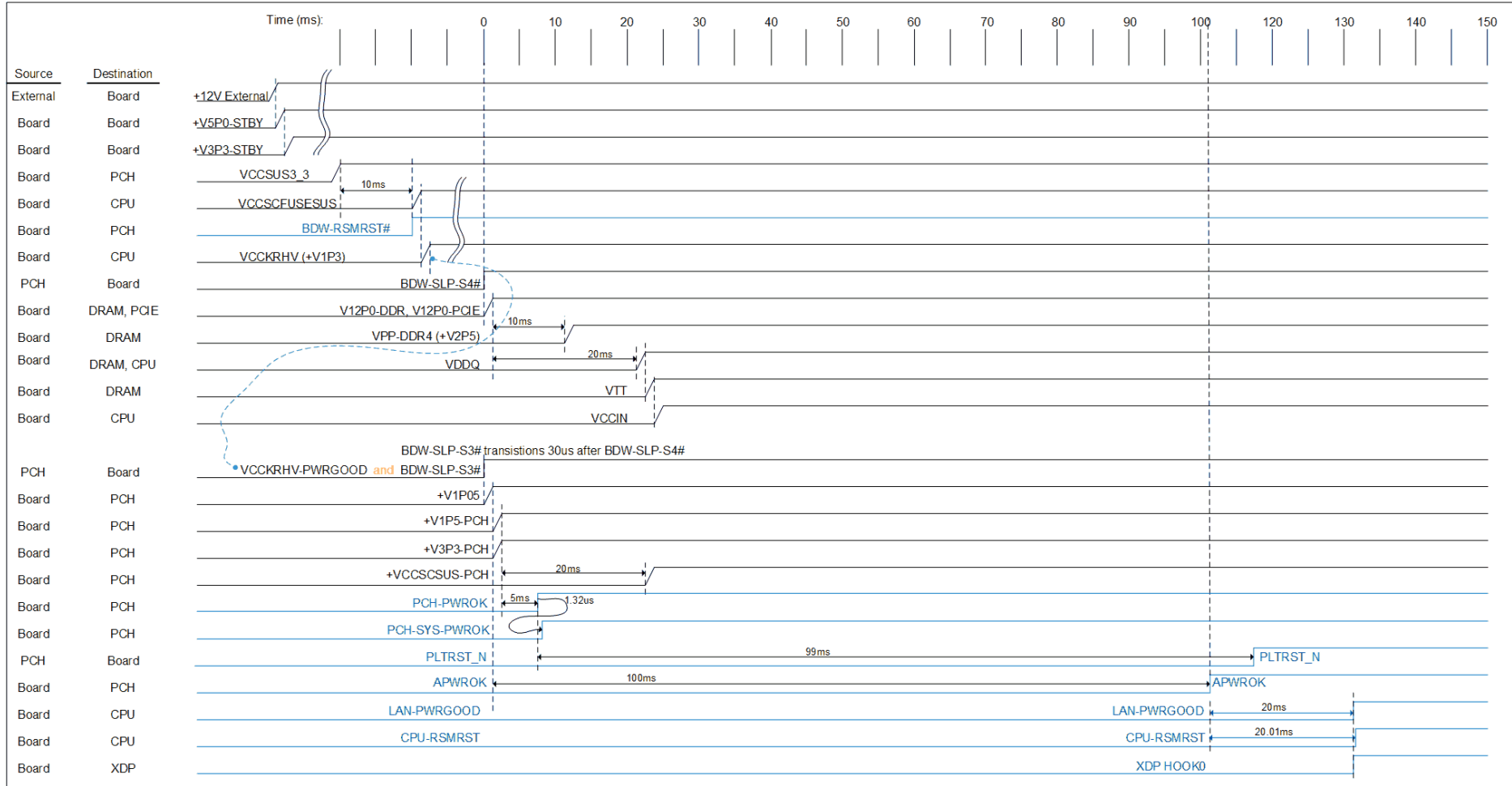
Power Tree Diagram

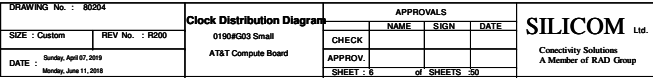
0190M003 Small
AT&T Compute Board

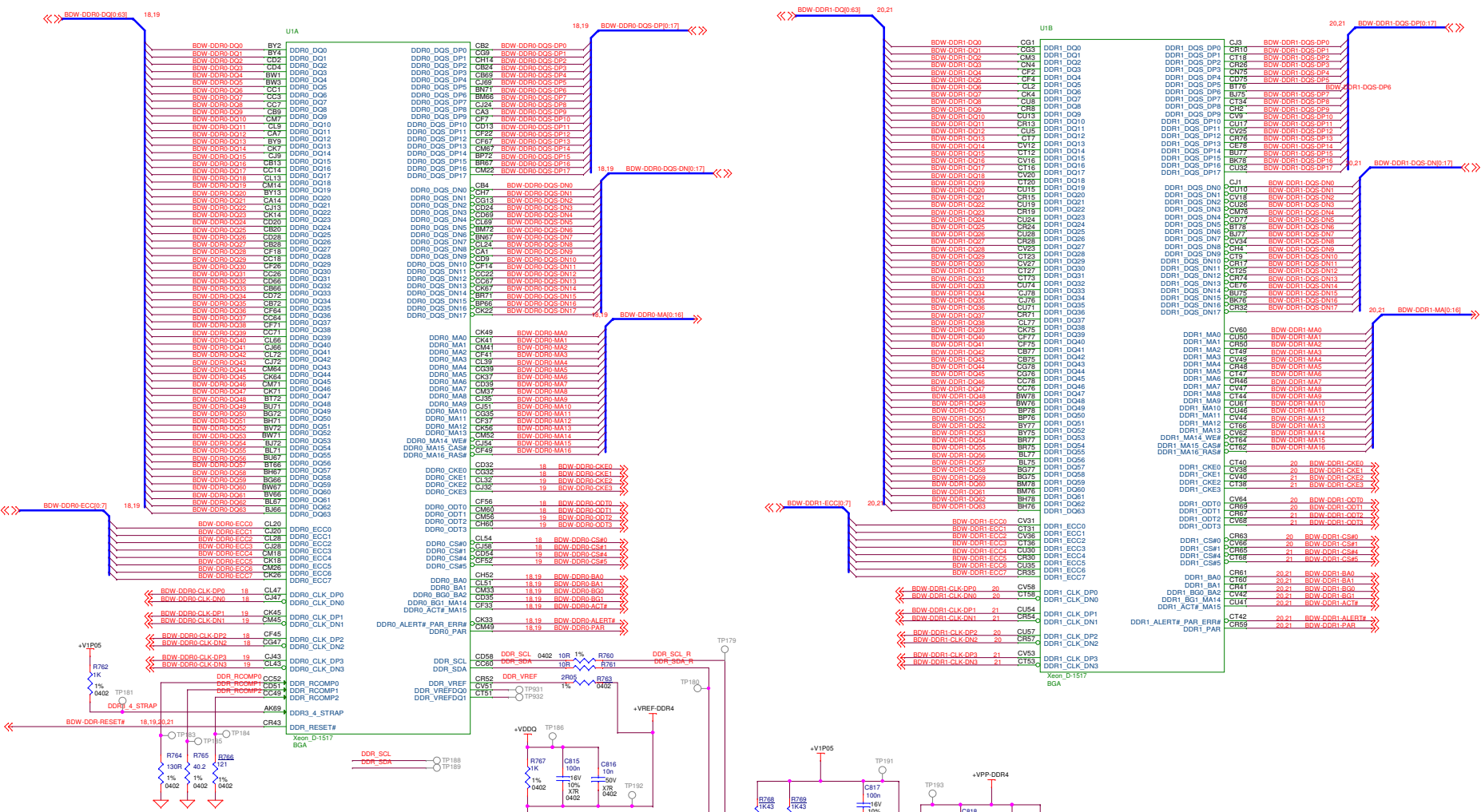
APPROVALS

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SHEET : 4	of SHEETS : 30		

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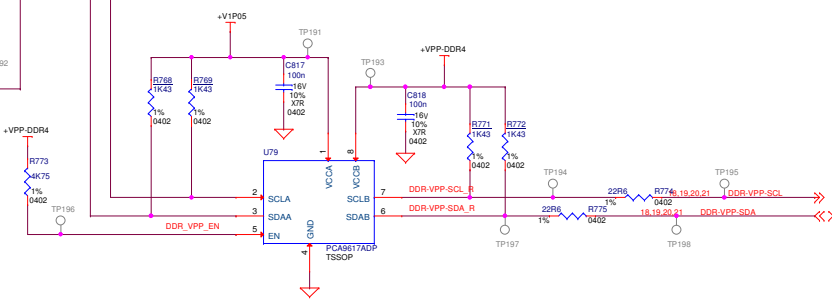


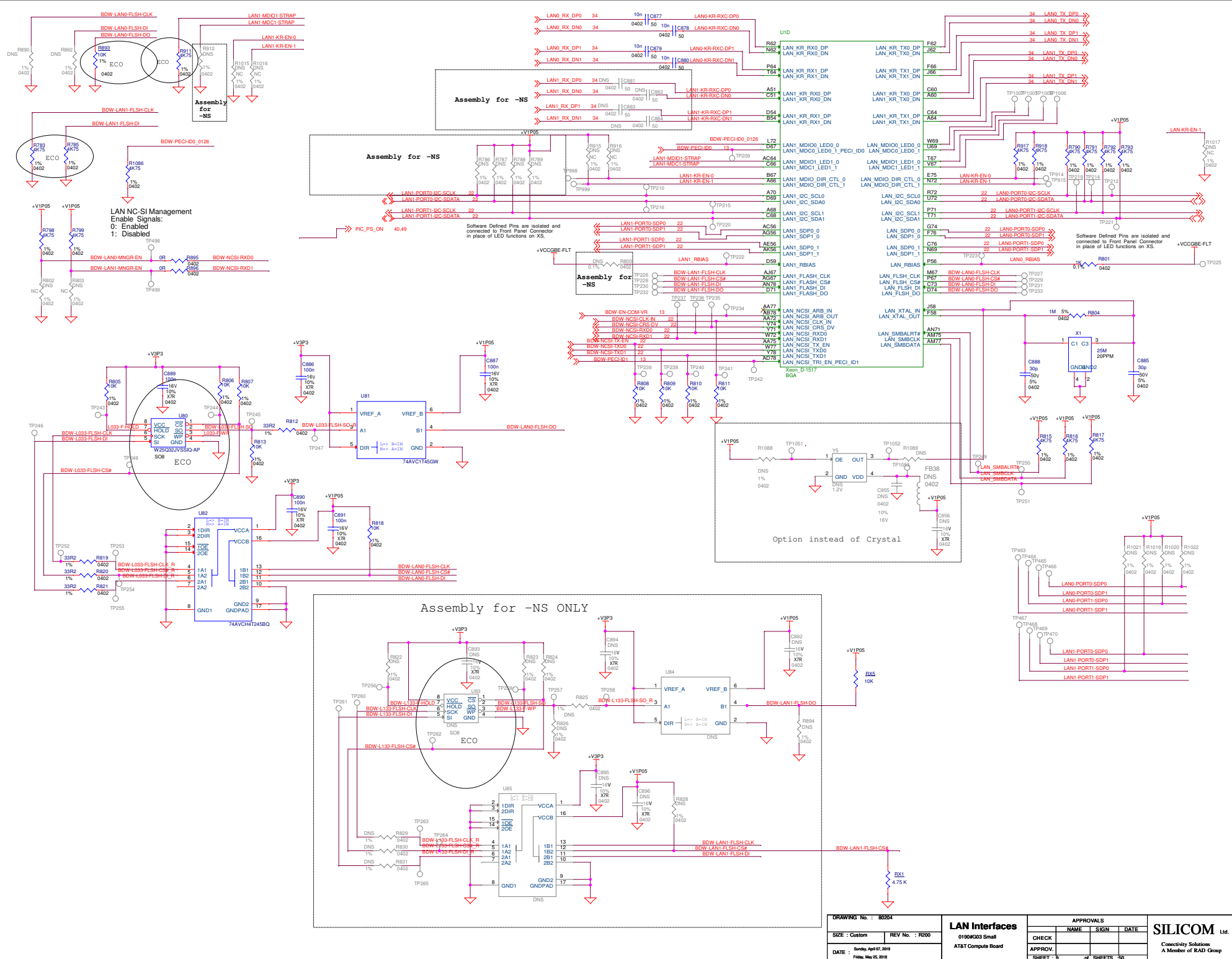


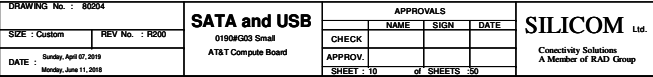
Routing Notes:

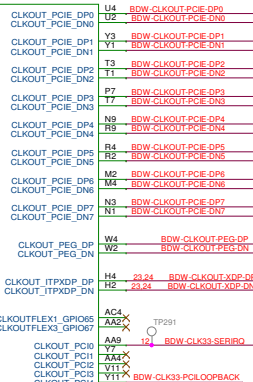
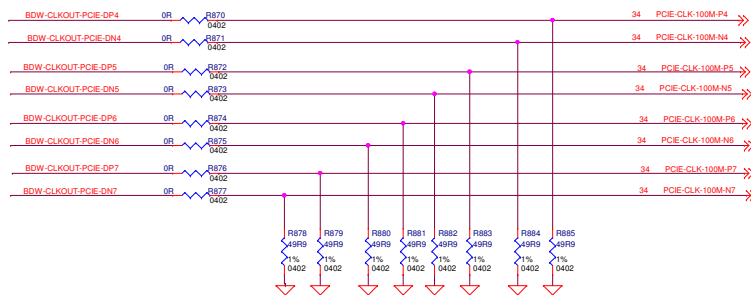
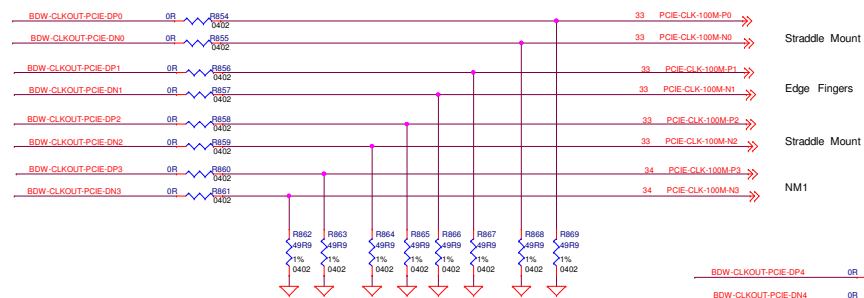
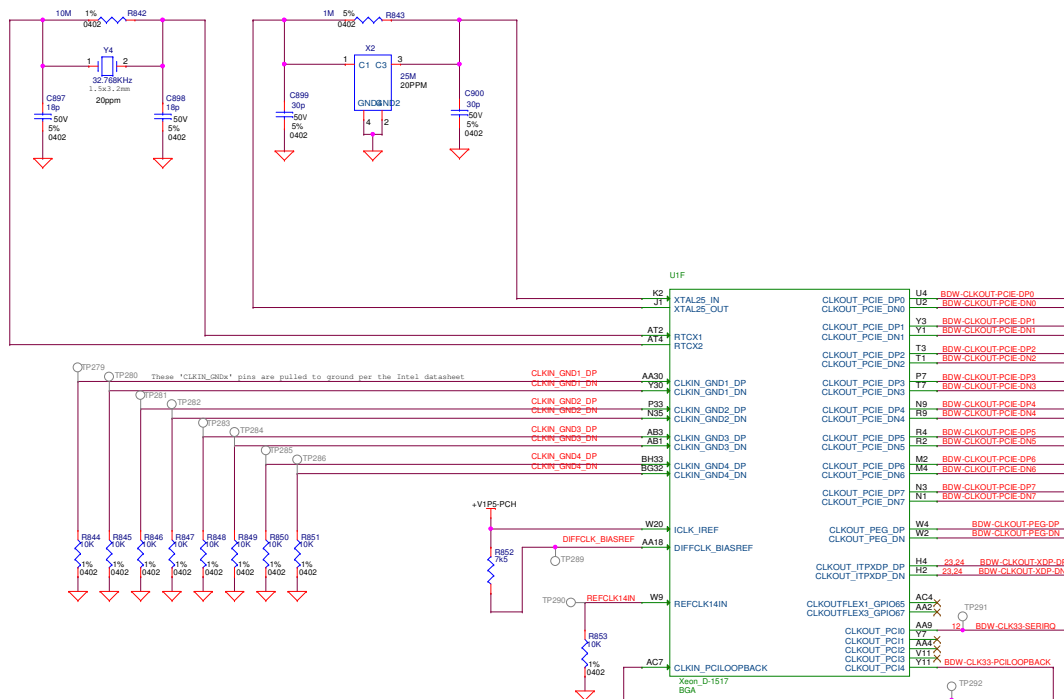
For each DDR channel DIMM is to be placed farther from the SOC, and DIMM0 is to be placed nearer to the SOC.
In that case, the signals are to be routed as:

DIMM0 (farther)	DIMM1 (nearer)
DDR _x _CLK_0_2	DDR _x _CLK_1_3
DDR _x _CKE_1_0	DDR _x _CKE_3_2
DDR _x _ODT_1_0	DDR _x _ODT_3_2
DDR _x _CS_1_0	DDR _x _CS_5_4









Straddle Mount
Edge Fingers
Straddle Mount
NM1
Management Module
NM1
NM0
NM0

Management Module
NM1
NM0
NM0

DRAWING No. : 80504

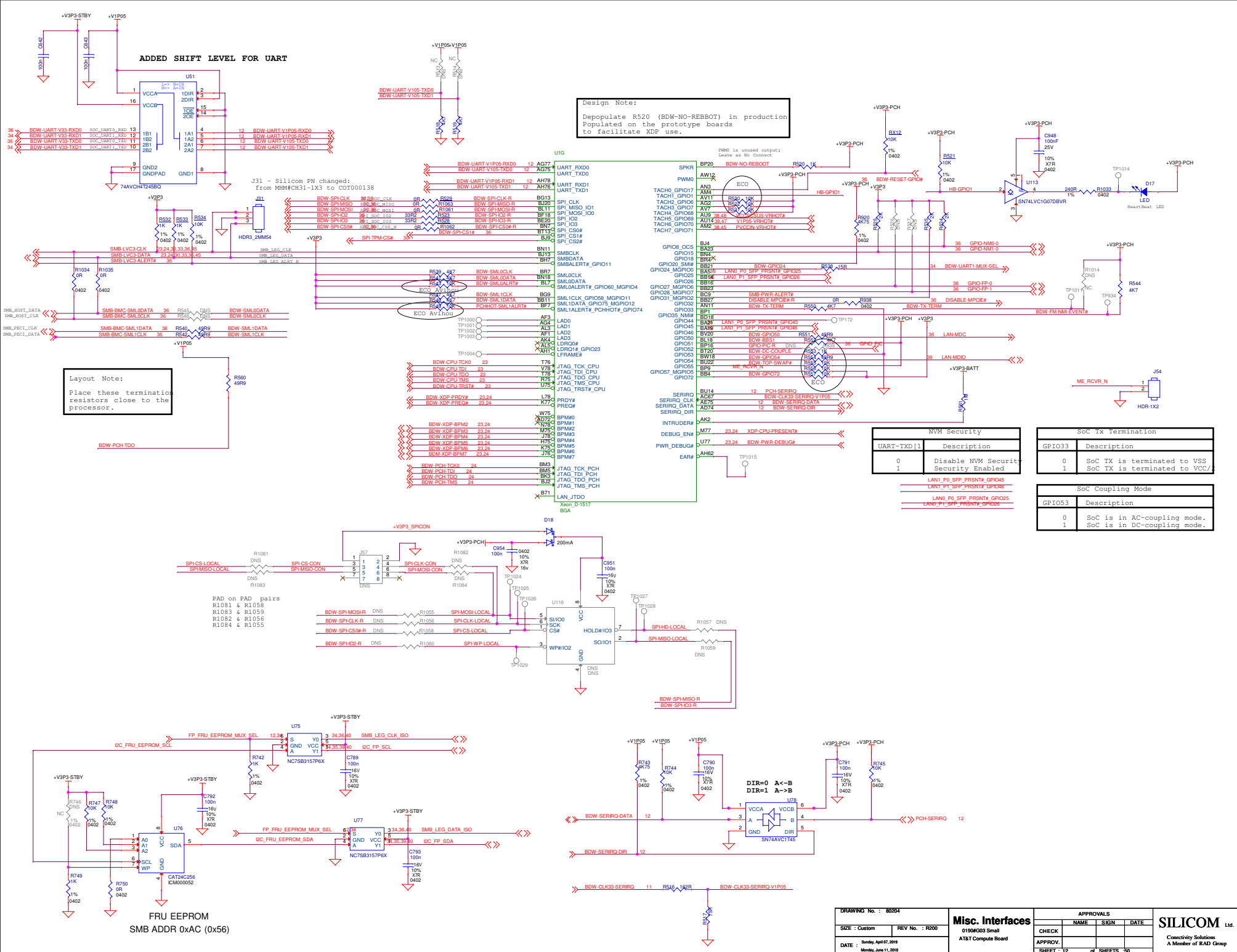
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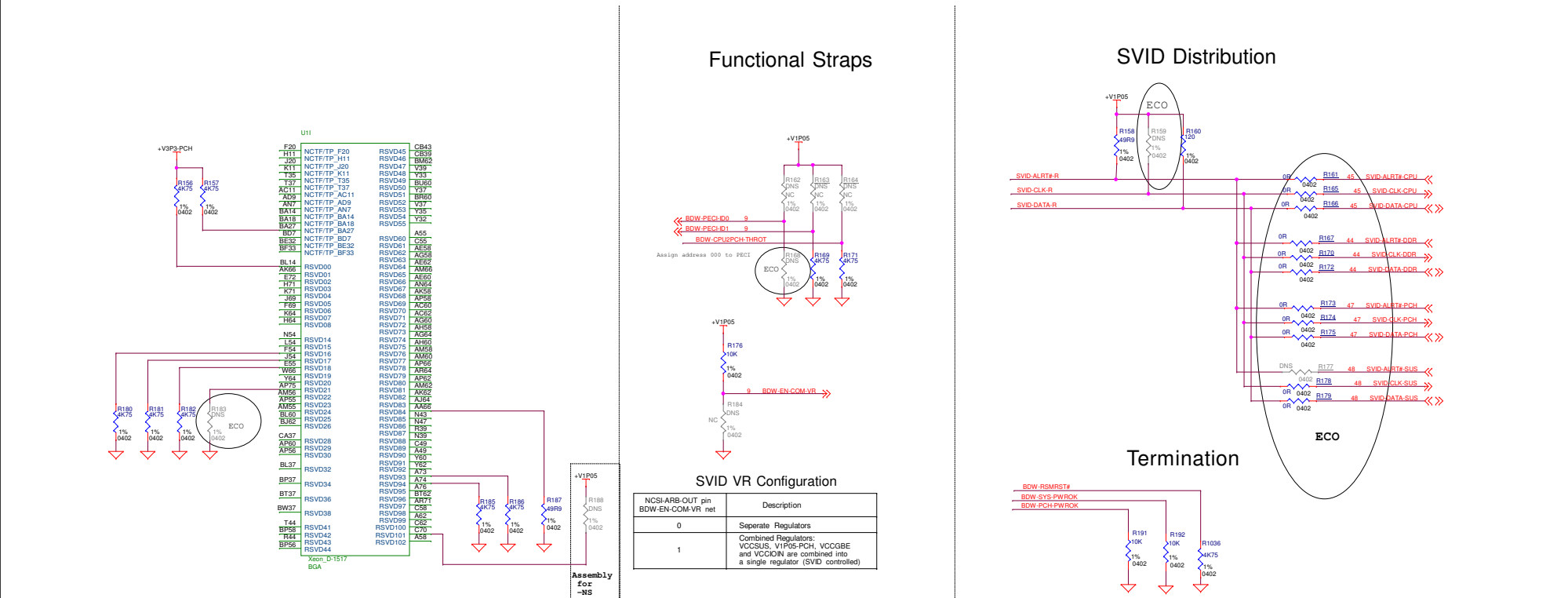
DATE : Sunday, April 07, 2019
Saturday, May 19, 2018

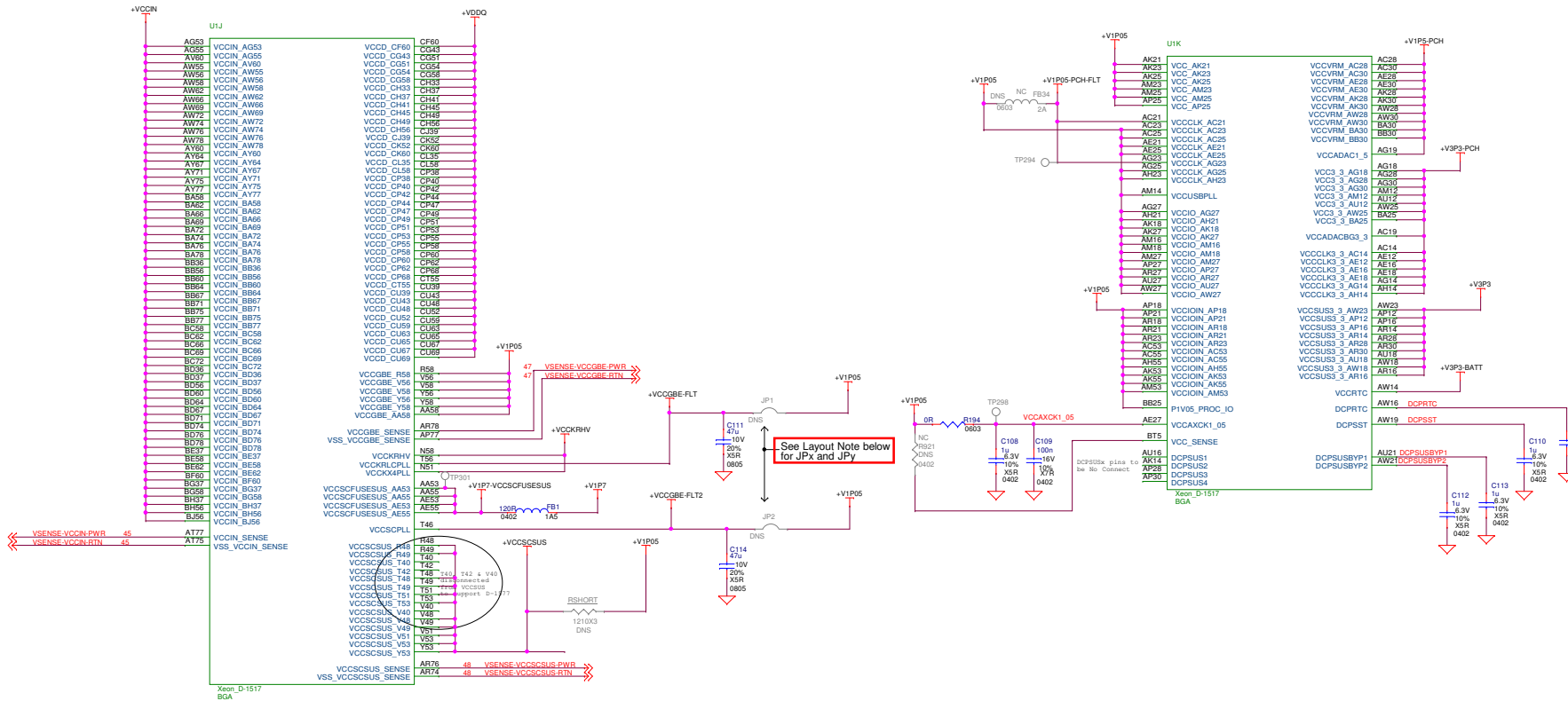
Clocks
0190G03 Small
A18T Compute Board

APPROVALS		
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SHEET : 11	of SHEETS : 30	

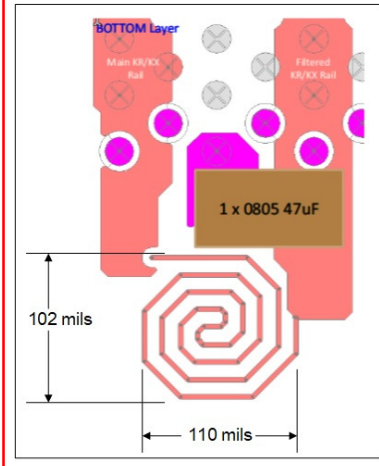
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Layout note:
Diagram of 4mil x 850mil trace,
from Intel documentation.



DRAWING No. : 80304

SIZE : Custom REV No. : R200

DATE : Sunday, April 07, 2019

Tuesday, July 17, 2018

Power

01906003 Small

AT&T Compute Board

APPROVALS

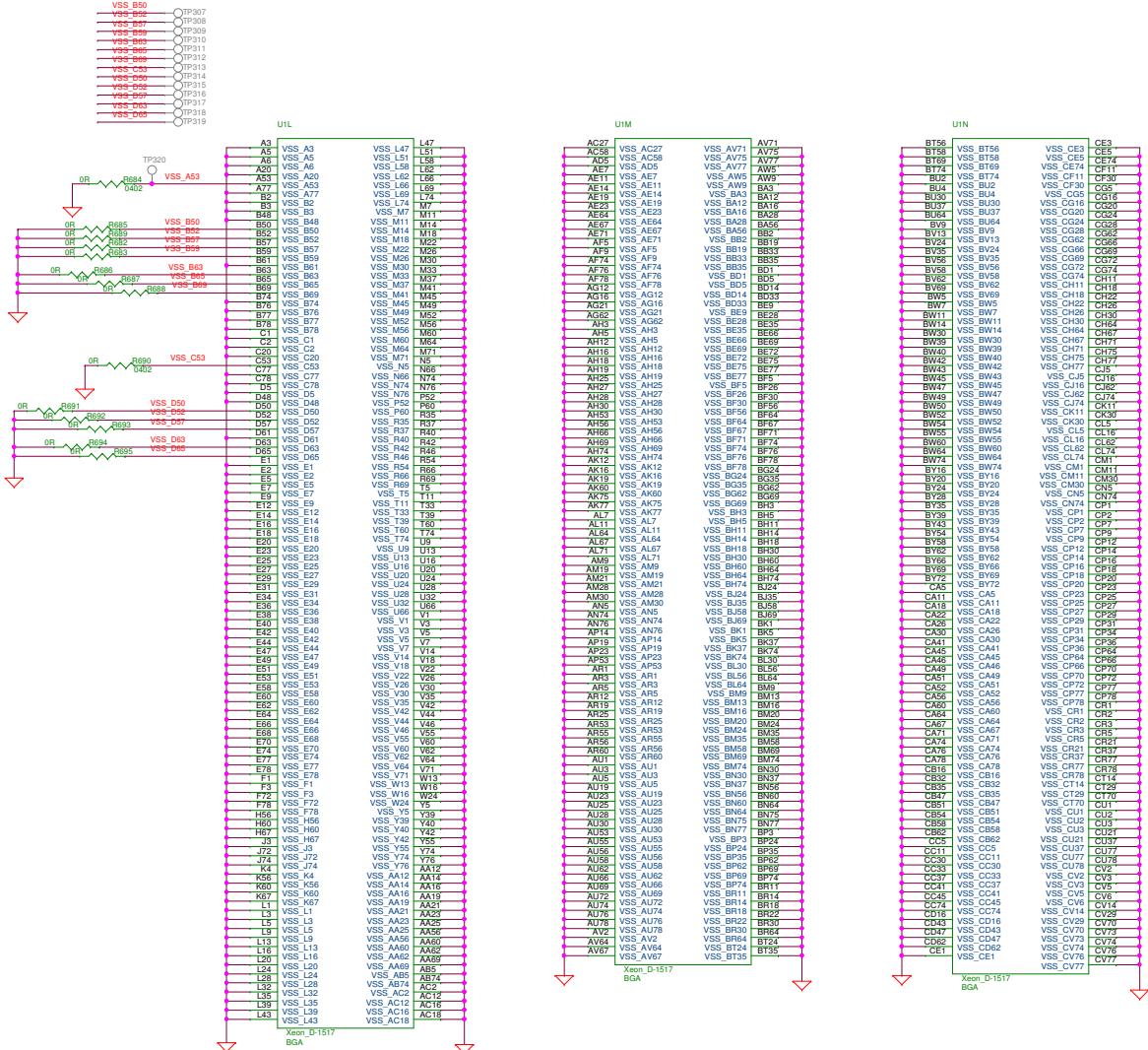
CHECK NAME SIGN DATE

APPROV. SHEET : 14 of SHEETS : 30

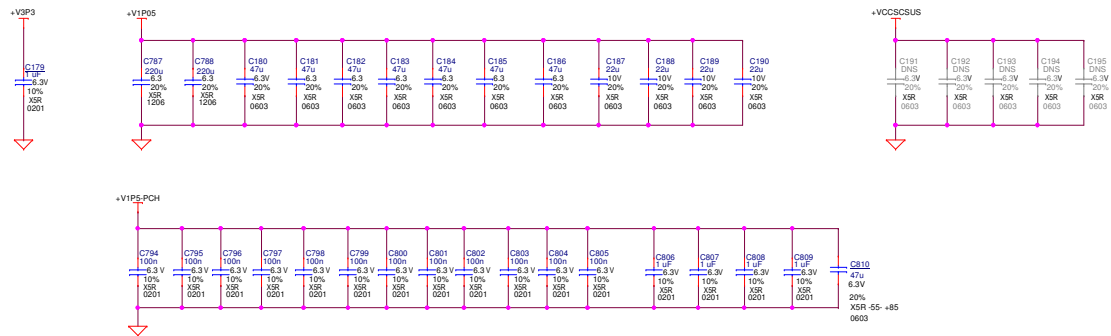
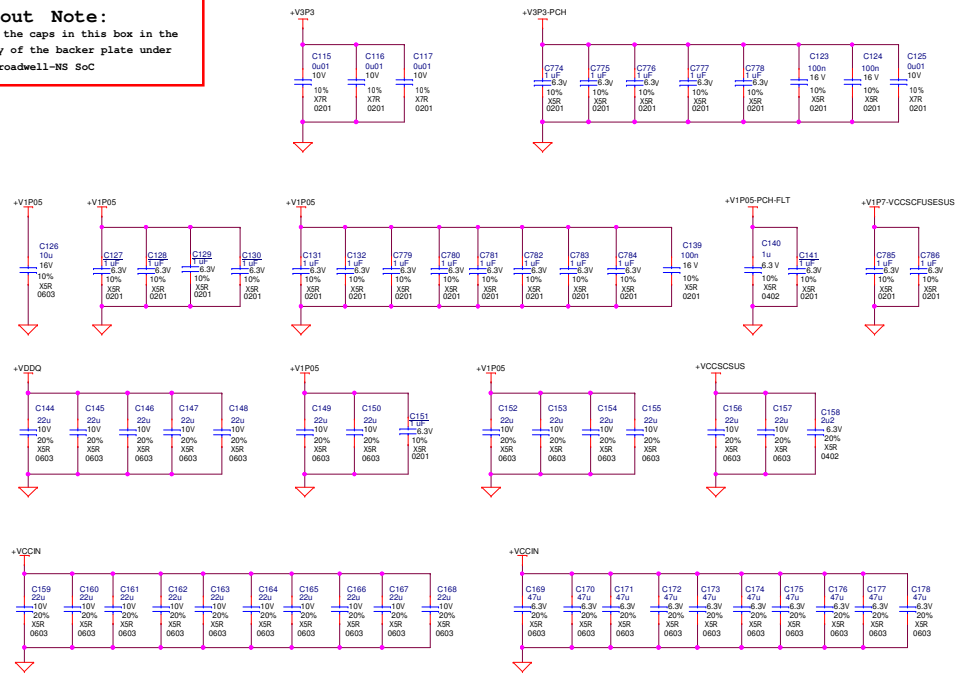
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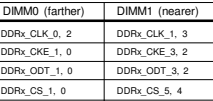


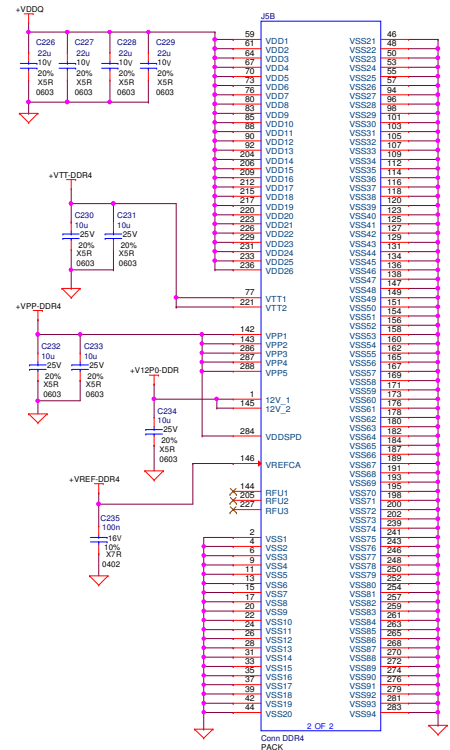
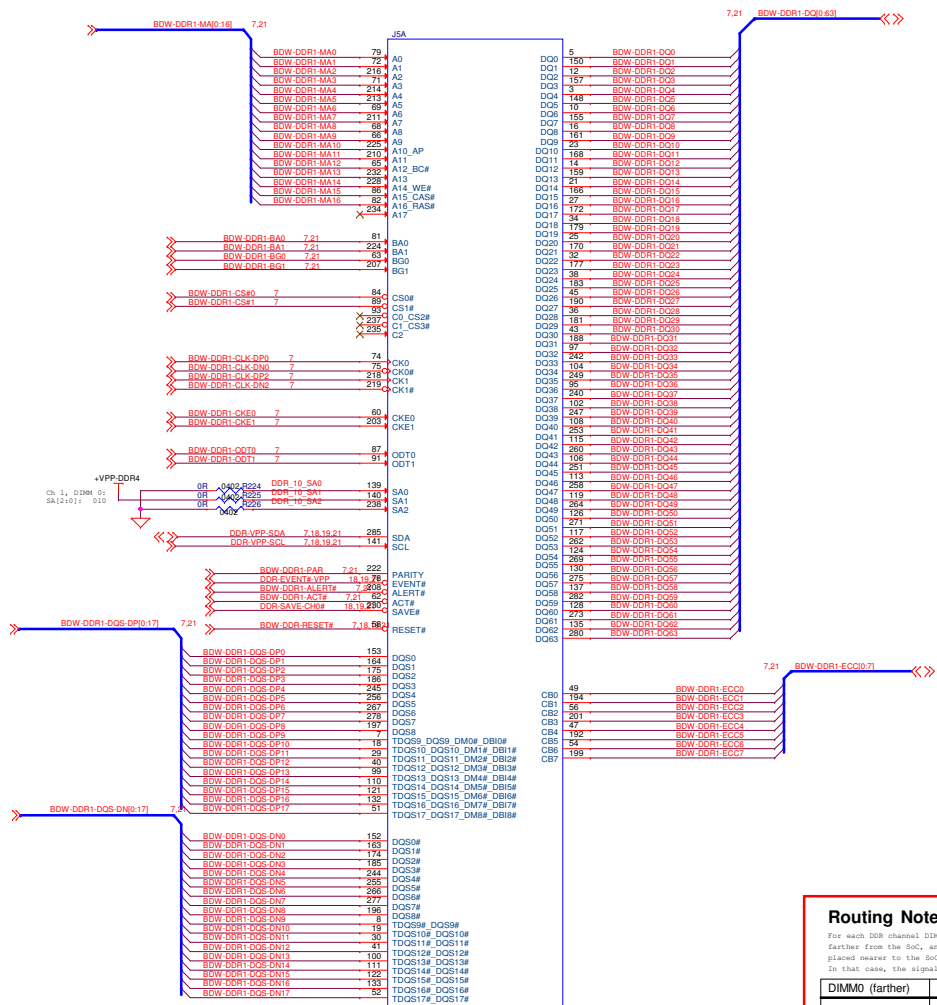
Place the caps in this box in the cavity of the backer plate under the Broadwell-NS SoC



DRAWING No. : 80204		Decoupling 0190G03 Small AT&T Computer Board	APPROVALS				SILICOM Concivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			NAME	SIGN	DATE	
			CHECK				
			APPROV.				
DATE : Sunday, April 07, 2019 Saturday, May 19, 2018			SHEET : 14		SHEETS : 50		

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Routing Notes:

For each DDR channel DIMM0 is to be placed farther from the SoC, and DIMM1 is to be placed nearer to the SoC.

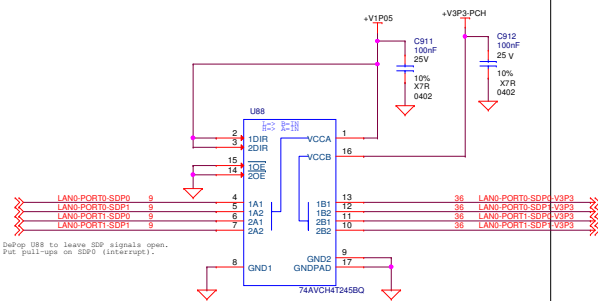
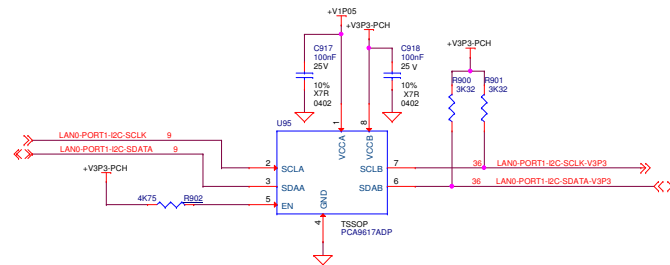
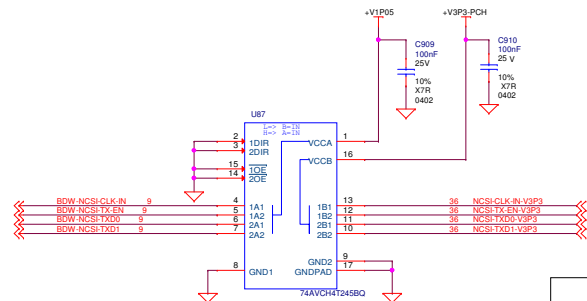
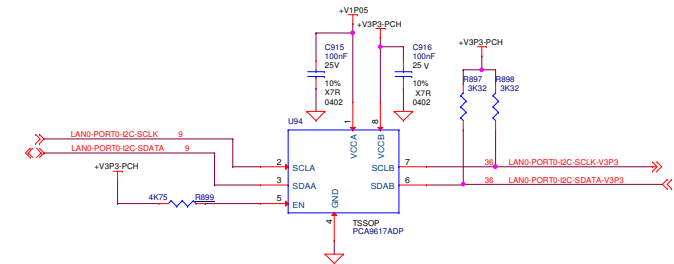
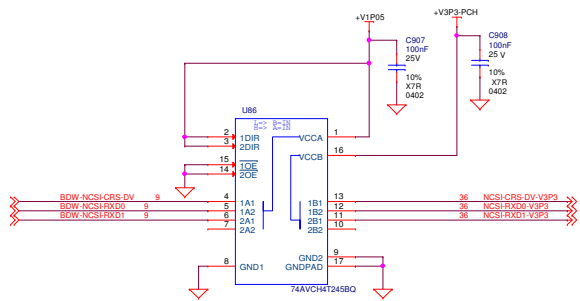
In that case, the signals are to be routed as:

DIMM0 (farther)	DIMM1 (nearer)
DDR _x _CLK_0_2	DDR _x _CLK_1_3
DDR _x _CKE_1_0	DDR _x _CKE_3_2
DDR _x _ODT_1_0	DDR _x _ODT_3_2
DDR _x _CS_1_0	DDR _x _CS_5_4

DDR4 Channel 1, DIMM 0

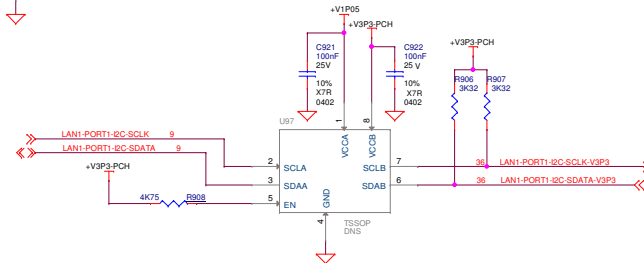
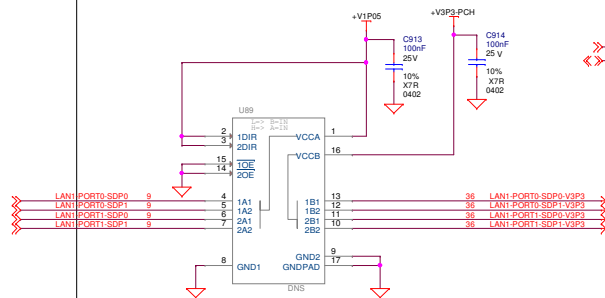
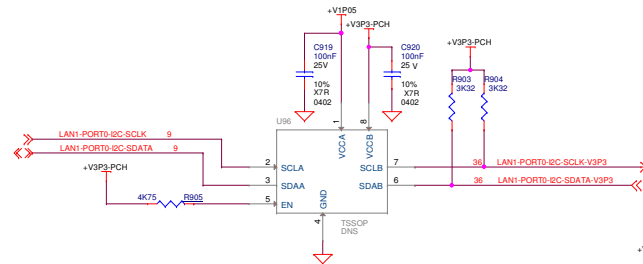
DRAWING No. : 80304		DDR Ch 1, DIMM 0 01909G3 Small AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200		CHECK	NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019			APPROV.				
DATE : Tuesday, July 17, 2018			SHEET : 50	of SHEETS : 50			

SHEET : 20 of SHEETS : 30



DePop U88 to leave SDP signals open.
Put pull-ups on SDP0 (interrupts).

Not used in this design



DRAWING No. : 80504

SIZE : Custom REV No. : R200

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Monday, June 11, 2018

LAN Level Shifters

0190WG03 Small

AT&T Compute Board

APPROVALS

CHECK NAME SIGN DATE

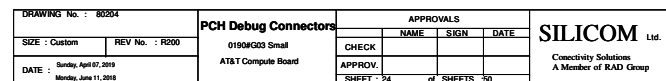
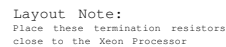
APPROV.

SHEET : 22 of SHEETS : 30

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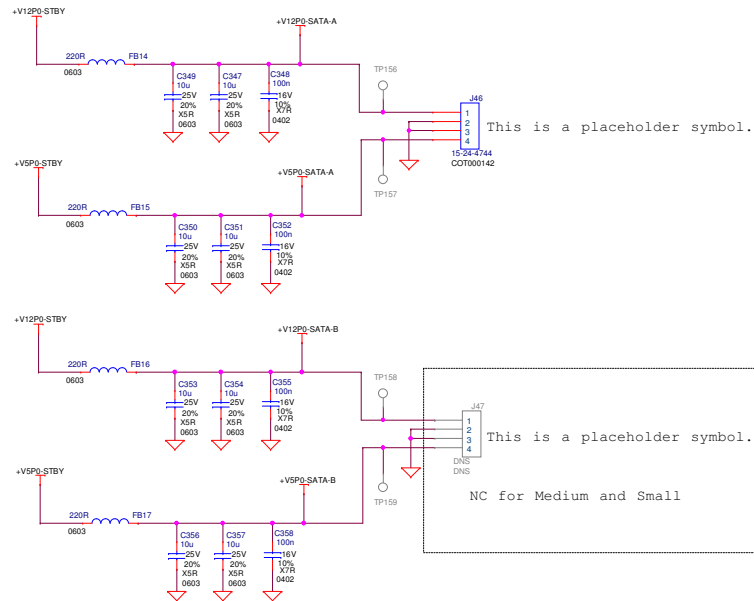
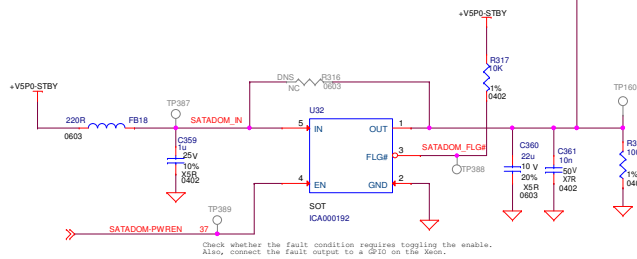
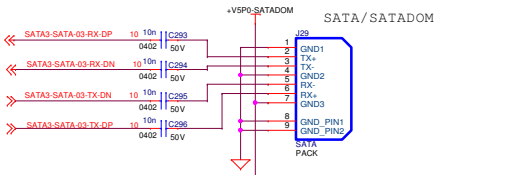
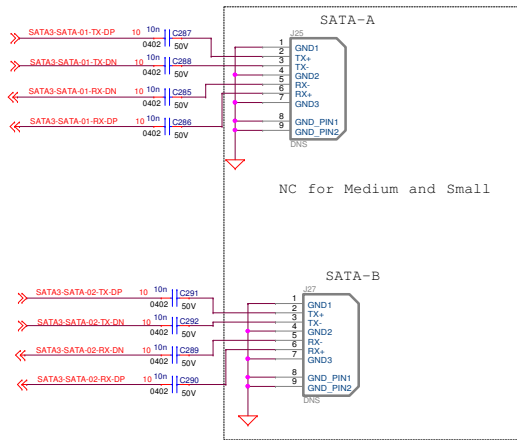
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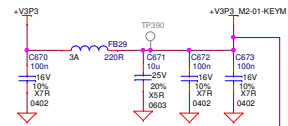


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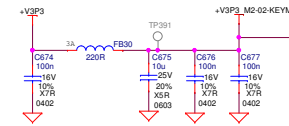
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DRAWING No. : 80504		Blank 0190RG03 Small AT&T Compute Board	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group	
SIZE : Custom	REV No. : R200			NAME	SIGN		DATE
DATE : Sunday, April 07, 2019			CHECK				
Monday, June 11, 2019			APPROV.				
			SHEET : 28 of SHEETS : 30				

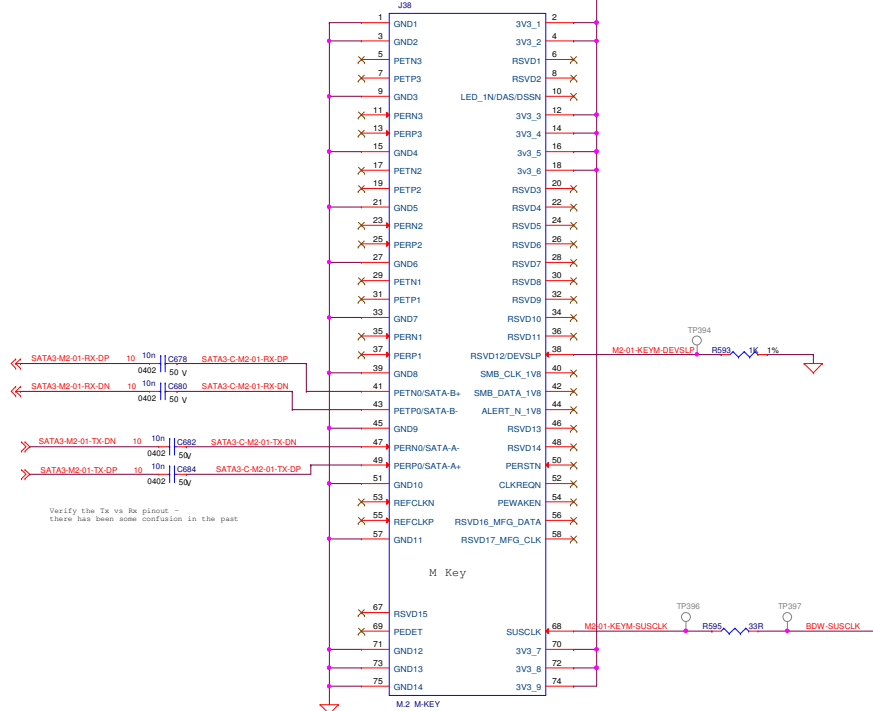




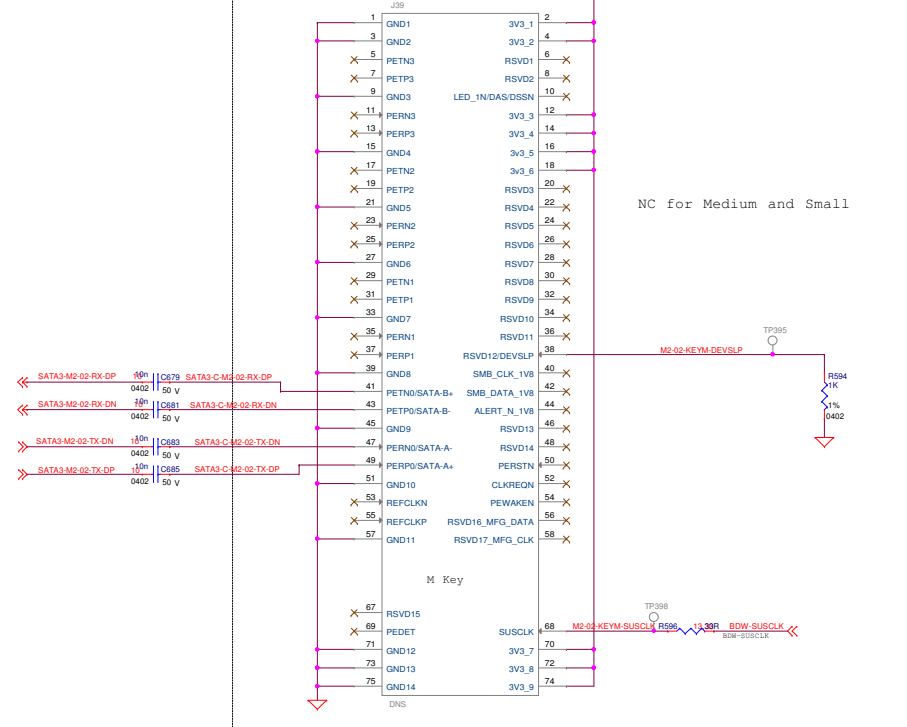
The pinout of the M.2, M-Key connector on the -0144 design is different than the pinout on this page. It is necessary to resolve these differences

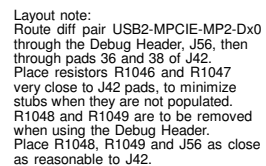
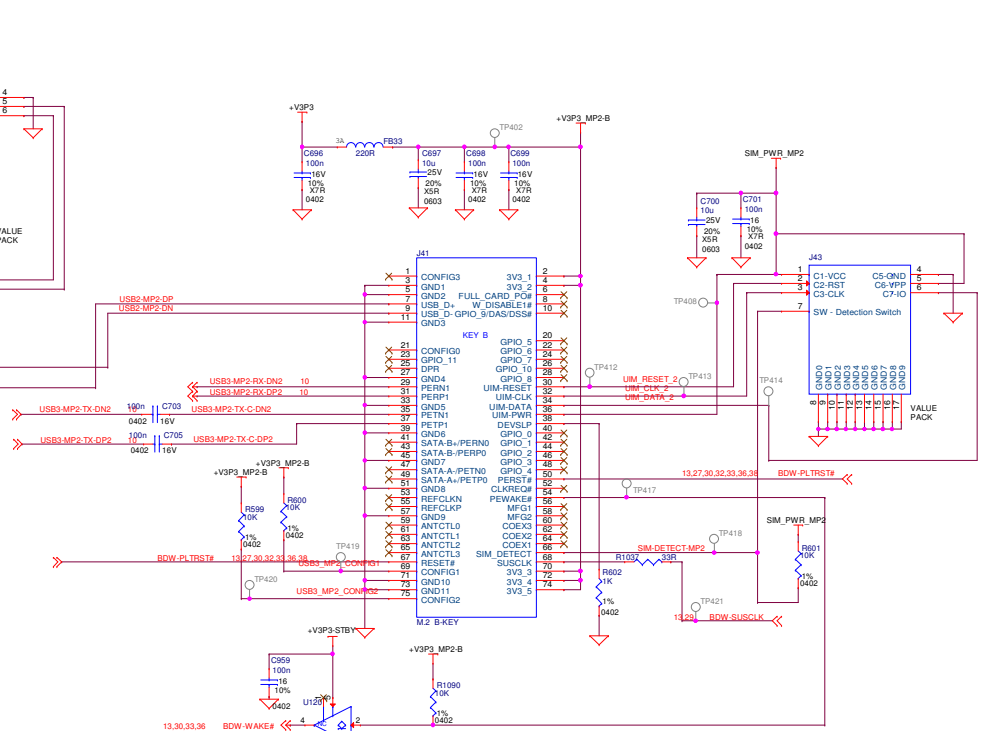


M.2 - 01 Connector



M.2 - 02 Connector



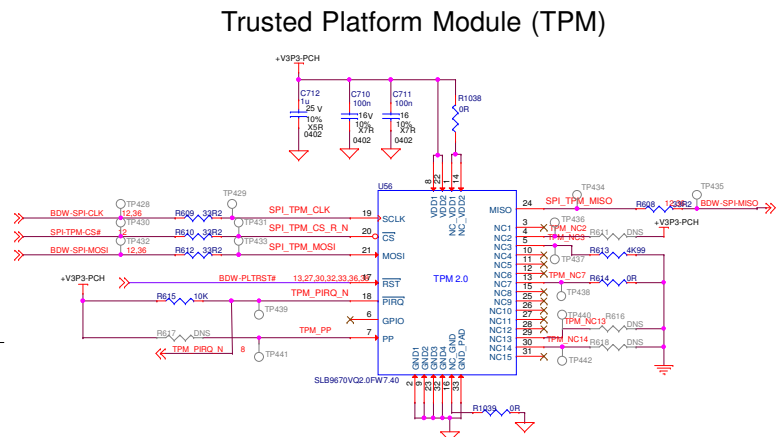


R1046 and R1047 are NC when using the mPCIe connector; they are populated when using the M.2 connector. Place them as close as reasonable to J42.

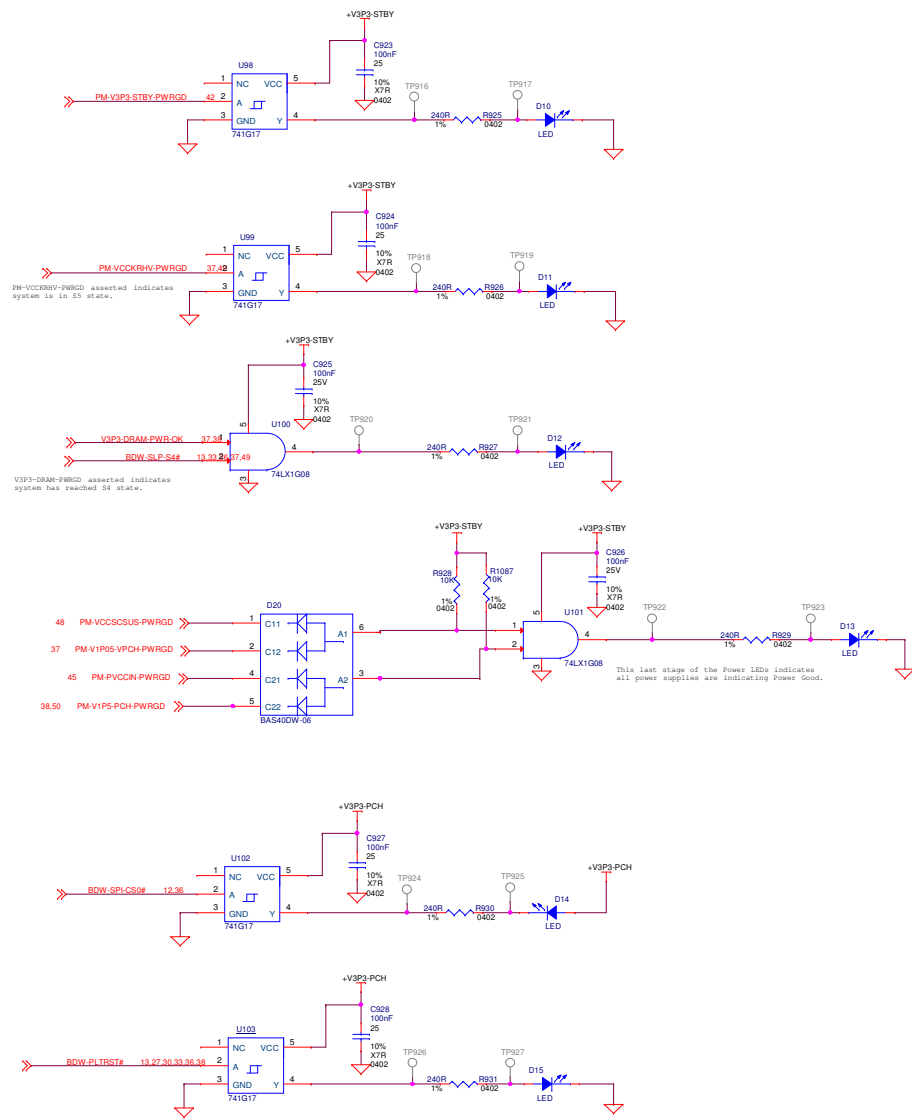
TPM Pin	Part	Populate Part	
		Infineon	Atmel
7	R***	note 1	
4	R***		note 2
29	R***		X
30	R***		X

Notes:

1. Pin on Infineon part has internal PD. Populate pullup R*** to gain "super user" access.
2. Pin on Atmel part has internal PD. Populate pullup R*** to gain "super user" access.



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DRAWING No. : 80204		LEDs 0190W03 Small AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200						
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DATE : Sunday, April 07, 2019 Tuesday, July 17, 2018			SHEET : 32	of SHEETS : 50			



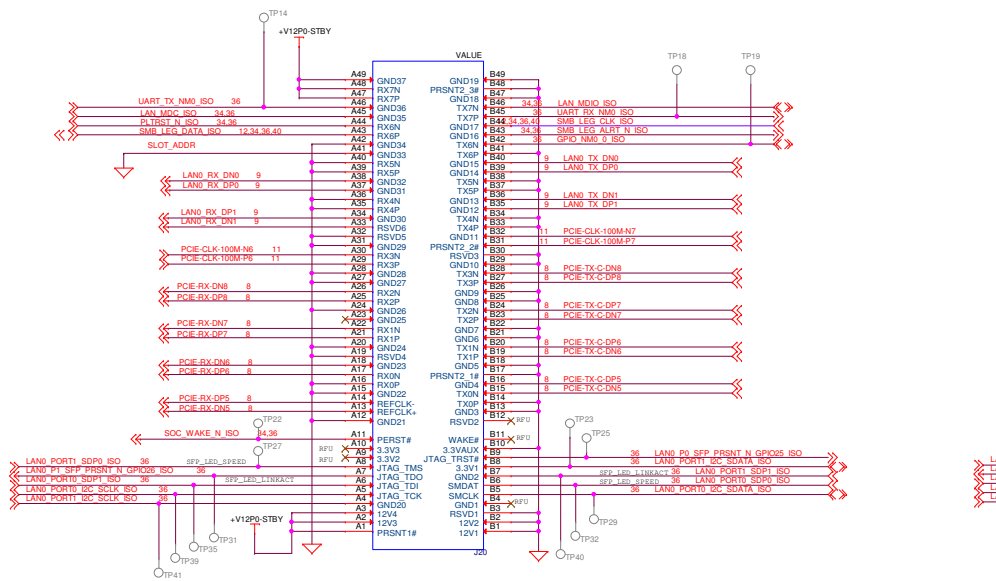
12V DDR Core Load Switch

Determine why this clock connection is in place.
If not removed, there should be zero ohm resistors to allow to disconnect.

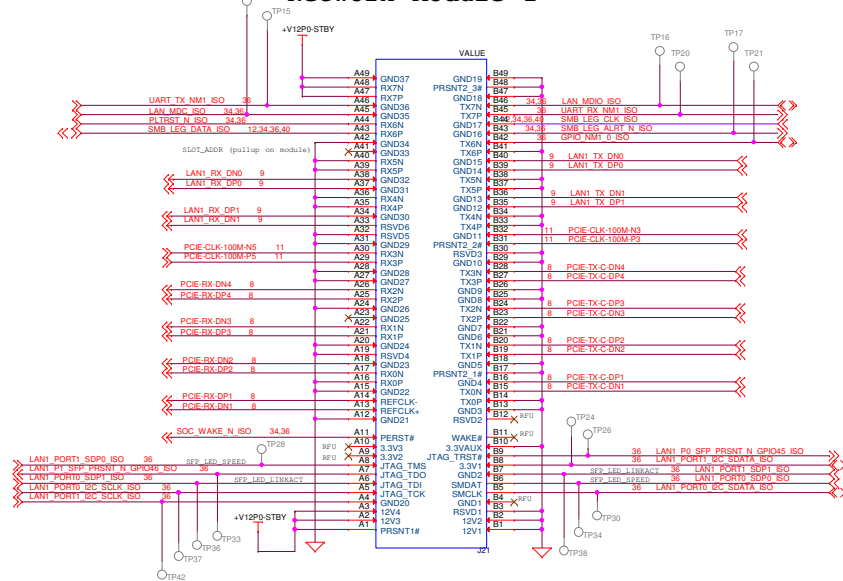
DRAWING No.: 00204		Side Expenditure Slots 0104003 Small AT&T Compute Board	APPROVALS <table> <tr> <th></th> <th>NAME</th> <th>SIGN</th> <th>DATE</th> </tr> <tr> <td>CHECK</td> <td></td> <td></td> <td></td> </tr> <tr> <td>APPROV.</td> <td></td> <td></td> <td></td> </tr> <tr> <td>SHEET: 33</td> <td colspan="3">of SHEETS: 50</td> </tr> </table>					NAME	SIGN	DATE	CHECK				APPROV.				SHEET: 33	of SHEETS: 50			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
	NAME		SIGN	DATE																			
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DATE: Sunday, April 07, 2018 Wednesday, October 31, 2018																							

NOTE:
The net names on these connectors were copied from the -0150 schematic. They will need to be updated to reflect their use in this design, once the Xeon is placed.

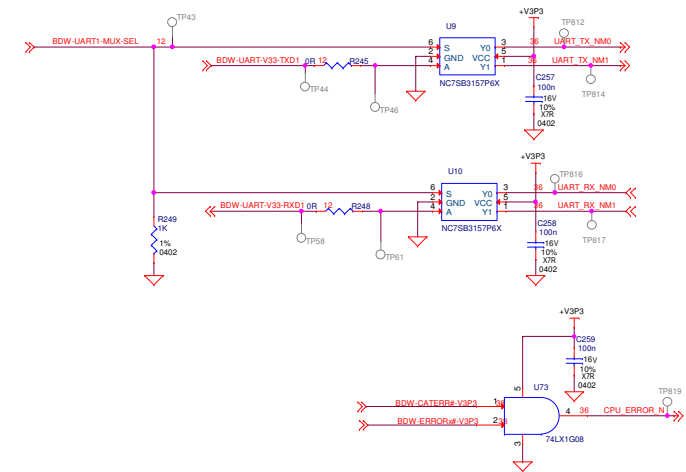
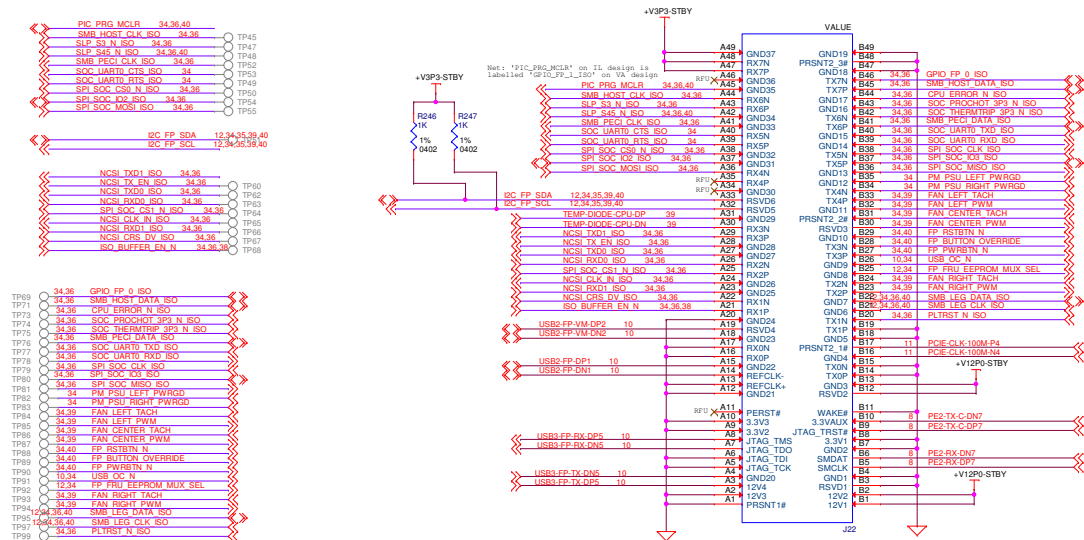
Network Module 0



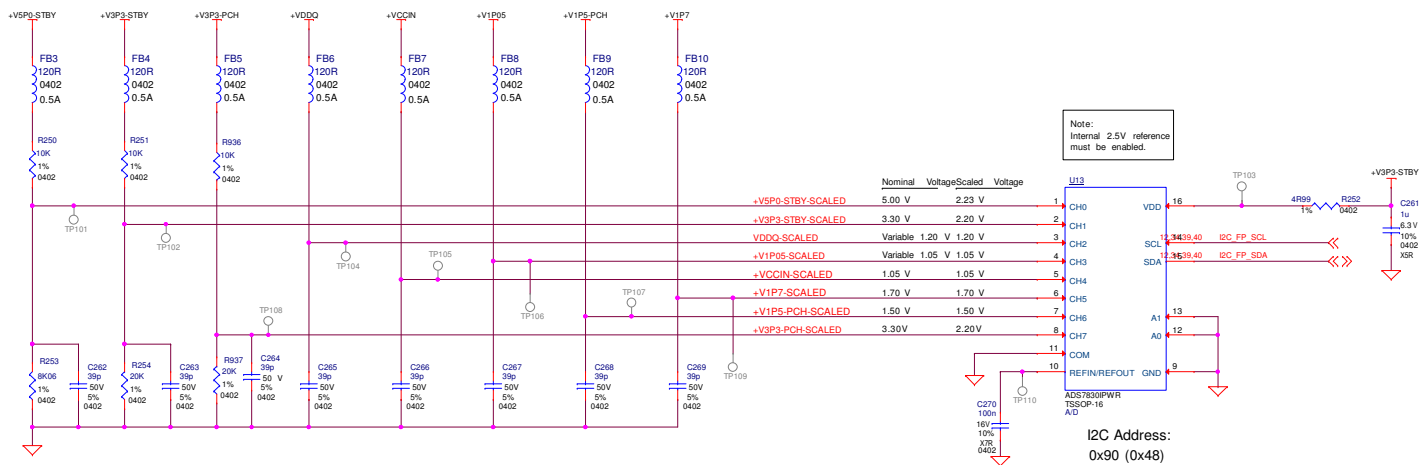
Network Module 1



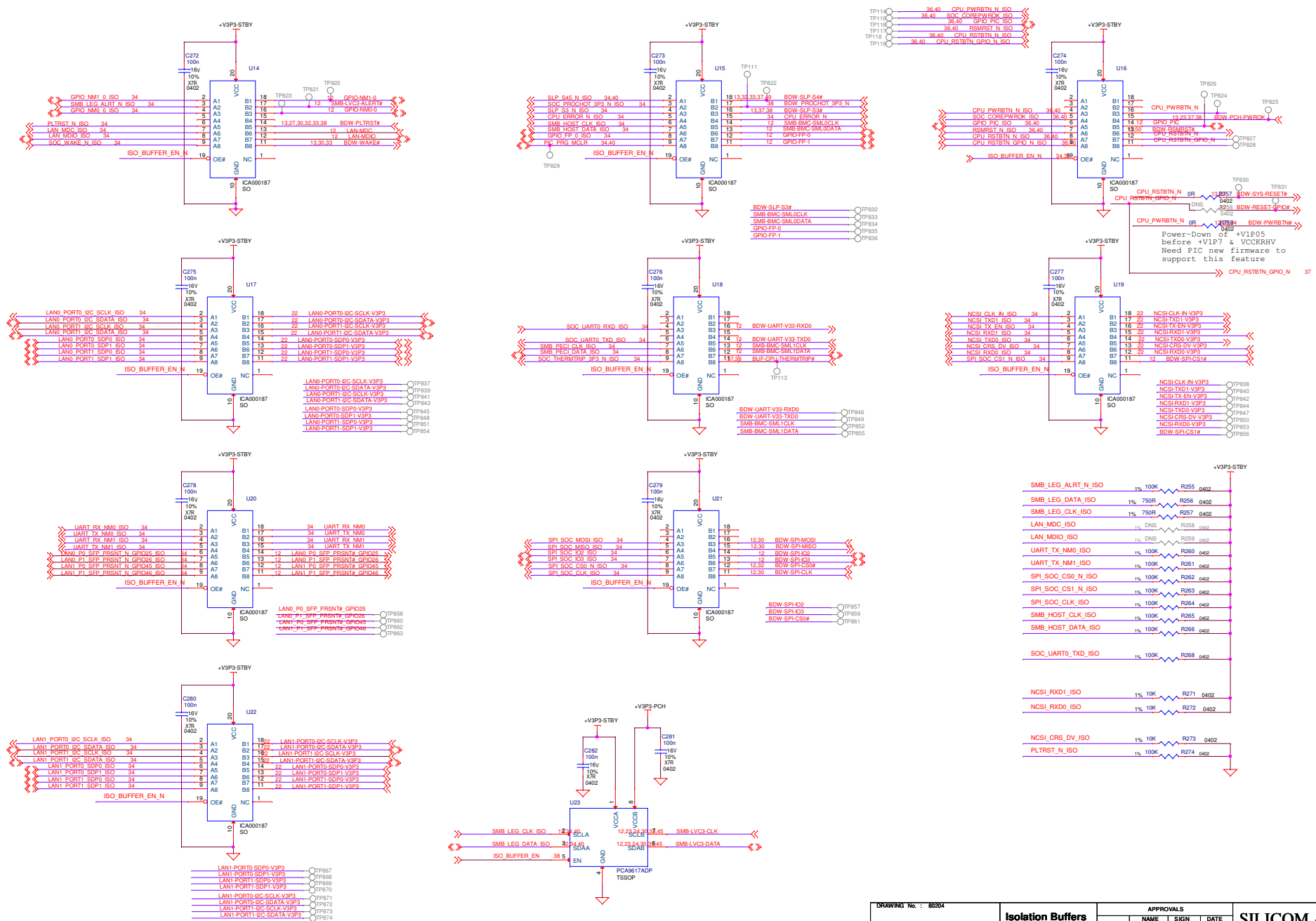
Front Panel I/O Module



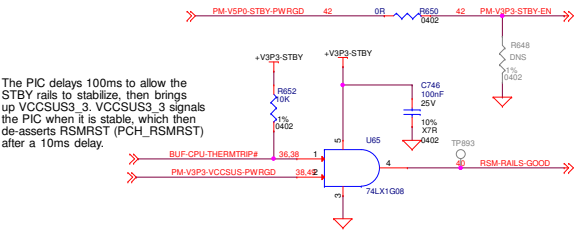
ADC Voltage Monitor
(0 to +2.5 V Range)



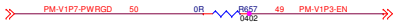
3.3V Isolation Buffers



+V5P0-STBY comes up when the 12V input rises above 9.3V. The +V5P0-STBY then enables +V3P3-STBY, which then powers the PIC controller.
PIC has an internal POR of 40-140ms.



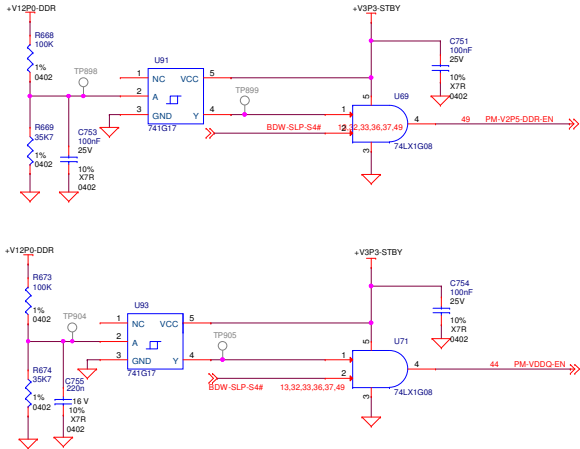
RSMRST also enables VCCSCFUSEBUS (+V1P7), which then enables VCCKRHV (+V1P3).



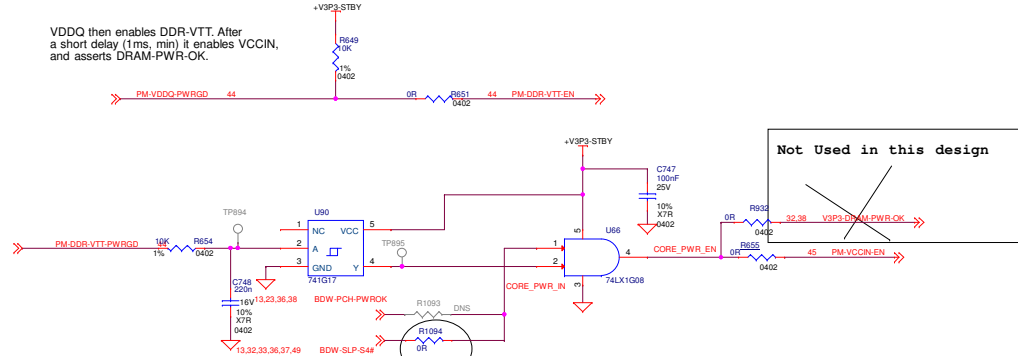
PIC loops monitoring the front panel buttons and signals the Broadwell when the Power Button is pressed, which then de-asserts SLP_S4#, and after 30us delay, SLP_S3#

BDW-SLP-S4 enables the 12V rails to the PCIe expansion connector and the DDR DIMMs.

+V12P0-DDR enables +V2P5-DDR and VDDQ.
+V2P5 is delayed approx 10ms and VDDQ is delayed another 10-12 ms.

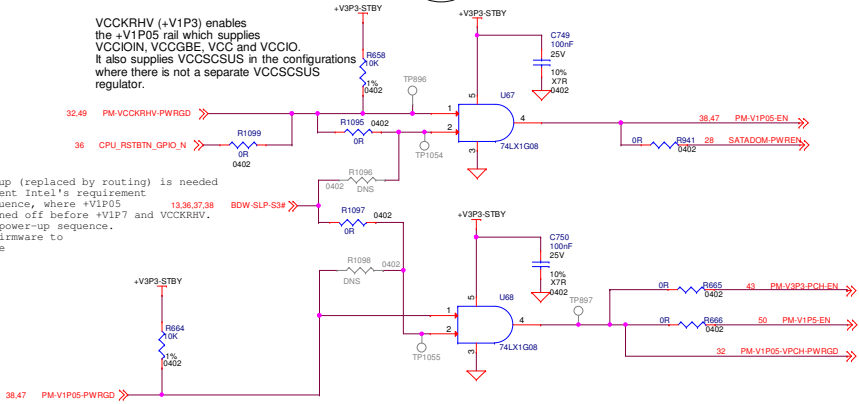


VDDQ then enables DDR-VTT. After a short delay (1ms, min) it enables VCCIN, and asserts DRAM-PWR-OK.



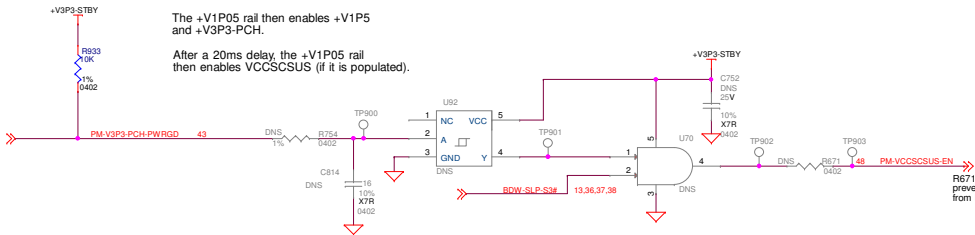
VCCKRHV (+V1P3) enables the +V1P05 rail which supplies VCCIOIN, VCCGBE, VCC and VCCIO. It also supplies VCCSCSUS in the configurations where there is not a separate VCCSCSUS regulator.

This manual touch-up (replaced by routing) is needed in order to implement Intel's requirement for power-down sequence, where +V1P05 rail should be turned off before +V1P7 and VCCKRHV. Doesn't impact on power-up sequence. Required new PIC firmware to support this change



The +V1P05 rail then enables +V1P5 and +V3P3-PCH.

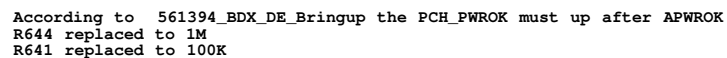
After a 20ms delay, the +V1P05 rail then enables VCCSCSUS (if it is populated).



Cause to VDDQ up after PCH-PWROK

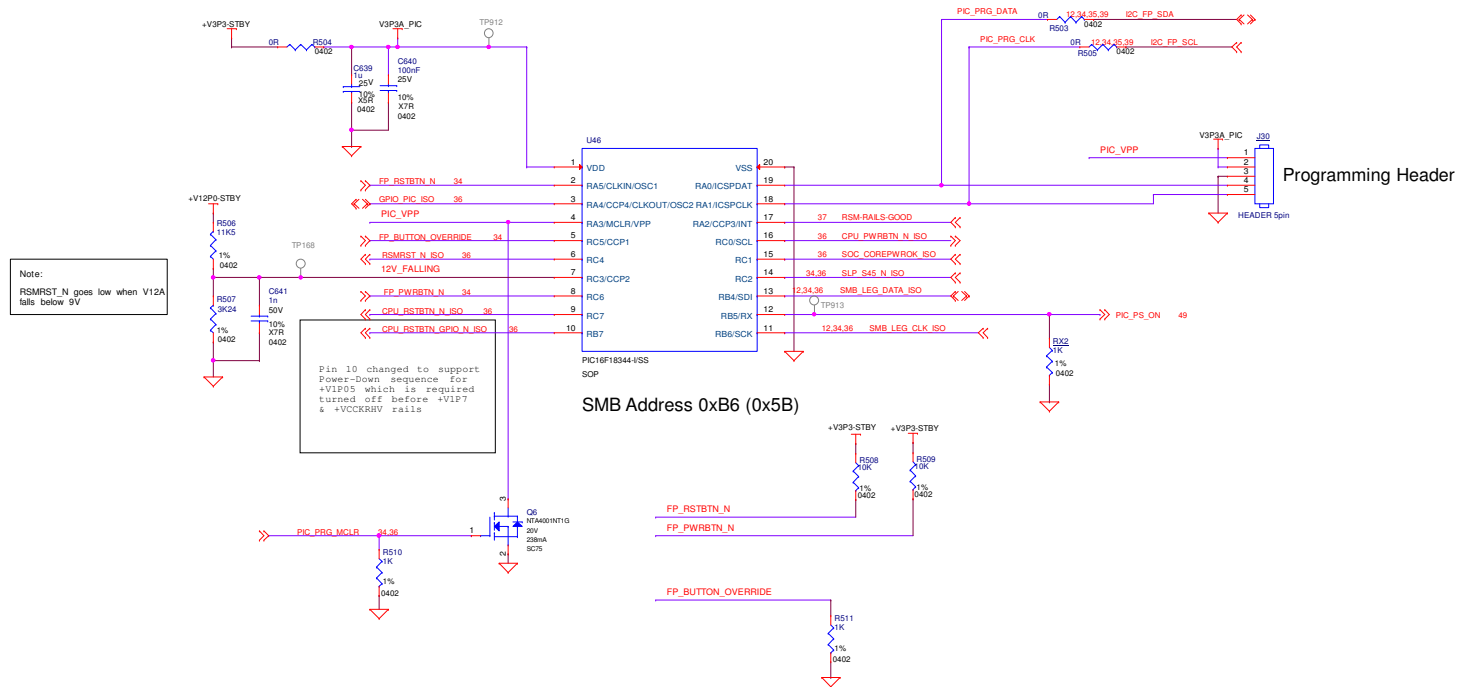
R671 is NC for the initial build to prevent VCCSCSUS regulator (U43) from being Enabled.

3.3V <--> 1.05V Level Shifting

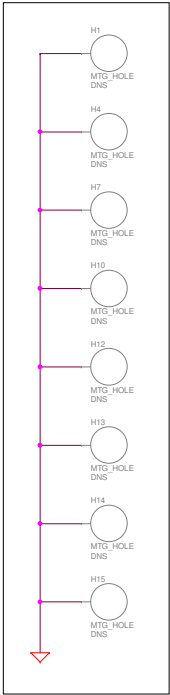


DRAWING No. : 80204		Power Sequencing & Level Shifters 0100K003 Small AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200		CHECK	NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019 Thursday, July 19, 2018			APPROV.				
			SHEET : 18		SHEETS : 50		

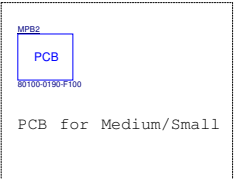
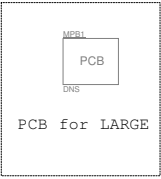
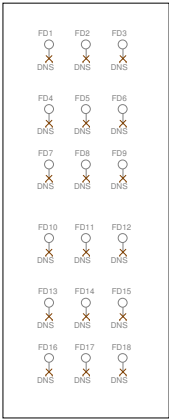
PIC Microcontroller



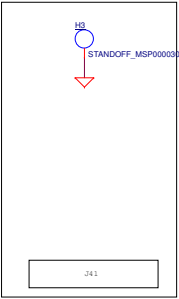
Mounting Holes



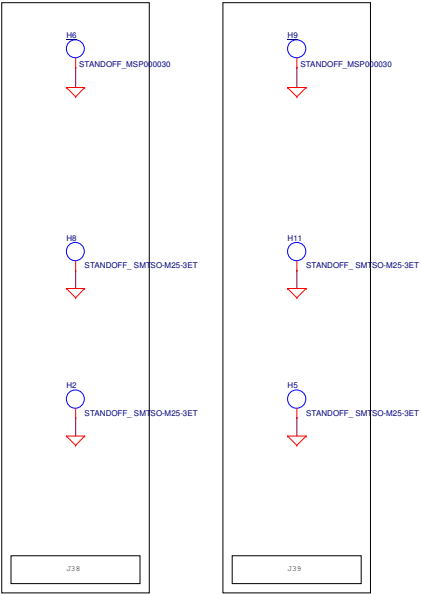
Fiducials



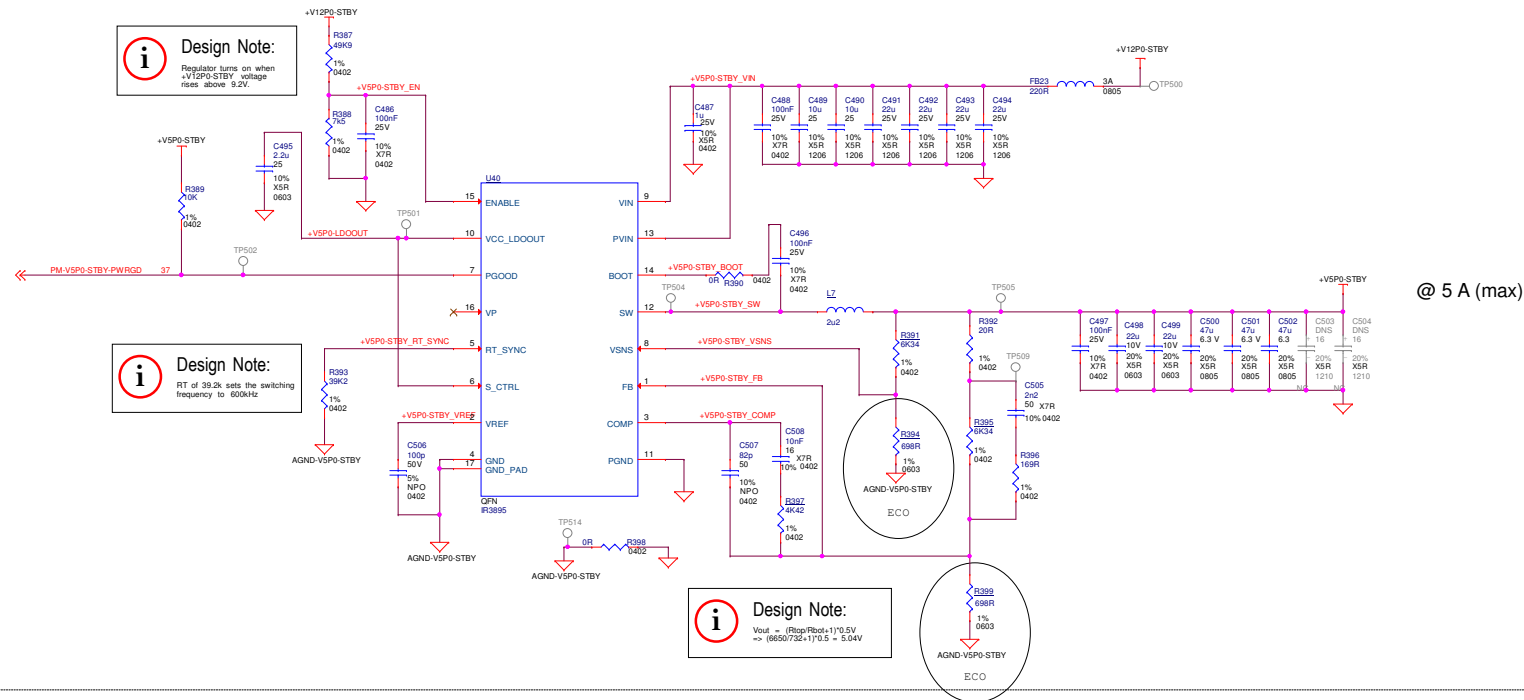
M.2 Standoffs



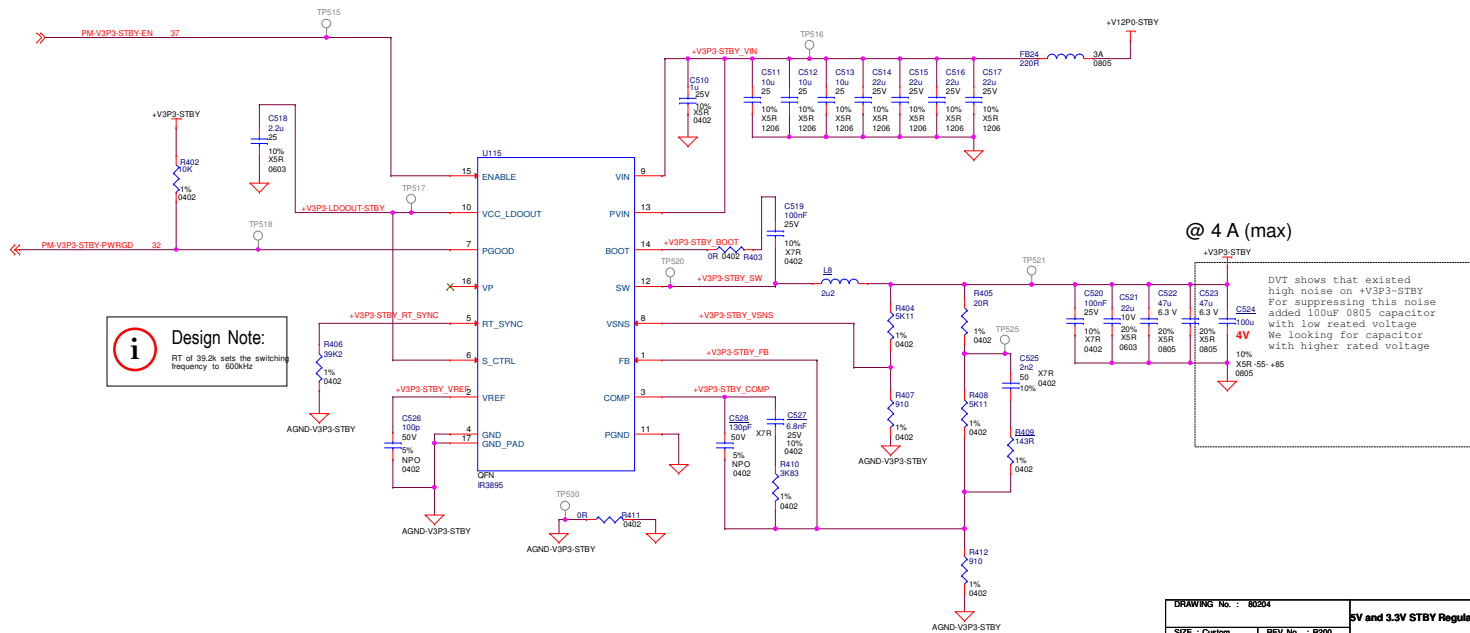
M.2 Standoffs



5V STBY Switching Regulator

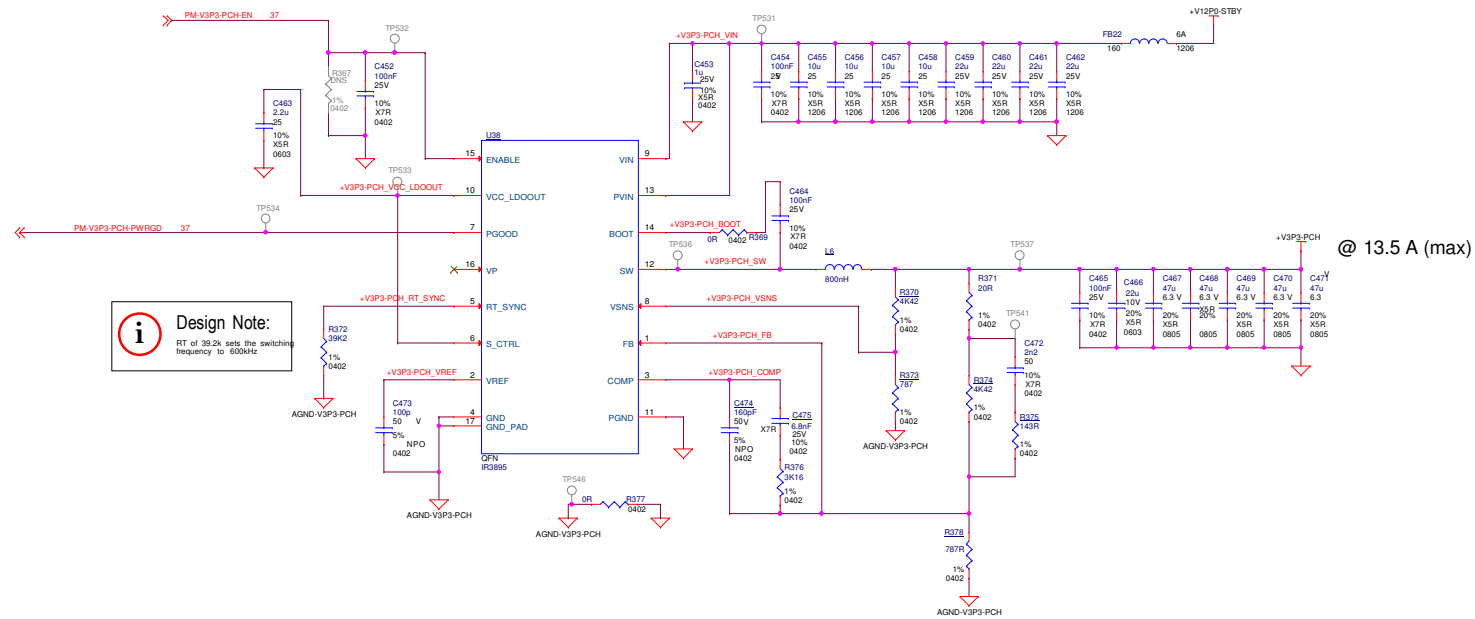


3.3V STBY Switching Regulator



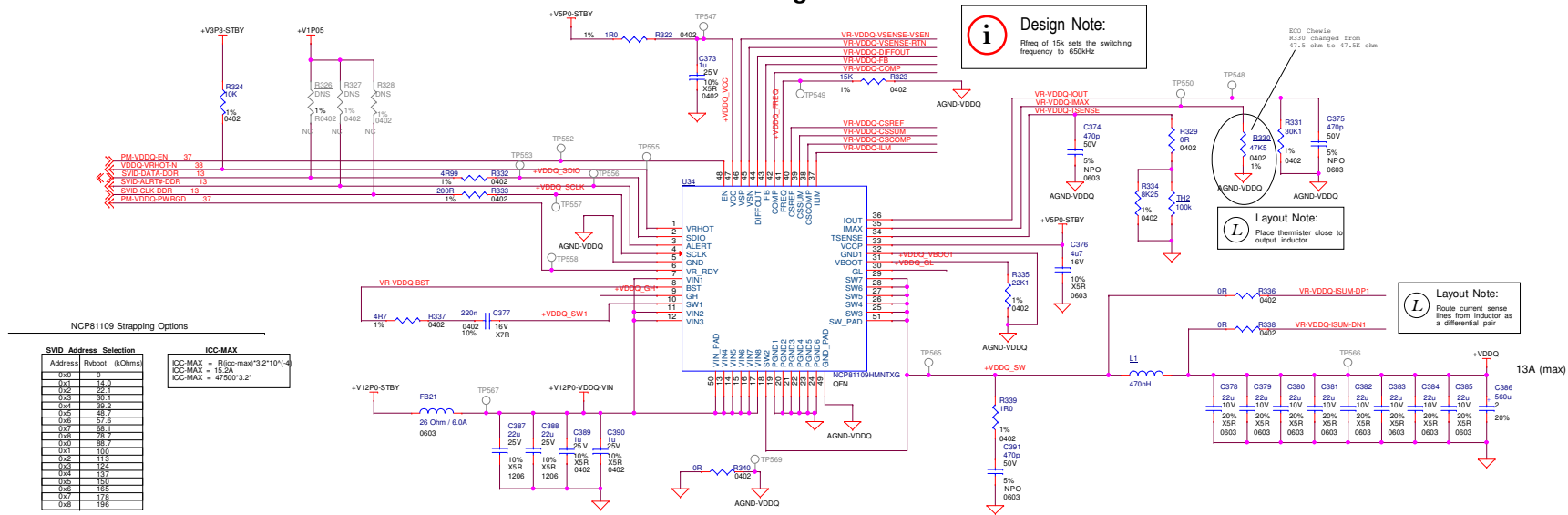
DRAWING No. : 80504		5V and 3.3V STBY Regulators		APPROVALS		SILICOM Ltd.
SIZE : Custom	REV No. : R200	0190KG03 Small AT&T Compute Board		CHECK	NAME SIGN DATE	
DATE : Sunday, April 07, 2019				APPROV.		
Wednesday, July 18, 2018					SHEET : 42 of SHEETS : 30	

3.3V PCH Switching Regulator

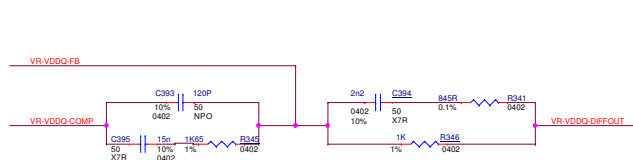


DRAWING No. : 80204		3.3V PCH Regulator 0190G03 Small AT&T Compute Board	APPROVALS				SILICON Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019 Wednesday, July 18, 2018			CHECK				
			APPROV.				
			SHEET : 43	of	SHEETS : 50		

VDDQ Regulator

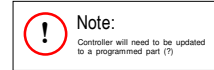


VDDQ Regulator Loop Compensation Network

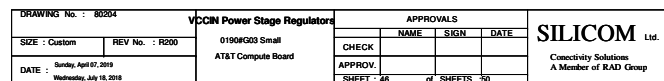


Design Note:

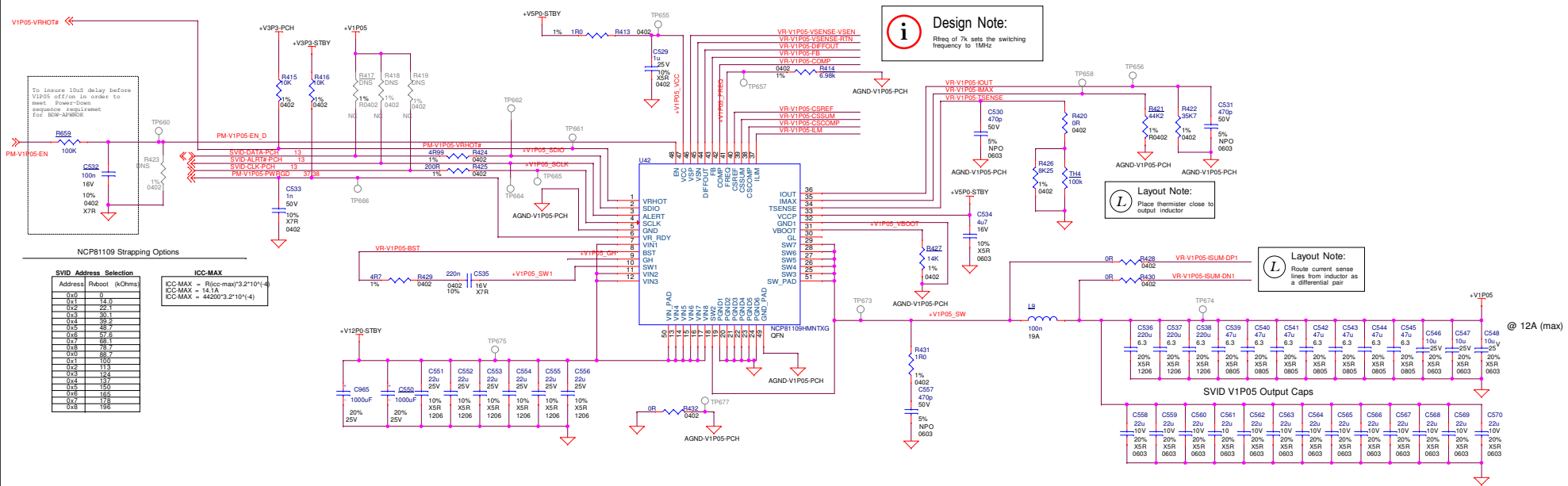
¶ NCP81111 needs to be reprogrammed in-circuit, use Devantech USB to I2C adapter (PN R286-USB-I2C) and GUI from On-Semi. See On-Semi NCP81111 programming presentation for overview.



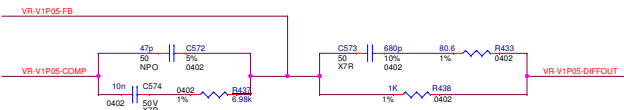
TEST3	TEST2	SVID Address "Offset"
0-Ohms to GND	0-Ohms to GND	0x0
22K-Ohms to GND	0-Ohms to GND	0x1



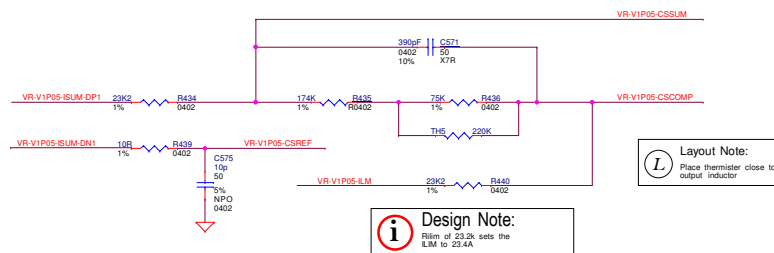
SVID V1P05 "Combined" Regulator



V1P05 Regulator Loop Compensation Network

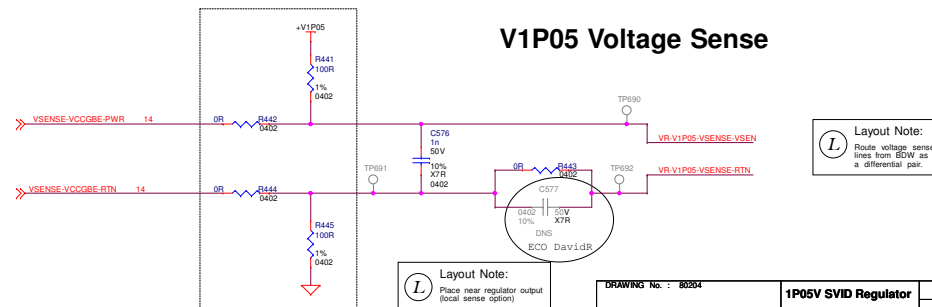


V1P05 Current Loop Compensation



12V DDR Core Load Switch

V1P05 Voltage Sense



DRAWING No. : 80304

SIZE : Custom

REV No. : R200

DATE : Sunday, April 07, 2019

Wednesday, July 18, 2018

1P05V SVID Regulator

0190AG03 Small

AT&T Compute Board

APPROVALS

CHECK NAME SIGN DATE

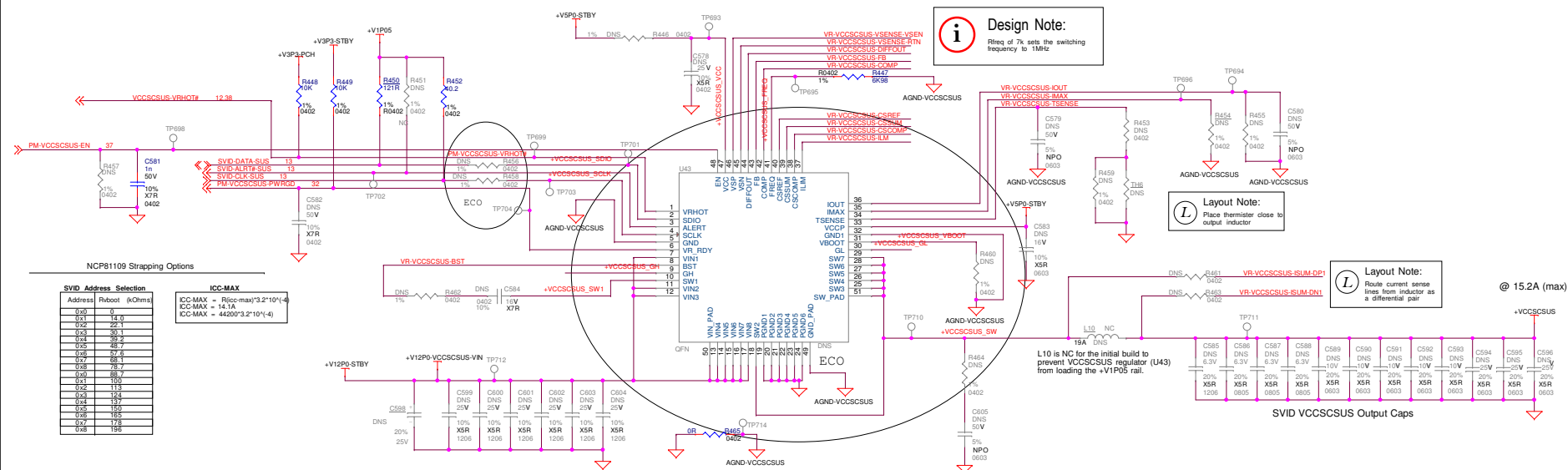
APPROV.

SHEET : 47 of SHEETS : 30

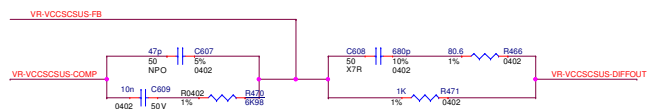
SILICOM Ltd.

Connectivity Solutions
A Member of RAD Group

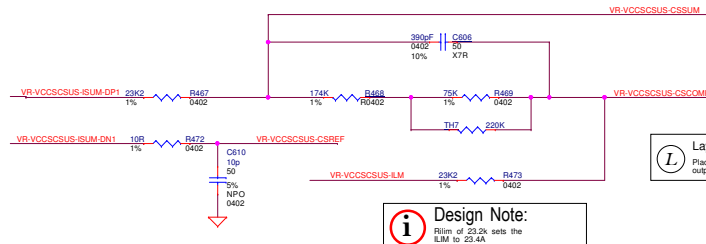
SVID VCCSCSUS Regulator



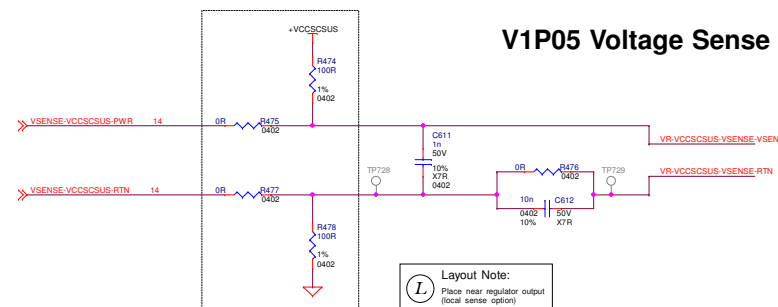
VCCSCSUS Voltage Loop Compensation Network



V1P05 Current Loop Compensation



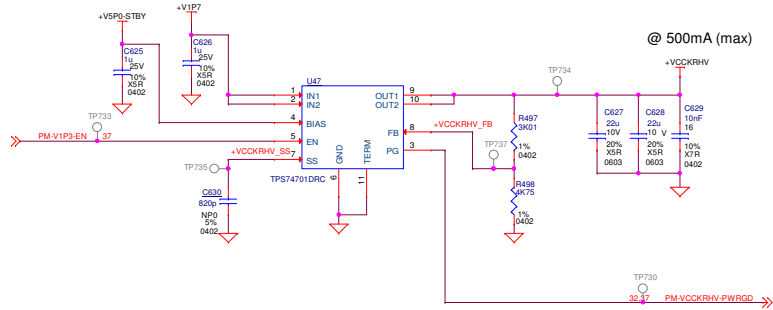
V1P05 Voltage Sense



SVID	Address	Selection
	Address	Rvboot (kOhms)
	0x0	0
	0x1	14.0
	0x2	22.1
	0x3	30.1
	0x4	39.2
	0x5	48.7
	0x6	57.6
	0x7	68.1
	0x8	78.7
	0x9	88.7
	0xA	100
	0xB	113
	0xC	124
	0xD	137
	0xE	150
	0xF	165
	0x7	178
	0x8	196

$$\begin{aligned} \text{ICC-MAX} &= R(\text{icc-max}) \cdot 3.2 \cdot 10^{(-4)} \\ \text{ICC-MAX} &= 14.1\text{A} \\ \text{ICC-MAX} &= 44200 \cdot 3.2 \cdot 10^{(-4)} \end{aligned}$$

1.3V Linear Regulator



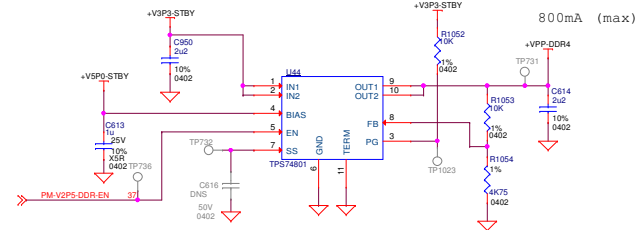
Design Note:

$t_{ss} = C_{in} \times 0.8V / 0.44\mu A$
 $t_{ss} = 0.00082 \times 0.8 / 0.44$
 $t_{ss} = 1.49msec$

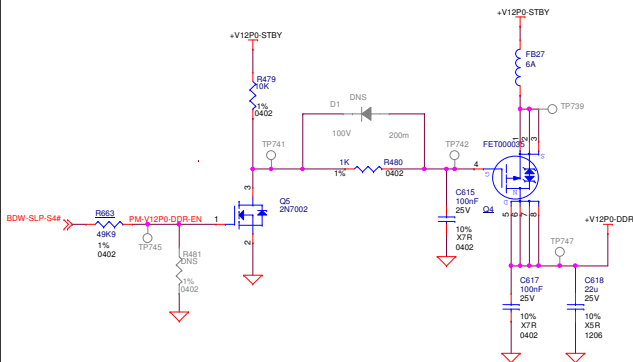
Design Note:

$V_{out} = (R_{top}/R_{bot} + 1) \times 0.8V$
 $\Rightarrow (3.01/4.75 + 1) \times 0.8 = 1.31V$

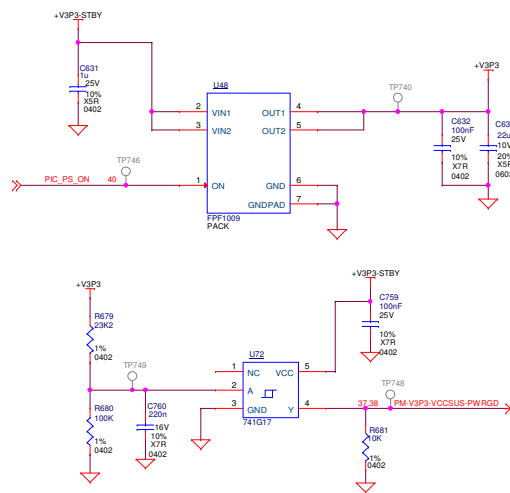
2.5V Linear Regulator for DDR4



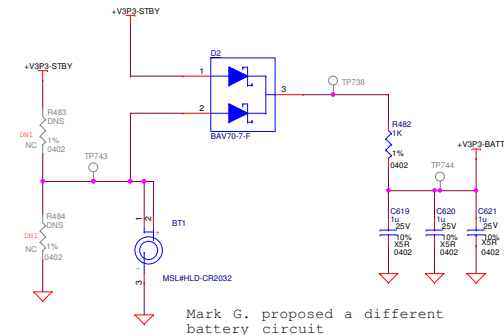
12V DDR Core Load Switch



3.3V Suspend Load Switch



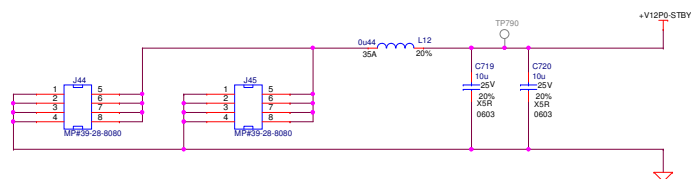
Battery Backup



Mark G. proposed a different battery circuit

DRAWING No. : 80204		Downstream Regulators 0190MG03 Smart AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200		CHECK	NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019			APPROV.				
Wednesday, July 18, 2018			SHEET : 49	of	SHEETS : 50		

Anticipated current:
Nominal: 11A
Max: 23A



The schematic diagram illustrates the power management section for the i.MX8M Mini, showing the connections between the PMIC (PMIC1) and the system power rails. The PMIC is represented by a block with pins labeled with their functions and pin numbers. The power rails are color-coded: red for VPS, blue for VPP, and green for VDD. The diagram includes various capacitors (C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000, C1001, C1002, C1003, C1004, C1005, C1006, C1007, C1008, C1009, C1010, C1011, C1012, C1013, C1014, C1015, C1016, C1017, C1018, C1019, C1020, C1021, C1022, C1023, C1024, C1025, C1026, C1027, C1028, C1029, C1030, C1031, C1032, C1033, C1034, C1035, C1036, C1037, C1038, C1039, C1040, C1041, C1042, C1043, C1044, C1045, C1046, C1047, C1048, C1049, C1050, C1051, C1052, C1053, C1054, C1055, C1056, C1057, C1058, C1059, C1060, C1061, C1062, C1063, C1064, C1065, C1066, C1067, C1068, C1069, C1070, C1071, C1072, C1073, C1074, C1075, C1076, C1077, C1078, C1079, C1080, C1081, C1082, C1083, C1084, C1085, C1086, C1087, C1088, C1089, C1090, C1091, C1092, C1093, C1094, C1095, C1096, C1097, C1098, C1099, C1100, C1101, C1102, C1103, C1104, C1105, C1106, C1107, C1108, C1109, C1110, C1111, C1112, C1113, C1114, C1115, C1116, C1117, C1118, C1119, C1120, C1121, C1122, C1123, C1124, C1125, C1126, C1127, C1128, C1129, C1130, C1131, C1132, C1133, C1134, C1135, C1136, C1137, C1138, C1139, C1140, C1141, C1142, C1143, C1144, C1145, C1146, C1147, C1148, C1149, C1150, C1151, C1152, C1153, C1154, C1155, C1156, C1157, C1158, C1159, C1160, C1161, C1162, C1163, C1164, C1165, C1166, C1167, C1168, C1169, C1170, C1171, C1172, C1173, C1174, C1175, C1176, C1177, C1178, C1179, C1180, C1181, C1182, C1183, C1184, C1185, C1186, C1187, C1188, C1189, C1190, C1191, C1192, C1193, C1194, C1195, C1196, C1197, C1198, C1199, C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209, C1210, C1211, C1212, C1213, C1214, C1215, C1216, C1217, C1218, C1219, C1220, C1221, C1222, C1223, C1224, C1225, C1226, C1227, C1228, C1229, C1230, C1231, C1232, C1233, C1234, C1235, C1236, C1237, C1238, C1239, C1240, C1241, C1242, C1243, C1244, C1245, C1246, C1247, C1248, C1249, C1250, C1251, C1252, C1253, C1254, C1255, C1256, C1257, C1258, C1259, C1260, C1261, C1262, C1263, C1264, C1265, C1266, C1267, C1268, C1269, C1270, C1271, C1272, C1273, C1274, C1275, C1276, C1277, C1278, C1279, C1280, C1281, C1282, C1283, C1284, C1285, C1286, C1287, C1288, C1289, C1290, C1291, C1292, C1293, C1294, C1295, C1296, C1297, C1298, C1299, C1300, C1301, C1302, C1303, C1304, C1305, C1306, C1307, C1308, C1309, C1310, C1311, C1312, C1313, C1314, C1315, C1316, C1317, C1318, C1319, C1320, C1321, C1322, C1323, C1324, C1325, C1326, C1327, C1328, C1329, C1330, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, C1341, C1342, C1343, C1344, C1345, C1346, C1347, C1348, C1349, C1350, C1351, C1352, C1353, C1354, C1355, C1356, C1357, C1358, C1359, C1360, C1361, C1362, C1363, C1364, C1365, C1366, C1367, C1368, C1369, C1370, C1371, C1372, C1373, C1374, C1375, C1376, C1377, C1378, C1379, C1380, C1381, C1382, C1383, C1384, C1385, C1386, C1387, C1388, C1389, C1390, C1391, C1392, C1393, C1394, C1395, C1396, C1397, C1398, C1399, C1400, C1401, C1402, C1403, C1404, C1405, C1406, C1407, C1408, C1409, C1410, C1411, C1412, C1413, C1414, C1415, C1416, C1417, C1418, C1419, C1420, C1421, C1422, C1423, C1424, C1425, C1426, C1427, C1428, C1429,

The schematic diagram illustrates the PM-VIP7-PWRGR circuit. It is powered by +V5P3_STBY and +V3P3_STBY. The circuit includes a PM-VIP7-PWRGR IC (U49) with pins 11 (PVIN), 12 (PUNC), 13 (AVIN), 14 (VOS), 15 (PG), 16 (FB), 17 (FSD), and 18 (DEF). The circuit includes a feedback network with resistors R500, R501, R502, and R503, and capacitors C636, C637, C638, C639, C640, and C641. A switch SW1 is connected to pin 12. The output is +V1P7, which is also connected to a +V1P7_FSW signal. The circuit is tested with a PM-VIP7-PWRGR test fixture.

i **Design Note:**
 $V_{out} = (R_{top}/R_{bot}+1)*0.8V$
 $\Rightarrow (93.1/82.5+1)*0.8 = 1.70V$

DRAWING No. : 60204	
SIZE : Custom	REV No. : R200
DATE : Sunday, April 07, 2019 Wednesday, July 18, 2018	

**Power Entry /
Downstream Regulators**

0190GG3 Small

AT&T Compute Board

APPROVALS		
NAME	SIGN	DATE
CHECK		
APPROV.		
SHEET : 50 of SHEETS : 50		

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