

AT&T - Medium/Small - IO Board

80200-0186-G00, Rev: R100

DRAWING No. :		80200-0186-G00	APPROVALS			SILICOM Ltd. Conectivity Solutions A Member of RAD Group	
SIZE : A4	REV No. : R100			NAME	SIGN		DATE
DATE : Sunday, December 16, 2018			CHECK	Nadav Y.	Nadav Y.		
DATE : Wednesday, March 21, 2012			APPROV.	David C.	David C.		
			SHEET : 1 of SHEETS : 49				

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SIZE : A4	REV No. : R100		CHECK	NAME	SIGN		DATE
DATE : Sunday, December 16, 2018			APPROV.	Nadav Y.	Nadav Y.		
Wednesday, December 28, 2011				David C.	David C.		
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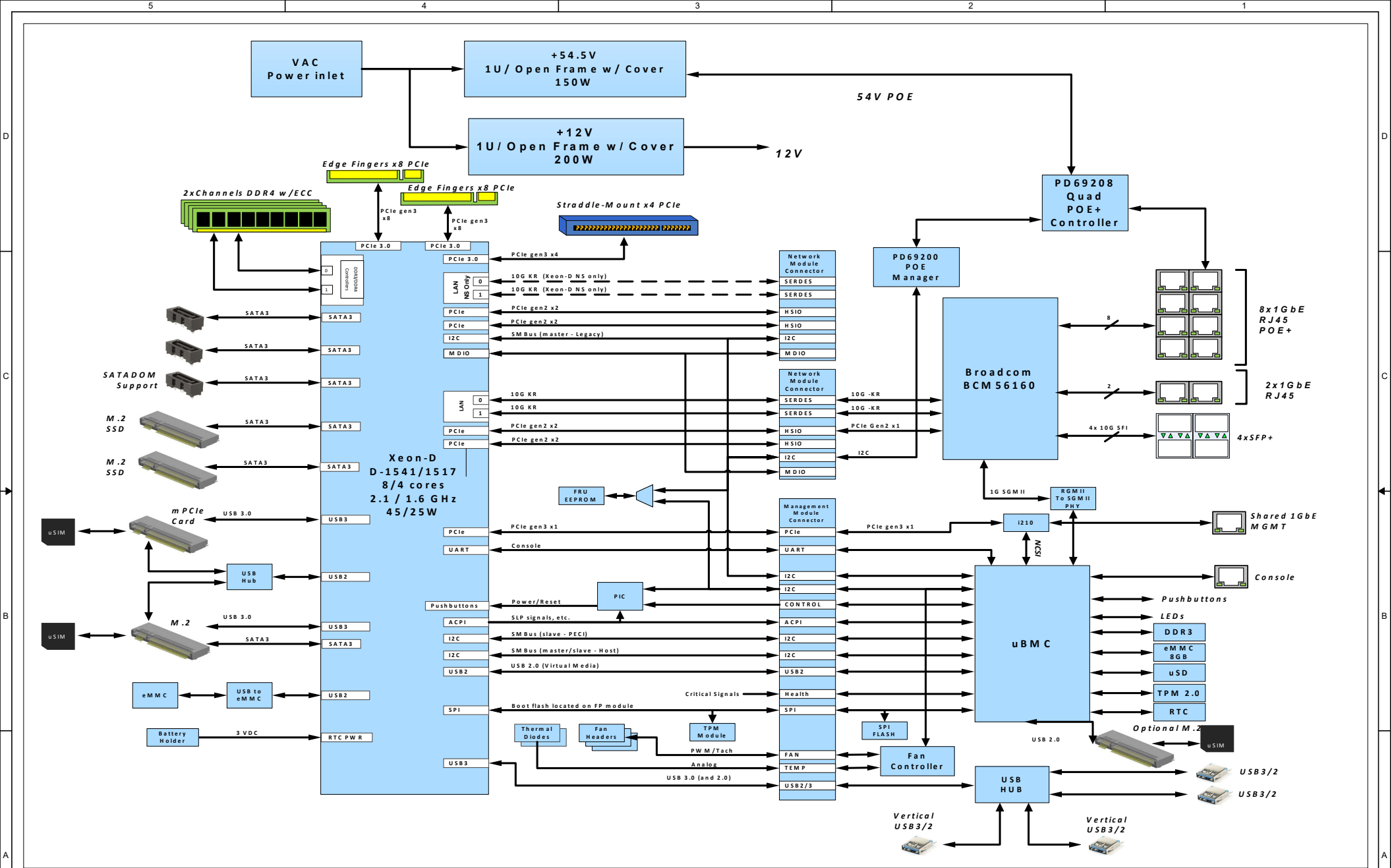
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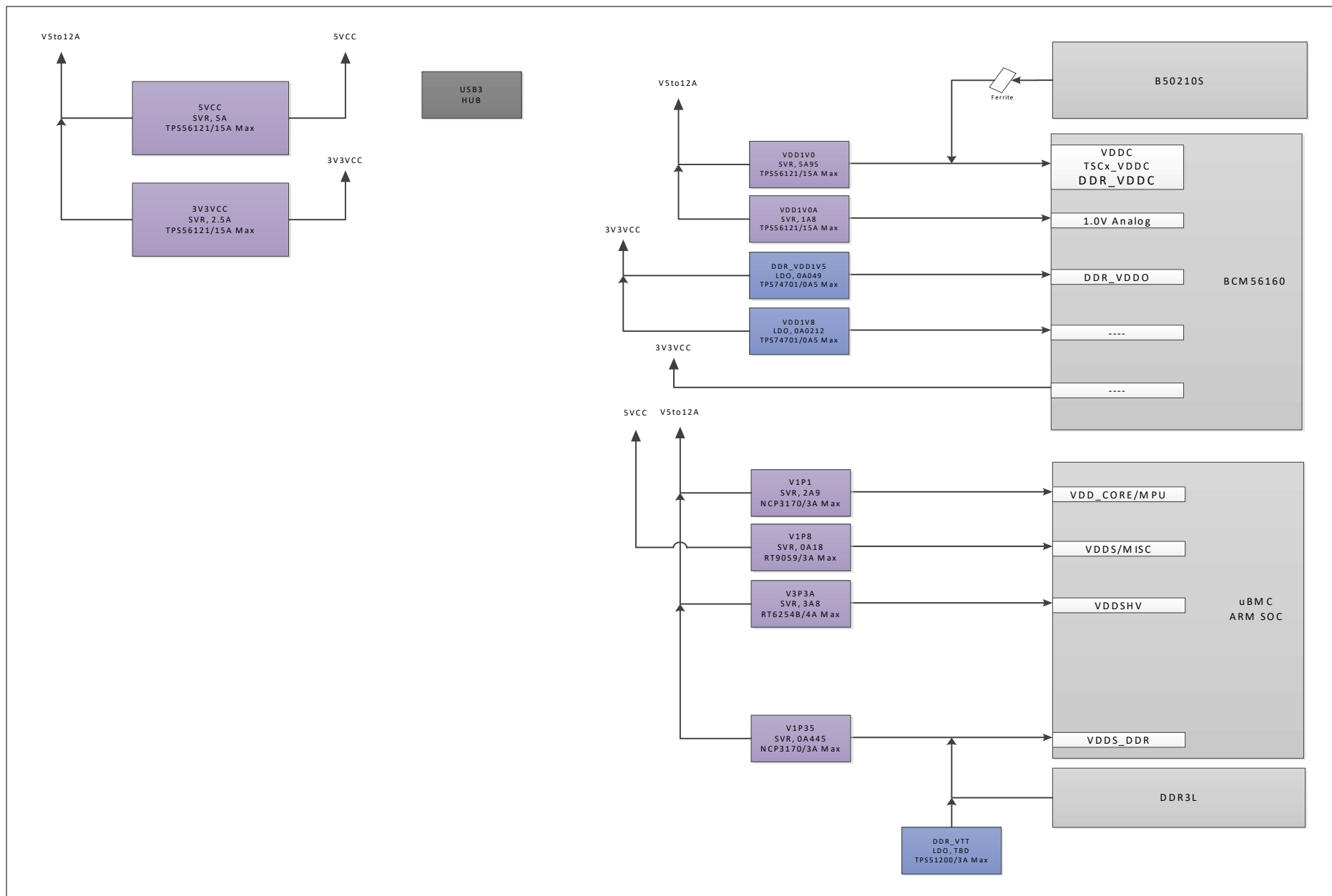
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Sunday, May 06, 2018			APPROV.	David C.	David C.	
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DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Conectivity Solutions A Member of RAD Group
SIZE : A4	REV No. : R100		CHECK	NAME	SIGN	DATE	
DATE : Sunday, December 16, 2018 Wednesday, December 28, 2011			APPROV.	Nadav Y.	Nadav Y.		
				David C.	David C.		
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		Block Diagram					



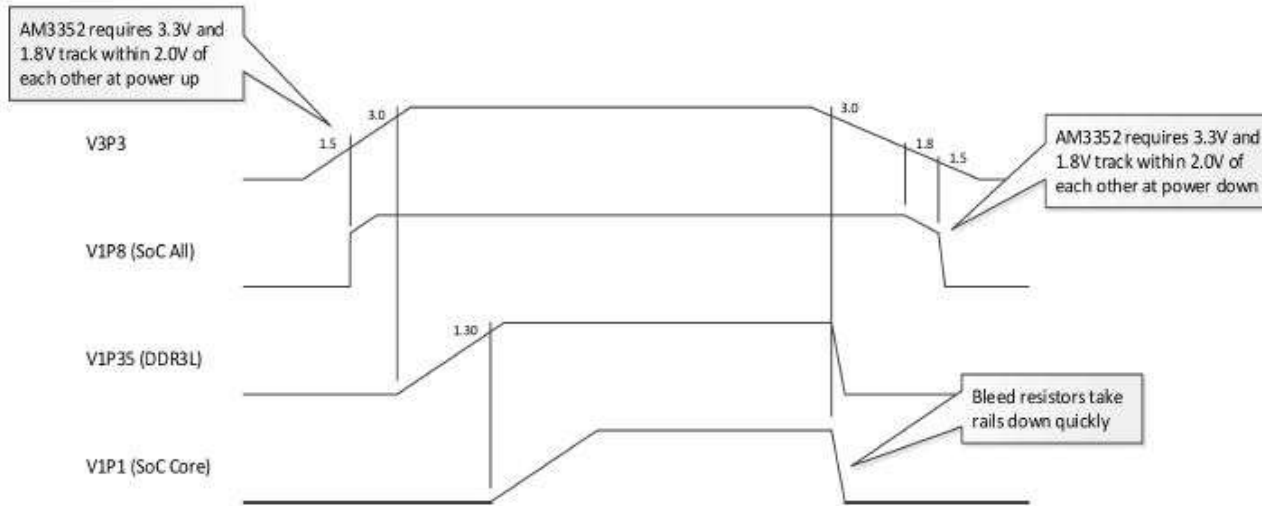
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SIZE : A4	REV No. : R100
DATE : Sunday, December 16, 2018 Sunday, May 06, 2018	

80200-0186-G00	
Power Block Diagram	

APPROVALS			
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APPROV.	David C.	David C.	
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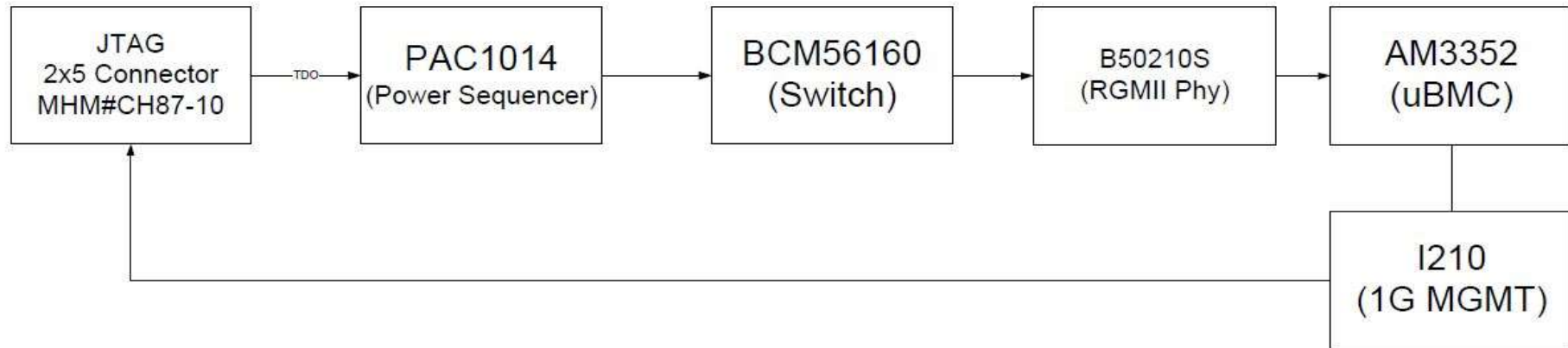
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SoC-Specific Power Sequence



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SIZE : A4	REV No. : R100		CHECK	NAME	SIGN		DATE
DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018			Power Sequence	Nadav Y.	Nadav Y.		
			APPROV.	David C.	David C.		
			SHEET : 7 of SHEETS : 49				

JTAG Block Diagram



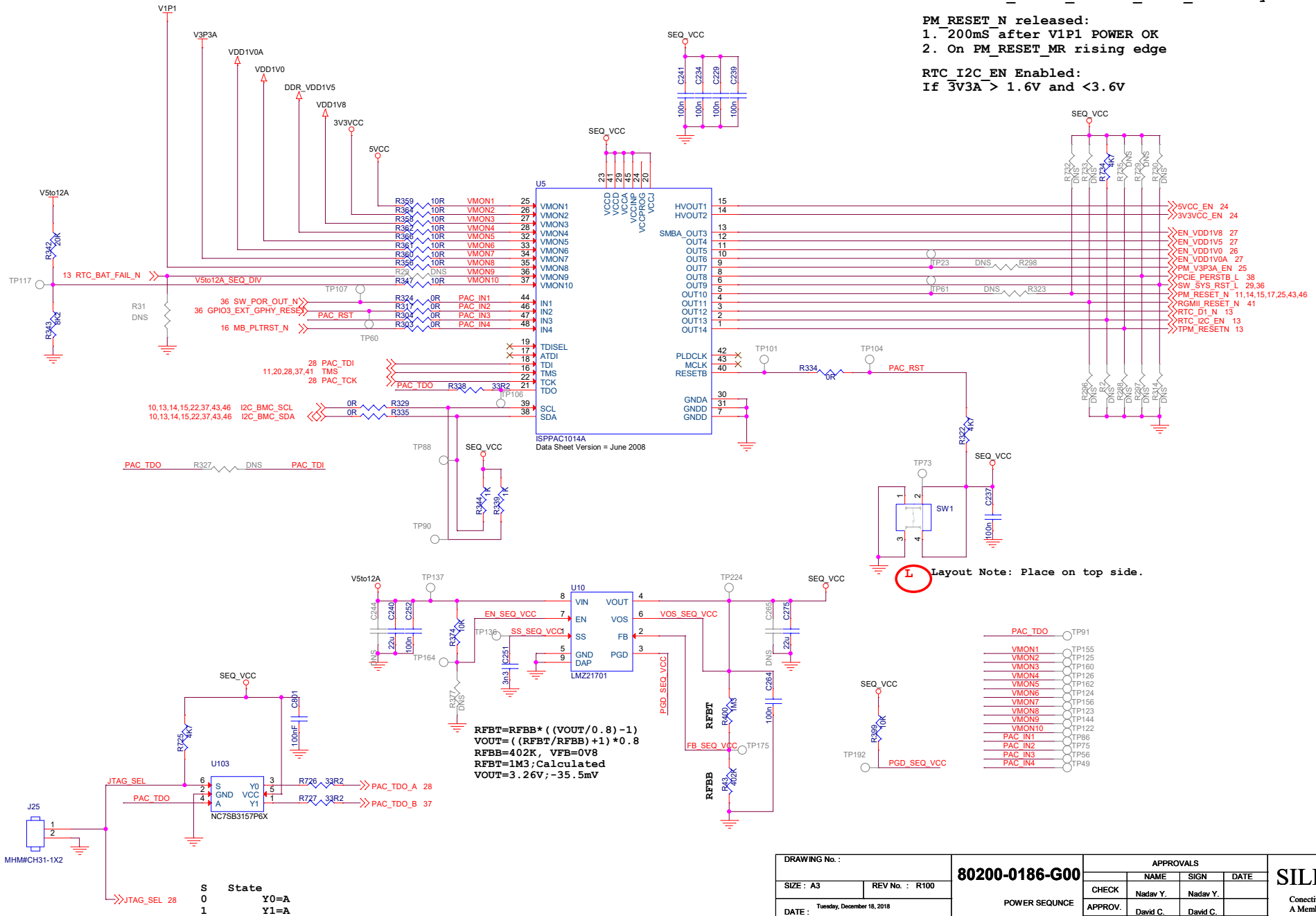
Notes:

1. each TDO/TDI has a short

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DATE : Sunday, December 16, 2018			JTAG Block Diagram		APPROV.	Nadav Y.		Nadav Y.	
Wednesday, May 23, 2018						David C.		David C.	
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POWER SEQUENCE

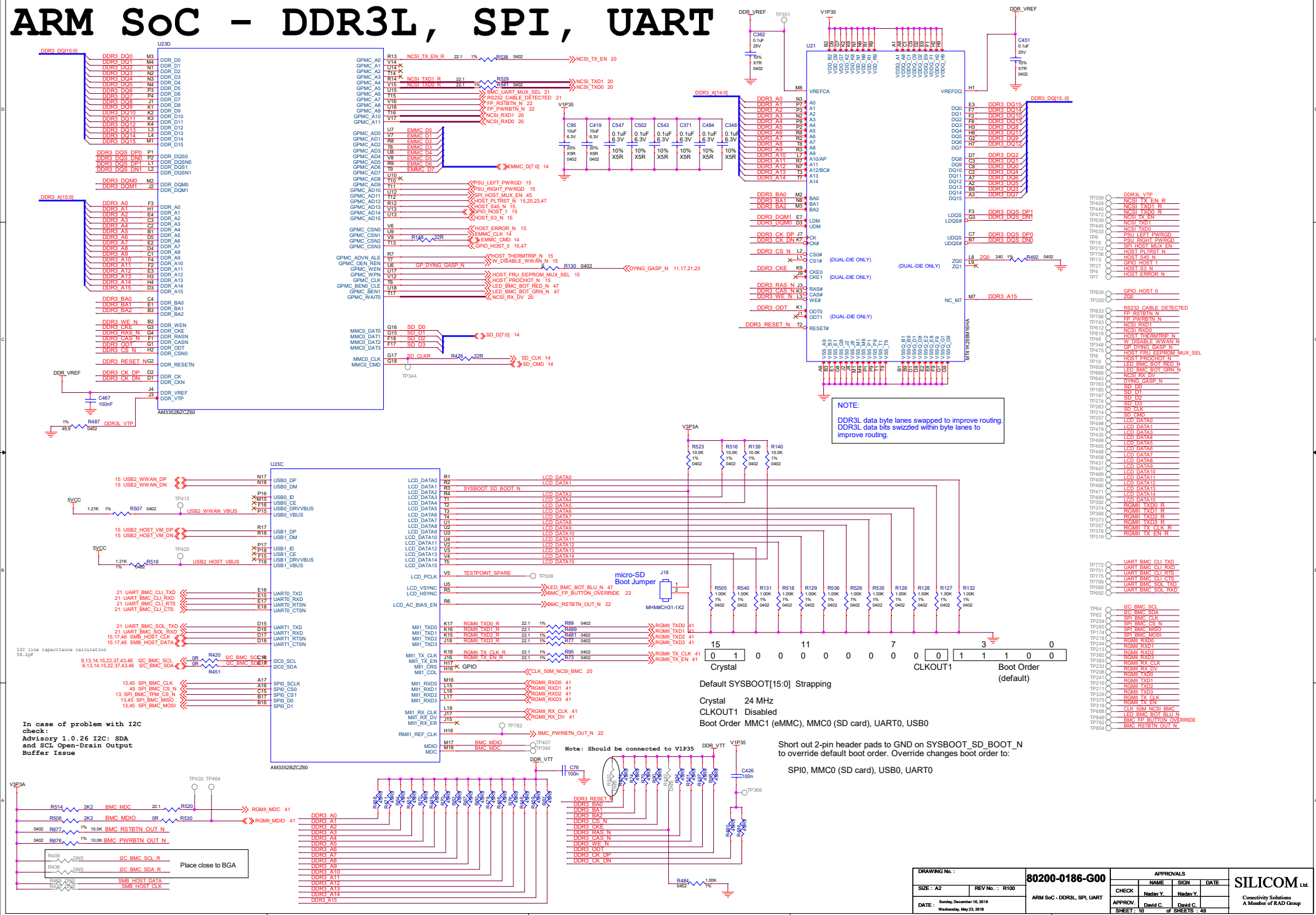
- PCIE PERSTB L released:
1. 50mS after SW RESET N is up
 2. With MB_PLTRST_N if SW_RESET_N already released
- PM_RESET_N released:
1. 200mS after V1P1 POWER OK
 2. On PM_RESET_MR rising edge
- RTC I2C EN Enabled:
- If 3V3A > 1.6V and <3.6V



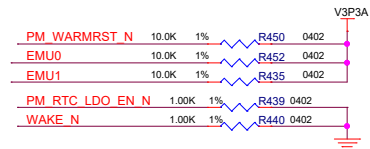
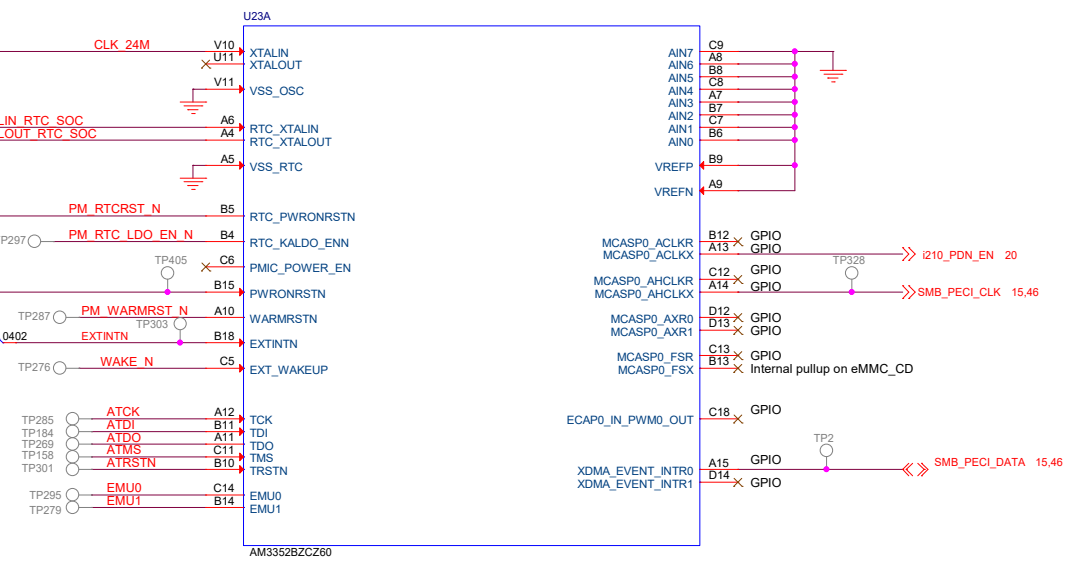
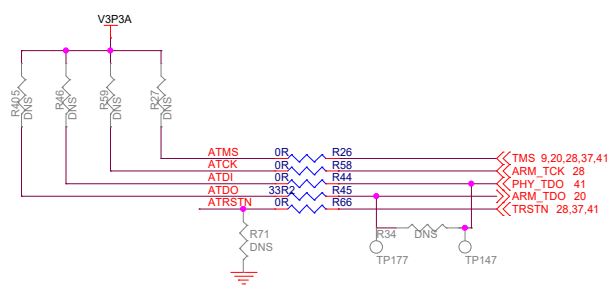
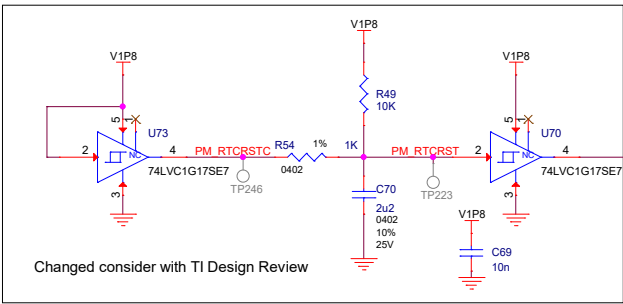
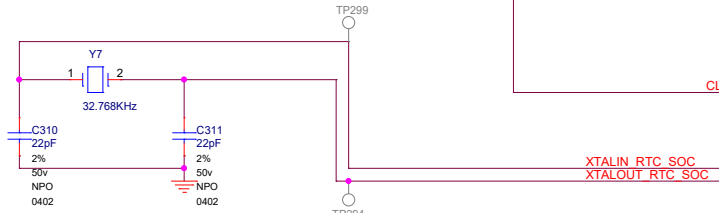
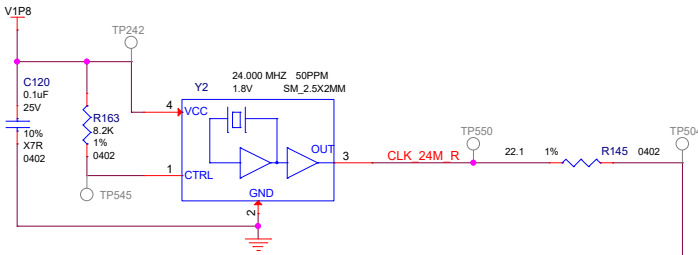
L Layout Note: Place on top side.

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Sunday, May 06, 2018			SHEET : 9			of SHEETS : 49

ARM SoC - DDR3L, SPI, UART



ARM SoC - Clocks, ADC, JTAG



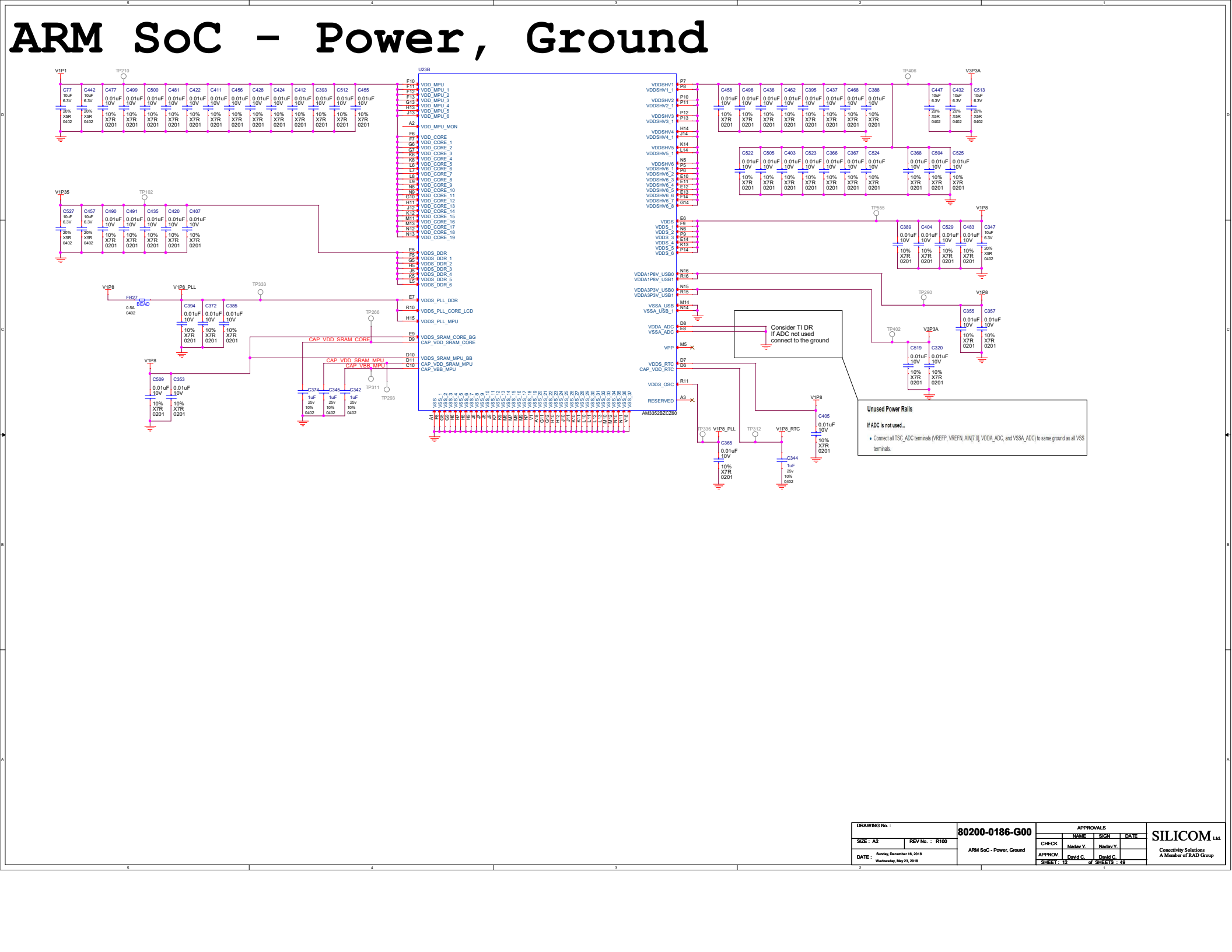
DRAWING No. :		80200-0186-G00 ARM SoC - Clocks, ADC, JTAG	APPROVALS				 Concivity Solutions A Member of RAD Group
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DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018			SHEET : 11 of SHEETS : 49				

ARM SoC - Power, Ground

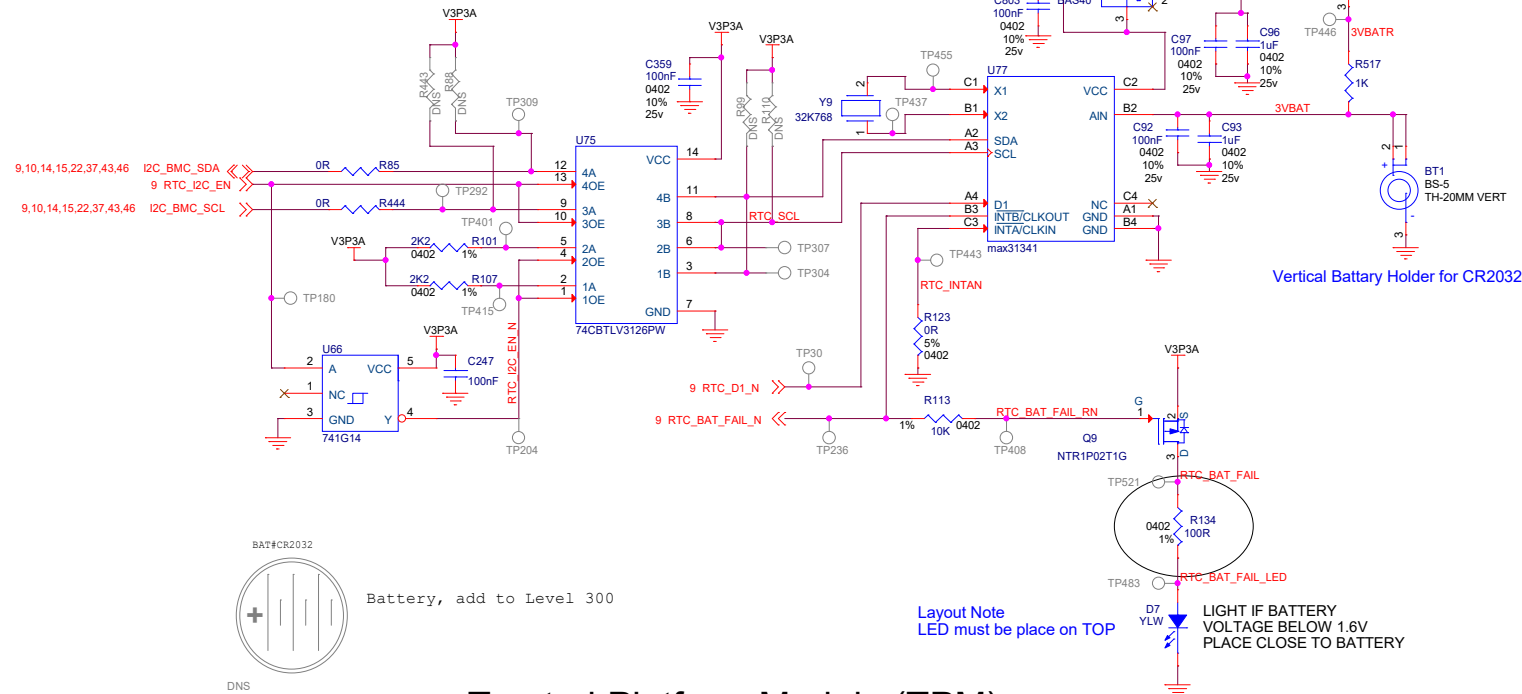
ARM SoC - Power, Ground

U238

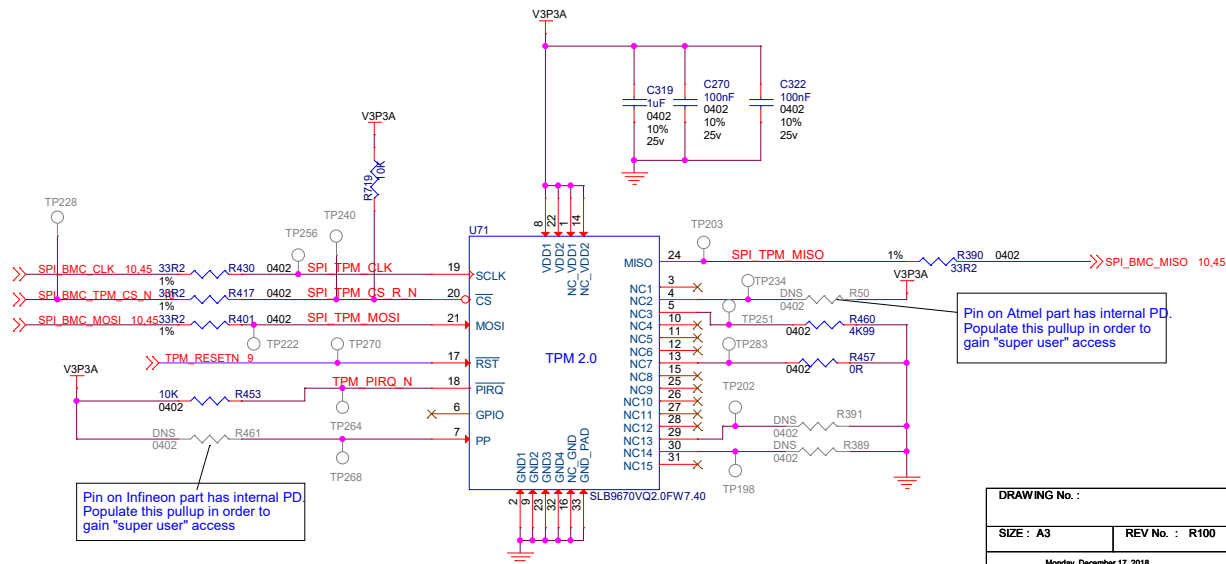
F10 VDD_MPU_1
F11 VDD_MPU_2
F12 VDD_MPU_3
F13 VDD_MPU_4
F14 VDD_MPU_5
F15 VDD_MPU_6
A2 VDD_MPU_MON
F6 VDD_CORE_1
F7 VDD_CORE_2
F8 VDD_CORE_3
F9 VDD_CORE_4
F10 VDD_CORE_5
F11 VDD_CORE_6
F12 VDD_CORE_7
F13 VDD_CORE_8
F14 VDD_CORE_9
F15 VDD_CORE_10
F16 VDD_CORE_11
F17 VDD_CORE_12
F18 VDD_CORE_13
F19 VDD_CORE_14
F20 VDD_CORE_15
F21 VDD_CORE_16
F22 VDD_CORE_17
F23 VDD_CORE_18
F24 VDD_CORE_19
E5 VDDA1PRV_USB8
E6 VDDA1PRV_USB8
E7 VDDA1PRV_USB8
E8 VDDA1PRV_USB8
E9 VDDA1PRV_USB8
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RTC

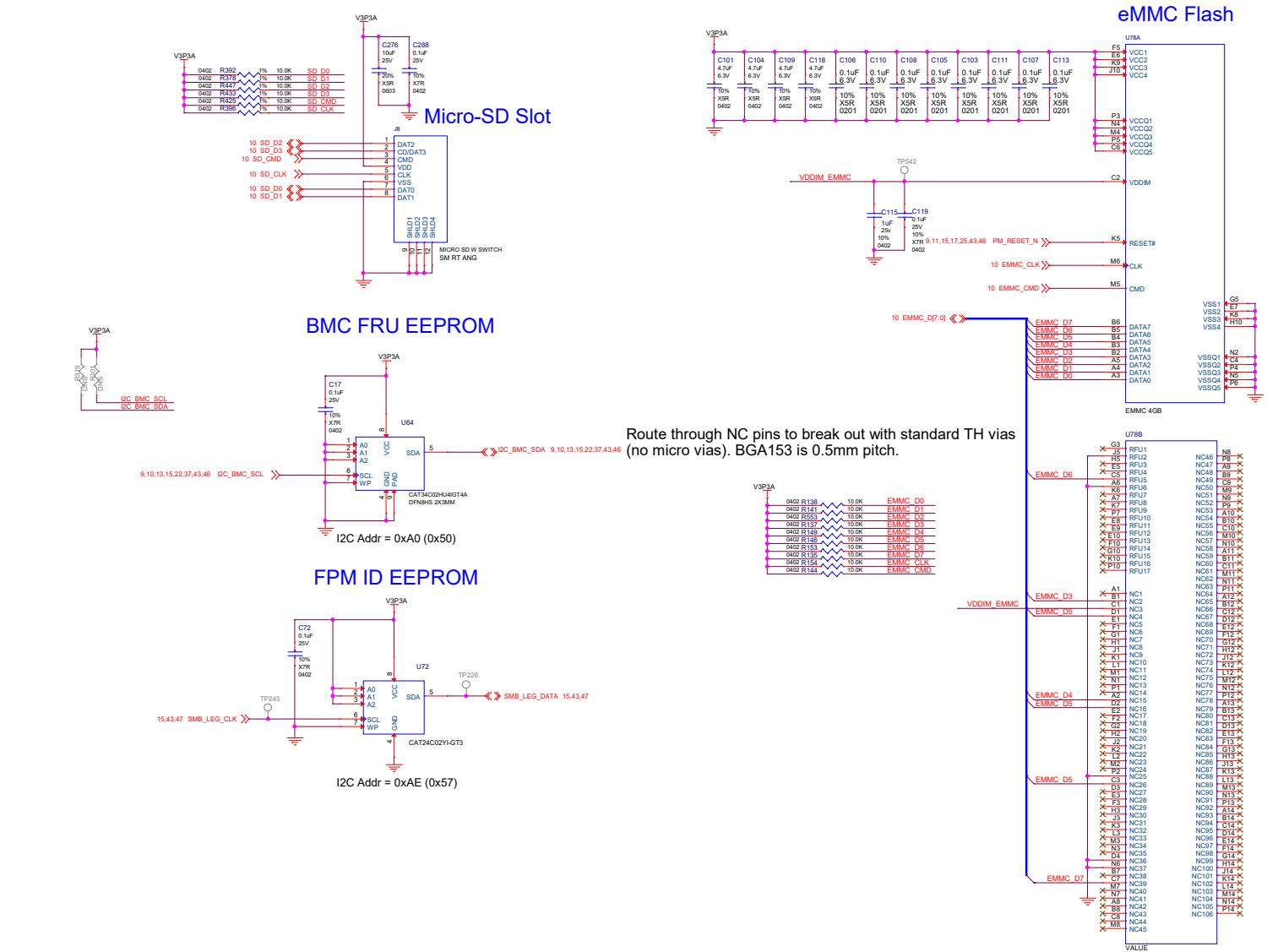


Trusted Platform Module (TPM)



DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Conectivity Solutions A Member of RAD Group
SIZE : A3	REV No. : R100			NAME	SIGN	DATE	
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			APPROV.	David C.	David C.		
		SHEET : 13 of SHEETS : 49					

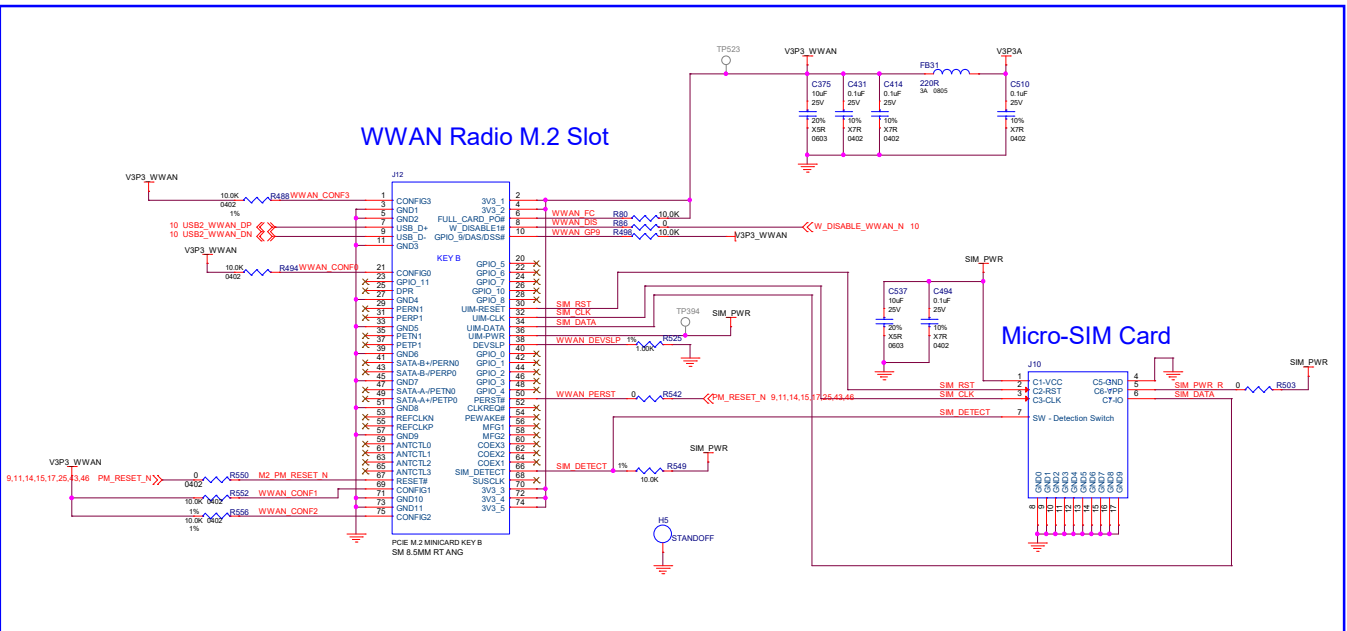
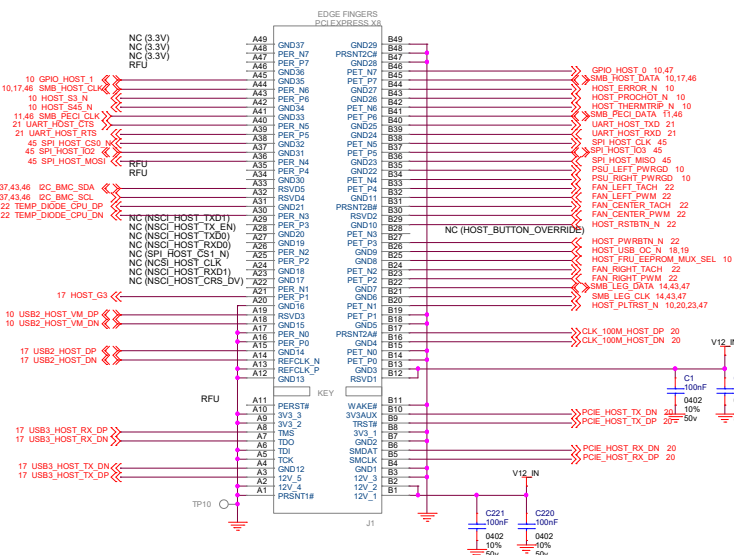
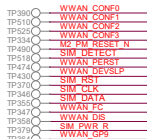
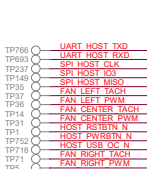
EEPROMs, micro-SD, eMMC



Route through NC pins to break out with standard TH vias (no micro vias). BGA153 is 0.5mm pitch.

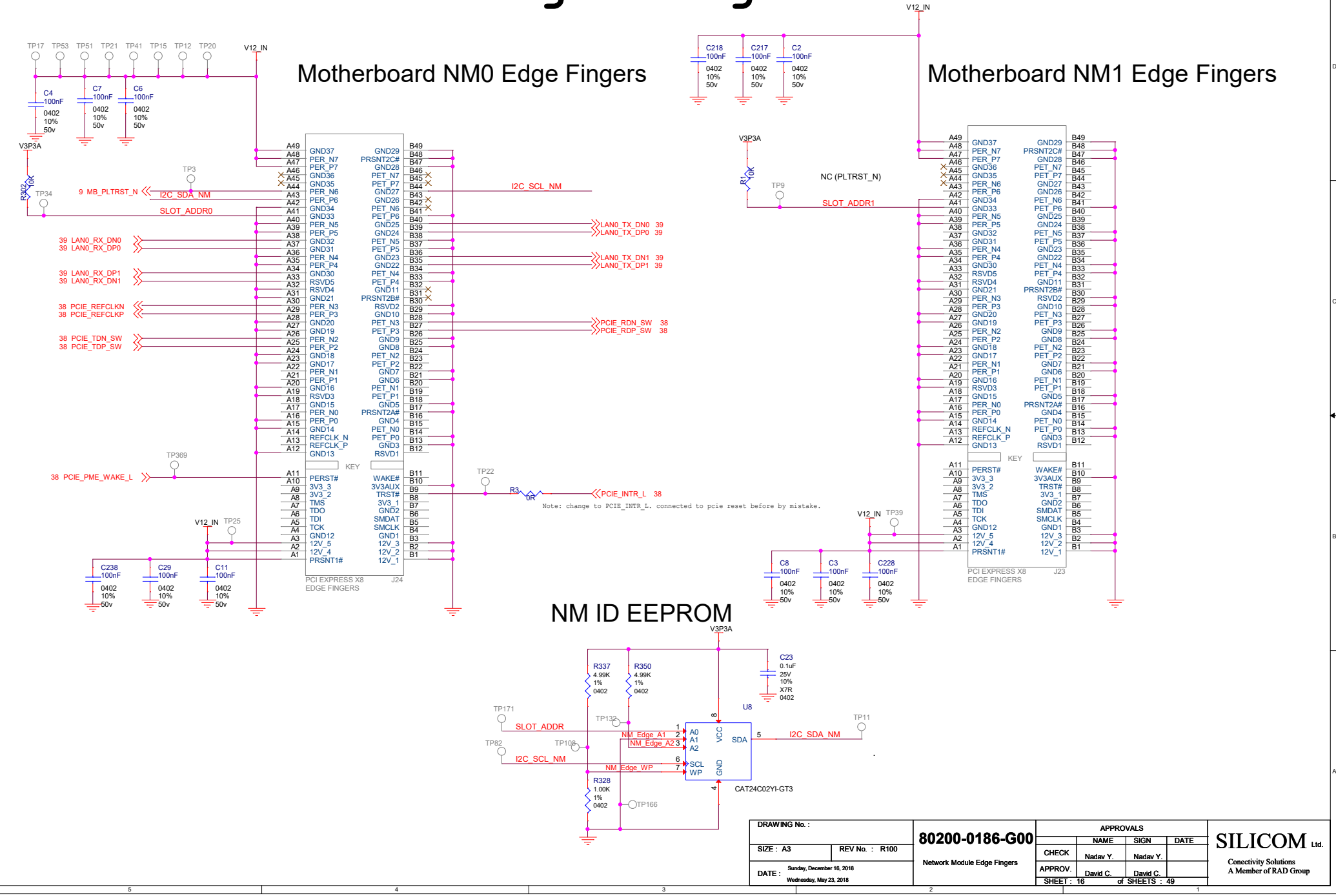
DRAWING No. :		80200-0186-G00		APPROVALS		SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A2	REV No. : R100	EEPROMs, uSD, eMMC		CHECK	NAME	
DATE : Sunday, December 16, 2018				APPROV.	David C.	
Wednesday, May 23, 2018				SHEET : 14	of SHEETS : 49	

Motherboard FPM Connector and WWAN

TP531 **HOST G3**

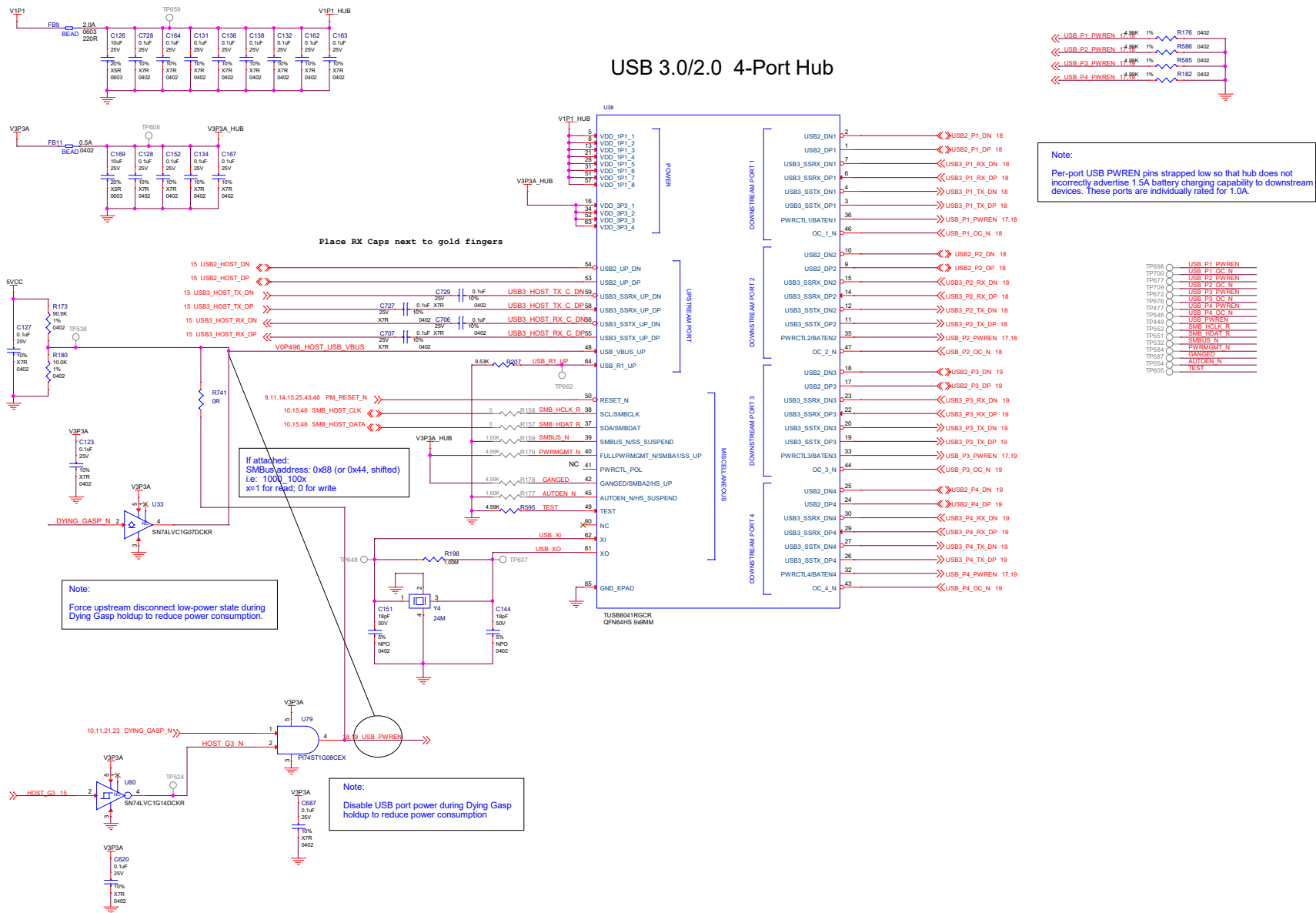
DRAWING NO. :		80200-0186-C00 MIS FPM Conn. & WWAN	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of EAD Group
SIZE : A2	REV NO. : R100		CHECK	Naday Y.	Naday Y.	
DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018			APPROV. :	David C.	David C.	
			SHEET : 15	OF : 49		

Network Module Edge Fingers



DRAWING No. :		80200-0186-G00 Network Module Edge Fingers	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A3	REV No. : R100		NAME	SIGN	DATE	
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			APPROV.	David C.	David C.	
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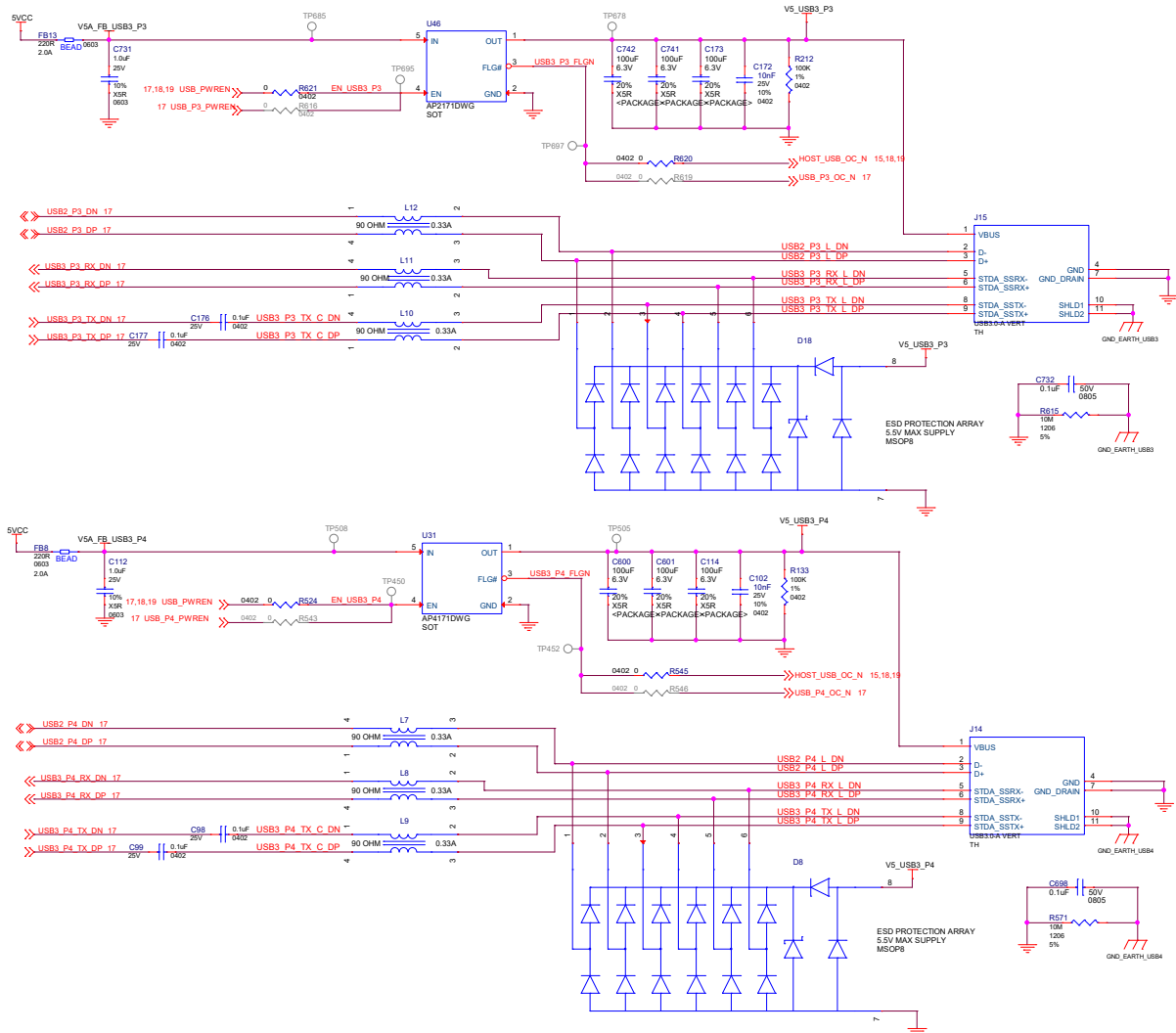
USB 3.0/2.0 4-Port Hub



DRAWING No. :		80200-0186-G00 USB 3.0/2.0 4-Port Hub	APPROVALS			 Connectivity Solutions A Member of RAD Group
SIZE : A2	REV No. : R100		CHECK	Nadav Y.	Nadav Y.	
DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018			APPROV.	David C.	David C.	
			SHEET : 17	of SHEETS : 49		

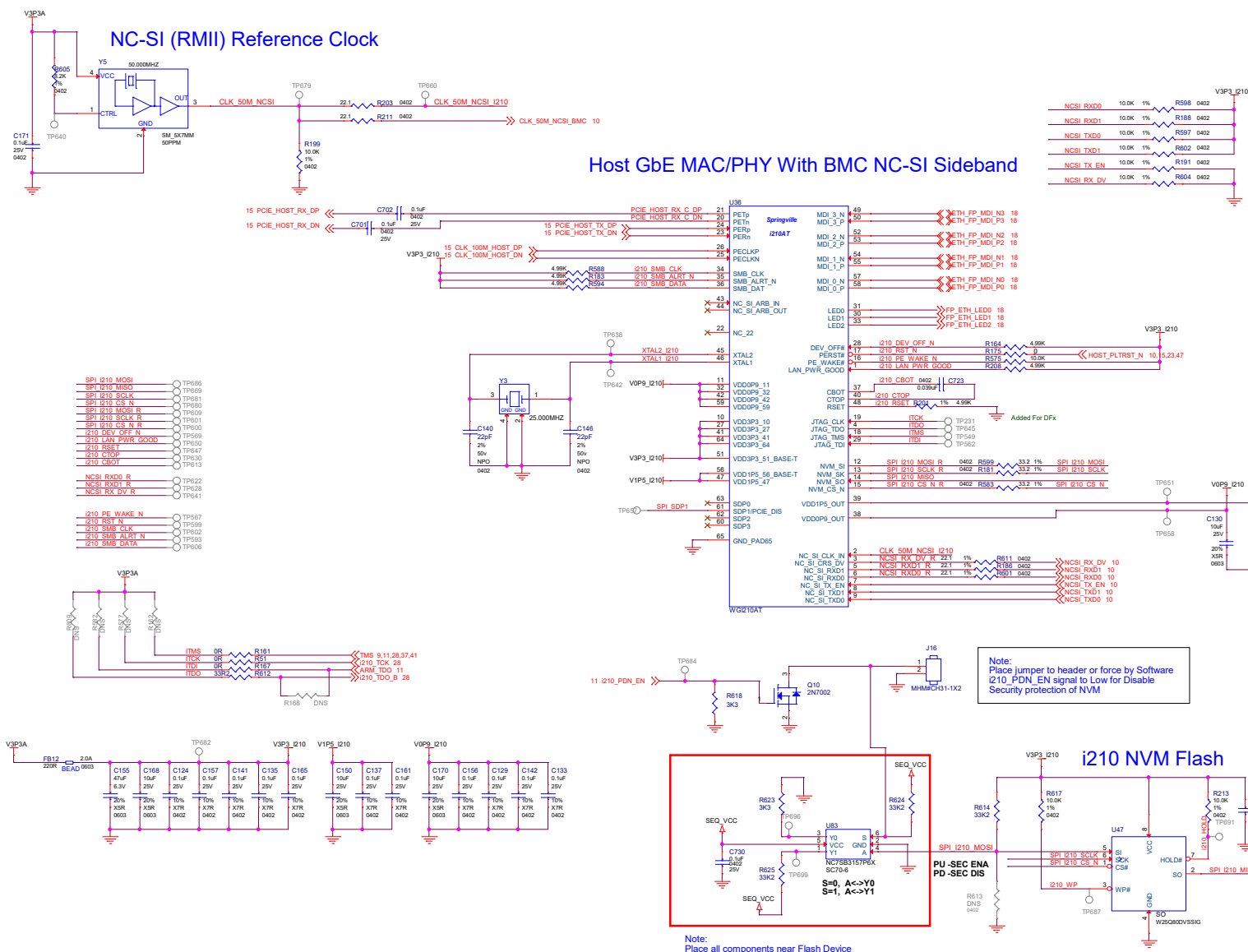
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DATE : Sunday, December 18, 2018				Nadav Y.	Nadav Y.		
Wednesday, May 23, 2018			USB 3.0/2.0 and GbE FP Ports	APPROV.	David C.		David C.
			SHEET : 1	SHEET : 1			

USB 3.0/2.0 Back Panel Ports



DRAWING No. :		80200-0186-G00 USB 3.0/2.0 Back Panel Ports	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A2			CHECK	NAME	SIGN	DATE	
REV No. : R100				Nadav Y.	Nadav Y.		
DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018				APPROV. David C.	David C.		
			SHEET : 19	OF SHEETS : 49			

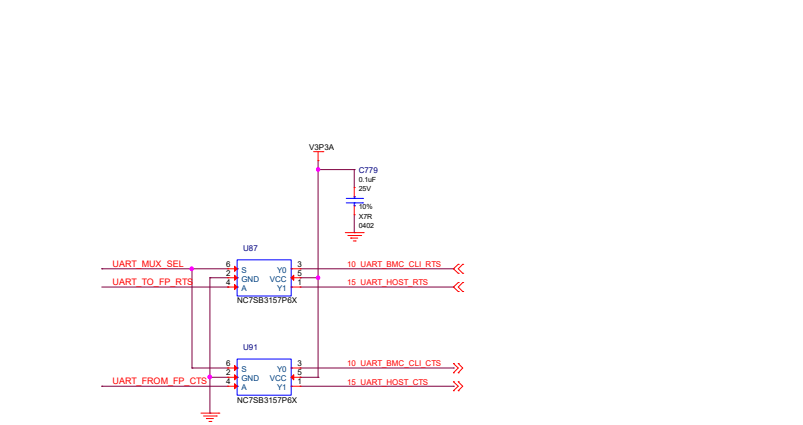
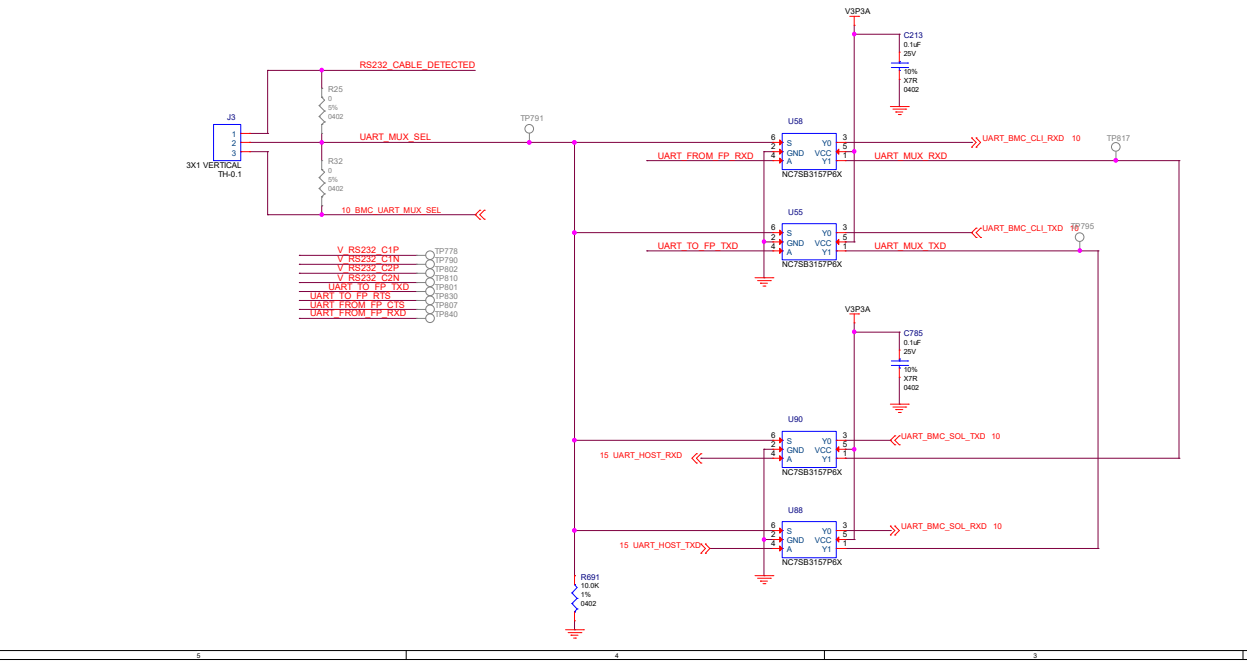
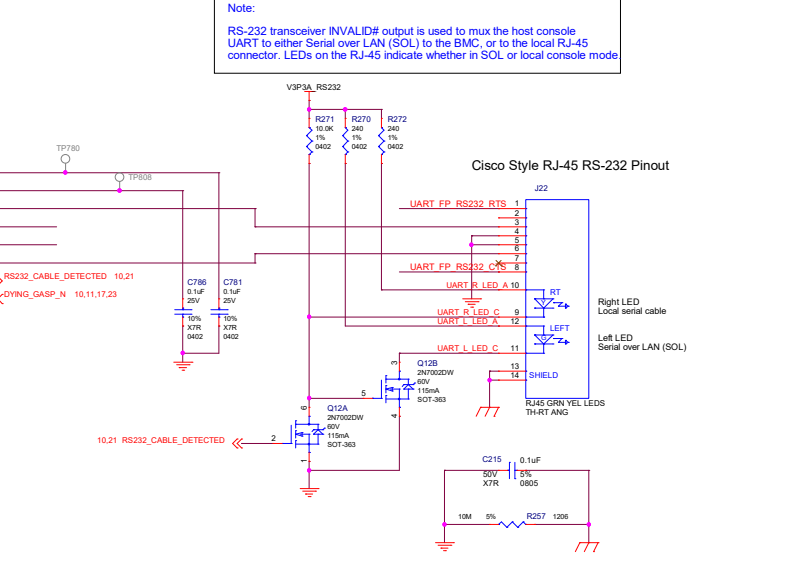
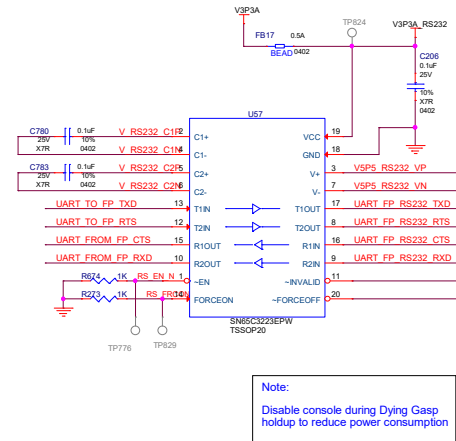
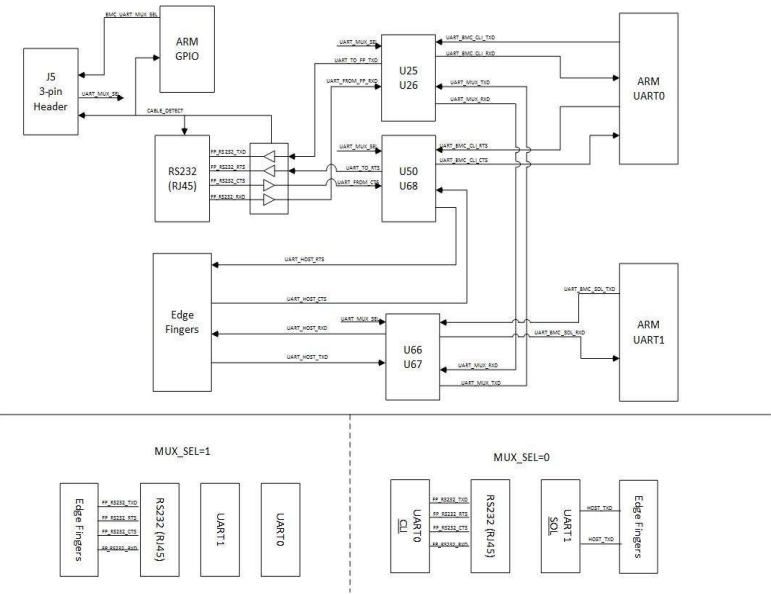
Host GbE MAC/PHY With BMC NC-SI Sideband



DRAWING No. :		80200-0186-G00 1GSE MAC/PHY With BMC NC-SI	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAP Group		
SIZE : A2			REV No. : R100		CHECK	NAME		SIGN	DATE
DATE : Sunday, December 16, 2018			David Y. Nadav Y.						
DATE : Wednesday, May 23, 2018			APPROV. Nadav C. David C.						

CPU Console, BMC Console

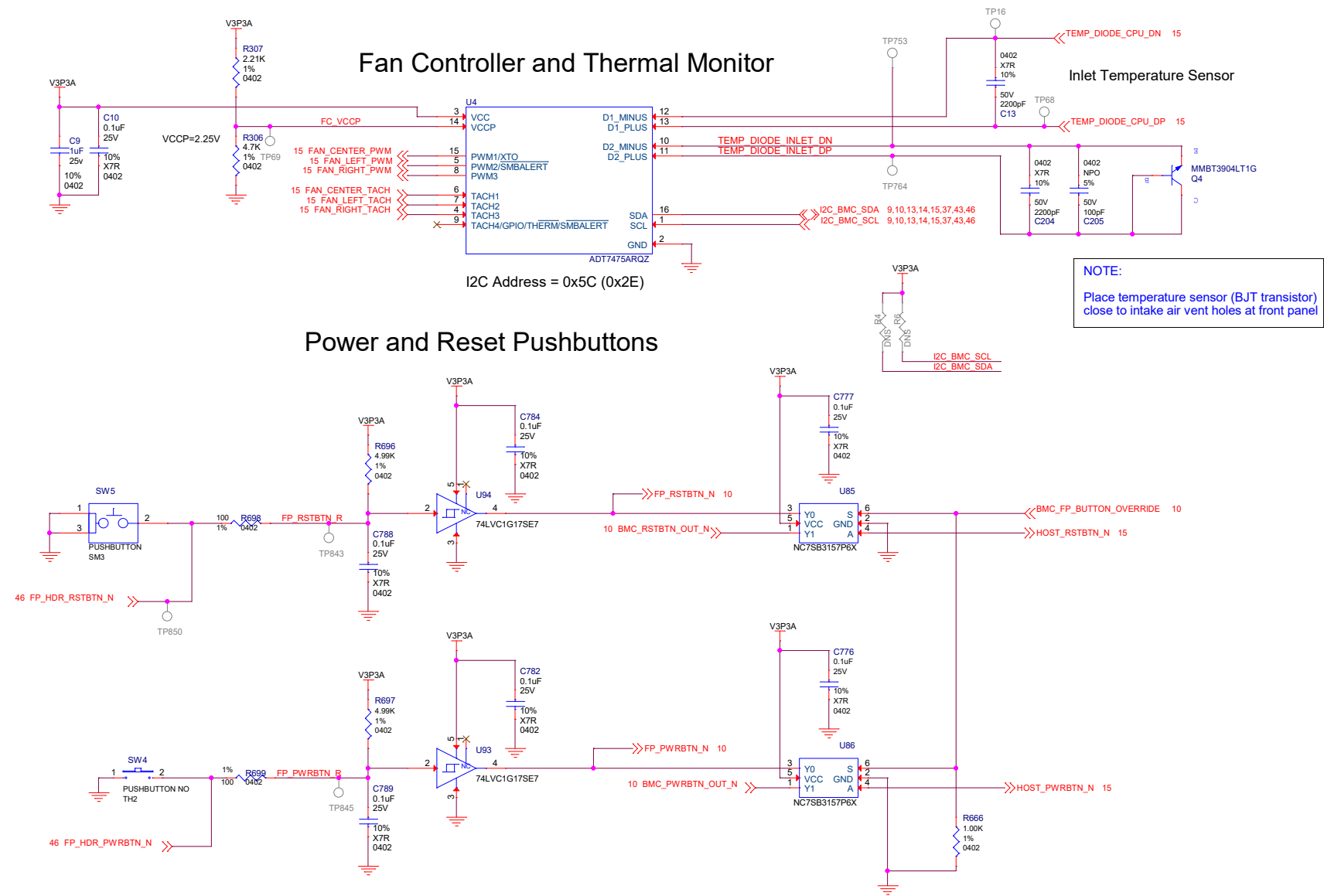
Host Console Port



CPU Console, BMC Console

DRAWING No. :		80200-0186-G00	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A2			REV No. : R100		CPU Console, BMC Console	
DATE : Sunday, December 16, 2018			CHECK	Nadav Y.		
DATE : Wednesday, May 23, 2018			APPROV.	David C.	David C.	
		SHEET : 21 of SHEETS : 49				

Fan Controller/Thermal Monitor, Buttons

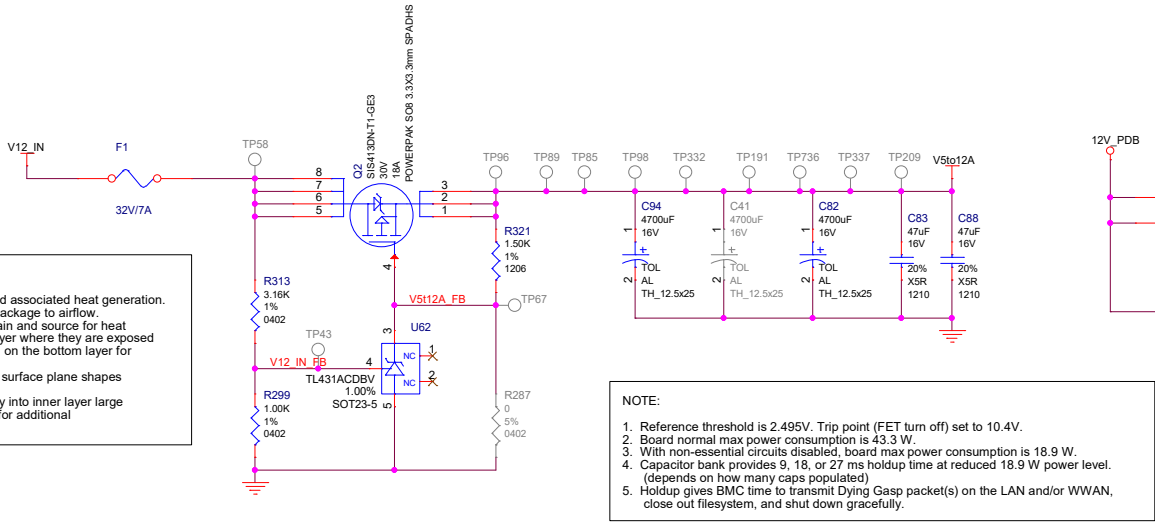


DRAWING No. :		80200-0186-000		APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A3	REV No. : R100	Fan Controller and Thermal Monitor		CHECK	NAME	SIGN	DATE
DATE : Sunday, December 16, 2018				APPROV.	David Y.	Nadav Y.	
Wednesday, May 23, 2018					David C.	David C.	
				SHEET : 22 of SHEETS : 49			

Power Input, Dying Gasp Holdup

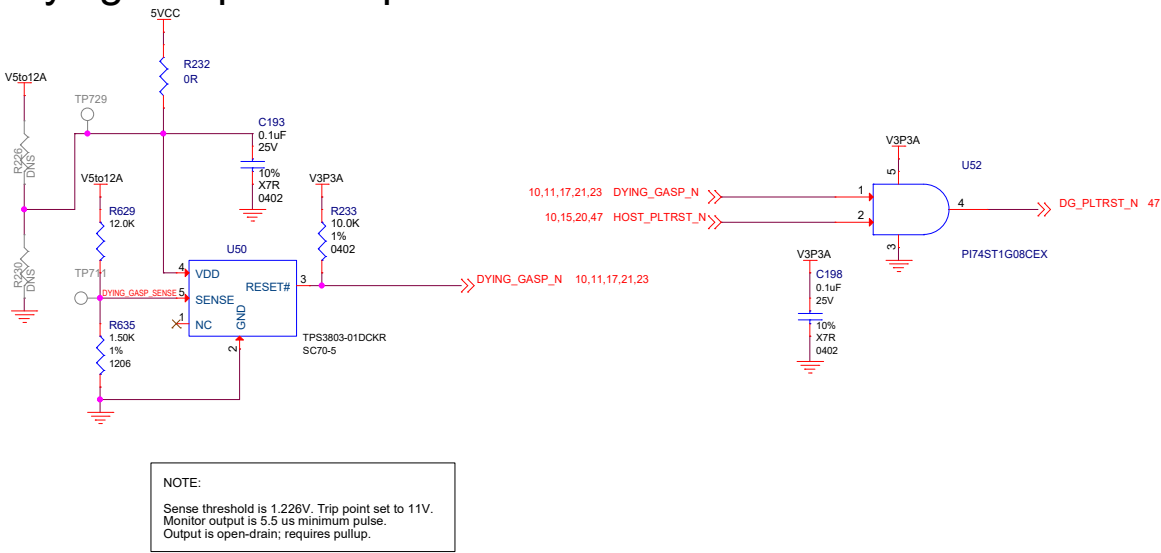
Power Input

- LAYOUT NOTE:
- 1. FET R_{ds(on)} will cause extra loss and associated heat generation.
 - 2. Place FET on top layer to expose package to airflow.
 - 3. Use large plane shapes for FET drain and source for heat dissipation, especially on the top layer where they are exposed to airflow and preferably duplicated on the bottom layer for additional exposure.
 - 4. Bury FET drain and source pads in surface plane shapes (do not use thermal relief spokes).
 - 5. Tie outer layer plane shapes heavily into inner layer large plane shapes with large via arrays for additional heatsinking capability.



- NOTE:
- 1. Reference threshold is 2.495V. Trip point (FET turn off) set to 10.4V.
 - 2. Board normal max power consumption is 43.3 W.
 - 3. With non-essential circuits disabled, board max power consumption is 18.9 W.
 - 4. Capacitor bank provides 9, 18, or 27 ms holdup time at reduced 18.9 W power level. (depends on how many caps populated)
 - 5. Holdup gives BMC time to transmit Dying Gasp packet(s) on the LAN and/or WWAN, close out filesystem, and shut down gracefully.

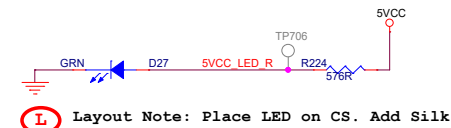
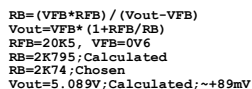
Dying Gasp Interrupt Monitor



- NOTE:
- Sense threshold is 1.226V. Trip point set to 11V.
 - Monitor output is 5.5 us minimum pulse.
 - Output is open-drain, requires pullup.

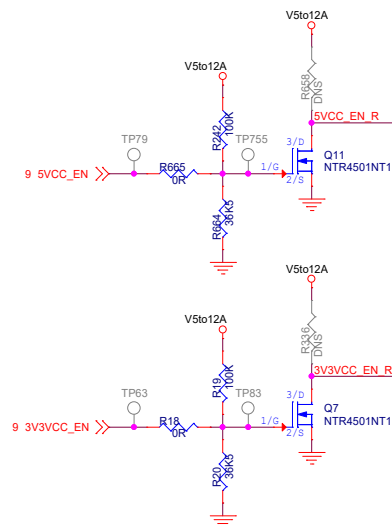
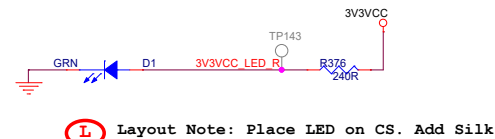
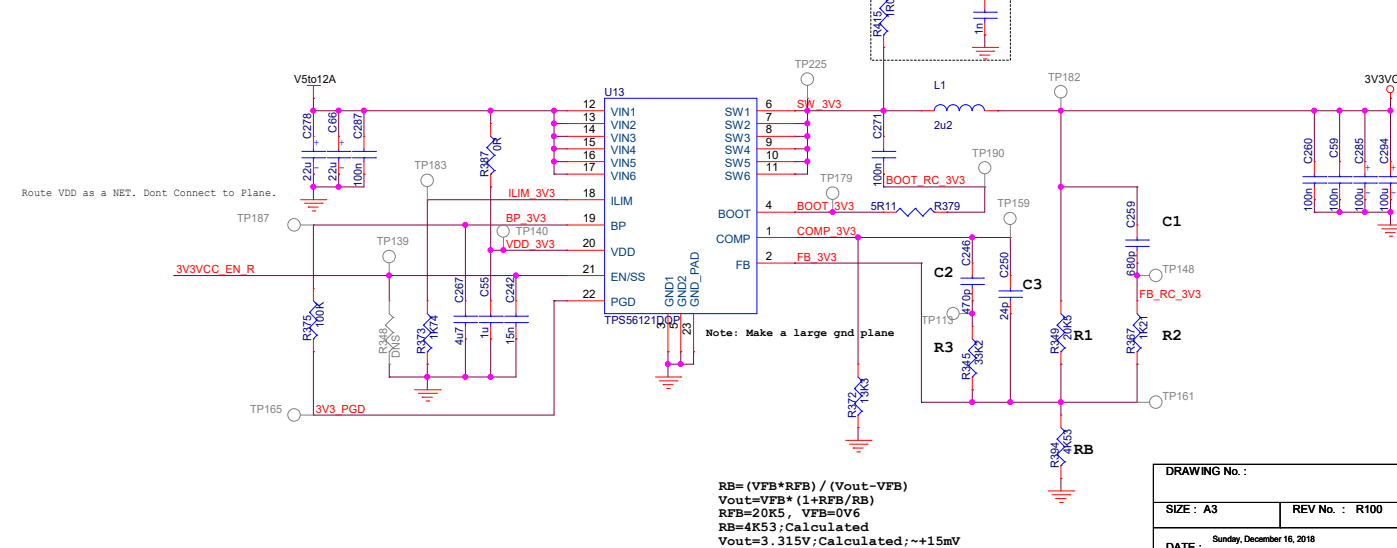
DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group					
SIZE : A3			REV No. : R100									
DATE : Sunday, December 16, 2018		Power: Input, Dying Gasp Holdup		CHECK		NAME		SIGN		DATE		
Wednesday, May 23, 2018				APPROV.		Nadav Y.		Nadav Y.				
				SHEET : 23		David C.		David C.		of SHEETS : 49		

$I_{max}=15A$; $F_{switch}=950kHz$, $E_{eff}=0.9$, $I_{out}=5A$, $P_{out}=25W$,
V5to12A



```
Devices:
ARM:AM3352 ; Current - Not Clear
USB3HUB ; Current - 778mA - Note: 3.0 host / 4 SS Devices and Hub in U0
4x USB Ports; Current - 4x1A = 4MAx
Dying Gasp Monitor ; Current - 5uA
VIP8 PS; Current - 180mA
Status LED - 5mA
FP LED (3x3); Current - 9x5mA = 45mA
```

Total Current - 5A Max


$$I_{\max}=15\text{A}; F_{\text{switch}}=950\text{kHz}, \text{Eff}=0.9, I_{\text{out}}=6\text{A}, P_{\text{out}}=19.8\text{W},$$


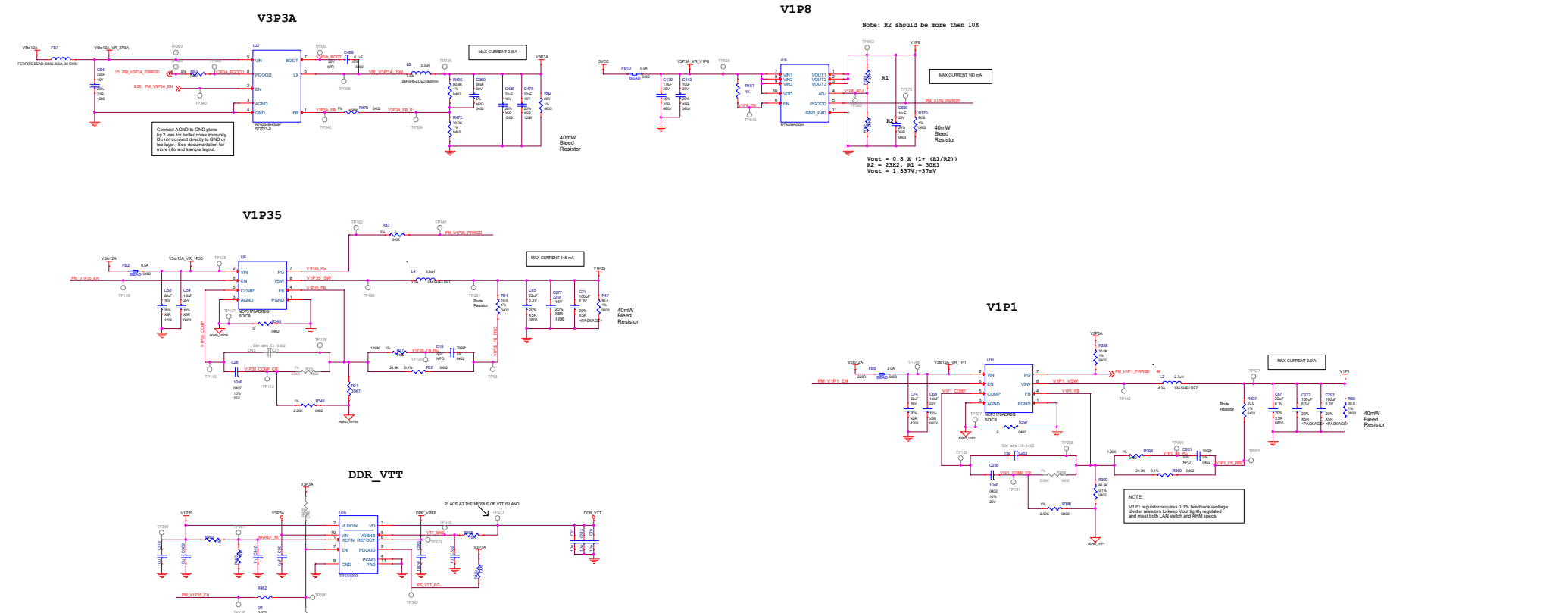
```

Devices:
VDD1V8, Current - 0.212A
DDR VDD1V5, Current - 0.049A
SFP+ (SR/LR), Current - 4x 303mA = 1.212A
LED SFP+ - 8x 5mA = 0.04A
2x1GbE - 4x 5mA = 0.02A
8x1GbE - 16x 5mA = 0.08A
BRM SW - 0.693A
RGMII PHY - 0.0919A
Logic - ~0.1A

```

Total Current - 2.4979A Max

DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group	
SIZE : A3			REV No. : R100		NAME	SIGN		DATE
DATE : Sunday, December 16, 2018			5VCC, 3V3VCC	CHECK	Nadav Y.	Nadav Y.		
Wednesday, May 23, 2018				APPROV.	David C.	David C.		
			SHEET : 24 of SHEETS : 49					

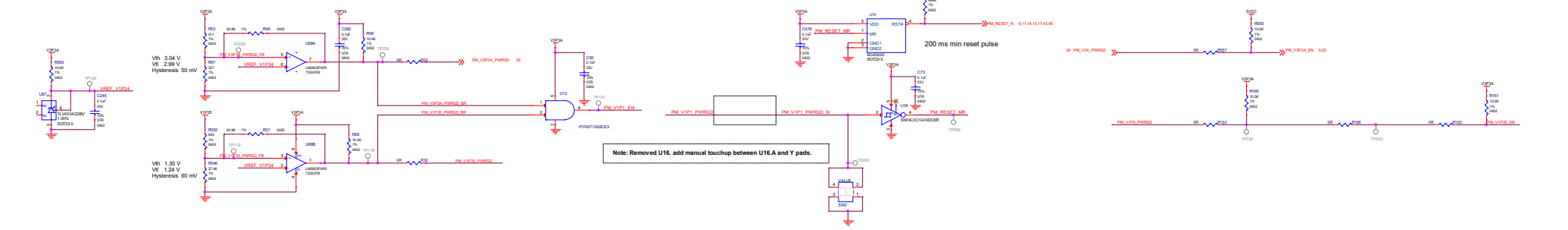


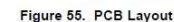
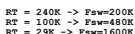
- SOC Power Sequence:
1. PM_V2P5 Enabled after V3P3A
 2. PM_V1P35 Enabled after V1P8
 3. PM_V1P1 Enabled: After V3P3A reached 3.04V & V1P35 reached 1.301V
- PM_V1P1 Disabled:
1. When above doesn't exist
 2. If V3P3A above 3.8V or V1P35 above 1.45V

SoC Power Sequence Comparator

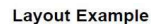
Voltage Supervisor / Reset Generation

Power Sequence

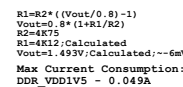


$$I_{\max}=6A; f_{\text{switch}}=480\text{kHz}, \text{ Eff}=0.9, I_{\text{out}}=1.797A, P_{\text{out}}=1.797W$$


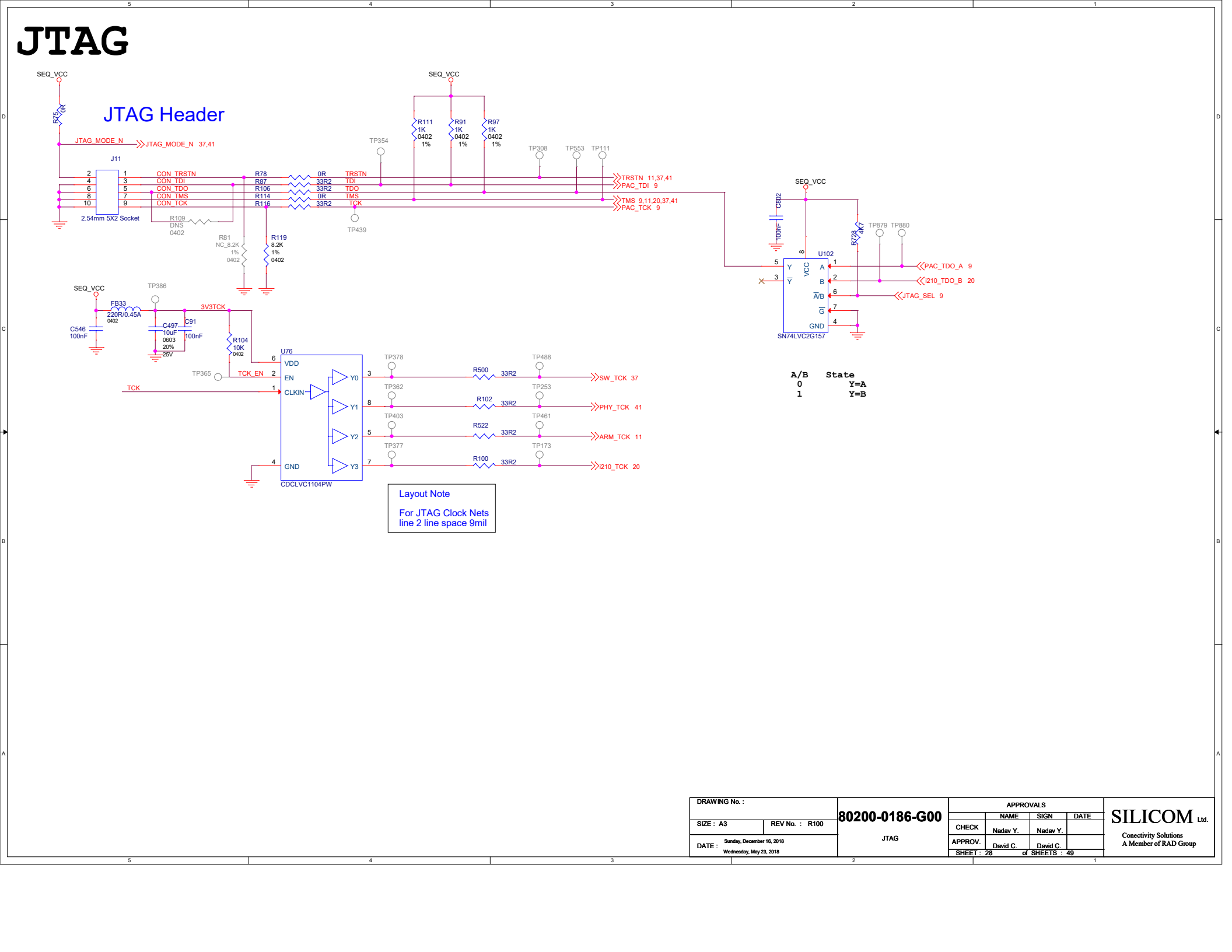
VDD1V8



DDR VDD1V5



DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group		
SIZE : A2			REV No. : R100		CHECK	Nadav Y.		Nadav Y.	
DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018			VDD1VGA, DDR_VDD1V5, VDD1V5		APPROV.	David C.		David C.	
					SHEET : 27	of SHEETS : 49			

[illegible]

JTAG Header

JTAG Mode N

JTAG Mode A

JTAG Mode B

Layout Note

For JTAG Clock Nets
line 2 line space 9mil

APPROVALS

NAME	SIGN	DATE
CHECK	Nadav Y.	Nadav Y.
APPROV.	David C.	David C.

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A Member of RAD Group

DRAWING No. : 80200-0186-G00

SIZE : A3 **REV No. :** R100

DATE : Sunday, December 16, 2018
Wednesday, May 23, 2018

JTAG

SHEET : 28 of SHEETS : 49

JTAG Header

JTAG_MODE N >> JTAG_MODE_N 37,41

2.54mm 5X2 Socket

CON TRSTN
CON TDI
CON TDO
CON TMS
CON TCK

R78
R87
R106
R114
R116
R109
R81
R119
R104

0R
33R2
33R2
0R
33R2
DNS
0402
1%
8.2K
0402
1%
10K
0402

TRSTN
TDI
TDO
TMS
TCK

TP354
TP308
TP553
TP111
TP439
TP386
TP365
TP378
TP362
TP403
TP377
TP488
TP253
TP461
TP173

SEQ_VCC
SEQ_VCC
SEQ_VCC

FB33
C546
C497
C91
R104
U76
CDCLVC1104PW

220R/0.45A
100nF
100nF
100nF
1%
0402
20%
25V
VDD
EN
CLKIN
GND

3V3TCK
TCK
TCK_EN

Y0
Y1
Y2
Y3

TP378
TP362
TP403
TP377
TP488
TP253
TP461
TP173

R500
R102
R522
R100

33R2
33R2
33R2
33R2

>>SW_TCK 37
>>PHY_TCK 41
>>ARM_TCK 11
>>i210_TCK 20

Layout Note
For JTAG Clock Nets
line 2 line space 9mil

SEQ_VCC
SEQ_VCC
SEQ_VCC

C812
U102
SN74LVC2G157

VCC
A
B
A/B
G
GND

1
2
6
7
4

>>PAC_TDO_A 9
>>i210_TDO_B 20
>>JTAG_SEL 9

A/B
0
1

State
Y=A
Y=B

JTAG Header

JTAG_MODE N >> JTAG_MODE_N 37,41

2.54mm 5X2 Socket

CON TRSTN
CON TDI
CON TDO
CON TMS
CON TCK

R78
R87
R106
R114
R116
R109
R81
R119
R104

0R
33R2
33R2
0R
33R2
DNS 0402
NC_8.2K 1% 0402
8.2K 1% 0402
10K 10K 0402

TRSTN
TDI
TDO
TMS
TCK

TP354
TP308
TP553
TP111
TP439
TP386
TP365
TP378
TP362
TP403
TP377
TP488
TP253
TP461
TP173

CDCLVC1104PW

Layout Note

For JTAG Clock Nets
line 2 line space 9mil

SN74VHC157

A/B State
0 Y=A
1 Y=B

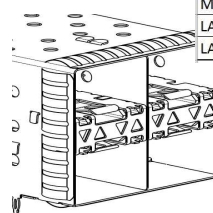
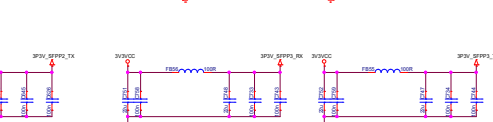
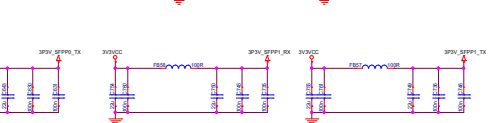
APPROVALS

NAME	SIGN	DATE
CHECK	Nadav Y.	Nadav Y.
APPROV.	David C.	David C.

SHEET : 28 of SHEETS : 49

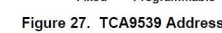
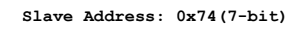
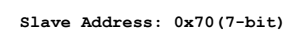
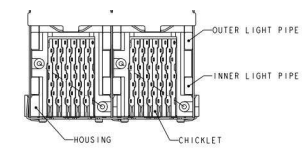
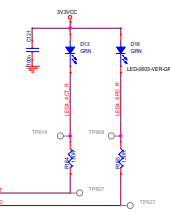
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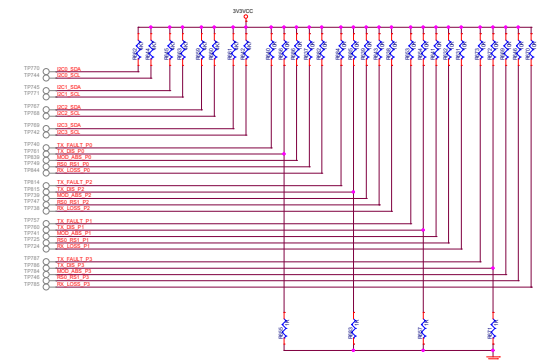


Note:
Arrow Down refers to lower port
Arrow Up refers to upper port

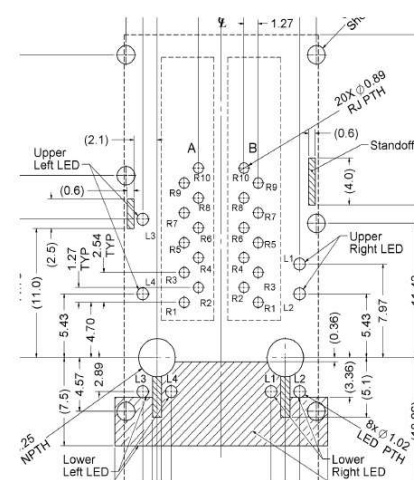
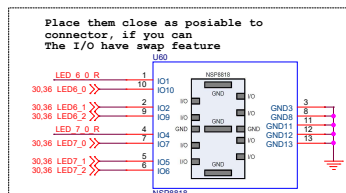
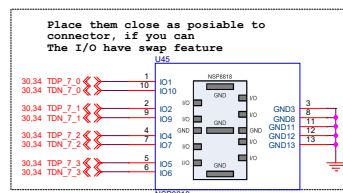
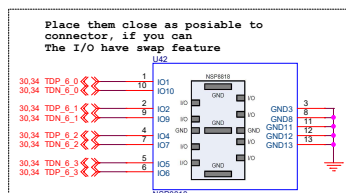
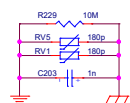
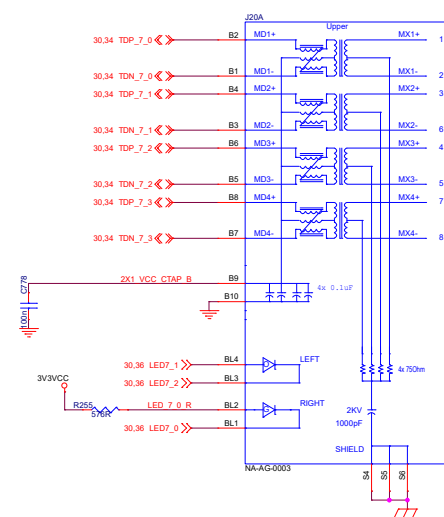
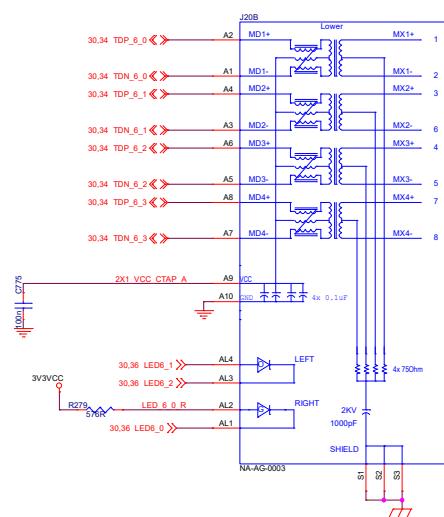
PORT1	PORT3
	
 	 
D17D13	D16D12
	
PORT2	PORT4



INPUTS		I ² C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 0x74 (hexadecimal)
L	H	117 (decimal), 0x75 (hexadecimal)
H	L	118 (decimal), 0x76 (hexadecimal)
H	H	119 (decimal), 0x77 (hexadecimal)



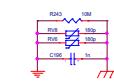
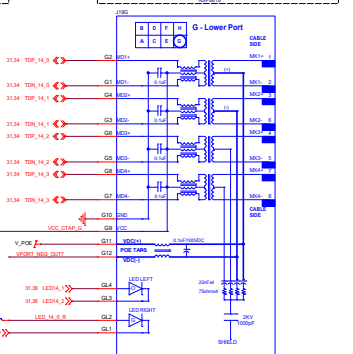
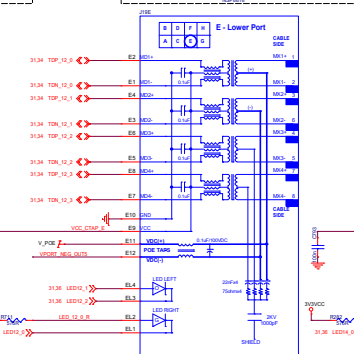
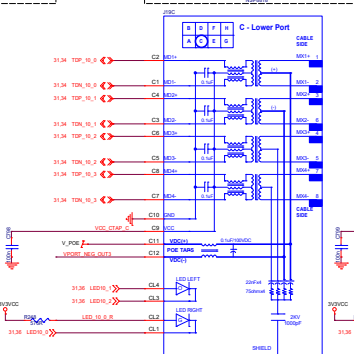
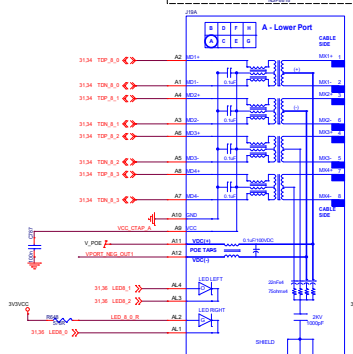
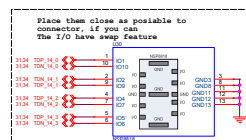
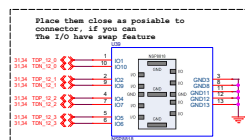
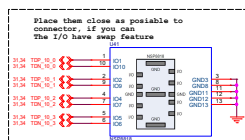
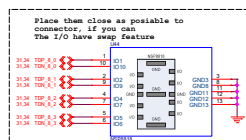
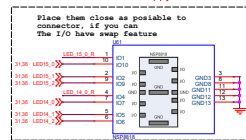
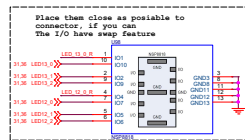
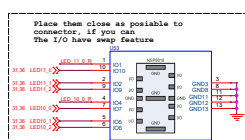
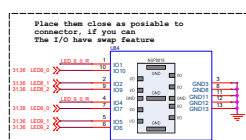
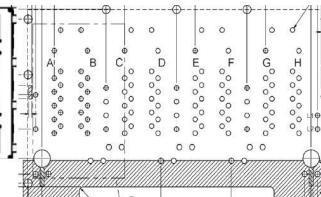
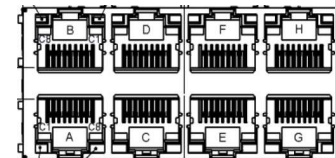
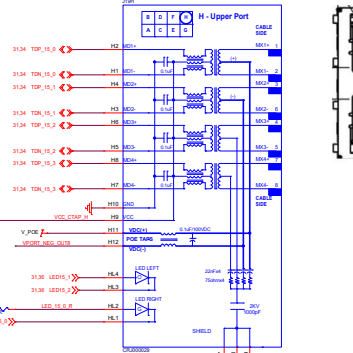
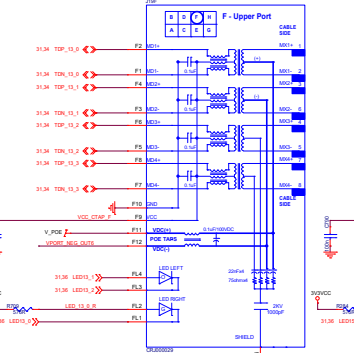
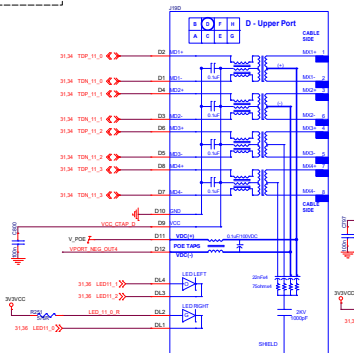
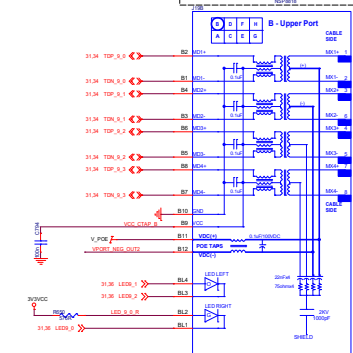
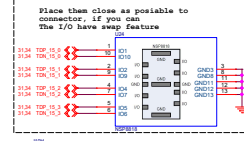
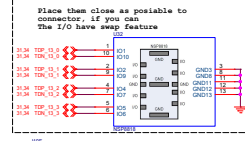
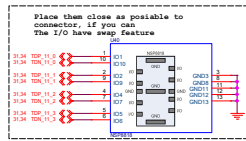
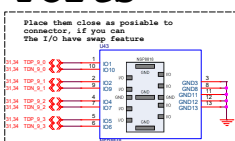
L Layout Note: All TP should be placed on RJ45



DRAWING No. :		80200-0186-000 2x1G6 RJ45	APPROVALS				 SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A2	REV No. : R100		CHECK	NAME	SIGN	DATE	
DATE : Sunday, December 10, 2018				Nadev Y.	Nadev Y.		
Wednesday, May 23, 2018			APPROV.	David C.	David C.		
			SHEET	1 of 1			

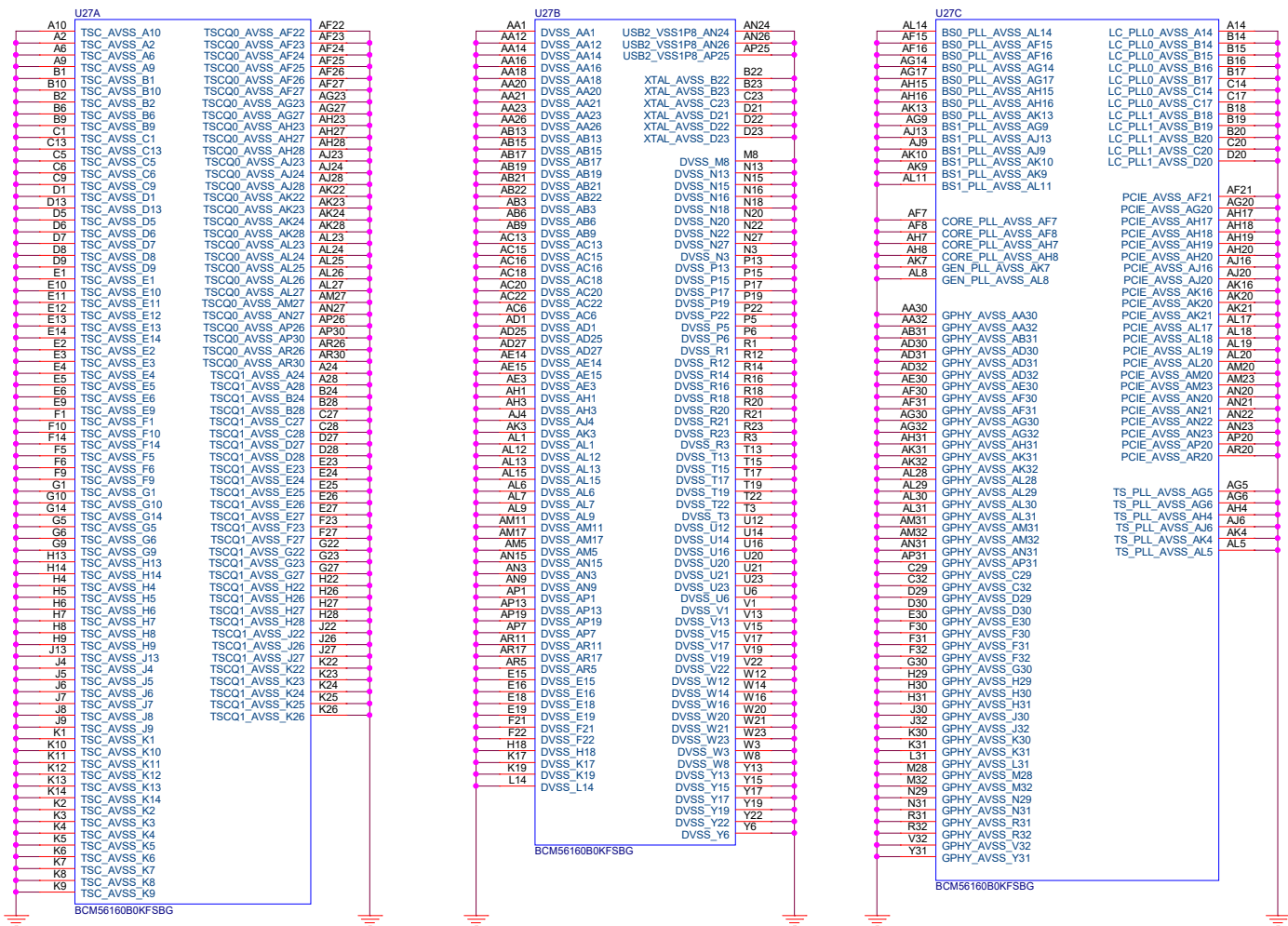
Right: Link/Act
Left: Speec

Place them close as possible to
connector, if you can
The I/O have swap feature



Division No. : 		80200-0186-G00 2nd POE + Parts	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIDE : AJ REV No. : R130			CHECK	NAME	SIGN	DATE	
				Nader Y.	Nader Y.		
			APPROV.	David C.	David C.		
DATE: Sunday, December 18, 2011 Wednesday, May 09, 2012		SHEET 31 of 38					

BCM56160 - AGND, DGND



DRAWING No. :		REV No. : R100		APPROVALS	
SIZE : A3				NAME	SIGN
DATE : Sunday, December 16, 2018				CHECK	DATE
Wednesday, May 05, 2016				Nadav Y.	Nadav Y.
				APPROV.	David C.
				SHEET : 32	of SHEETS : 49

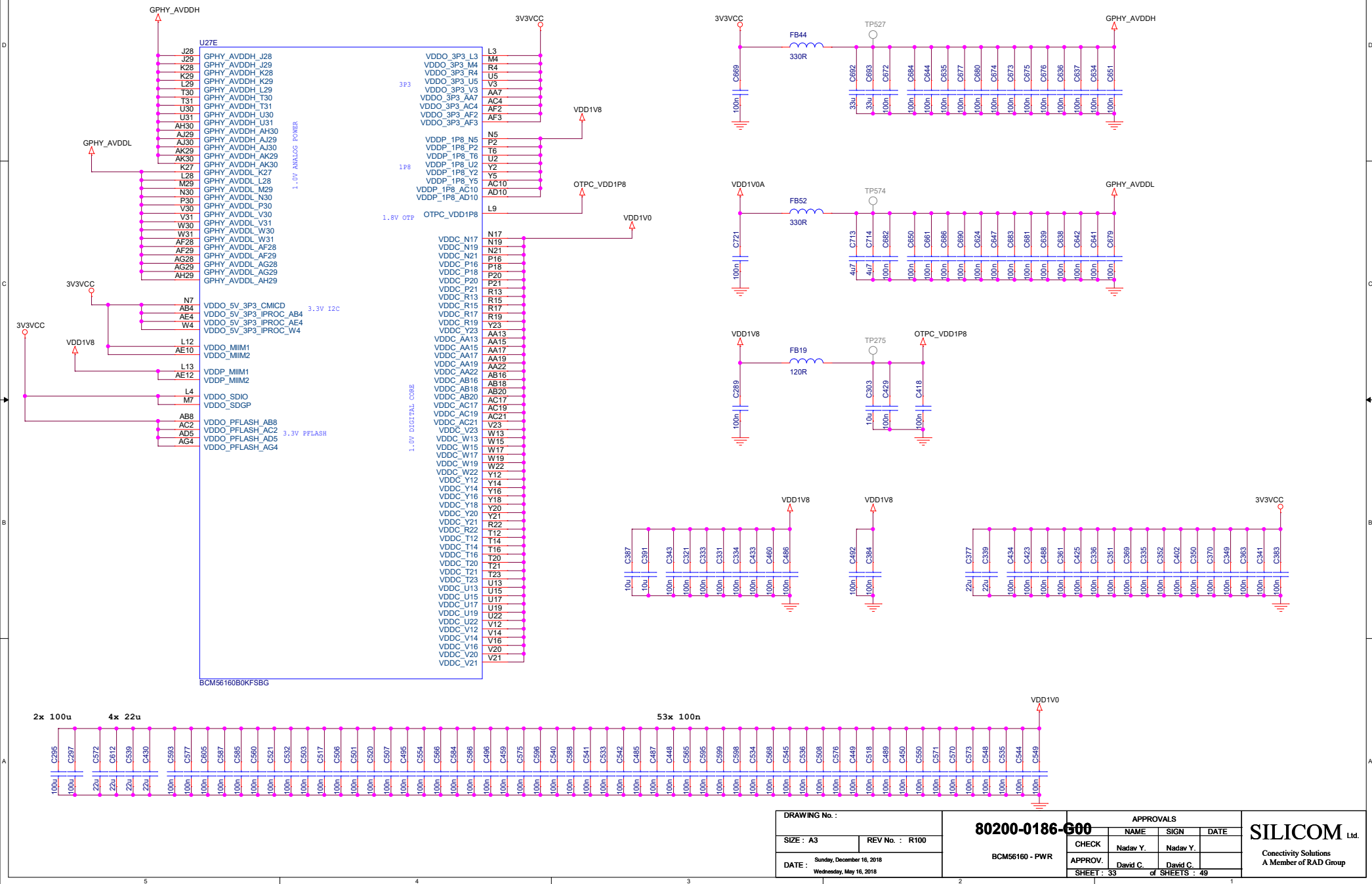
80200-0186-000

BCM56160 - GND

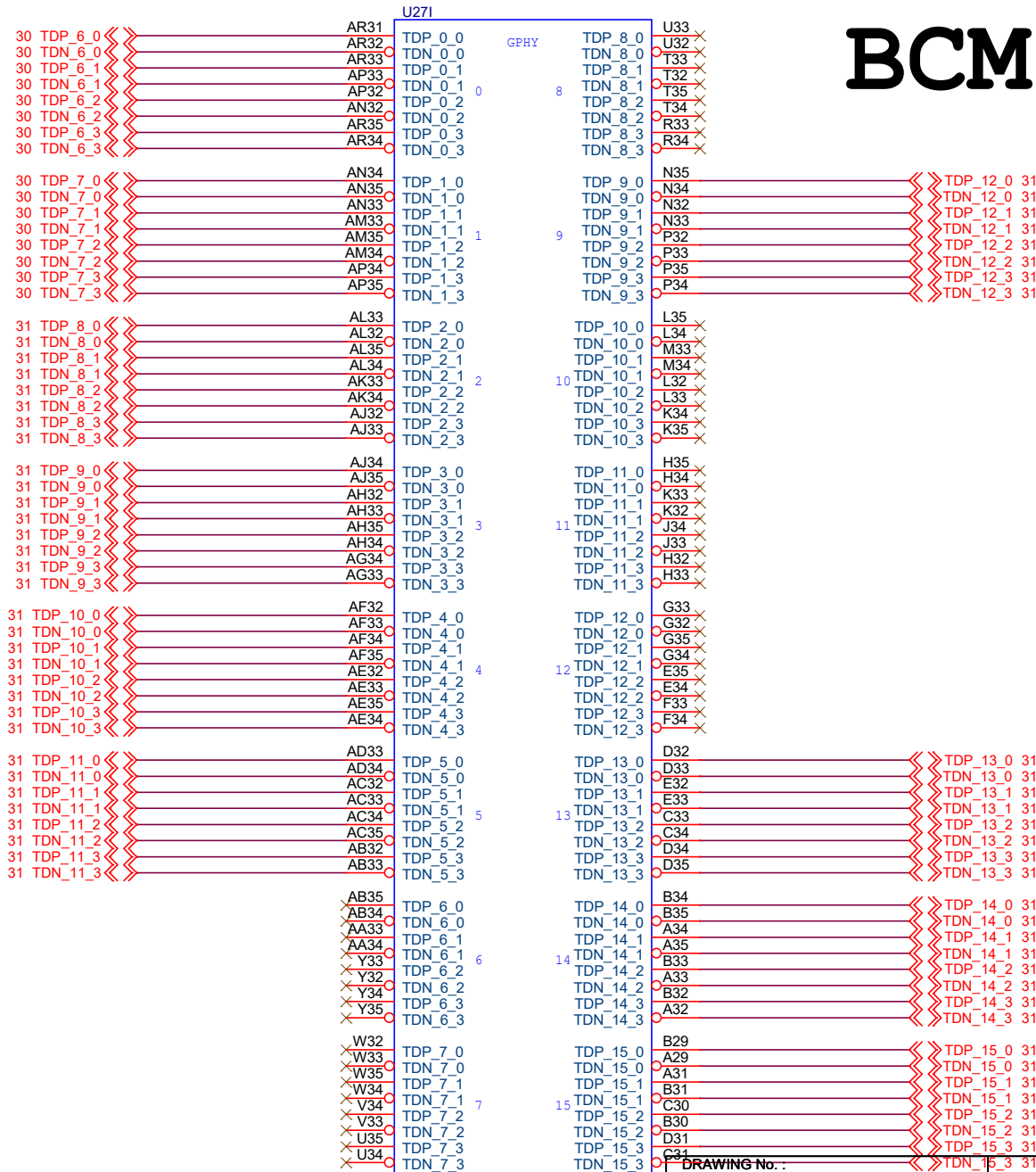
SILICOM Ltd.

Connectivity Solutions
A Member of RAD Group

BCM56160 – PWR



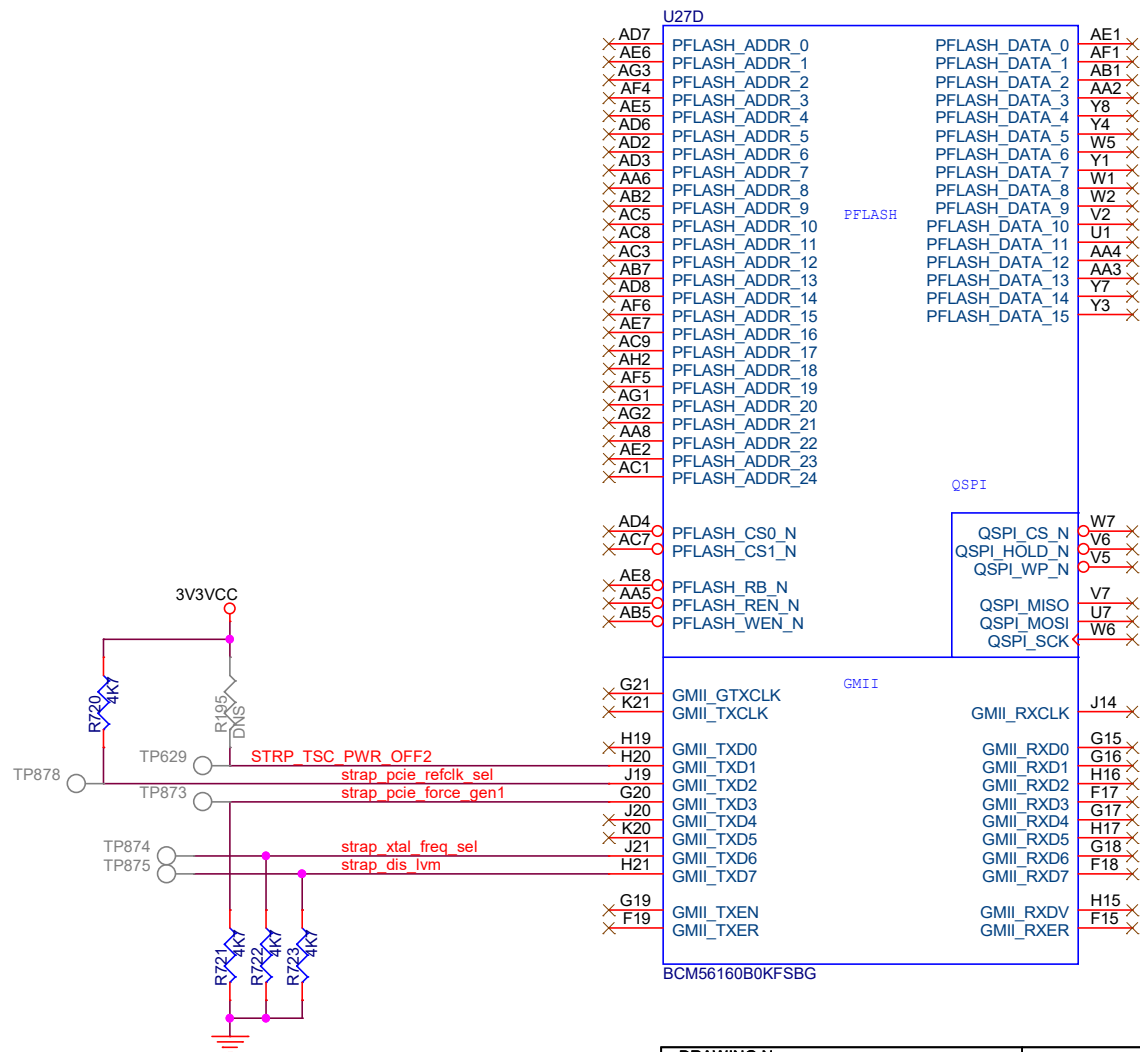
BCM56160 - GPHY



FP Port #	SW P#	SFP+ 2x2	RJ45 2x1	RJ45 2x4
1	TSC0/0	1	N/A	N/A
2	TSC0/1	2	N/A	N/A
3	TSC0/2	3	N/A	N/A
4	TSC0/3	4	N/A	N/A
5	0	N/A	0	N/A
6	1	N/A	1	N/A
7	2	N/A	N/A	0
8	3	N/A	N/A	1
9	4	N/A	N/A	2
10	5	N/A	N/A	3
11	9	N/A	N/A	4
12	13	N/A	N/A	5
13	14	N/A	N/A	6
14	15	N/A	N/A	7

DRAWING No. :		80200-0186-G00	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group	
SIZE : A4	REV No. : R100		CHECK	NAME	SIGN		DATE
DATE : Sunday, December 16, 2018 Wednesday, May 16, 2018			APPROV.	Nadav Y.	Nadav Y.		
				David C.	David C.		
		BCM56160 - GPHY	SHEET : 34 of SHEETS : 49				

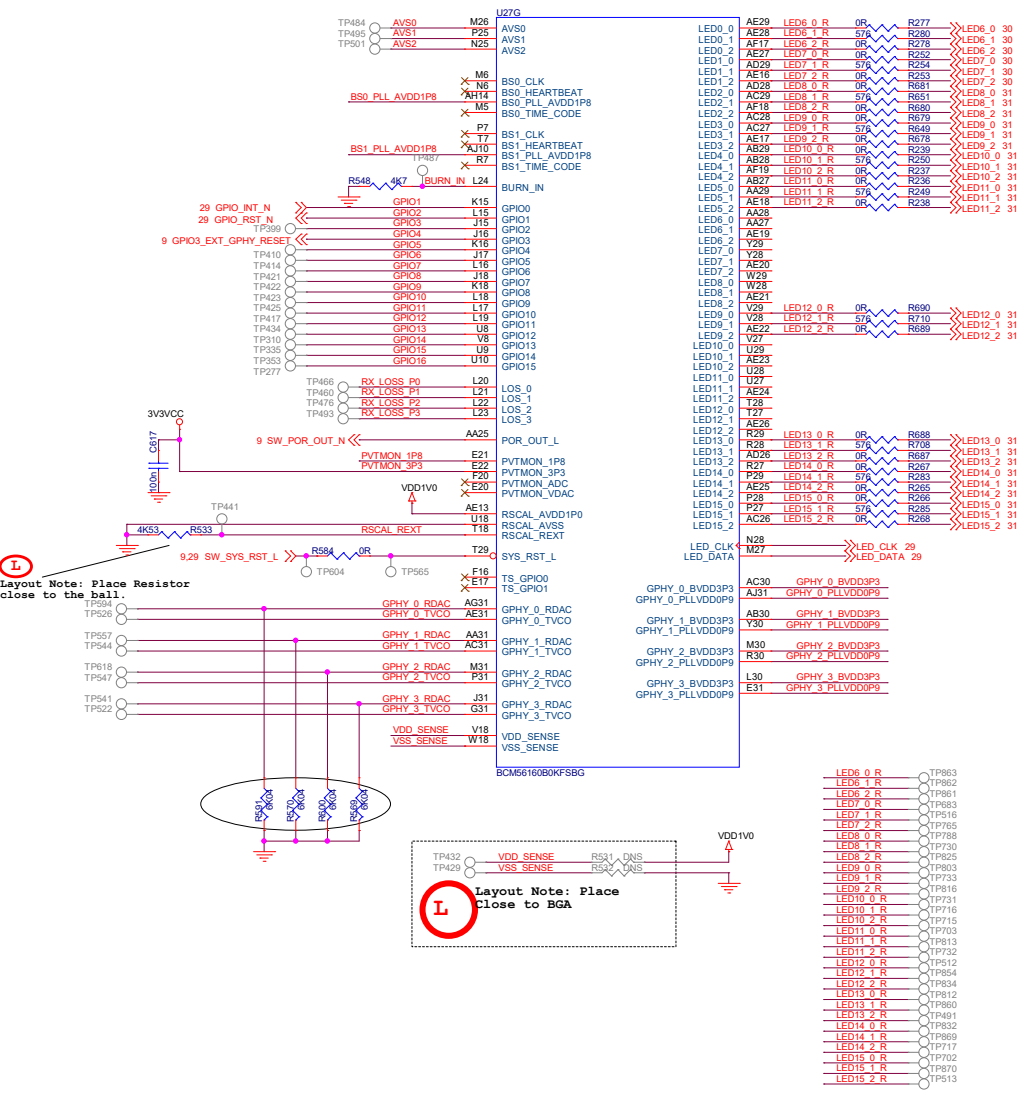
BCM56160 - QSPI, RGMII, PFLASH



DRAWING No. :		80200-0186-G00 BCM56160 - QSPI, RGMII, PFLASH	APPROVALS			SILICOM Ltd. Conectivity Solutions A Member of RAD Group	
SIZE : A4			REV No. : R100	NAME	SIGN		DATE
DATE : Sunday, December 16, 2018			BCM56160 - QSPI, RGMII, PFLASH	CHECK	Nadav Y.		Nadav Y.
Wednesday, May 16, 2018				APPROV.	David C.		David C.
				SHEET : 35	of SHEETS : 49		

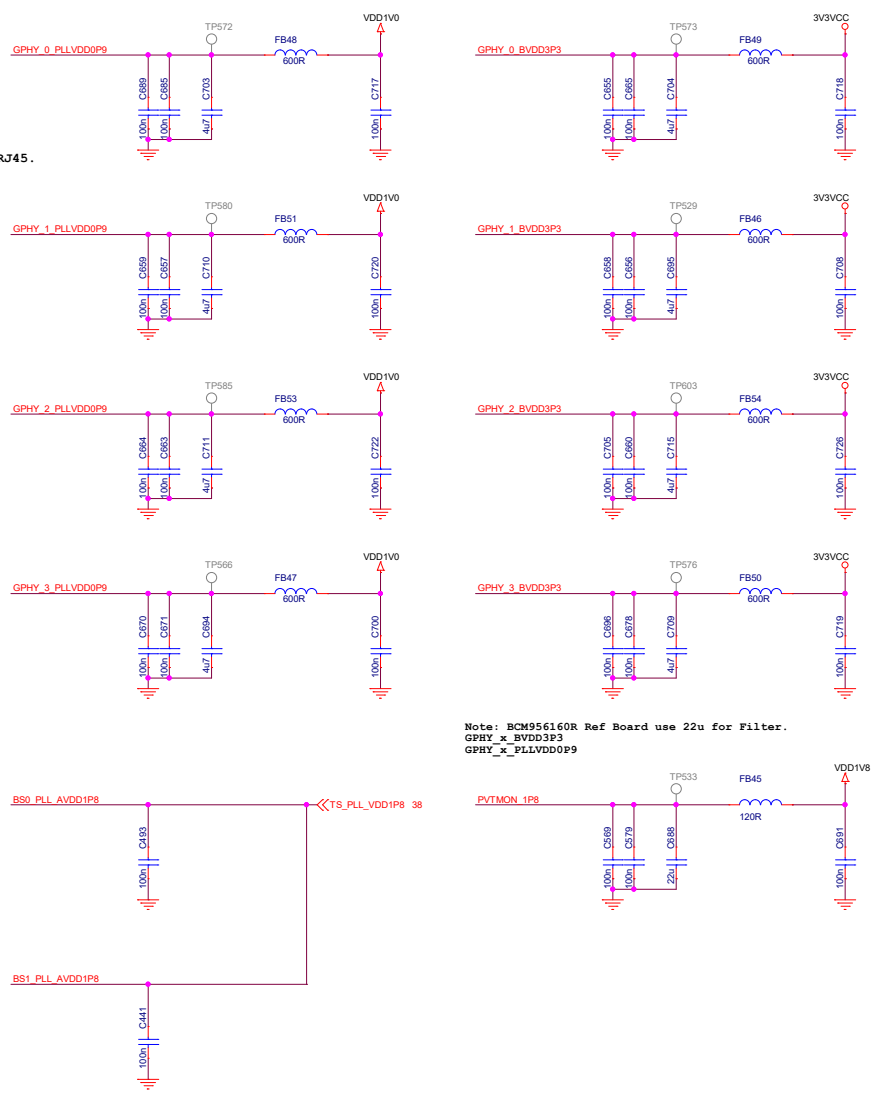
BCM56160 - LED, GPIO

Layout Note: place short resistor close to RJ45.



Layout Note: Place Resistor close to the ball.

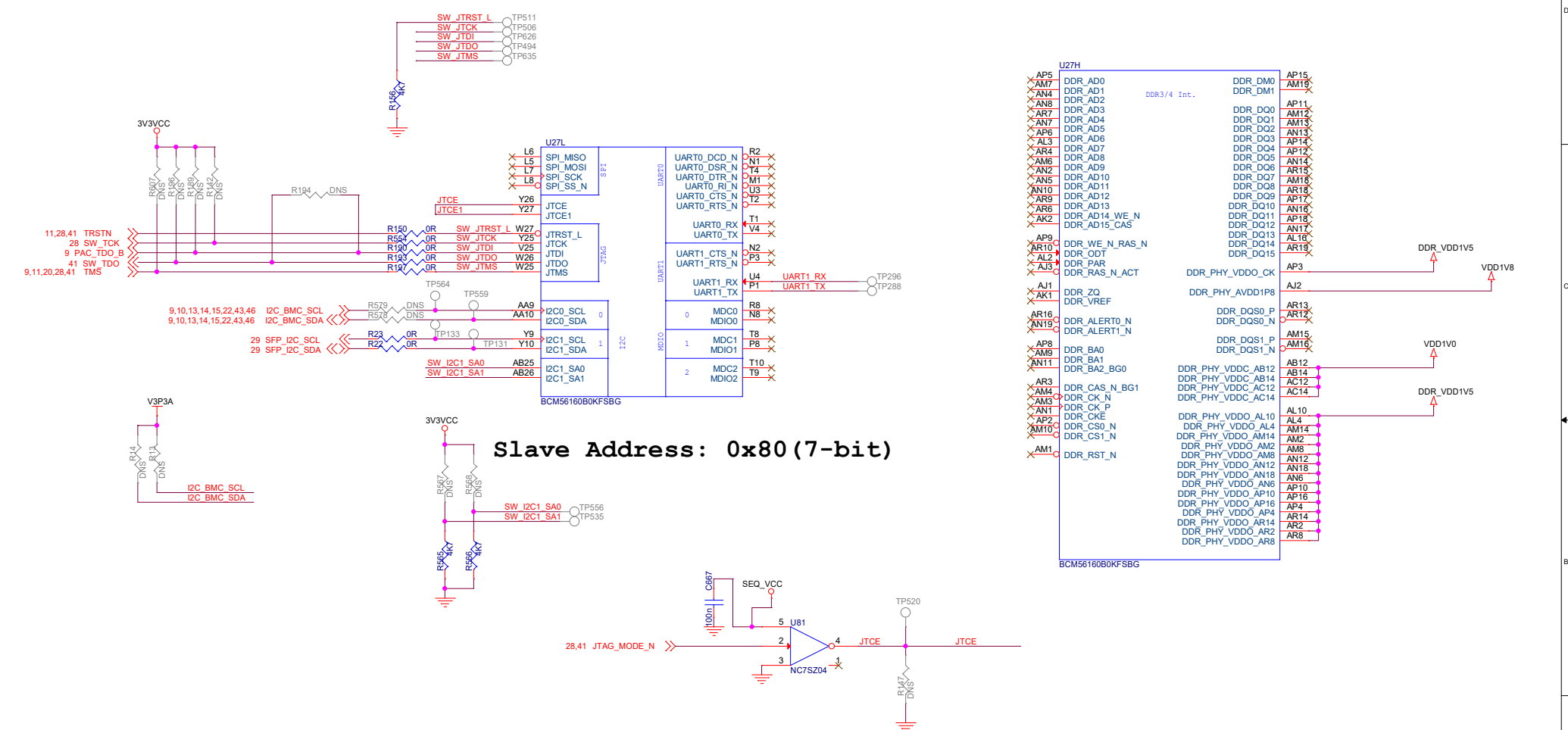
Layout Note: Place close to BGA



Note: BCM956160R Ref Board use 22u for Filter.
GPHY_x_BVDD3P3
GPHY_x_PLLVDD0P9

DRAWING No. :		80200-0186-G00	APPROVALS			SILICOM Ltd. Concivity Solutions A Member of RAD Group	
SIZE : Custom	REV No. : R100		CHECK	NAME	SIGN		DATE
DATE : Tuesday, December 18, 2018 Wednesday, May 16, 2018				Nadav Y.	Nadav Y.		
			APPROV.	David C.	David C.		
			SHEET : 36 of SHEETS : 49				

BCM56160 - SPI, JTAG, UART, DDR

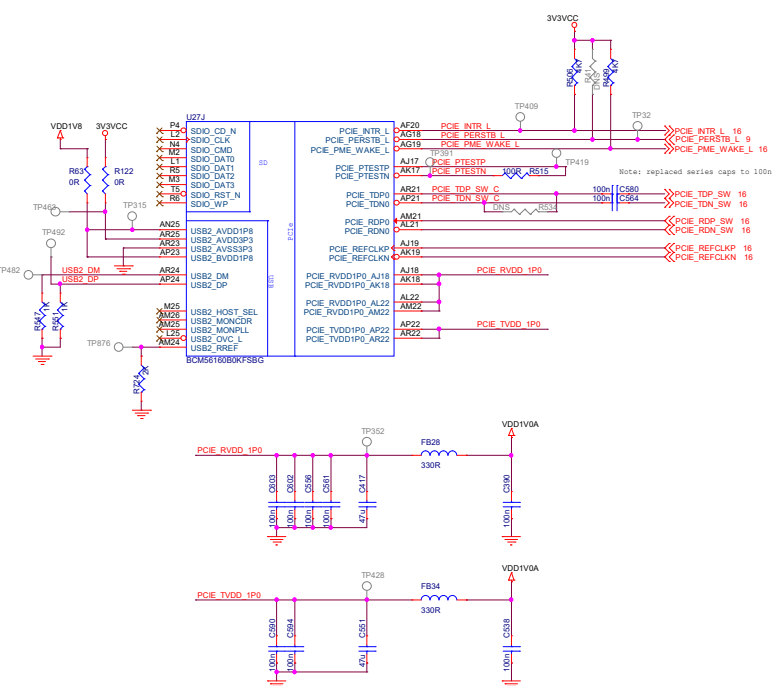


Slave Address: 0x80 (7-bit)

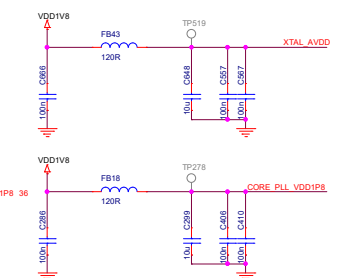
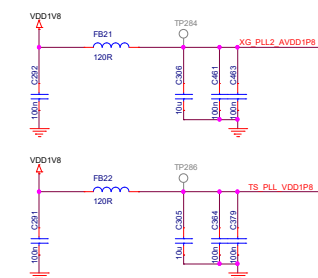
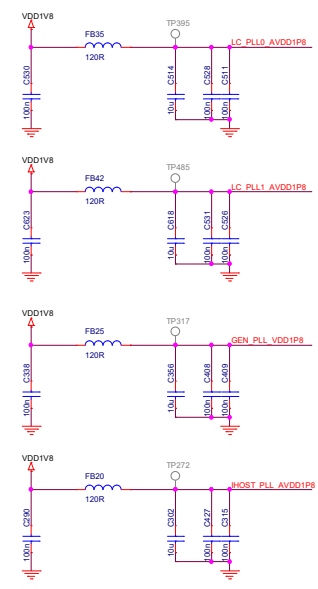
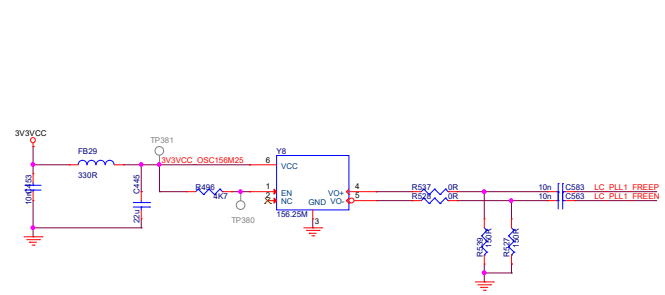
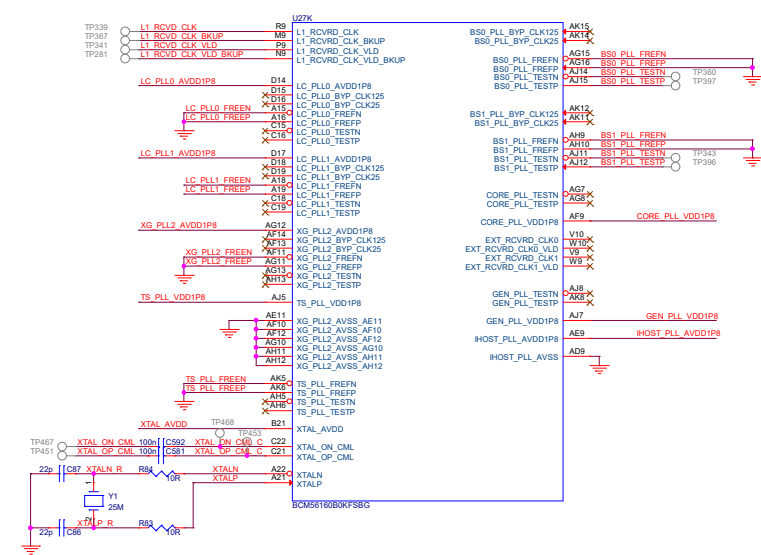
Signal/Bus Name	Qty.	I/O Type	Rate	Tech	Pin Description
I2C1_SA[1:0]	2	I _{PD}	Static	CMOS, 3.3V	CMICd BSC BSC1 Address When in Slave Mode 0: Address is 0x80 (Default) 1: Address is 0x81 2: Address is 0x82 3: Address is 0x83

DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Conectivity Solutions A Member of RAD Group
SIZE : A3			CHECK	NAME	SIGN	DATE	
REV No. : R100				Nadav Y.	Nadav Y.		
DATE : Sunday, December 16, 2018				APPROV.	David C.	David C.	
Wednesday, May 16, 2018		BCM56160 - SPI, JTAG, UART, DDR		SHEET : 37		of SHEETS : 49	

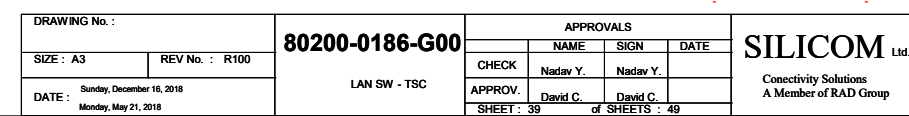
BCM56160 - SD, USB, PCIe, PLL



Layout Note: All etch GND traces of PLL should be short as possible to eliminate the pickup of noise.

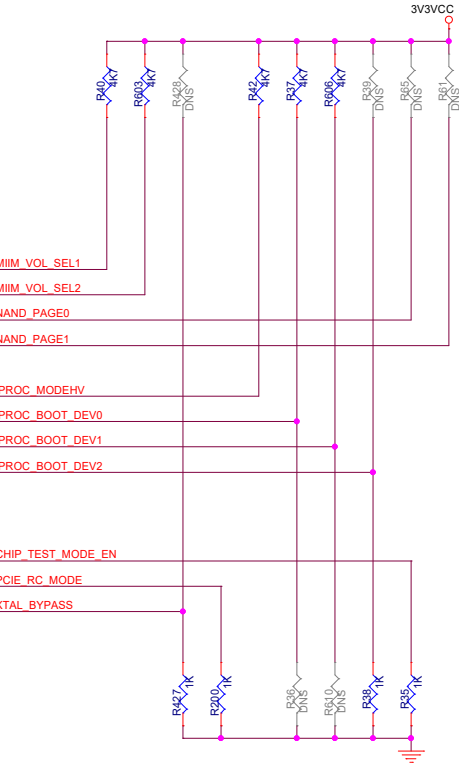
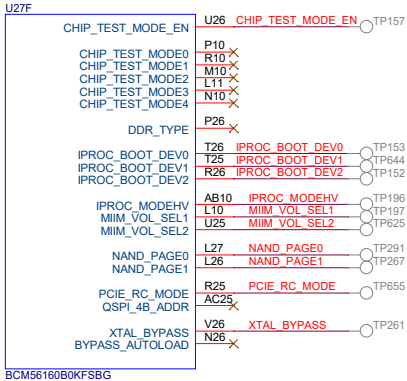


DRAWING No. :		80200-0186-G00		APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A2	REV No. : R100			CHECK	NAME	SIGN	DATE
DATE : Sunday, December 16, 2018		BCM56160 - SD, USB, PCIe, PLL		APPROV.	David C.	Nadav Y.	
Monday, May 21, 2018				SHEET : 38	of SHEETS : 49		

[illegible]

DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd Connectivity Solutions A Member of RAD Group		
SIZE: A3			REV No. : R100			NAME		SIGN	DATE
					CHECK	Nadav Y.		Nadav Y.	
					APPROV.	David C.		David C.	
DATE: Sunday, December 16, 2018 Monday, May 21, 2018					SHEET : 39	of SHEETS : 49			
		LAN SW - TSC							

BCM56160 – Configuration



Strap Pin Interface

The BCM56160/BCM56162 has strap pins which are used to set boot devices, PCIe usage, configuration of different FLASH types, etc. and those strap pins are sampled during the chip reset stage. Most of them have internal pull-up or down resistors. All strap pin settings are listed in Table 6 for convenience. To strap the pin to a high level, the user needs to connect the pin to 3.3V through a 4.7K ohm resistor. To strap the pin to a low level, the user needs to connect the pin to ground through a 1K ohm resistor.

Table 8: Strap Pin Setting			
Strap Pins	Function Description	Pin Name	Default Value
IPROC_BOOT_DEV[2]	Boot Device 0: SPI NOR FLASH 1: NAND FLASH 2: Boot ROM 3: Host processor (code are expected to be directly fetched and executed from external host memory)	IPROC_BOOT_DEV2	0
IPROC_BOOT_DEV[1]		IPROC_BOOT_DEV1	0
IPROC_BOOT_DEV[0]		IPROC_BOOT_DEV0	0
strap_nand_type[3]	NAND Type 0: NAND + ECC disabled & 16B spare - 512B sector 1: NAND + 1 bit ECC & 16B spare - 512B sector 2: NAND + 4 bit ECC & 16B spare - 512B sector 3: NAND + 8 bit ECC & 16B spare - 512B sector 4: NAND + 8 bit ECC & 27B spare - 512B sector 5: NAND + 12 bit ECC & 27B spare - 512B sector 6: NAND + 24 bit ECC & 27B spare - 1K sector 7: NAND + 30 bit ECC & 27B spare - 1K sector 8: NAND + 40 bit ECC & 45B spare - 1K sector	GMII_TXEN	0
strap_nand_type[2]		GMII_TXER	0
strap_nand_type[1]		LED_DATA	0
strap_nand_type[0]		LED_CLK	0

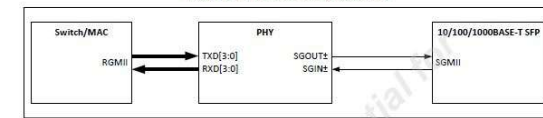
Table 8: Strap Pin Setting (Cont.)			
Strap Pins	Function Description	Pin Name	Default Value
NAND_PAGE[1]	NAND Page Size 0: 1 KB page 1: 2 KB page 2: 4 KB page 3: 8 KB page	NAND_PAGE1	0
NAND_PAGE[0]		NAND_PAGE0	0
strap_icpll1_refclk_sel	LCPLL1 Reference Clock Source Selection 1: from l_refclk, Xtal 0: from LCPLL1 differential pad	L1_RCVRD_CLK_VALID_BKUP	0
QSPI_4B_ADDR	SPI Flash Addressing Mode 1: SPI4-byte addressing mode 0: SPI3-byte addressing mode	QSPI_4B_ADDR	0
I2C_SA1	I2C1 (cmicd12c) address when in slave mode 0: address 0x80 1: address 0x81 2: address 0x82 3: address 0x83	I2C_SA1	0
I2C_SA0		I2C_SA0	0
PCIE_RC_MODE	PCIE RC/EP mode 1: RC 0: EP	PCIE_RC_MODE	0
strap_pcie_refclk_sel	PCIE Reference Clock Source Selection 1: External clock source 0: Internal clock source	GMII_TXD2	1
strap_pcie_force_gen1	Force PCIE Gen1 Compliant 1: Gen1 0: Gen2	GMII_TXD3	0
USB2_HOST_SEL	USB2 Host Mode Selection 1: Host 0: Slave	USB2_HOST_SEL	1
XTAL_BYPASS	Selection between Osc and Xtal 1: OSC 0: Xtal	XTAL_BYPASS	0
MIIM_VOLT_SEL2	MIIM2 voltage selection 1: 3.3V/2.5V 0: 1.2V	MIIM_VOLT_SEL2	1 ^a
MIIM_VOLT_SEL1	MIIM1 voltage selection 1: 3.3V/2.5V 0: 1.2V	MIIM_VOLT_SEL1	1 ^a

Table 8: Strap Pin Setting (Cont.)

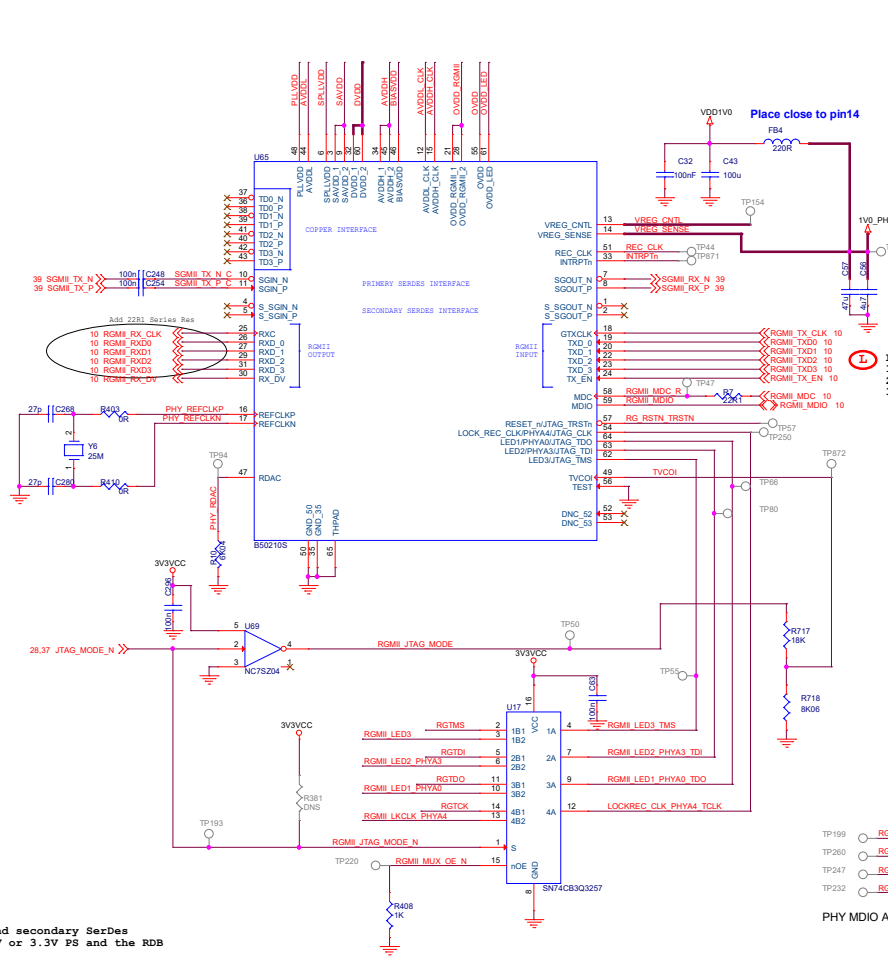
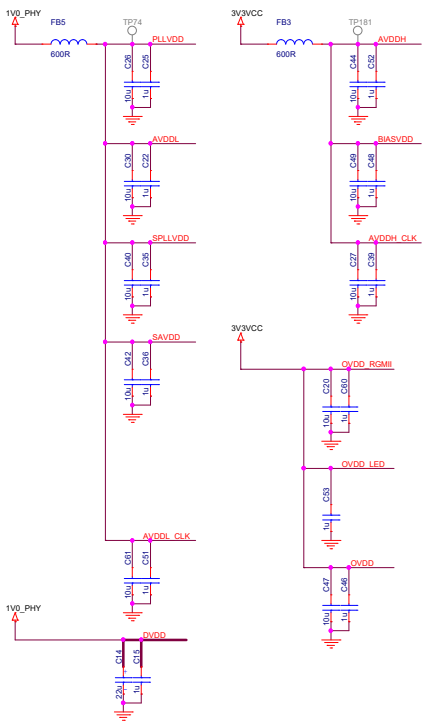
Strap Pins	Function Description	Pin Name	Default Value
DDR_TYPE	DDR type selection 1: DDR4 0: DDR3	DDR_TYPE	0
strap_pnor_nand_mw	Parallel NOR Flash or NAND Flash Memory Width 0: 8 bit 1: 16 bit	JTDO	1
strap_tsc_pwr_off[3]	Indicate TSC Core3 power is off 0: Indicate Power is On 1: Indicate Power is Off	GMII_TXD1	0
strap_tsc_pwr_off[2]	Indicate TSC Core2 power is off 0: Indicate Power is On 1: Indicate Power is Off	GMII_TXD4	0
strap_tsc_pwr_off[1]	Indicate TSC Core1 power is off 0: Indicate Power is On 1: Indicate Power is Off	GMII_TXD5	0
strap_tsc_pwr_off[0]	Indicate TSC Core0 power is off 0: Indicate Power is On 1: Indicate Power is Off	MDC0	0
strap_xtal_freq_sel	Xtal Clock Frequency Selection 1: 50M 0: 25M	GMII_TXD6	0
IPROC_MODEHV	Flash/qspi 3.3V/1.8V Power Selection 1: 3.3V 0: 1.8V	IPROC_MODEHV	N/A ^a

a. An external pull up/down resistor on PCB can not be saved for normal operation.

DRAWING No. :		80200-0186-G00		APPROVALS		SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A3		REV No. : R100		NAME	SIGN	DATE
DATE : Sunday, December 16, 2018		Wednesday, May 23, 2018		CHECK	Nadav Y.	Nadav Y.
				APPROV.	David C.	David C.
				SHEET : 40 of SHEETS : 49		



RGMII to SGMII- B50210S

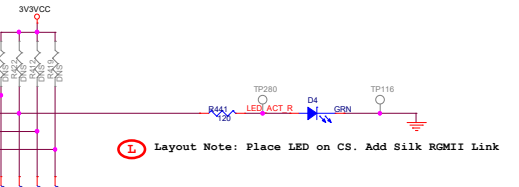
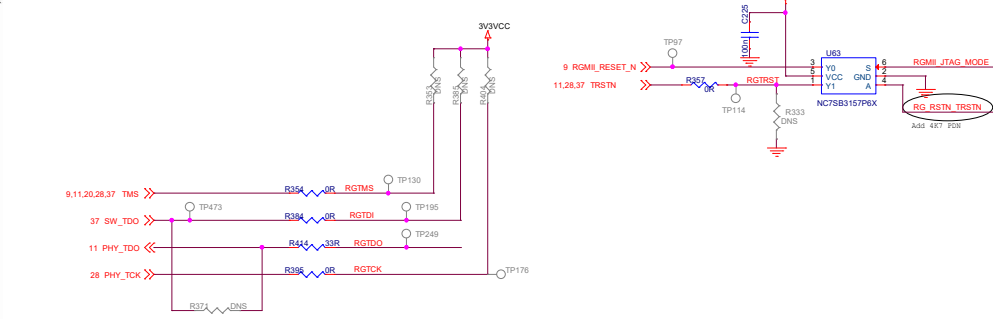
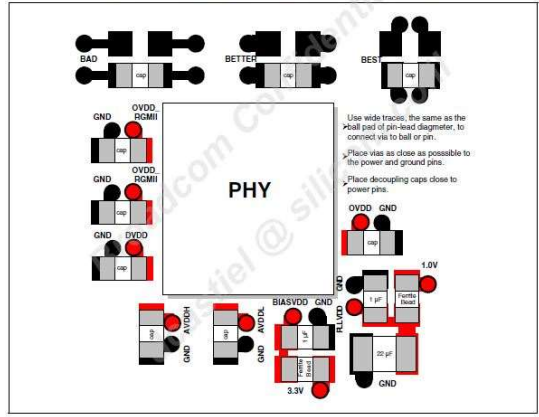


Layout Note:
 1. Trace route 50ohm.
 2. Trace lenght match 9.8mm.
 3. skew between signal 0.07n = 0.25".

Layout Note: Place Close to MDIO Pin.

- Layout Note:** 1u Cap should be placed close to its designated pin. see placemet recommendation in picture below.
- Design Note:** another option for inductor is P/N: EL0806475MT. MPN: LB2016T47R (TAIYODEN).
- Design Note:** from AN301 Hardware Consideration in RGMII-to SGMII(Slave) mode, users may leave the B50210S copper and secondary SerDes interface floating. the OVDD RGMII pads must be tied to 1 1.8V, 2.5V or 3.3V PS and the RDB register 0x810 bits [1:0] RGMII_SEL_REG must be set.

Figure 25: Filtering Component Layout (Recommended Method)

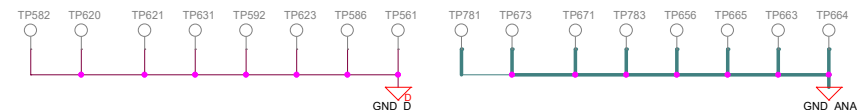
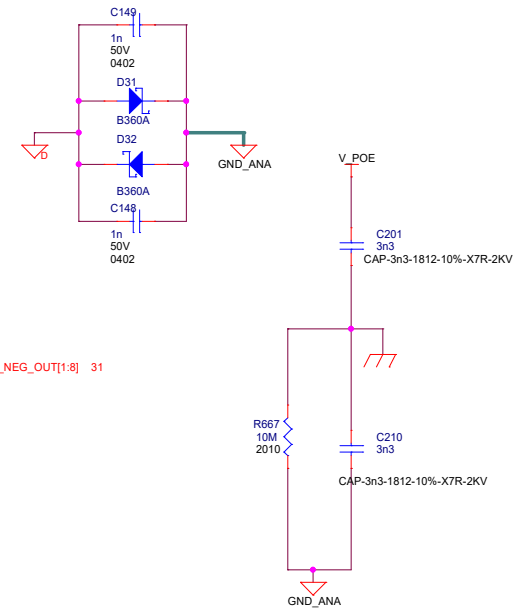
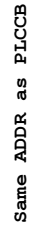


Layout Note: Place LED on CS. Add Silk RGMII Link

DRAWING No. :		80200-0186-G00	APPROVALS			SILICOM Ltd Connectivity Solutions A Member of RAD Group
SIZE : A2			CHECK			
REV No. : R100			Nadary Y. Nadary Y.			
DATE : Sunday, December 16, 2018 Thursday, May 17, 2018			APPROV. David C. David C.			
		RGMIII to SGMI-850210S	SHEET : 41 of SHEETS : 49			

Circuitry Solutions
A Member of RAD Group

The +54.5V output of the supply will be used as a Power Over Ethernet (PoE) source, and the products that use this supply must comply with the requirements of "Power Sourcing Equipment" as required in IEEE 802.3at – "+54.5V". In particular, the power supply must allow the products to comply with requirements for common mode noise on the +54.5V output. Noise relative to chassis ground is to be measured on each of the PoE output terminals, the noise must have a peak to peak amplitude of less than 100mV at the scope input.

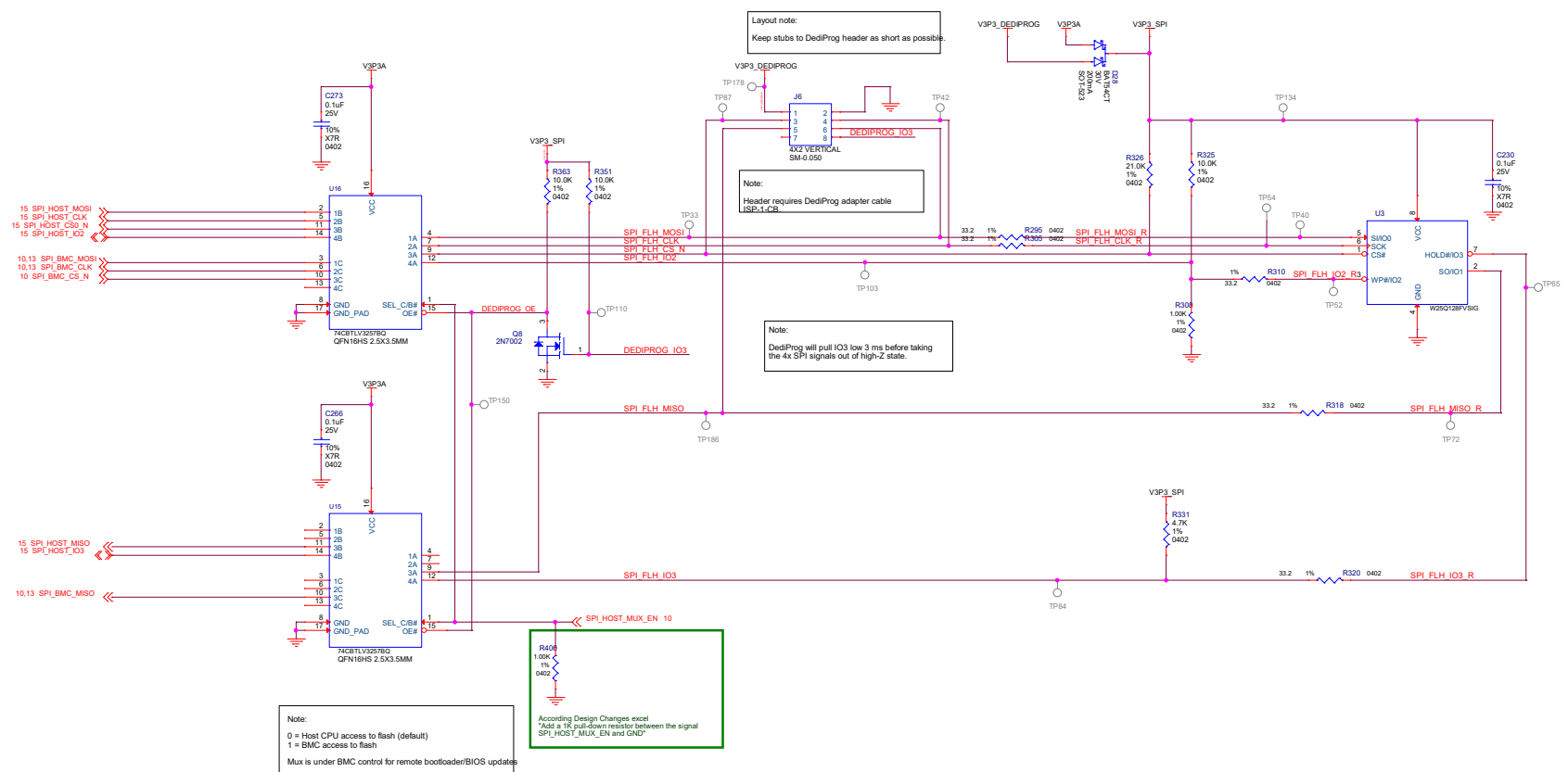


DRAWING No. :		80200-0186-G00 POE+ Controller PD69208	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : A3	REV No. : R100			NAME	SIGN	DATE	
			CHECK	Nadav Y.	Nadav Y.		
DATE : Sunday, December 16, 2018			APPROV.	David C.	David C.		
Wednesday, May 23, 2018			SHEET : 42	of SHEETS : 49			

BLANK

DRAWING No. :		80200-0186-G00 BLANK	APPROVALS			SILICOM Ltd. Conectivity Solutions A Member of RAD Group
SIZE : A4 REV No. : R100			NAME	SIGN	DATE	
DATE : Sunday, December 16, 2018			CHECK	Nadav Y.	Nadav Y.	
Sunday, June 17, 2018			APPROV.	David C.	David C.	
		SHEET : 44 of SHEETS : 49				

Host Boot Flash, Mux, DediProg



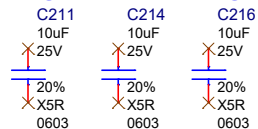
Note:
0 = Host CPU access to flash (default)
1 = BMC access to flash
Mux is under BMC control for remote bootloader/BIOS updates

According Design Changes excel
*Add a 1k pull-down resistor between the signal
SPI_HOST_MUX_EN and GND*

DRAWING No. :		80200-0186-000	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group	
SIZE : A2	REV No. : R100		CHECK	NAME	SIGN		DATE
DATE : Sunday, December 16, 2018			APPROV.	Nadav Y.	Nadav Y.		
Monday, June 18, 2018				David C.	David C.		
		SHEET : 45		of SHEETS : 49			

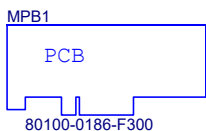
Misc, Debug LEDs

Light Blocking Caps For LED Lightpipe

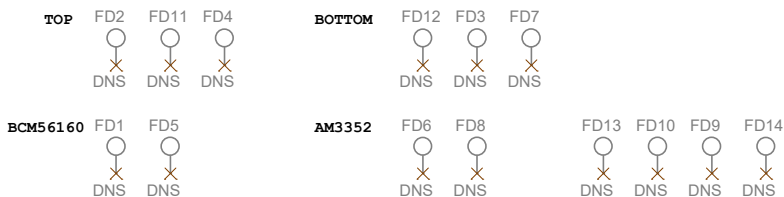


Note

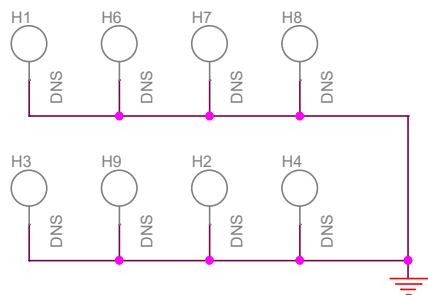
Light-blocking caps must be as tall as possible and still fit underneath the 1.40 mm lightpipe hood. Capacitor height must include both cap thickness and some tolerance for solder thickness. This cap was selected because the max height is 1.0 mm, allowing a little bit of tolerance for solder paste.



Fiducial Marks

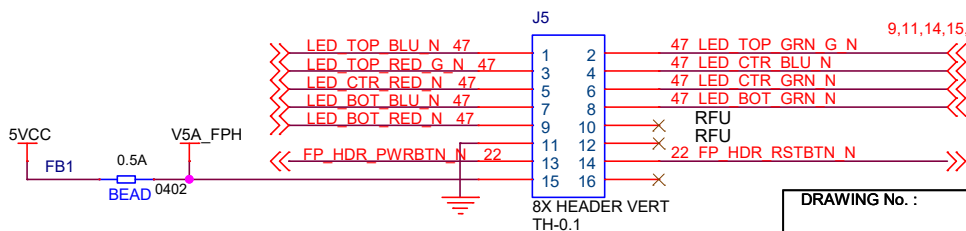


Mounting Holes

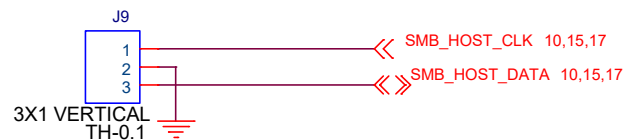
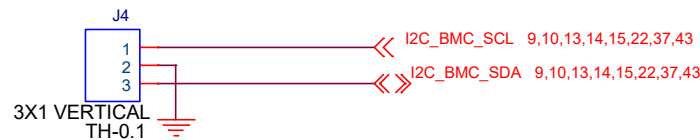


Tracking Label

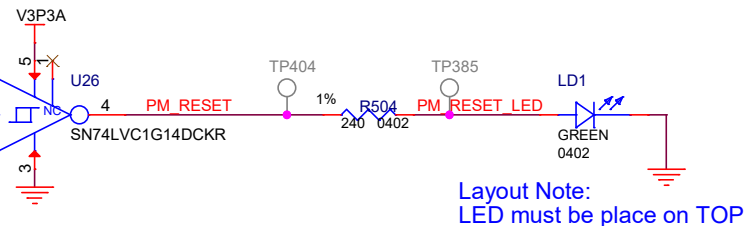
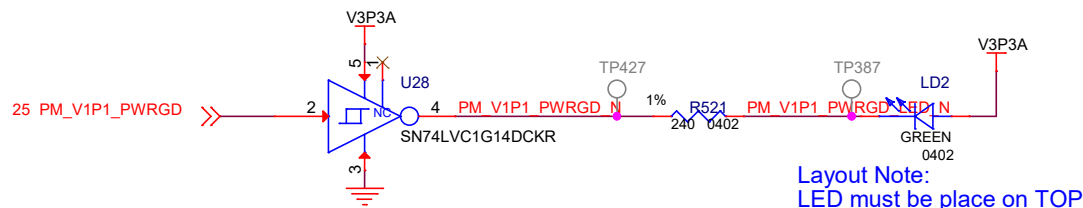
Front Panel Header



Debug Headers



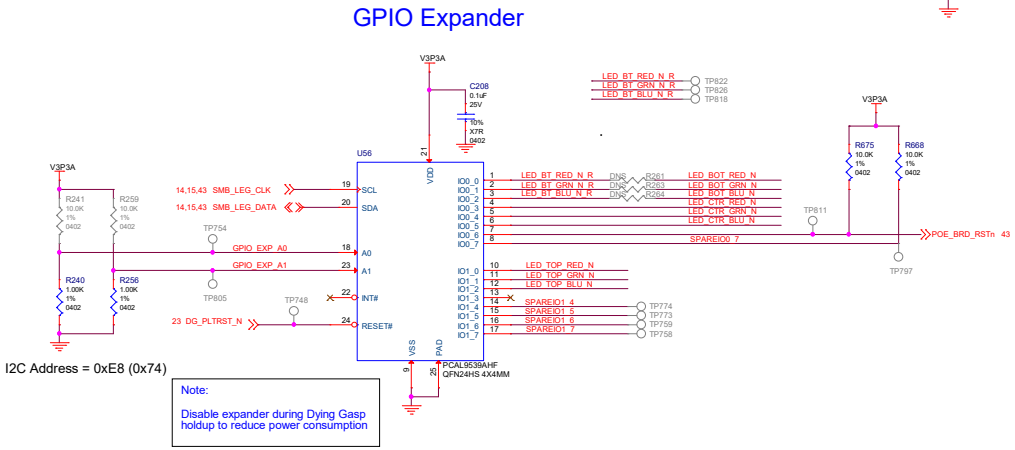
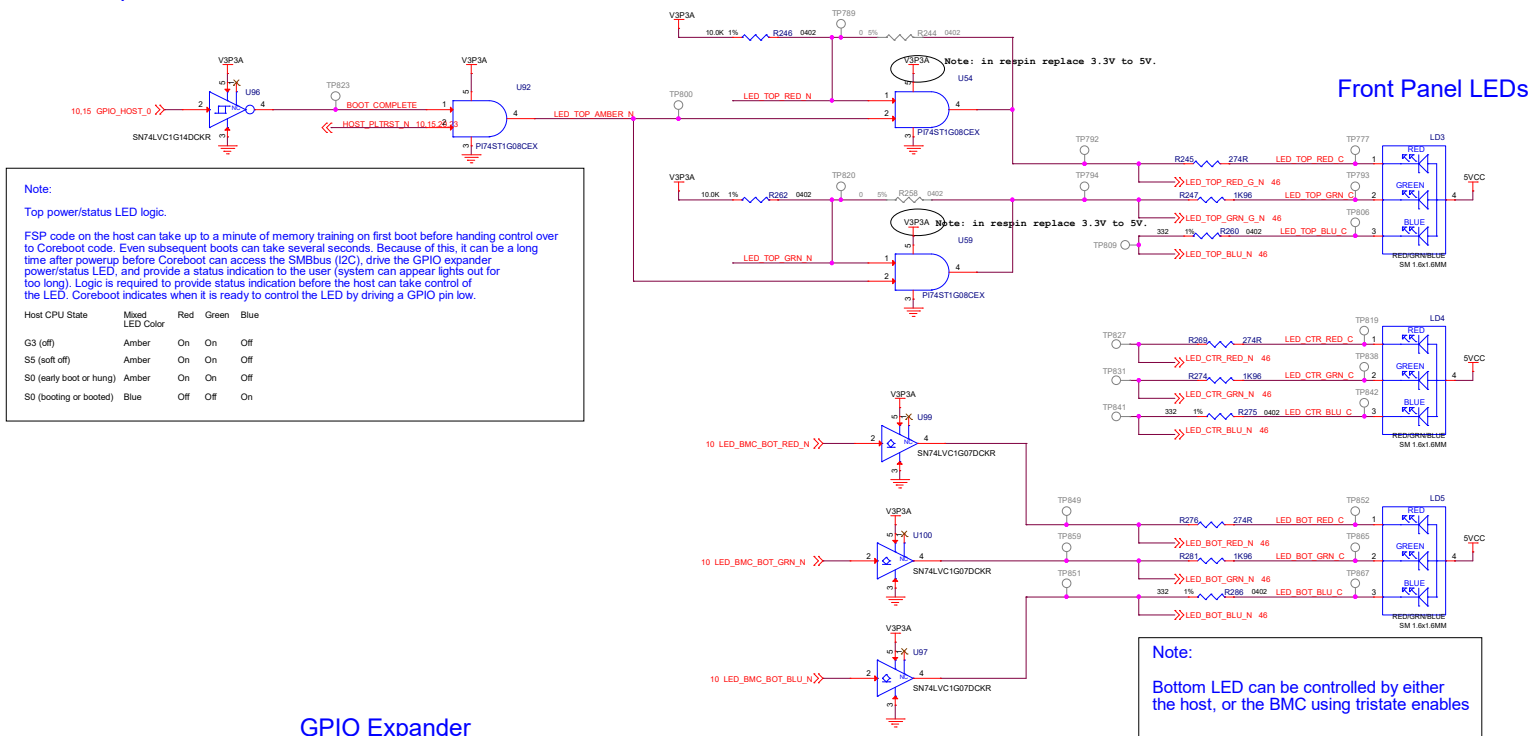
Debug LEDs



DRAWING No. :		80200-0186-G00	APPROVALS				SILICOM Ltd. Conectivity Solutions A Member of RAD Group
SIZE : A4	REV No. : R100			NAME	SIGN	DATE	
DATE : Sunday, December 16, 2018 Wednesday, May 23, 2018			CHECK	Nadav Y.	Nadav Y.		
			APPROV.	David C.	David C.		
			SHEET : 46 of SHEETS : 49				
		Misc, Debug LEDs					

GPIO Expander, Front Panel LEDs, Buzzer

GPIO Expander, Front Panel LEDs, Buzzer



Rev	Description
X100-00	Initial Release
X101-00	Rampup Fix
X200-00	PCB Respin, fix of missing connection to BCM56160, other chages are below.

Ramp Up and PCB respin changes.Update BOM.

Change List:

1. JTAG - Power rail from 3V3VCC to SEQ_VCC to: connector, PUP and clock buffer.
2. R75 change from 2K2 to 0R.
3. Remove R69 - prevented from VDD1V0 to start.
4. Added MUX for JTAG Chain to support PAC flash.

5. Added strap options to BCM56160.
XTAL Clock - 0 - 250MHz
PCIe Ref Clock - 1 - ECT Clock
Force Gen 2 - 0
Chip Test Function - 0
6. Adding DfP to VCC of RTC(uBMC).
7. Adding FUP to TFM(uBMC) CS.
8. Adding H5 to BCM. Spacer for M.2.
9. Fix VIPB PS voltage divider per datasheet.
a. Change R581 to 30K1.
b. Change R165 to 23K2.
10. JTRST SW Strap added - R165-4K7.
11. Enable I2C access to SFP I2C and Sidebands.

T&T Medium/Small IO Board Alpha ECO:

Add in 80400-0179-G10 and 80400-0180

- ```

1k CPW000034 = Power Cable, 34VDC PS to I/O Board, 300mm, M/S
1k CPW000034 = Power Cable, 12VDC PS to I/O Board, 300mm, M/S
1k CPW000035 = Switch to Power Supply Cable, 150mm, WHT/BLK,M/S
3k CBL000092 = GND Cable, 150mm, Green/Yellow, M/S
1k CP00000034 = AC Inlet
1k MA0000131 = Mesh assembly - chassis for M/S vCPE
3k MSLFAN-40X40X28M4 - remove current fans

1k ICM000083 = 240GS M.2 to Replace ICM000082 in 80400-0179-G10 only.

```

```
1x INIT#000800 - PAC init file - power sequencer, refdes: U5 (using lattice diamond programmer)
1x INIT#000801 - BIOS init file - refdes: J6 (using dediprog)
```

80200-0186-G00 Rev change from X200 to X300

3. Update PCB from 00101816-2020 to P305 fix I2C bug
4. Update PCB from 00101816-2020 to P305 fix I2C bug
5. Replace J19 from CRJ000021 to CRJ000023
6. Add E56S160 I2C series short resistor that connect to SPFX I2C bus. add D23/3 - E56020100057.
7. J203 RESET N - Remove PNP to avoid leakage. E502 - NC
8. Remove M15C Short Resistor - R244, R258, R296, A516.
9. Add R739, R737, R740, Q13. Add enable logic to VDDIO.
8. Changing I2C address from 0x20 to 0x18 (7bit) for P305 controller, the address is not in I2C register in M15C. I2C address is 0x20 (7bit) for P305 controller.
9. C155 had a 0805 part while the FP is 0603. Change to E5600076.

10. Change refdes: R245, R269, R276 to ER#0402274RFT.
11. Change refdes: R247, R274, R281 to ER#04021K96FT.
12. Remove refdes: R261, R263 and R264.
13. Replace R718 to ER#04028K06FT. Voltage divider (to 1V) for RGMII PHY TRST Pin.
14. Replace R717 to ER#040218KFT. Voltage divider (to 1V) for RGMII PHY TRST Pin.
15. Remove R2, R288 and R29.

**Note:**

ECO is missing: SCW000045 and MSP000033 (qty of 2 for each\)\from 80400-0179-G10, 80400-0180-G10 since they are missing data to be approved in agile. will be added in Beta ECO.

## Beta ECO, Version after

- ```

A. At R4040-0179-D10 Remove R4030-0182-D02 and add R4030-0190-D03.
B. At R4040-0180-D12 Remove R4030-0181-D02 and add R4030-0189-D02.
C. At R4040-0179-D00
Remove ICM005983 and add ICM001040.
D. At Medium R4040-0180-D00
Remove 1a FAN PM from the area behind DIMMs 23,34,35,36, and add FAN blockers PM. MAN0000160 installed FAN1
B. Change 2a FAN PM from MAN000101 to MLEFAN-40X042BPM at the area behind CPU (FAN3, FAN4).
C. Add 1a FAN PM from MAN0000160 behind of the power supply (FAN5).
D. Add 2a FAN blockers PM from MAN0000160 behind M2 and POE power supply (FAN4, FAN5).
E. At Small R4040-0179-D00
Remove 1a FAN PM from MAN0000160 from the area behind DIMMs 23,34,35,36, and add FAN blockers PM. MAN0000160 installed FAN1
C. Add 1a FAN PM from MAN000101 behind of the power supply of LV2, near power entry (FAN3 and 6).
D. Add 2a FAN blockers PM from MAN0000160 behind of the power supply of LV2, near power entry and the CPU.

```

4. Add 2x 2x 2x blocks p/n 888000100 behind K.2 and for power supply (1A14, 1A15).

Note: All FANS already replaced from P/FAN0000013 to MSL/FAN-40X40X28MM by ECO-007166.

4. Changes in 80200-0186-G00:
1. Add R734, R735 ER#04024K7FT
2. Remove R29,R31.

5. Changes in 80200-0186-G00:
1. Add R369, ER#04022K55FT.
2. Add C257, C274,ECC000005.

6. At 80300-0186-G00:
Remove INIT#000801 and add INIT#000817.

Note:

ORDER No.: SO# : 41 REV No. : R100 DATE: Sunday, December 10, 2018 Monday, June 10, 2019		80200-0186-G00 Version Control	<table border="1"> <tr> <th colspan="4">APPROVALS</th> </tr> <tr> <th></th> <th>NAME</th> <th>SIGN</th> <th>DATE</th> </tr> <tr> <td>CHECK</td> <td>Nader Y.</td> <td>Nader Y.</td> <td></td> </tr> <tr> <td>APPROV.</td> <td>David C.</td> <td>David C.</td> <td></td> </tr> <tr> <td>SHEET : 59</td> <td colspan="2">OF SHEETS : 59</td> <td></td> </tr> </table>	APPROVALS					NAME	SIGN	DATE	CHECK	Nader Y.	Nader Y.		APPROV.	David C.	David C.		SHEET : 59	OF SHEETS : 59			SILICOM Ltd. Connectivity Solutions A Member of RAD Group
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