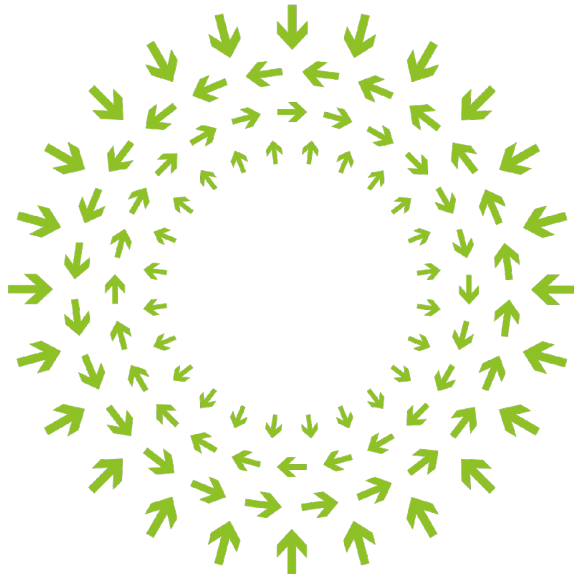




OPEN

Compute Project

Signal Conditioner Standard Footprint

1.0.0

Base Specification

Effective March 13, 2026

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Version History

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2. Compliance with OCP Tenets

2.1. Openness

The Signal Conditioner Standard Footprint Base Specification is an open standard based upon contributions and/or feedback from hyperscalers, component suppliers, and connector vendors. It provides all details required for an integrated circuit (IC) component supplier to design a compatible package and for a system designer to implement a compatible board/system. One of the objectives of contributing this specification to the industry is to facilitate the design of boards/systems utilizing signal conditioners, and to do so in such a way as to enable multi-vendor optionality.

2.2. Efficiency

The Signal Conditioner Standard Footprint drives efficiency in multiple ways. The modularity of its design—the ability to increase signal density by “tiling” multiple signal conditioner packages—reduces overall PCB area and enabled design flexibility. The carefully designed signal escape pattern and close compatibility with commonly used backplane connectors reduces the area and layout effort required to implement a complex system board design. The small body size also reduces PCB area and associated material cost.

2.3. Impact

The Signal Conditioner Standard Footprint Base Specification defines a standardized footprint for signal conditioners used in scale-up and scale-out AI infrastructure and related systems. The specification accelerates design cycles by leveraging pre-optimized, pre-studied signal breakouts while enabling multi-vendor optionality for more resilient supply chains.

2.4. Scale

The Signal Conditioner Standard Footprint supports signal rates up to 128 Gbaud (e.g., 256 Gbps PAM4) per lane and densities up to 48 SerDes lanes in a 33-mm x 22-mm area, enabling numerous high-lane-count and high-data-rate system topologies.

2.5. Sustainability

The Signal Conditioner Standard Footprint minimizes the device body size as much as possible while conforming to high-volume manufacturing (HVM) PCB design rules. Reducing body size reduces the materials needed to manufacture these devices and the associated system PCB—thus reducing the environmental impact associated with manufacturing these components.

3. Overview

AI scale-up fabrics consist of a large number of high-speed serial connections between accelerators and switches which often span a full rack or sometimes multiple racks. Closing the link budget at speeds of 100+ Gbps per lane often requires the use of signal conditioner devices—Retimers, Gearboxes, etc., collectively referred to as “Retimers” in this document. With hundreds of differential pairs routed on a single board and thousands routed within a rack, space optimization is a key consideration when implementing Retimers in a system. Package loss, crosstalk, route-ability, and other factors likewise play heavily into the ease or difficulty of incorporating such devices into a system. In the absence of a standard footprint, enabling multi-vendor optionality becomes difficult and requires complex re-design of large subsystems.

The purpose of this document is to establish a standard footprint and specification for Retimers which is optimized for such backplane applications. The goals include:

- Minimum body size and maximum signal density
- Compliance with standard high-volume manufacturing (HVM) PCB design rules targeting thick (e.g., 200 mil) PCBs
- Routing simplicity when interfacing with common backplane connectors
- Optimum signal integrity performance for speeds up to 256 Gbps PAM4
- Optimum power integrity performance
- Maximum design compatibility between vendors, while still supporting vendor-defined features
- Extensible to multiple scale-up protocols

In scope – This document specifies:

- Package body size dimensions
- Footprint and pinout, including high-speed pins, low-speed I/Os, flexible predefined power regions, and vendor-defined pins
- Package signal integrity (insertion loss and crosstalk) targets
- Multi-vendor board design enablement through BoM stuffing management

Out of scope – This document does not specify:

- Retimer feature set
- Programming model
- Start-up sequence
- Package Z height
- Maximum thermal design power (TDP)
- Maximum (peak) current per power supply rail
- Specification of vendor-defined pin functionality

The primary difference between this specification and similar documents (see [1]) are:

- This specification is protocol-agnostic and supports signal rates up to 256 Gbps PAM4
- This specification supports “tiling” multiple devices to improve PCB area utilization for high-signal-count system boards

4. Base Specifications

4.1. System Design Targets

The footprints specified in this document support the following PCB design rules which are geared towards a maximum PCB thickness of 200 mil. Thicker PCB designs may be possible but will require further analysis. The PCB design targets are summarized in Figure 4-1 and Table 4-1.

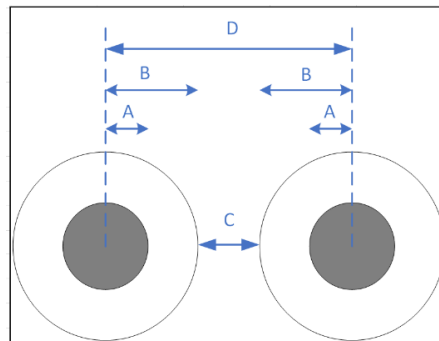


Figure 4-1: Via dimensions reference diagram

Table 4-1: System PCB design targets

Parameter		Value	Units	Comment
If via drill size = 8 mil (can support up to and including 200 mil thick PCB)				
PCB technologies supporting aspect ratio of 25:1				
A	Half of via drill size	4	mil	Via drill size = 8 mil
B	Half of minimum via pad size	8	mil	Pad size = 16 mil
C	Minimum clearance between via pads	7	mil	VIPPO process
D	Minimum via-to-via pitch	23	mil	$D = B + B + C$
If via drill size = 10 mil (can support >200 mil thick PCB)				
PCB technologies supporting aspect ratio of 20:1				
A	Half of via drill size	5	mil	Via size = 10 mil
B	Half of minimum via pad size	9	mil	Pad size = 18 mil
C	Minimum clearance between via pads	7	mil	VIPPO process
D	Minimum via-to-via pitch	25	mil	$D = B + B + C$

4.2. Body Size

Three body sizes are defined: 8-lane (x8) and 16-lane (x16) footprints—optimized for 8- and 16-column backplane connector implementations—and a 24-lane (x24) footprint—optimized for 12-column backplane connector implementations. The number of bi-directional lanes refers to the number of Tx and Rx pairs on each of the two sides of the Retimer, as shown in Figure 4-2.

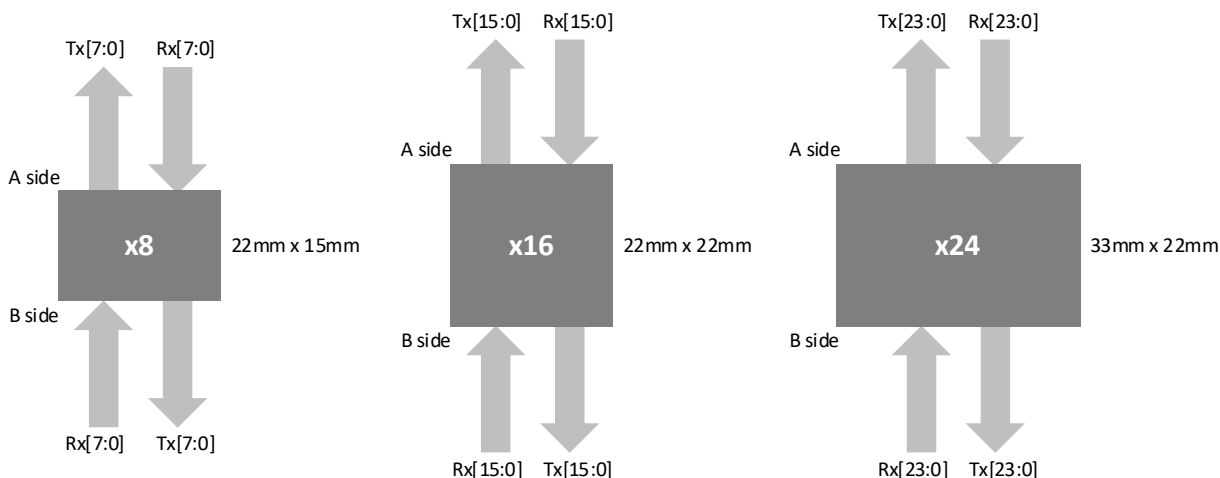


Figure 4-2: Bi-directional lane illustration for x8, x16, and x24

The package body sizes and other physical parameters are listed in Table 4-2.

Table 4-2: Package physical parameters

Bi-Directional Lane Count	Unit	8-Lane footprint	16-Lane footprint	24-Lane footprint
Body size x dimension	mm	22.00 ±0.05	22.00 ±0.05	33.00 ±0.05
Body size y dimension	mm	15.00 ±0.05	22.00 ±0.05	22.00 ±0.05
Total number of pins	-	536	792	1200
Number of SerDes lanes	-	16	32	48
Number of Rx differential pairs	-	16	32	48
Number of Tx differential pairs	-	16	32	48
Number of power pins	-	108	108	180
Number of differential REFCLK ¹ inputs	-	1	2	3
Number of low-speed/GPIO pins	-	48	44	40
Minimum pin pitch, center to center	mm	0.65 ±0.05	0.65 ±0.05	0.65 ±0.05
BGA ball diameter	mm	0.35 ±0.05	0.35 ±0.05	0.35 ±0.05
Recommended pad size	mm	0.35	0.35	0.35

¹REFCLK specifications are deferred to the corresponding interface specification (e.g., PCI Express, IEEE802.3, etc.).

4.3. Footprint

4.3.1. 8-Lane Bi-Directional Footprint

The 8-lane footprint with key dimensions is shown in Figure 4-3, annotated with key dimensions.

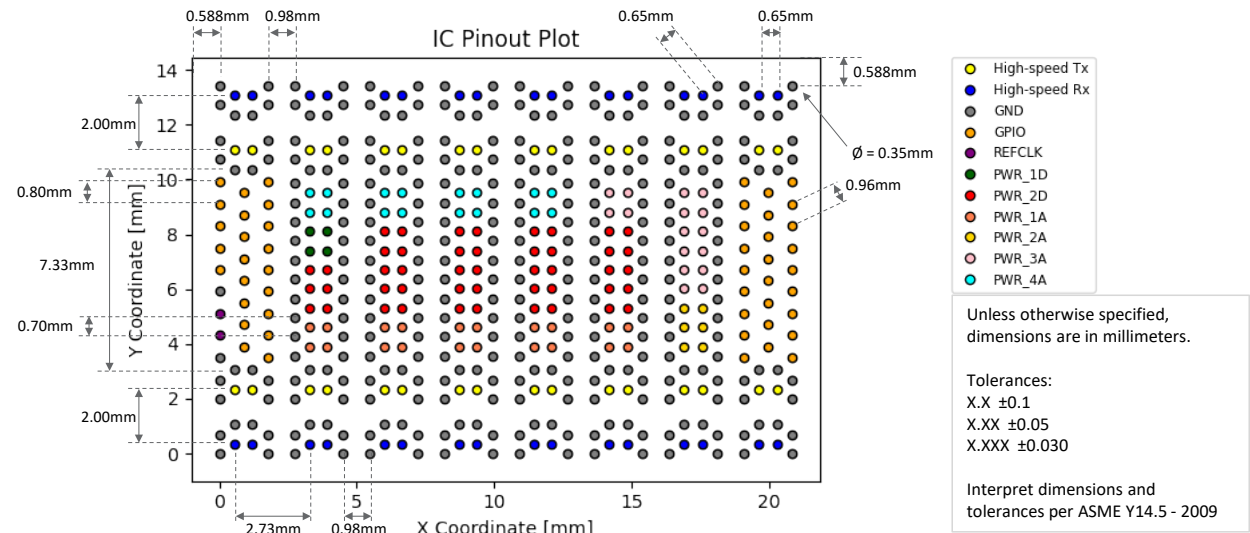


Figure 4-3: 8-Lane footprint (pin locations are to scale)

4.3.2. 16-Lane Bi-Directional Footprint

The 16-lane footprint is shown in Figure 4-4, annotated with key dimensions.

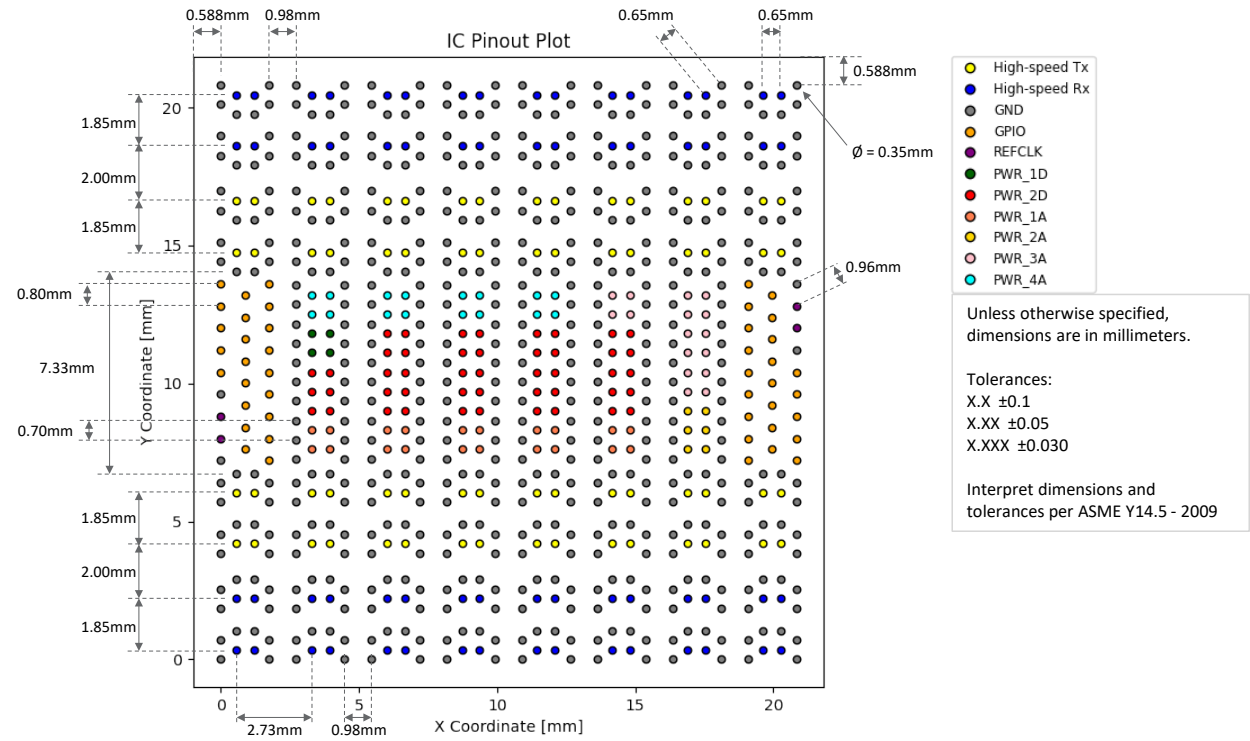


Figure 4-4: 16-Lane footprint with annotations (pin locations are to scale)

4.3.3. 24-Lane Bi-Directional Footprint

The 24-lane footprint is shown in Figure 4-5, annotated with key dimensions.

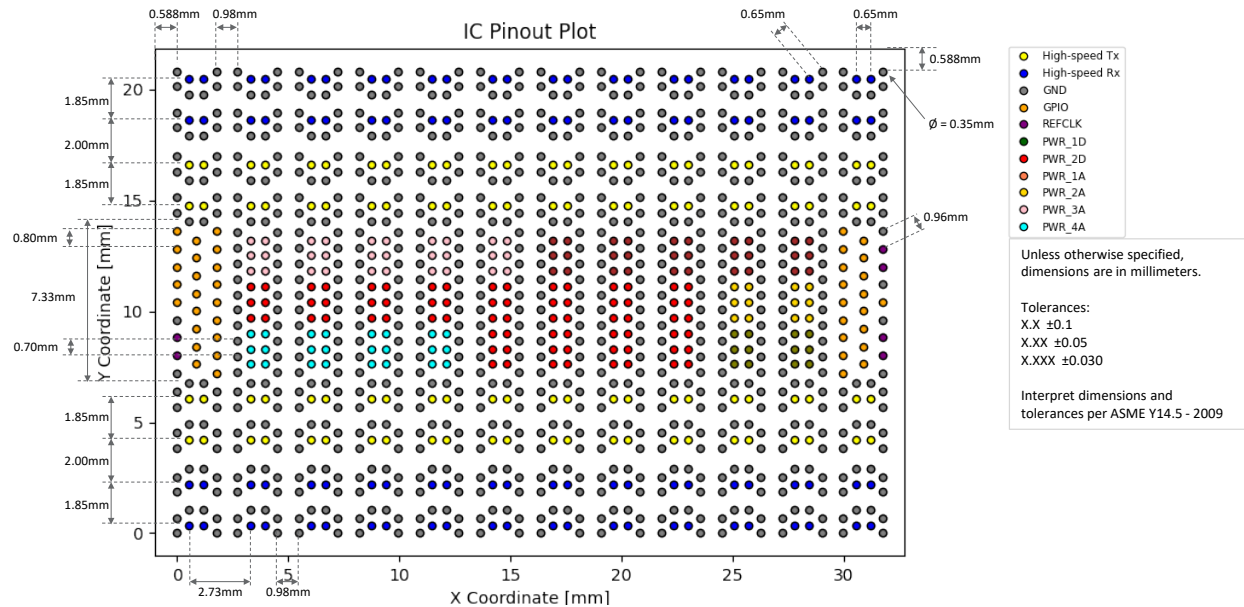


Figure 4-5: 24-lane footprint (pin locations are to scale)

4.4. High-Speed Signals

These footprints aim to maximize signal density while maintaining good signal integrity performance and route-ability to commonly used backplane connectors. Every high-speed differential pair is encased by a protective GND shield with adequate space provided to escape the high-speed signals into an inner-layer routing channel.

4.4.1. Differential Pair Geometry

The pitch between like differential pairs (e.g., Tx pair N to Tx pair N+1; or Rx pair N to Rx pair N+1) is 2.73 mm horizontally and 1.85 mm vertically, as shown in Figure 4-6. The pitch between unlike differential pairs (Tx pair to Rx pair) is 2.73 mm horizontally and 2.00 mm vertically, to provide extra isolation against near-end crosstalk, as shown in Figure 4-7.

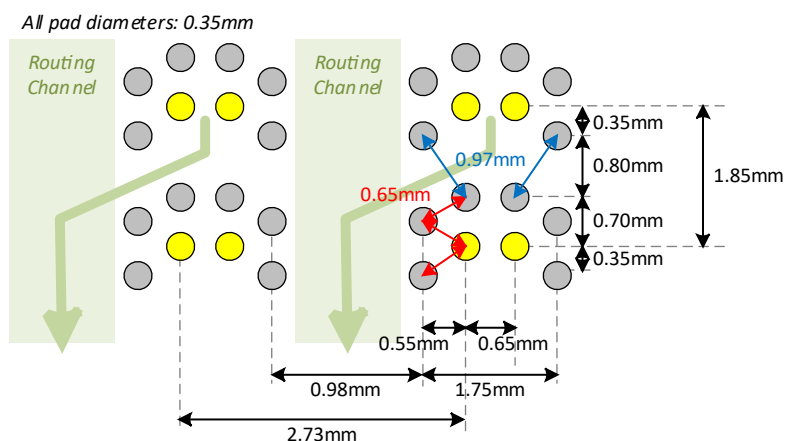


Figure 4-6: High-speed pin group dimensions for pairs of the same direction (not to scale; distances are center-to-center)

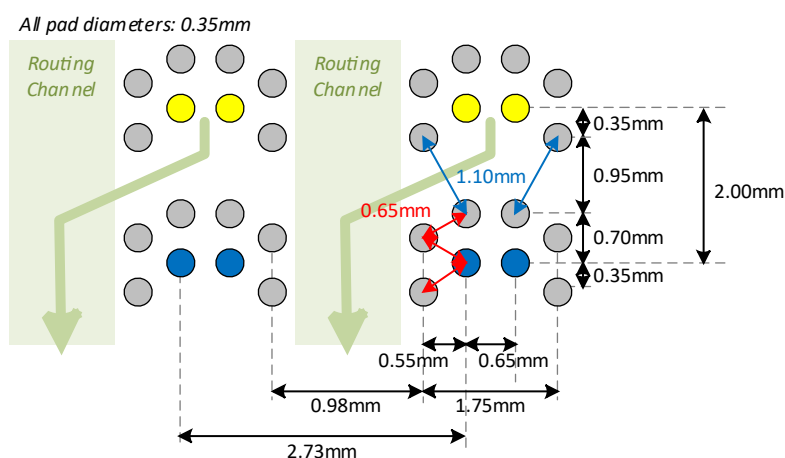


Figure 4-7: High-speed pin group dimensions for pairs in opposite directions (not to scale; distances are center-to-center)

4.4.2. Internal AC Coupling

In high-lane-count system board designs, placing series AC coupling capacitors on the board can be challenging. To address this design challenge, the high-speed signals in the Retimer shall be internally AC-coupled in a manner that is most appropriate for the target protocol and application, as summarized in Table 4-3. Internal AC coupling may be implemented on the silicon or on the package substrate.

Table 4-3: Internal AC coupling requirements

Target Protocol(s) or Application(s)	Required Internal AC Coupling	Comment
PCI Express	All high-speed transmit differential pairs	PCI Express and associated form factor specification (e.g., CEM) require system components to AC couple the transmit signals.
Ethernet, UALink	All high-speed receive differential pairs	The convention in Ethernet is the AC couple the receive signals.
Other applications where it is known <i>a priori</i> that internal AC coupling is not required	None	If a Retimer device is targeted for a specific application where it is known <i>a priori</i> that AC coupling capacitors are either unnecessary or will be implemented elsewhere in the system, then no internal AC coupling is required.

In all cases, the Retimer's documentation (e.g., datasheet or platform design guide) shall clearly describe the manner of internal AC coupling or no internal AC coupling, as the case may be.

4.4.3. High-Speed P/N Skew

The high-speed differential pair and surrounding ground pin geometry allows for inner-layer trace escapes which are fully symmetric between P and N. In practice, the length mismatch between P and N when escaping the pin field can be kept within 0.5 mil in the layout. The PCB routing example provided (see Section 4.11) illustrates this fully-symmetric escape.

4.5. Power Pin Usage

The power pins are arranged in the center of the footprint in such a way as to not impede the high-speed routing channels passing through the pin field. Six power "islands" are established to support up to six unique power rails: Four analog supplies (PWR_1A, PWR_2A, PWR_3A, and PWR_4A), one digital I/O supply (PWR_1D), and one core digital supply (PWR_2D). Analog supplies are defined as supplies which typically require a ferrite bead filter to achieve minimal power supply noise. A digital I/O supply is defined as a supply which determines the signaling voltage (e.g., 1.8 V, 1.2 V, etc.) of the low-speed digital I/O interfaces (e.g., I2C, SPI, JTAG, etc.). A core digital supply is defined as a supply which generally powers digital circuits and is therefore less sensitive to noise than analog circuits and does not require a ferrite bead filter. It is not practical to pre-define the voltage and current requirements for each rail, since different IC solutions targeting different data rates and implemented in different process technologies will have different voltage and current requirements.

Not all IC implementations will require six unique voltage rails, so in such cases the rails may be consolidated to simplify system board design. For example, a specific IC implementation may only require three unique power supply voltages. The IC supplier will then designate which

supply islands—PWR_[4:1]A and PWR_[2:1]D—map to which of the three unique voltages. The system designer can then implement a board design with three regulators driving the noted power island groupings.

Figure 4-8 is illustrative of the placement of the power islands for the x16 footprint, the contiguous planes that can connect them, and the accommodation of high-speed routing channels in between. Multiple layers can be used to create larger planes.

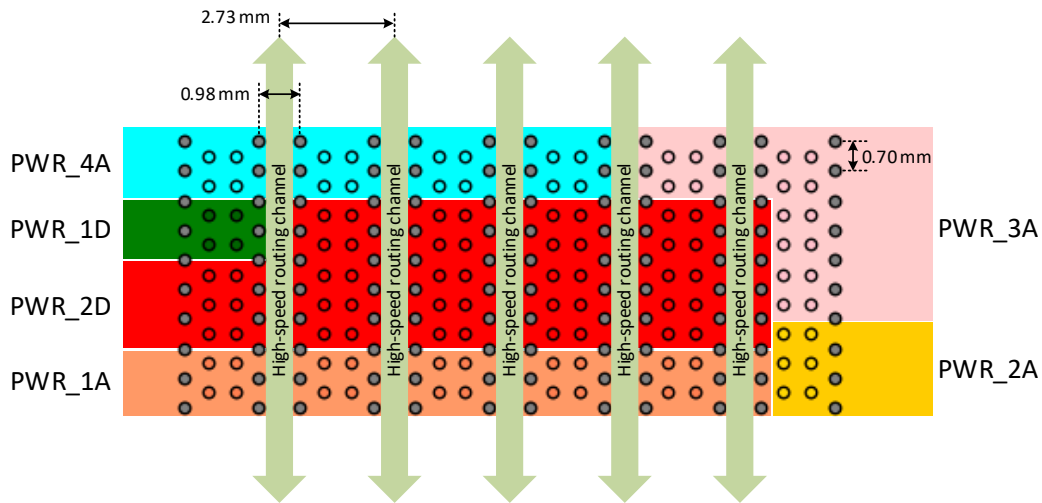


Figure 4-8: Example power pin "islands" for 16-lane footprint

The allocation of BGAs for the six unique power rails is given in Table 4-4.

Table 4-4: Power pin allocation

Power rail	Description	Number of BGAs allocated		
		x8 footprint	x16 footprint	x24 footprint
GND	Ground	120 ¹	120 ¹	200 ¹
PWR_1A	Serdes analog high-voltage supply	20	20	28
PWR_2A	Serdes analog low-current supply	6	6	12
PWR_3A	Serdes analog medium-voltage supply	16	16	26
PWR_4A	Serdes analog low-voltage supply	16	16	24
PWR_1D	IO supply (VDDIO)	4	4	4
PWR_2D	Serdes/Core digital supply (VDDD)	46	46	86

¹These numbers represent GND pin allocation in the center "power" region. Additional GND pins are located throughout the pinout.

4.6. Low-Speed and General-Purpose I/Os

The footprint includes two groups of low-speed I/Os with 52 total pins. The spacing between low-speed I/O pins is purposefully designed to facilitate multi-layer breakout of the I/O signals and to minimize disruptions to inner power and ground planes.

The 0.8-mm vertical spacing and the 0.875-mm horizontal spacing allow for the outer two columns to be escaped on the surface layer (microstrip), while the inner-most column can be escaped with micro vias on an inner layer. The advantage of this approach is that it does not introduce signal vias adjacent to the high-speed routing channel which runs vertically through the pin field, thus optimizing high-speed signal integrity. In addition, the single column of micro vias does not impede the routing of power into the center of the pin field, thereby optimizing power integrity.

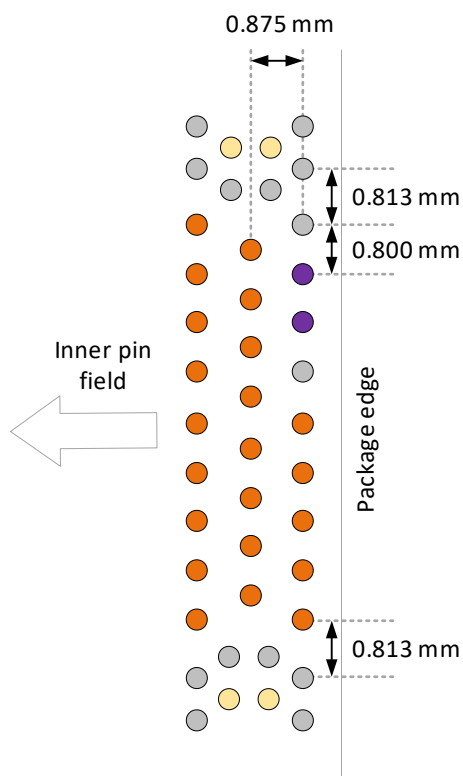


Figure 4-9: GPIO signal group between high-speed differential pairs (replicated on East and West sides of the footprint)

Table 4-5 summarizes the list of low-speed and general-purpose I/O functions which, if **optionally** implemented in a given device, shall be mapped to the designated pin for maximum commonality.

Table 4-5: Low-speed and general-purpose signals/functions

Pin Name	Type	Description
ADDR1	I	SMBus/I2C/I3C/MDIO address strap
ADDR2	I	SMBus/I2C/I3C/MDIO address strap
ADDR3	I	SMBus/I2C/I3C/MDIO address strap
DN	I/O	USB port DN
DP	I/O	USB port DP
I2CM_SCL	I/O	I2C controller port clock
I2CM_SDA	I/O	I2C controller port data
INT_N	O	Open-drain interrupt output
JTAG_TCK	I	JTAG test clock
JTAG_TDI	I	JTAG test data input
JTAG_TDO	O	JTAG test data output
JTAG_TMS	I	JTAG test mode select
JTAG_TRST_N	I	JTAG test reset, active low
LINK_RESET_N	I	Link-level logical reset, active low ¹
MDC	I/O	MDIO clock
MDIO	I/O	MDIO data
REFCLKN1	I	Reference clock 1 ²
REFCLKP1	I	Reference clock 1 ²
REFCLKN2	I	Reference clock 2 (for x16 and x24 implementations only) ²
REFCLKP2	I	Reference clock 2 (for x16 and x24 implementations only) ²
REFCLKN3	I	Reference clock 3 (for x24 implementations only) ²
REFCLKP3	I	Reference clock 3 (for x24 implementations only) ²
RESET_N	I	Full chip reset, active low
SCL	I/O	I2C target port for management, clock
SDA	I/O	I2C target port for management, data
SPI_CS_N	O	SPI controller port chip select output
SPI_MISO	I	SPI controller port input data
SPI_MOSI	O	SPI controller port output data
SPI_SCLK	O	SPI controller port SCLK
VD	I/O	Vendor-defined I/O

¹In PCI Express applications, this is the fundamental PCIe® Reset (PERST#)

²Reference clock inputs to the Retimer component shall comply with the specifications in the applicable standard: PCI Express®, Ethernet, UALink®, etc.

4.7. Board Routing

The horizontal pitch of the high-speed signal pairs, 2.7 mm, aligns closely with commonly used backplane connectors' column pitch. Backplane connectors come in different row and column configurations. The x8 footprint aligns well with 8-column, 4-row configurations. The x16 footprint aligns well with 8-column and 16-column configurations. The x24 footprint aligns well with 12-column configurations. All footprints support “tiled” placement wherein the high-speed signals from one device can route entirely underneath another device, unimpeded by vias. This enables the use of multiple devices to support larger row count backplane connectors while placing all devices in the “shadow” of the connector. This is illustrated in Figure 4-10.

Signal Conditioner Standard Footprint

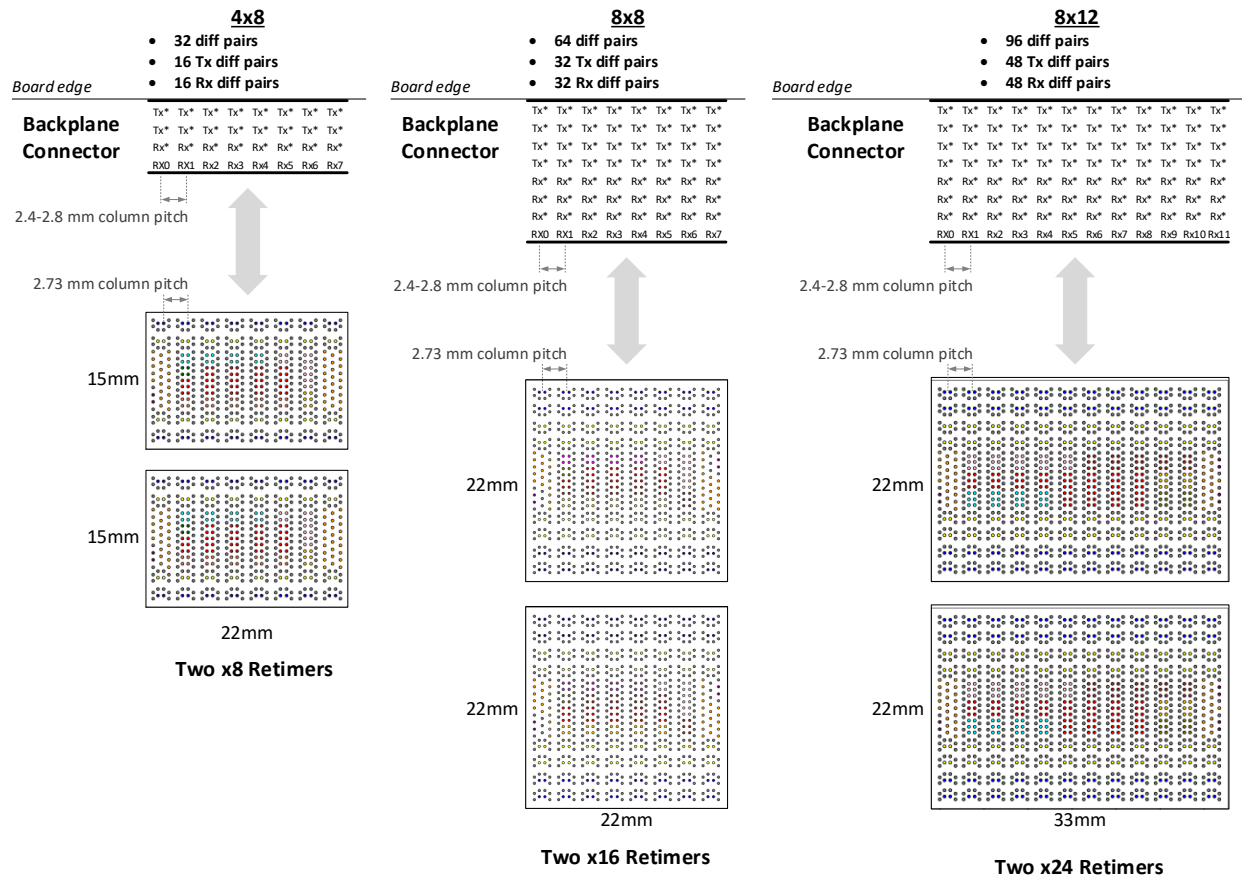


Figure 4-10: Example placement of "tiled" devices in line with backplane connectors

Figure 4-11 shows an example PCB routing of a "tiled" implementation with two x16 devices wherein 32 Tx differential pairs and 32 Rx differential pairs are routed to a backplane connector (not shown) in eight layers. Refer to the example PCB board file (sc_standard_footprint_pcb_routing_example_x16.brd).

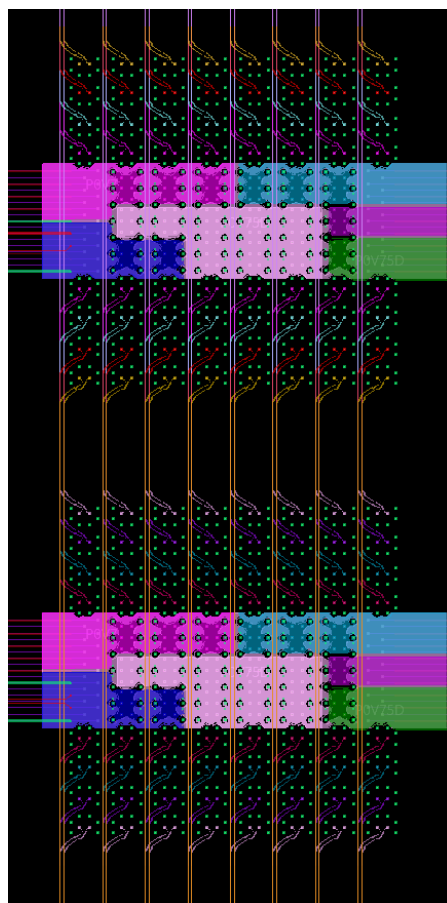


Figure 4-11: Example board layout showing two x16 devices in a "tiled" configuration

4.8. Signal Integrity

4.8.1. PCB High-Speed Breakout

There are generally two strategies which can be employed to breakout the high-speed differential pairs: (1) a via-in-pad plated over (VIPPO) with 1:1 via-to-pad arrangement and (2) an offset via arrangement. Figure 4-12 and Figure 4-13 illustrate these two strategies.

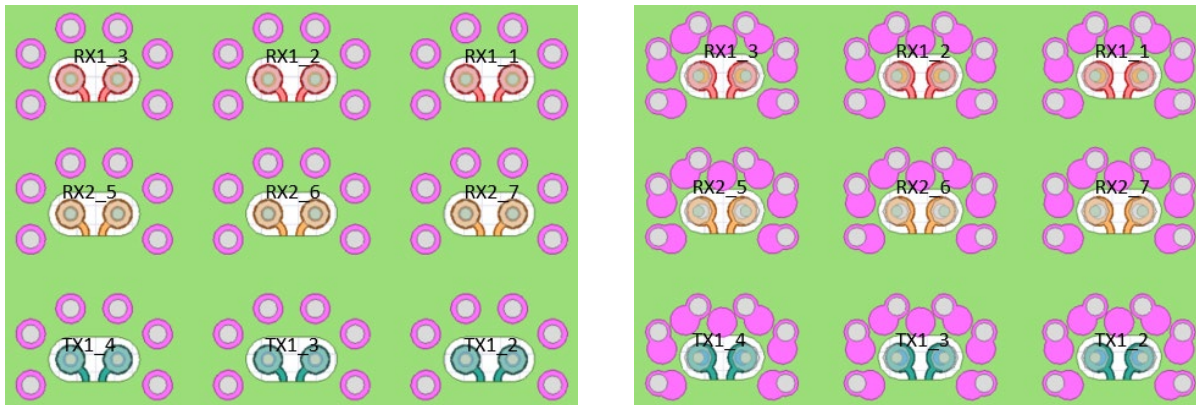


Figure 4-12: 1:1 VIPPO arrangement (left) vs. offset via arrangement (right)

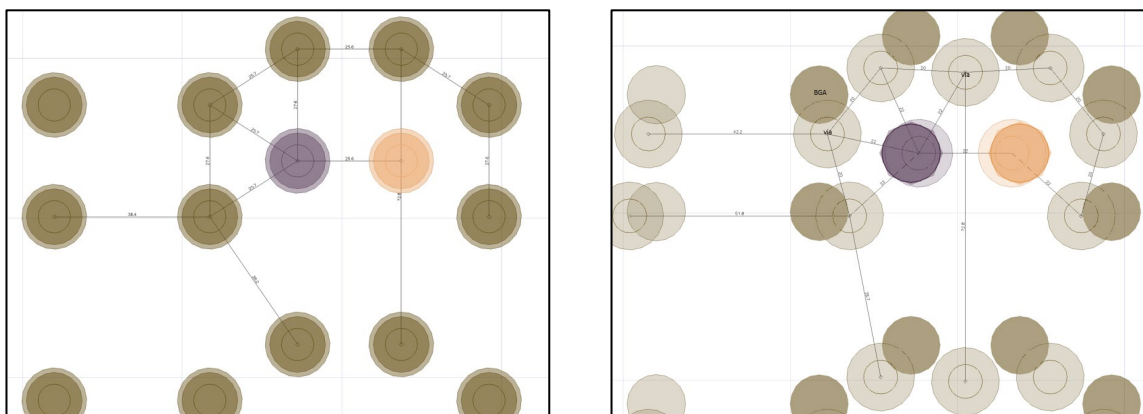


Figure 4-13: Zoomed-in view of 1:1 VIPPO arrangement (left) vs. offset via arrangement (right)

The offset via approach yields better signal integrity performance, especially in terms of crosstalk. Example crosstalk performance for five-aggressor FEXT and three-aggressor NEXT is summarized in Table 4-6. Actual results may vary depending on stackup, via drill size, drill-to-metal spacing, etc.

Table 4-6: Example high-speed signal breakout crosstalk performance

Stackup	Parameter	1:1 VIPPO arrangement			Offset via arrangement		
		DC to 26.5625 GHz	DC to 32 GHz	DC to 53.125 GHz	DC to 26.5625 GHz	DC to 32 GHz	DC to 53.125 GHz
50 mil (shortest via: 20 mil)	FEXT	-78 dB	-75 dB	-65/-74 dB ¹	-88 dB	-85 dB	-75 dB
	NEXT	-82 dB	-80 dB	-65/-72 dB ¹	-94 dB	-90 dB	-75 dB
130 mil (shortest via: 100 mil)	FEXT	-64 dB	-62 dB	-52/-66 dB ¹	-80 dB	-76 dB	-66 dB
	NEXT	-76 dB	-76 dB	-68/-76 dB ¹	-88 dB	-88 dB	-70 dB
200 mil (shortest via: 170 mil)	FEXT	-60 dB	-58 dB	-48/-58 dB ¹	-74 dB	-72 dB	-60 dB
	NEXT	-74 dB	-72 dB	-60/-68 dB ¹	-88 dB	-84 dB	-70 dB

¹Results shown for two cases: A/B. A is 8 mil signal via with 8 mil GND via; B is 8 mil signal via and 10 mil GND via (better crosstalk performance).

4.8.2. Package Substrate High-Speed Breakout

To facilitate channel budgeting and the design of system boards which may utilize multiple vendors' solutions, Table 4-7 specifies the maximum insertion loss from BGA ball to die bump allowed in a package implementation.

Table 4-7: Package high-speed signal insertion loss limits

Pins	Package Insertion Loss Limit (Depends on Max Rate Supported)			
	Max rate = 106.25 Gbps PAM4	Max rate = 128 Gbps PAM4	Max rate = 212.5 Gbps PAM4	Max rate = 256 Gbps PAM4
	DC to 26.5625 GHz	DC to 32 GHz	DC to 53.125 GHz	DC to 64 GHz
A_RX*	<1.75 dB	<2.00 dB	<2.75 dB	<3.25 dB
B_RX*	<1.75 dB	<2.00 dB	<2.75 dB	<3.25 dB
A_TX*	<1.50 dB	<1.75 dB	<2.25 dB	<2.75 dB
B_TX*	<1.50 dB	<1.75 dB	<2.25 dB	<2.75 dB

4.9. Power Integrity

The power integrity performance of this footprint will depend heavily on board stackup, copper thickness, and other parameters. The pinout allows for power to be routed into the center region from the sides with minimal blockage. The wide (0.8-mm) spacing of the GPIO pins helps to minimize power blockage.

4.10. Thermals and Mechanicals

The thermal performance of this footprint will depend heavily on package material selection, lid style, thermal interface material, and other variables. The dense array of power and ground pins and corresponding vias in the center of the pin field will help with die-to-board thermal dissipation.

The Z height of this standard footprint package is not specified.

4.11. Supplemental Materials

Table 4-8 lists the supplemental documents that accompany this specification.

Table 4-8: Supplemental Material

File/Folder	Description
sc_standard_footprint_pinout_x8_v1.0.0.xlsx	x8 pinout including pin names, numbers, coordinates, and pad sizes
sc_standard_footprint_pinout_x16_v1.0.0.xlsx	x16 pinout including pin names, numbers, coordinates, and pad sizes
sc_standard_footprint_pinout_x24_v1.0.0.xlsx	x24 pinout including pin names, numbers, coordinates, and pad sizes
sc_standard_footprint_pcb_routing_example_x16_v1.0.0.brd	x16 pinout routing example showing tiled placement
sc_standard_footprint_pcb_breakout/*_v1.0.0.s32p	sNp touchstone files of example board breakout for a 200 mil stackup
sc_standard_footprint_pkg_substrate_breakout/*_v1.0.0.s36p	sNp touchstone files of example package substrate breakout.

4.12. Compliance

This section is the checklist for the consumers of this specification to adhere to in order for them to declare they comply to the requirements.

Table 4-9: Base specification compliance table

Item	Requirement	Reference	Mandatory
1	Package body size conforms to x8, x16, or x24 body size noted in this specification.	Table 4-2	Yes
2	Package BGA ball diameter conforms to the diameter noted in this specification.	Table 4-2	Yes
3	Package pinout—pin functions and pin coordinates—conforms to the example pinout XLSX files noted in this specification. Pins noted as “vendor-defined” or “vendor-specific” do not have a pre-defined function and are therefore not subject to this requirement.	Table 4-8	Yes
4	Power pin assignment shall map up to six unique supply voltages to the six defined power pin groupings: PWR_[4:1]A and PWR_[2:1]D. If fewer than six unique supply voltages are needed in a particular implementation, then power islands may be merged accordingly.	Section 4.5	Yes
5	The component’s documentation (e.g., datasheet) must note whether the high-speed signals are AC-coupled internally (either on-package or on-die) or not.	Section 4.4.2	Yes
6	If the component implements the optional low-speed and general-purpose I/O functions listed in Table 4-5, then it must place those functions in the corresponding pin locations noted in this specification.	Table 4-5	Yes
7	The package insertion loss, from die bump to package BGA ball, must comply with the insertion loss limits noted in this specification.	Table 4-7	Yes

4.13. References

[1] Intel. “PCI Express 6.X Retimer Supplemental Features and Standard BGA Footprint.” 21 Feb. 2025, <https://www.intel.com/content/www/us/en/content-details/763884/pci-express-6-x-retimer-supplemental-features-and-standard-bga-footprint.html>