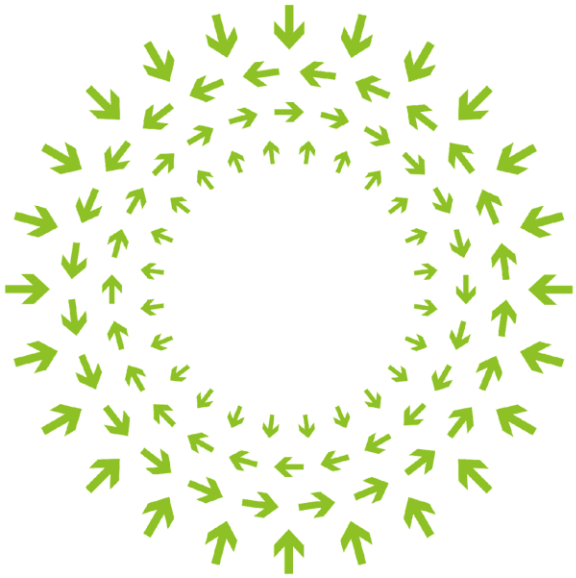

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Shasta HW System Specifications

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Authors:

Architecture: Gopa Parameswaran

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1. License

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1) The above license does not apply to the Appendix or Appendices. The information in the Appendix or Appendices is for reference only and non-normative in nature.

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1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

Molex

Quanta

List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

Molex

Quanta

2. Compliance with OCP Tenets

Please describe how this Specification complies to the following OCP tenets. Compliance is required for at least three of the four tenets. The ideals behind open sourcing stipulate that everyone benefits when we share and work together. Any open source project is designed to promote sharing of design elements with peers and to help them understand and adopt those contributions. There is no purpose in sharing if all parties aren't aligned with that philosophy. The IC will look beyond the contribution for evidence that the contributor is aligned with this philosophy. The contributor actions, past and present, are evidence of alignment and conviction to all the tenets.

2.1. Openness

Shasta Modular chassis is designed to go with Open rack V3. Specification is developed in collaboration with Quanta and Molex. Chassis manager in Shasta is built with SC-SCM module which is already released to OCP, There are no other proprietary hardware or software component involved in this design.

2.2. Efficiency

Shasta reduces the time it takes to deploy devices in Open rack V3. Some of the use cases include deployment of disaggregated network attached devices in data centers. Disaggregation helps to reduce CapEx, deploying these devices in a modular chassis that supports hot swap helps DC operators to reduce OpEx as well.

2.3. Impact

Currently most of the devices getting deployed in data centers are general purpose CPUs and storage nodes. In future there is going to be many domain specific devices like accelerators will be deployed in DCs. Developing PCIe cards to go into standard servers is one of the fastest ways to deploy them. This has power and cooling challenges and does not support hot swap. Shasta modular chassis address these concerns and enable faster deployment of devices in Open Rack V3, widely accepted OCP rack.

2.4. Scale

Chassis is developed in collaboration with large DC hardware suppliers Molex and Quanta. We have component vendors like FPGA accelerators, Video codecs evaluating Shasta as platform to deploy their devices. There are other inference device vendors with PCIe cards evaluating

Shasta as platform to deploy their PCIe cards (with jacket card) for faster deployment with hot swap support.

2.5. Sustainability

Shasta chassis enables deployment of devices like accelerators into data center by developing modules instead of a standalone system. This will enable reuse of good amount of software and hardware developed for data center. With serviceability reduced to conveniently replacing a module without impacting the rest of the modules and chassis, blast radius of failure is reduced to an individual module for most of the failure cases.

In the case of Shasta, the power budget of 4RU is aggregated and re-allocated to various modules. This will enable us to develop better power management and power budgeting with enhanced device utilization.

3. Version Table

Date	Version #	Author	Description
20220908	1.0	Alan Liu Gopa Parameswaran	Initial Release
20230417	2.0	Gopa Parameswaran	Updated with OCP team feedback.

4. Scope

This document defines the technical details for following types of specification:

- base specification for an intended physical.

Any supplier seeking OCP recognition for a hardware product based on this Specification must be 100% compliant with any and all features or requirements described in this Specification.

Examples of the types of Specs are given for reference only and can be found in the OCP Contribution Portal:
De-facto Standard - OpenHBI Spec
Server - Mt Jade Server
Network - Wedge 400
Rack- Open Rack V2.2
Storage - Datacenter NVMe SSD Spec
Cards - NIC3.0
Revision Update - Minipack2
Version Update - Minipack1 V2.0

Examples of <hardware product type> are for reference only and can be found in our OCP Marketplace:
Card: NIC2.0 Adapter Card
Server: Tioga Pass Server
Gateway: Disaggregated Cell Site Gateway
Rack: ORv2
Edge Server: Airframe Open Edge 1U Server
Storage Server: Goose Lake JBOD
Modules: Optical Transceiver
GPU: Yosemite V2

5. Overview

Shasta chassis is designed to support deployment of hot swappable modules in Open rack V3. Modules are the faster way to deploy devises in open rack relative to blades because of the HW & SW development effort and validation effort. PCIe cards installed in server blades are one way to deploy devices as modules. But this approach has power and cooling challenges and also does not support hot swap. Shasta addresses these concerns; with jacket card we can even deploy PCIe cards with hot swap support.

More and more application specific devices like accelerators, video transcoders etc are coming up in industry. Data centers can benefit from an eco-system that supports faster deployment of these devices into currently used platforms like Open rack V3. Inside Shasta chassis, modules can get significant airflow without any significant obstruction in air flow path unlike PCIe slots in server, we could even power and air cool 700W devices in certain configuration. All these modules can be hot swapable.

We are contributing Shasta specification as first phase, this will also cover significant amount of design details as given in following sections. Later we will be contributing the design files and firmware as we complete design and validation.

6. Rack Compatibility

This specification defines the design details for Shasta, an infrastructure system for OpenRack V3. Shasta will function as modular chassis for OpenRack V3.
Shasta contains 8 PMs (Processing Module), 1 CMM (Chassis Management Module), 1 PDB and 2 fan boards. The head-node (LS – Local Server) is connected to the CMM over Gen4 x8 PCIe cable. The CMM connects to the PM modules over cable backplane. In a typical deployment 2 redundant TOR switches could be connected to the head-node and each of the PMs in Shasta chassis.
CMM has a DC-SCM module for chassis management and PCIe switch to extend PCIe connectivity to PMs. There is a power harness in rear side of chassis which provides the power connection to rack's power bus bar and uses RJ45 connector in front of CMM for interfacing the Shasta to the management switch.
There are two fan boards in Shasta which provide the signals and power connection for a total of 8 fans (each 4 fans). The fan boards may vary depending on design.

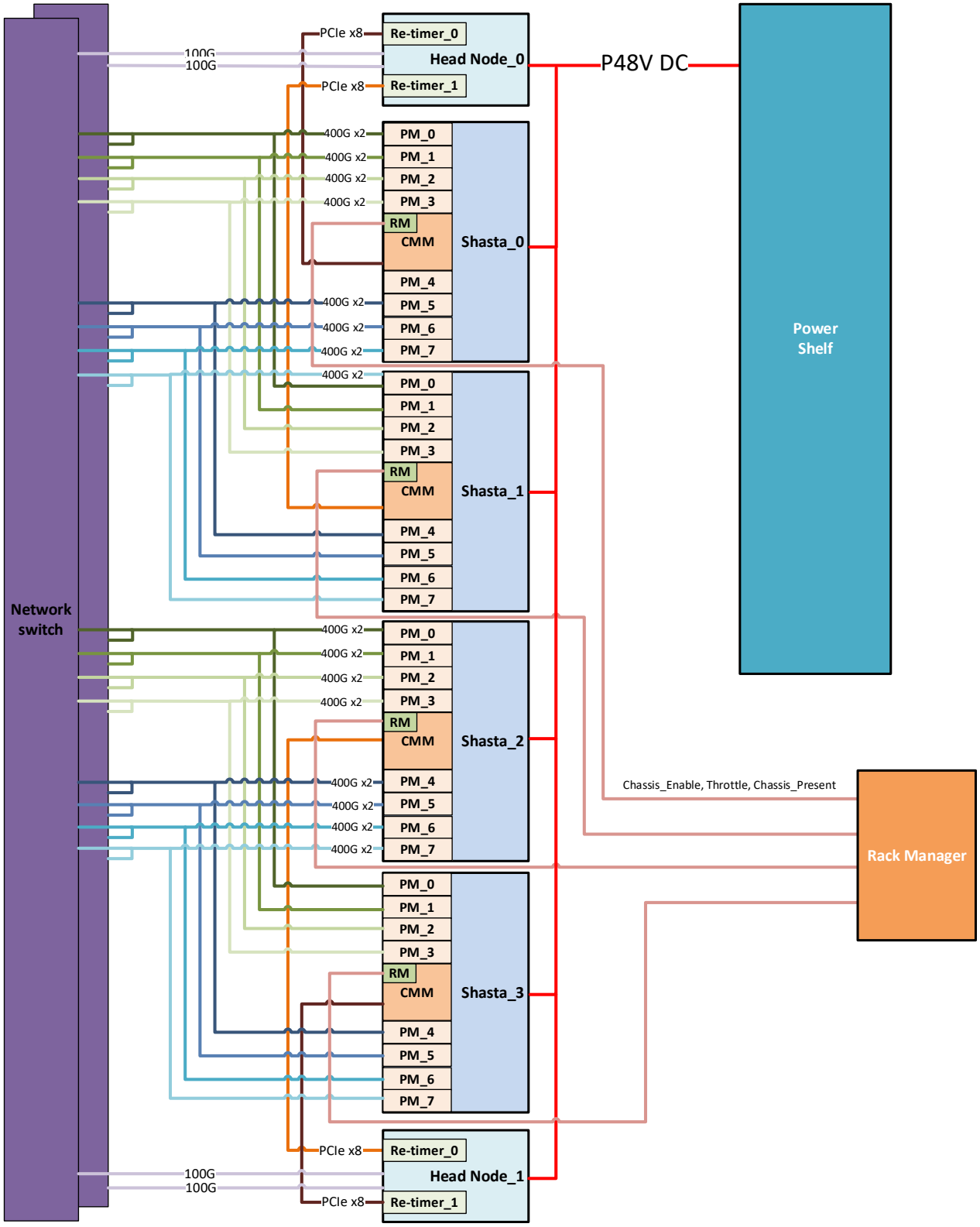


Figure 1 Detailed Rack Level Block Diagram

6.1. Chassis installation in Rack

6.1.1. Step1: Install the inner rail bracket on the system chassis

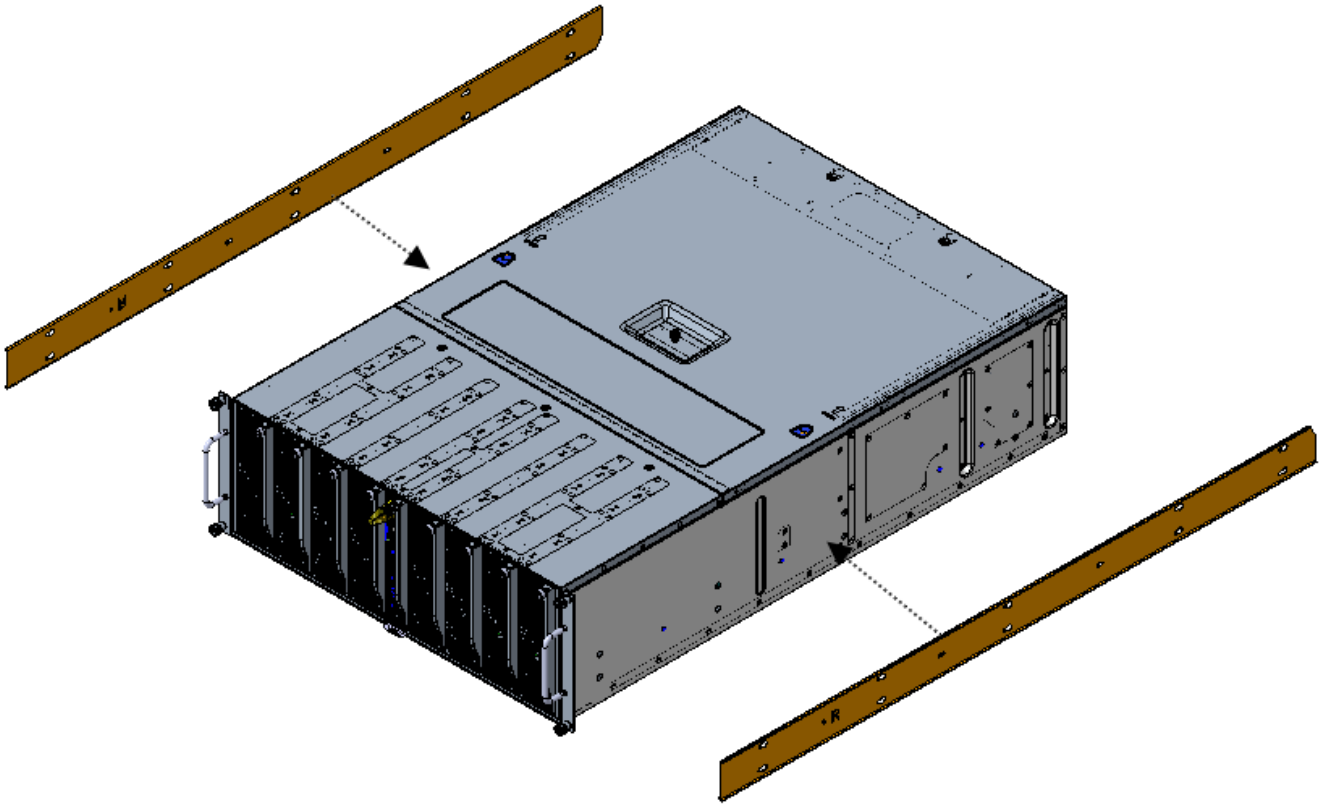


Figure 2 Chassis installation Step 1

6.1.2. Step2: Put the system and align to the outside rail of rack

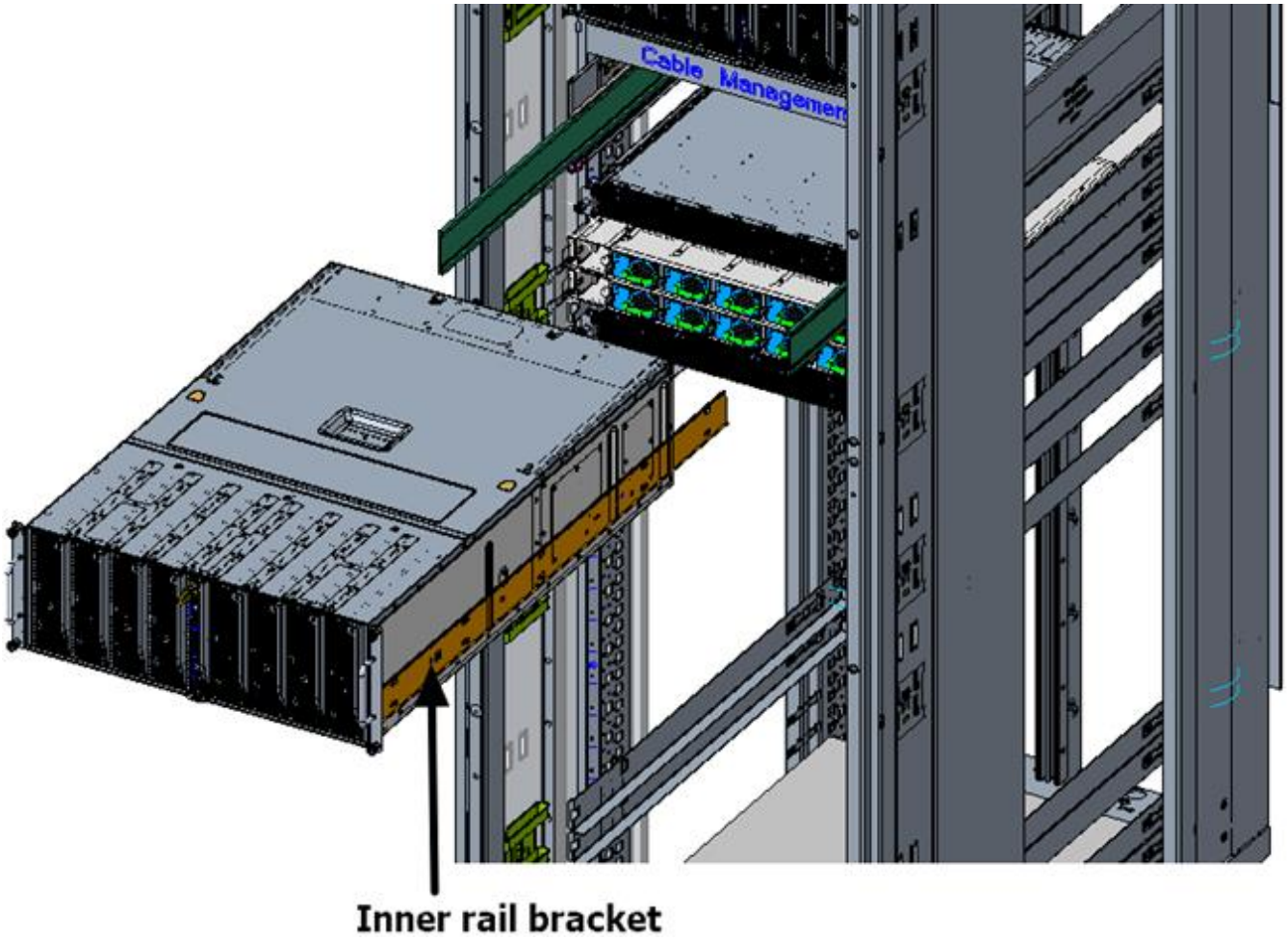


Figure 3 Chassis installation Step 2

6.1.3. Step3: Push and slide the system in position

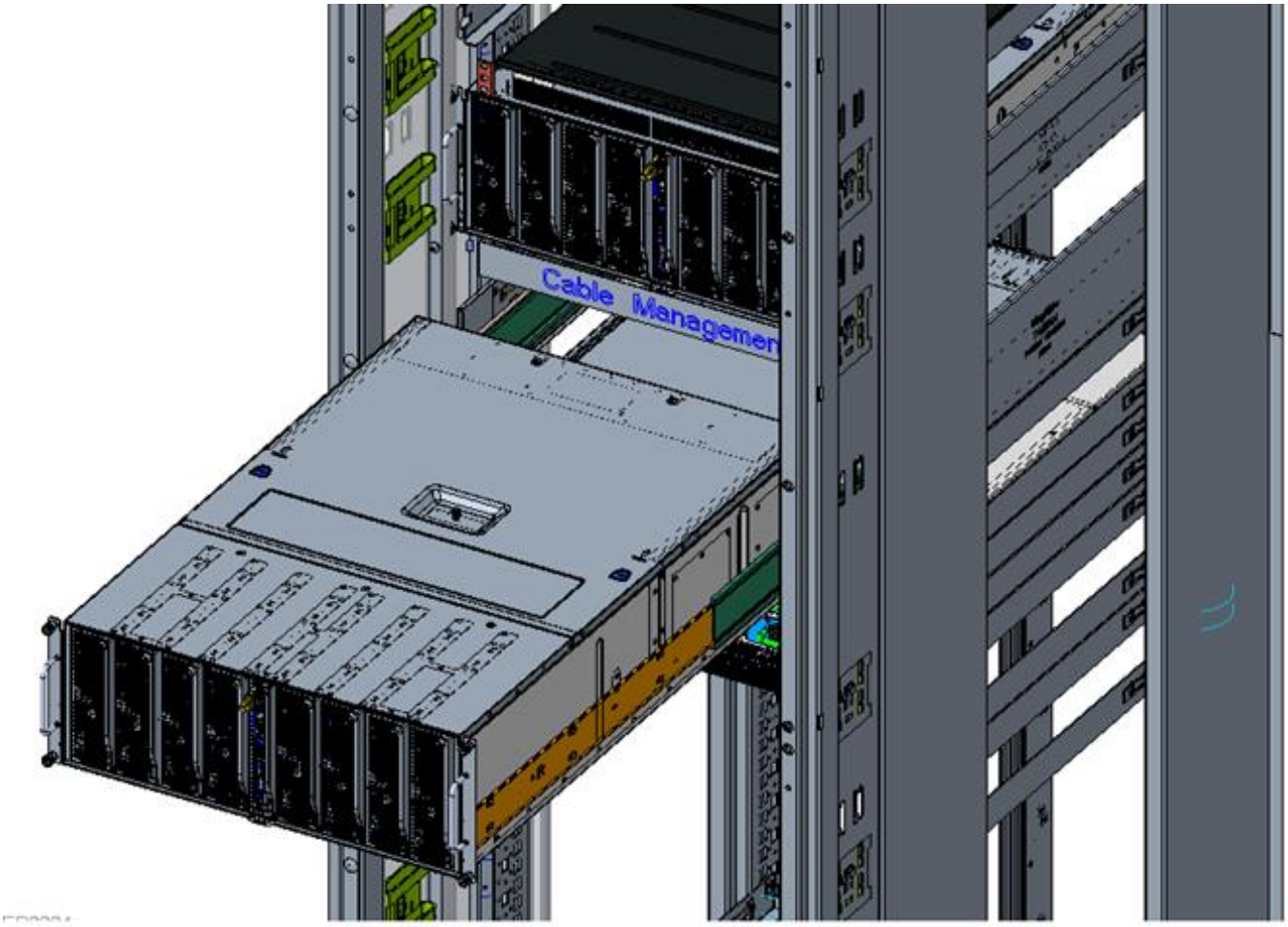
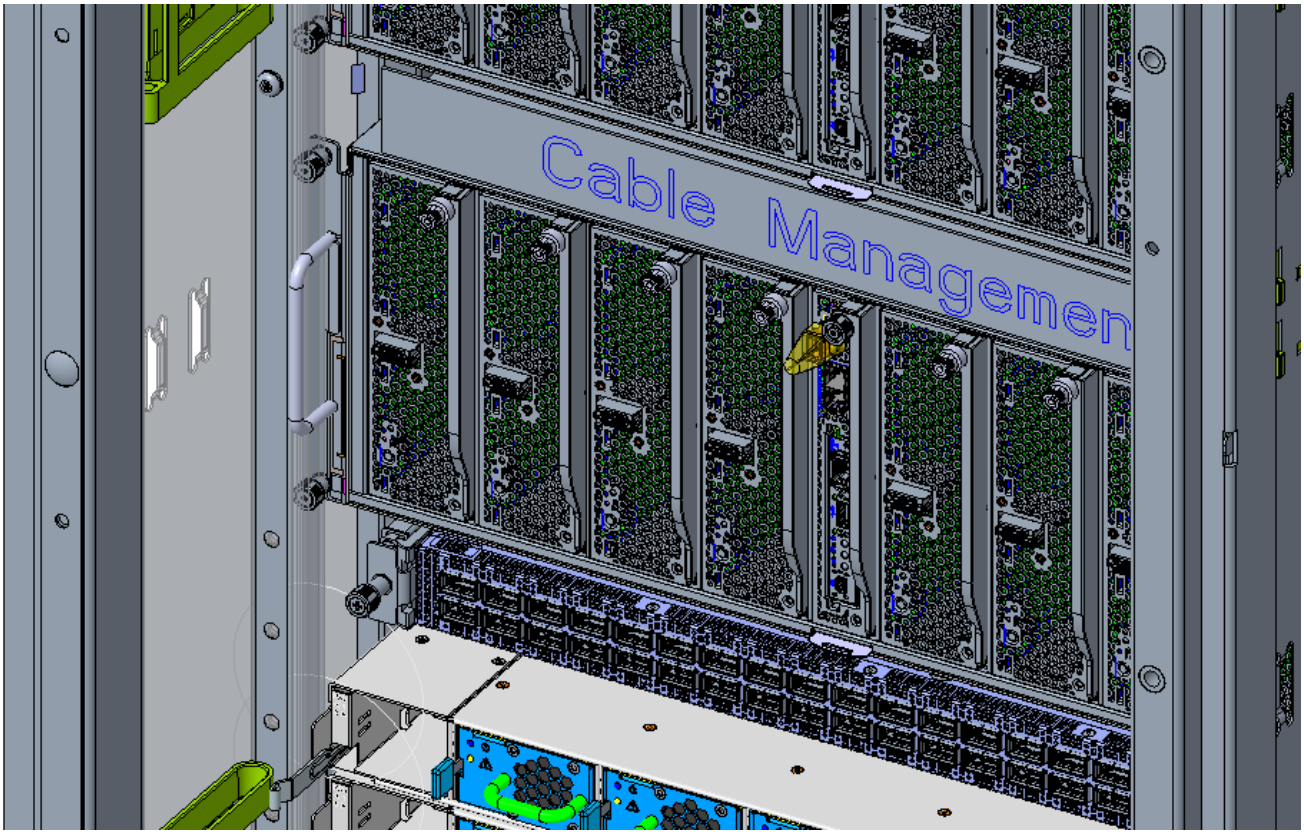


Figure 4 Chassis installation Step 3

6.1.4. Step4: Secure system and fasten 4 thumb screws to the rack


Cable Managemen

ad

Figure 5 Chassis installation Step 4

7. Physical Specifications

The system topology for Shasta includes one CMM, 8 PMs (depending on solution and power budget, the PM q'ty may be different), one PDB, two fan boards and eight fan modules. The system topology is shown in Figure 6. (Dotted line is connected to second Shasta chassis (Shasta_1))

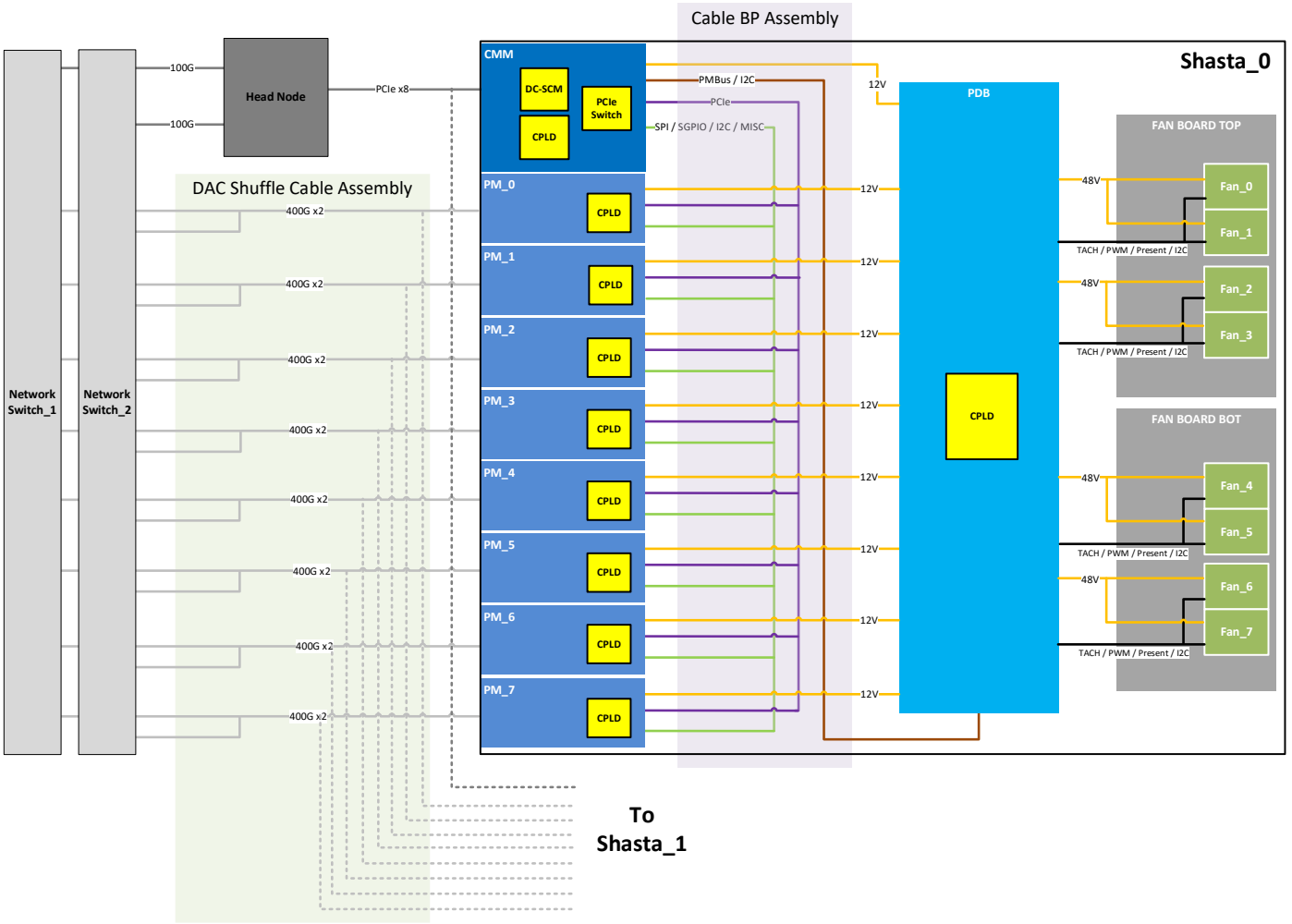


Figure 6 Shasta System Topology

7.1. CMM

The CMM includes the following major subsystems that are detailed in the sections below:

- DC-SCM: DC-SCM v1.0

- PCIe Switch: Broadcom, PEX88024 or PEX88048
- CPLD: Lattice, LCMXO3LF-4300C-5BG256C
- Local Clock: Silicon, SI52202-A01BGMR
- Clock MUX: Renesas, 9ZML1245AKILFT
- Sequencer: Maxim, MAX34452

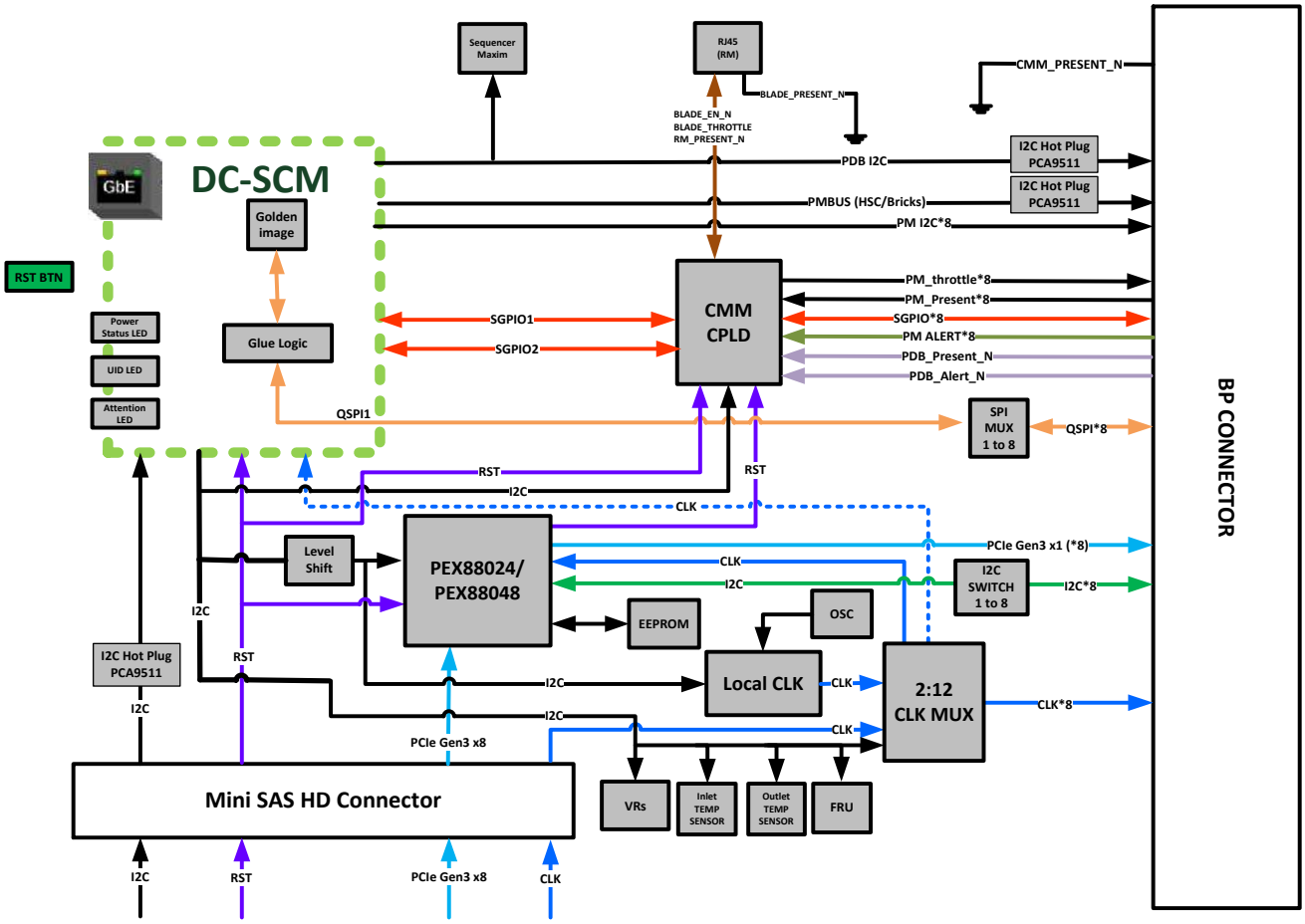


Figure 7 CMM Block Diagram

7.1.1. DC-SCM

The CMM uses a DC-SCM module to provide management and security functionality. The module form factor is adherent to the OCP DC-SCM 1.0 Specification. The DC-SCM connector interface is shown in Table 1. (This is referenced from OCP DC-SCM specification document, Version 1.0, Figure 1 and Table 3.)

This list below includes the primary features of the DC-SCM. Note that information in this section referring to DC-SCM describes the baseline expected features set required for server management.

- BMC (ASPEED AST2600) and associated DDR4 memory

- BMC boot flashes
- eMMC Boot device
- Golden flash
- Cerberus Security
- TPM 2.0 module
- BMC dedicated LAN for communication with Rack Manager
- SMBus /I2C Support
- FRUID EEPROM for storage of manufacturing data and event logs
- Fan Control via an external CPLD located on the PDB
- Thermal sensors for inlet and outlet temperature monitoring
- Power monitoring through the 12V Hot Swap Controller circuitry
- Monitor power status
- Service LEDs
- An eFUSE is supported to protect against pin damage or accidental hot removal or insertion of the DC-SCM board.

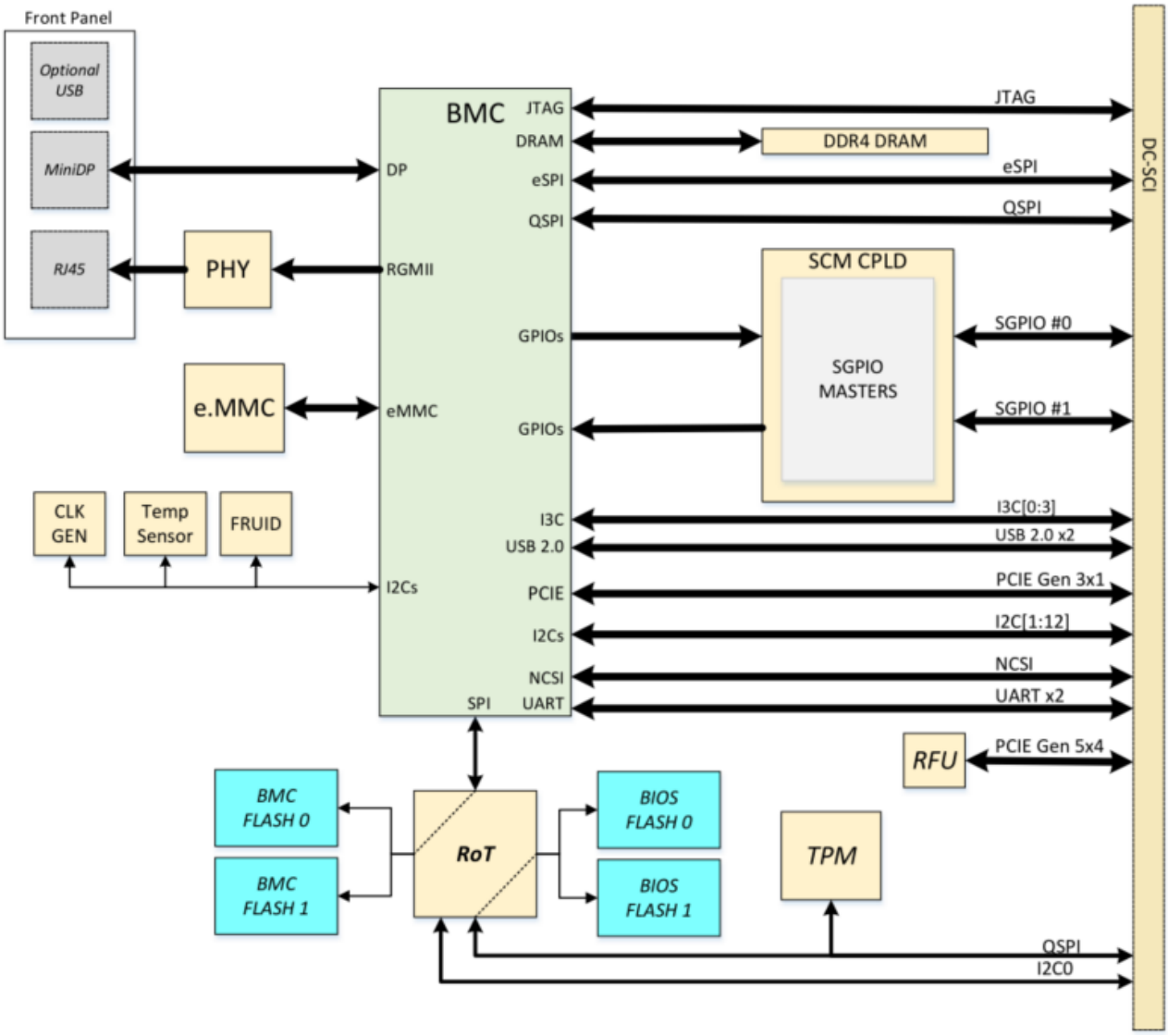


Figure 8 DC-SCM Block Diagram (OCP DC-SCM specification document, Version 1.0, Figure 1)

Pin No.	Contact Sequence	Pin Name	Pin No.	Contact Sequence	Pin Name
OA1	2nd mate	P12V_AUX	OB1	2nd mate	P12V_AUX
OA2	2nd mate	P12V_AUX	OB2	2nd mate	P12V_AUX
OA3	1st mate	GND	OB3	2nd mate	PRSNT0_N
OA4	1st mate	GND	OB4	1st mate	GND
OA5	2nd mate	I3C[0]_SCL	OB5	2nd mate	UART1_SCM_TX
OA6	2nd mate	I3C[0]_SDA	OB6	2nd mate	UART1_SCM_RX
OA7	2nd mate	I3C[1]_SCL	OB7	1st mate	GND
OA8	2nd mate	I3C[1]_SDA	OB8	2nd mate	UART0_SCM_TX
OA9	2nd mate	I3C[2]_SCL	OB9	2nd mate	UART0_SCM_RX
OA10	2nd mate	I3C[2]_SDA	OB10	1st mate	GND
OA11	2nd mate	I3C[3]_SCL	OB11	2nd mate	SPI0_CLK
OA12	2nd mate	I3C[3]_SDA	OB12	2nd mate	SPI0_CS_N
OA13	1st mate	GND	OB13	2nd mate	SPI0_MOSI
OA14	2nd mate	VIRTUAL_RESEAT	OB14	2nd mate	SPI0_MISO
Key					
A1	2nd mate	I2C[0]_SCL	B1	2nd mate	ESPI_CLK
A2	2nd mate	I2C[0]_SDA	B2	2nd mate	ESPI_CS0_N
A3	2nd mate	I2C[1]_SCL	B3	2nd mate	ESPI_ALERT_N
A4	2nd mate	I2C[1]_SDA	B4	2nd mate	ESPI_RESET_N
A5	2nd mate	I2C[2]_SCL	B5	2nd mate	ESPI_IO0
A6	2nd mate	I2C[2]_SDA	B6	2nd mate	ESPI_IO1
A7	2nd mate	I2C[3]_SCL	B7	2nd mate	ESPI_IO2
A8	2nd mate	I2C[3]_SDA	B8	2nd mate	ESPI_IO3
A9	2nd mate	I2C[4]_SCL	B9	2nd mate	RSVD3
A10	2nd mate	I2C[4]_SDA	B10	1st mate	GND
A11	2nd mate	I2C[5]_SCL	B11	2nd mate	QSPI0_CLK
A12	2nd mate	I2C[5]_SDA	B12	2nd mate	QSPI0_CS0_N
A13	1st mate	GND	B13	2nd mate	QSPI0_D0
A14	2nd mate	CLK_100M_PCIE_DP	B14	2nd mate	QSPI0_D1
A15	2nd mate	CLK_100M_PCIE_DN	B15	2nd mate	QSPI0_D2
A16	1st mate	GND	B16	2nd mate	QSPI0_D3
A17	2nd mate	PCIE_BMC_TX_DP	B17	1st mate	GND
A18	2nd mate	PCIE_BMC_TX_DN	B18	2nd mate	NCSI_CLK
A19	1st mate	GND	B19	2nd mate	NCSI_CRS_DV
A20	2nd mate	PCIE_BMC_RX_DP	B20	2nd mate	NCSI_TXEN
A21	2nd mate	PCIE_BMC_RX_DN	B21	2nd mate	NCSI_TXD0
A22	1st mate	GND	B22	2nd mate	NCSI_TXD1
A23	2nd mate	I2C[6]_SCL	B23	2nd mate	NCSI_RXER
A24	2nd mate	I2C[6]_SDA	B24	2nd mate	NCSI_RXD0
A25	2nd mate	I2C[7]_SCL	B25	2nd mate	NCSI_RXD1
A26	2nd mate	I2C[7]_SDA	B26	1st mate	GND
A27	2nd mate	I2C[8]_SCL	B27	2nd mate	PECI_BMC
A28	2nd mate	I2C[8]_SDA	B28	2nd mate	PVCCIO_PECI
Key					

A29	2nd mate	I2C[9]_SCL	B29	2nd mate	SGPIO0_DO
A30	2nd mate	I2C[9]_SDA	B30	2nd mate	SGPIO_CLK
A31	2nd mate	I2C[10]_SCL	B31	2nd mate	SGPIO0_DI
A32	2nd mate	I2C[10]_SDA	B32	2nd mate	SGPIO0_LD
A33	1st mate	GND	B33	1st mate	GND
A34	2nd mate	JTAG_TCK	B34	2nd mate	SGPIO1_DO
A35	2nd mate	JTAG_TMS	B35	2nd mate	RSVD2
A36	2nd mate	JTAG_TDI	B36	2nd mate	SGPIO1_DI
A37	2nd mate	JTAG_TDO	B37	2nd mate	SGPIO1_LD
A38	2nd mate	I2C[11]_SCL	B38	1st mate	GND
A39	2nd mate	I2C[11]_SDA	B39	2nd mate	SGPIO_RESET_N
A40	2nd mate	I2C[12]_SCL	B40	2nd mate	SGPIO_INTR_N
A41	2nd mate	I2C[12]_SDA	B41	2nd mate	P3V0_BAT
A42	1st mate	GND	B42	2nd mate	QSPI0_CS1_N
Key					
A43	2nd mate	HPM_FW_RECOVERY	B43	2nd mate	QSPI1_CLK
A44	2nd mate	HPM_STBY_RDY	B44	2nd mate	QSPI1_CS0_N
A45	2nd mate	HPM_STBY_EN	B45	2nd mate	QSPI1_D0
A46	2nd mate	HPM_STBY_RST_N	B46	2nd mate	QSPI1_D1
A47	2nd mate	SYS_PWRBTN_N	B47	2nd mate	QSPI1_D2
A48	2nd mate	SYS_PWROK	B48	2nd mate	QSPI1_D3
A49	2nd mate	DBP_PREQ_N	B49	1st mate	GND
A50	2nd mate	DBP_PRDY_N	B50	2nd mate	USB2_DP
A51	2nd mate	RST_PLTRST_BUF_N	B51	2nd mate	USB2_DN
A52	2nd mate	SPARE1	B52	1st mate	GND
A53	2nd mate	RoT_CPU_RST_N	B53	2nd mate	USB1_DP
A54	2nd mate	CHASI#	B54	2nd mate	USB1_DN
A55	2nd mate	SPARE0	B55	1st mate	GND
A56	2nd mate	IRQ_N	B56	2nd mate	RSVD0
A57	2nd mate	PRSNT1_N	B57	2nd mate	RSVD1
A58	1st mate	GND	B58	1st mate	GND
A59	2nd mate	PCIE_HPM_RXP[0]	B59	2nd mate	PCIE_HPM_TXP[0]
A60	2nd mate	PCIE_HPM_RXN[0]	B60	2nd mate	PCIE_HPM_TXN[0]
A61	1st mate	GND	B61	1st mate	GND
A62	2nd mate	PCIE_HPM_RXP[1]	B62	2nd mate	PCIE_HPM_TXP[1]
A63	2nd mate	PCIE_HPM_RXN[1]	B63	2nd mate	PCIE_HPM_TXN[1]
A64	1st mate	GND	B64	1st mate	GND
A65	2nd mate	PCIE_HPM_RXP[2]	B65	2nd mate	PCIE_HPM_TXP[2]
A66	2nd mate	PCIE_HPM_RXN[2]	B66	2nd mate	PCIE_HPM_TXN[2]
A67	1st mate	GND	B67	1st mate	GND
A68	2nd mate	PCIE_HPM_RXP[3]	B68	2nd mate	PCIE_HPM_TXP[3]
A69	2nd mate	PCIE_HPM_RXN[3]	B69	2nd mate	PCIE_HPM_TXN[3]
A70	1st mate	GND	B70	1st mate	GND

Table 1 DC-SCM Assignment (OCP DC-SCM specification document, Version 1.0, Table 3)

7.1.2. PCIe Switch

CMM has a Gen4 PCIe switch (Broadcom, PEX88024) to connect head-node to PM. Gen4 x1 PCIe cable over cable backplane from CMM to reach PM. This chapter below includes the primary features of the PCIe switch. Refer to "PEX88024 PCIe 4.0 Switch Data Sheet Version 2.4".

7.1.2.1. Structural Characteristics

The device offers the following structural characteristics:

- PCIe 2.5 GT/s, 5 GT/s, 8 GT/s, and 16 GT/s
- Supports up to 17 lanes
- Supports up to 10 ports

7.1.2.2. Switch Function Characteristics

Following are the functional characteristics of this switch:

- Serial hot plug
- PCIe link clocking modes that support separate reference clock independent SSC (SRIS), separate reference clock with no SSC (SRNS), spread spectrum clocking (SSC) isolation, and common clocking mode
- Configuration through external Serial Peripheral Interface (SPI) Flash memory is required, there is no way to fully configure using strap and strap pins

7.1.2.3. PCI Express Features

The switch offers many PCIe features, including:

- Host, fabric, and downstream port containment
- Advanced Error Reporting (AER)
- Dynamic link width change
- Speed negotiation
- PCIe Multicast
- Power management

7.1.2.4. Advanced and Infrastructure Features

The switch offers the following advanced and infrastructure features:

- Secure boot operating modes
- Dynamic port reconfiguration (DPR)
- Data integrity mechanisms on data path and control path
- 4-MB error checking and correction (ECC)
- Traffic class based queuing
- Completion TLPs with the relaxed-ordering attribute bypass other blocked TLPs
- Upstream port egress read pacing
- Process monitor

7.1.2.5. Debug and Diagnostic Features

The device offers the following debug and diagnostic features:

- Lane based error injection
- Packet generator
- Link error counters per port
- SerDes eye monitor
- Lane error status
- Performance monitor

7.1.3. CMM CPLD

There is a CPLD in CMM module which provide the features as below,

- Communicate with DC-SCM through SGPIO/I2C to expand the control I/O for BMC to PMs
- GPIO expansion
- Reset control
- SGPIO converge and expansion
- Support CPLD FW update in run time

DC-SCM communicates with CMM CPLD (Lattice, LCMXO3LF-4300C-5BG256C) via slave SGPIO/I2C to implement CMM/PM control signals. It also implements SGPIO between CMM/PM CPLD to reduce the BP connector and cable signal quantity between CMM and PM. The block diagram below shows the Shasta CMM CPLD block diagram. The Shasta CMM CPLD code provides the following important modules.

- I2C
- SGPIO Master
- SGPIO Slave
- Hitless update

Clock	Frequency
System Clock	25M Hz
SMBus	100K Hz
SGPIO	25M Hz

Table 2 CMM CPLD Internal Clock

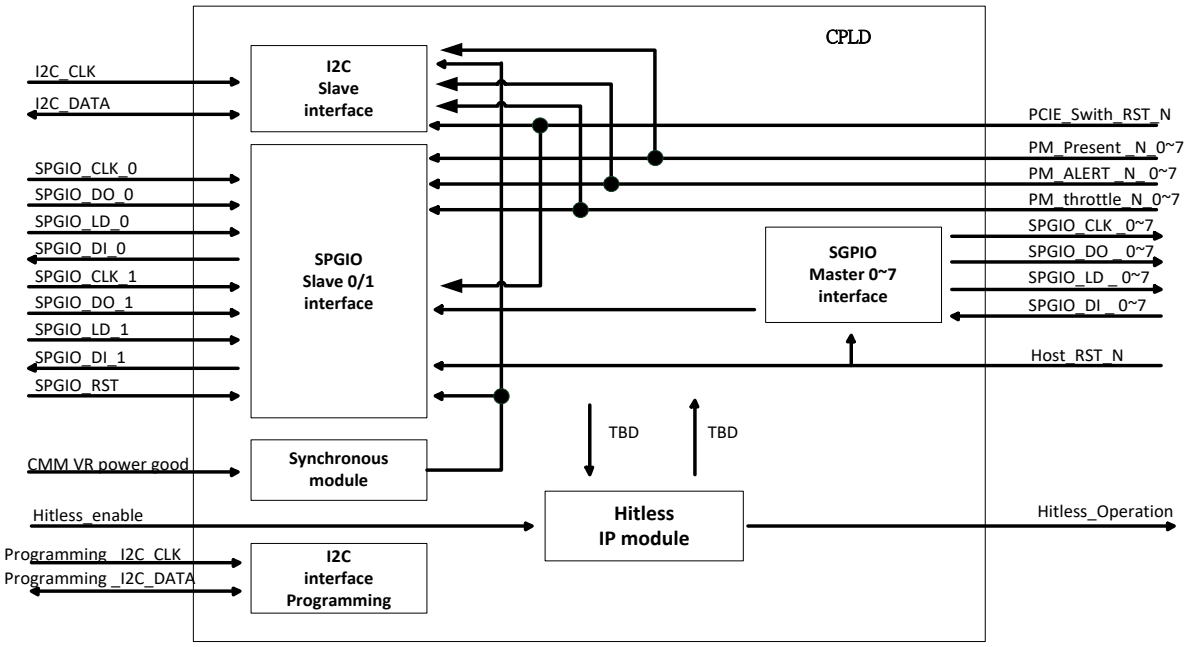


Figure 9 CMM CPLD Block Diagram

7.1.3.1. I2C Interface

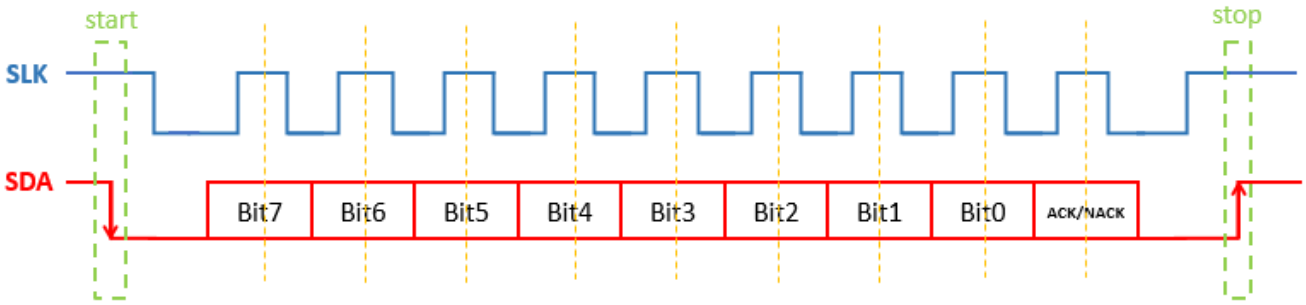


Figure 10 I2C Interface

- Max Frequency：100KHz
- Every data should be 8 bits and after sending data should send ACK data(1bit).
- ACK data is low to response that the data was received.
- Change the data when SLK is low and latch the data when SLK is high.
- The start condition is a high-to-low transition on SDA while SCL is high.
- The stop condition is a low-to-high transition on SDA while SCL is high.

7.1.3.2. SGPIO Interface

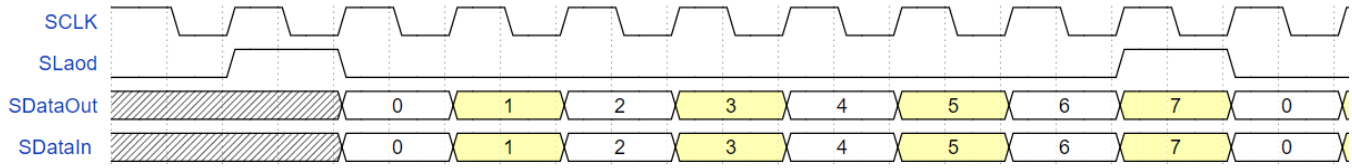


Figure 11 SGPIO Interface

- SLOAD is a pulse valid for one clock cycle. When sampled high on a clock edge, LOAD triggers loading of GPIOs into a latch for transmission. This latched value is what is shifted out on SDataOut on subsequent clocks.
- SDataOut is transmitted by master to slave.
- SDataIn receives the master from Slave.
- Bit length can be defined.

Note: For SGPIO bit definitions please refer to the chapter of Shasta CMM SGPIO Map.

7.1.3.3. CPLD FW Update in run time (Hitless Update)

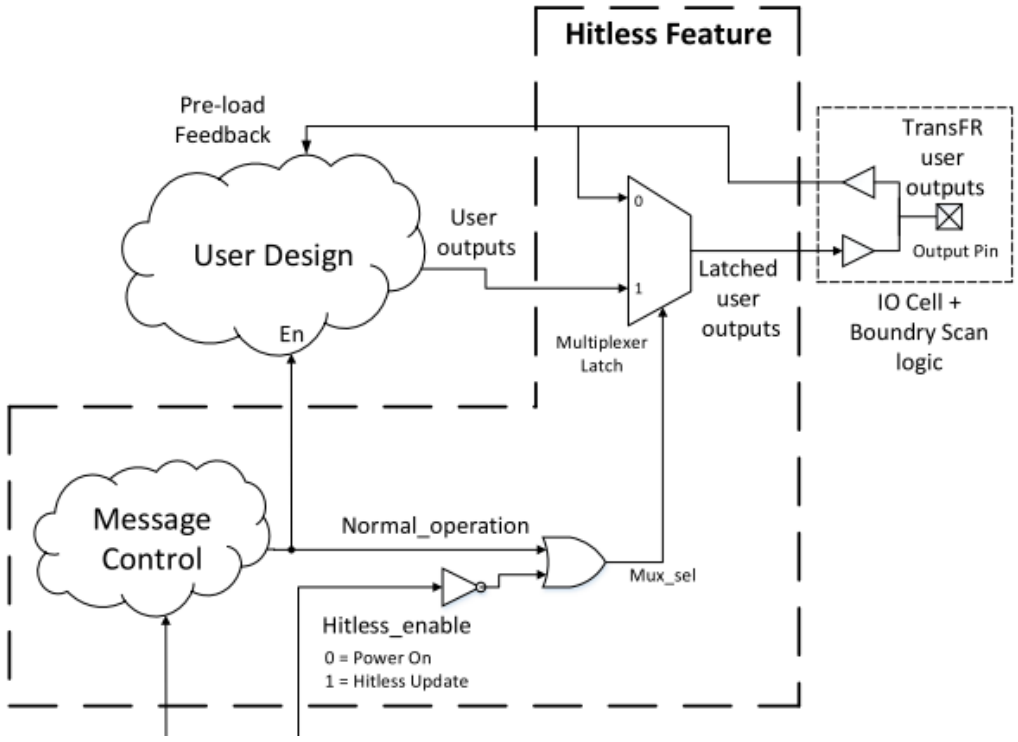


Figure 12 Hitless I/O

A Normal_operation signal is used to support the hitless I/O circuit. Normal_operation must have a default global reset signal GSR value of False.

A Hitless_enable signal is used to control multiplexer latch.

The TransFR circuit in the Boundary Scan logic in the I/O cell latches the output value.

If user need update CPLD FW, hitless_enable needs to be asserted.

The Hitless_enable is active high, multiplexer latch switch to 0, TransFR Boundary Scan logic holds the output states.

Wait update FW done, hitlees_enable will deasserted.

Hitless_enable	Normal_operation	User Design Output
X	1	Normal Operation
0	0	User Defined Power-up State
1	0	User Defined Hold/Preload State

Table 3 Hitless setting

The hitless I/O logic must cover two primary scenarios: Power-up and Hitless Reconfiguration. The control input Hitless_en is driven by an external controller to determine which scenario is active.
If Hitless_en is false, the user logic starts from a power-up reset state. If true, the user logic can utilize the values held in the TransFR Boundary Scan I/O cells to initialize the control logic to resume from the pre-update state.

7.1.4. CMM Local Clock

The SI52202 is the industry's highest performance and lowest power PCI Express clock generator for PCIe Gen 1/2/3/4/5 and SRIS applications. All differential clock outputs are compliant to PCIe Gen1/2/3/4/5 common clock and separate reference clock architecture specifications. The Si52202 feature individual hardware control pins for enabling and disabling each output, spread spectrum enable/disable for EMI reduction, and frequency select to select 100, 133, or 200 MHz differential output frequencies. These features can also be controlled via I2C. Refer to "SI52202-A01BGMR datasheet Rev. 1.0".

7.1.4.1. Features

- Output 100 MHz PCIe Gen 1/2/3/4/5 and SRIS compliant clock generator, with push-pull HCSL output drivers
- Low jitter of 0.13 ps rms max to meet PCIe Gen5 specifications with design margin
- Low power consumption
- Individual hardware control pins and I2C controls for Output Enable, Spread Spectrum Enable and Frequency Select
    - Output Enable function easily disables unused outputs for power saving

  - Spread Enable function to turn on/off spread spectrum and to select spread levels, either down spread 0.25% or 0.5%
  - Frequency Select function to select output frequency of 100 MHz

- Adjustable slew rate to improve signal quality for different applications and board designs
- I2C support with readback capabilities
- Operating Ambient Temperature range: –40 °C to 85 °C

7.1.5. Clock MUX

The 9ZML1245 device is third generation enhanced. Each input clock has software adjustable input-to-output delay when operating in Zero-Delay (ZDB) mode. The devices also implement an extensive set of features ensuring that clocks are well behaved with today's ever more complex power-up sequencing. Refer to " SI52202-A01BGMR datasheet Rev. 1.0". Refer to "9ZML1245/9ZML1255/9ZML1256 datasheet October 9, 2020".

7.1.5.1. Features

- Low-power HCSL (LP-HCSL) outputs
- Flexible Power Sequencing (FPS) configuration via SMBus
- Input-to-output delay: 0ps default
- Selectable ZDB bandwidths minimizes jitter peaking in cascaded ZDB topologies
- Hardware/SMBus control of ZDB and FOB modes
- Spread-spectrum compatible
- Up to 400MHz FOB operation
- 100MHz ZDB mode operation
- -40°C to +85°C operating temperature range

7.1.6. CMM Sequencer

The MAX34452 is a power-supply system manager that is capable of monitoring different voltage rails or currents and is also capable of sequencing and margining power supplies. The system manager monitors the power-supply output voltages and currents and constantly checks them for user-programmable over and under threshold limits. If a fault is detected, the device automatically shuts down the system in an orderly fashion. The device can sequence the supplies in any order at both power-up and power-down with time-based or event-based sequencing. Refer to "MAX34452 datasheet Rev 0; 6/21".

7.1.6.1. Benefits and Features

- Integration Enables Management of Multiple Power Supplies to Maximize System Performance

  - Voltage or Current Monitoring
  - Sequencing and Margining
  - Remote Ground Sensing Improves Measurement Accuracy
  - Automatic Closed-Loop Margining
- Fast, Reliable Control and Fault Detection Improves System Reliability
  - Fast Minimum/Maximum Threshold Excursion Detection
  - Reports Peak, Minimum, and Average Levels for a Number of Parameters
  - On-Board Nonvolatile Black Box Fault Logging and Default Configuration Setting

7.1.7. CMM I2C Bus Components

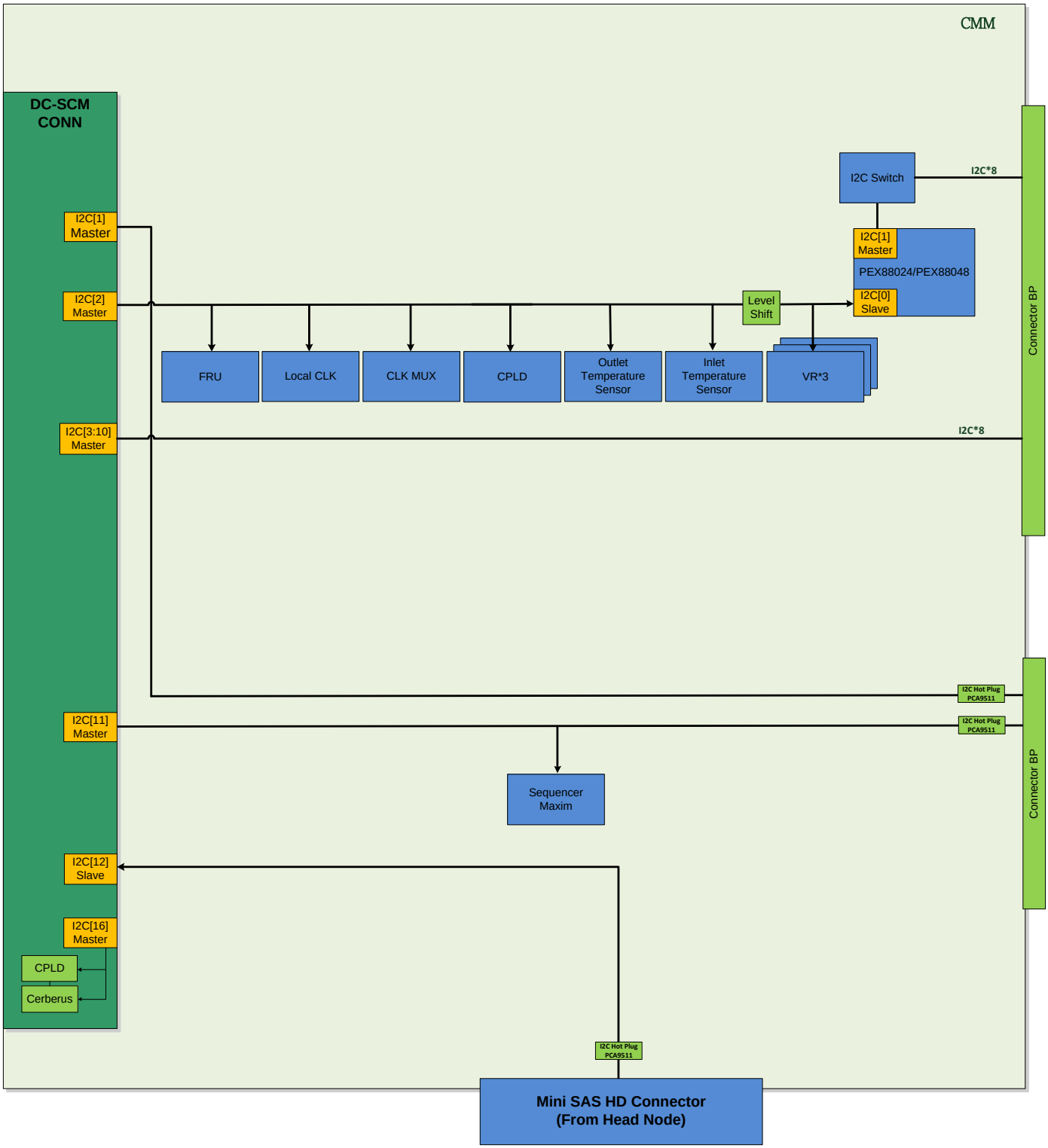


Figure 13 CMM I2C Block Diagram

7.1.7.1. PCIe Switch

The PCIe switch has both I2C master and I2C slave functionality. The I2C slave port is connected to the DC-SCM internally on CMM, while the I2C master port is connected to the IO expander (Table 14) externally on PM.

7.1.7.2. Voltage regulators

PMBus telemetry of output current, output voltage, input voltage and junction temperature.

7.1.7.3. Local Clock

To enhance the flexibility and function of the clock synthesizer, an I2C interface is provided. Through the I2C interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the I2C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

7.1.7.4. Clock MUX

Local clock and Host clock Mux. The 9ZML1256 has an I2C Write Lockout pin for increased device and system security. Flexible Power Sequencing (FPS) configuration via SMBus. Hardware/SMBus control of ZDB and FOB modes.

7.1.7.5. CPLD

CPLD for IO expansion, SGPIO bridge and Misc functions. Every MachXO3L/LF device contains two I2C IP cores. These are the primary and secondary I2C IP cores. Either of the two cores can be configured either as an I2C master or as an I2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

7.1.7.6. Inlet/Outlet Temperature Sensor (TMP75)

The TMP75 is a remote temperature sensor monitor with a built-in local temperature sensor. The device communicates with DC-SCM to program the alarm thresholds and to read temperature data. The TMP75 needs to be calibrated to accurately read the CMM ambient temperature via the remote temperature sensor monitor.

7.1.7.7. FRU ID EEPROM (MRP 24AA1026T-I)

The MRP 24AA1026T-I/SN or equivalent is a 1024Kb serial EEPROM accessed over I2C from DC-SCM. It is used for tracking manufacturing information in the field. Contents of the FRUID EEPROM are defined in the Shasta FRUID Specification.

7.1.7.8. Sequencer (MAX34452)

From a software perspective, the device appears as a PMBus device capable of executing a subset of PMBus commands. The device employs a number of standard SMBus protocols (e.g., Write Word, Read Word, Write Byte, Read Byte, Send Byte, etc.) to program output voltage and warning/fault thresholds, read monitored data, and provide access to all manufacturer-specific commands.

7.1.7.9. I2C Switch

The PCA9544A is a 1-of-4 bi-directional translating multiplexer, controlled via the I2C-bus. The SCL/SDA upstream pair fans out to four SCx/SDx downstream pairs, or channels. The downstream pairs connect to the I2C switch (Table 13) in each PM. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register.

7.1.8. MiniSAS HD x2 Connecter

Shasta uses 2 MiniSAS x4 connectors. The pinout of this connector is detailed in Table 4.

SAS_1 Pin	SAS_1 Function	SAS_2 Pin	SAS_2 Function
1A1	CLK_P	2A1	NC
1A2	CLK_N	2A2	NC
1A3	GND	2A3	GND
1A4	RX0_P	2A4	RX4_P
1A5	RX0_N	2A5	RX4_N
1A6	GND	2A6	GND
1A7	RX3_P	2A7	RX7_P
1A8	RX3_N	2A8	RX7_N
1A9	GND	2A9	GND
1B1	PERST#	2B1	PERST#
1B2	GND	2B2	GND
1B3	GND	2B3	GND
1B4	RX1_P	2B4	RX5_P
1B5	RX1_N	2B5	RX5_N
1B6	GND	2B6	GND
1B7	RX2_P	2B7	RX6_P
1B8	RX2_N	2B8	RX6_N
1B9	GND	2B9	GND
1C1	I2C_SCL	2C1	NC
1C2	I2C_SDA	2C2	NC
1C3	GND	2C3	GND
1C4	TX0_P	2C4	TX4_P
1C5	TX0_N	2C5	TX4_N

1C6	GND	2C6	GND
1C7	TX3_P	2C7	TX7_P
1C8	TX3_N	2C8	TX7_N
1C9	GND	2C9	GND
1D1	NC	2D1	NC
1D2	NC	2D2	NC
1D3	GND	2D3	GND
1D4	TX1_P	2D4	TX5_P
1D5	TX1_N	2D5	TX5_N
1D6	GND	2D6	GND
1D7	TX2_P	2D7	TX6_P
1D8	TX2_N	2D8	TX6_N
1D9	GND	2D9	GND

Table 4 MiniSAS HD x2 Connecter Pin Assignment

7.1.9. Rack management RJ45 Connecter

Shasta uses RJ45 connector for rack management. The pinout of this connector is detailed in Table 5.

Pin number	Function	Description
P1	RM_THROTTLE+	Active high signal used to put the system into a low power (power cap) state. This signal should default low (inactive) if the Rack Manager is not present. The Rack Manager drives this signal to multiple servers. Therefore, the server must take care to electrically isolate this signal to avoid power leakage between servers.
P2	RM_THROTTLE-	
P3	NC	NA
P4	RM_PRESENT_N	Active low signal used to communicate physical presence of the Rack Manager to the server. This signal should be tied to GND in the Rack Manager.
P5	BLADE_PRESENT_N	Active low signal used to communicate physical presence of the server to the Rack Manager. This signal should be tied to GND in the server.
P6	NC	NA
P7	GND	Ground
P8	BLADE_EN_N	Active low signal used to enable/disable power to the server. A pulldown resistor is used in the system to ensure a default low state if the RM is removed.

Table 5 RM RJ45 Connecter Pin Assignment

7.1.10. CMM Backplane Connector Pin List

7.1.10.1. CMM to PM

CMM to PM signals are detailed in Table 6. The connectors shall be Molex MPN 171320-1026 or equivalent. This table is taken from "Shasta pin list_20220913".

Function	Signals	Pin Qty	Description
PCIe	PCIe GEN3 TX_P	8	PCIe to PM
	PCIe GEN3 RX_P	8	PCIe to PM
	PCIe GEN3 TX_N	8	PCIe to PM
	PCIe GEN3 RX_N	8	PCIe to PM
	PCIe GEN3 CLK_P	8	PCIe clock to PM
	PCIe GEN3 CLK_N	8	PCIe clock to PM
PM I2C	I2C_SCL	8	I2C to PM
	I2C_SDA	8	I2C to PM
PM Present	Present	8	PM present input
PCIe Switch I2C	I2C_SCL (Master)	8	I2C from PCIe switch to PM for hot plug
	I2C_SDA (Master)	8	I2C from PCIe switch to PM for hot plug
MISC	Alert (PM)	8	Alert and/or Interrupt from PM
	Throttle	8	Throttle to PM
SPI	MISO (SPI from BMC to Cerberus)	8	SPI
	MOSI (SPI from BMC to Cerberus)	8	SPI
	CLK (SPI from BMC to Cerberus)	8	SPI
	CS_N (SPI from BMC to Cerberus)	8	SPI
	IO2 (SPI from BMC to Cerberus)	8	SPI Quad
	IO3 (SPI from BMC to Cerberus)	8	SPI Quad
SGPIO	In	8	SGPIO to PM for sideband signals
	Out	8	SGPIO to PM for sideband signals
	LD	8	SGPIO to PM for sideband signals
	CLK	8	SGPIO to PM for sideband signals

Table 6 CMM to PM Pin List

7.1.10.2. CMM to PDB

CMM to PDB signals are detailed in Table 7. The connector shall be Molex MPN 171320-9034 or equivalent. This table is taken from "Shasta pin list_20220913".

Function	Signals	Pin Qty	Description
PMBus	PMBus_SCL	1	PMBus to fan boards FRU, HSC and bricks
	PMBus_SDA	1	PMBus to fan boards FRU, HSC and bricks
I2C	I2C_SCL	1	I2C to PDB for PDB related components, FRU, FAN control and CPLD
	I2C_SDA	1	I2C to PDB for PDB related components, FRU, FAN control and CPLD
Present	CMM_PRESENT_N	1	CMM present output
	PDB_PRESENT_N	1	PDB present input
Alert	PDB_ALERT_N	1	PDB alert

Table 7 CMM to PDB Pin List

7.1.11. CMM Power Architecture

The CMM power block diagram is shown in Figure 14. The capacity of each voltage converter is sized to conservatively provide maximum power for the rail, independent of the total power budget for the CMM. All voltage sources must meet the respective component manufacturer's recommended operating conditions.

Standby power:

1. P12V_STBY is enabled by P12V_IN.
2. P12V_SCM and P3V3_STBY are enabled by P12V_STBY.

Main power:

1. P12V is enabled by CPLD after CPLD gets HPM_STBY_EN is high.
2. P3V3, P1V8, PEX_0V9 and PEX_1V8 are enabled by sequencer.

	Input Source	Power Rail	Power Level	Current
Main Power	P12V	PEX_0V9	0.9V	15.94A
	P12V	PEX_1V8	1.8V	1.94A
	P12V	P1V8	1.8V	0.12A
	P12V	P3V3	3.3V	0.12A
	P12V_IN	P12V	12V	1.71A

Stand by Power	P12V_STBY	P3V3_STBY	3.3V	0.02A
	P12V_STBY	P12V_SCM	12V	2.8A
	P12V_IN	P12V_STBY	12V	3.12A

Table 8 CMM Power Distribution

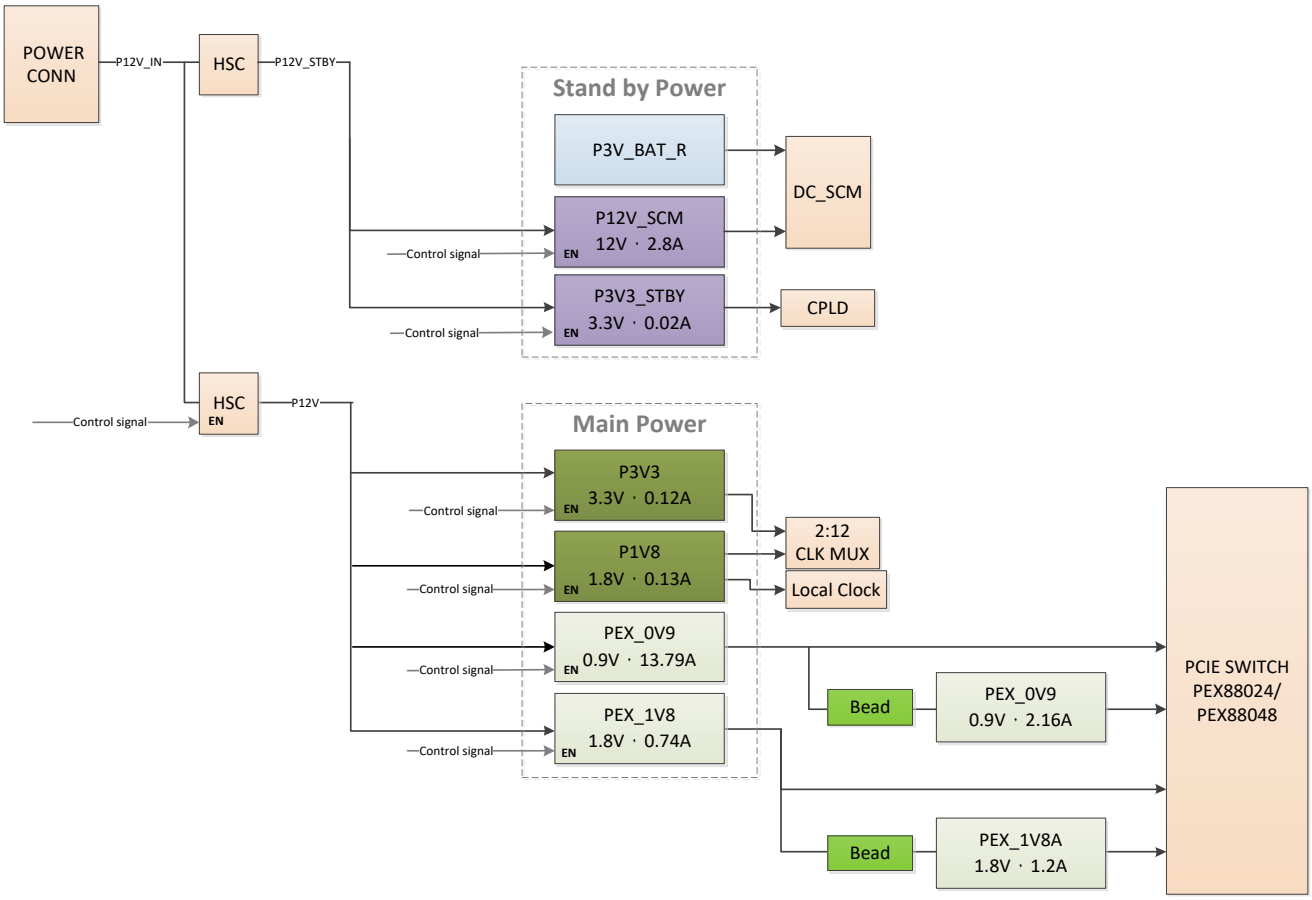


Figure 14 CMM Power Block Diagram

7.1.12. CMM Power Sequencing

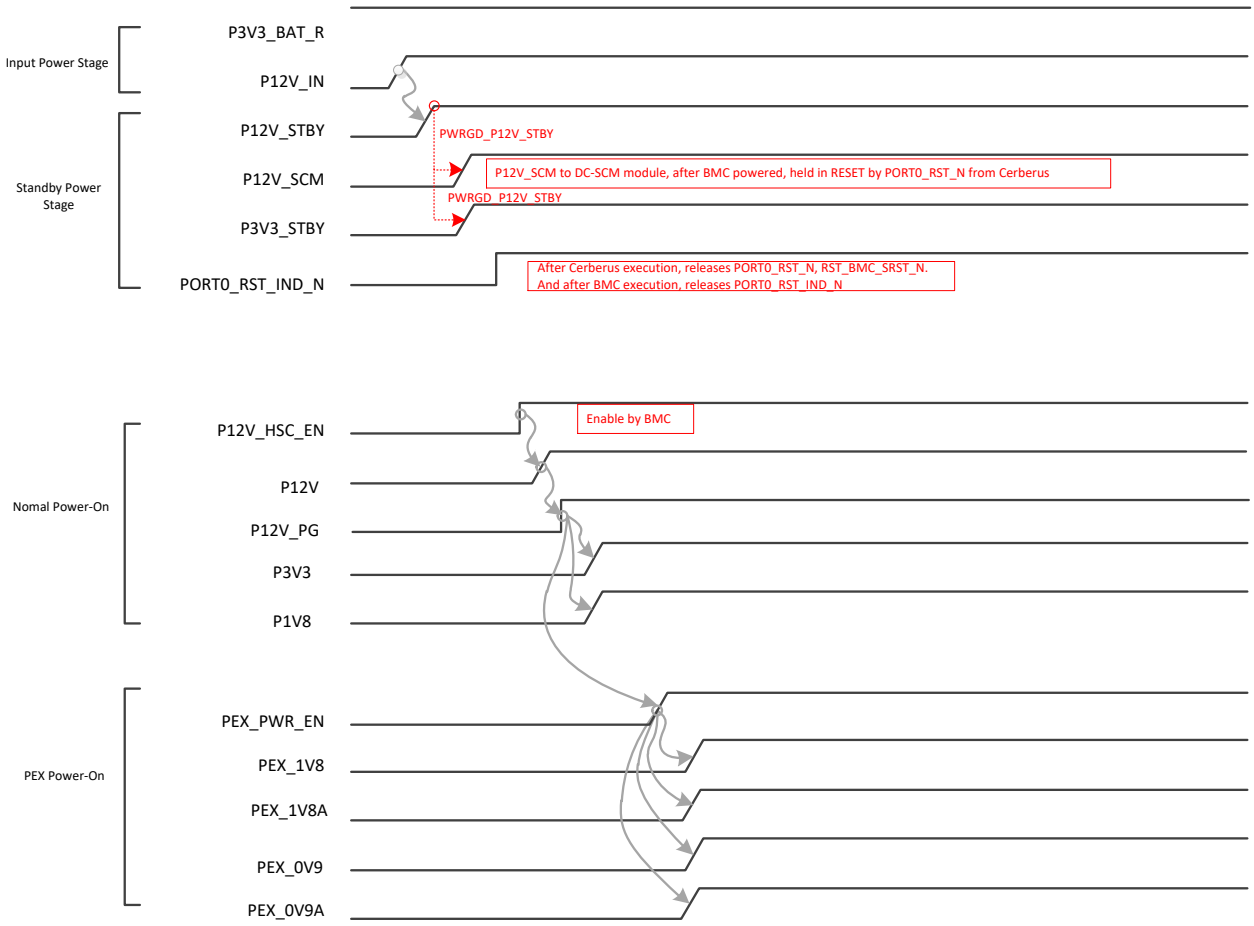


Figure 15 CMM Power Sequencing

7.1.13. CMM Clock Block Diagram

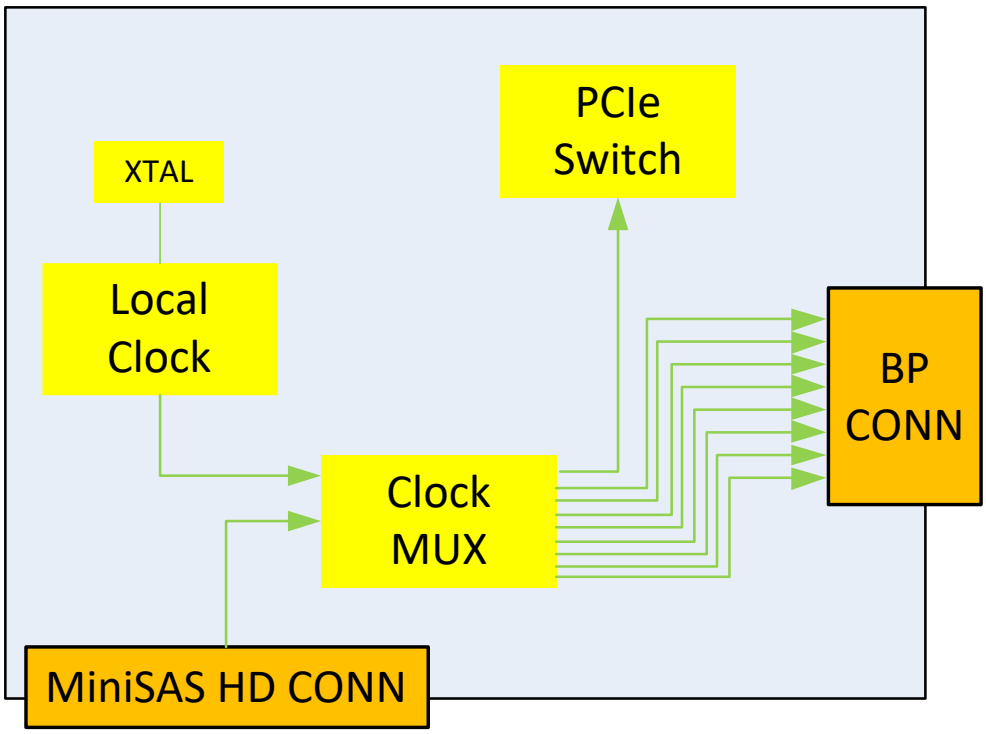


Figure 16 CMM Clock Block Diagram

7.1.14. CMM SPI Block Diagram

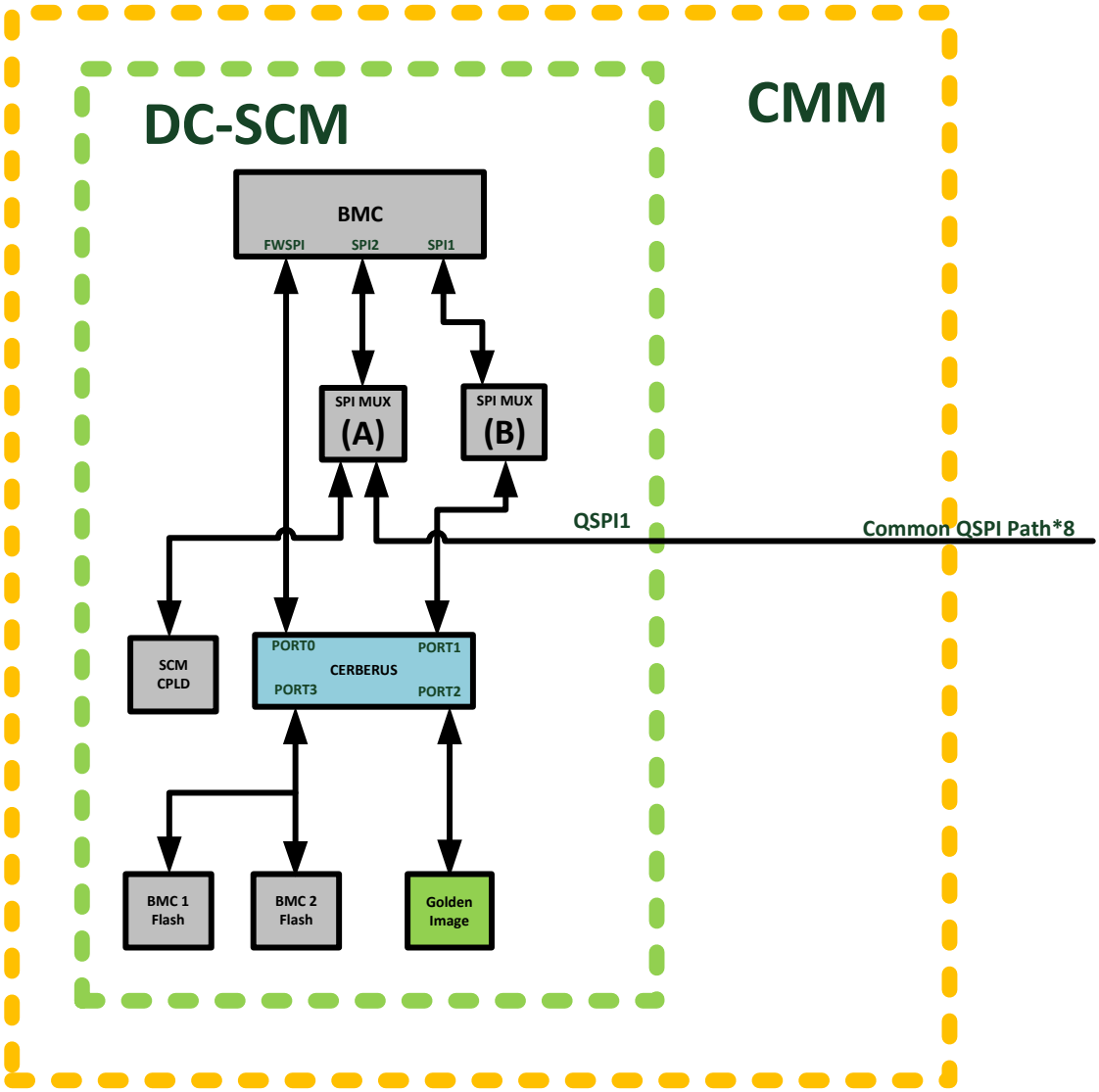


Figure 17 CMM SPI Block Diagram (SPI fanout buffer is not shown)

7.1.15. CMM Stack-up

Table 9 shows the 14-layer PCB stack-up. For CMM, we will use the same stack-up strategy but with lower layer count. This is being evaluated at this time. One way to reduce the layer count is to remove two power cores (4G, 5P, 20P, 21G) and two HS signal cores (8G, 9S, and 16S, 17G). This will also reduce the board thickness accordingly. This stack-up uses R-5785 (GN) material or equivalent. The stack-up is for reference, it may implement with lower cost of stack-up if it is applicable.

STACKUP							
						Target Z (ohms) - MicroStrip	
						Target Z (ohms) - StripLine	
						Z tolerance	
						Z Type	
Layer#	Material	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Glass Fabric	Er
		Soldermask		0.60			3.8
1		TOP	0.5+plating	1.95			
	IT-170GRA1	PP		2.70	±0.709	1080x1	3.8
2		GND	1 (RTF)	1.30			
	IT-170GRA1	CORE		3.00	±0.709	1086x1	3.8
3		IN1	1 (RTF)	1.30			
	IT-170GRA1	PP		9.00	±1.5	2116x2	3.9
4		GND1	1 (RTF)	1.30			
	IT-170GRA1	CORE		3.00	±0.709	1086x1	3.8
5		IN2	1 (RTF)	1.30			
	IT-170GRA1	PP		6.00	±0.984	1506x1	3.8
6		GND2	1 (RTF)	1.30			
	IT-170GRA1	CORE		3.00	±0.709	1086x1	3.8
7		VCC	2 (RTF)	2.60			
	IT-170GRA1	PP		12.00	±1.97	2116x3	3.9
8		VCC1	2 (RTF)	2.60			
	IT-170GRA1	CORE		3.00	±0.709	1086x1	3.8
9		GND3	1 (RTF)	1.30			
	IT-170GRA1	PP		6.00	±0.984	1506x1	3.8
10		IN3	1 (RTF)	1.30			
	IT-170GRA1	CORE		3.00	±0.709	1086x1	3.8
11		GND4	1 (RTF)	1.30			
	IT-170GRA1	PP		9.00	±1.5	2116x2	3.9
12		IN4	1 (RTF)	1.30			
	IT-170GRA1	CORE		3.00	±0.709	1086x1	3.8
13		GND5	1 (RTF)	1.30			
	IT-170GRA1	PP		2.70	±0.709	1080x1	3.8
14		BOTTOM	0.5+plating	1.95			
		Soldermask		0.60			3.8
			Total	88.70	±10%		

Table 9 CMM Stack-up

7.1.16. CMM PCB Placement Strategy

Layout views of the CMM showing major component locations are shown in Figure 18.

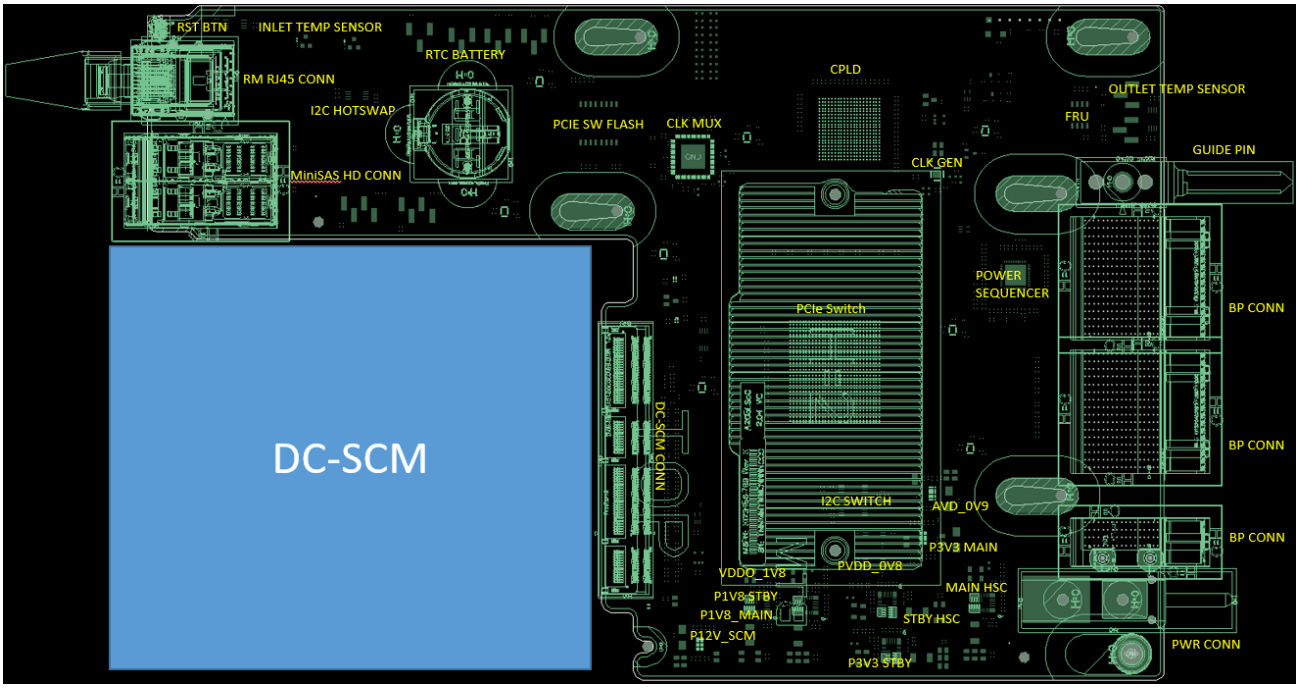


Figure 18 CMM Layout Placement (TOP View)

7.2. PM

The PM solution will vary depending on the solution, it may be FPGA, GPU or other solutions. Here is a use case example of common logic,

- CPLD: Lattice, LCMXO3LF-4300C-5BG256C
- Local Clock: Silicon, SI52202-A01BGMR
- Clock Buffer: TI, LMK00334
- Sequencer: Maxim, MAX34452

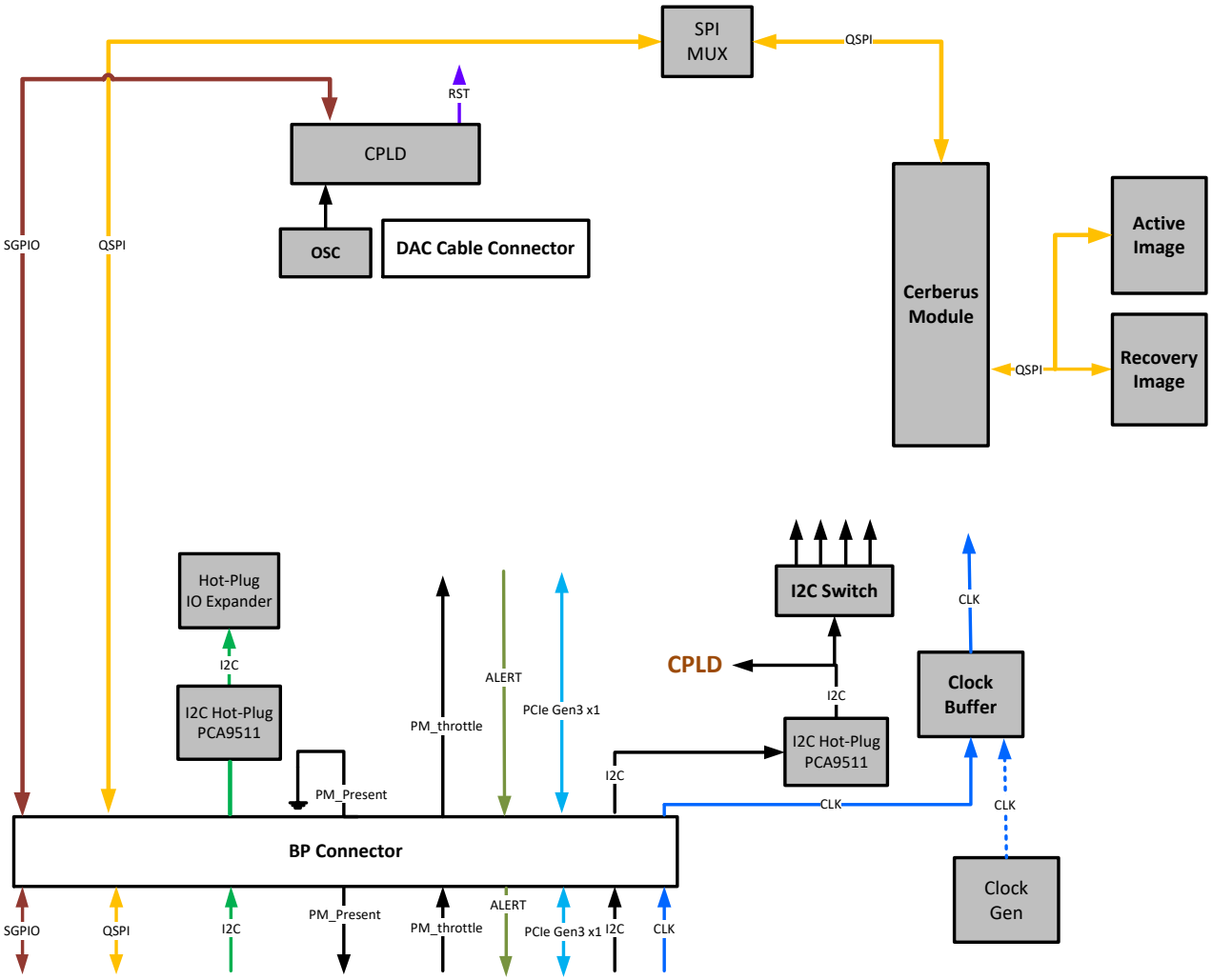


Figure 19 PM Common logic Block Diagram of use case

7.2.1. Cerberus (security module)

PM has a plug-in card which enables secure boot for server BMC and peripherals. The primary data interfaces for the module is shown in Figure 20. The Cerberus connector interface is shown in Table 10. (This is referenced from Olympus Cerberus Security Module specification document, Version 1.1, Figure 2 and Table 3.)

- Plug-in module with 40-pin connector interface.
- MCU Root of Trust Processor with Secure Boot
- Supports one SPI RoT (Root of Trust) boot interface (P0)
- Supports one QSPI RoT boot interface (P1)
- Supports one QSPI Flash Interface (P2)

- Supports one SPI Flash Interface (P3)
- Supports one QSPI flash on module for RoT boot.
- Supports a second SPI flash on module for RoT failover boot.
- CPLD (sCPLD) on module for SPI filtering.
- External zero delay hardware mux/de-mux bus switch on module.
- I2C interface between RoT and external devices.
- GPIO support for reset control of external processors.
-

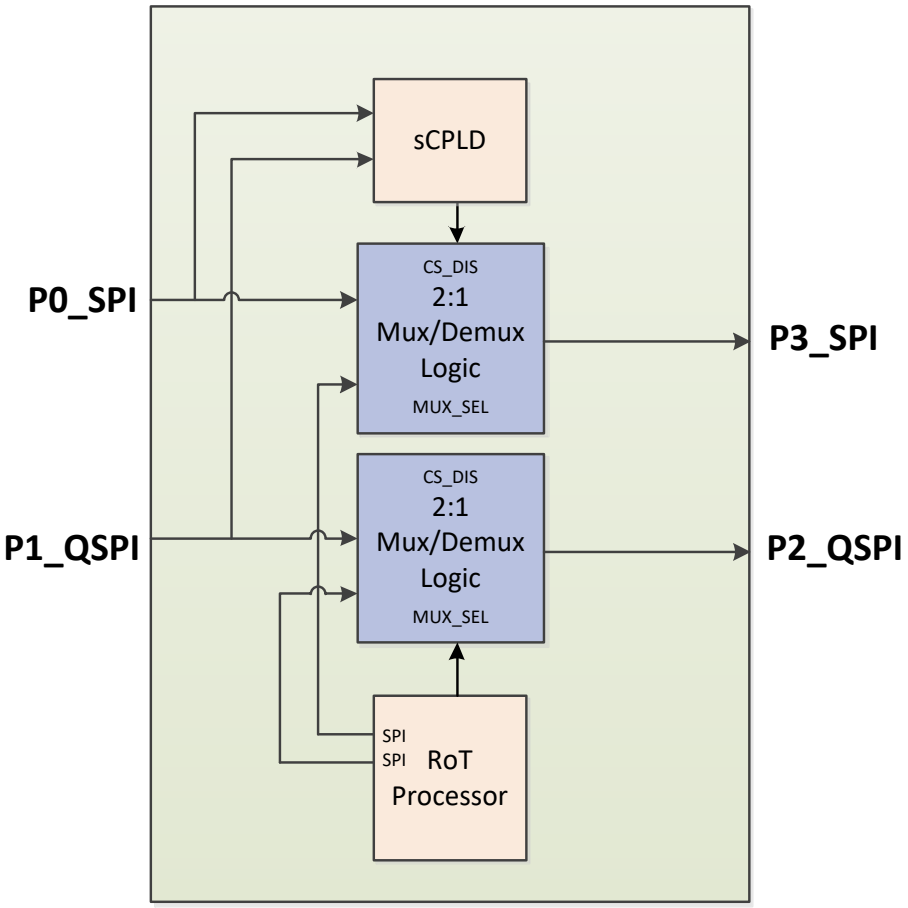


Figure 20 Cerberus Block Diagram (Olympus Cerberus Security Module specification document, Version 1.1, Figure 2)

The mating connector that is used on the PM for Cerberus is TBD.

Pin #	Signal name	RoT Direction	Description
1	PORT0_SPI_SCK	I	SPI clock from port 0 external processor. NC if port 0 is unused.
3	GND		Ground
5	PORT0_SPI_MOSI	I	MOSI from port 0 external processor. NC if port 0 is unused.
7	PORT0_SPI_CS0#	I	Main chip select from port 0 external processor. NC if port 0 is unused.
9	PORT0_SPI_MISO	O	MISO from port 0 external processor. NC if port 0 is unused.
11	PORT0_SPI_CS1#	I	Failover chip select from port 0 external processor. NC if port 0 is unused or does not support boot failover.
13	PORT0_RST_IND#	I	Reset indicator from port 0 external processor. Must assert when the processor is in reset and deassert when it is out of reset. NC if port 0 is unused.
15	PORT0_RST#	O(OD)	Reset control for the port 0 external processer. PU on MB. NC if port 0 is unused.
17	INTRUSION_DET#	I	Chassis intrusion detection indicator. PU on MB. NC if intrusion detection is not supported.
19	PORT1_RST_AUTH#	I	Reset indicator from port 1 external processor. Must assert when the processor is in reset and is ready for Cerberus to take control of SPI flash for authentication. Must deassert when the processor is out of reset or authentication is not allowed. NC if port 1 is unused.
21	PON_RESET#	I	Should be connected to the power good signal of the "always on" 3.3V_STBY power domain, which powers the Cerberus module delayed by 20ms. The signal must have monotonic rising and falling edges and meet the electrical input specifications of the Cerberus module specified in Table 20 of the NXP LPC54S0XX data sheet [1].
23	PORT1_RST_IND#	I	Reset indicator from port 1 external processor. Must assert when the processor is in reset and deassert when it is out of reset. NC if port 1 in unused.
25	PORT1_RST#	O	Reset control for the port 1 external processor. Typically, a PD on the MB, but some platforms may choose to have a PU. NC if port 1 is unused.
27	PORT1_QSPI_D3	I/O	QSPI D3 from port 1 external processor. NC if port 1 is unused or QSPI is not supported.
29	PORT1_QSPI_D2	I/O	QSPI D2 from port 1 external processor. NC if port 1 is unused or QSPI is not supported.
31	PORT1_QSPI_D1	I/O	QSPI D1 (MISO) from port 1 external processor. NC if port 1 is unused.
33	PORT1_QSPI_D0	I/O	QSPI D0 (MOSI) from port 1 external processor. NC if port 1 is unused.
35	PORT1_QSPI_CS0#	I	Main chip select from port 1 external processor. Only one CS is supported on port 1. NC if port 1 is unused.
37	GND		Ground
39	PORT1_SPI_SCK	I	SPI clock from port 1 external processor. NC if port 1 is unused.

Pin #	Signal name	RoT Direction	Description
2	PORT3_SPI_SCK	O	SPI clock to port 0 flash devices. NC if port 0 is unused.
4	GND		Ground
6	PORT3_SPI_MOSI	O	MOSI to port 0 flash devices. NC if port 0 is unused.
8	PORT3_SPI_CS0#	O	Chip select for port 0 flash device #1. NC if port 0 is unused.
10	PORT3_SPI_MISO	I	MISO to port 0 flash devices. NC if port 0 is unused.
12	PORT3_SPI_CS1#	O	Chip select for port 0 flash device #2. NC if port 0 is unused or if operating with only a single flash device.
14	I2C0_SCL (Multi-master)	I/O	I2C SCL for communicating with the Cerberus module. PU on MB.
16	I2C0_SDA (Multi-master)	I/O	I2C SDA for communicating with the Cerberus module. PU on MB.
18	P3V3		Should be connected to 3.3V from main board
20	P3V3		Should be connected to 3.3V from main board
22	I2C1_SCL (RoT Master)	O	I2C SCL for platform CPLD communication. PU on Cerberus. NC if there is no platform CPLD.
24	I2C1_SDA (RoT Master)	I/O	I2C SDA for platform CPLD communication. PU on Cerberus. NC if there is no platform CPLD.
26	PORT2_QSPI_IO3	I/O	QSPI D3 to port 1 flash devices. NC if port 1 is unused or QSPI is not supported.
28	PORT2_QSPI_IO2	I/O	QSPI D2 to port 1 flash devices. NC if port 1 is unused or QSPI is not supported.
30	PORT2_QSPI_IO1	I/O	QSPI D1 (MISO) to port 1 flash devices. NC if port 1 is unused.
32	PORT2_QSPI_IO0	I/O	QSPI D0 (MOSI) to port 1 flash devices. NC if port 1 is unused.
34	PORT2_QSPI_CS1#	O	Chip select for port 1 flash device #2. NC if port 1 is unused or if operating with only a single flash device.
36	PORT2_QSPI_CS0#	O	Chip select for port 1 flash device #1. NC if port 1 is unused.
38	GND		Ground
40	PORT2_QSPI_SCK	O	SPI clock to port 1 flash devices. NC if port 1 is unused.

Table 10 Cerberus Assignment (Olympus Cerberus Security Module specification document, Version 1.1, Table 3)

7.2.2. PM CPLD

The CPLD used in the PM is TBD. DC-SCM communicates with PM CPLD via slave I2C to implement CMM/PM control signals, and a Hitless update function (online programming doesn't need AC cycle). The I2C bus can relieve the signals traffic while BMC is busy. It also implements SGPIO between CMM/PM CPLD to reduce the BP connector and cable signal quantity between CMM and PM.

The below use case is an example to shows the Shasta PM CPLD block diagram. The Shasta PM CPLD code provides the following important modules.

- I2C
- SGPIO Slave
- Hitless update

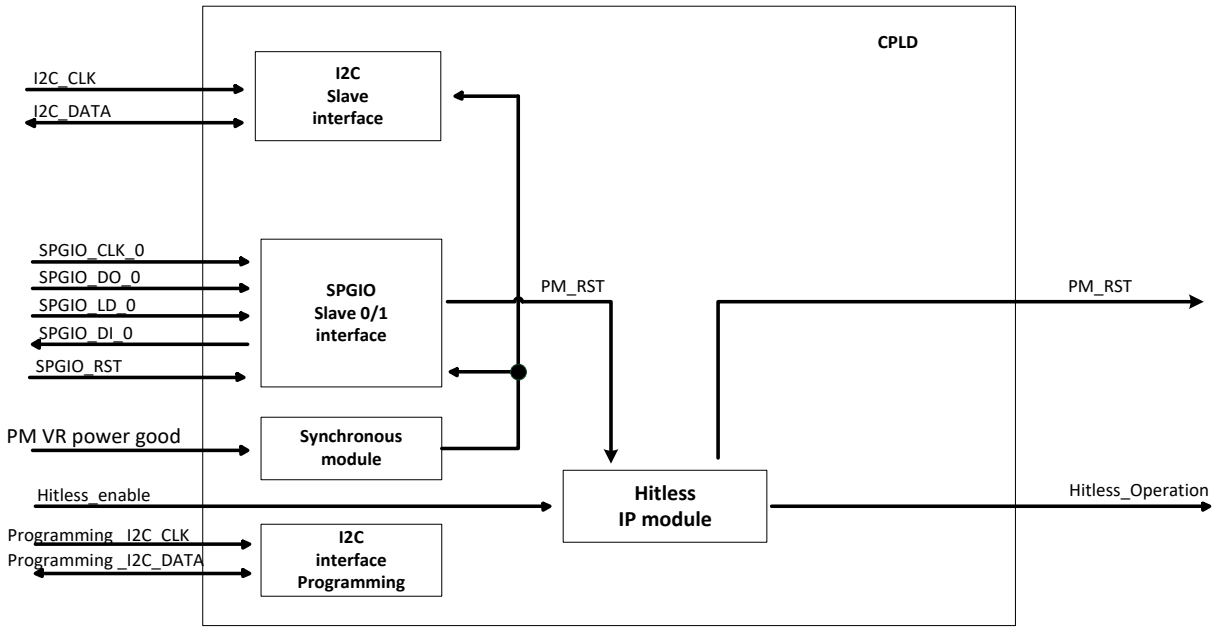


Figure 21 PM CPLD Block Diagram

The CPLD requires an input clock of 25Mhz. Table 11 shows the information for this clock

Clock	Frequency
System Clock	25MHz
SGPIO_CLK	25MHz

Table 11 PM CPLD External Clock

There is also a SMBus interface along with SGPIO. The SMBus will run at 100 Mhz while the SGPIO runs at 25 Mhz.

7.2.3. PM Sequencer

This example use case uses the MAX34452 to sequence and margin the voltage. It will also be used to monitor the status of the voltage rails. The sequence will be described more in detail in the power section. Refer to "MAX34452 datasheet Rev 0; 6/21".

7.2.4. PM I2C Bus Components

The I2C bus on PM will vary, below is an example for PM I2C bus.

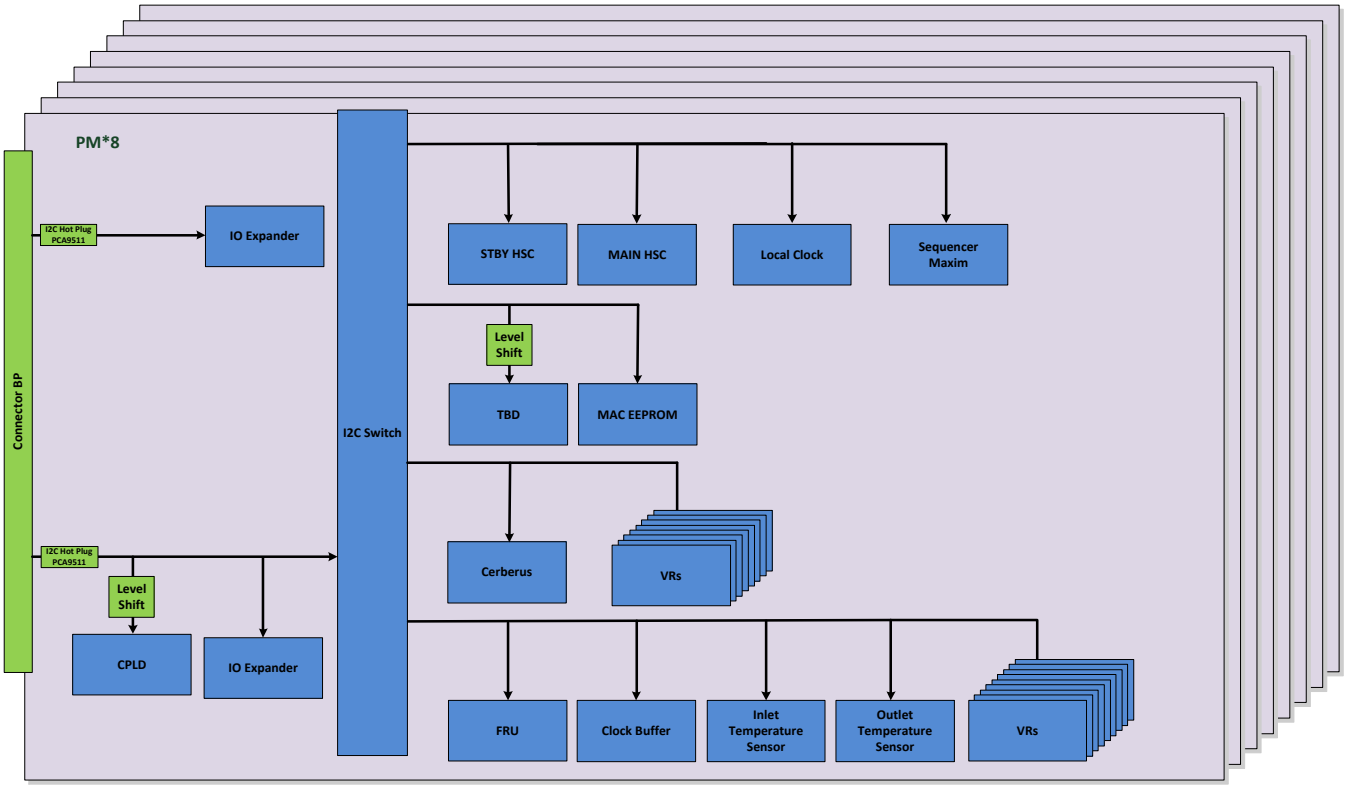


Figure 22 PM I2C Block Diagram (Buffers between voltage domains not shown)

The I2C Switch has 4 Channels. The Table below shows which channel has which components.

	Device
Channel 0	STBY HSC
	MAIN HSC
	IO Expander
	Local Clock
	Sequencer
Channel 1	MAC EEPROM
	TBD
Channel 2	Cerberus
	VRs
Channel 3	FRU
	Clock Buffer
	Inlet Temperature Sensor
	Outlet Temperature Sensor
	VRs

Table 12 PM I2C Switch

7.2.4.1. Voltage regulators

PMBus for telemetry of output current, output voltage, input voltage and junction temperature.

7.2.4.2. Local Clock

To enhance the flexibility and function of the clock synthesizer, an I2C interface is provided. Through the I2C interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the I2C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

7.2.4.3. CPLD

Every MachXO3L/LF device contains two I2C IP cores. These are the primary and secondary I2C IP cores. Either of the two cores can be configured either as an I2C master or as an I2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

7.2.4.4. Inlet/Outlet Temperature Sensor (TMP75)

The TMP75 is a remote temperature sensor monitor with a built-in local temperature sensor. The device communicates with DC-SCM to program the alarm thresholds and to read temperature data. The TMP75 needs to be calibrated to accurately read the PM ambient temperature via the remote temperature sensor monitor.

7.2.4.5. FRU ID EEPROM (MRP 24AA1026T-I)

The MRP 24AA1026T-I/SN or equivalent is a 1024Kb serial EEPROM accessed over I2C from DC-SCM. It is used for tracking manufacturing information in the field. Contents of the FRUID EEPROM are defined in the Shasta FRUID Specification.

7.2.4.6. Main/Standby Power Hot Swap Controller

The power subsystem includes a hot swap controller with I2C interface connected to DC-SCM. This device allows DC-SCM to monitor total power consumed by the PM.

7.2.4.7. MAC EEPROM (ST M24128-BRMN6TP)

The ST M24128-BRMN6TP or equivalent is a 128Kb serial EEPROM accessed over I2C from DC-SCM. It is used to store the starting MAC address and the count (8) of total MAC addresses for the two network interface ports.

7.2.4.8. Sequencer (MAX34452)

From a software perspective, the device appears as a PMBus device capable of executing a subset of PMBus commands. The device employs a number of standard SMBus protocols (e.g.,

Write Word, Read Word, Write Byte, Read Byte, Send Byte, etc.) to program output voltage and warning/fault thresholds, read monitored data, and provide access to all manufacturer-specific commands.

7.2.4.9. Cerberus

The module supports three I2C interfaces to the RoT Processor.

- I2C0 is connected to FC3 I2C port on the RoT. This bus is a multi-master bus used for external communication to Cerberus. It will typically be connected to a BMC. For maximum reliability, this should be a dedicated bus between Cerberus and the external processor. If it is required that other I2C devices be put on this bus, only other multi-master I2C devices should be added.
- I2C1 is connected to FC4 I2C port on the RoT. This bus is expected to be mastered by the RoT with external slave devices on the main board. This will typically be connected to the main board CPLD to support additional platform flows.

7.2.4.10. I2C Switch

The PCA9544A is a 1-of-4 bi-directional translating multiplexer, controlled via the I2C-bus. The SCL/SDA upstream pair fans out to four SCx/SDx downstream pairs, or channels. The downstream pairs connect to STBY HSC, Main HSC, IO expander, local clock, sequencer, MAC EEPROM, Cerberus, VRs, FRU, clock buffer, Inlet and outlet temperature sensor in each PM. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register.

7.2.4.11. I2C GPIO Expander For PM Reset signals (PCA9575)

This expander is used to toggle GPIO to reset I2C devices in the system. The PCA9575 provides 16 bits of GPIO expansion. Any of the 16 I/O ports can be configured as an input or output independent of each other and default on start-up to inputs.
I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum.
The output stage consists of two banks each of 8-bit configuration registers, input registers, interrupt mask registers, output registers, bus-hold and pull-up/pull-down registers and polarity inversion registers. These registers allow the system master to program and configure 16 GPIOs through the I2C-bus.

BMC I2C Bus	I2C Switch Channel	Pin	Signals	I/O	Description
I2C [3:10]	Channel 0	P00	TBD	TBD	TBD
I2C [3:10]	Channel 0	P01	TBD	TBD	TBD

I2C [3:10]	Channel 0	P02	TBD	TBD	TBD
I2C [3:10]	Channel 0	P03	TBD	TBD	TBD
I2C [3:10]	Channel 0	P04	TBD	TBD	TBD
I2C [3:10]	Channel 0	P05	TBD	TBD	TBD
I2C [3:10]	Channel 0	P06	TBD	TBD	TBD
I2C [3:10]	Channel 0	P07	TBD	TBD	TBD
I2C [3:10]	Channel 0	P08	TBD	TBD	TBD
I2C [3:10]	Channel 0	P09	TBD	TBD	TBD
I2C [3:10]	Channel 0	P10	TBD	TBD	TBD
I2C [3:10]	Channel 0	P11	TBD	TBD	TBD
I2C [3:10]	Channel 0	P12	TBD	TBD	TBD
I2C [3:10]	Channel 0	P13	TBD	TBD	TBD
I2C [3:10]	Channel 0	P14	TBD	TBD	TBD
I2C [3:10]	Channel 0	P15	TBD	TBD	TBD
I2C [3:10]	Channel 0	P16	TBD	TBD	TBD
I2C [3:10]	Channel 0	P17	TBD	TBD	TBD

Table 13 I2C GPIO Expander For PM Reset signals Pin Assignments

7.2.5. I2C GPIO Expander For CMM PCIe Switch

This GPIO expander is for PCIe hot-plug interface. The PCA9575 provides 16 bits of GPIO expansion. Any of the 16 I/O ports can be configured as an input or output independent of each other and default on start-up to inputs.
I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum. PCA9575 has built-in level shifting feature that makes these

devices extremely flexible in mixed signal environments where communication between incompatible I/Os is required.
The output stage consists of two banks each of 8-bit configuration registers, input registers, interrupt mask registers, output registers, bus-hold and pull-up/pull-down registers and polarity inversion registers. These registers allow the system master to program and configure 16 GPIOs through the I2C-bus.

PCIe Switch I2C Bus	Pin	Signal name	I/O	Description
I2C [1]	P00	CHIP_PRSNT_N	I	ASIC present
I2C [1]	P01	PCIe_PWR_EN	O	Enable PCIe power
I2C [1]	P02	ATTN_N	I	Attention enable
I2C [1]	P03	Set_SHP_ADDR	I	Set serial hot plug address
I2C [1]	P04	TBD	TBD	TBD
I2C [1]	P05	TBD	TBD	TBD
I2C [1]	P06	TBD	TBD	TBD
I2C [1]	P07	TBD	TBD	TBD
I2C [1]	P08	TBD	TBD	TBD
I2C [1]	P09	TBD	TBD	TBD
I2C [1]	P10	TBD	TBD	TBD
I2C [1]	P11	TBD	TBD	TBD
I2C [1]	P12	TBD	TBD	TBD
I2C [1]	P13	TBD	TBD	TBD
I2C [1]	P14	TBD	TBD	TBD
I2C [1]	P15	TBD	TBD	TBD
I2C [1]	P16	TBD	TBD	TBD
I2C [1]	P17	TBD	TBD	TBD

Table 14 I2C GPIO Expander For CMM PCIe Switch Pin Assignments

7.2.6. Inlet and Outlet Temperature Sensors

The PM has two TMP75 temperature sensors. One for Inlet and one for Outlet. The critical values are still TBD.

7.2.7. External 400GE Connection

Here is a use case example in which PM includes 1 impulse 4x4 DC connector for network connections from the PM to the top-of-rack (TOR) network switch (or external NIC). The connectors interfacing 400GbE shall be Molex MPN 173540-9018 or equivalent.

TBD

Figure 23 Impulse 4x4 DC Connector Illustration

The table below shows the pin mapping for the cable:

Pin	Function	Pin Qty	Description
A1	TX1_P	1	PCIe GEN4 transceiver lane 1 positive signal
B1	TX1_N	1	PCIe GEN4 transceiver lane 1 negative signal
C1	TX2_P	1	PCIe GEN4 transceiver lane 2 positive signal
D1	TX2_N	1	PCIe GEN4 transceiver lane 2 negative signal
E1	RX1_P	1	PCIe GEN4 receiver lane 1 positive signal
F1	RX1_N	1	PCIe GEN4 receiver lane 1 negative signal
G1	RX2_P	1	PCIe GEN4 receiver lane 2 positive signal
H1	RX2_N	1	PCIe GEN4 receiver lane 2 negative signal
A2	TX3_P	1	PCIe GEN4 transceiver lane 3 positive signal
B2	TX3_N	1	PCIe GEN4 transceiver lane 3 negative signal
C2	TX4_P	1	PCIe GEN4 transceiver lane 4 positive signal
D2	TX4_N	1	PCIe GEN4 transceiver lane 4 negative signal
E2	RX3_P	1	PCIe GEN4 receiver lane 3 positive signal
F2	RX3_N	1	PCIe GEN4 receiver lane 3 negative signal
G2	RX4_P	1	PCIe GEN4 receiver lane 4 positive signal
H2	RX4_N	1	PCIe GEN4 receiver lane 4 negative signal

Table 15 Impulse 4x4 DC Connector Pinout

7.2.8. PM Backplane Connector Pin List

PM backplane connector detailed in Table 16. The connectors interfacing 400GbE shall be Molex MPN 171320-9034 or equivalent. Refer to "Shasta pin list_20220913".

Function	Signals	Pin Qty	Description
PCIe	PCIe GEN3 TX_P	1	PCIe to CMM
	PCIe GEN3 RX_P	1	PCIe to CMM
	PCIe GEN3 TX_N	1	PCIe to CMM
	PCIe GEN3 RX_N	1	PCIe to CMM
	PCIe GEN3 CLK_P	1	PCIe clock to CMM
	PCIe GEN3 CLK_N	1	PCIe clock to CMM
I2C to PM devices	I2C_SCL	1	I2C from DC_SCM of CMM
	I2C_SDA	1	I2C from DC_SCM of CMM

PM Present	Present	1	PM present output
PCIe Switch	I2C_SCL (Master)	1	I2C from PCIe switch of CMM for Hot Plug
	I2C_SDA (Master)	1	I2C from PCIe switch of CMM for Hot Plug
MISC	Alert/Interrupt	1	Alert and/or Interrupt from PM
	Throttle	1	Throttle from CMM
SPI	MISO (SPI from BMC to Cerberus)	1	SPI
	MOSI (SPI from BMC to Cerberus)	1	SPI
	CLK (SPI from BMC to Cerberus)	1	SPI
	CS_N (SPI from BMC to Cerberus)	1	SPI
	IO2 (SPI from BMC to Cerberus)	1	SPI Quad
	IO3 (SPI from BMC to Cerberus)	1	SPI Quad
SGPIO	In	1	SGPIO from CMM for sideband signals
	Out	1	SGPIO from CMM for sideband signals
	LD	1	SGPIO from CMM for sideband signals
	CLK	1	SGPIO from CMM for sideband signals

Table 16 PM Backplane Connector pin list

7.2.9. PM Power Architecture

The PM power architecture will vary depending on the solution user design in. The PM power block diagram shown in Figure 24 and table 17 is a use case of example. The capacity of each voltage converter is sized to conservatively provide maximum power for the rail, independent of the total power budget for the PM respectively. All voltage sources must meet the respective component manufacturer's recommended operating conditions.

Standby power:

1. P12V_STBY is enabled by P12V_IN.
2. P3V3_STBY is enabled by P12V_STBY.
3. P1V8_STBY is enabled by P3V3_STBY power good.

Main power:

1. P12V is enabled by CPLD after CPLD gets HPM_STBY_EN is high.
2. P3V3, P1V8 are enabled by sequencer.

Input Source	Power Rail	Power Rail	Current
P12V	P3V3_QSFP	3.3V	TBD
P12V	P1V8	1.8V	TBD
P12V	P3V3	3.3V	TBD
P12V_IN	P12V	12V	TBD
P12V_STBY	P1V8_STBY	1.8V	TBD
P12V_STBY	P3V3_STBY	3.3V	TBD
P12V_IN	P12V_STBY	12V	TBD

Table 17 PM Power Distribution

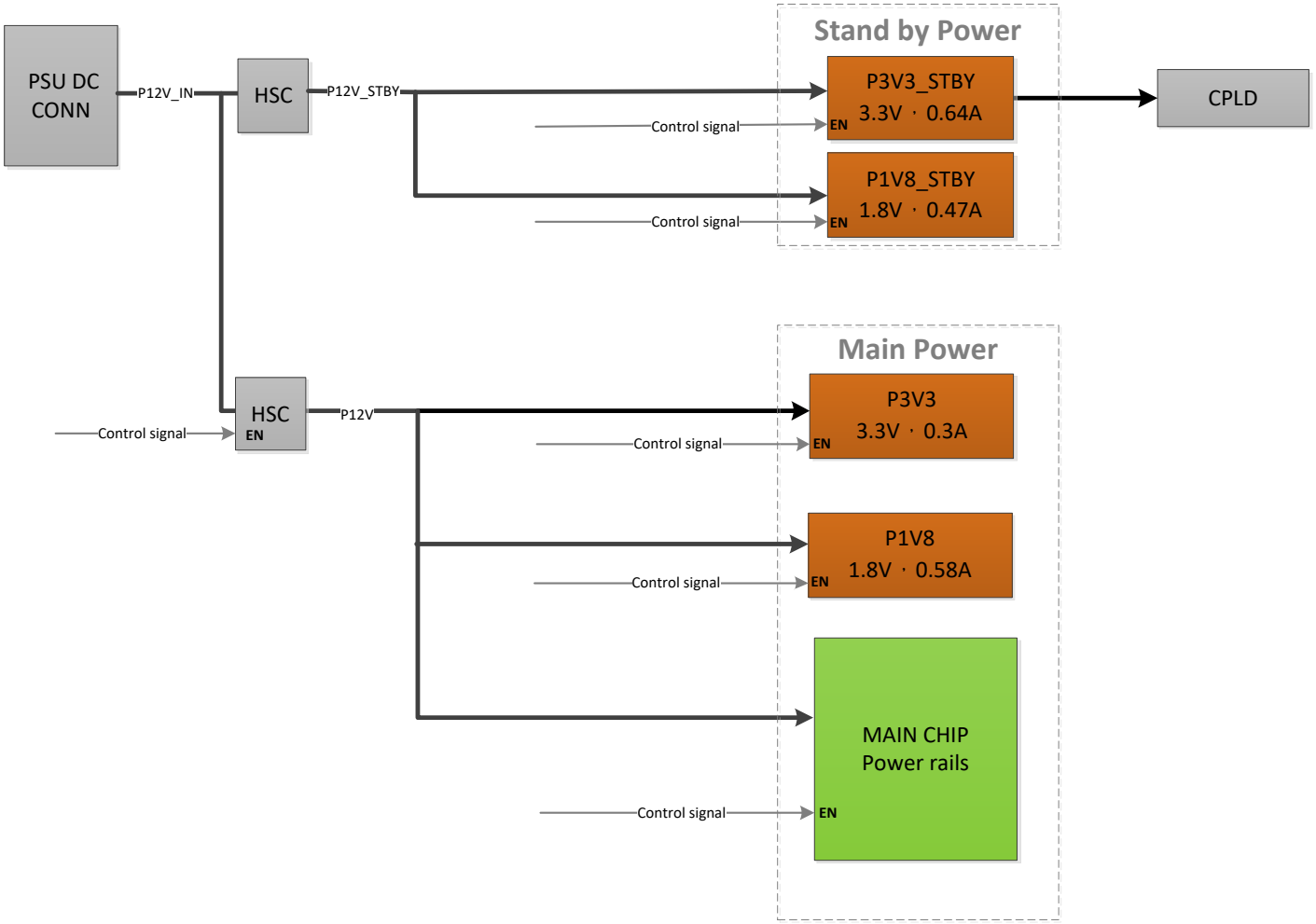


Figure 24 PM Power Block Diagram example

7.2.10. PM Power sequencing

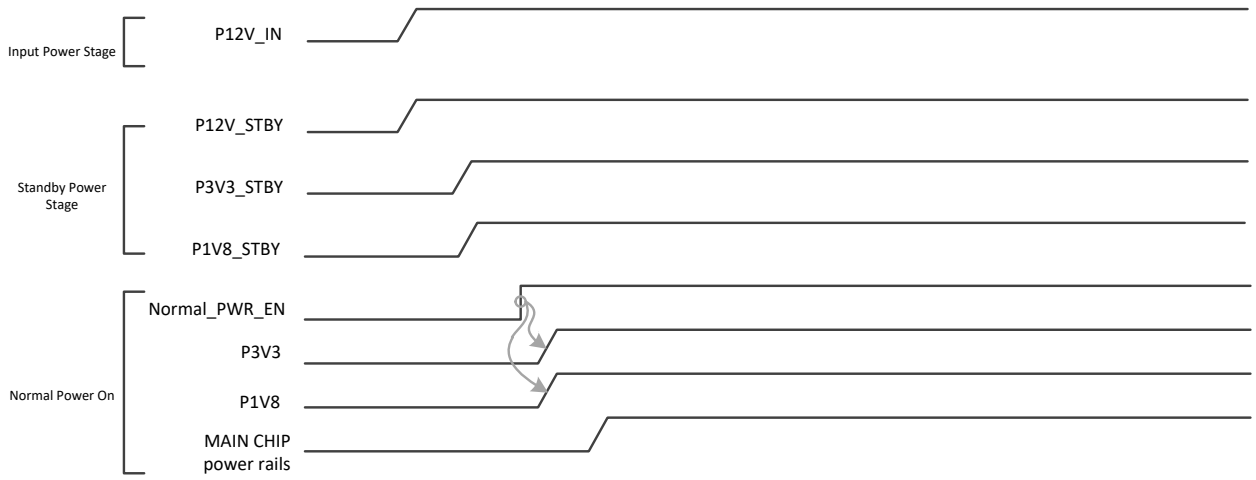


Figure 25 PM Power Sequencing

7.2.11. PM Clock Block Diagram

The PM uses the SI52202 to generate the 100 MHz PCI-E Clock. This clock generator is PCI-E Gen 5 compliant. There is a fanout buffer (LMK00334) which then feeds the clocks. For spread spectrum purposes there is a 100 MHz clock that is coming from the Head Node; which is being fed into the Clock buffer. Below is the block diagram for this:

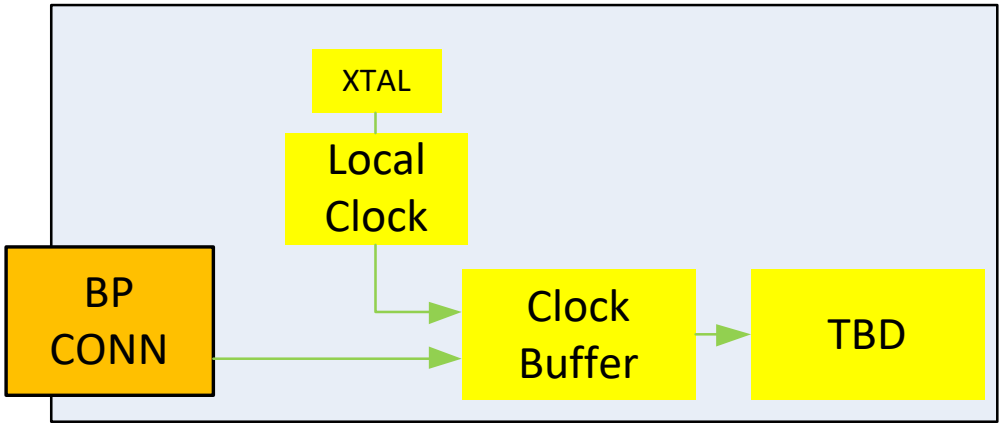


Figure 26 PM Clock Block Diagram

7.2.12. PM SPI Block Diagram

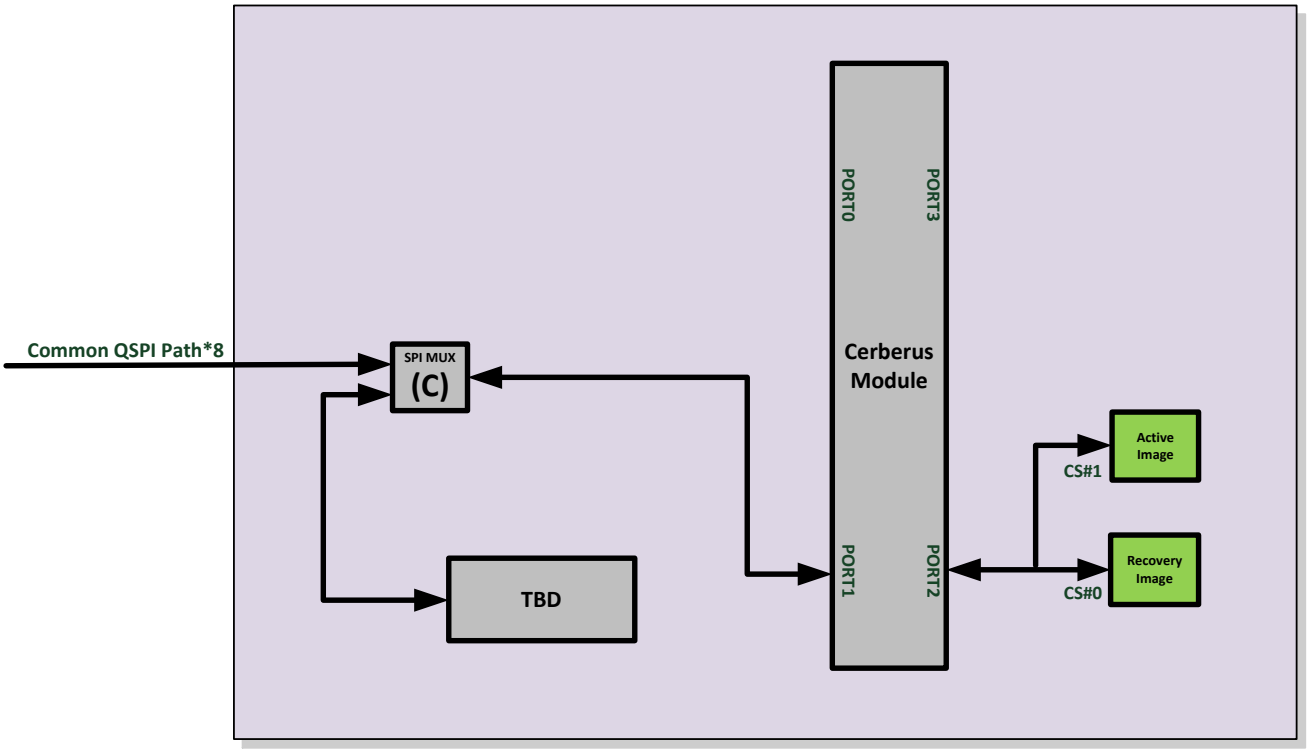


Figure 27 PM SPI Block Diagram

8. Thermal Design Requirements

There are two type of modules which are PM & CMM in system. The maximum power support of main chip for PM is 500W; The maximum power support of main chip for CMM is 30W. The chipset operating temperature sets the limits for which the system must be designed to meet. PM & CMM card operating conditions may verify with respect to inlet temperature, airflow, and heatsink design. It is up to the system designer to consider these variables and meet the temperature limits specified in this document.

9. I/O System

9.1. PCI Express Interface

The Shasta contains two PCIe interfaces.

- PCIe Gen4 x8 from head-node to CMM PCIe switch via a PCIe cable and 2 MiniSAS x4 connectors.
- PCIe Gen4 x1 from CMM PCIe switch to each PM via a Gen4 x1 Cable BP and BP connector.

Because the system will be used in rack with a generic server, it must meet the PCIe electrical specifications. PCIe SIG compliance and interoperability testing is required.
The rack PCIe topology is shown in Figure 28.

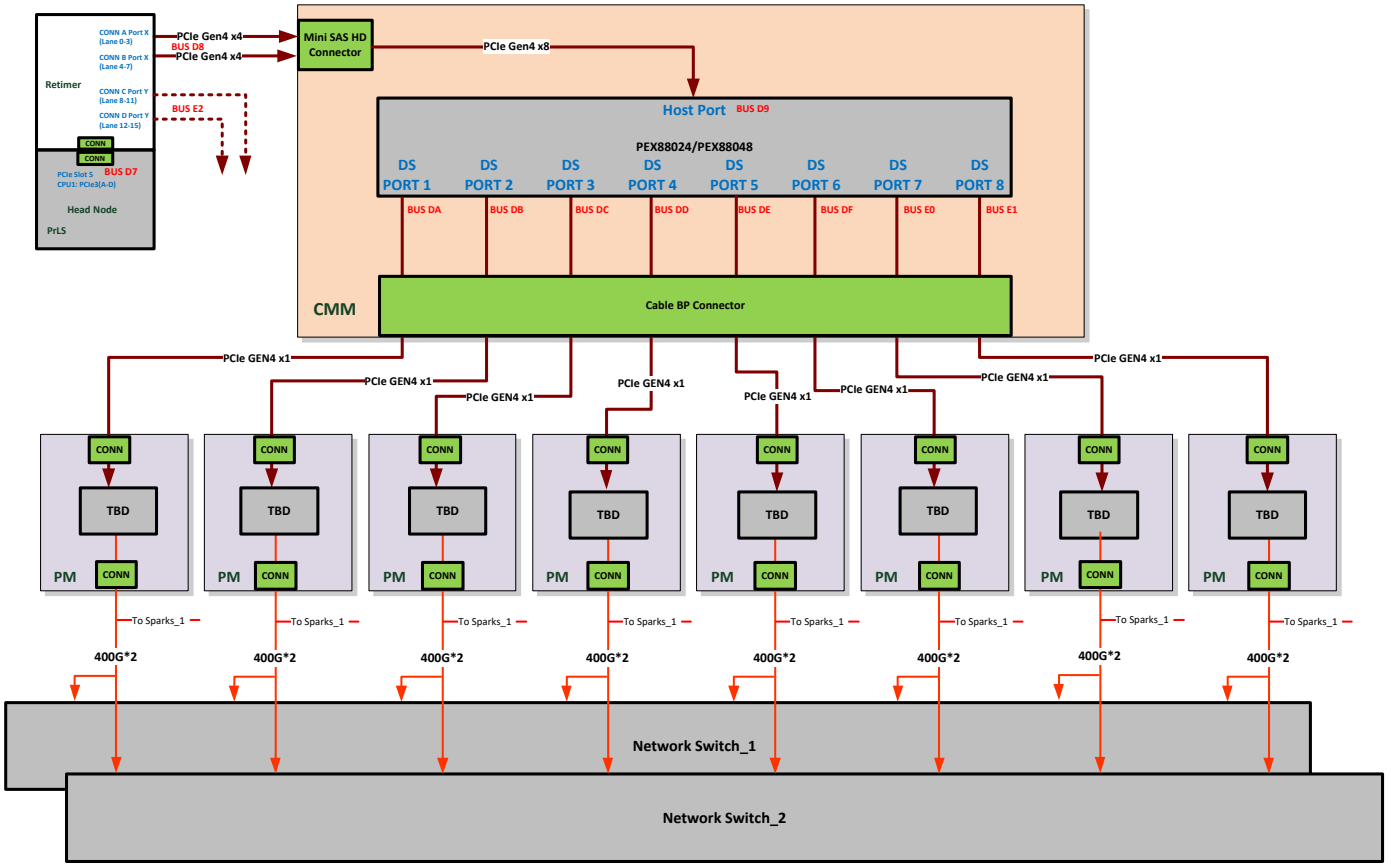


Figure 28 PCIe Topology

9.1.1. External PCIe Interface

The Shasta interfaces with head-node through two standard MiniSAS x4 connectors. Head-node will provide a physical x8 lane PCIe minimum Gen4 interface, including I2C, reset, 1 pair of differential clock signals, to the CMM.
The two standard MiniSAS x4 connectors pin assignment is covered in Table 4. The electrical specification for the primary interface must meet PCI-Express Gen 4.0 Specifications. The external MiniSAS HD interface shall be verified to pass the PCIe electrical compliance tests.

9.1.2. Internal PCIe Interface

The internal PCIe switch connect Gen4 x8 head-node interface (CMM) to each PMs over PCIe Gen4 x1 (PM) interface. The purpose of this interface is to provide device management capabilities from head-node.

9.2. One of possible use case - External Network Interface

In one of possible use case Shasta implements 8 4x100Gbs ports to two Top-Of-Rack (TOR) Network Switches. Shasta presents 8 external network interfaces, each supporting 400Gbs Ethernet over a Direct Attached Copper (DAC) cable. Physical connections are made using 8 impulse 4x4 DC connectors.

9.3. LED Indicators

The CMM provides several LEDs to indicate the status of the board. They are used for development and sustaining debug work.
LEDs are located on the front edge of the board to be visible from the front of a running system. See Table 19 for LED definitions and “Location” number. See Figure 29 for LED ordering and location.

Board	Location	Description
CMM	D53	Power Status LED
CMM	D54	UID LED
CMM	D55	Attention LED

Table 18 LED Definitions

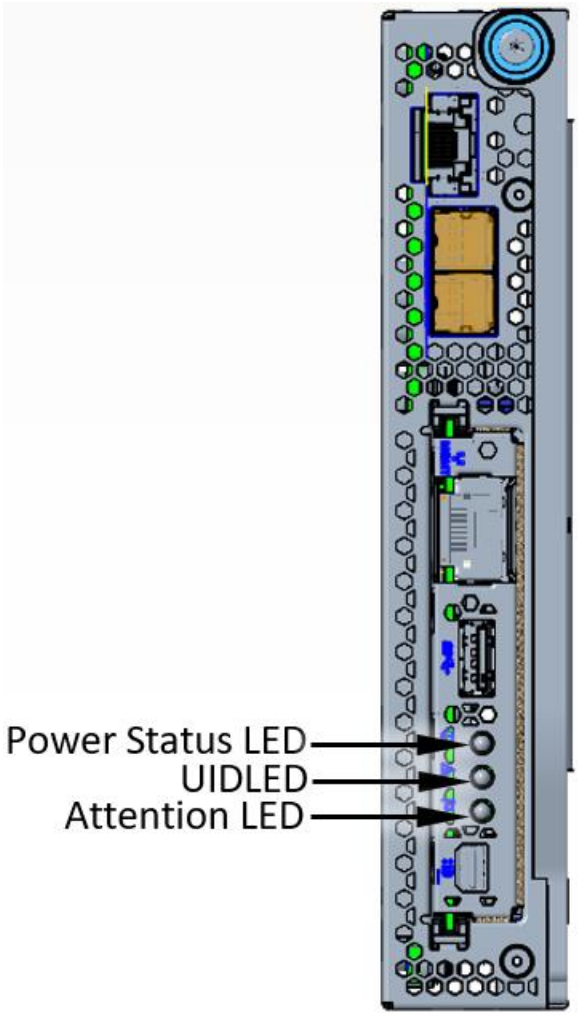


Figure 29 CMM LED Locations

9.4. External Buttons

The CMM has one button located on it.

1. Reset Button

The purpose of this button is TBD, it is connected to the CPLD on the CMM.

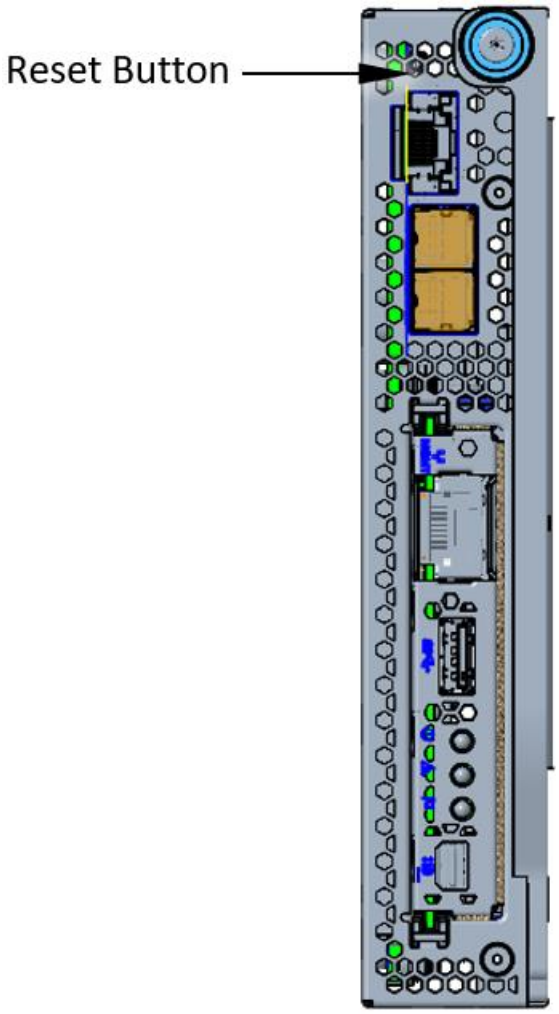


Figure 30 CMM Button Location

9.5. Debug/Test Headers

There should be debug/test headers for hooking up analyzers or an oscilloscope. Examples include:

1. I2C
2. SPI
3. Test pins to unused CPLD Pins
4. Test pins on power nets
5. Debug LEDs
6. Power on Jumper to enable bench testing
7. MAX34452 (Power Sequencer) 3 pin header to access GUI
8. Power header to hook up bench power supply

Any hook that allows for a board to be brought up on the bench would be helpful. This section is still TBD so more additions are welcome.

10. Rear Side Power, I/O, Expansion Board and Midplane Subsystems

10.1. PDB

The major component of the PDB is the CPLD (Lattice, LCMXO3LF-2100C-5BG256C).

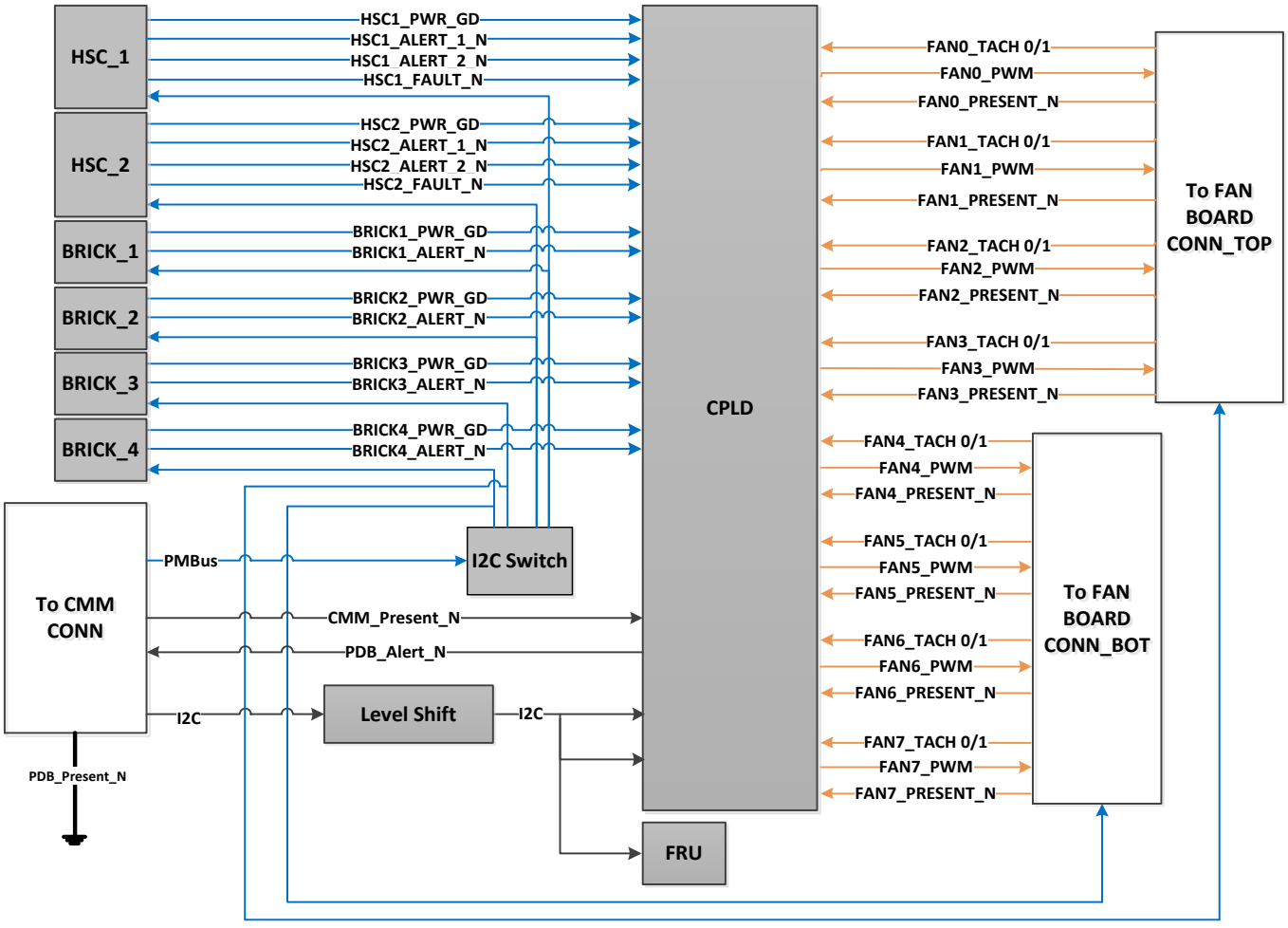


Figure 31 PDB Block Diagram

10.1.1. PDB CPLD

DC-SCM communicates with PDB CPLD (Lattice, LCMXO3LF-2100C-5BG256C) via slave I2C to implement HSC/bricks signals, Fan control signals, and a Hitless update function (online programming doesn't need AC cycle). That can reduce the BP connector and cable signal

quantity between CMM and PDB, such as HSC PG/alert/fault, brick PG/alert, FAN_TCH, FAN_PWM, Fan_PRESENT_N, etc. And, CPLD also would be an intelligent controller to control Fan while CMM is unplugged or damaged.

The below block diagram shows Shasta PDB CPLD block diagram. The Shasta PDB CPLD code provides the following important modules.

- I2C
- PWM module
- RPM module
- Hitless update
- Fan full speed control

Clock	Frequency
System Clock	25M Hz
SMBus	100K Hz

Table 19 PDB Internal Clock

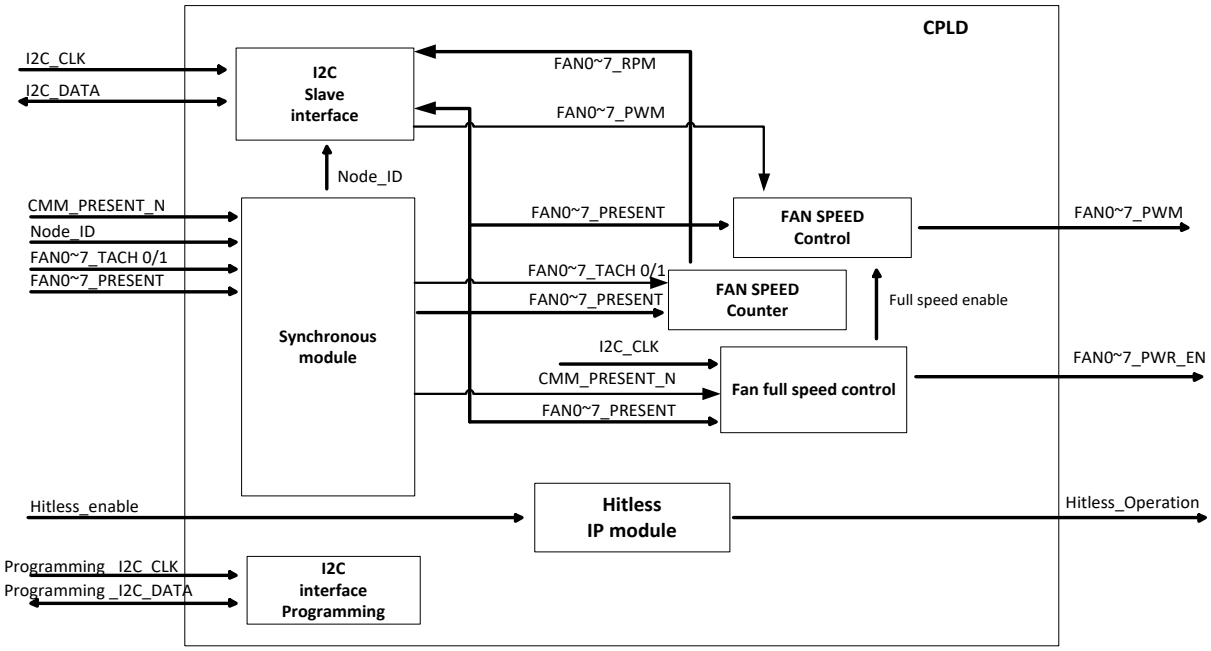


Figure 32 PDB CPLD Block Diagram

10.1.1.1. I2C Interface

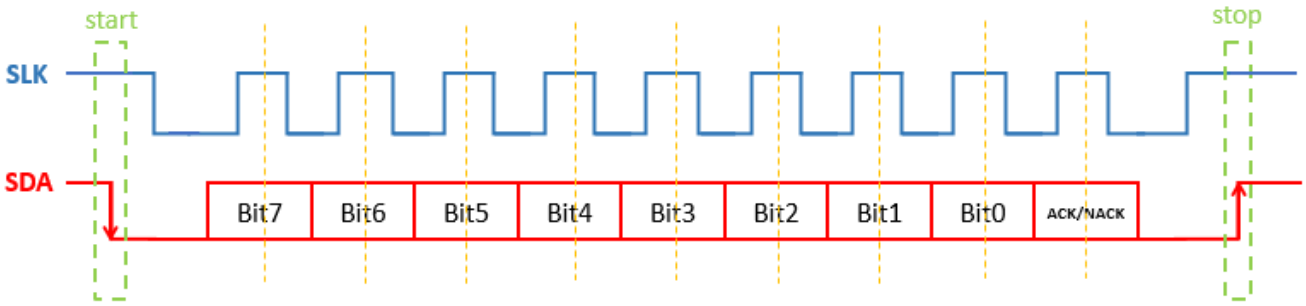


Figure 33 I2C Interface

- Max Frequency：100KHz
- Every data should be 8 bits and after sending data should send ACK data(1bit).
- ACK data is low to response that the data was received.
- Change the data when SLK is low and latch the data when SLK is high.
- The start condition is a high-to-low transition on SDA while SCL is high.
- The stop condition is a low-to-high transition on SDA while SCL is high.

10.1.1.2. FAN SPEED Control

The fan speed control circuit is generated as a 25KHz PWM signal.

The circuit can though i2c register 0x56~0x5B control PWM duty cycle.

The duty maximum is 100%(0x64h).

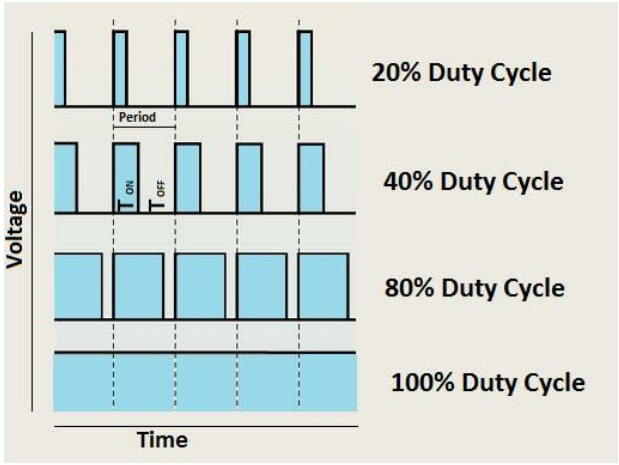
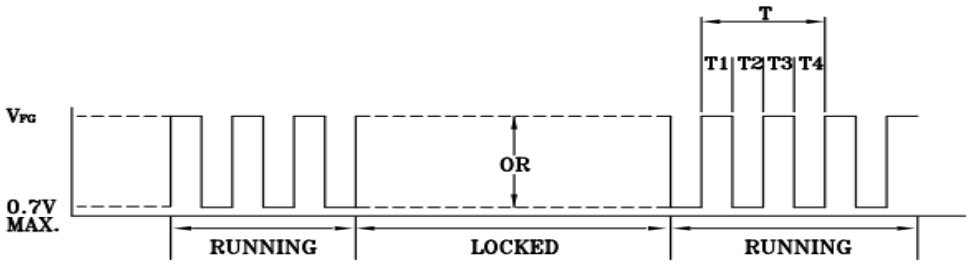


Figure 34 FAN SPEED Control

10.1.1.3. FAN Speed Counter

The fan speed counter circuit will count Fan Tach signal, use calculation formula to get RPM, calculation formula as shown below.

The calculation result is shown to i2c register 0x06h~0x1Dh.



T=T1+T2+T3+T4=60/N (Sec) N: SPEED (RPM)

Figure 35 FAN SPEED Counter

10.1.1.4. Hitless I/O

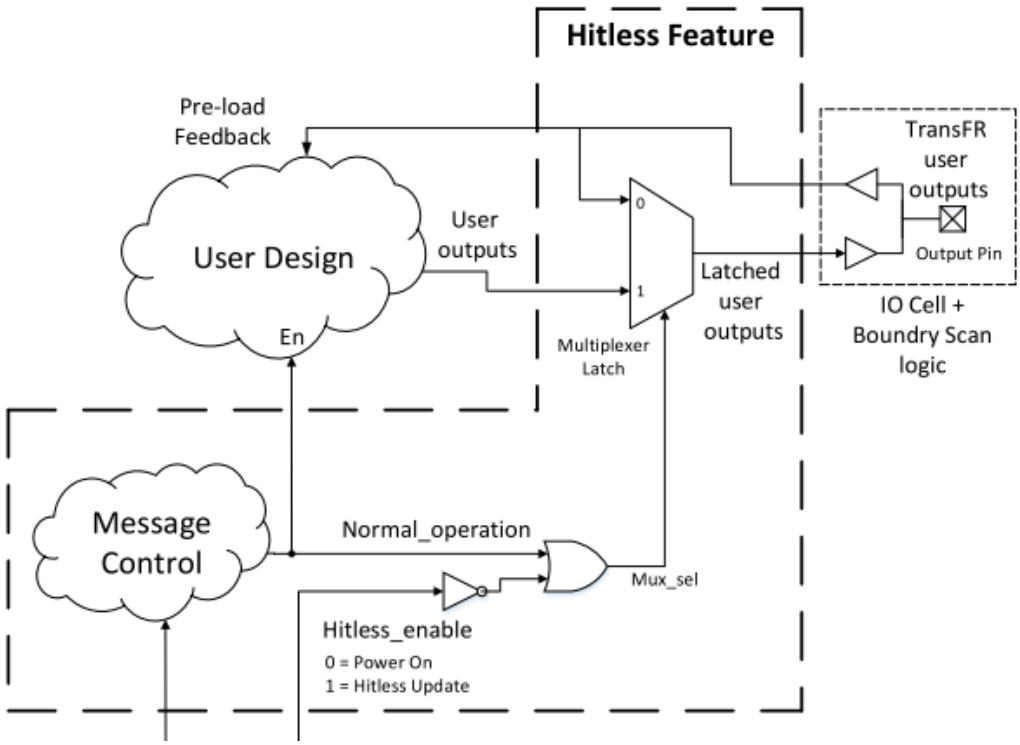


Figure 36 Hitless I/O

A Normal_operation signal is used to support the hitless I/O circuit. Normal_operation must have a default global reset signal GSR value of False.

A Hitless_enable signal is used to control multiplexer latch.

The TransFR circuit in the Boundary Scan logic in the I/O cell latches the output value.

If user needs to update CPLD FW, hitless_enable is asserted.

The Hitless_enable is active high, multiplexer latch switch to 0, TransFR Boundary Scan logic holds the output states.

Wait update FW done, hitlees_enable is then de-asserted.

Hitless_enable	Normal_operation	User Design Output
X	1	Normal Operation
0	0	User Defined Power-up State
1	0	User Defined Hold/Preload State

Table 20 Hitless setting

The hitless I/O logic must cover two primary scenarios: Power-up and Hitless Reconfiguration. The control input Hitless_en is driven by an external controller to determine which scenario is active.
If Hitless_en is false, the user logic starts from a power-up reset state. If true, the user logic can utilize the values held in the TransFR Boundary Scan I/O cells to initialize the control logic to resume from the pre-update state.

10.1.2. PDB I2C Bus Components

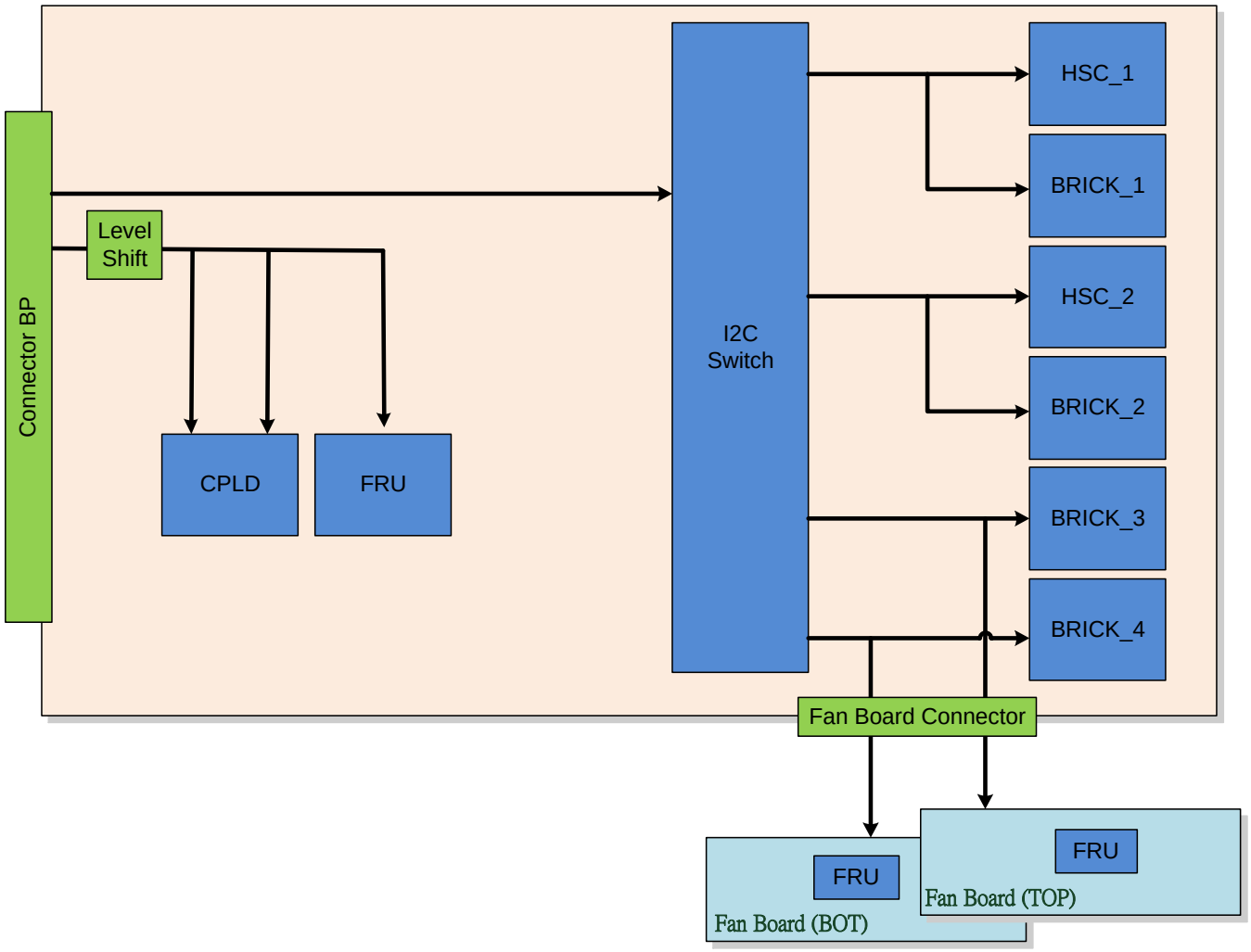


Figure 37 PDB I2C Block Diagram

10.1.2.1. CPLD

CPLD for fan control and GPIO expansion…etc. Every MachXO3L/LF device contains two I2C IP cores. These are the primary and secondary I2C IP cores. Either of the two cores can be configured either as an I2C master or as an I2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

10.1.2.2. FRU ID EEPROM (MRP 24AA1026T-I)

The MRP 24AA1026T-I/SN or equivalent is a 1024Kb serial EEPROM accessed over I2C from DC-SCM. It is used for tracking manufacturing information in the field. Contents of the FRUID EEPROM are defined in the Shasta FRUID Specification.

10.1.2.3. I2C Switch

The PCA9544A is a 1-of-4 bi-directional translating multiplexer, controlled via the I2C-bus. The SCL/SDA upstream pair fans out to four SCx/SDx downstream pairs, or channels. The downstream pairs connect to HSC, bricks and fan board FRU. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register.

10.1.2.4. HSC

PMBus is based on I2C and provides a more robust and fault tolerant bus. Functions such as bus timeout and packet error checking (PEC) are added to help achieve this robustness, together with more specific definitions of the bus messages used to read and write data to devices on the bus.

10.1.2.5. Brick

A digital PMBus interface to allow the module to be monitored, controlled and configured by the system. Both 100kHz and 400kHz bus speeds are supported by the module.

10.1.3. PDB To CMM Connector Pin List

PDB to CMM detailed in Table 22. Refer to “Shasta pin list_20220913”.

Pin	Signal name	Pin Qty	Description
A2	I2C_SDA	1	I2C from CMM for PDB related components, FRU, FAN control and CPLD
A3	I2C_SCL	1	I2C from CMM for PDB related components, FRU, FAN control and CPLD
A5	PMBus_SCL	1	PMBus to fan boards FRU, HSC and bricks

A6	PMBus_SDA	1	PMBus to fan boards FRU, HSC and bricks
A8	CMM_PRESENT_N	1	CMM present input
A11	PDB_PRESENT_N	1	PDB present output
A12	PDB_ALERT_N	1	PDB alert

Table 21 PDB To Backplane Connector Pin List

10.1.4. PDB To Fan Boards Connector Pin List

PDB to fan boards Connectors detailed in Table 23, 24, 25 and 26. Refer to “Shasta pin list_20220913”.

Pin	Signal name	I/O	Description
1	FAN0_TACH0	Input	Fan Tachometer
2	FAN2_TACH0	Input	Fan Tachometer
3	FAN0_TACH1	Input	Fan Tachometer
4	FAN2_TACH1	Input	Fan Tachometer
5	FAN0_PWM	Output	Fan PWM
6	FAN2_PWM	Output	Fan PWM
7	FAN0_PRESENT	Input	Fan Present
8	FAN2_PRESENT	Input	Fan Present
9	FAN1_TACH0	Input	Fan Tachometer
10	FAN3_TACH0	Input	Fan Tachometer
11	FAN1_TACH1	Input	Fan Tachometer
12	FAN3_TACH1	Input	Fan Tachometer
13	FAN1_PWM	Output	Fan PWM
14	FAN3_PWM	Output	Fan PWM
15	FAN1_PRESENT	Input	Fan Present
16	FAN3_PRESENT	Input	Fan Present
17	I2C_FAN_TOP_SCL	Output	I2C clock for fan board FRU
18	GND	NA	Ground
19	I2C_FAN_TOP_SDA	I/O	I2C data for fan board FRU
20	GND	NA	Ground

Table 22 PDB To Fan Boards Signals Connector_TOP Pin List

Pin	Signal name	I/O
1	GND	NA
2	GND	NA
3	GND	NA

4	GND	NA
5	GND	NA
6	GND	NA
7	GND	NA
8	GND	NA
9	GND	NA
10	GND	NA
11	GND	NA
12	GND	NA
13	P48V_FAN	Output
14	P48V_FAN	Output
15	P48V_FAN	Output
16	P48V_FAN	Output
17	P48V_FAN	Output
18	P48V_FAN	Output
19	P48V_FAN	Output
20	P48V_FAN	Output
21	P48V_FAN	Output
22	P48V_FAN	Output
23	P48V_FAN	Output
24	P3V3_STBY	Output

Table 23 PDB To Fan Boards Power Connector_TOP Pin List

Pin	Signal name	I/O	Description
1	FAN4_TACH0	Input	Fan Tachometer
2	FAN6_TACH0	Input	Fan Tachometer
3	FAN4_TACH1	Input	Fan Tachometer
4	FAN6_TACH1	Input	Fan Tachometer
5	FAN4_PWM	Output	Fan PWM
6	FAN6_PWM	Output	Fan PWM
7	FAN4_PRESENT	Input	Fan Present
8	FAN6_PRESENT	Input	Fan Present
9	FAN5_TACH0	Input	Fan Tachometer
10	FAN7_TACH0	Input	Fan Tachometer
11	FAN5_TACH1	Input	Fan Tachometer
12	FAN7_TACH1	Input	Fan Tachometer
13	FAN5_PWM	Output	Fan PWM
14	FAN7_PWM	Output	Fan PWM
15	FAN5_PRESENT	Input	Fan Present
16	FAN7_PRESENT	Input	Fan Present

17	I2C_FAN_BOT_SCL	Output	I2C clock for fan board FRU
18	GND	NA	Ground
19	I2C_FAN_BOT_SDA	I/O	I2C data for fan board FRU
20	GND	NA	Ground

Table 24 PDB To Fan Boards Signals Connector_BOT Pin List

Pin	Signal name	I/O
1	GND	NA
2	GND	NA
3	GND	NA
4	GND	NA
5	GND	NA
6	GND	NA
7	GND	NA
8	GND	NA
9	GND	NA
10	GND	NA
11	GND	NA
12	GND	NA
13	P48V_FAN	Output
14	P48V_FAN	Output
15	P48V_FAN	Output
16	P48V_FAN	Output
17	P48V_FAN	Output
18	P48V_FAN	Output
19	P48V_FAN	Output
20	P48V_FAN	Output
21	P48V_FAN	Output
22	P48V_FAN	Output
23	P48V_FAN	Output
24	P3V3_STBY	Output

Table 25 PDB To Fan Boards Power Connector_BOT Pin List

10.1.5. PDB Power Architecture

The PDB power block diagram is shown in Figure 38 and 39. The capacity of each voltage converter is sized to conservatively provide maximum power for the rail, independent of the total power budget for the PDB. All voltage sources must meet the respective component manufacturer's recommended operating conditions.
Standby power:

1. P12V_1_STBY is enabled by HSC_1 power good.
2. P12V_2_STBY is enabled by HSC_2 power good.
3. P3V3_STBY is enabled by Brick4 power good.
4. P48V_FAN_0/1/2/3/4/5/6/7 are enabled by CPLD when CPLD detects the FAN_PRESENT_N0/1/2/3/4/5/6/7 is low.

Input Source	Power Rail	Power Rail	Current
P48V_IN	P48V_IN_1	48V	TBD
P48V_IN	P48V_IN_2	48V	TBD
P48V_IN_1	P48V_1_STBY	48V	TBD
P48V_IN_2	P48V_2_STBY	48V	TBD
P48V_1_STBY	P12V_1_STBY	12V	TBD
P48V_2_STBY	P12V_2_STBY	12V	TBD
P12V_2_STBY	P3V3_STBY	3.3V	0.03A
P48V_2_STBY	P48V_FAN_0	48V	2.1A
P48V_2_STBY	P48V_FAN_1	48V	2.1A
P48V_2_STBY	P48V_FAN_2	48V	2.1A
P48V_2_STBY	P48V_FAN_3	48V	2.1A
P48V_2_STBY	P48V_FAN_4	48V	2.1A
P48V_2_STBY	P48V_FAN_5	48V	2.1A
P48V_2_STBY	P48V_FAN_6	48V	2.1A
P48V_2_STBY	P48V_FAN_7	48V	2.1A

Table 26 12V PDB Power Distribution

Input Source	Power Rail	Power Rail	Current
P48V_IN	P48V_IN_1	48V	TBD
P48V_IN	P48V_IN_2	48V	TBD
P48V_IN_1	P48V_1_STBY	48V	TBD
P48V_IN_2	P48V_2_STBY	48V	TBD
P48V_1_STBY	P3V3_STBY	3.3V	0.03A
P48V_2_STBY	P48V_FAN_0	48V	2.1A
P48V_2_STBY	P48V_FAN_1	48V	2.1A
P48V_2_STBY	P48V_FAN_2	48V	2.1A
P48V_2_STBY	P48V_FAN_3	48V	2.1A
P48V_2_STBY	P48V_FAN_4	48V	2.1A
P48V_2_STBY	P48V_FAN_5	48V	2.1A
P48V_2_STBY	P48V_FAN_6	48V	2.1A
P48V_2_STBY	P48V_FAN_7	48V	2.1A

Table 27 48V PDB Power Distribution

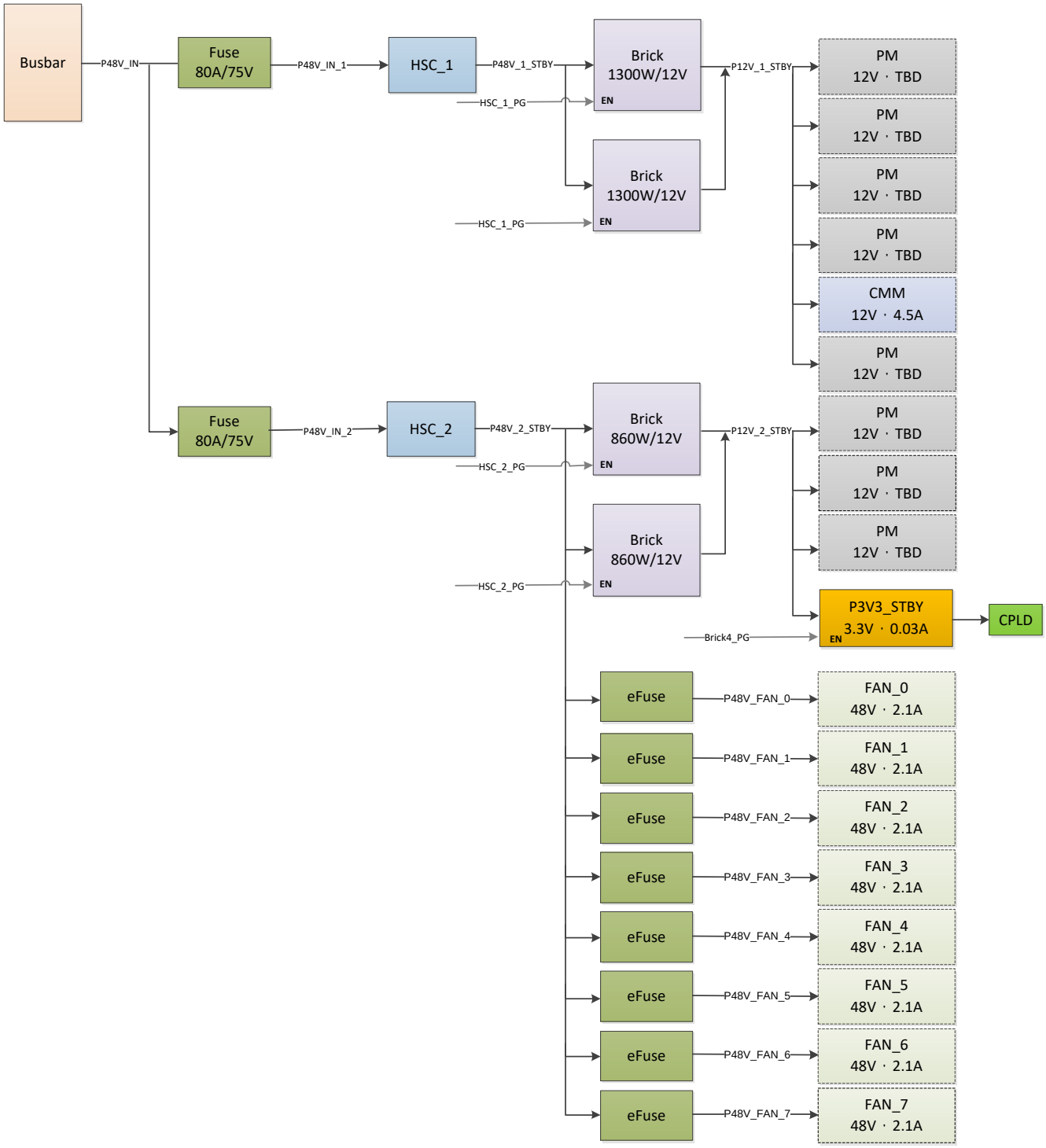


Figure 38 12V PDB Power Block Diagram

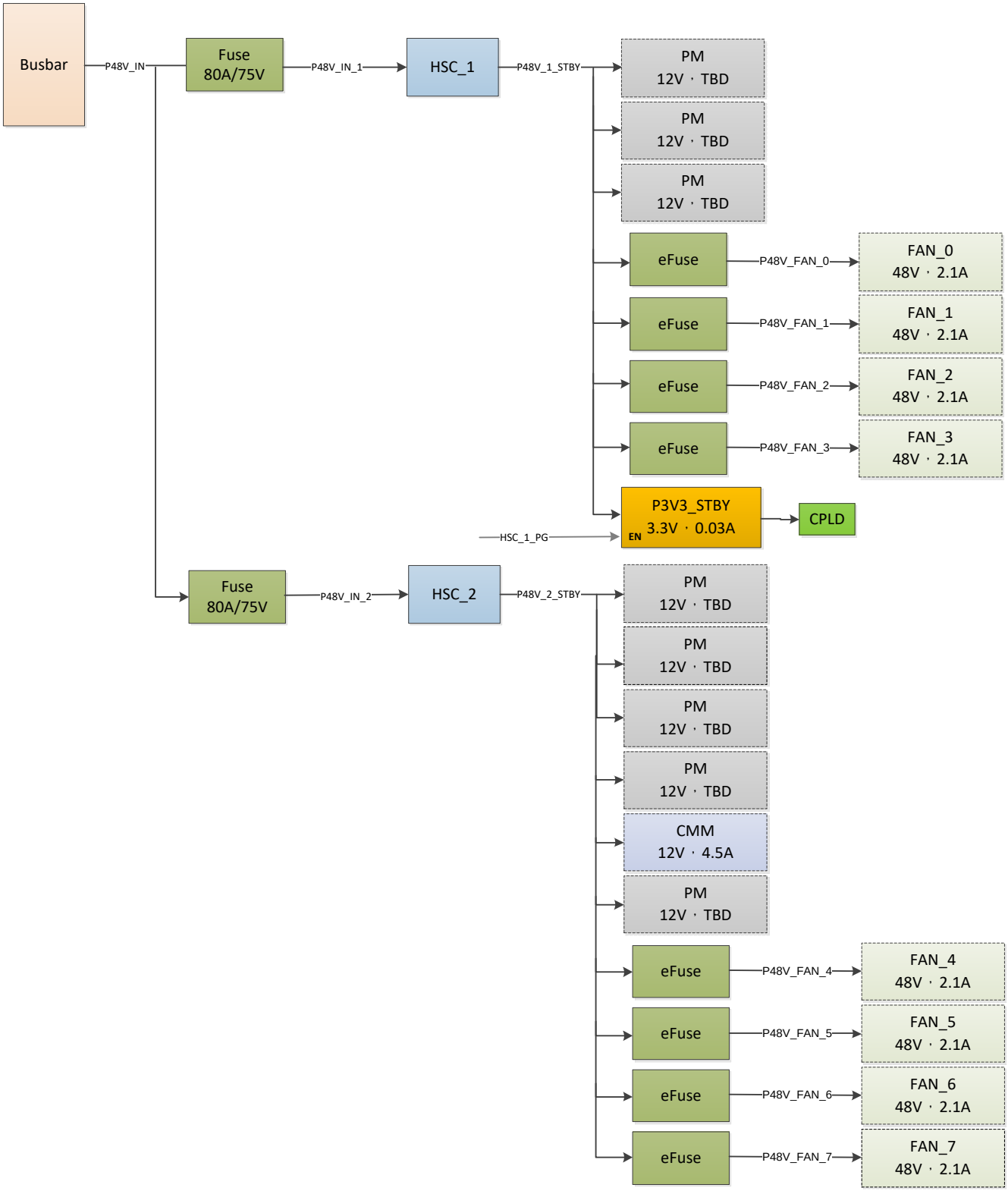


Figure 39 48V PDB Power Block Diagram

10.1.6. PDB Power Sequencing

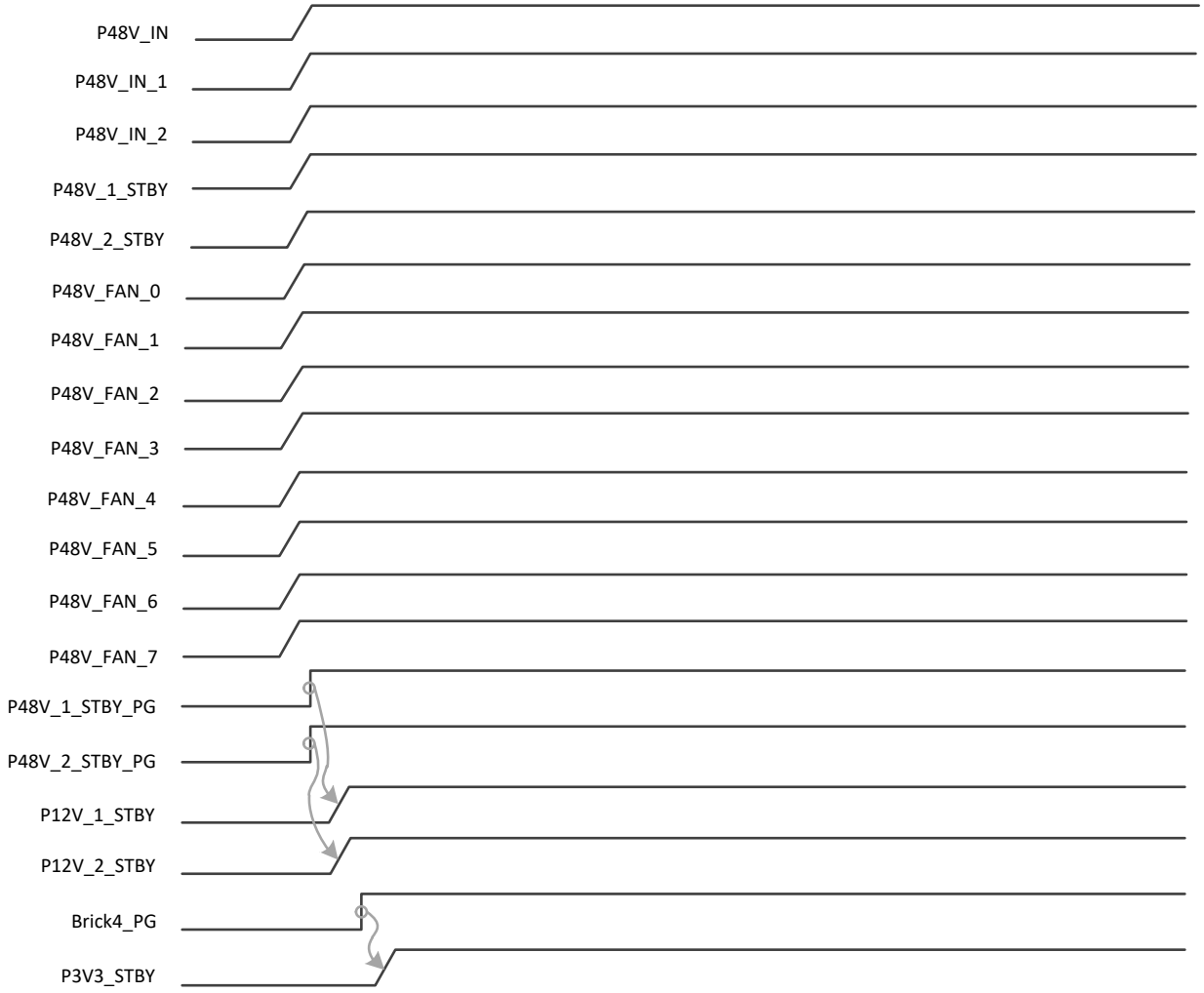


Figure 40 12V PDB Power Sequencing

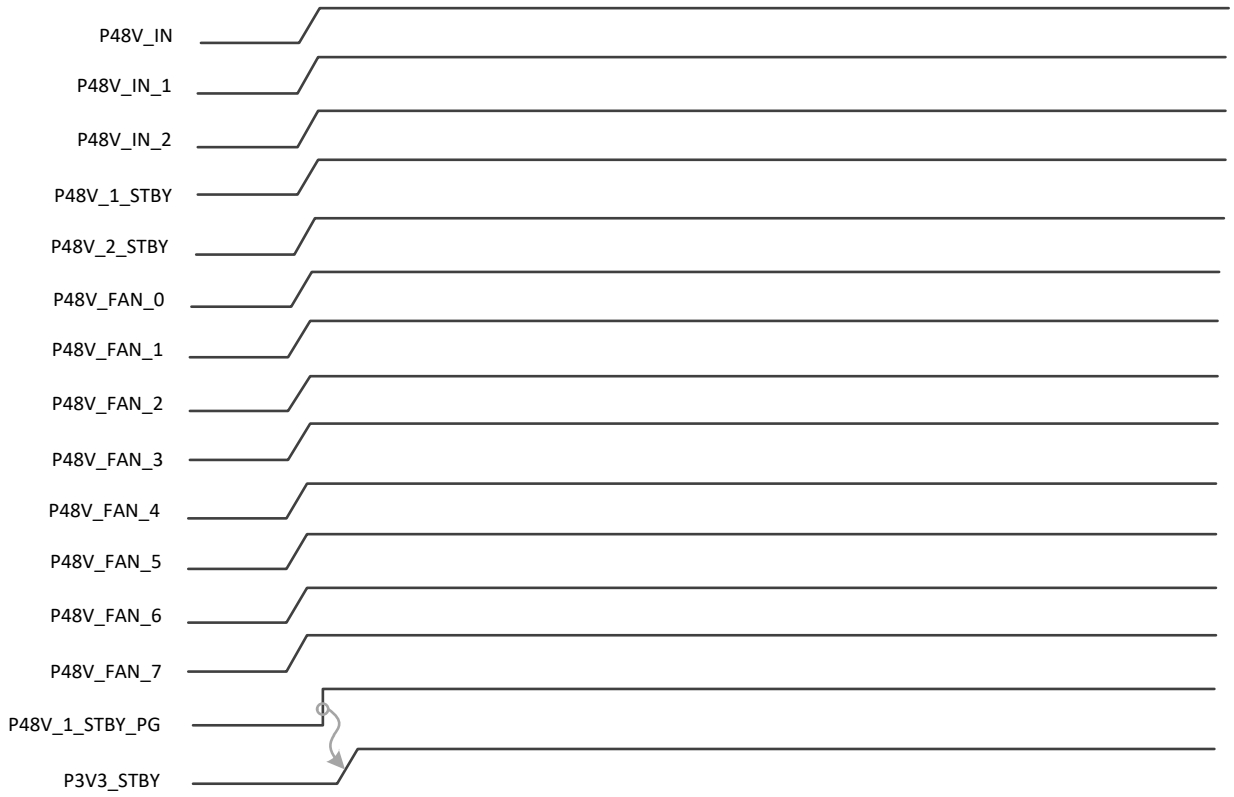


Figure 41 48V PDB Power Sequencing

10.1.7. PDB Stack-up

Table 28 shows the 4-layer PDB PCB stack-up. The stack-up uses material IT-170GRA1 or equivalent. The PCB thickness is 109.8 mils for reference.

STACKUP									
							Target Z (ohms) - MicroStrip	50	Breakout
							Target Z (ohms) - StripLine	50	
							Z tolerance	±10%	
							Z Type	Single	Single
Layer#	**Material**	**Description**	**Copper Weight (oz)**	**Thickness (mil)**	**Tolerance (mil)**	**Glass Fabric**	**Er**	**Width**	**Width**
		Soldermask		0.60			3.8		
1		TOP	0.5+plating	1.95				6.2	4
	IT-170GRA1	PP		3.70	±0.709	2113x1	3.66		
2		GND	2 (RTF)	2.60					
	IT-170GRA1	CORE		92.10	±7.09	Vendor Define	3.97		
3		GND1	2 (RTF)	2.60					
	IT-170GRA1	PP		3.70	±0.709	2113x1	3.66		
4		BOTTOM	0.5+plating	1.95				6.2	4
		Soldermask		0.60			3.8		
			Total	**109.80**	**±10%**				

Table 28 PDB Stack-up

10.1.8. PDB PCB Placement Strategy

Layout views of the PDB showing major component locations are shown in Figure 42.

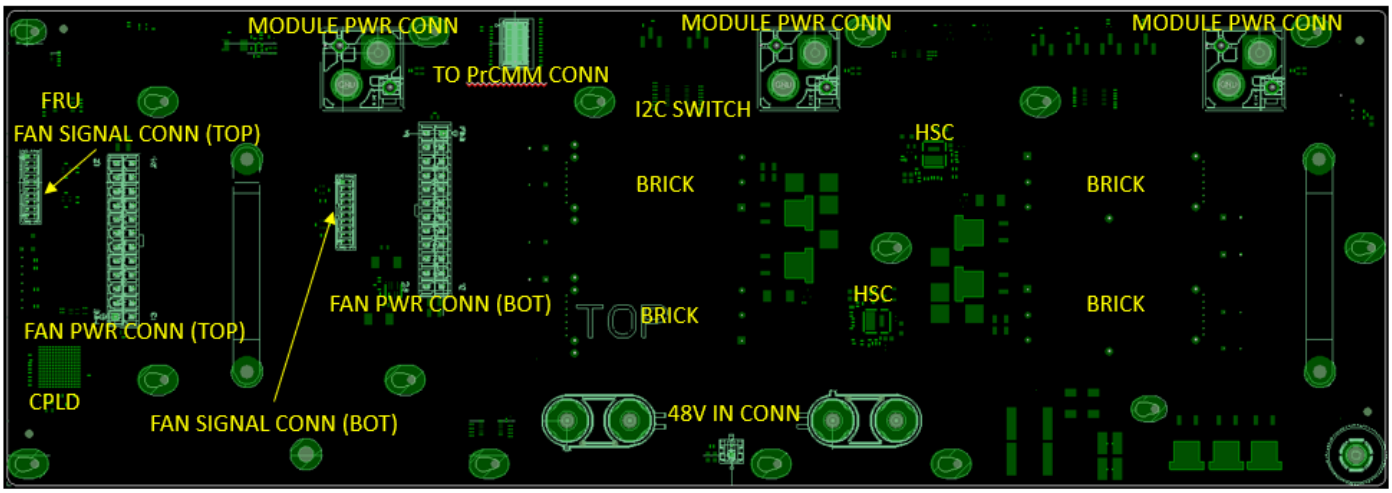


Figure 42 PDB Layout Placement (TOP View)

10.1.9. PDB Power Design

10.1.9.1. PDB Design Option1

Option 1: 12V PDB. (For Shasta design)

- 2 x HSC supplies to CMM/PM/Fan. (HSC_1 supplies to 2 bricks, and HSC_2 supplies to 2 bricks and 8 fans.)
- 2 x 1300W bricks and 2 x 860W bricks.

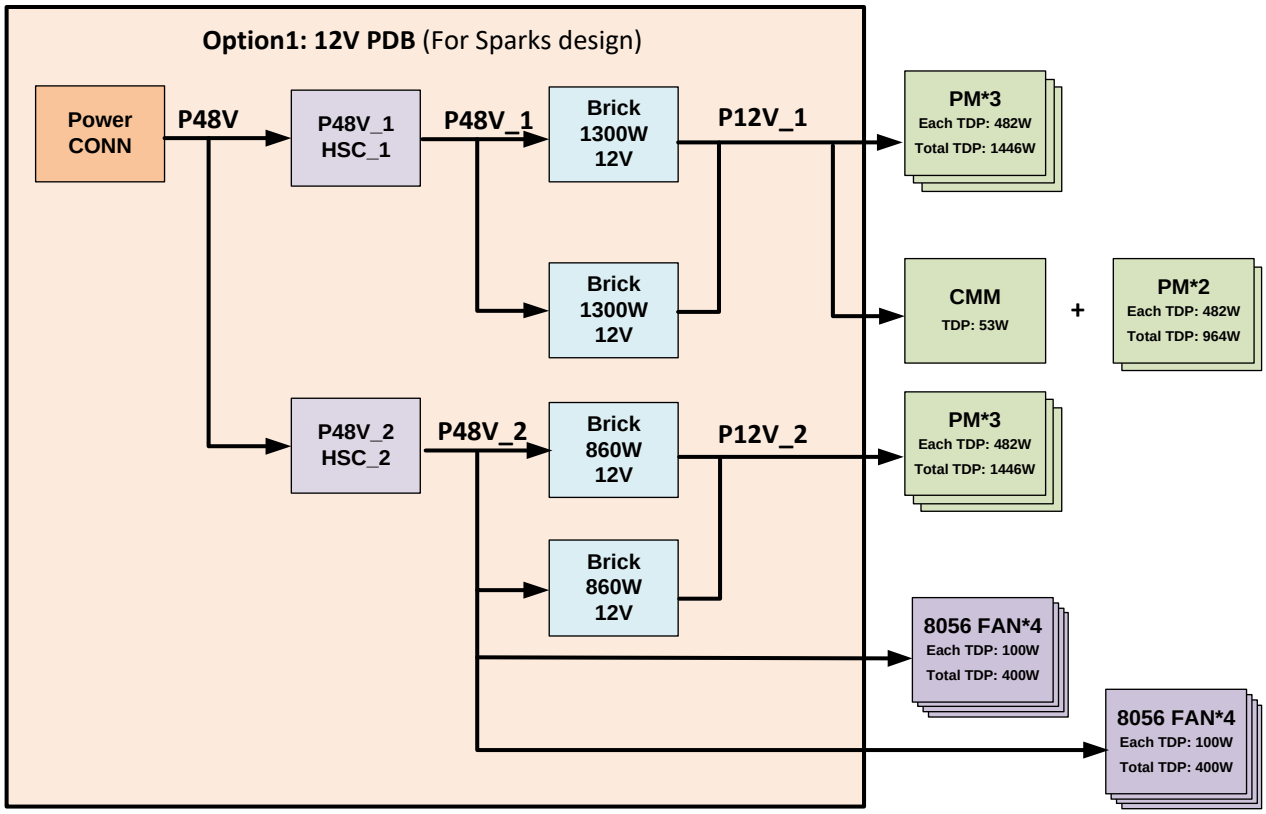


Figure 43 12V PDB. (For Shasta design)

10.1.9.2. PDB Design Option2

Option 2: 48V PDB. (For ASIC/solution support high voltage input)

- 2 x HSC supplies to CMM/PM/Fan. (HSC_1 supplies to PM*3 and Fan*4, and HSC_2 supplies to PM*5, CMM*1 and Fan*4.)

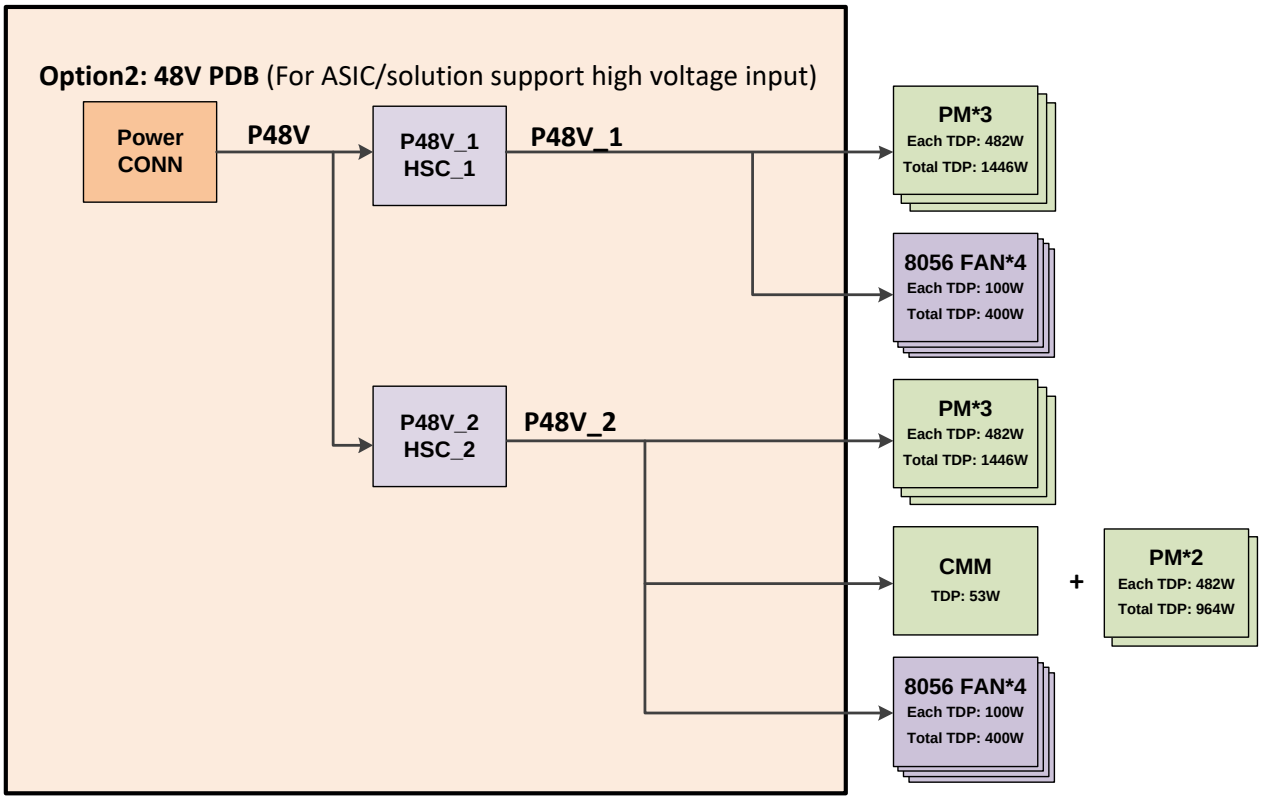


Figure 44 48V PDB. (For ASIC/solution support high voltage input)

10.1.9.3. Guide Pin for fool-proof Design

In order to support both 12V and 48V applications on CMM / PM, use the guide pin displacement for fool-proof design, prevent inappropriate module insert into the chassis.

10.1.9.3.1. 12V PDB CMM And 48V PDB CMM Guide Pin Difference

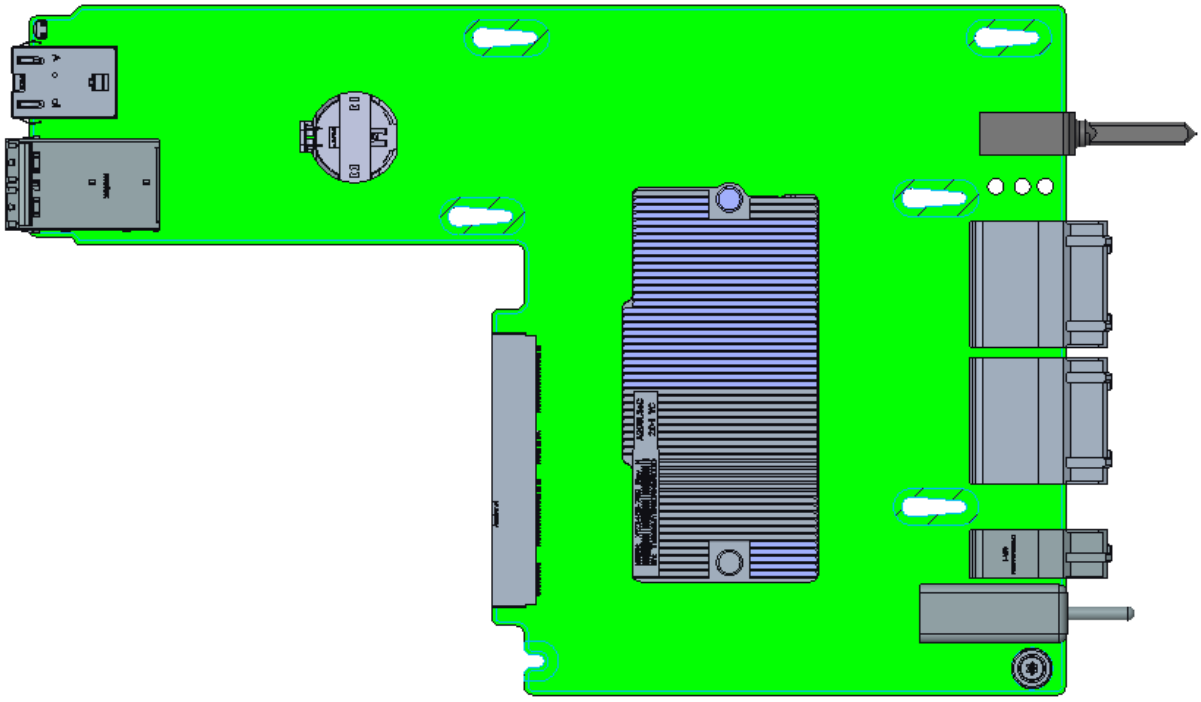


Figure 45 12V PDB CMM Guide Pin Location

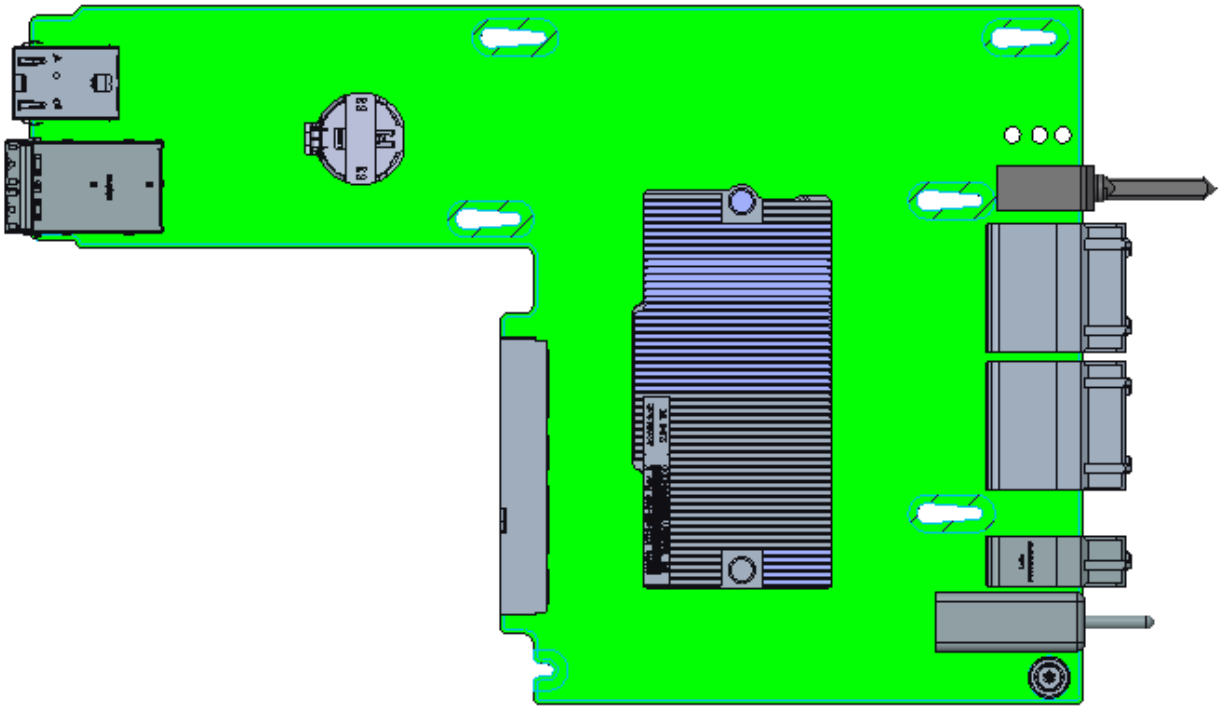


Figure 46 48V PDB CMM Guide Pin Location

10.1.9.3.2. 12V PDB PM And 48V PDB PM Guide Pin Difference

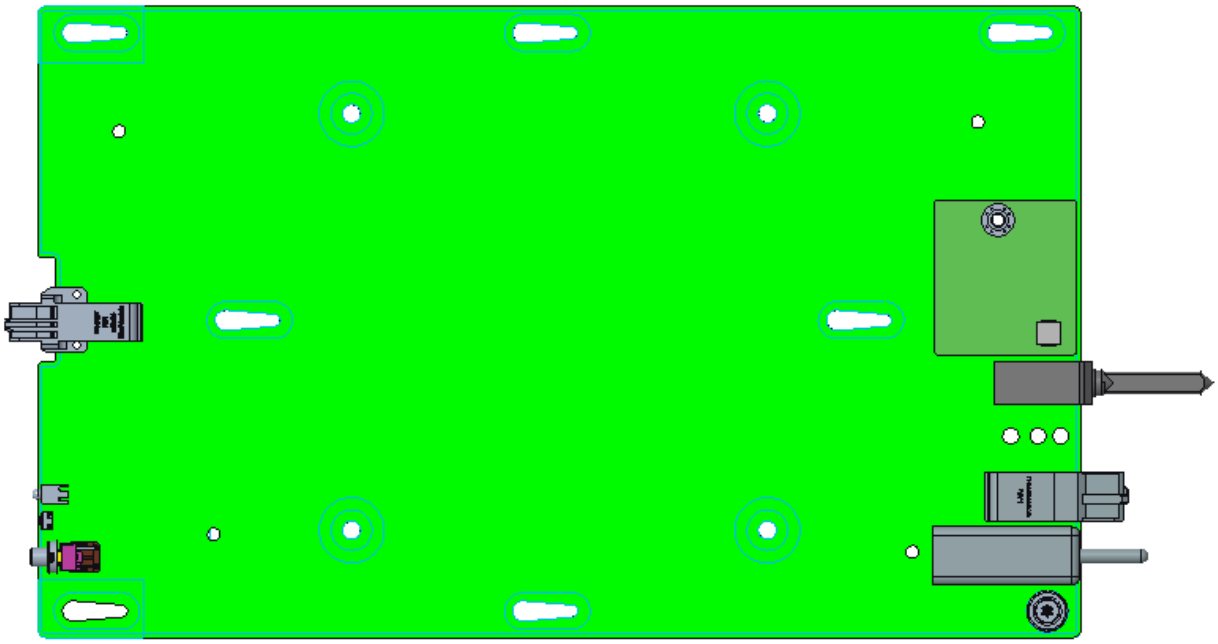


Figure 47 12V PDB PM Guide Pin Location

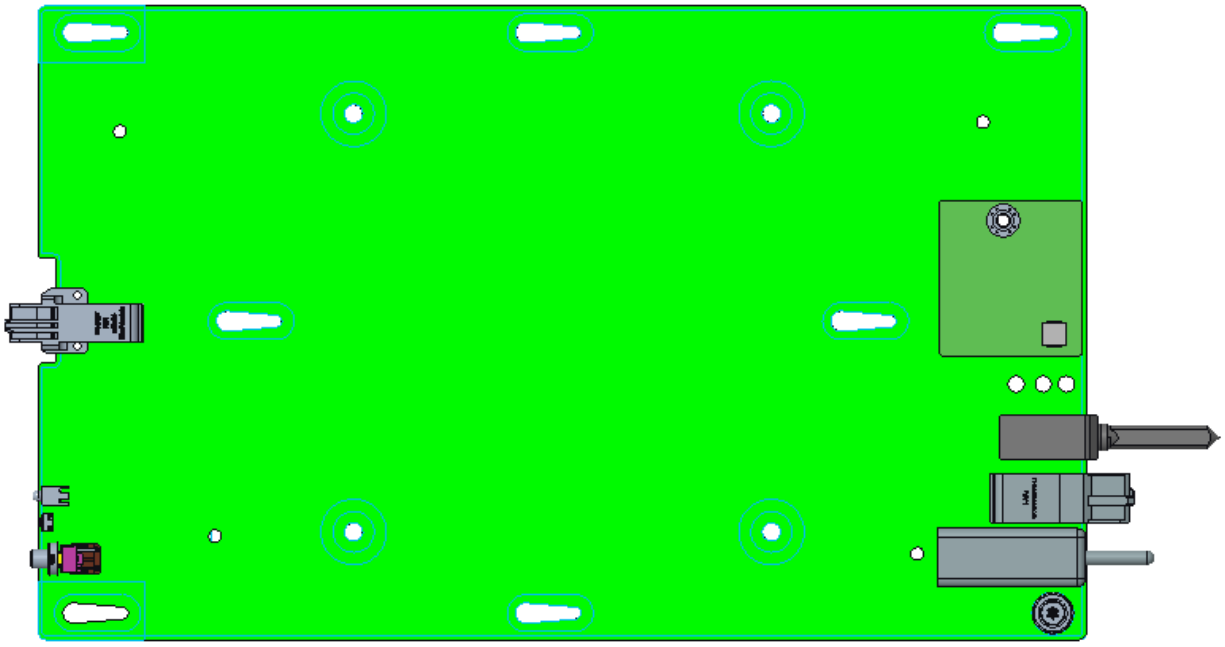


Figure 48 48V PDB PM Guide Pin Location

10.2. Fan Board

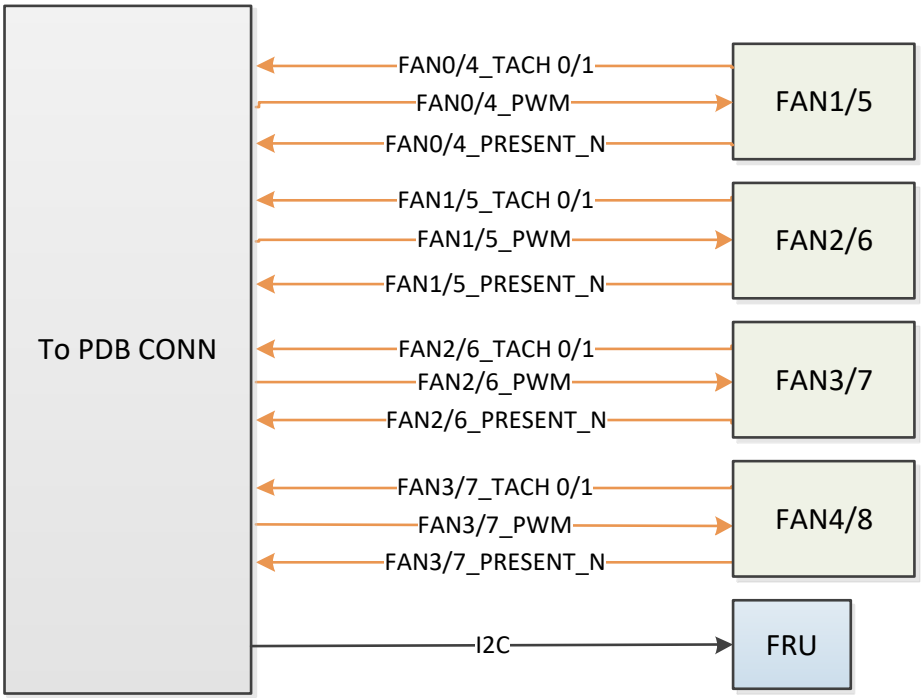


Figure 49 Fan Board Block Diagram

10.2.1. Fan Board I2C Bus Components

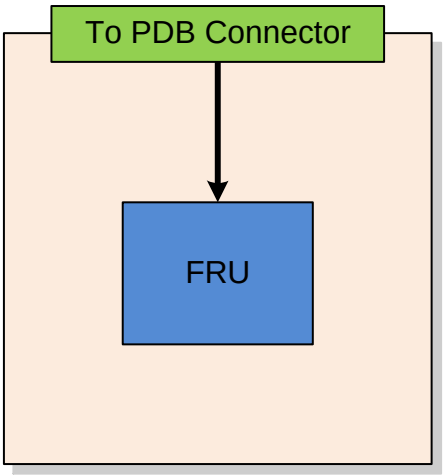


Figure 50 Fan Board I2C Block Diagram

10.2.1.1. FRU ID EEPROM (MRP 24AA1026T-I)

The MRP 24AA1026T-I/SN or equivalent is a 1024Kb serial EEPROM accessed over I2C from DC-SCM. It is used for tracking manufacturing information in the field. Contents of the FRUID EEPROM are defined in the Shasta FRUID Specification.

10.2.2. Fan Board To PDB Connector Pin List

Fan board to PDB Connector detailed in Table 29 and 30. Refer to “Shasta pin list_20220913”.

Pin	Signal name	I/O	Description
1	FAN0_TACH0	Input	Fan Tachometer
2	FAN2_TACH0	Input	Fan Tachometer
3	FAN0_TACH1	Input	Fan Tachometer
4	FAN2_TACH1	Input	Fan Tachometer
5	FAN0_PWM	Output	Fan PWM
6	FAN2_PWM	Output	Fan PWM
7	FAN0_PRESENT	Input	Fan Present
8	FAN2_PRESENT	Input	Fan Present
9	FAN1_TACH0	Input	Fan Tachometer
10	FAN3_TACH0	Input	Fan Tachometer
11	FAN1_TACH1	Input	Fan Tachometer
12	FAN3_TACH1	Input	Fan Tachometer
13	FAN1_PWM	Output	Fan PWM
14	FAN3_PWM	Output	Fan PWM
15	FAN1_PRESENT	Input	Fan Present
16	FAN3_PRESENT	Input	Fan Present
17	I2C_FAN_TOP_SCL	Output	I2C clock for fan board FRU
18	GND	NA	Ground
19	I2C_FAN_TOP_SDA	I/O	I2C data for fan board FRU
20	GND	NA	Ground

Table 29 Fan Board To PDB Signals Connector Pin List

Pin	Signal name	I/O
1	GND	NA
2	GND	NA
3	GND	NA
4	GND	NA
5	GND	NA
6	GND	NA

7	GND	NA
8	GND	NA
9	GND	NA
10	GND	NA
11	GND	NA
12	GND	NA
13	P48V_FAN	Output
14	P48V_FAN	Output
15	P48V_FAN	Output
16	P48V_FAN	Output
17	P48V_FAN	Output
18	P48V_FAN	Output
19	P48V_FAN	Output
20	P48V_FAN	Output
21	P48V_FAN	Output
22	P48V_FAN	Output
23	P48V_FAN	Output
24	P3V3_STBY	Output

Table 30 Fan Board To PDB Power Connector Pin List

10.2.3. Fan Board Stack-up

Table 31 shows the 4-layer fan board PCB stack-up. The stack-up uses material IT-170GRA1 or equivalent. The PCB thickness is 109.8 mils for reference.

STACKUP									
						Target Z (ohms) - MicroStrip		50	Breakout
						Target Z (ohms) - StripLine		50	
						Z tolerance		±10%	
						Z Type		Single	Single
Layer#	**Material**	**Description**	**Copper Weight (oz)**	**Thickness (mil)**	**Tolerance (mil)**	**Glass Fabric**	**Er**	**Width**	**Width**
		Soldermask		0.60			3.8		
1		TOP	0.5+plating	1.95				6.2	4
	IT-170GRA1	PP		3.70	±0.709	2113x1	3.66		
2		GND	2 (RTF)	2.60					
	IT-170GRA1	CORE		92.10	±7.09	Vendor Define	3.97		
3		GND1	2 (RTF)	2.60					
	IT-170GRA1	PP		3.70	±0.709	2113x1	3.66		
4		BOTTOM	0.5+plating	1.95				6.2	4
		Soldermask		0.60			3.8		
			Total	**109.80**	**±10%**				

Table 31 Fan Board Stack-up

10.2.4. Fan Board PCB Placement Strategy

Layout views of the fan board showing major component locations are shown in Figure 51.

Figure 51 Fan Board Layout Placement (TOP View)

11. Mechanical

11.1. Chassis

System Dimension (W x L x H): 521mm X 800mm X 188mm (4OU)

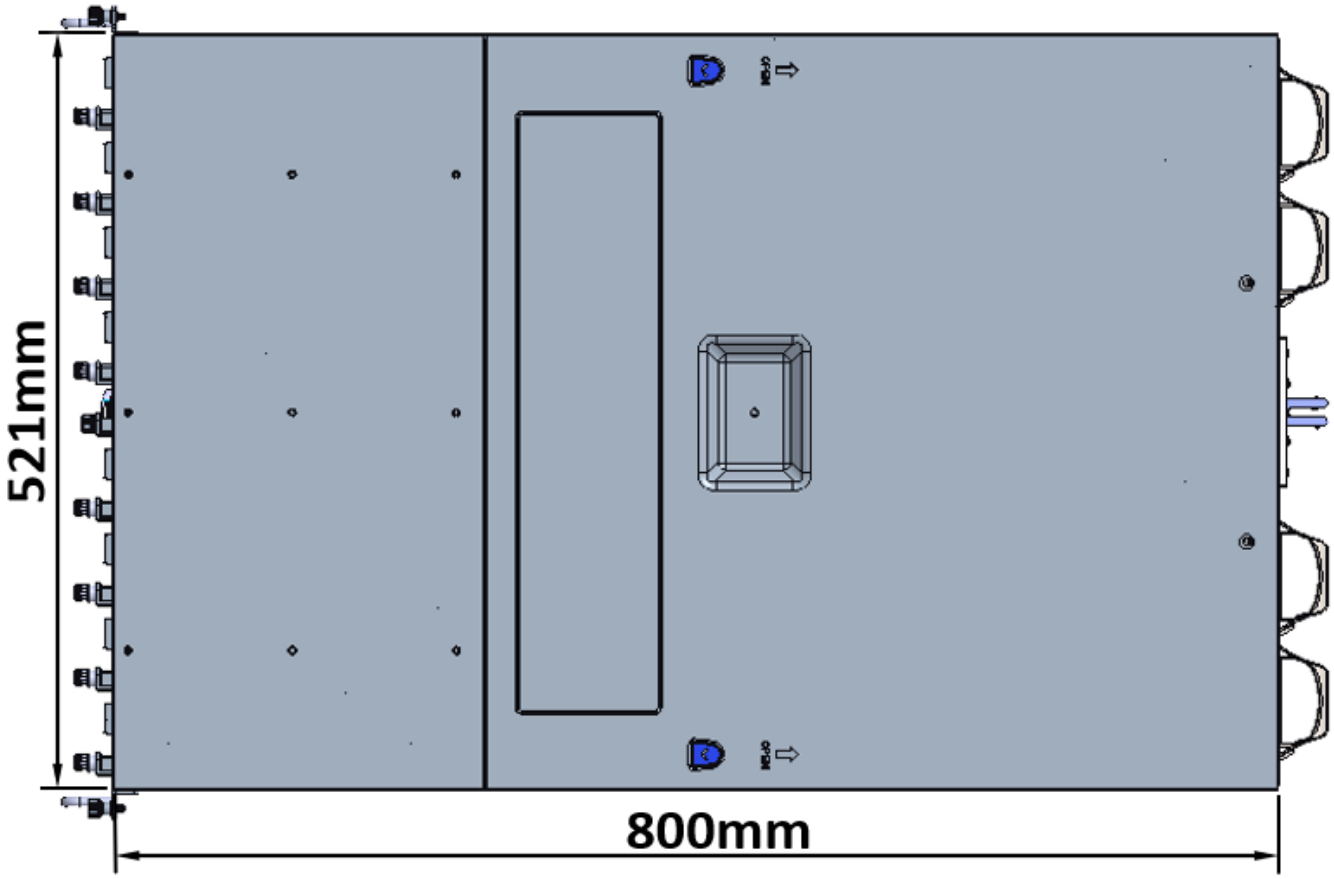


Figure 52 Chassis Top View

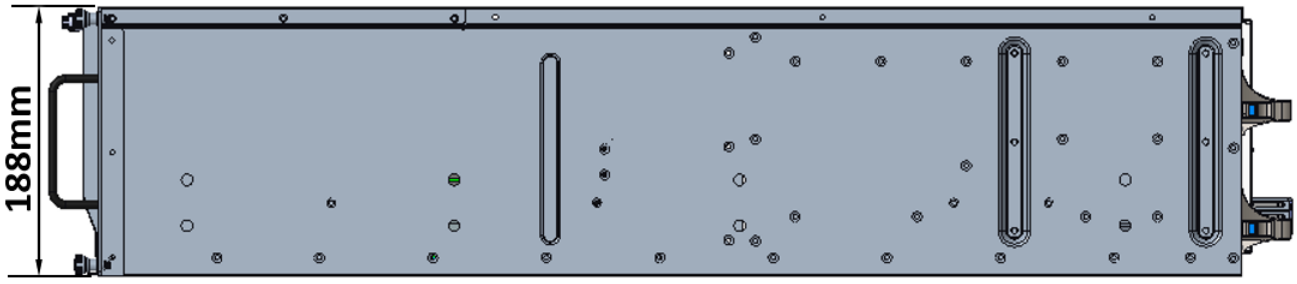


Figure 53 Chassis Side View

11.1.1. Chassis Front View

①Process Module (x8)

②Chassis Management Module

③Luggage Tag

④DC-SCM

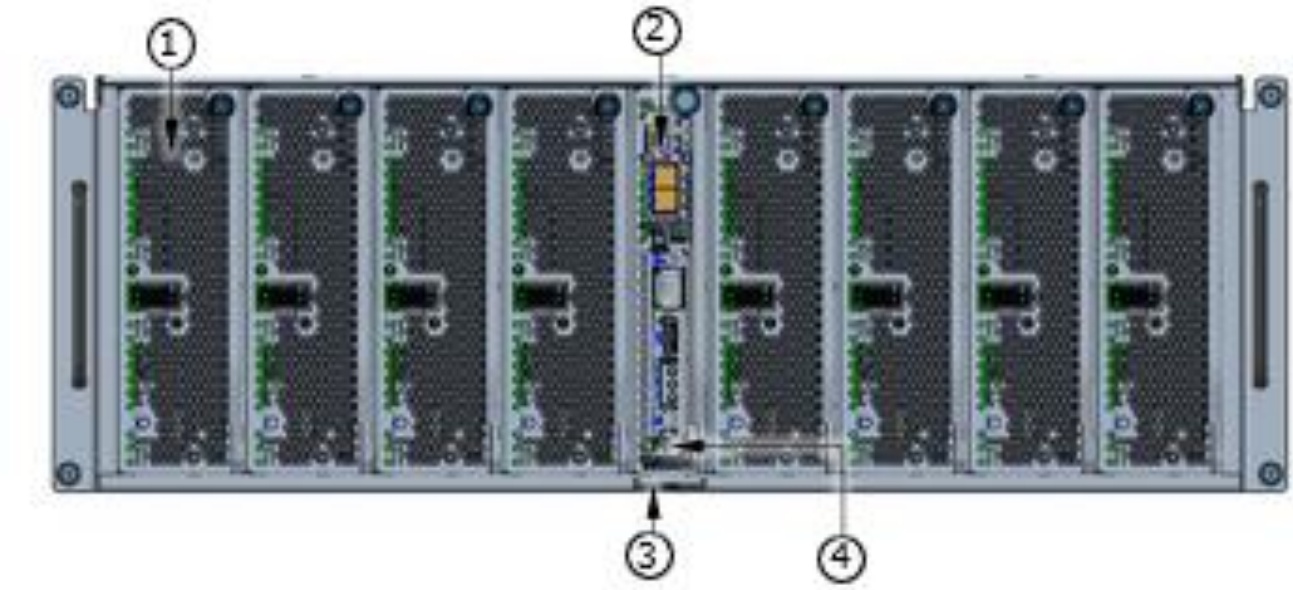


Figure 54 Chassis Front View

11.1.2. Chassis Rear View

⑤Rear Access Fan Module (x8)

⑥Bus Bar Power Connector

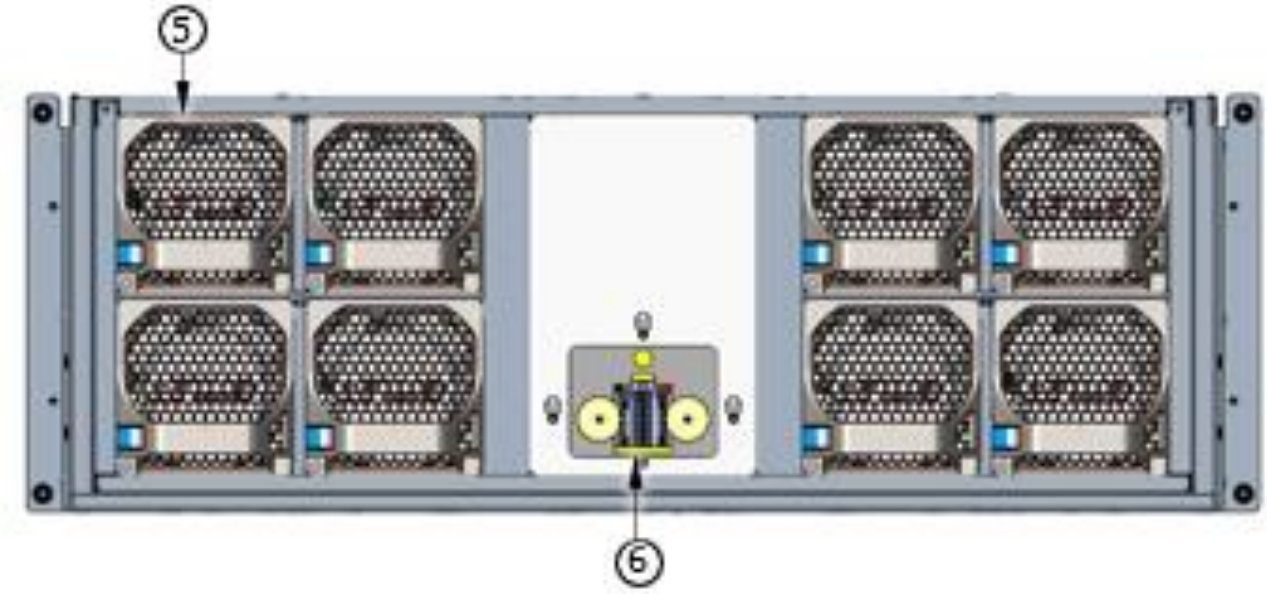


Figure 55 Chassis Rear View

11.1.3. Chassis ISO View

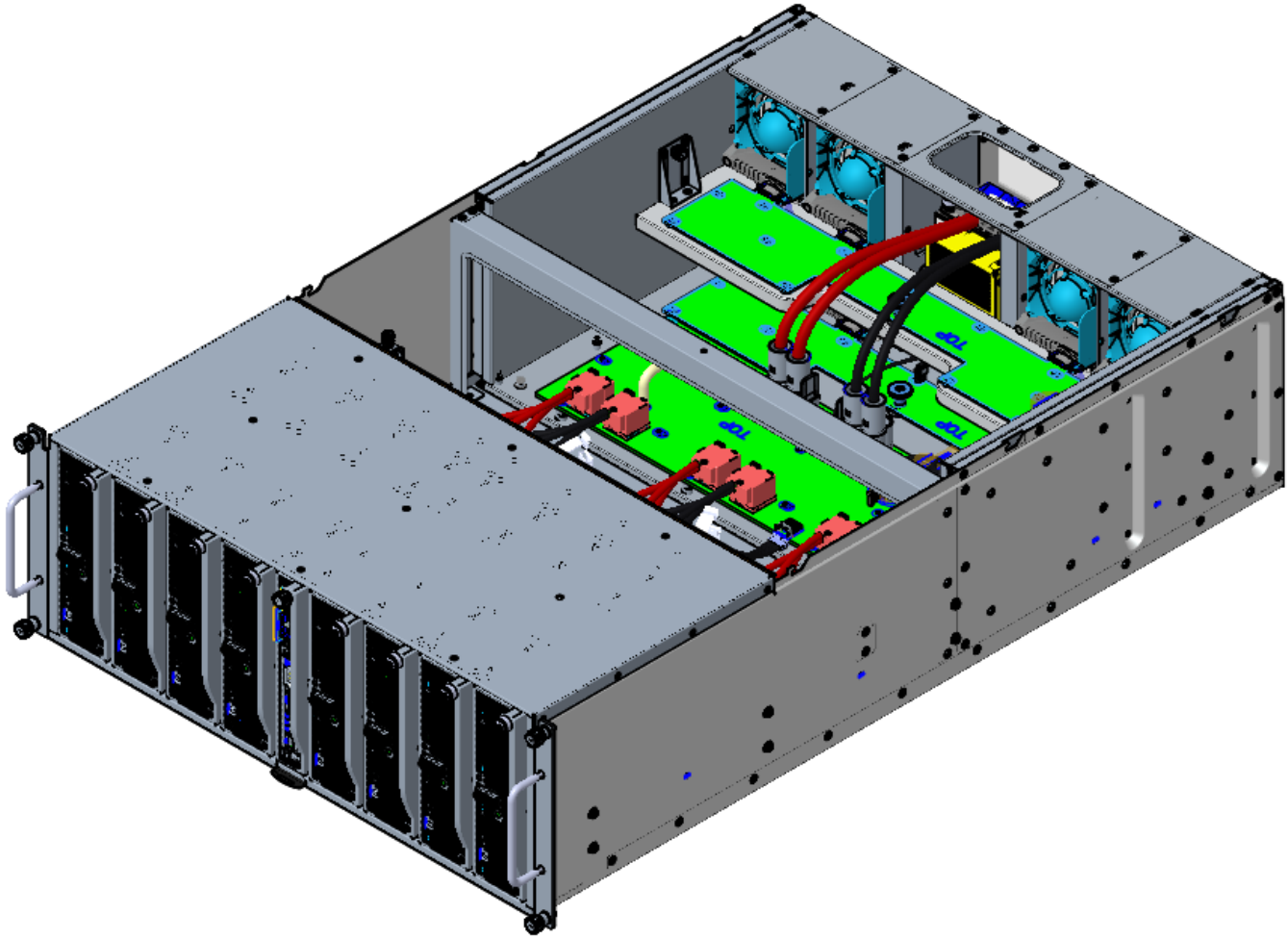


Figure 56 Chassis ISO View

11.1.4. Chassis Top View

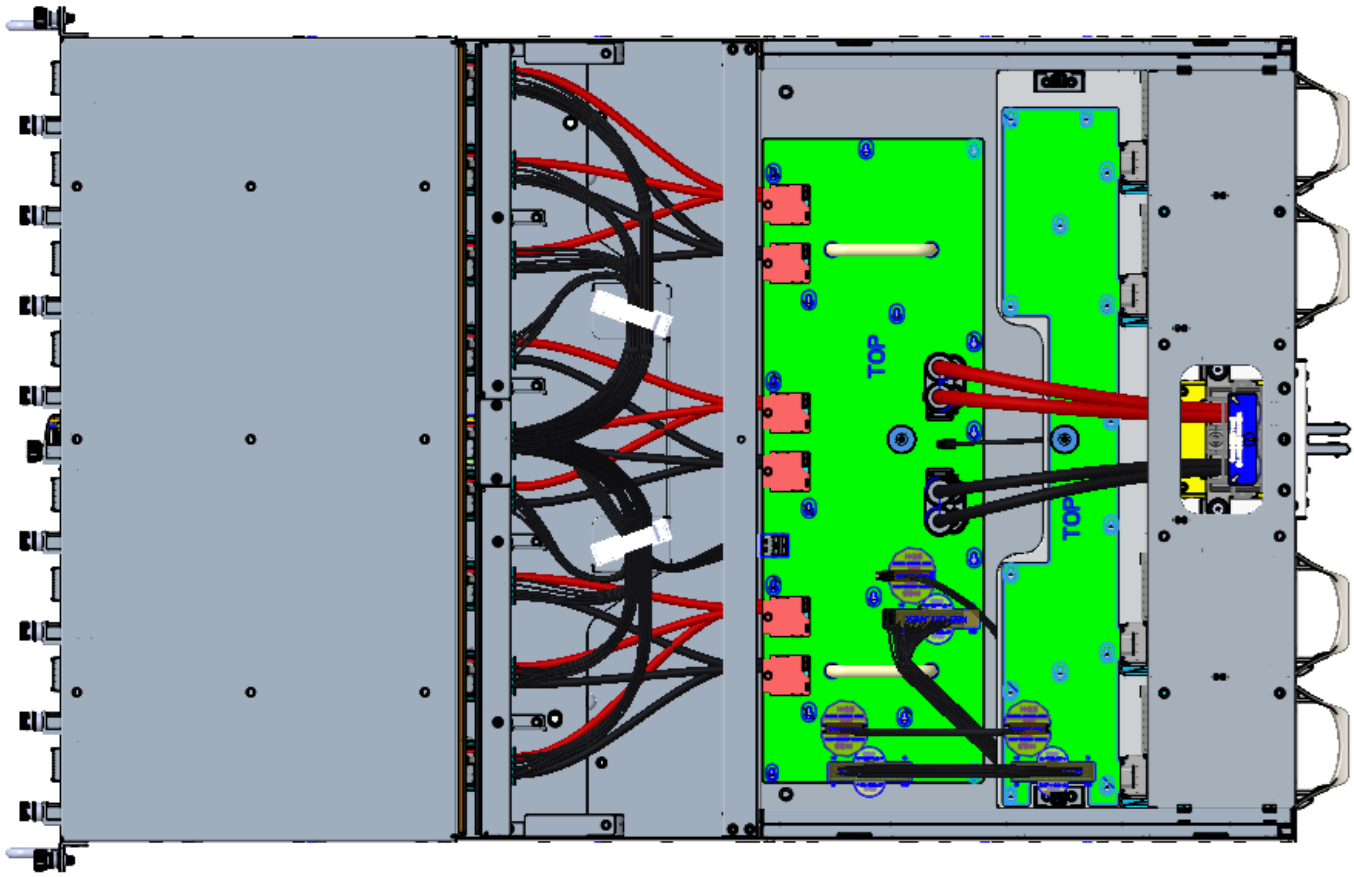


Figure 57 Chassis Top View

11.1.5. Included Components Distributions

①Process Module (x8)
②Chassis Management Module (x1)
③Hybrid Cable Tray
④PDB Board
⑤Busbar Clip cable Cage
⑥Fan Control Board
⑦Upper Fan Board Support Bracket
⑧Fan module (x8)

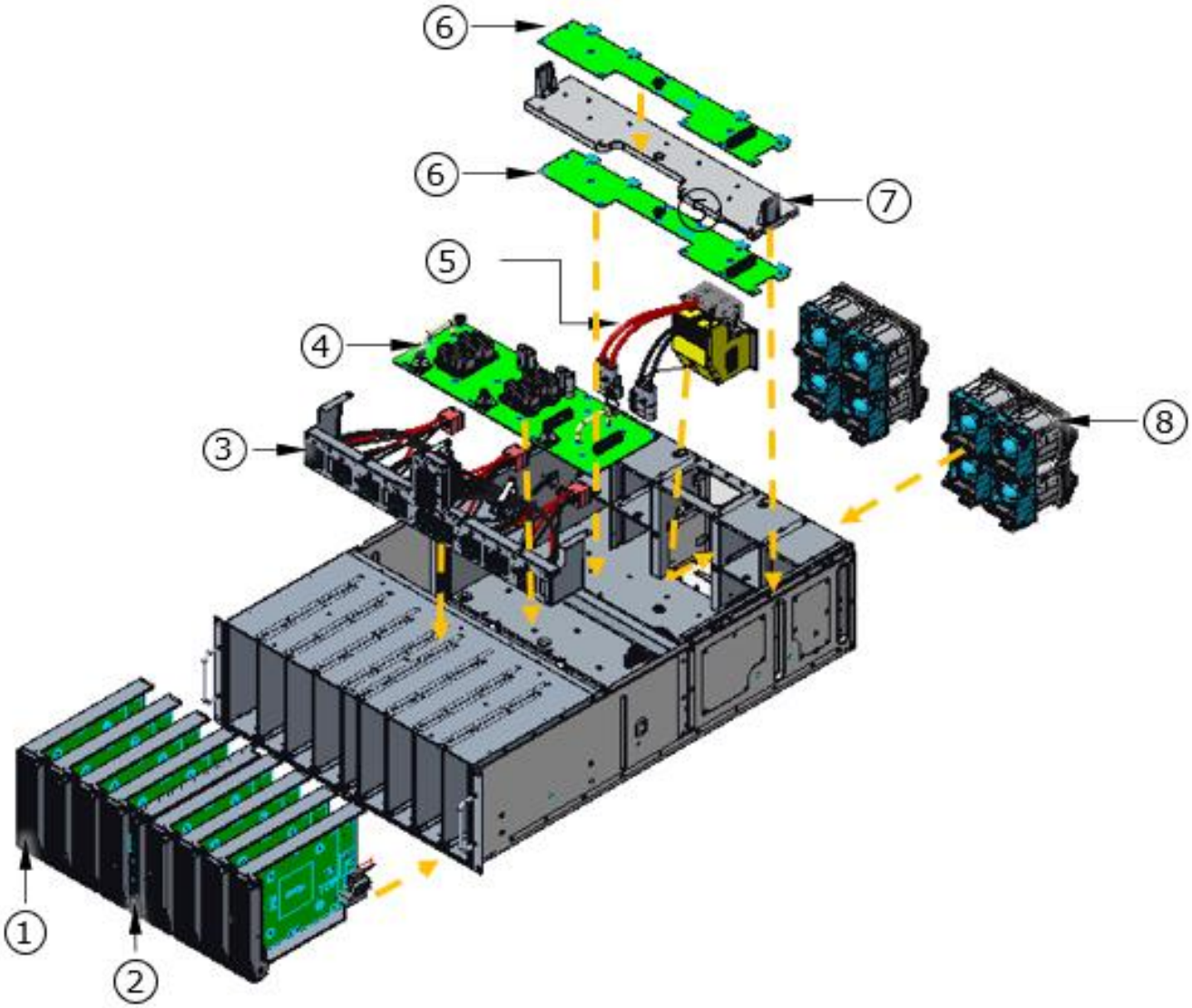


Figure 58 Included Components Distributions

11.2. Chassis Management Module (CMM) Overview

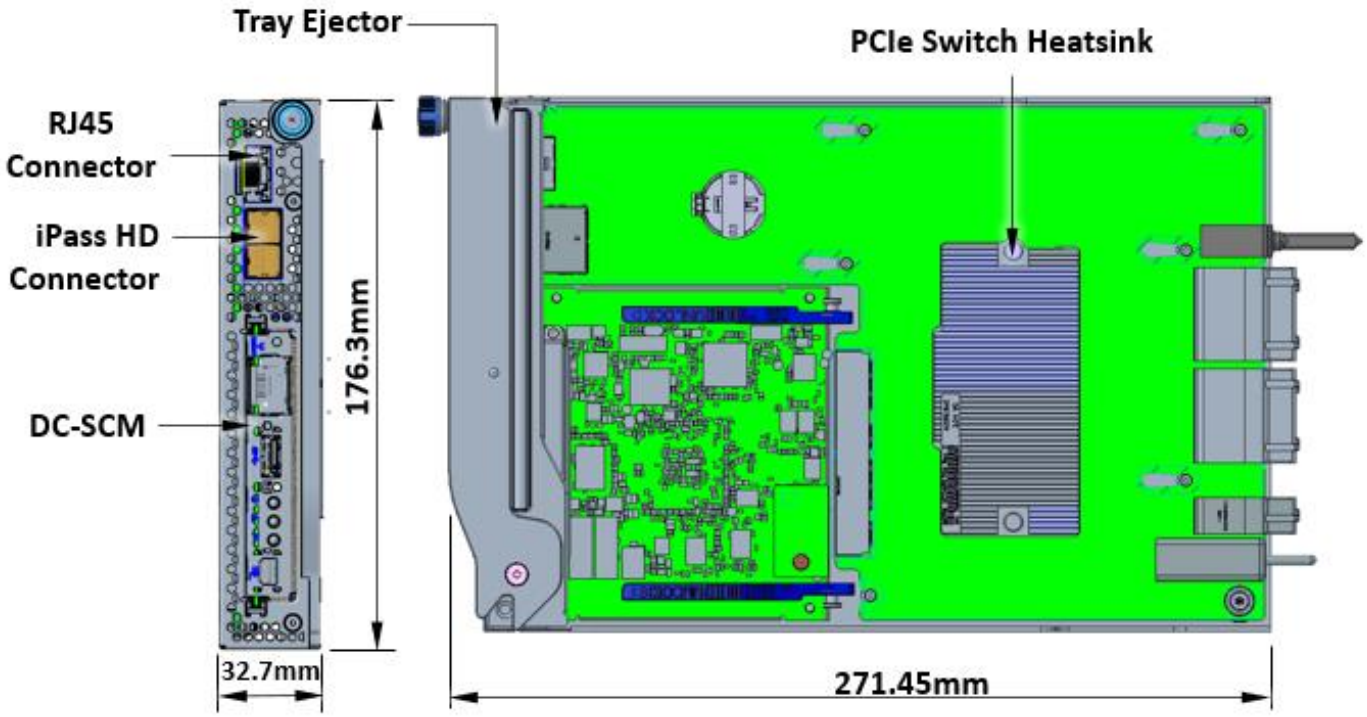


Figure 59 CMM Overview

11.3. Process Module (PM) Overview

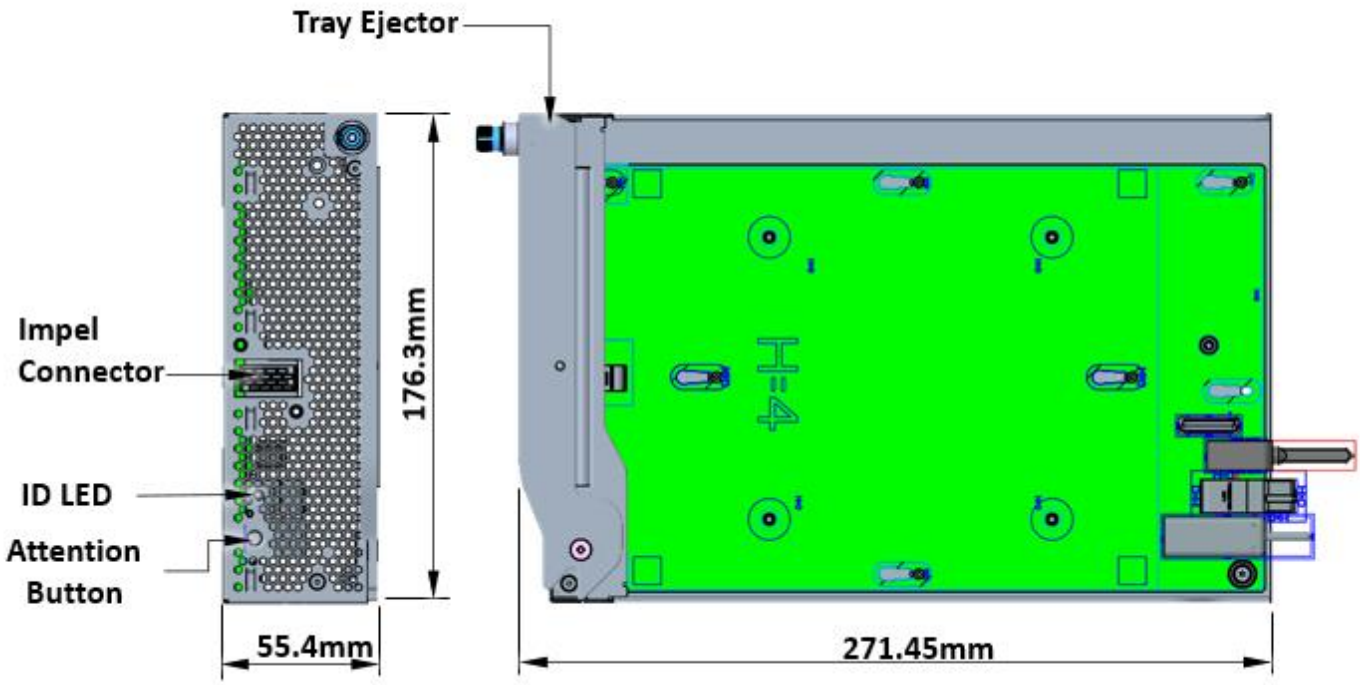


Figure 60 PM Overview

11.4. Serviceability

11.4.1. Chassis Management Module (CMM) Serviceability

①Release the thumb screw

②Open the ejector to cam-out the Chassis Management Module

③Complete the Chassis Management Module removing

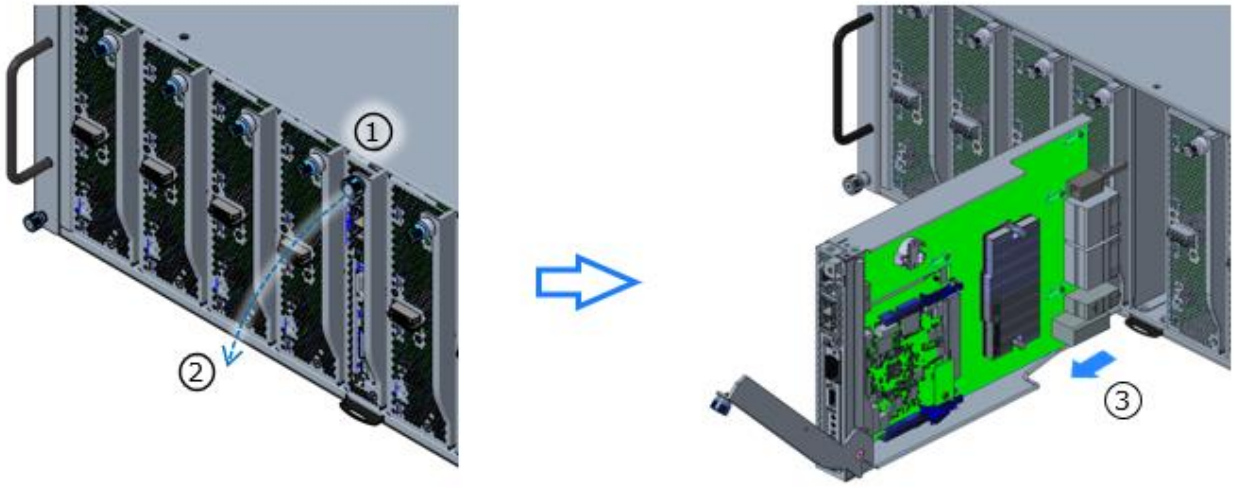


Figure 61 Chassis Management Module (CMM) Serviceability

11.4.2. Process Module (PM) Serviceability

①Release the thumb screw
②Open the ejector to cam-out the Process Module
③Complete the Process Module removing

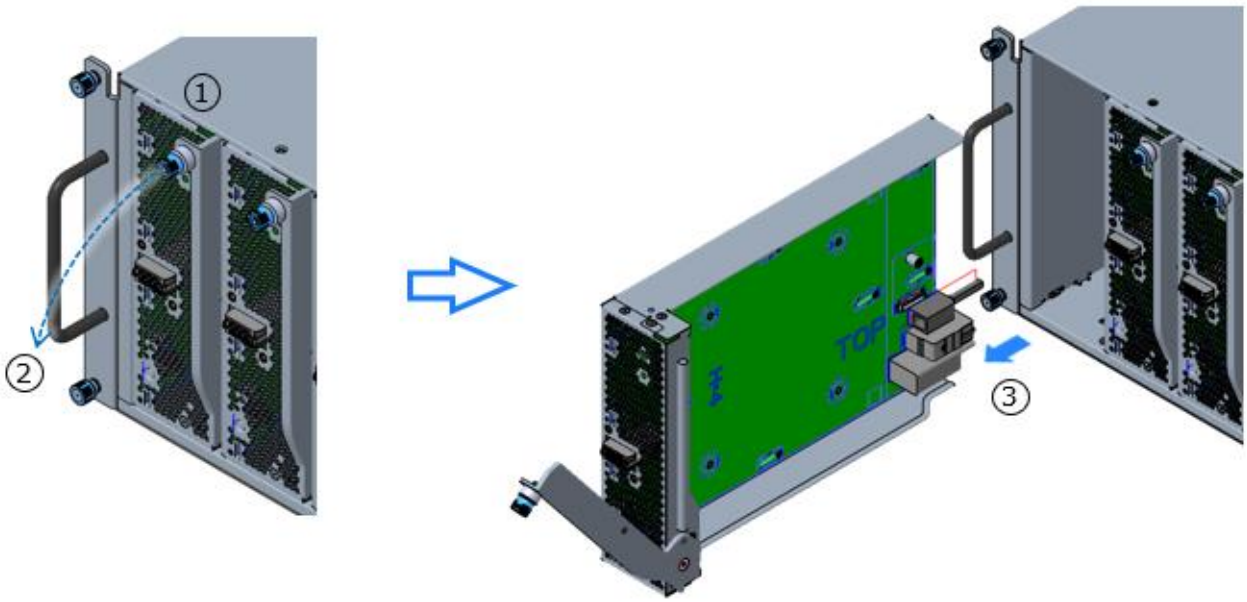


Figure 62 Process Module Serviceability

11.5. Cable Management Overview

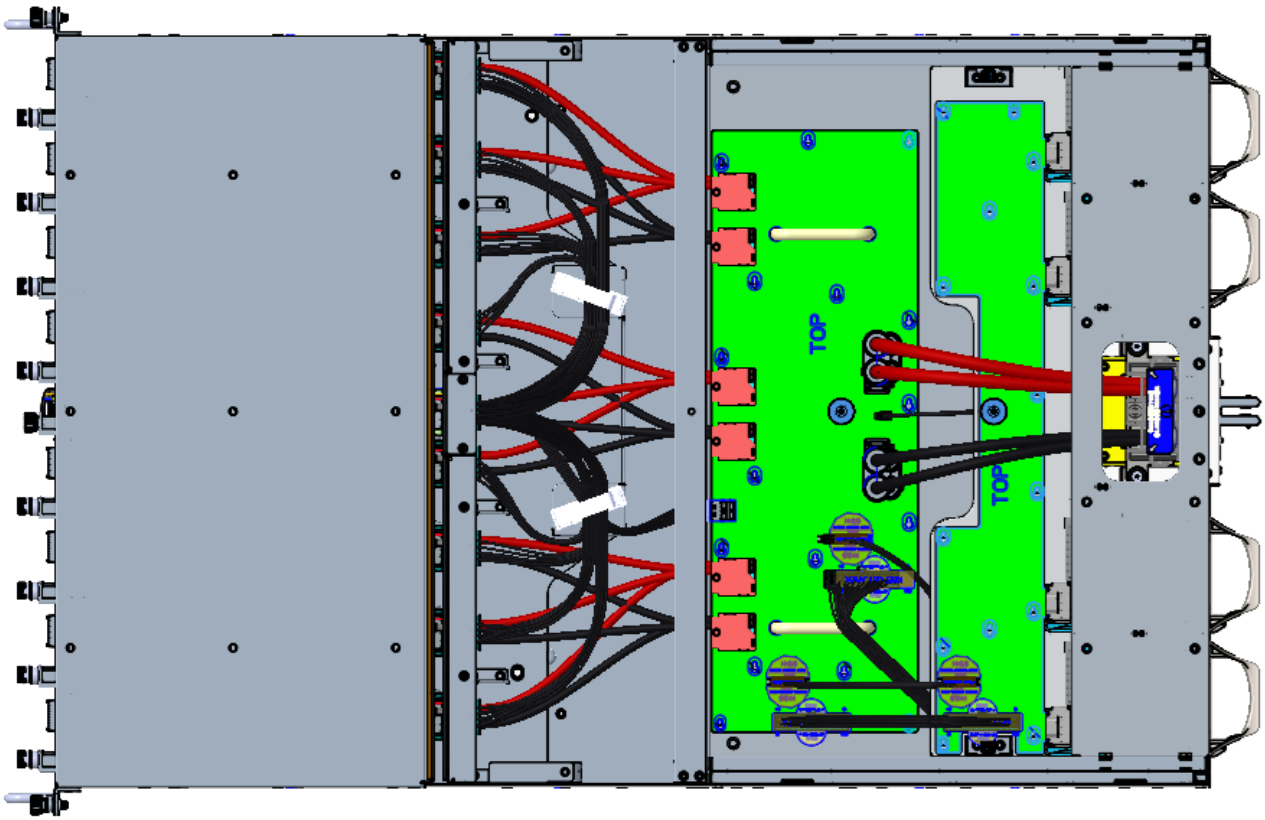


Figure 63 Cable Management Overview

11.5.1. Hybrid cable

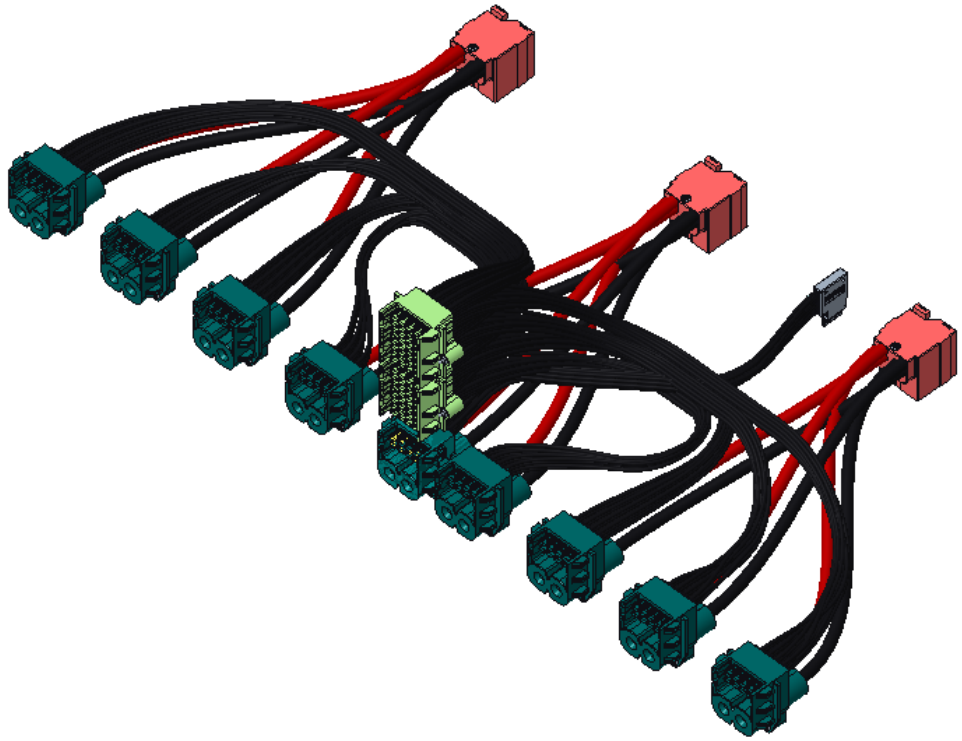


Figure 64 Hybrid Cable

11.5.2. Fan sideband cable

Figure 65 Fan Sideband Cable

11.5.3. Fan power cable

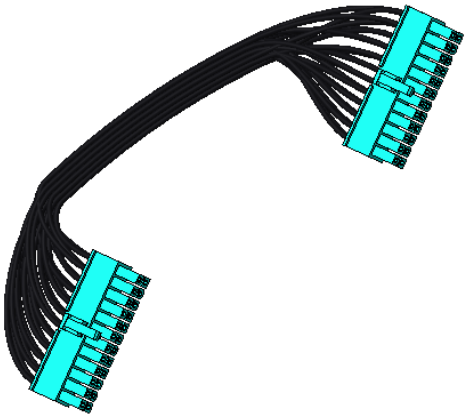


Figure 66 Fan Power Cable

11.5.4. Combined snapshot of busbar clip cable to busbar cable to PDB

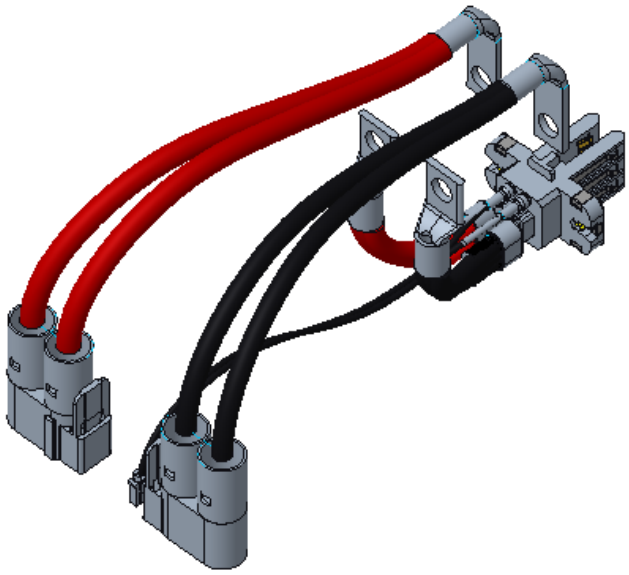


Figure 67 Combined snapshot of busbar clip cable to busbar cable to PDB

11.5.4.1. Busbar clip cable

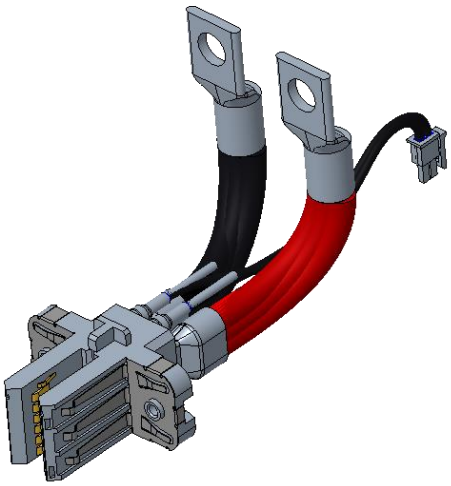


Figure 68 BusBar Clip Cable

11.5.4.2. Busbar cable to PDB

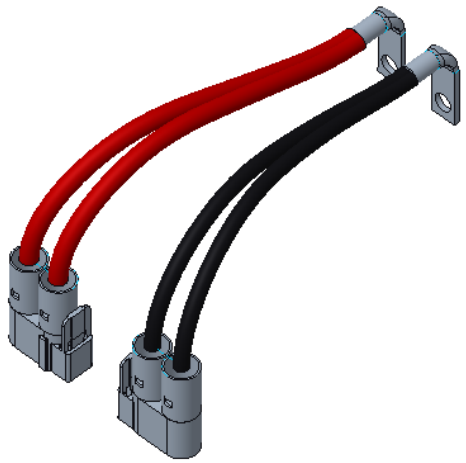


Figure 69 Busbar Cable to PDB

12. Onboard Power System

The CMM/PM accepts a conditioned 12V from the PDB. The CMM/PM shall derive all required voltages from the 12V source provided by the Molex power connector. The power connector shall be Molex MPN 2208634200 or equivalent. The power connector receives power from the PDB through the cables. The CMM/PM power budget by major components is summarized in Table 32 below.

Board	Component/subsystem	Max power
CMM	DC-SCM	~28W
CMM	PCIe Switch	~35W
PM	Chip	TBD
PM	Cerberus	~1W

Table 32 CMM/PM Power Budget

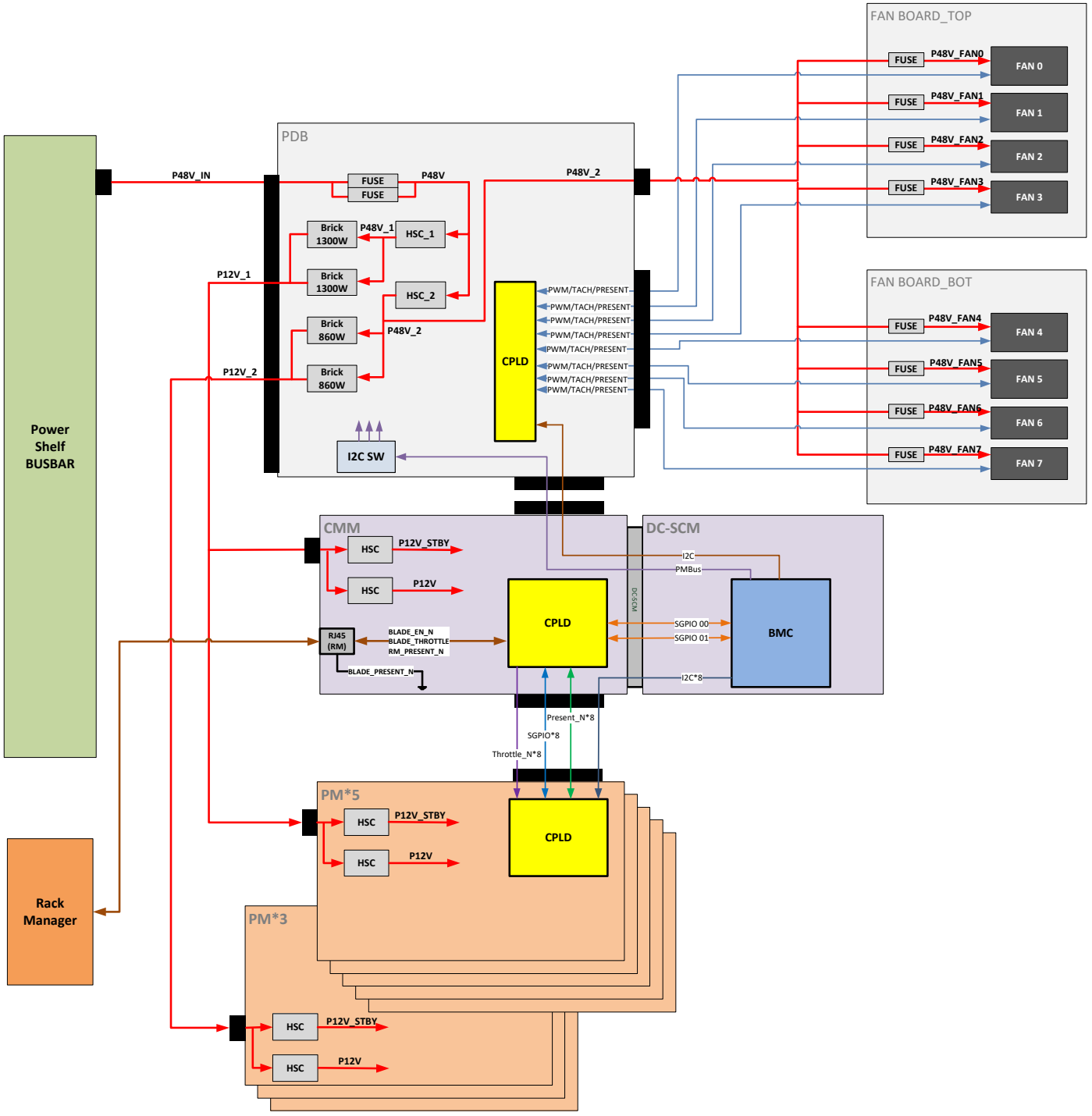


Figure 70 Shasta Power Block Diagram

12.1. Power Control & Sequencing

The power-up sequencing of all chip voltage must meet the recommended operating conditions specified in the chip product literature. The voltage sequence must be controlled on both power up and power down.
The power-up sequencing of all PCIe switch voltage sources must meet the recommended operating conditions specified in the PCIe switch product literature. The voltage sequence must be controlled on both power up and power down.

TBD

Figure 71 Shasta Power Sequencing

12.2. Power Monitoring

Monitoring of total CMM/PM power consumption is available from the Hot swap controller via its I2C connection to the BMC.

12.3. Power Throttling

Power throttling helps to cover the contingency that the total power consumption of the system exceeds the application specific rating of the power delivery system from the server through the internal power connector, along with the potential of overheating, several sources of information are routed to DC-SCM for monitoring.

12.4. Inrush Current

The PDB shall provide Hotswap to limit the turn-on inrush current on any initial current surge or spike that will not exceed **HOTSWAP MOSFET SOA, NXP PSMN4R8-100BSE 60V/20A@1ms**.

13. Environmental Regulations/Environmental Requirements

The system is deployed in an environmentally controlled location. The inlet of the chassis will be exposed to the environment described in Table 33. The system must have the capability to provide full functional operation under the conditions given.

Specification		Requirement
Inlet temperature	Operating	• 50°F to 95°F (10°C to 35°C) • Maximum rate of change: 18°F (10°C)/hour • Allowable derating guideline of 1.6°F/1000ft (0.9°C/304m) above 3000 ft.
	Non-operating	• -40°F to 140°F (-40°C to 60°C) • Rate of change less than 36°F (20°C)/hour

Table 33 Environmental Requirement

The system is required to use chassis fans to cool the electrical components. Eight 80mm fans may be used to cool the components. Each fan module will have 2 rotors in it. The maximum airflow allowed in a chassis must not exceed 158 CFM/kW. The system must also operate at its maximum power configuration without performance degradation with 2 fan rotors failed. Variable fan speed capability allows the rack to minimize energy consumption of the air movers and facilities in conditions that permit it. The fan speed is based on component temperature requirements within the system.

14. Hardware Management

14.1. Clocks distribution

The Shasta board design includes multiple clock sources summarized in Table 34, and shown in Figure 72.

Usage	CMM		PM	
Device	Clock MUX (9ZML1245AKILFT)		Clock Buffer (LMK00334)	
AC coupling for Device	TBD		TBD	
Termination for Device	TBD		TBD	
Source	CMM Local Clock GEN (SI52202-A01BGMR)	Head-Node Clock Signal	PM Local Clock GEN (SI52202-A01BGMR)	CMM Clock Signal
AC coupling for Source	TBD	TBD	TBD	TBD
Termination for Source	TBD	TBD	TBD	TBD

Frequency	100MHz	100MHz	100MHz	100MHz
I/O Type	HCSL	LVDS	LVDS	LVDS
ppm spec.	0	TBD	0	0
Jitter spec.	0.38ps (RMS)	TBD	0.38ps (RMS)	0.062ps (RMS)

Table 34 Clock Sources

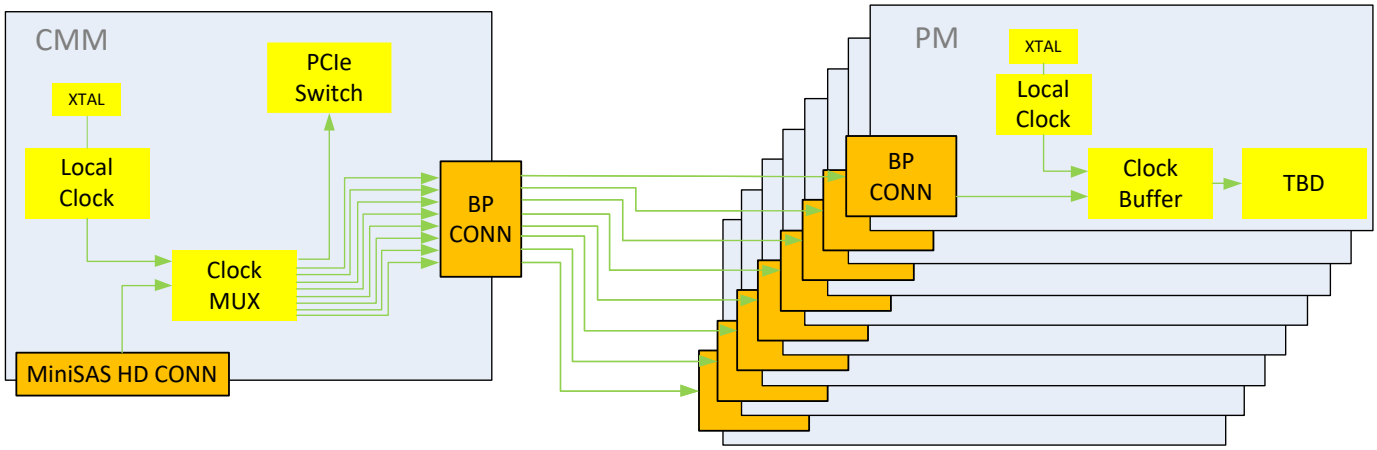


Figure 72 Shasta Clock Block Diagram

14.2. I2C Interfaces and Devices

The Shasta provides a set of resources to the DC-SCM's BMC via I2C. The I2C topology and addresses (7-bit) of Shasta are shown in Figure 73.

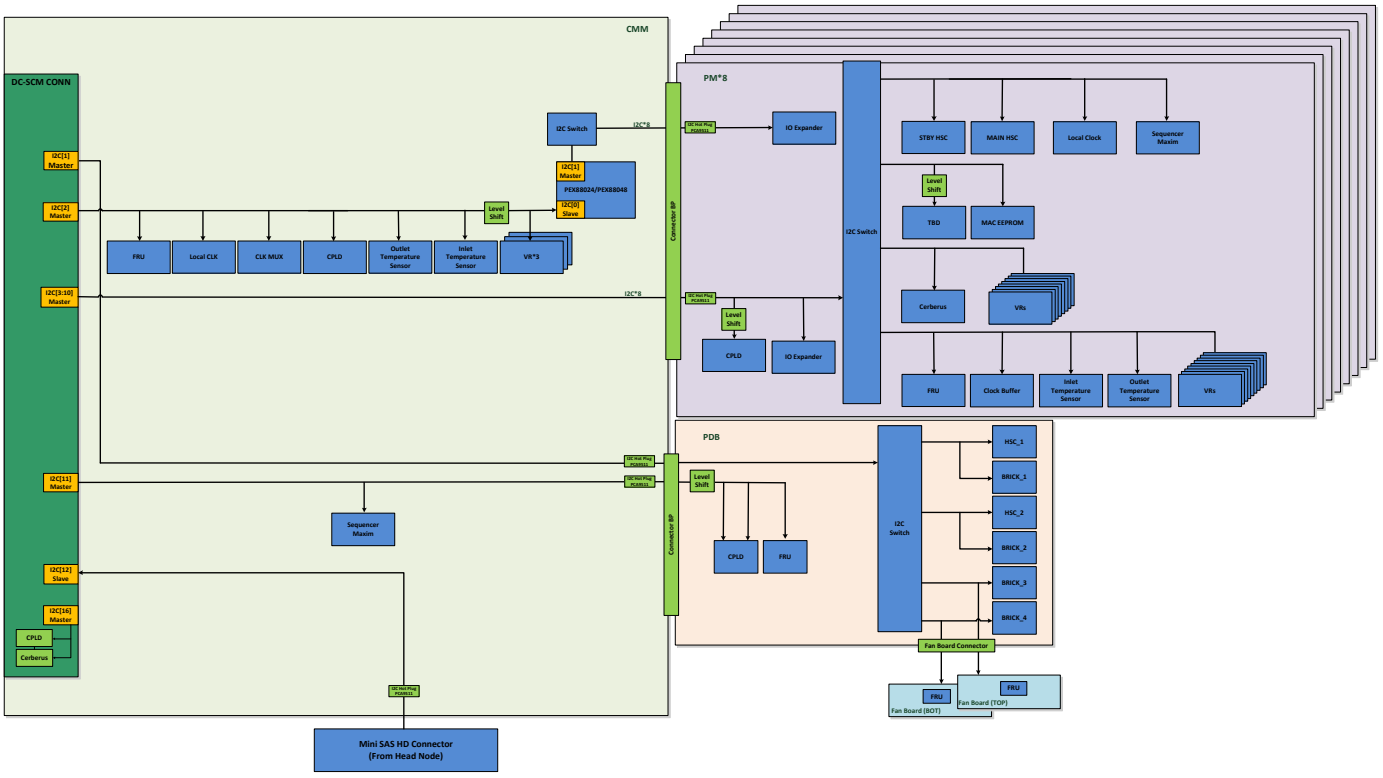


Figure 73 Shasta I2C Block Diagram

A few things to note:

1. The CMM acts as a slave device when being accessed by the head node.
2. Each PM has a dedicated I2C bus [3:10]
3. The PCI Switch has an I2C Bus that talks to each PM Module through an I2C Switch

14.3. Reset

The Shasta reset block diagram is shown in Figure 74.

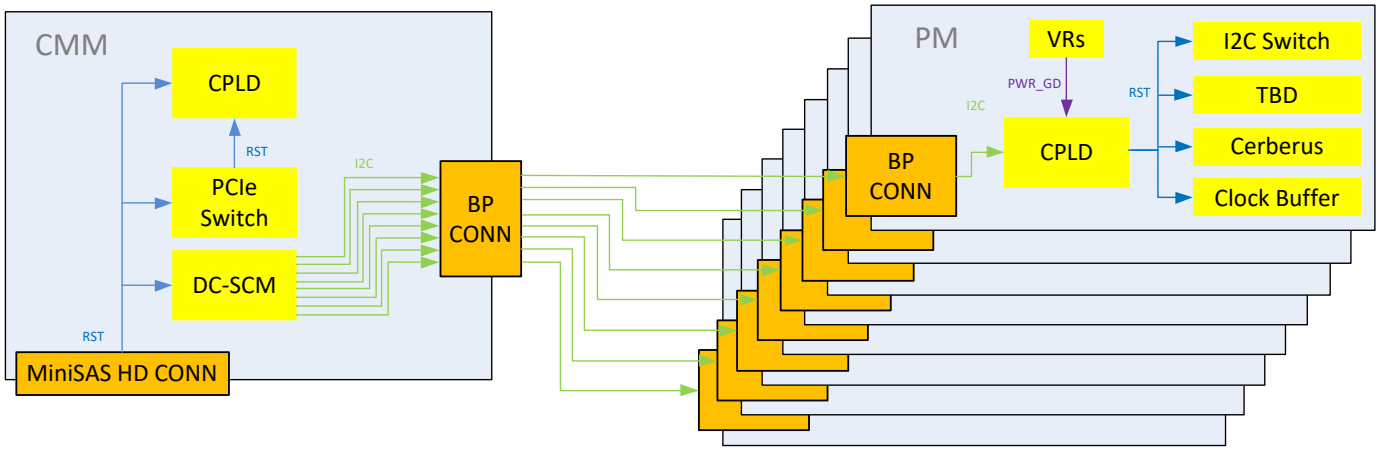


Figure 74 Reset Block Diagram

14.4. Hot Plug

CMM would detect the PM present as the hot plug notice. The related signals include PCIe, clock, I2C, PMBus, QSPI, SGPIO and other sideband signals.

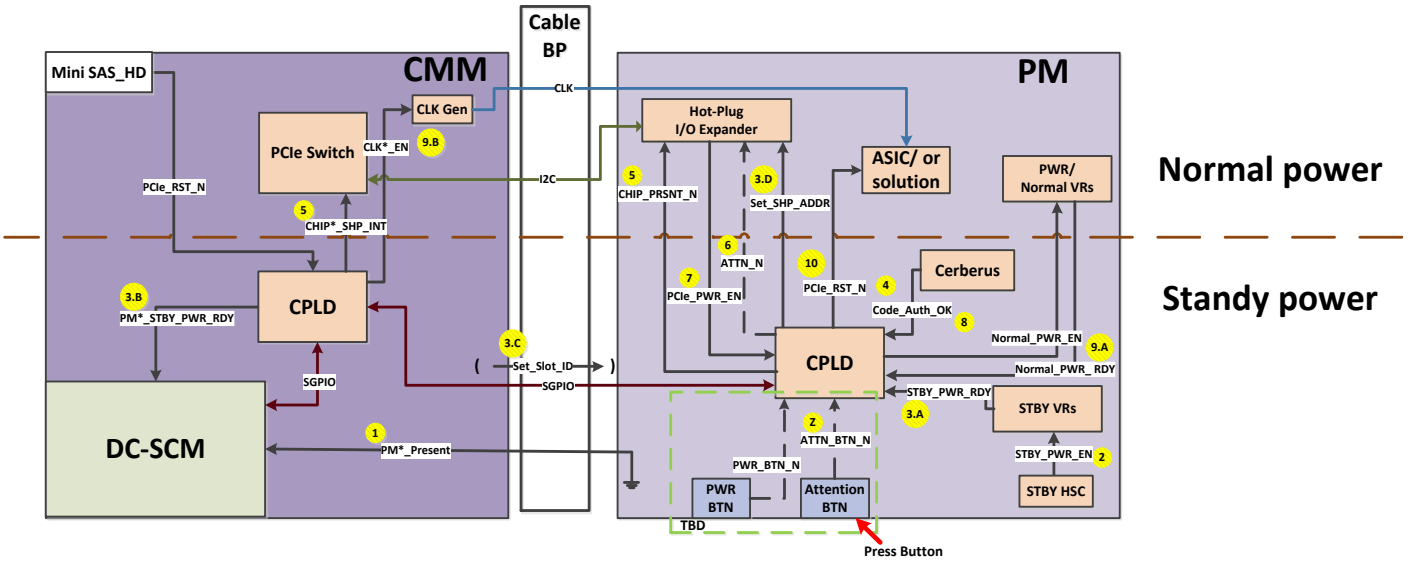


Figure 75 Hot Plug Block Diagram

14.5. SPI

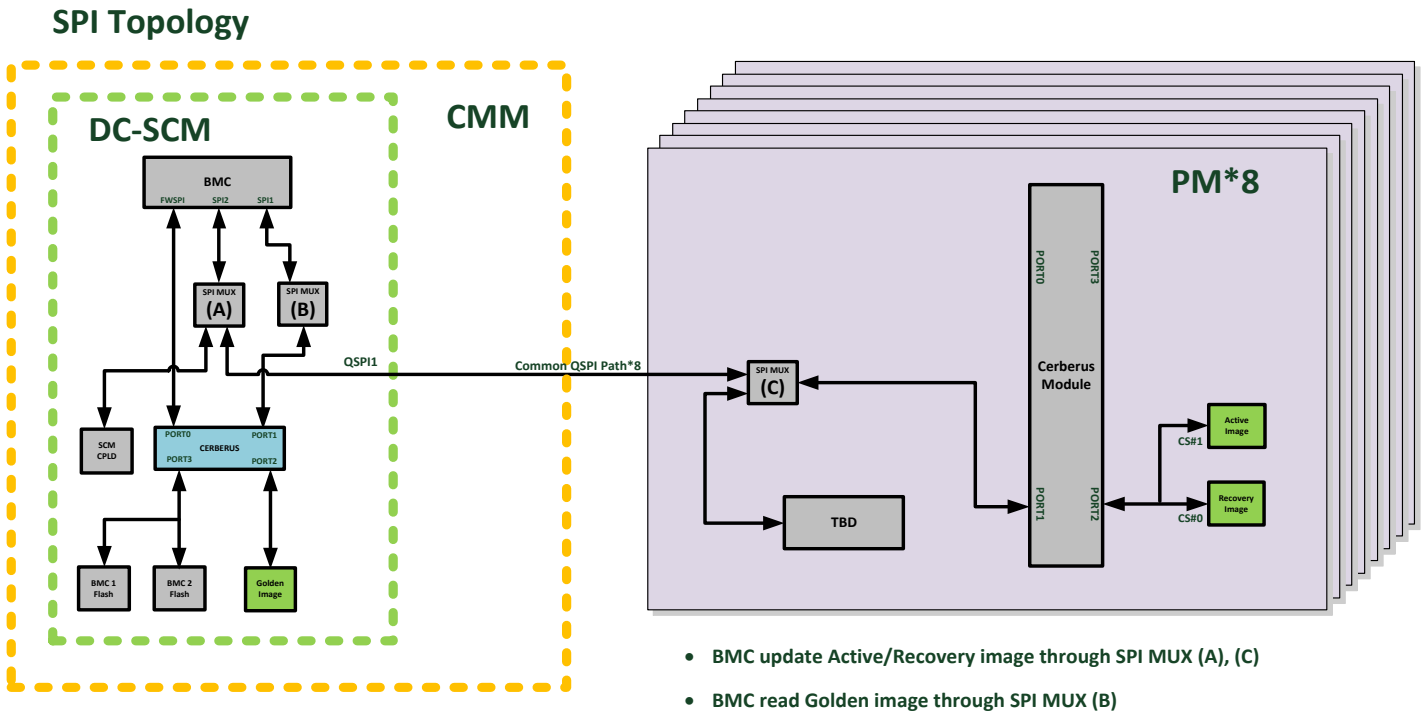


Figure 76 SPI Block Diagram (Fanout buffer for QSPI in the CMM not shown)

14.6. System FW Image flow

TBD

Figure 77 System FW Image flow

15. Security (only for Platform Boards and Systems)

Shasta Platform level security features are built around DC-SCM module we have in Shasta as chassis management sub-system. DC-SCM BMC images are attested by the Cerberus module in DC-SCM before letting BMC boot. PM modules could also have Cerberus module to attest the image in SPI flash before letting the devices load image.

16. References

OCP DC-SCM 1.0 Specification
OpenRack V3
Cerberus Security Module specification
An example PCIe re-timer card specification.

Appendix A - Checklist for IC approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes	If no, please state reason.
Was it approved in the OCP Contribution Portal?	Yes	If no, please state reason.
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	No	Quanta and Molex are the collaborators and potential Suppliers.
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	No	Potentially in 18 months. Microsoft has a product in planning which will be using Shasta as the chassis. Our estimate is it will take 18 months to get to production. Please have each Supplier fill out Appendix B.

Appendix B-__ <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist

(to be provided by each supplier seeking OCP recognition for a Hardware Product based on this specification)

Company:
Contact Info:

Product Name:
Product SKU#:
Link to Product Landing Page:

The following is needed for OCP hardware product recognition:

For OCP Inspired™

- All Suppliers must be a Silver, Gold or Platinum Member.
- Declare product is 100% compliant with specification
- Complete the OCP Inspired™ Product Recognition Checklist, which includes hardware management conformance checks and security profile.

For OCP Accepted™

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Complete the OCP Accepted™ Product Recognition Checklist, which includes hardware management conformance checks, security profile and open system firmware conformance checks.
- Submit a design package meeting OCP Hardware Design Guideline Contribution Checklist (if not already submitted by the contributor). If already submitted, declare the product is 100% compliant with the design package.
- Submit a firmware package including a firmware image, build scripts, documentation, test results and a tool that verifies modifications
- Submit the BMC source code, if applicable to product type

Please complete the OCP Inspired™ Product Recognition Submission Checklist or OCP Accepted™ Product Recognition Checklist and the following table.

Item	Details	Links
Which product recognition?	OCP Accepted™ or OCP Inspired™	Provide link for the appropriate Product Checklist
If OCP Accepted™, who provided the Design Package?		Link to OCP Contribution Database
Where can a potential adopter purchase the product?		Link to OCP Marketplace

Appendix C - Contribution Process FAQs

As a contributor to a hardware specification, here are some questions that often come up.

Q1. What type of hardware specification am I contributing to OCP? Is it any of the below?
- a. base specification for a de-facto standard (new standard with no hardware product on the horizon)
- b. base specification for an intended physical <hardware product type> (product may be coming but within the next 1-2 years)
- c. modification of an existing specification (state which existing spec is being modified)
  - i. either a complete revision update or
  - ii. a minor version update
- d. design spec (based on an existing base specification) with more refined design details (product coming in 12-15months)
- e. a detailed specification for a <hardware product type> for a very specific product being available in 3-6months of approval of this Spec
- f. If none of the above, please contact OCP Staff for better direction.

Q2. How do I know if what I am contributing will be accepted by OCP?
- a. Before contributing any specifications, please contact either OCP Staff (Archna Haylock or Michael Schill) or the Project Lead for the Project that best represents your contribution. For example, if you are contributing a Server Specification, please contact one of the Server Project Leads. You can see all the Projects here.
- b. They will help you with your contribution and help you navigate the process.

Q3. What is the contribution process for my hardware spec?
- a. Follow the flow for your spec type here.
- b. This flow is subject to change so please check with the OCP Staff for more information or any questions.

Q4.What if my spec is not developed yet and I want to collaborate with other companies?
- a. Please contact either OCP Staff (Archna Haylock or Michael Schill) or the Project Lead for the Project that best represents your contribution.
- b. They will help you find other collaborators and help you with the contribution process for a multi-party contribution.

Q5.I have a question on the Contribution License Agreement.
- a. Please contact OCP Staff and we can help you with questions.

Q6.Do I need to have a product in order to contribute a spec?
- a. Please see Q1. Some types of specs do not require an immediate product. Some do. Please work with the OCP Staff on better direction on your specification type.