Project Olympus

US1-EPYC

COVER PAGE

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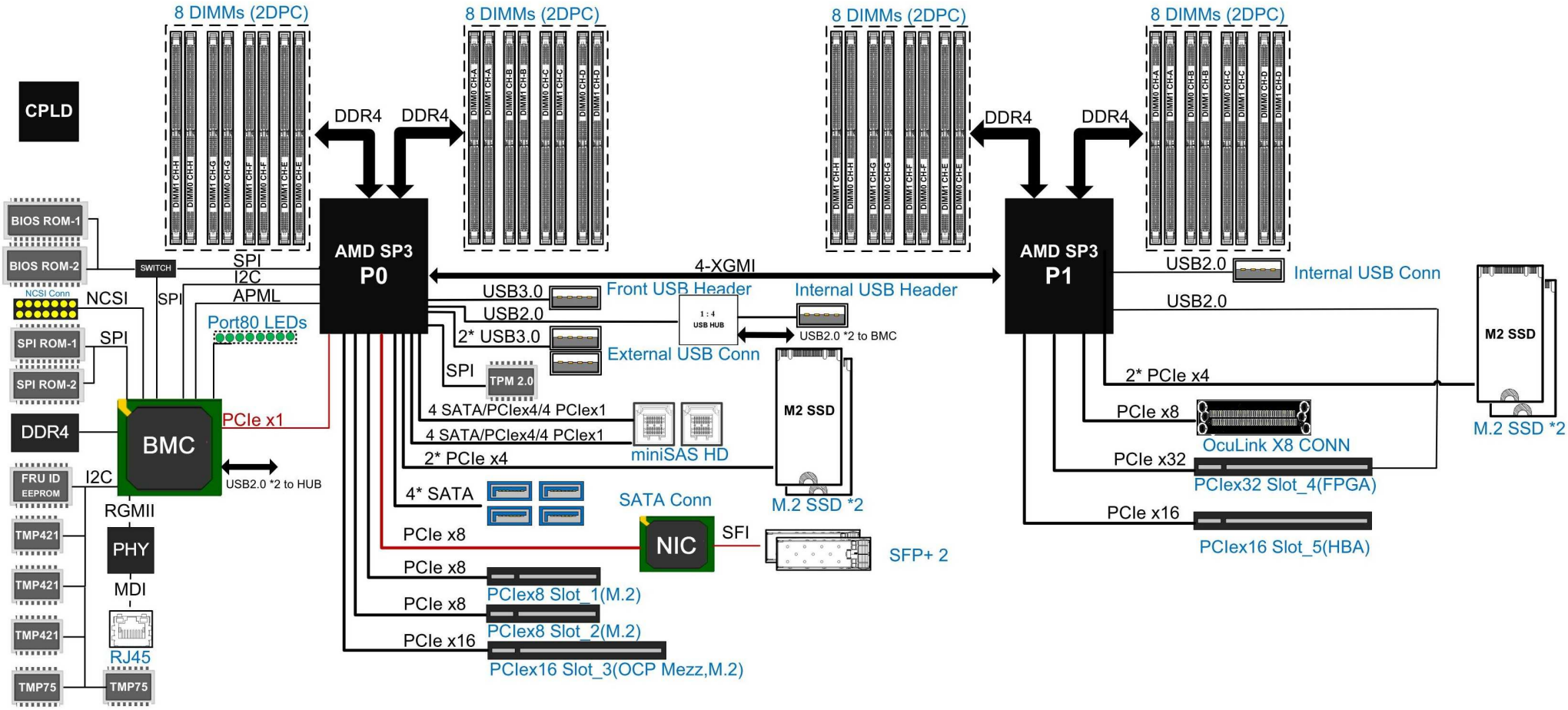
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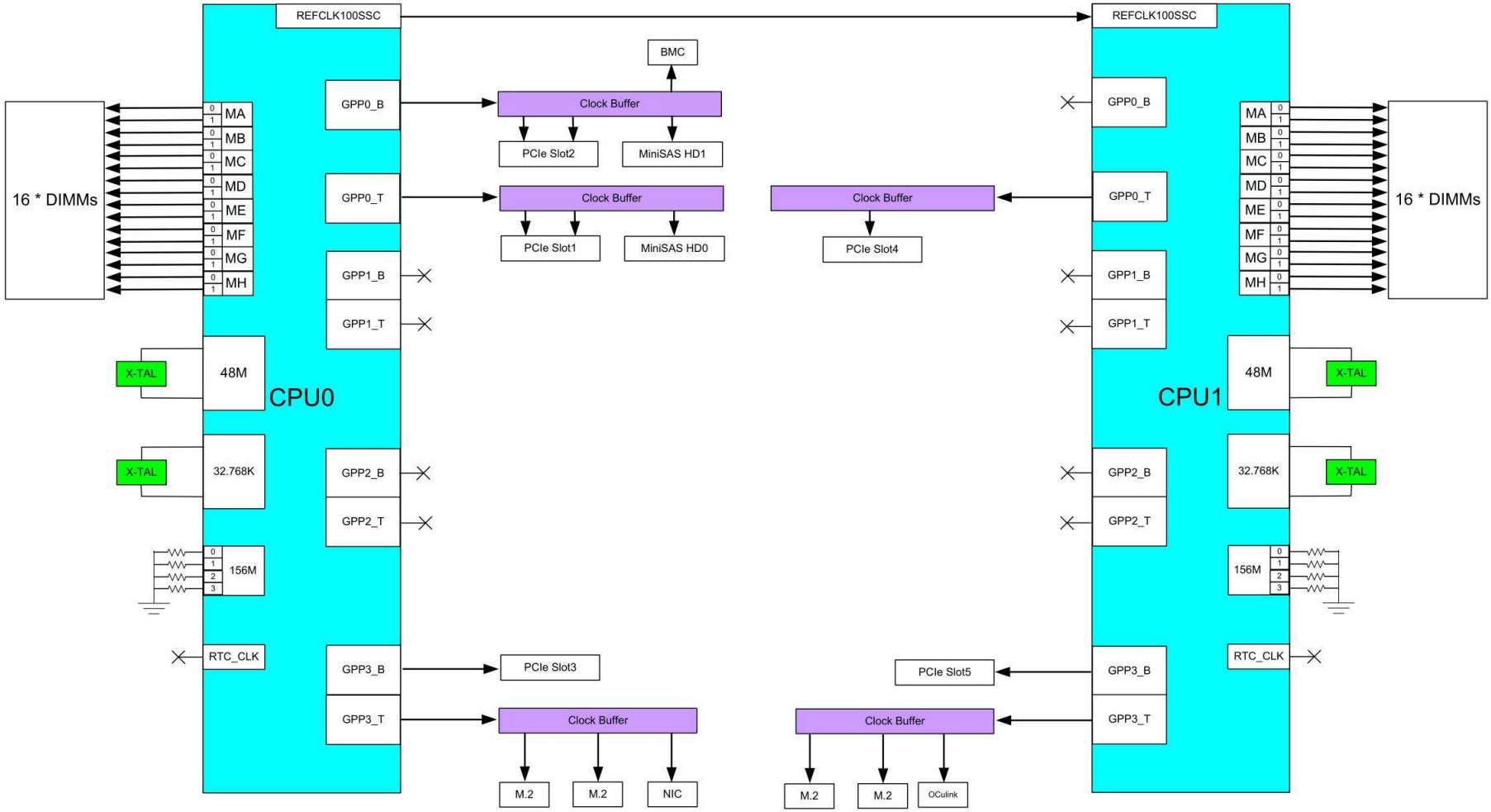
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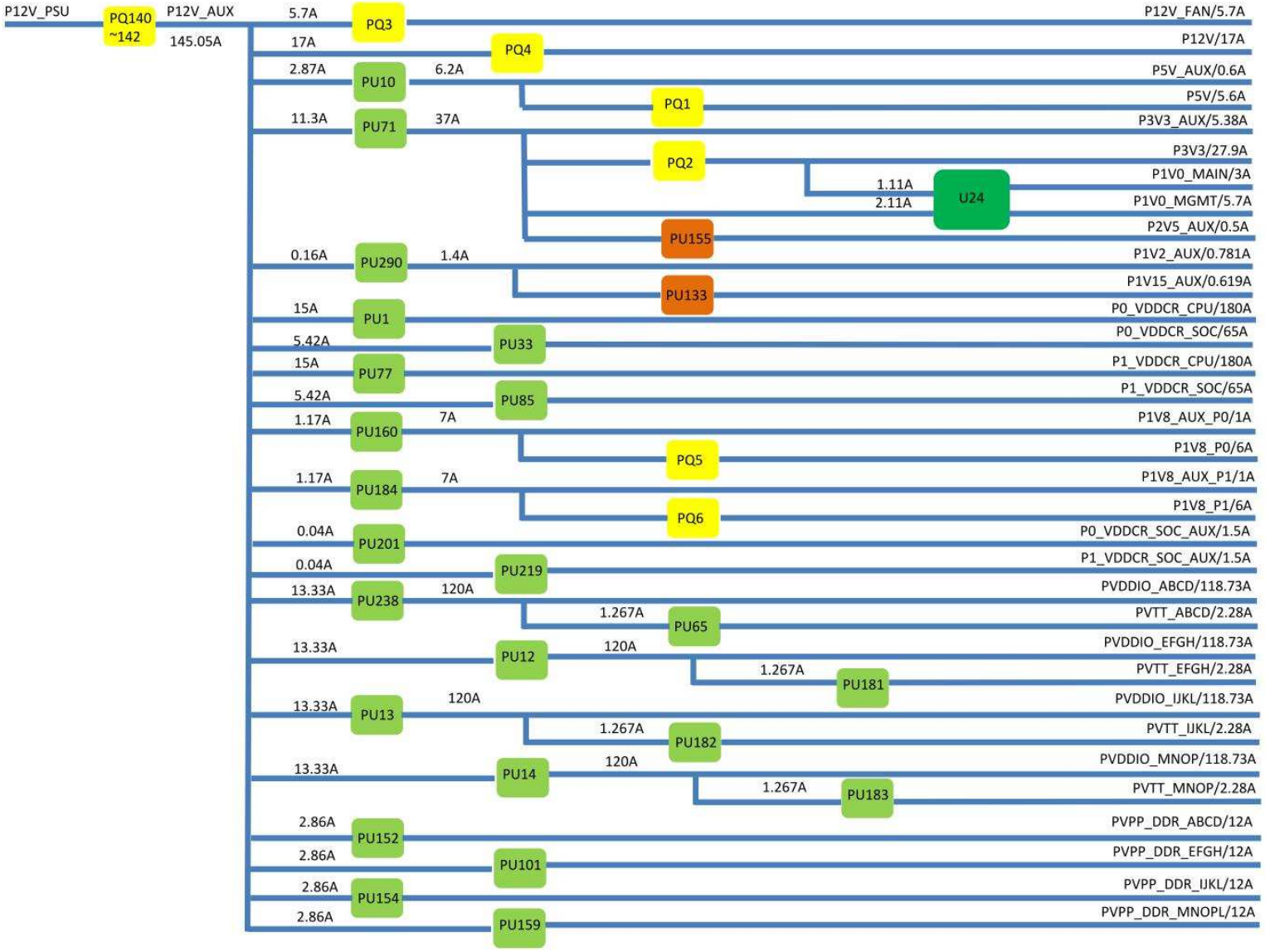
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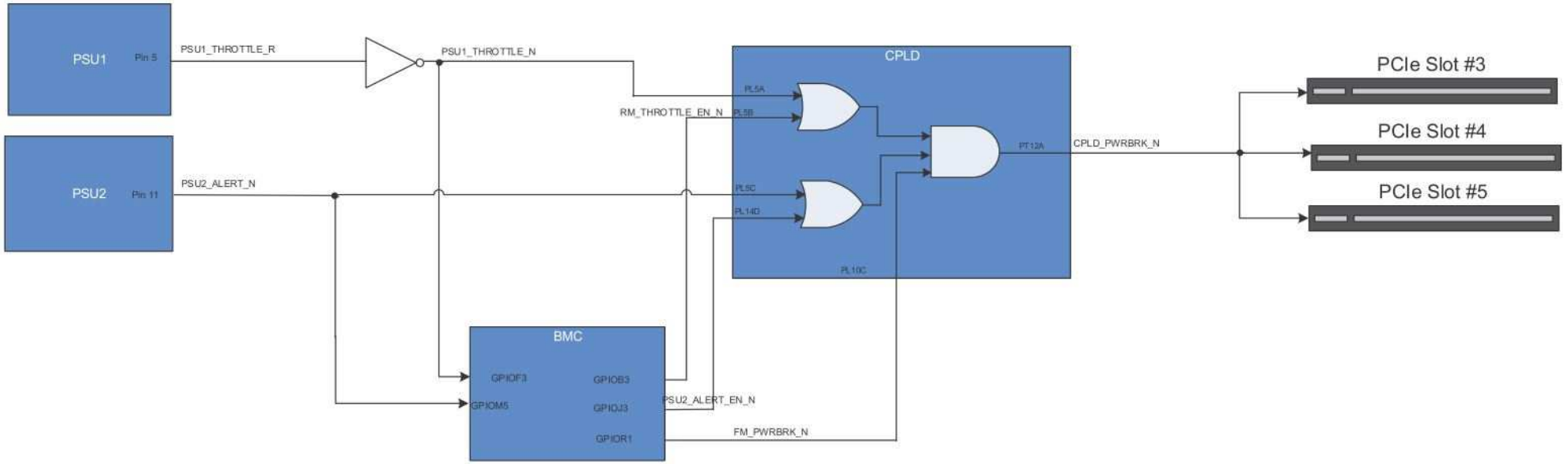
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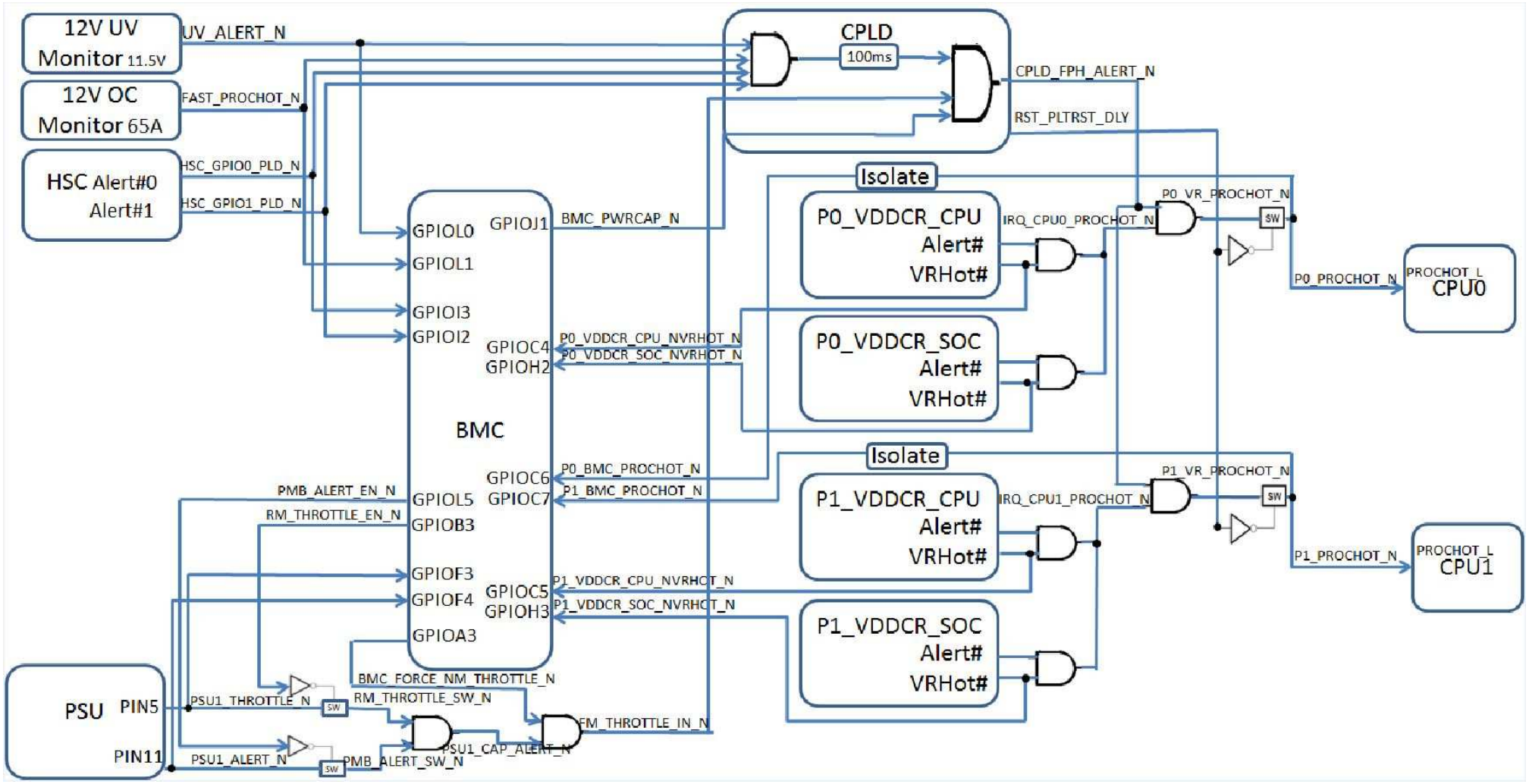
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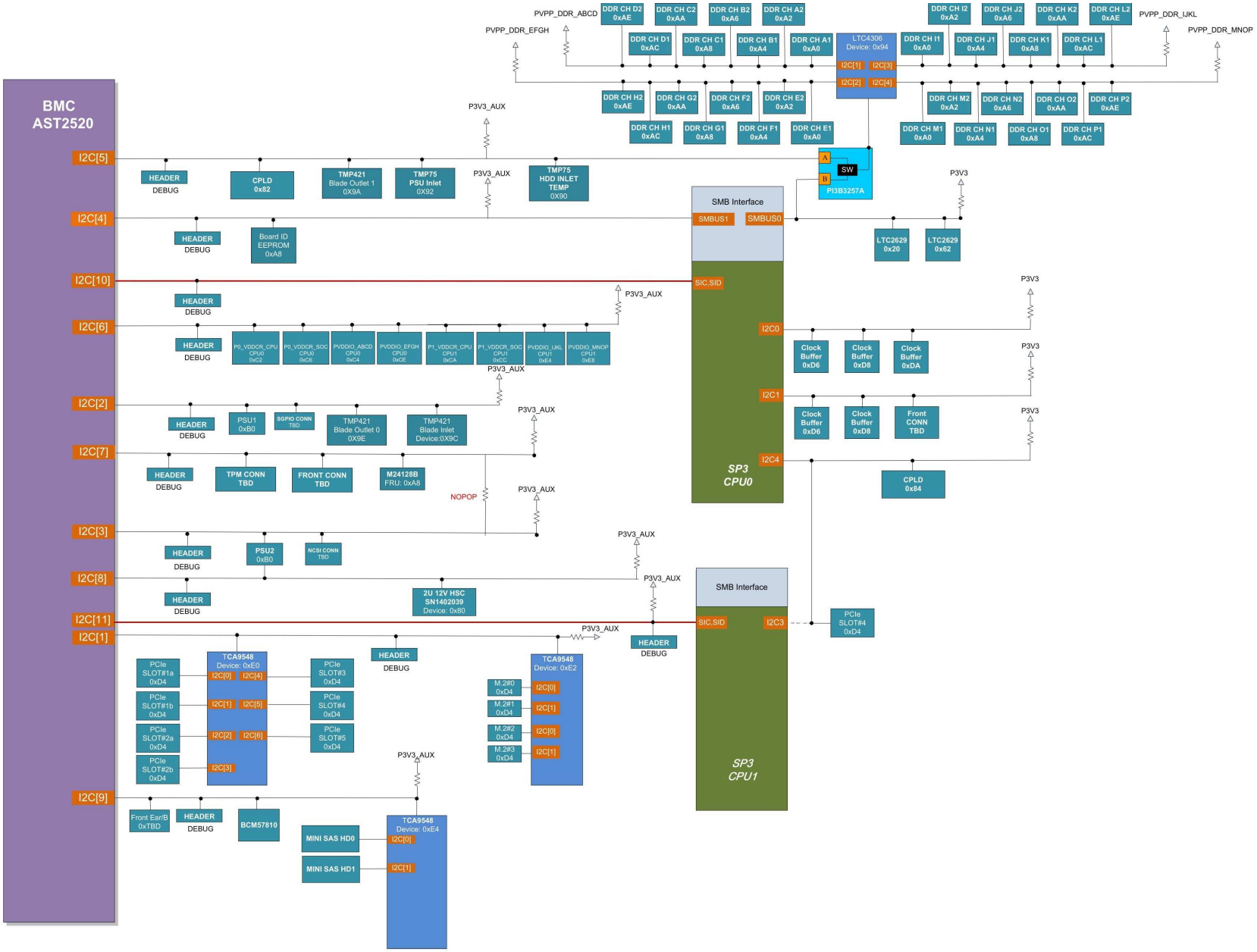
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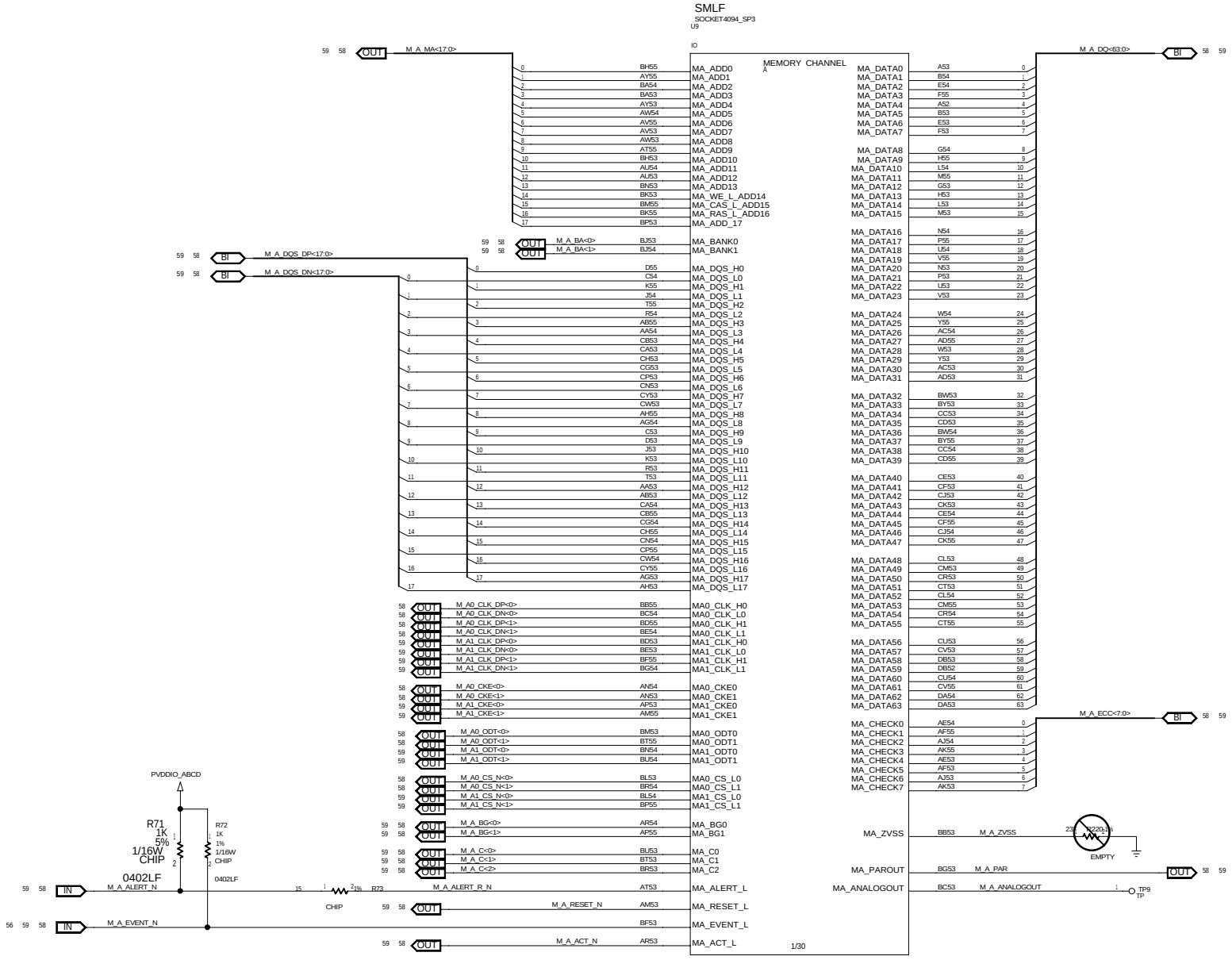
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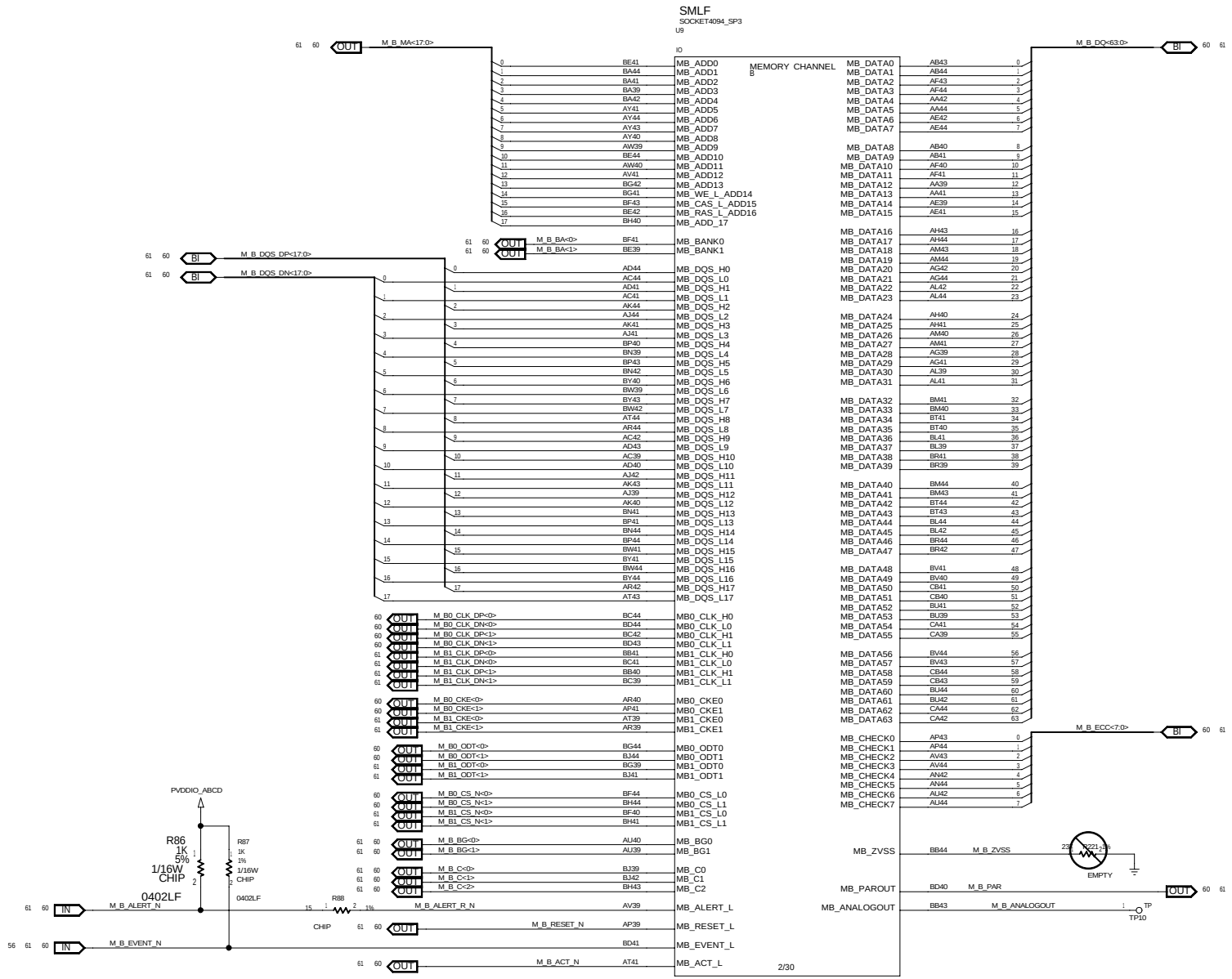
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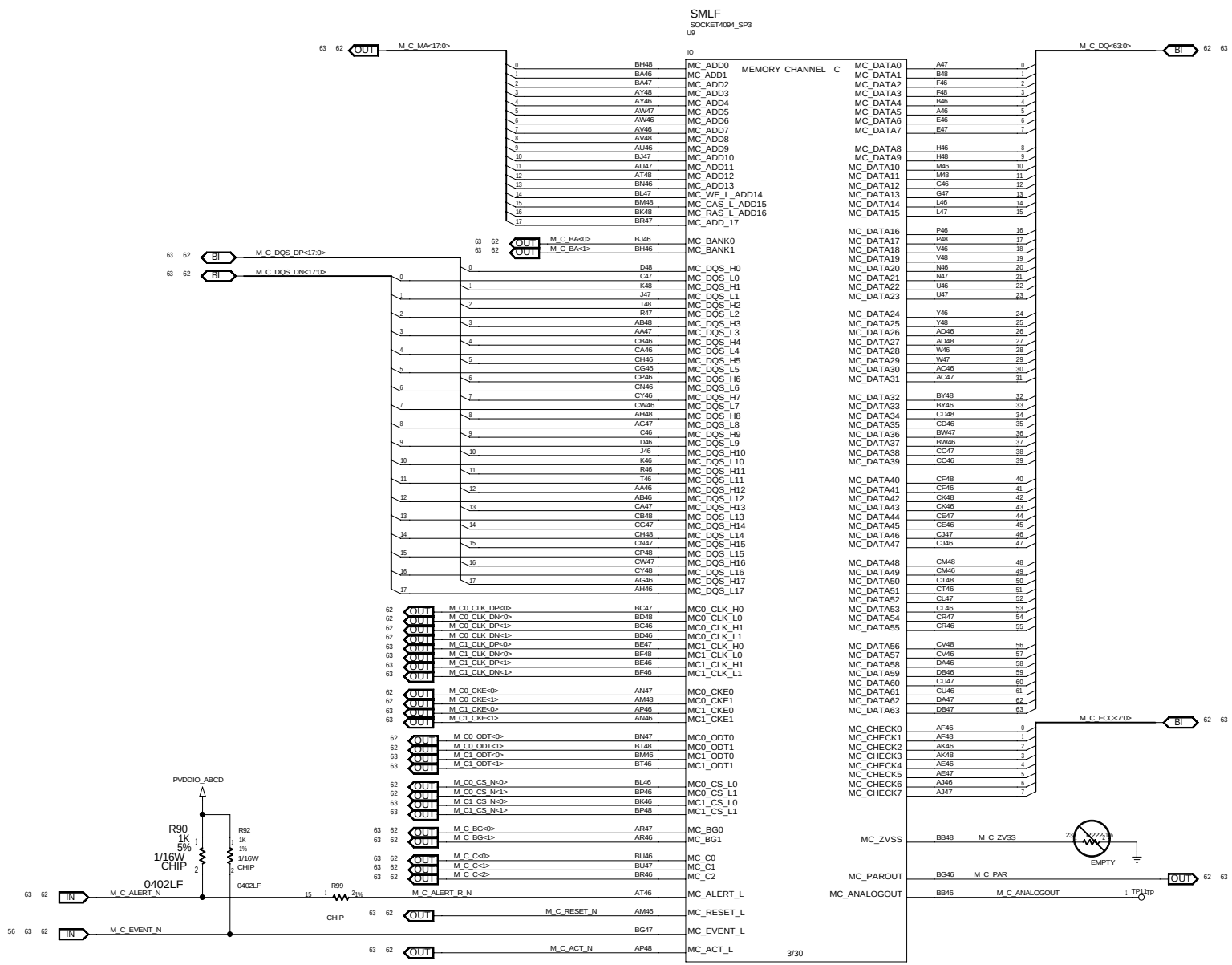


P0 MEMORY CHA (1 OF 19)

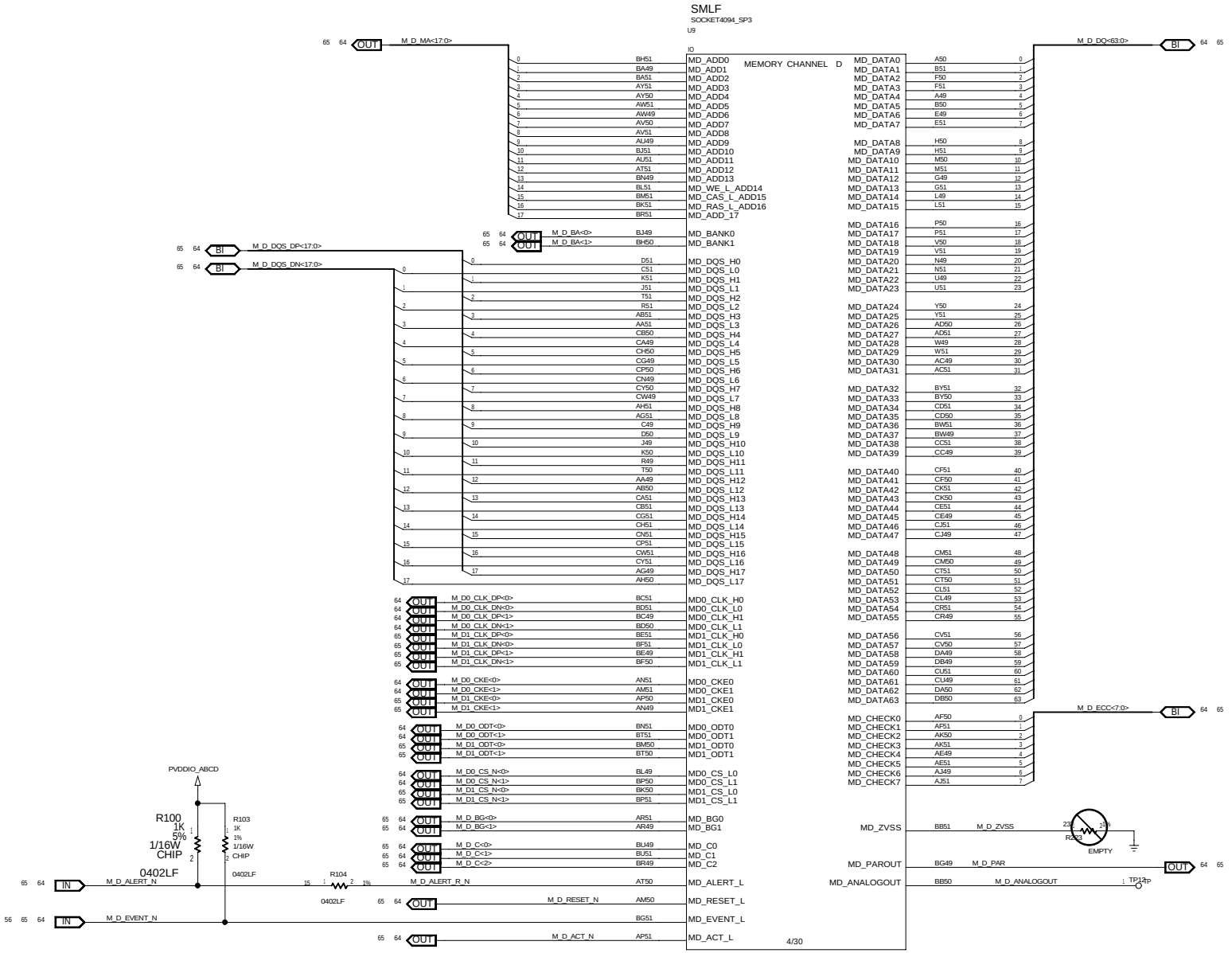
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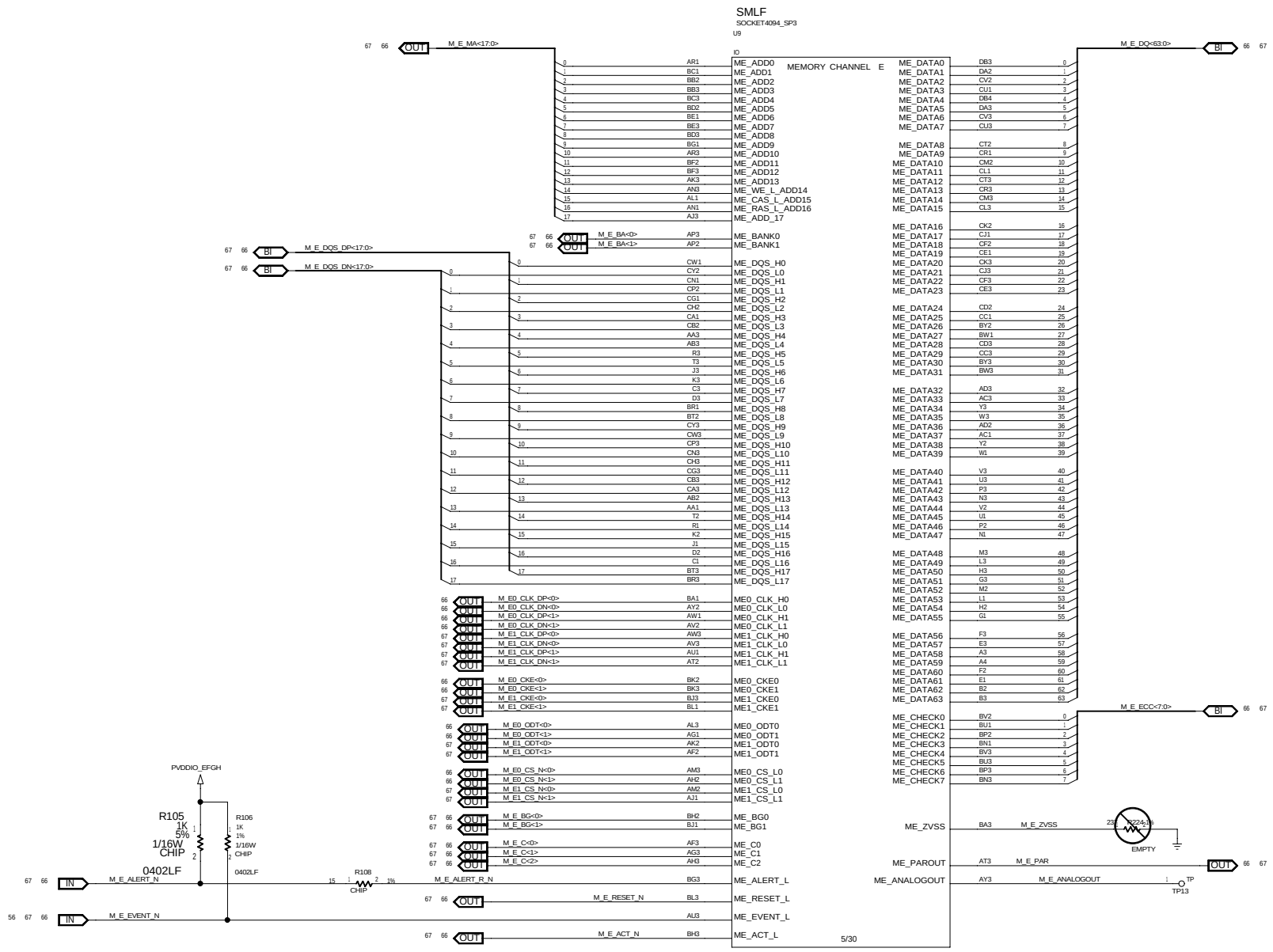


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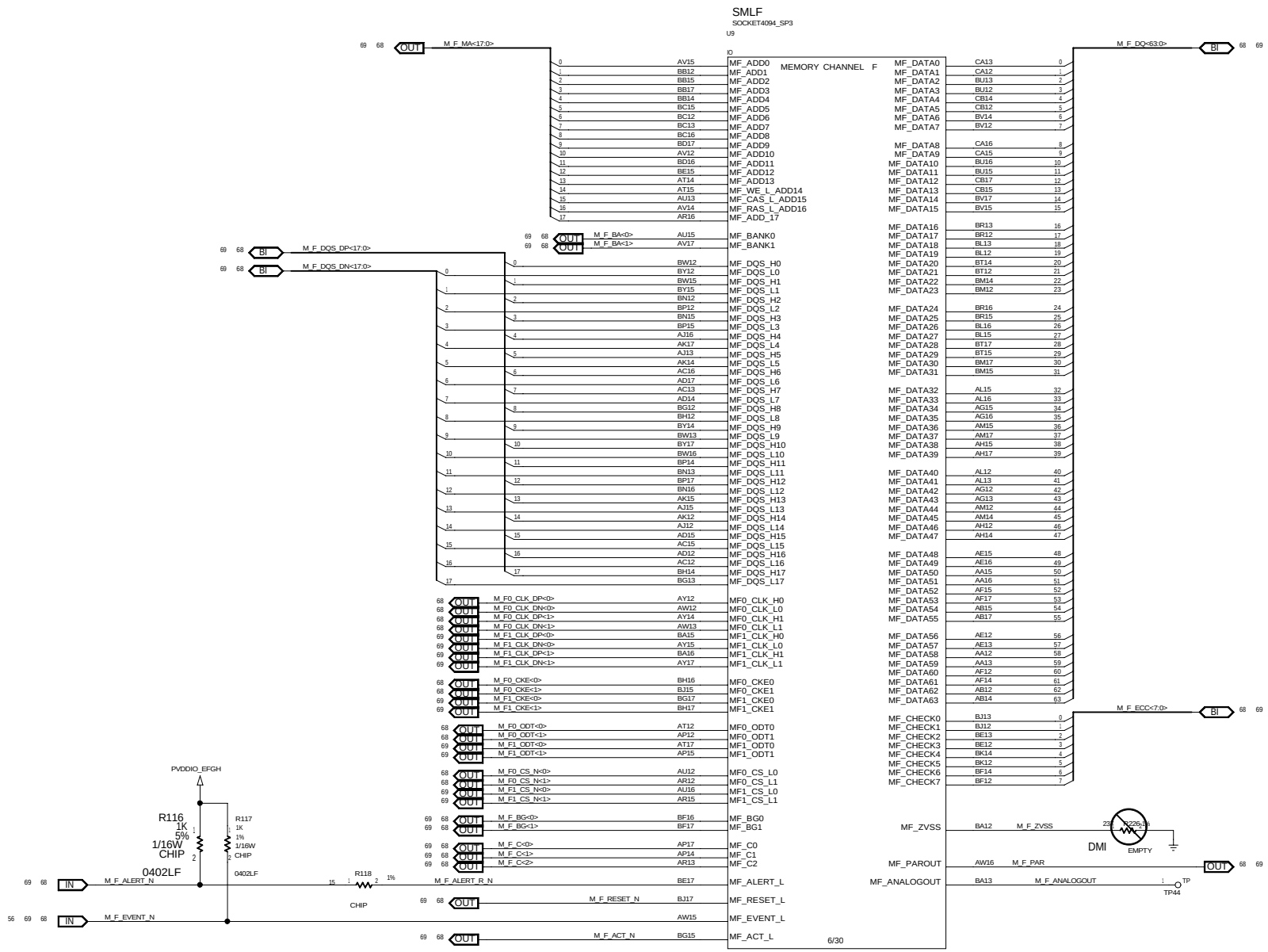
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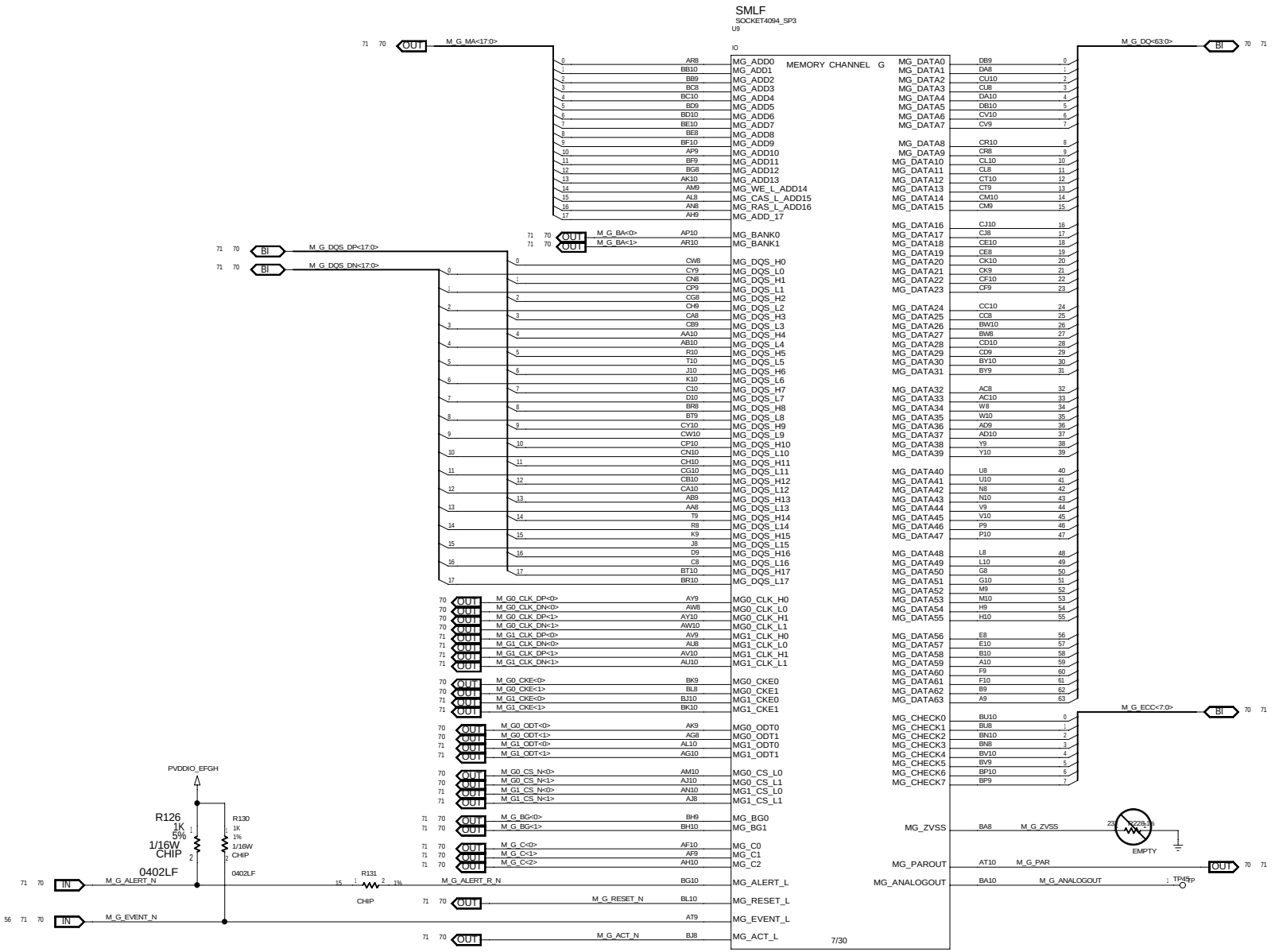
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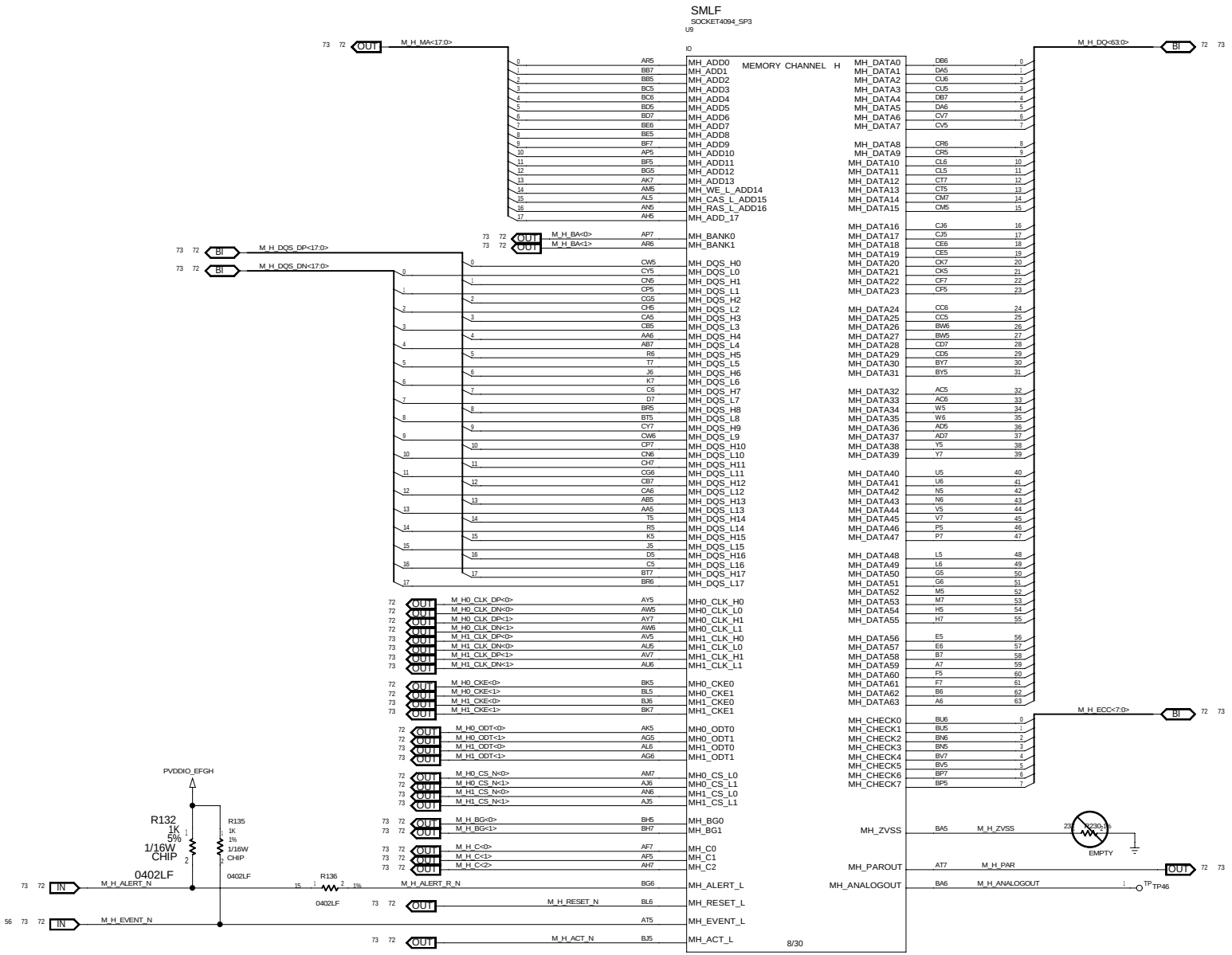


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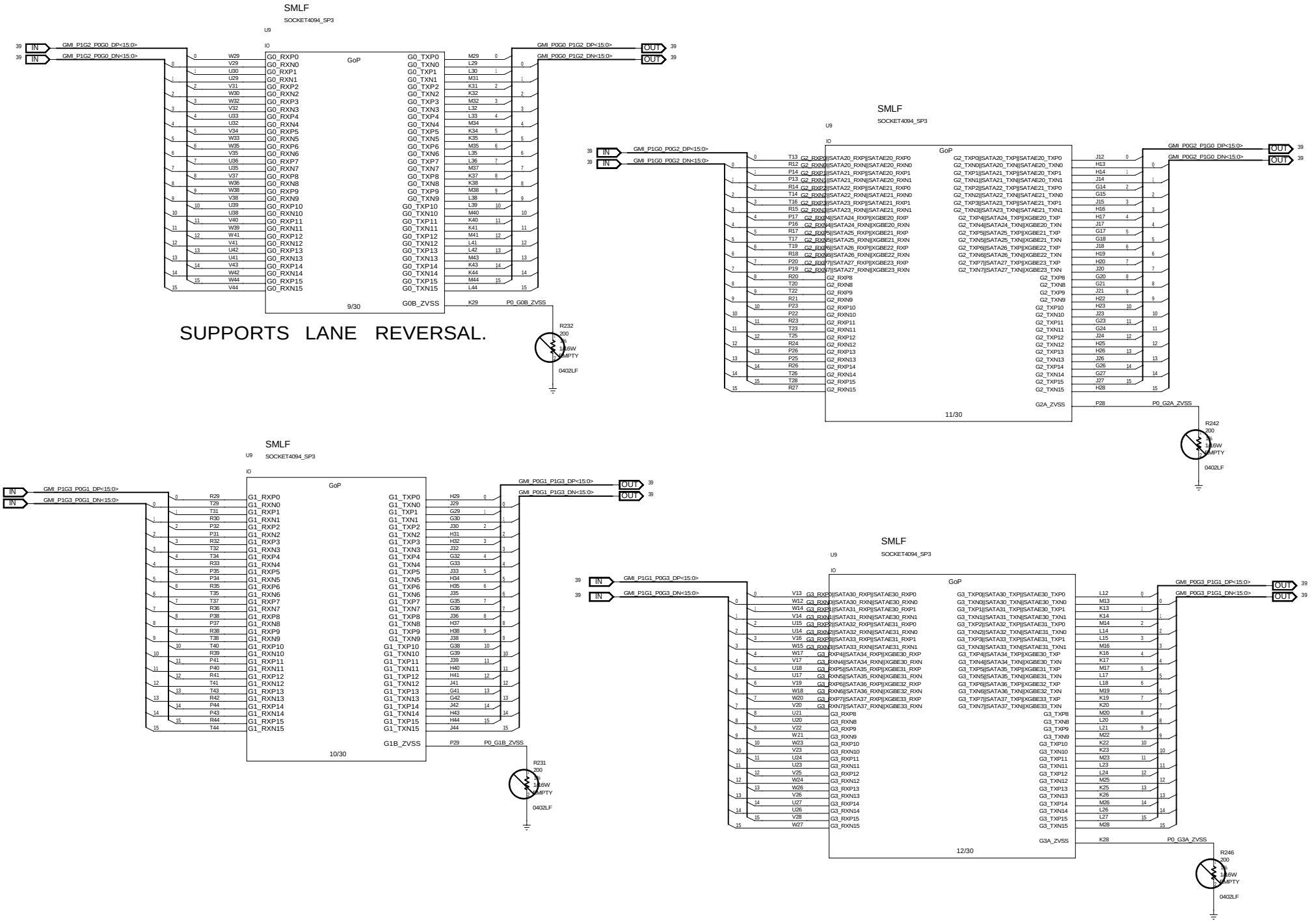
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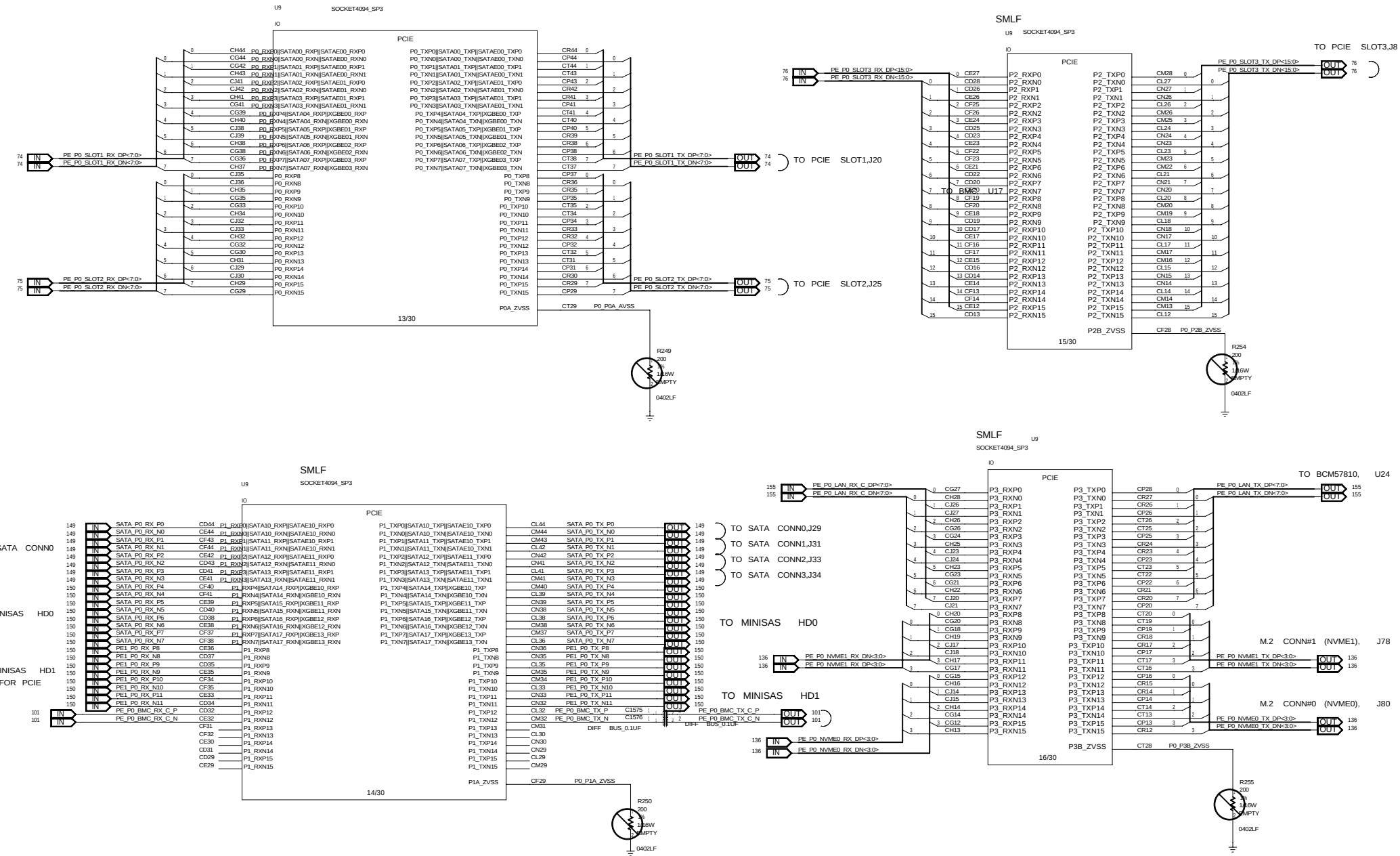
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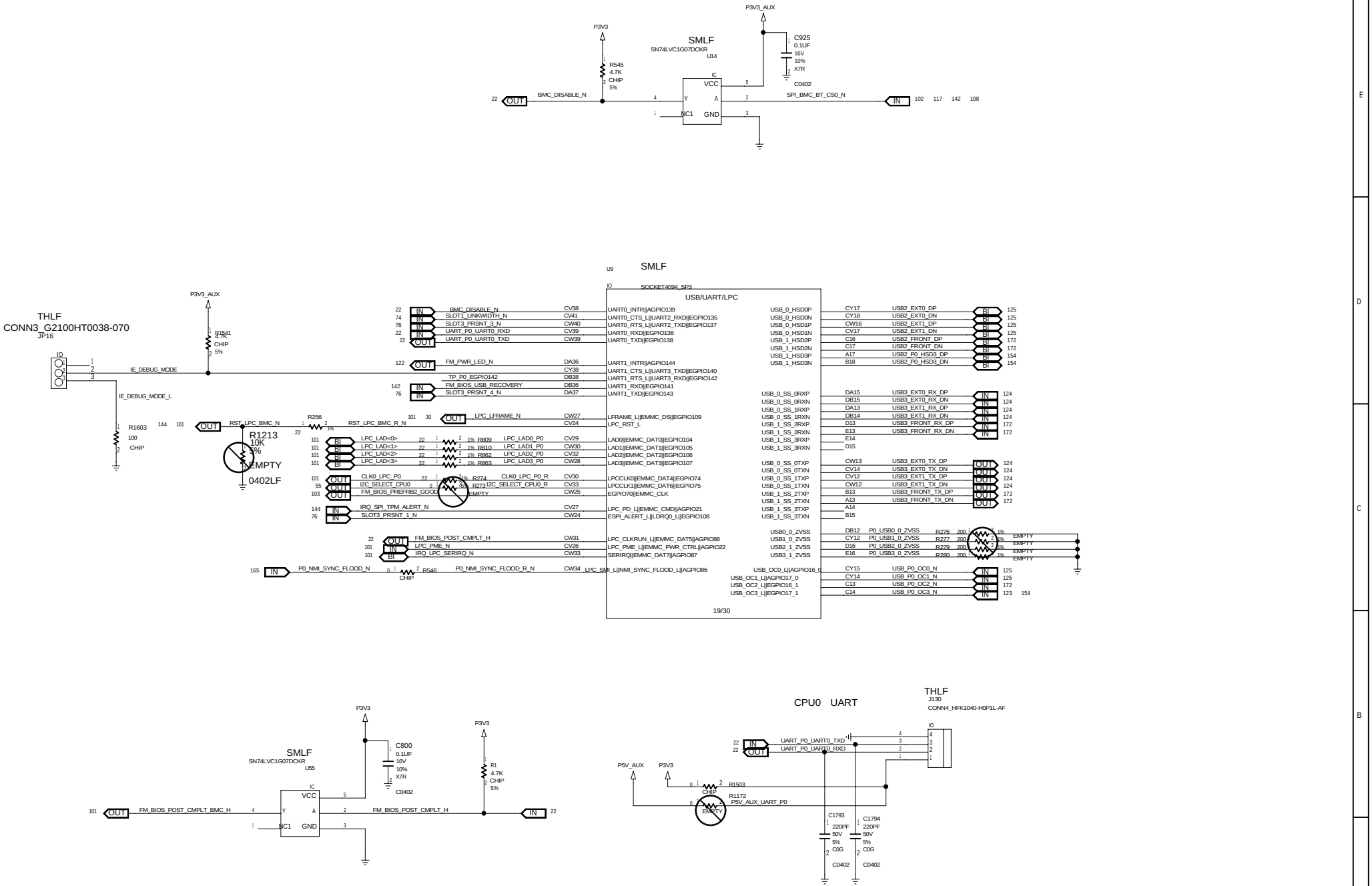
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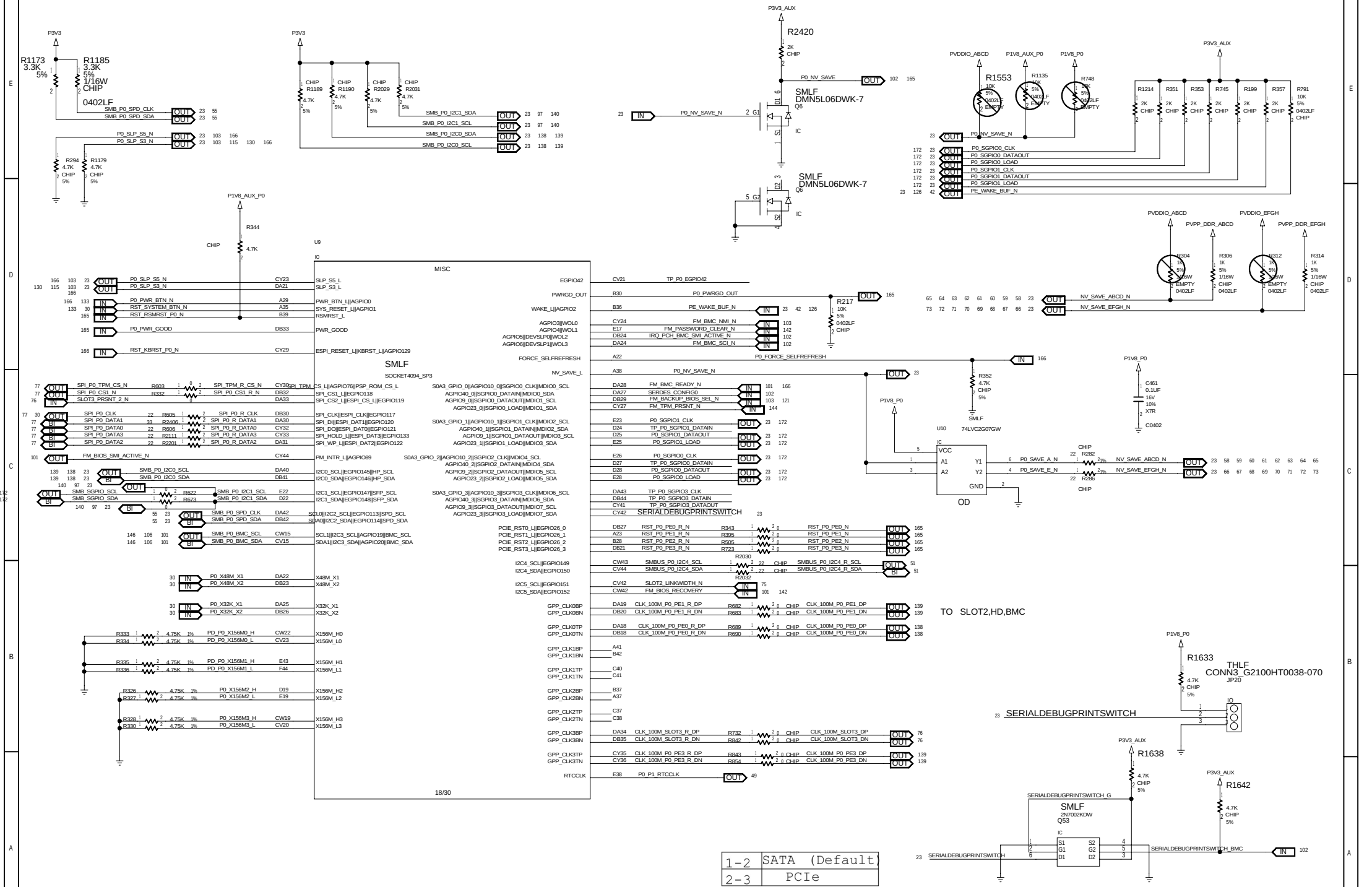
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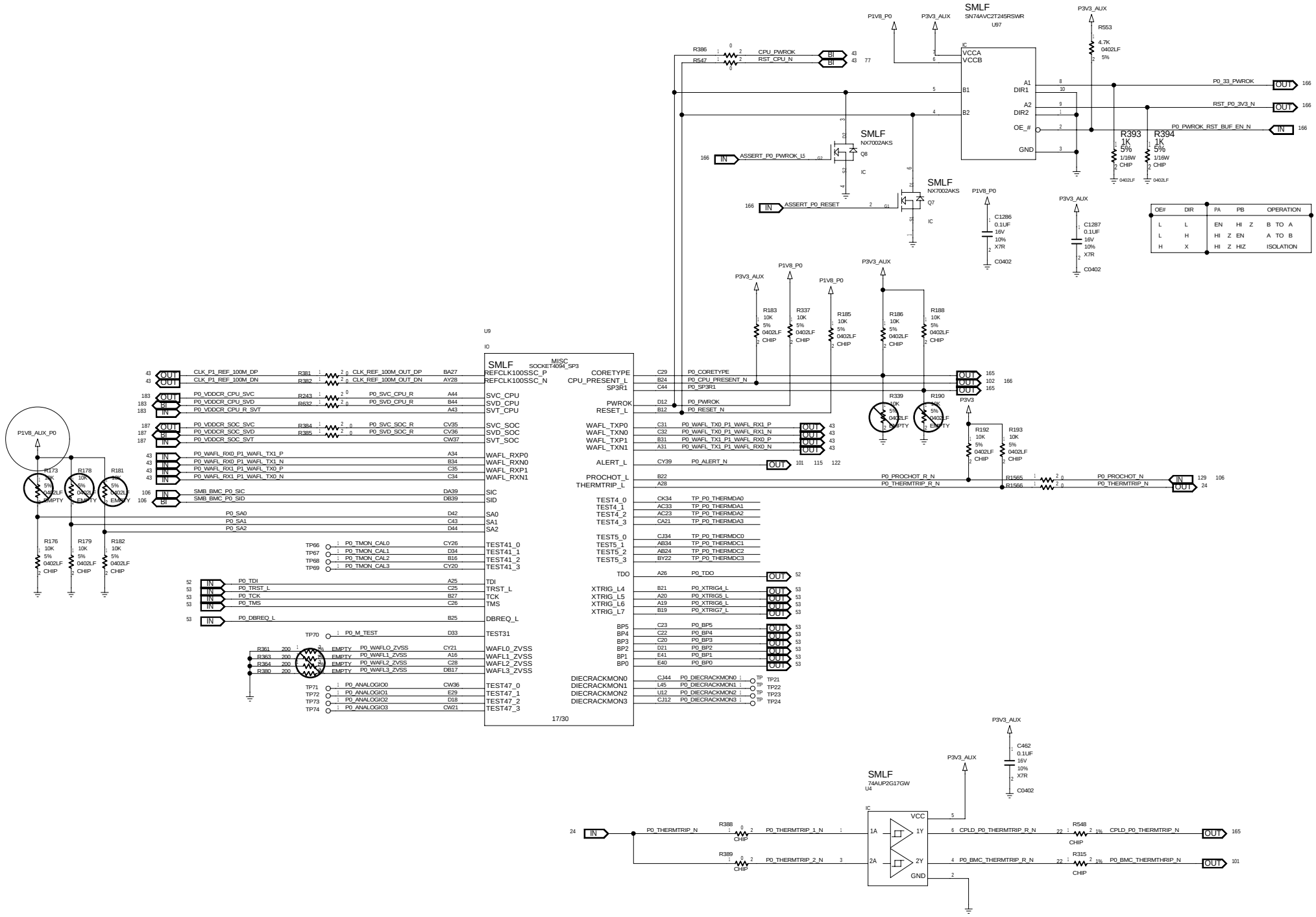


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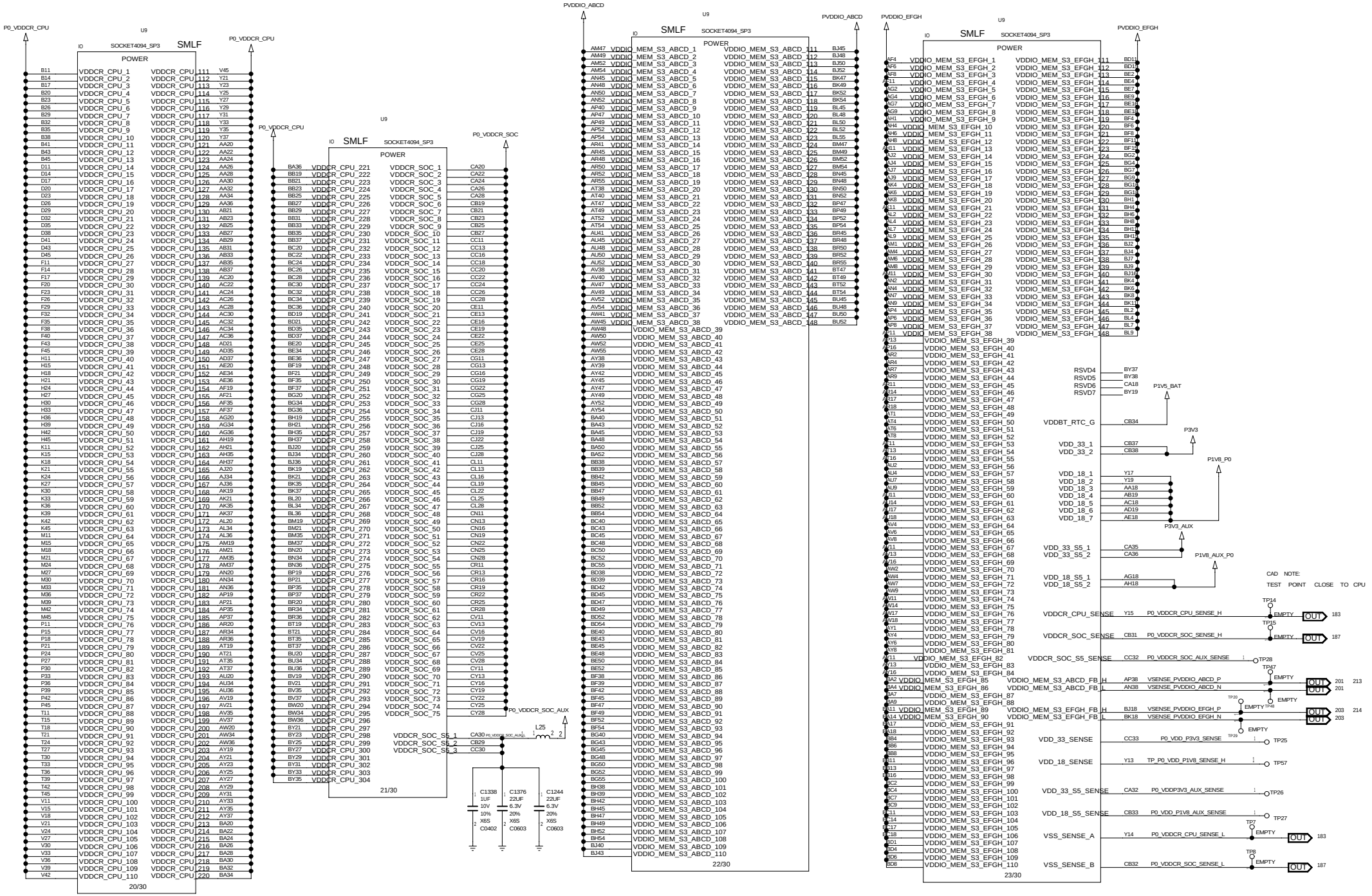
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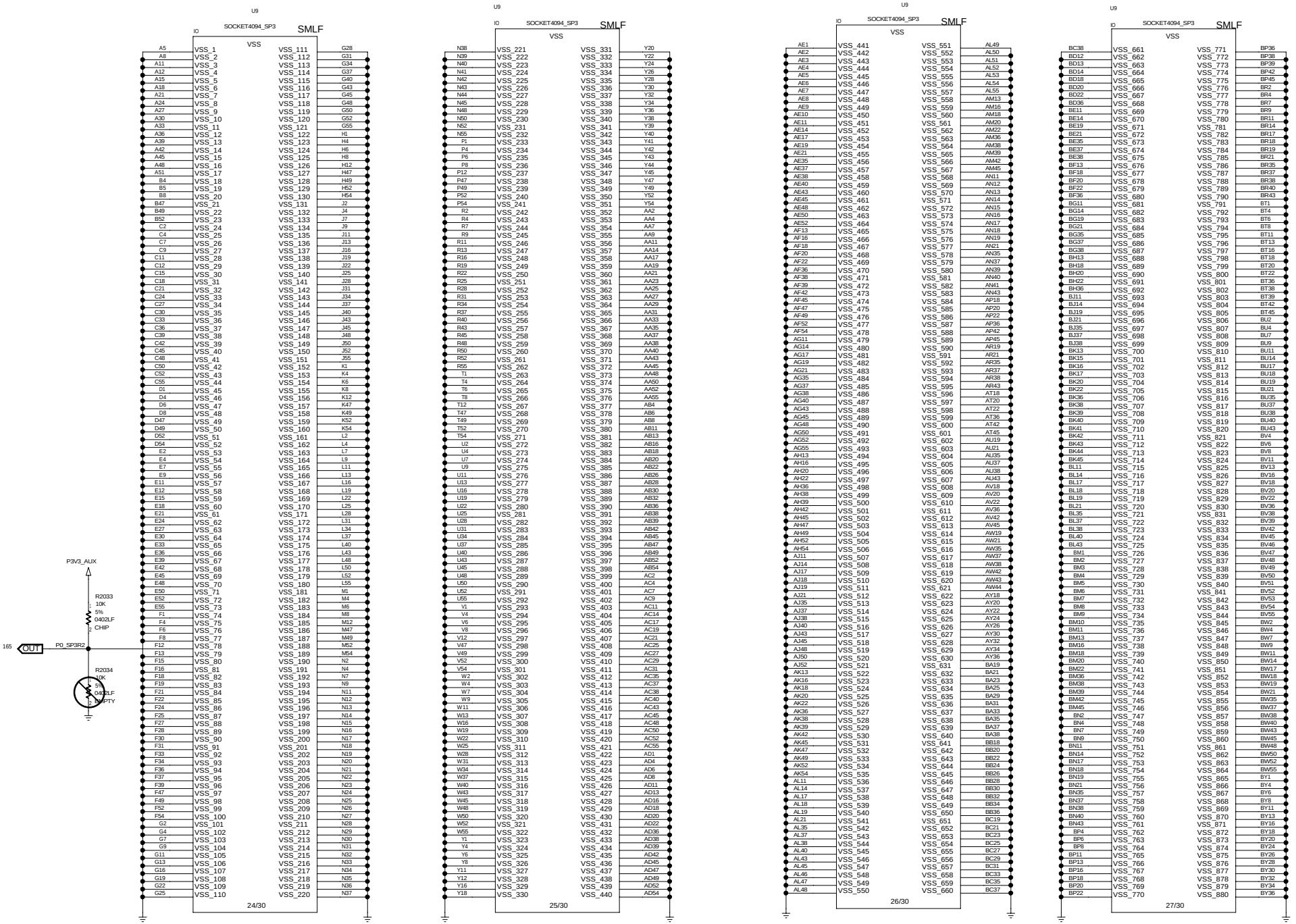


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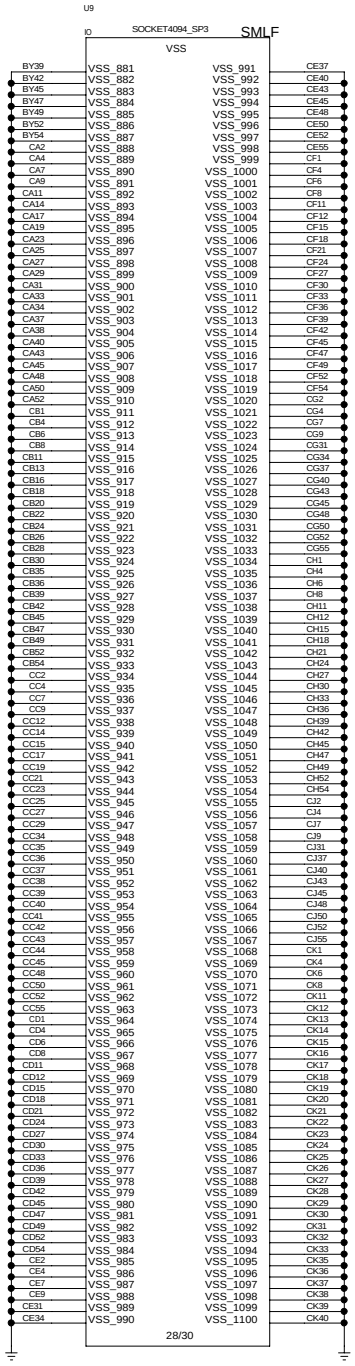
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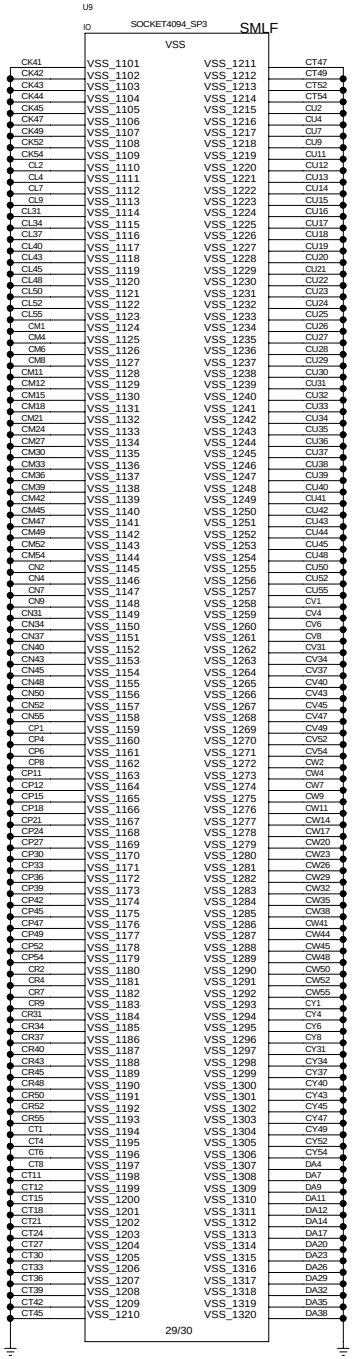
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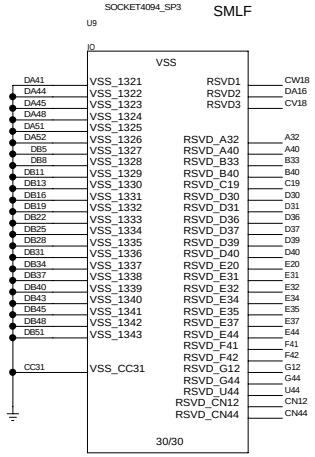


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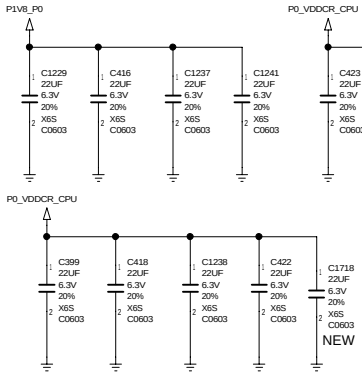


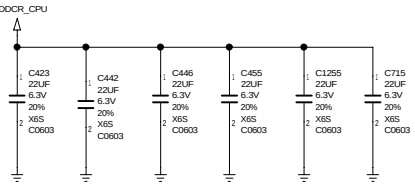




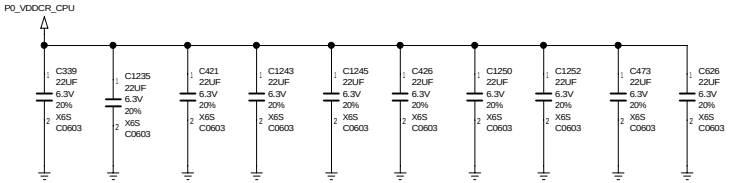
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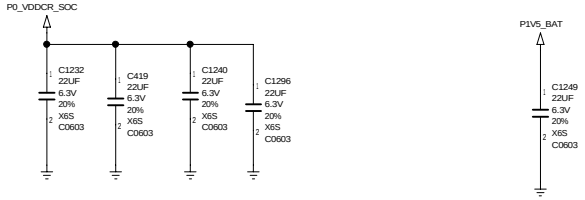
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- NORTH



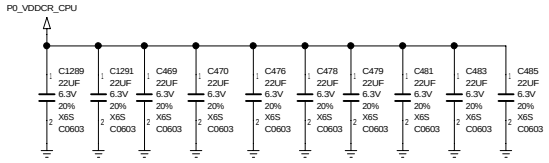


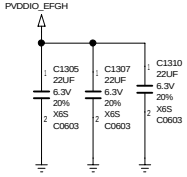
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- SOUTH

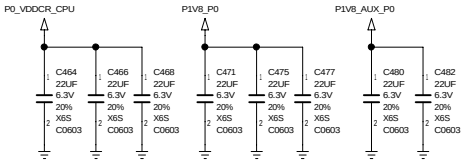


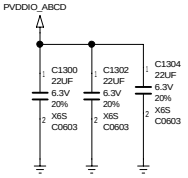


BOTTOM SIDE- NORTH

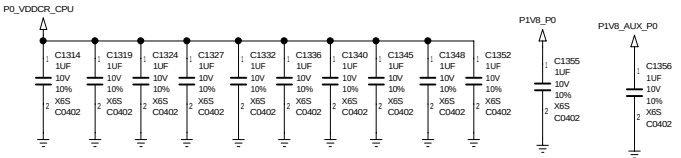


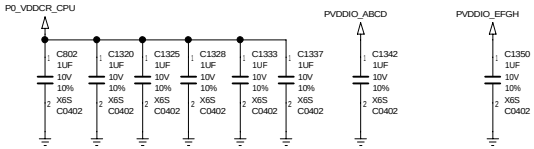




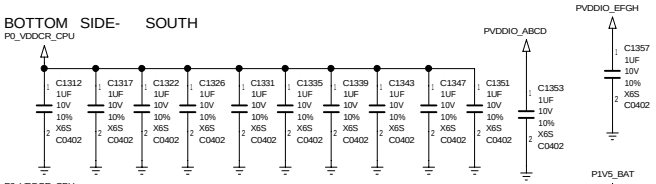


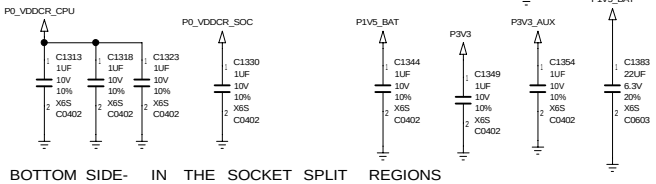
BOTTOM SIDE- NORTH





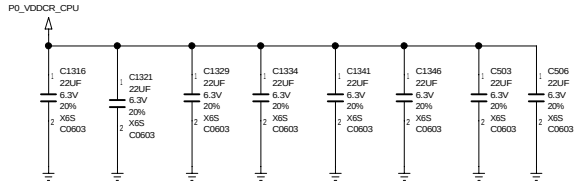
BOTTOM SIDE- SOUTH



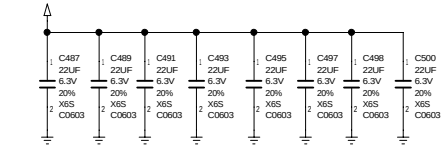


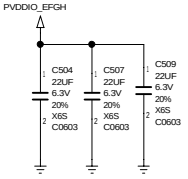
BOTTOM SIDE- IN THE SOCKET SPLIT REGIONS

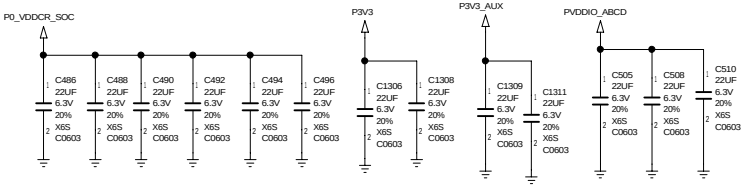
OEM SKT ONLY: NOT AVAILABLE IN SLT;CAN BE USED FOR RESISTORS



BOTTOM SIDE- SOUTH

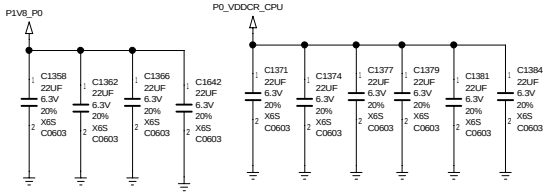


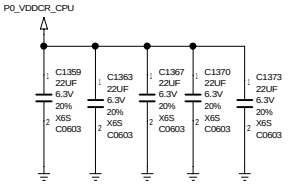




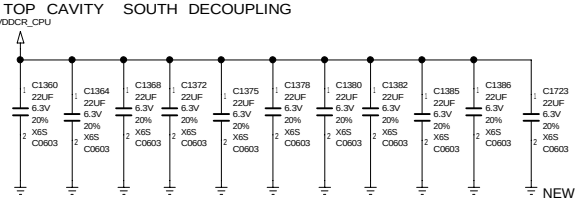
TOP SIDE DECOUPLING

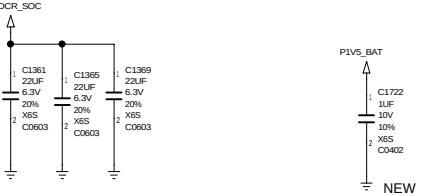
TOP CAVITY-NORTH DECOUPLING



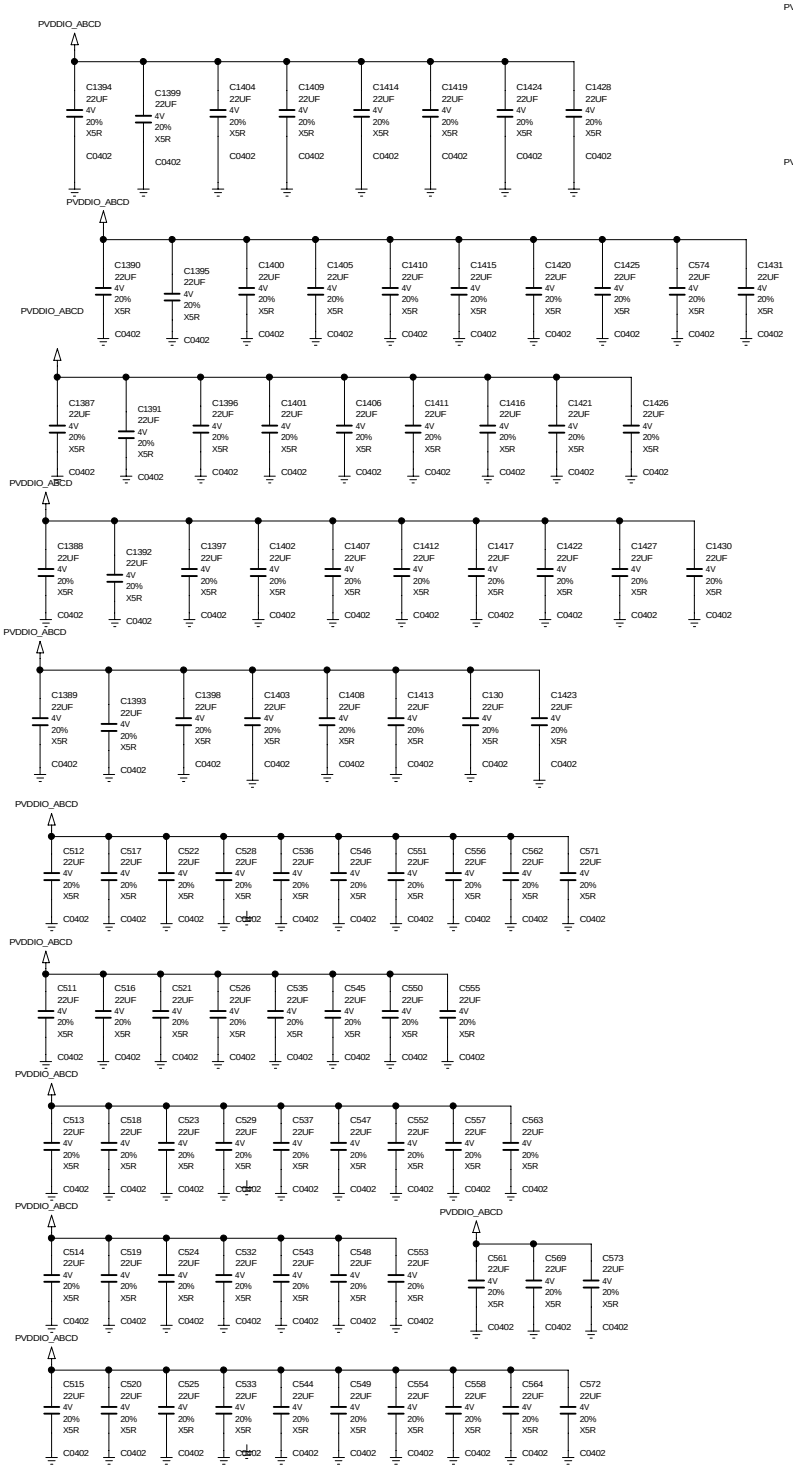


TOP CAVITY SOUTH DECOUPLING





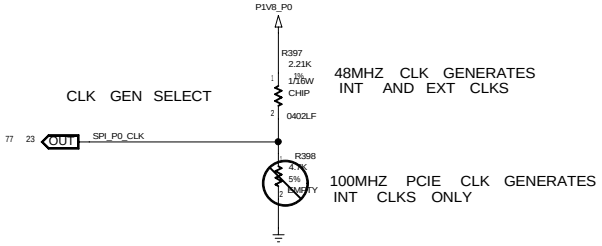
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		REVIEWER:		REV: <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:31 2017	SHEET 28 OF 226

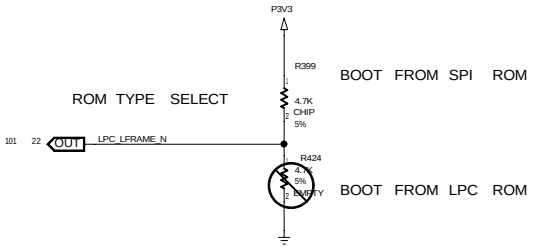


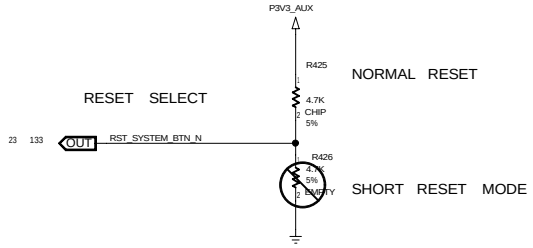
P0 DIMM DECOUPLING (18 OF 19)

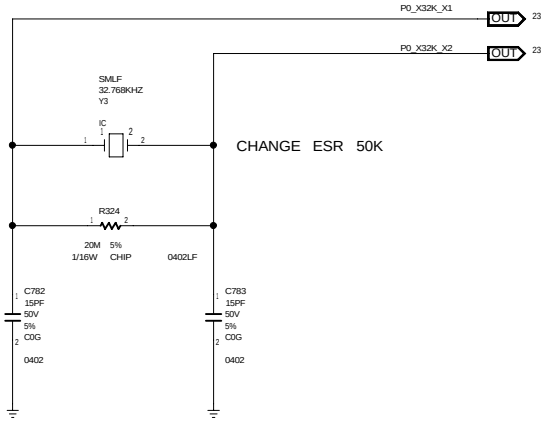
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	SIZE C	DATE Fri Dec 15 20:21:31 2017	SHEET 29 OF 226

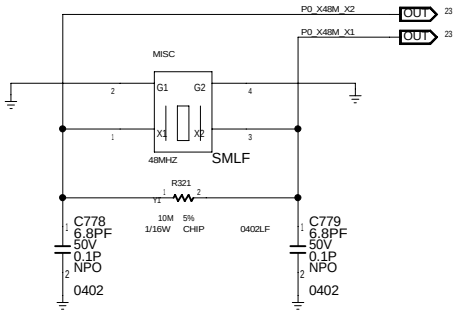
PROCESSOR STRAPS





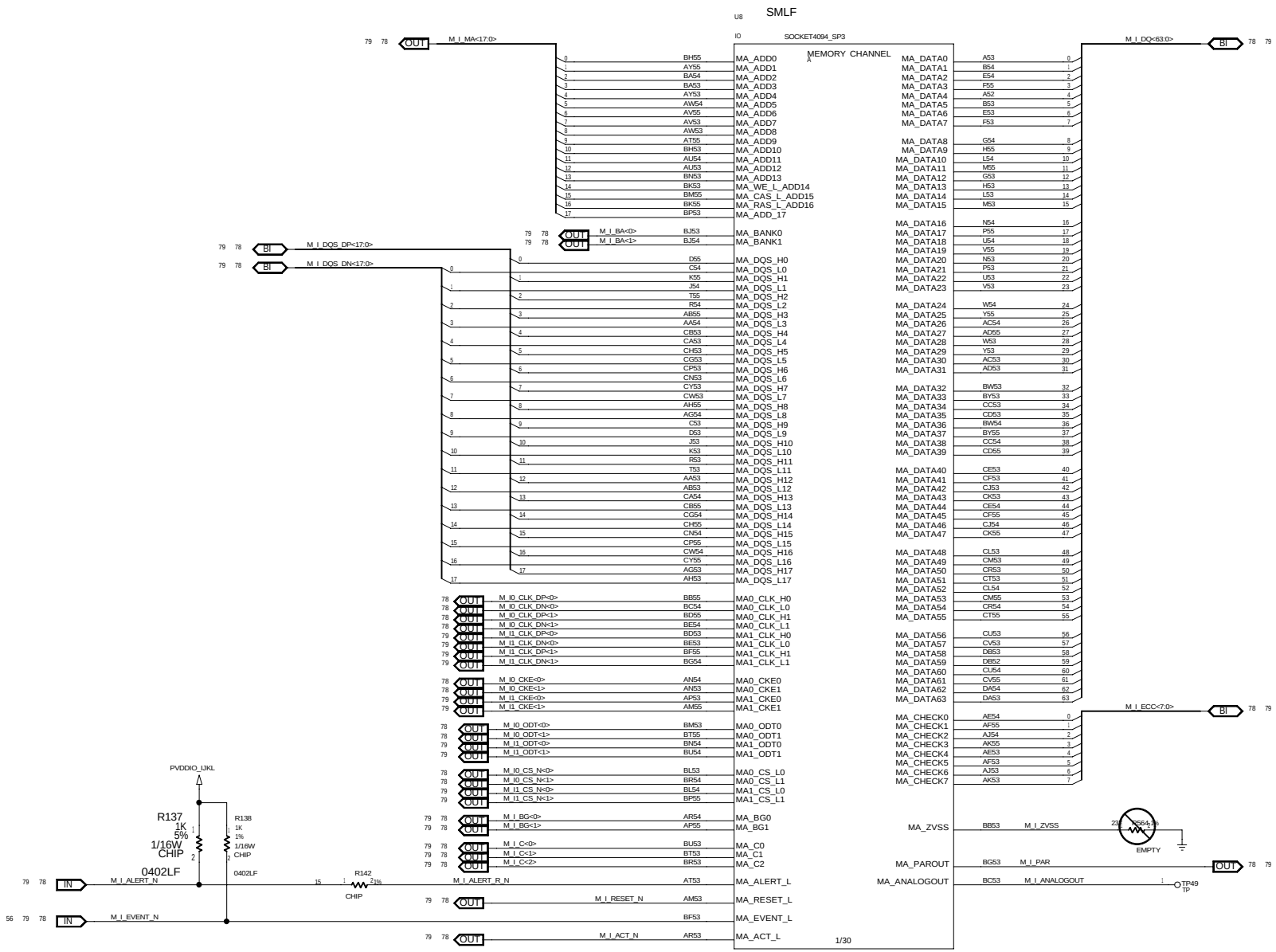






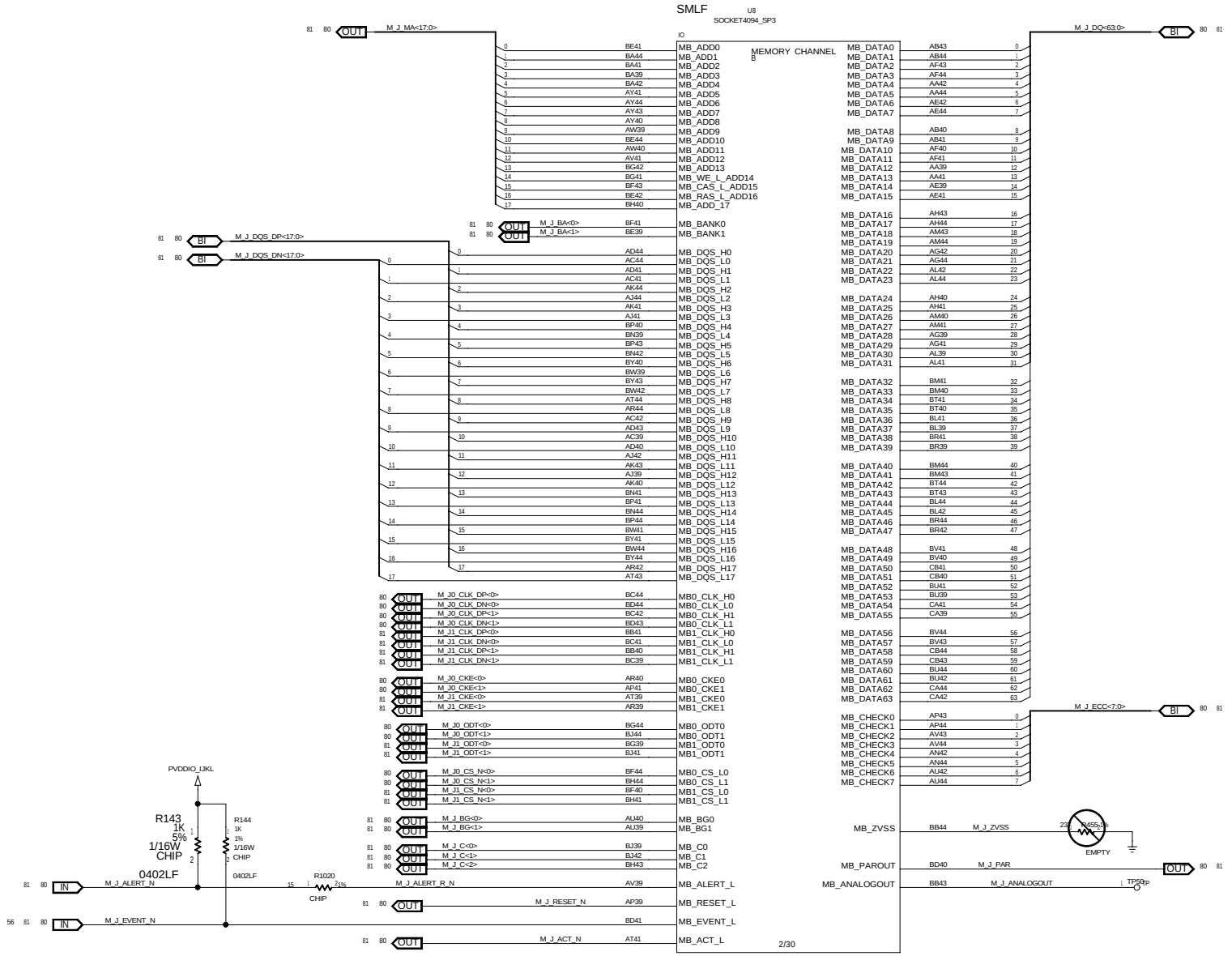
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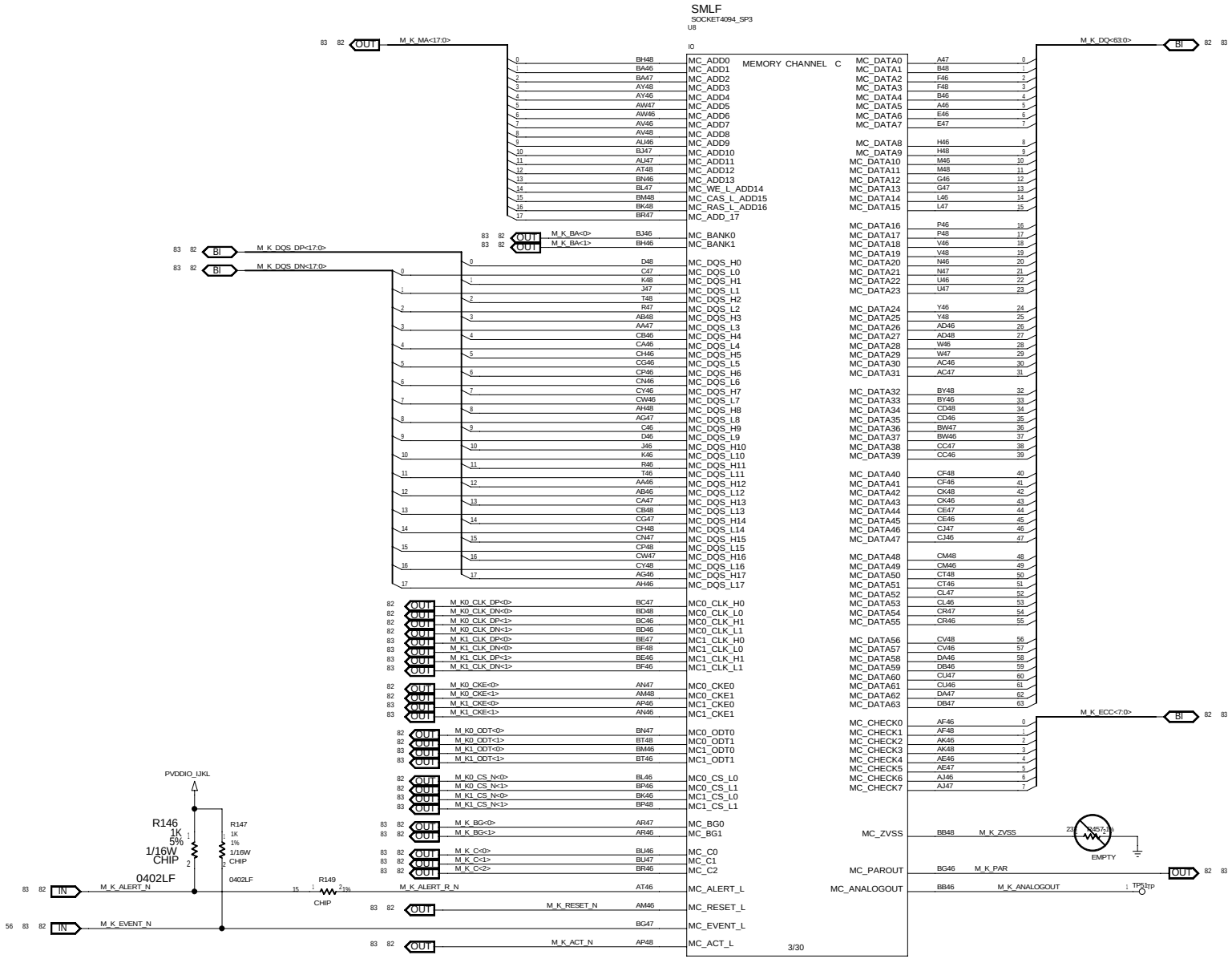
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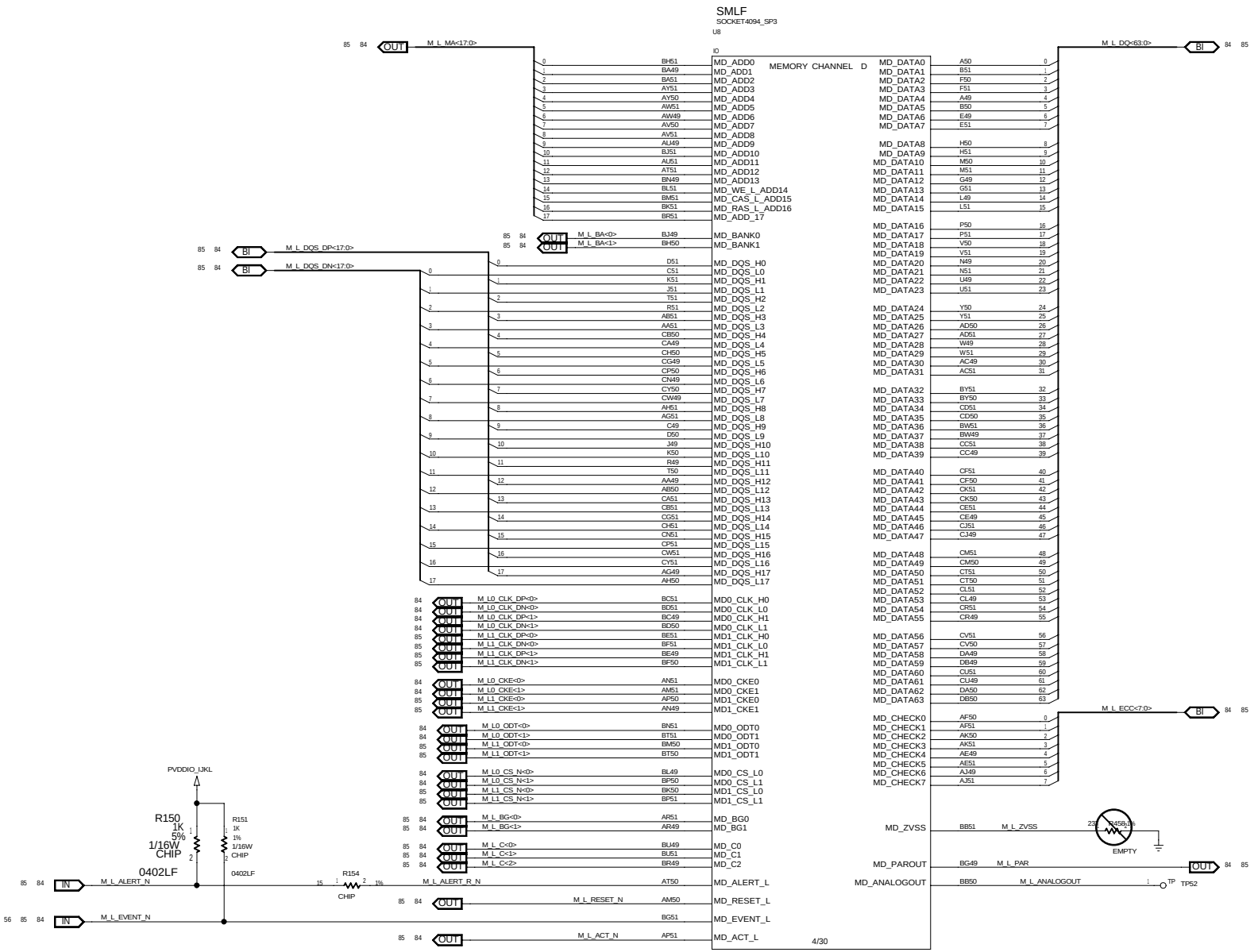
P1 MEMORY CHJ (2 OF 19)

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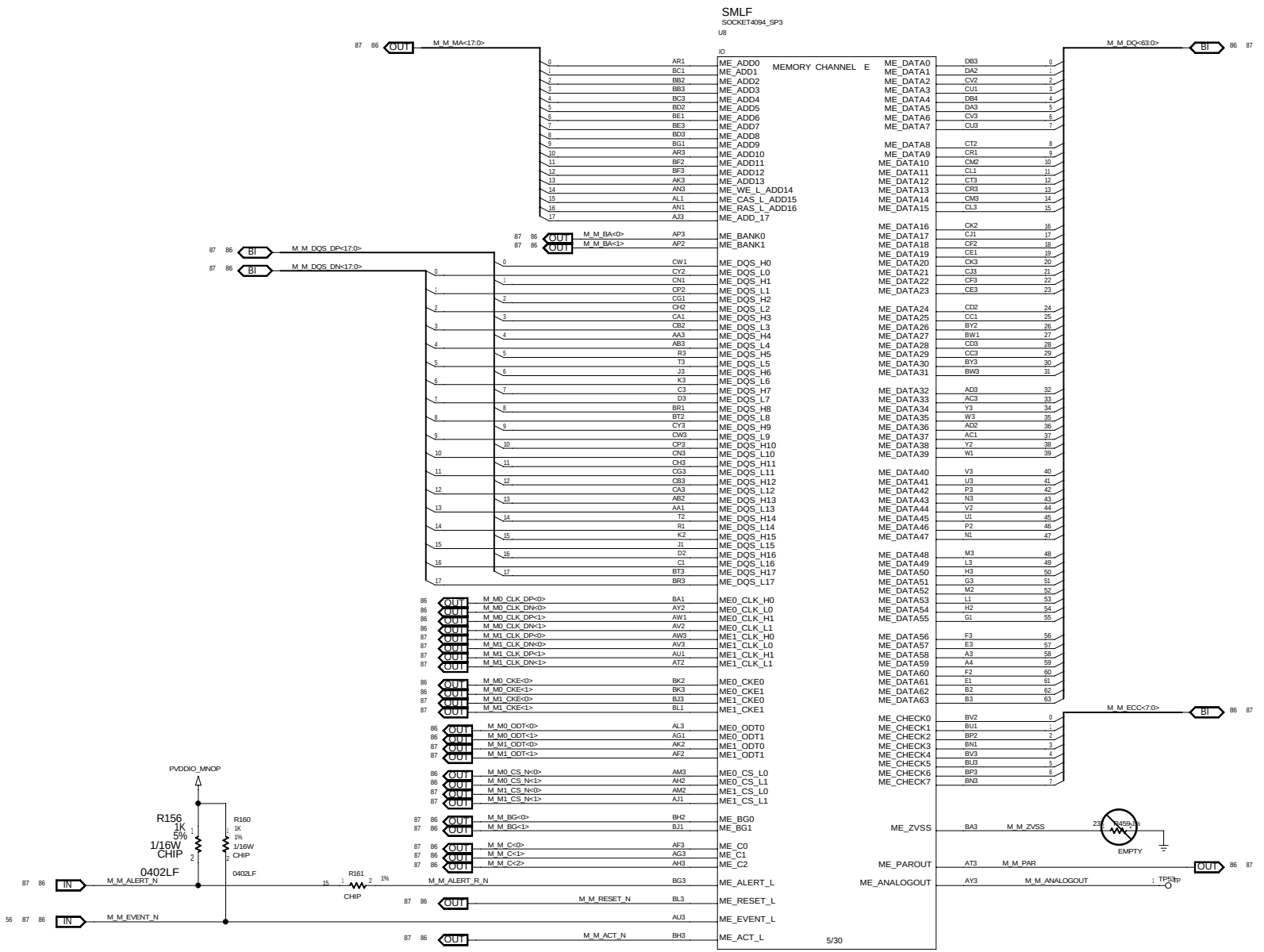
P1 MEMORY CHK (3 OF 19)

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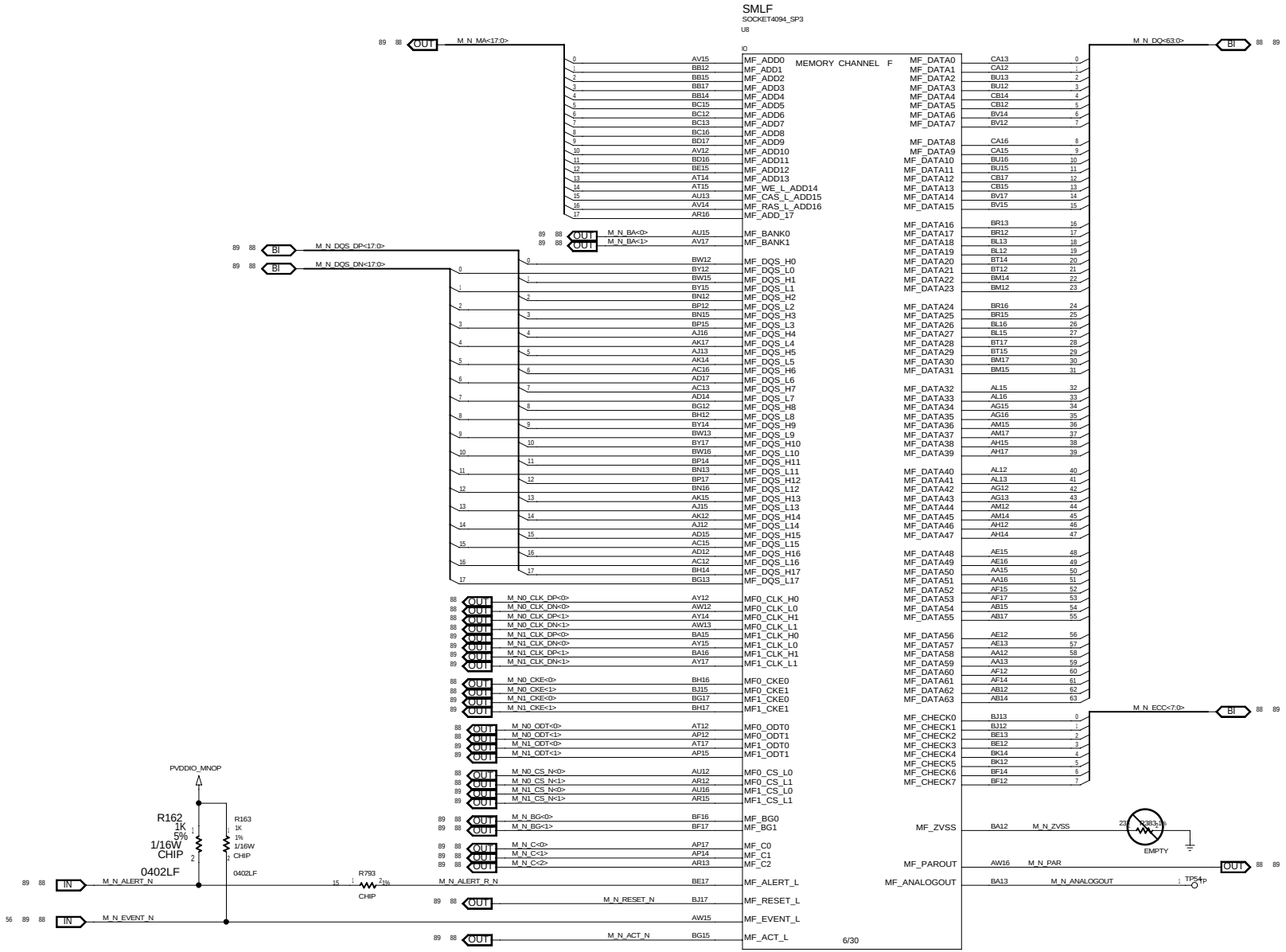


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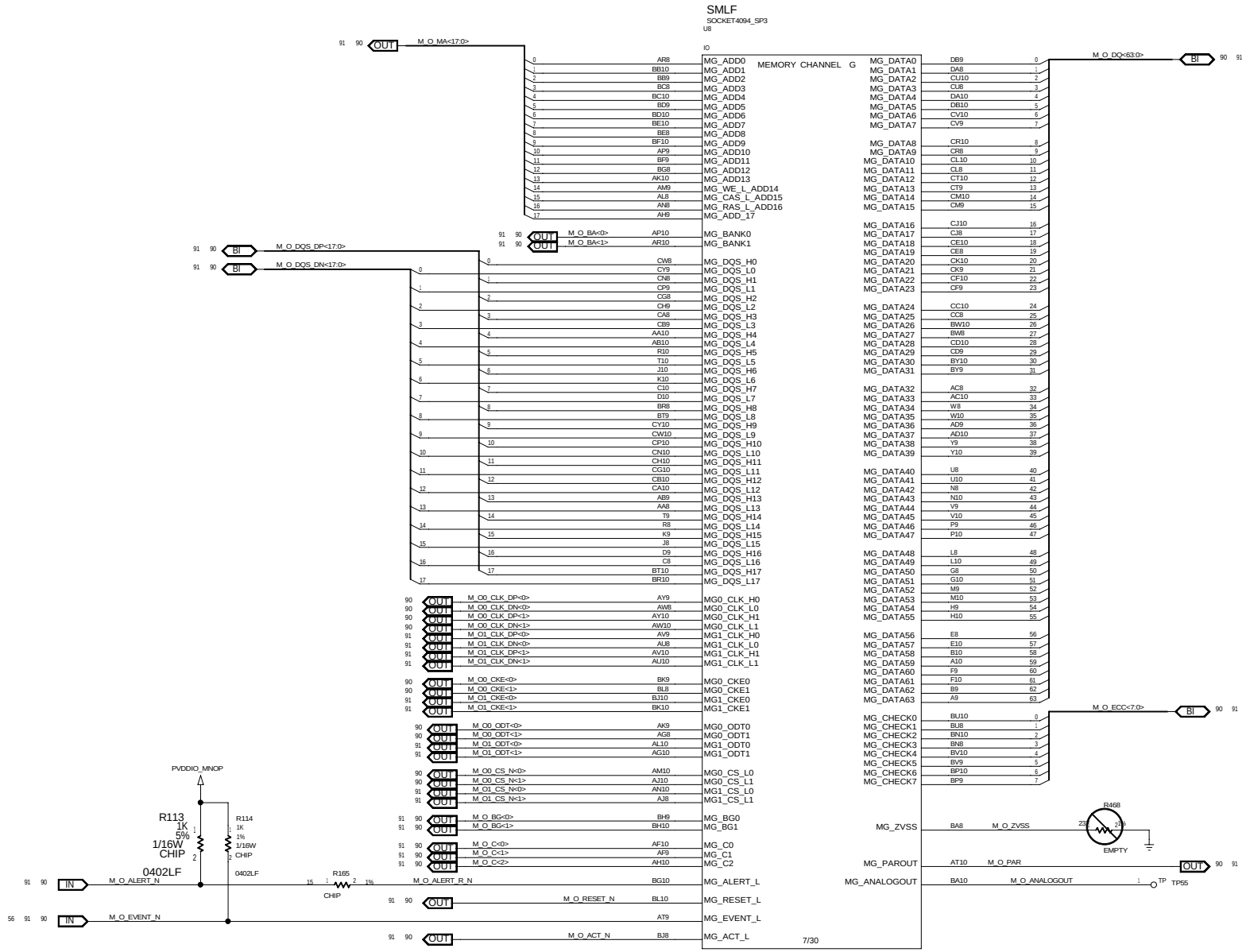


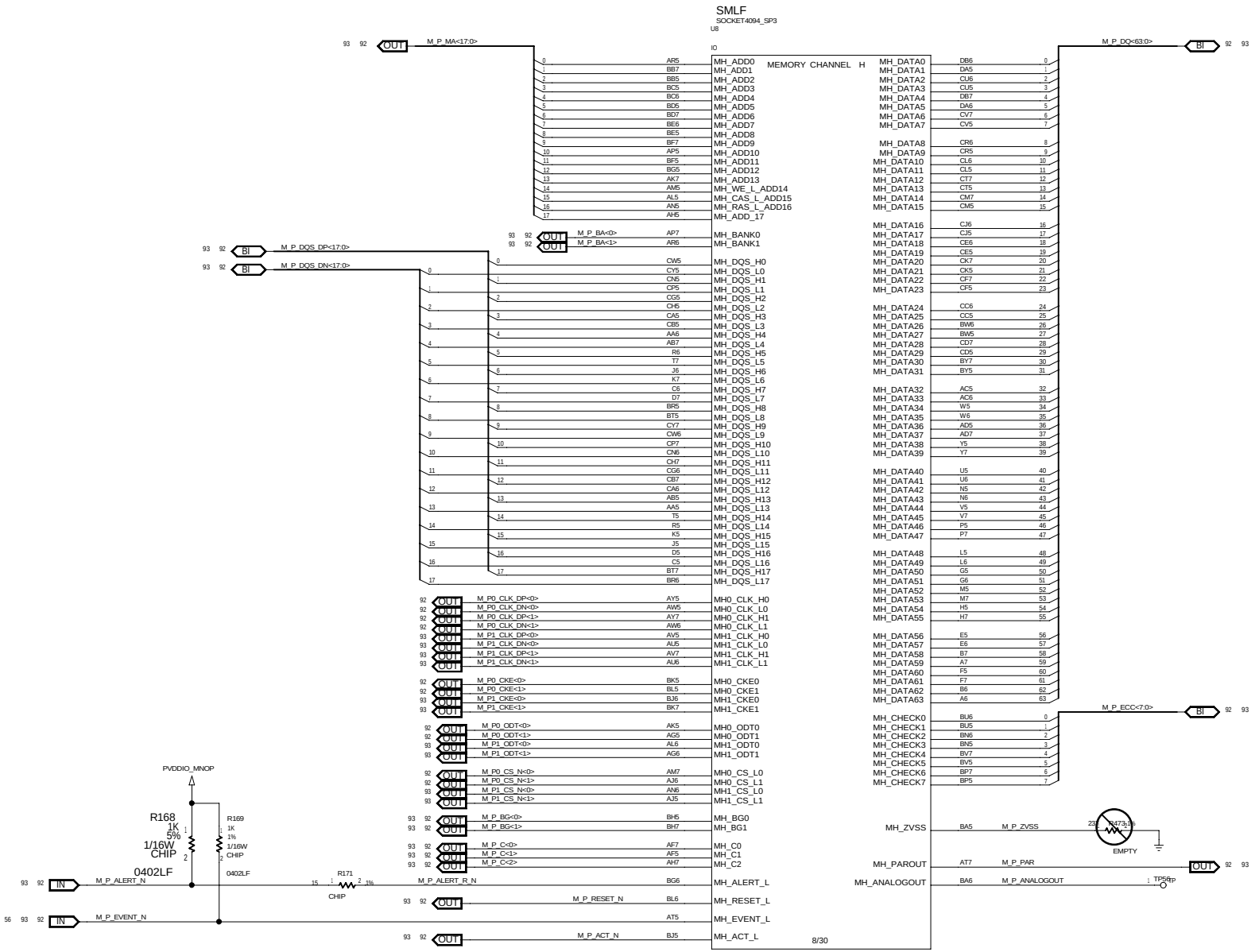
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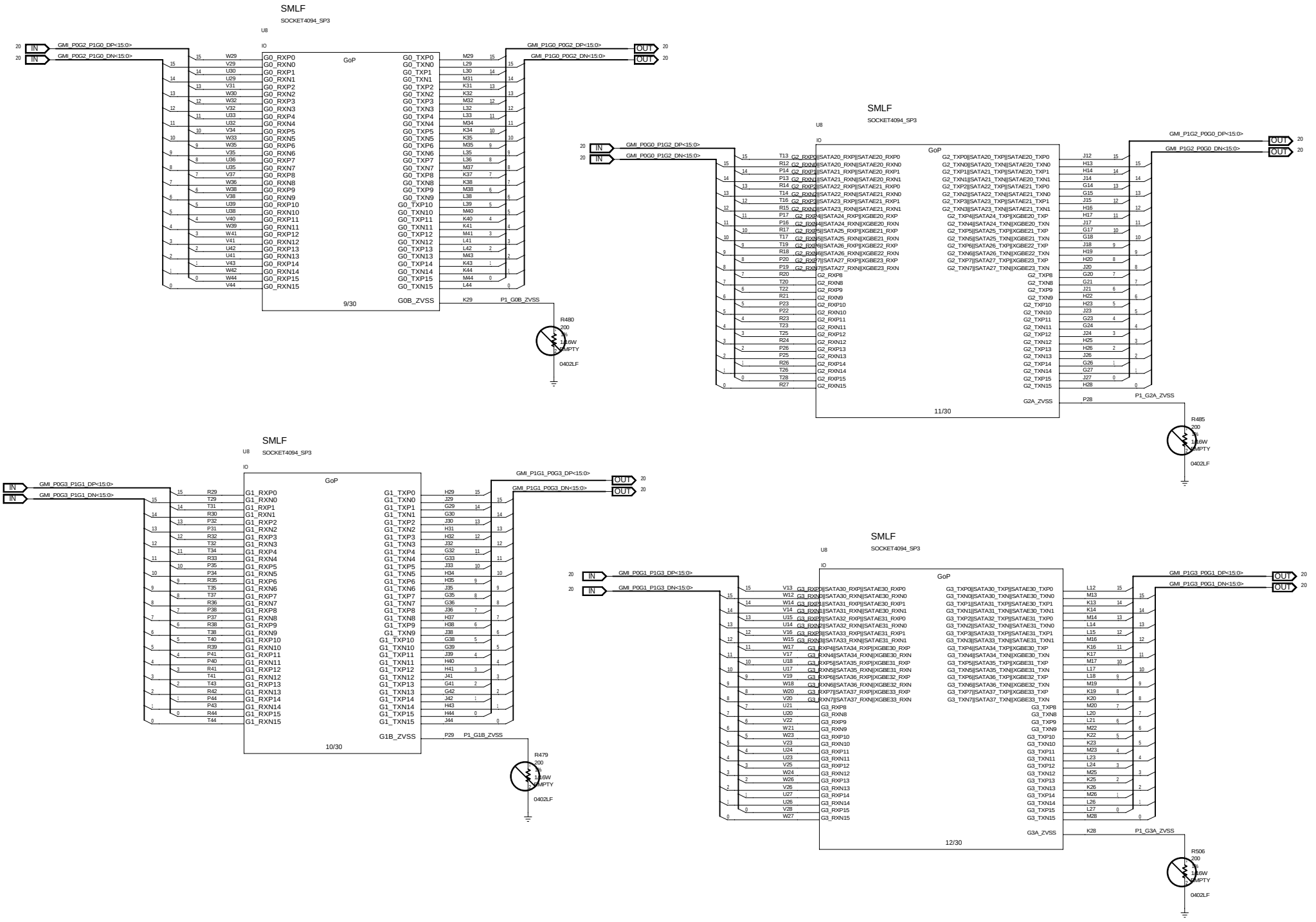
P1 MEMORY CHN (6 OF 19)

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SMLF
SOCKET4094_SP3
U8
IO
MEMORY CHANNEL G
M_O_MA<17:0>
M_O_BA<0>
M_O_BA<1>
M_O_DQS_DP<17:0>
M_O_DQS_DN<17:0>
M_O_DQ<63:0>
M_O_ECC<7:0>
M_O_CLK_DP<0>
M_O_CLK_DN<0>
M_O_CLK_DP<1>
M_O_CLK_DN<1>
M_O_CKE<0>
M_O_CKE<1>
M_O_ODT<0>
M_O_ODT<1>
M_O_CS_N<0>
M_O_CS_N<1>
M_O_BG<0>
M_O_BG<1>
M_O_C<0>
M_O_C<1>
M_O_C<2>
M_O_ALERT_N
M_O_EVENT_N
M_O_RESET_N
M_O_ACT_N
M_O_ZVSS
M_O_PAR
M_O_ANALOGOUT
MG_ADD0
MG_ADD1
MG_ADD2
MG_ADD3
MG_ADD4
MG_ADD5
MG_ADD6
MG_ADD7
MG_ADD8
MG_ADD9
MG_ADD10
MG_ADD11
MG_ADD12
MG_ADD13
MG_WE_L_ADD14
MG_CAS_L_ADD15
MG_RAS_L_ADD16
MG_ADD_17
MG_BANK0
MG_BANK1
MG_DQS_H0
MG_DQS_L0
MG_DQS_H1
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MG1_CLK_H1
MG1_CLK_L1
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MG1_CKE1
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MG0_ODT1
MG1_ODT0
MG1_ODT1
MG0_CS_L0
MG0_CS_L1
MG1_CS_L0
MG1_CS_L1
MG_BG0
MG_BG1
MG_C0
MG_C1
MG_C2
MG_ALERT_L
MG_RESET_L
MG_EVENT_L
MG_ACT_L
MG_ZVSS
MG_PAROUT
MG_ANALOGOUT
MG_DATA0
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MG_DATA2
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MG_DATA63
MG_CHECK0
MG_CHECK1
MG_CHECK2
MG_CHECK3
MG_CHECK4
MG_CHECK5
MG_CHECK6
MG_CHECK7
7/30
PVDDIO_MNOP
R113
1K
5%
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CHIP
R468
EMPTY
TP55

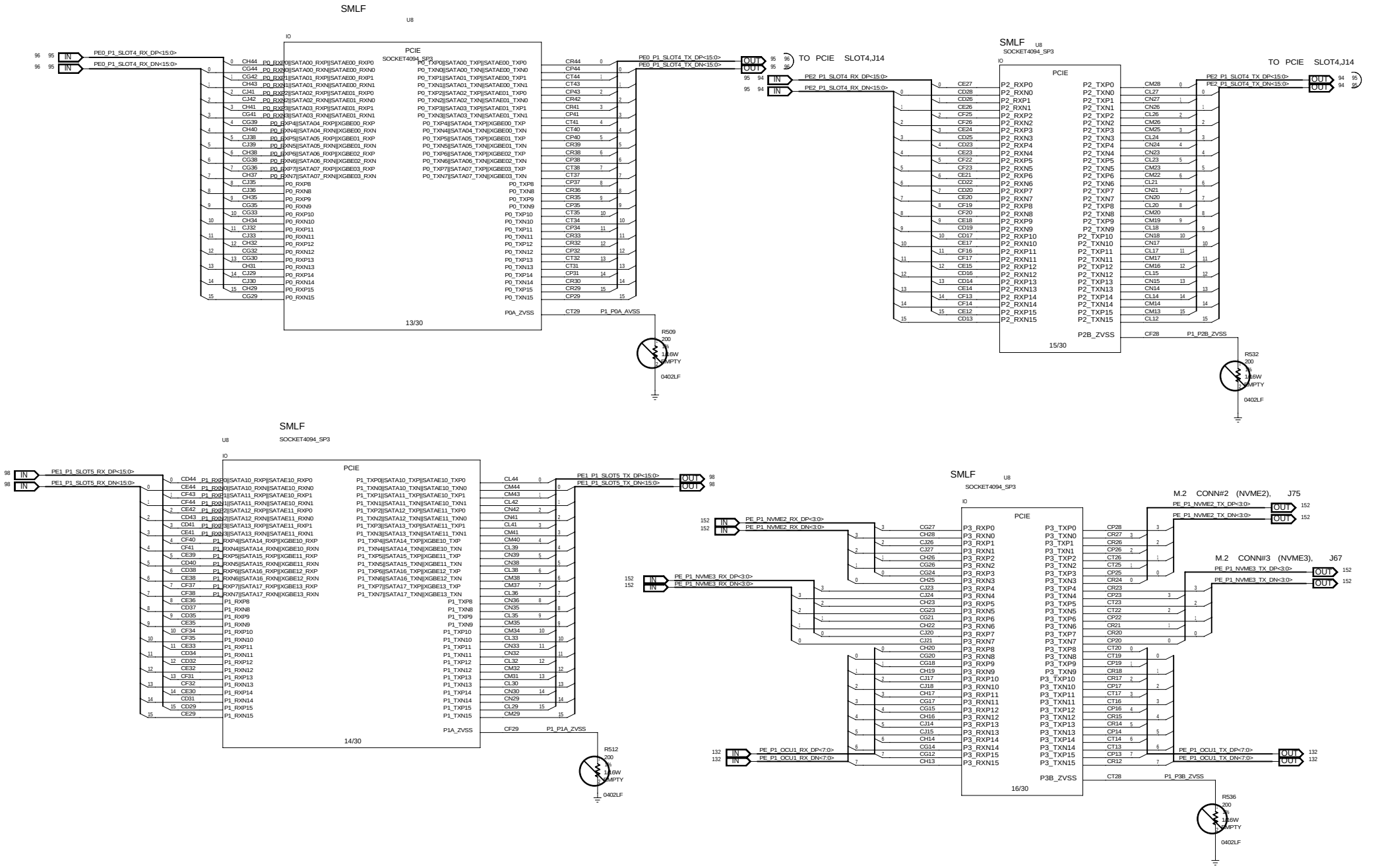


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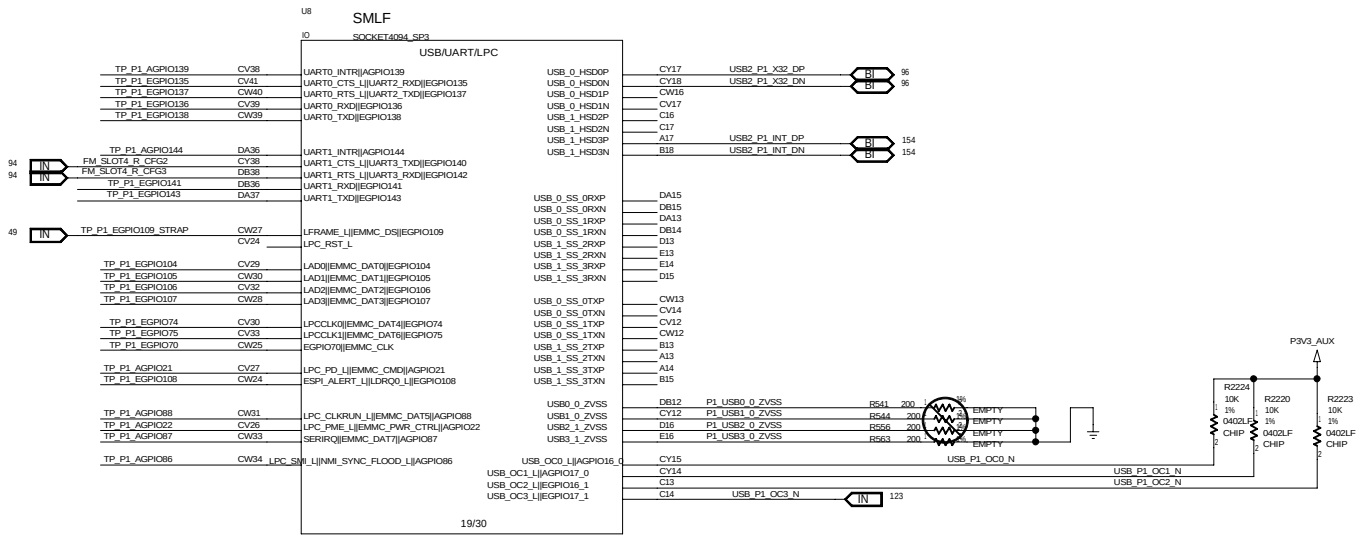
P1 xGMI (9 OF 19)

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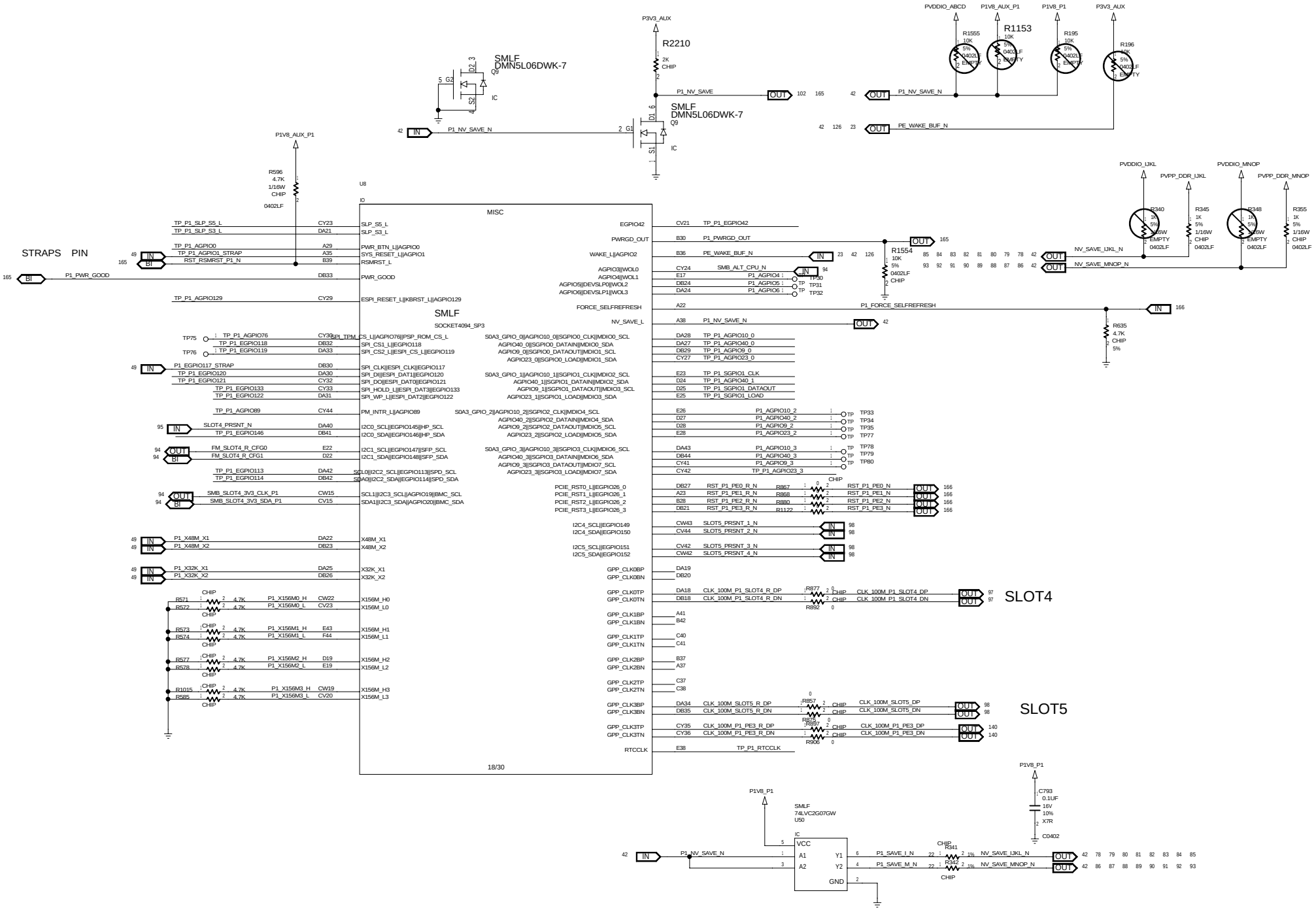
P1 PCIE & SATA (10 OF 19)

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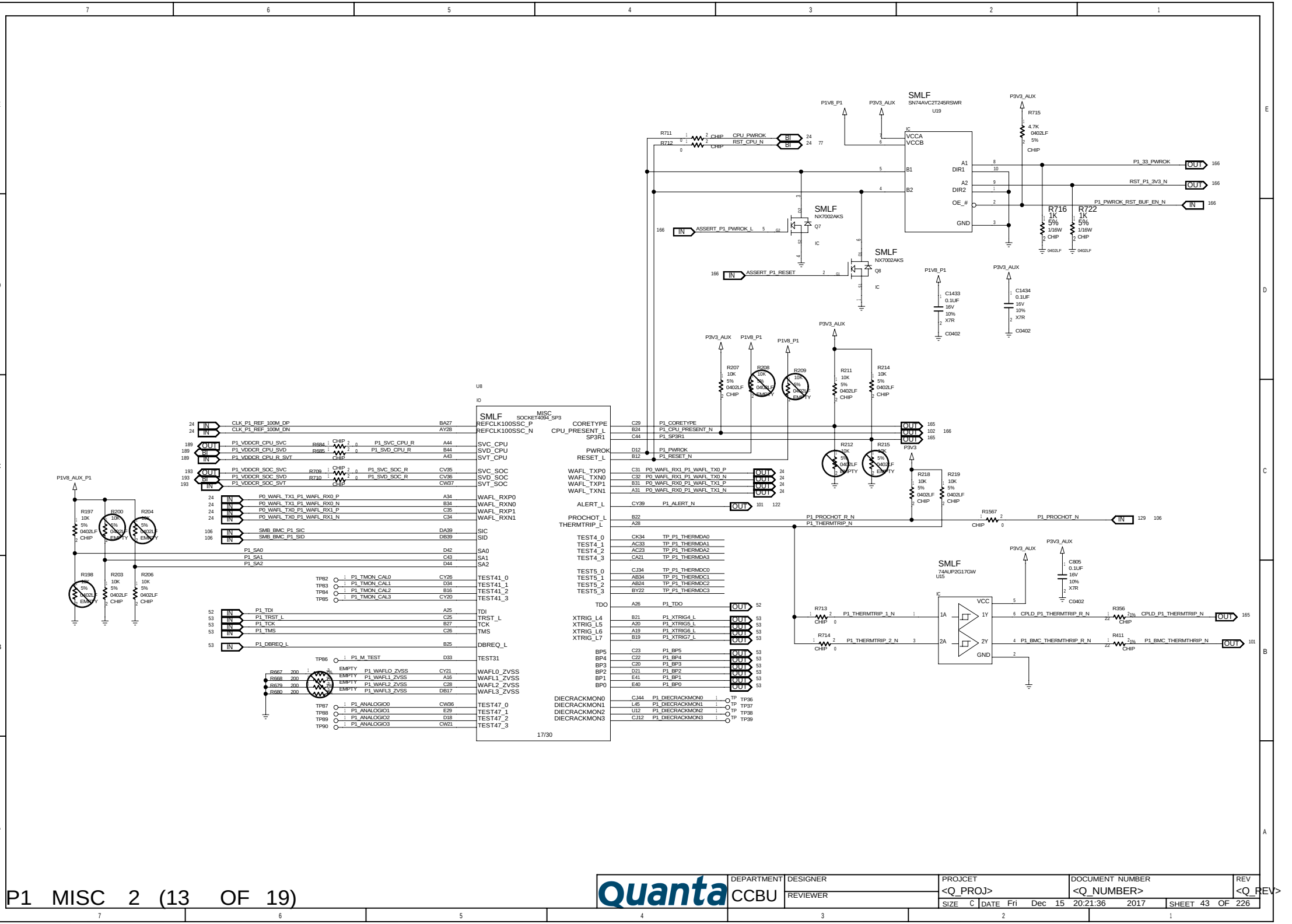


P1 USB, LPC & UART (11 OF 19)

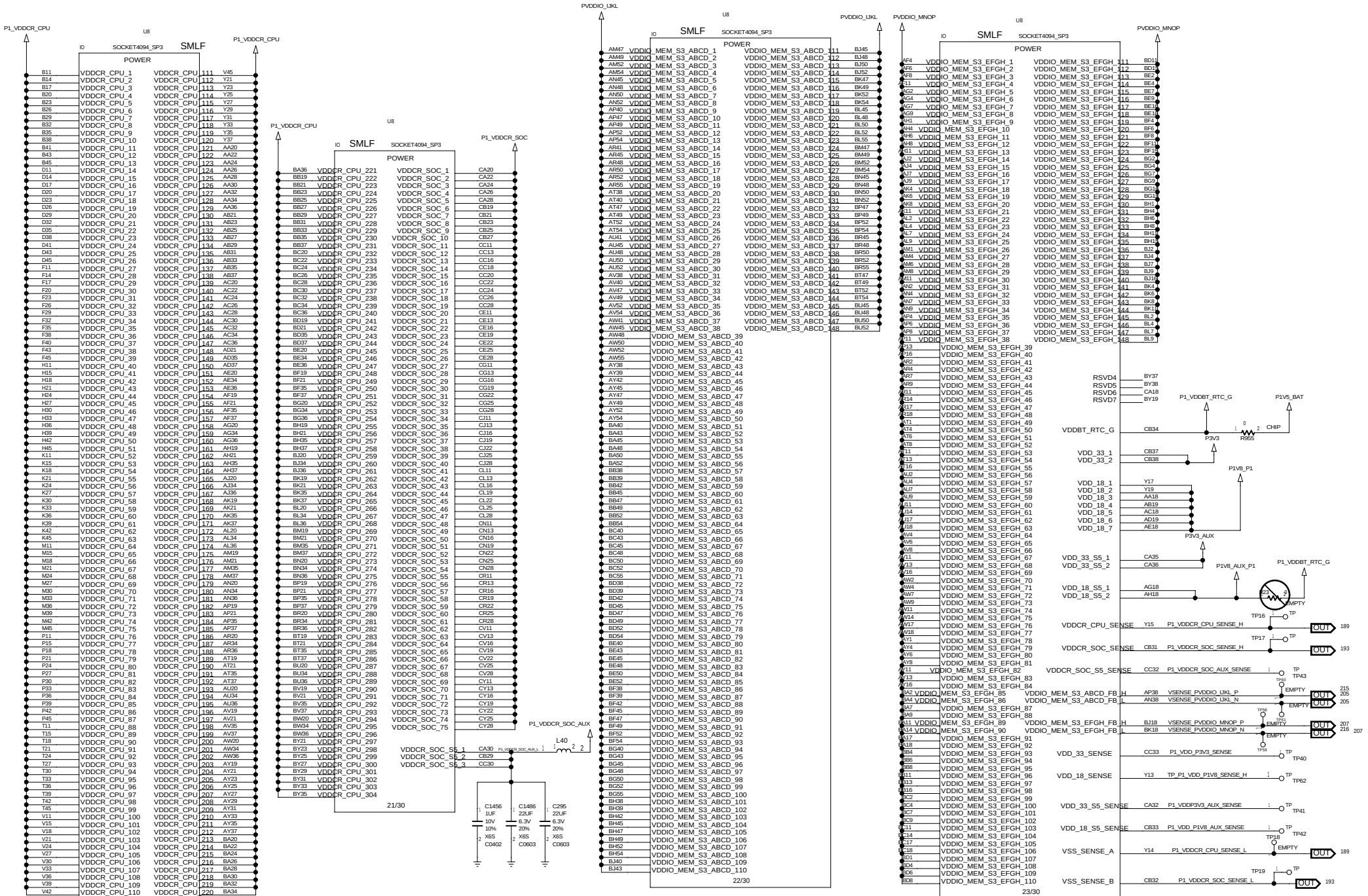
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			SIZE: C	DATE: Fri Dec 15 20:21:35 2017
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Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
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			SHEET 42 OF 226

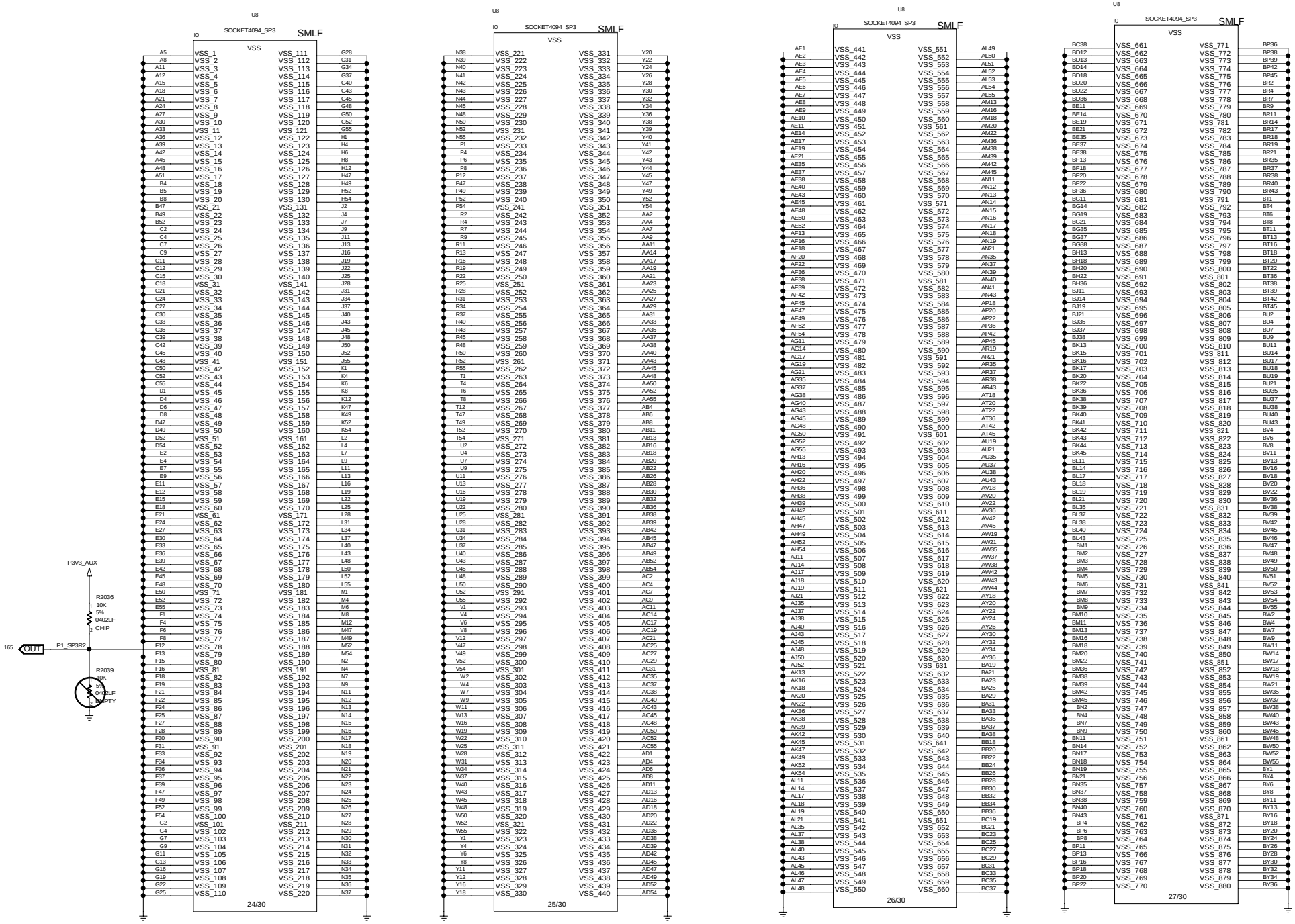


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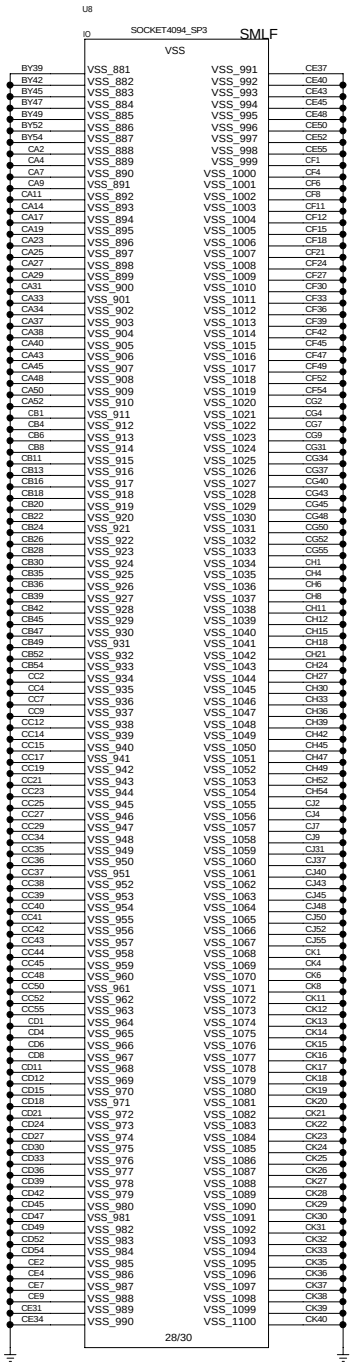


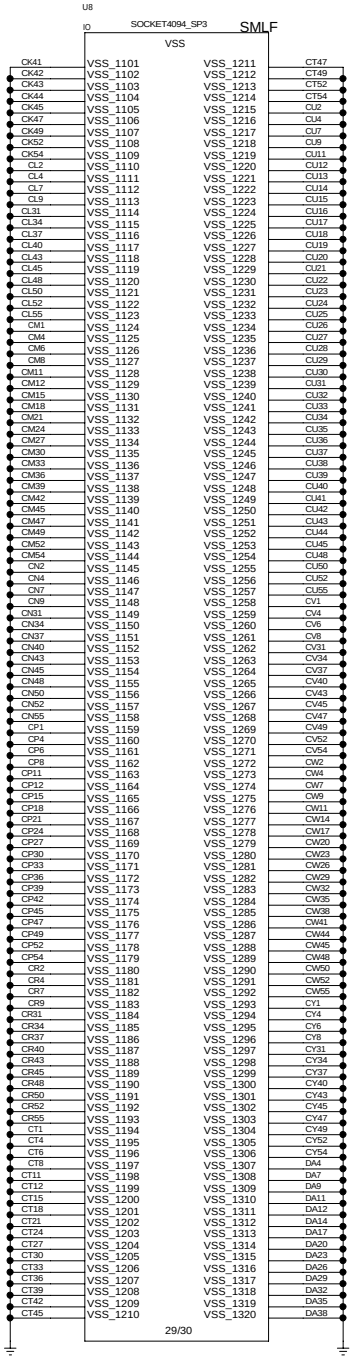
P1 POWER (14 OF 19)

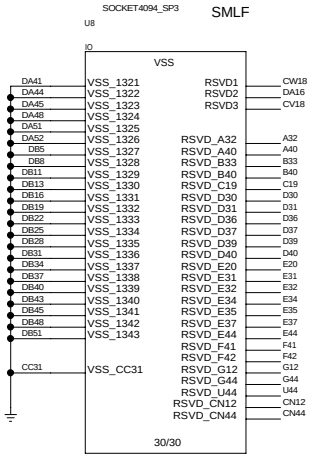
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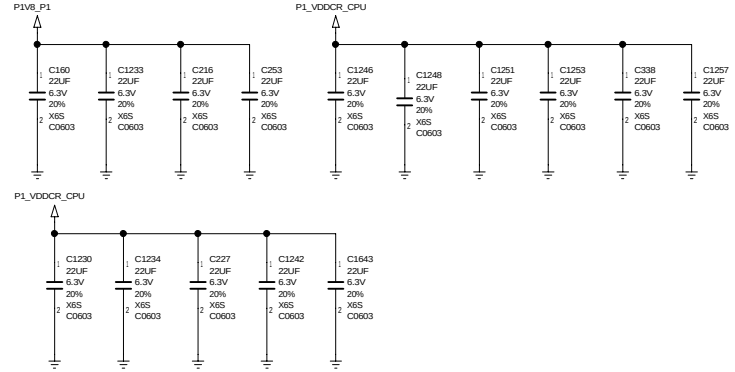


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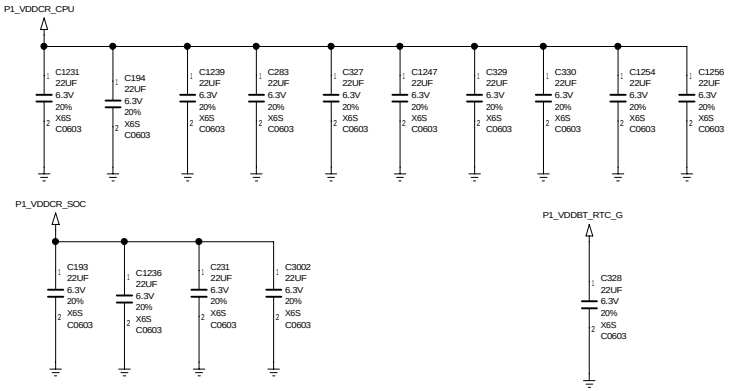
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VDDCR_CPU BOTTOM SIDE DECOUPLING

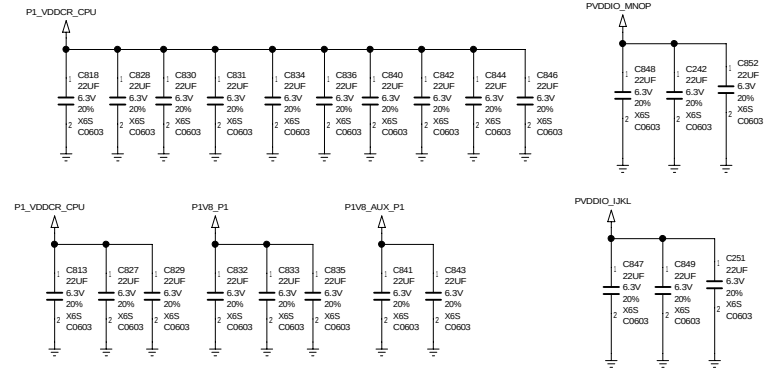
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- NORTH



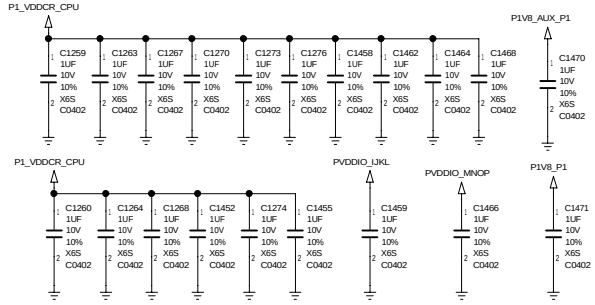
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- SOUTH



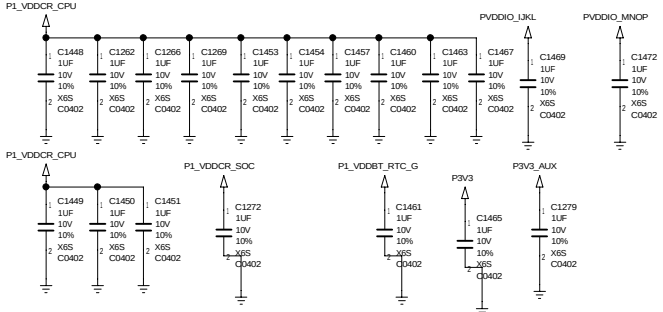
BOTTOM SIDE- NORTH



BOTTOM SIDE- NORTH

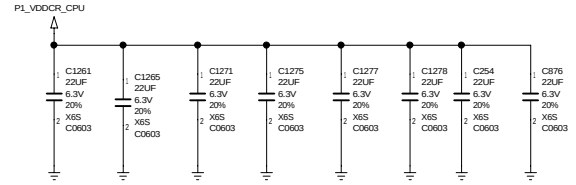


BOTTOM SIDE- SOUTH

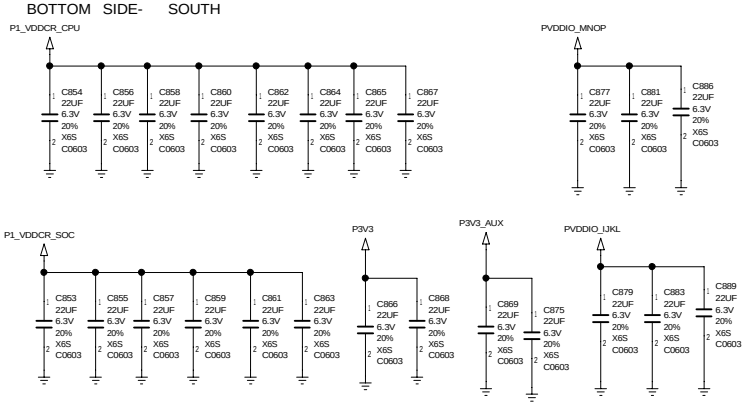


BOTTOM SIDE- IN THE SOCKET SPLIT REGIONS

OEM SKT ONLY: NOT AVAILABLE IN SLT;CAN BE USED FOR RESISTORS

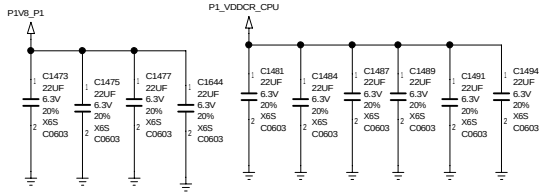


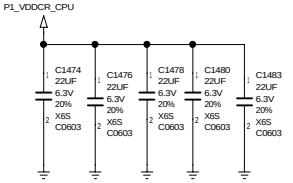
BOTTOM SIDE- SOUTH



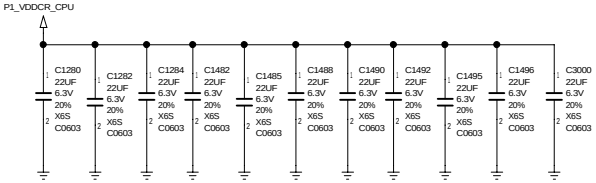
TOP SIDE DECOUPLING

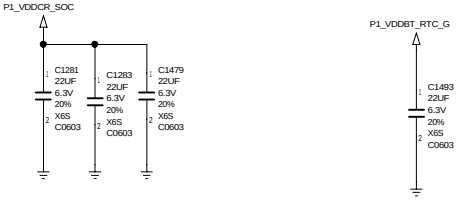
TOP CAVITY-NORTH DECOUPLING





TOP CAVITY SOUTH DECOUPLING





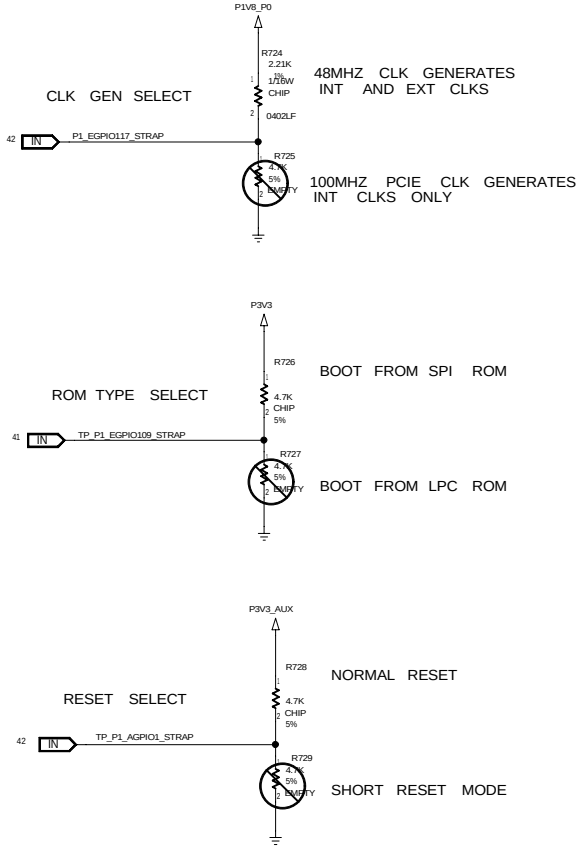
P1 DECOUPLING (17 OF 19)

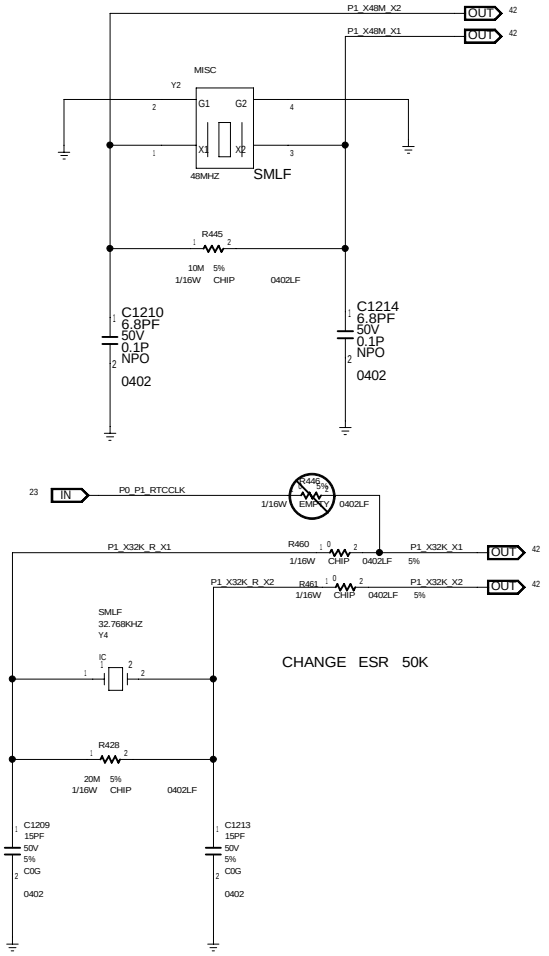
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		REVIEWER	SIZE C DATE Fri Dec 15 20:21:38 2017	SHEET 47 OF 226



Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>
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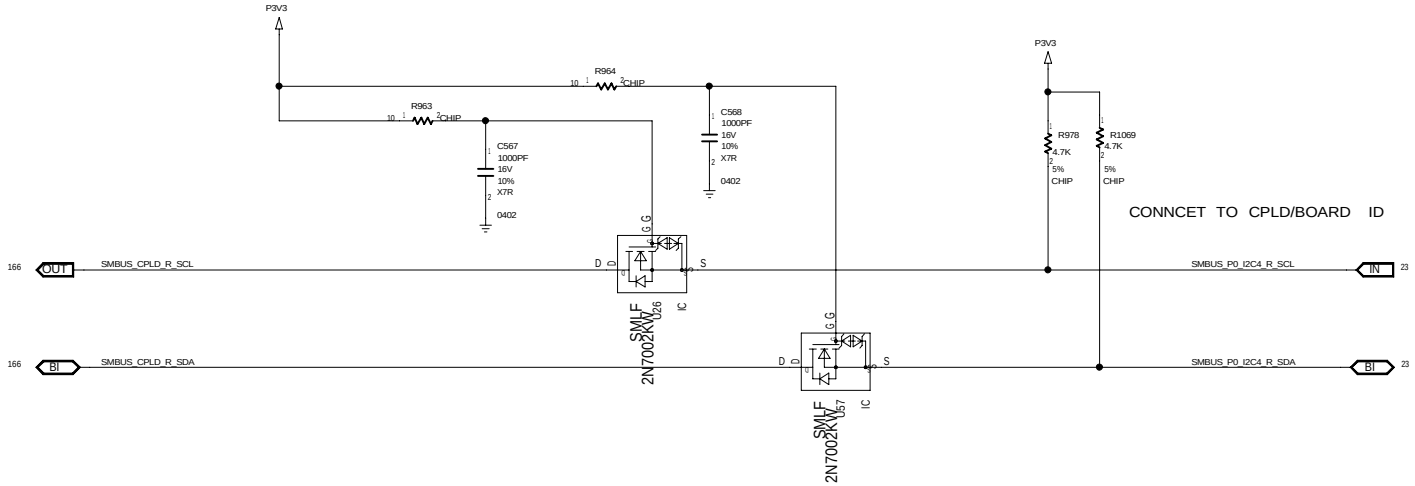
PROCESSOR STRAPS





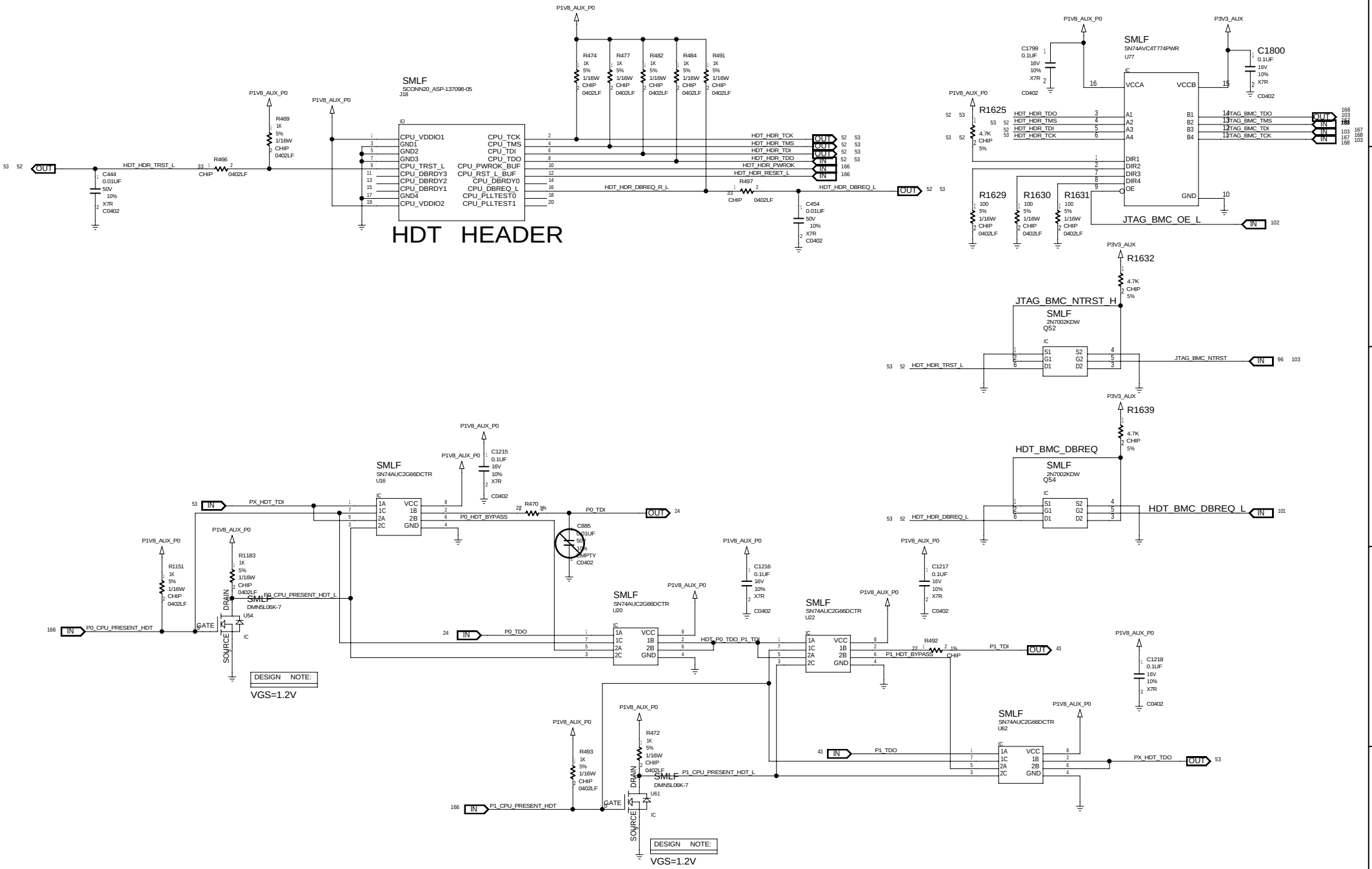
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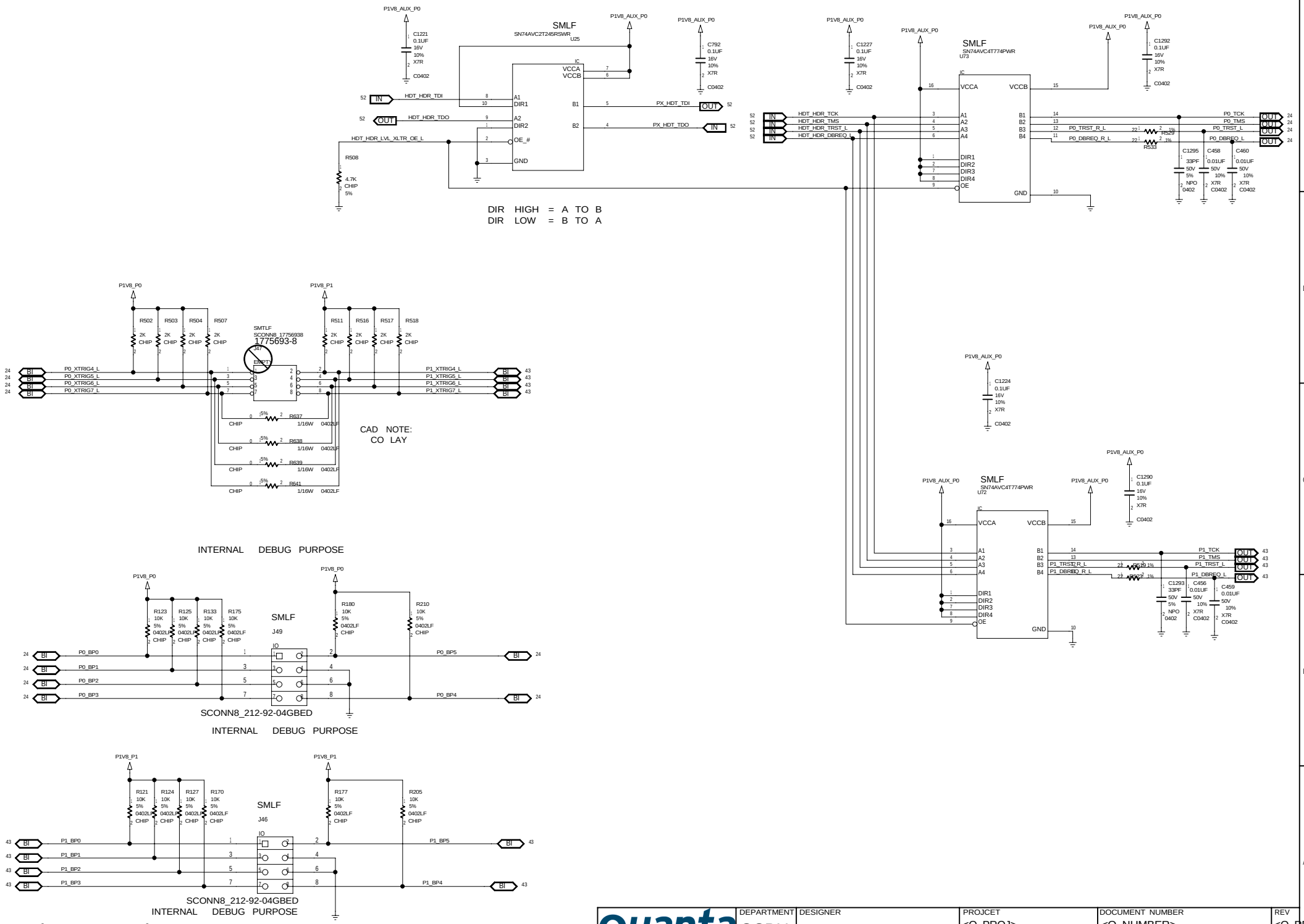
SMBUS ISOLATE for CPU0

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HDT (1 OF 2)

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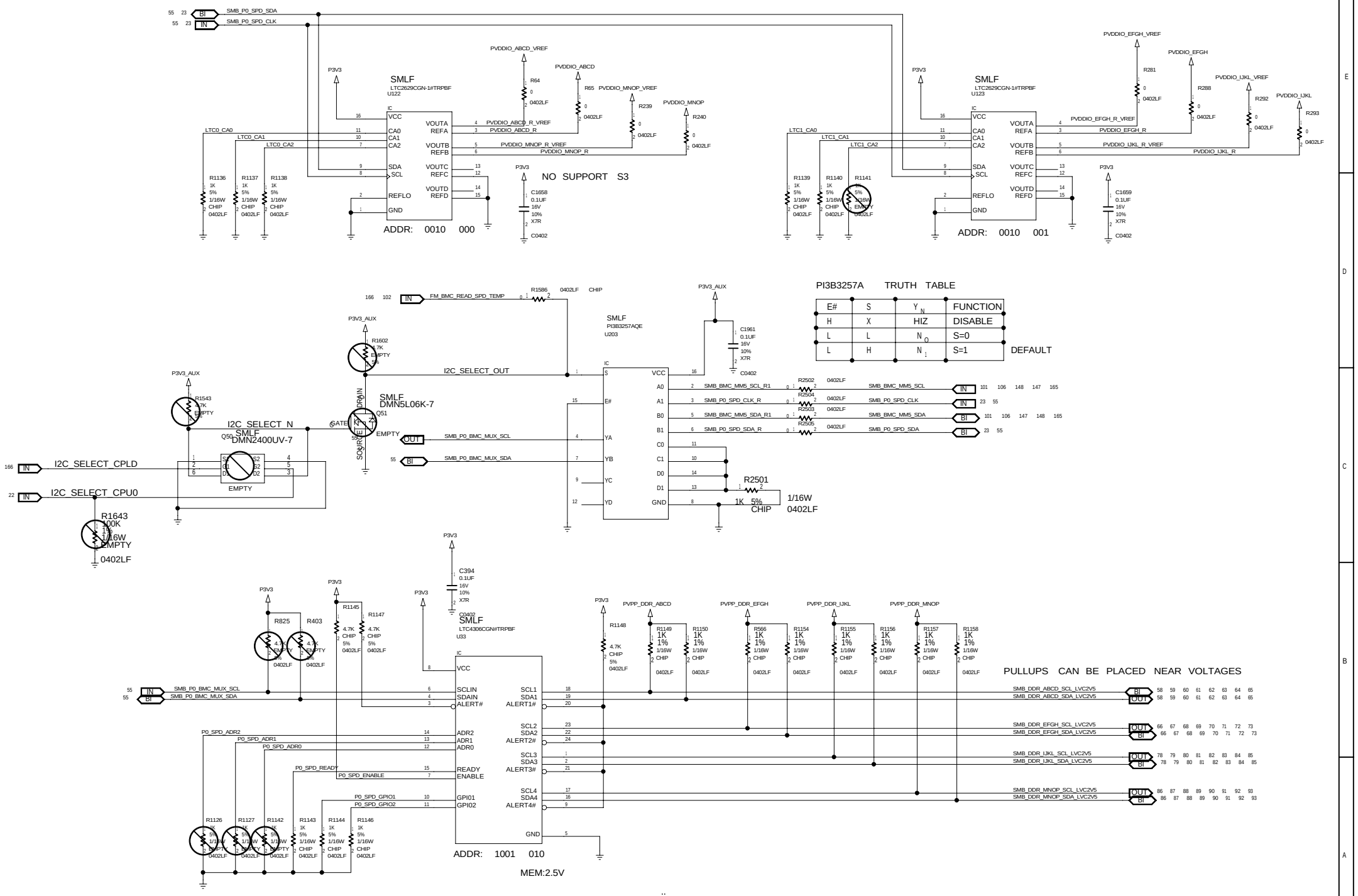


HDT (2 OF 2)

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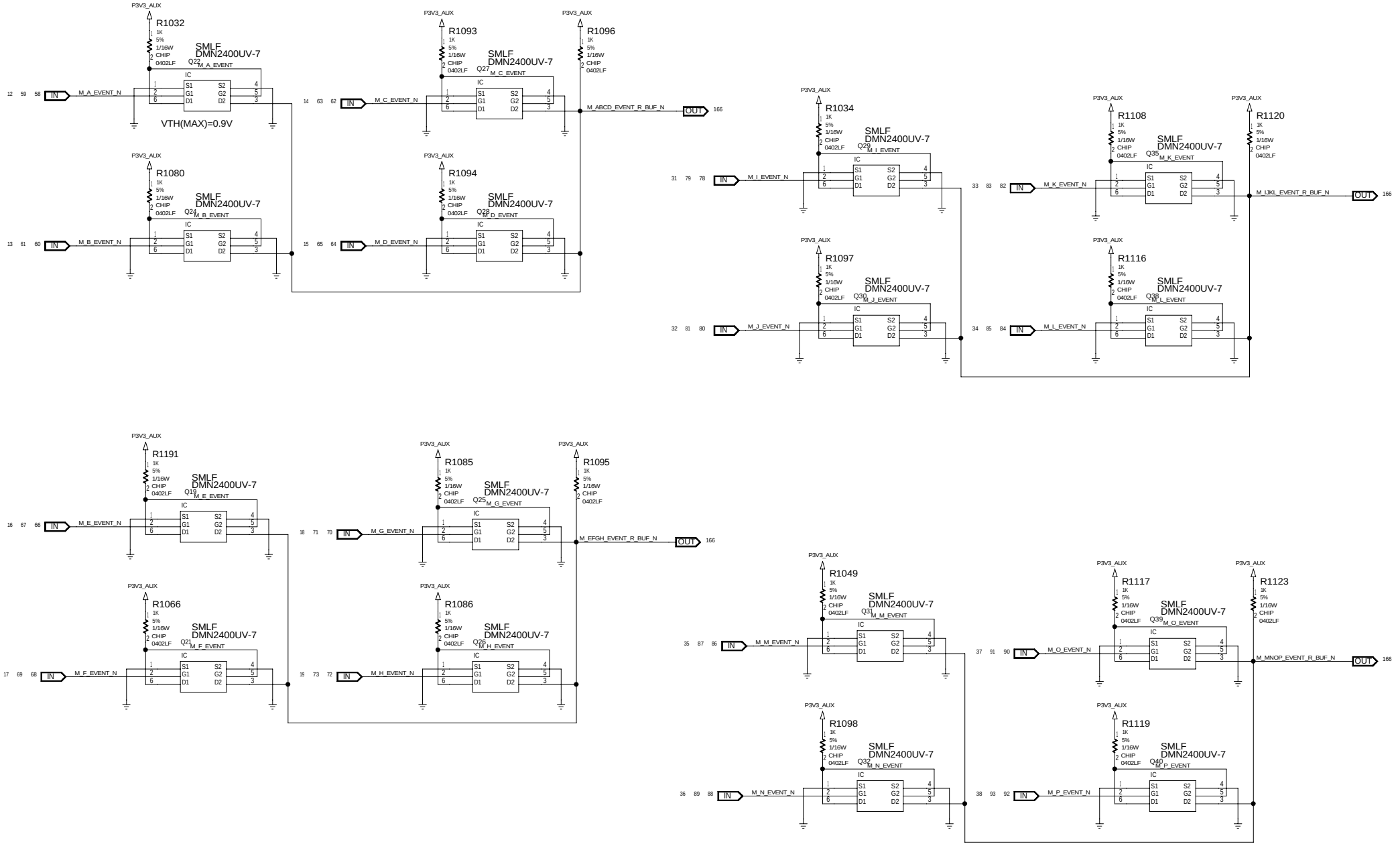
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DIMM SMBUS

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			SHEET 55 OF 226

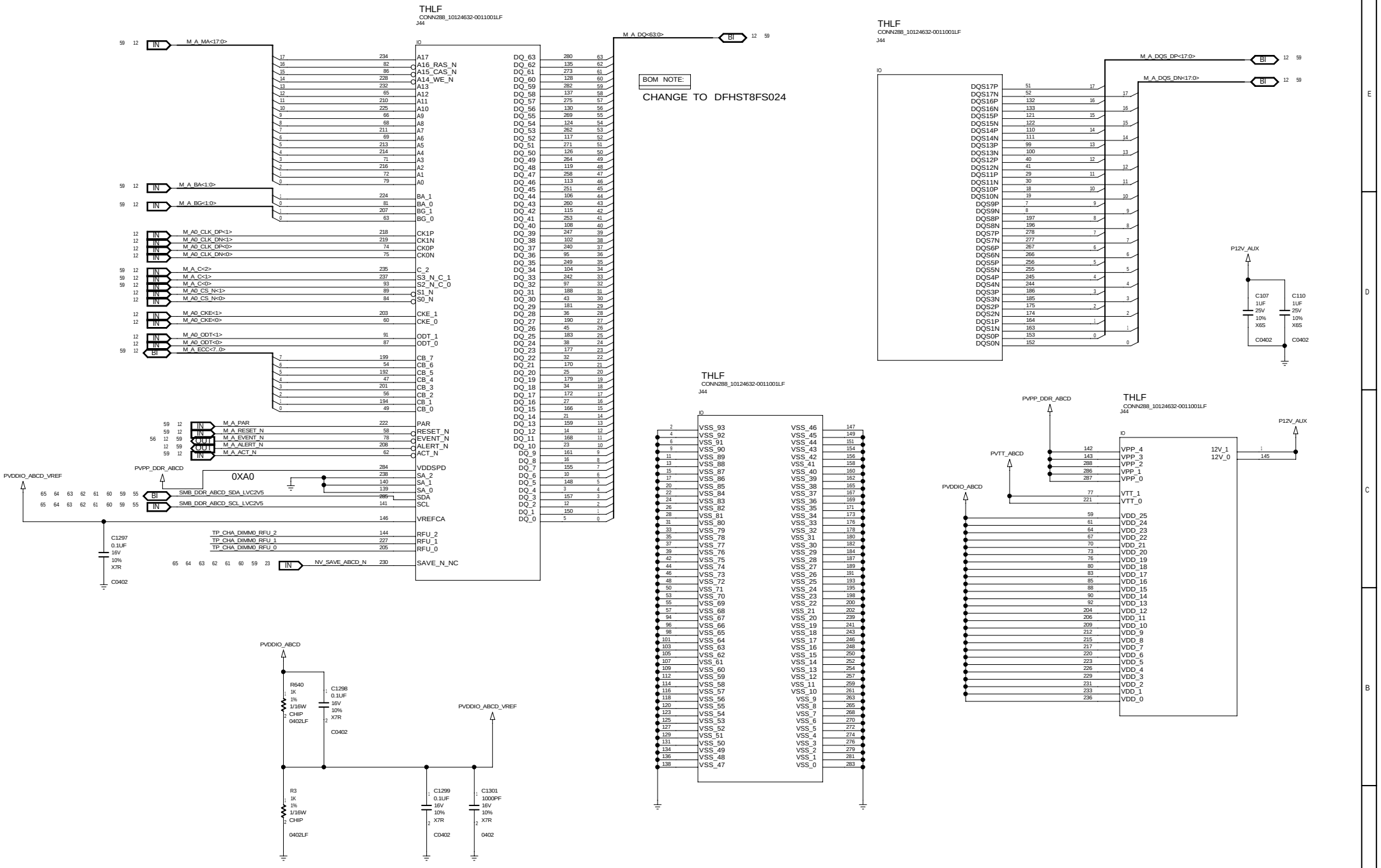


MEM_EVENT

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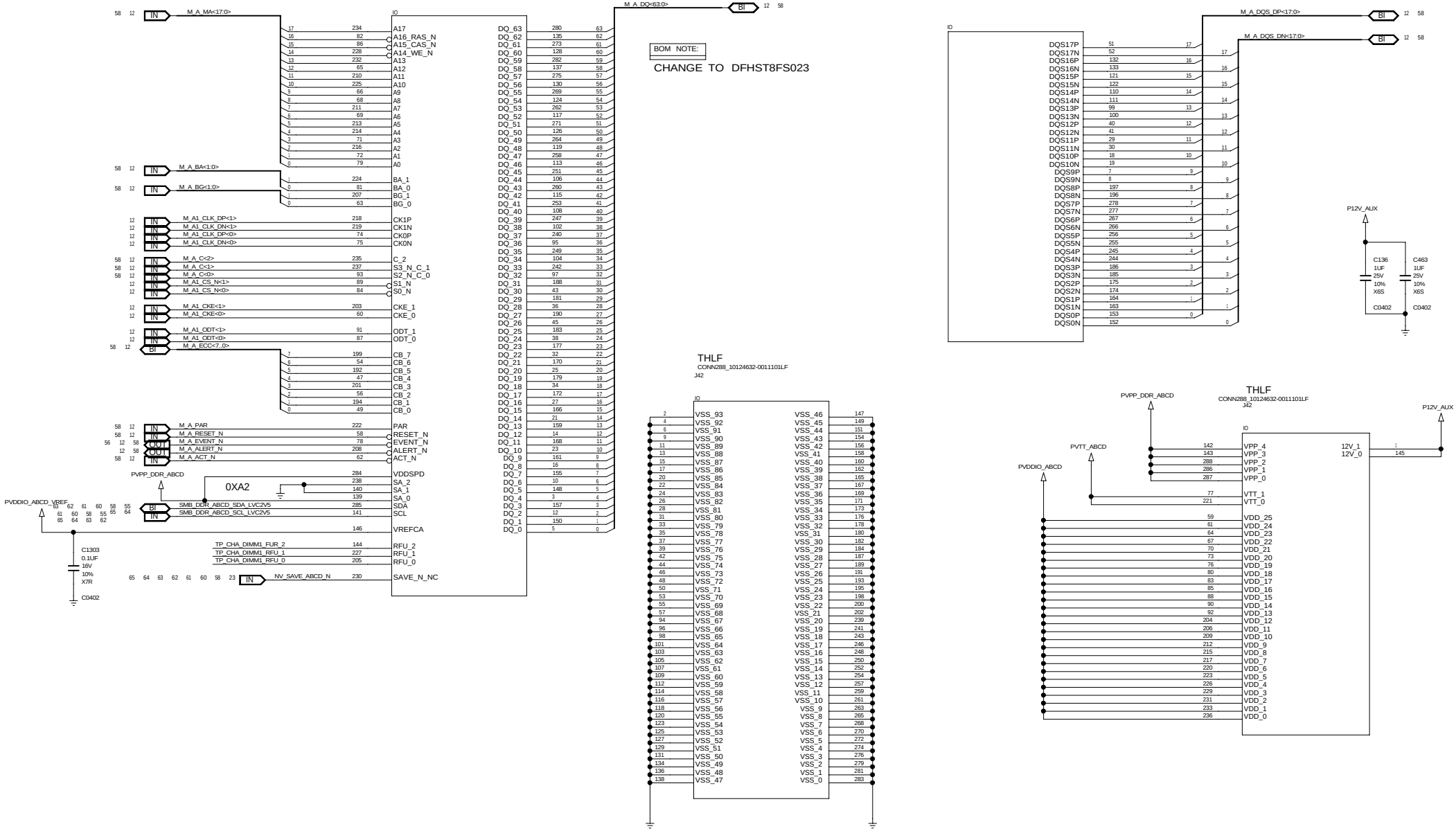
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LAYOUT: PLEASE NEAR DIMMS

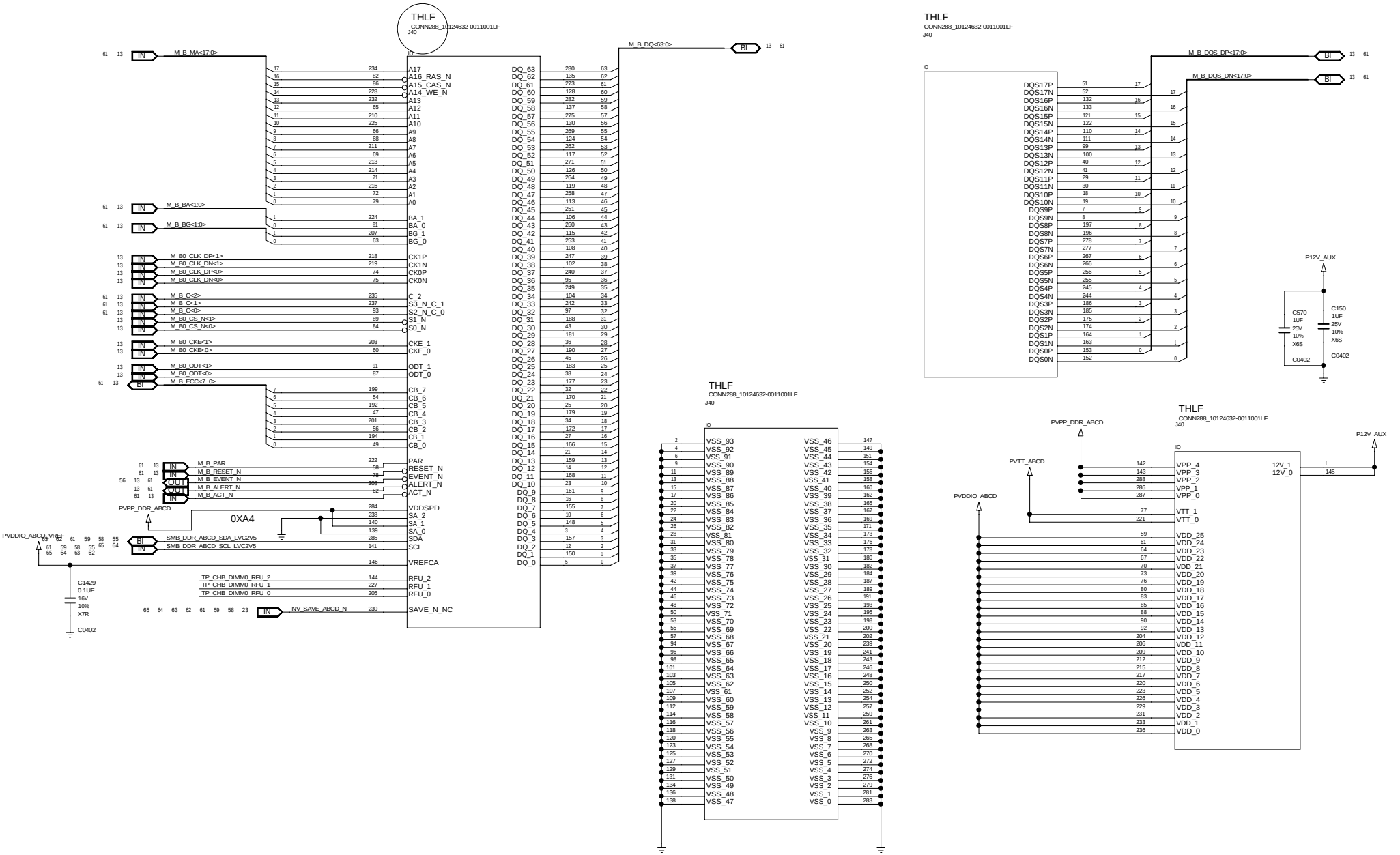
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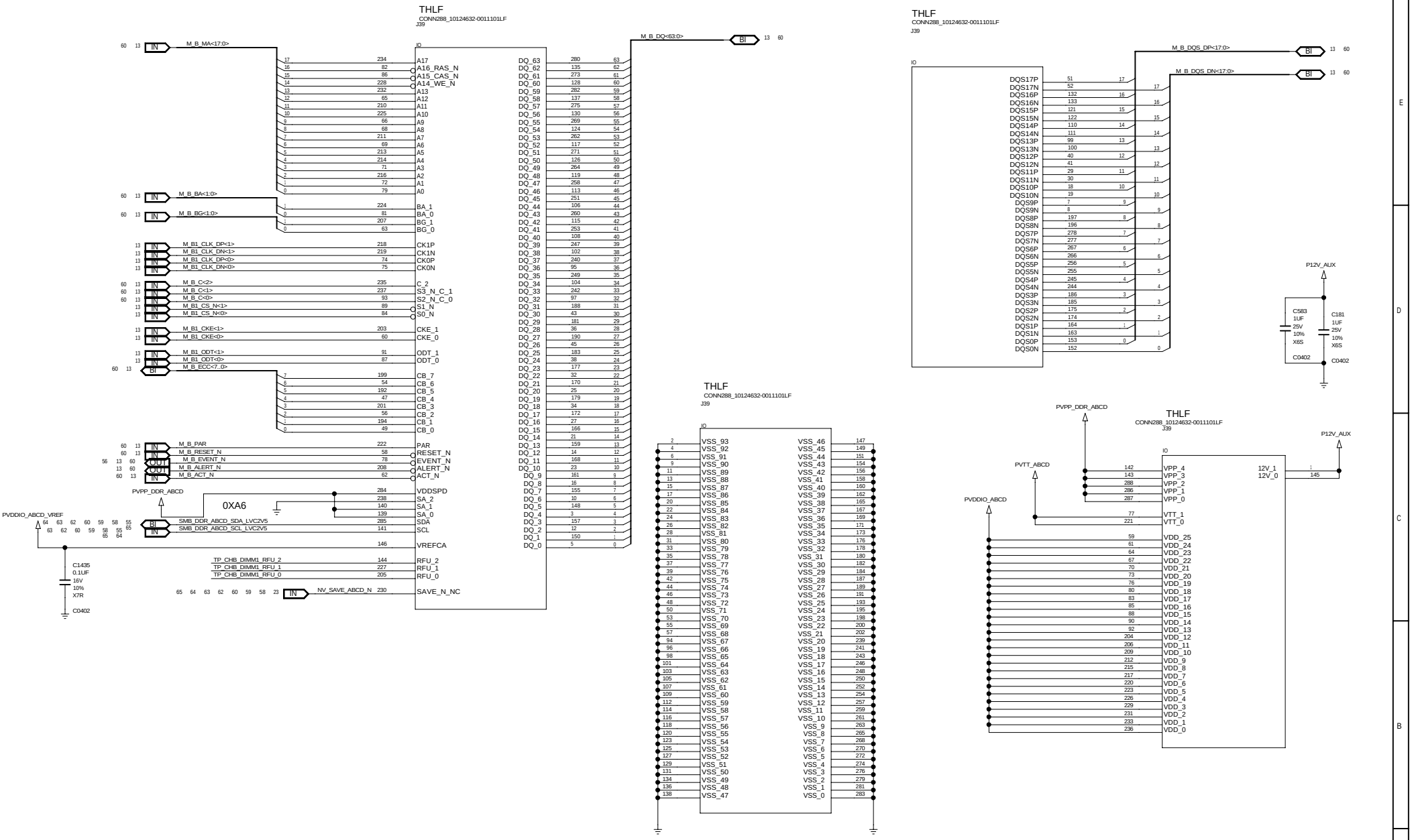
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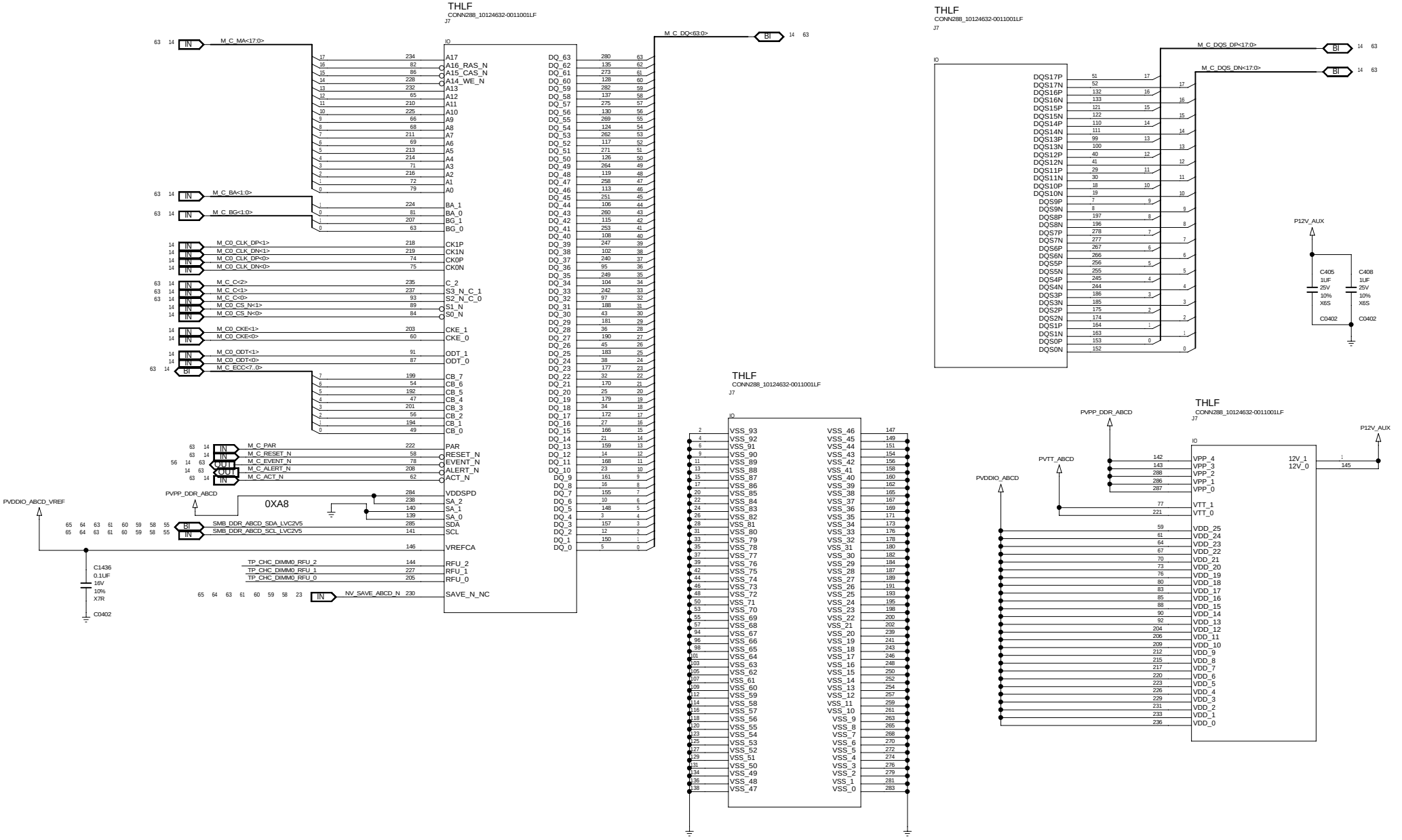
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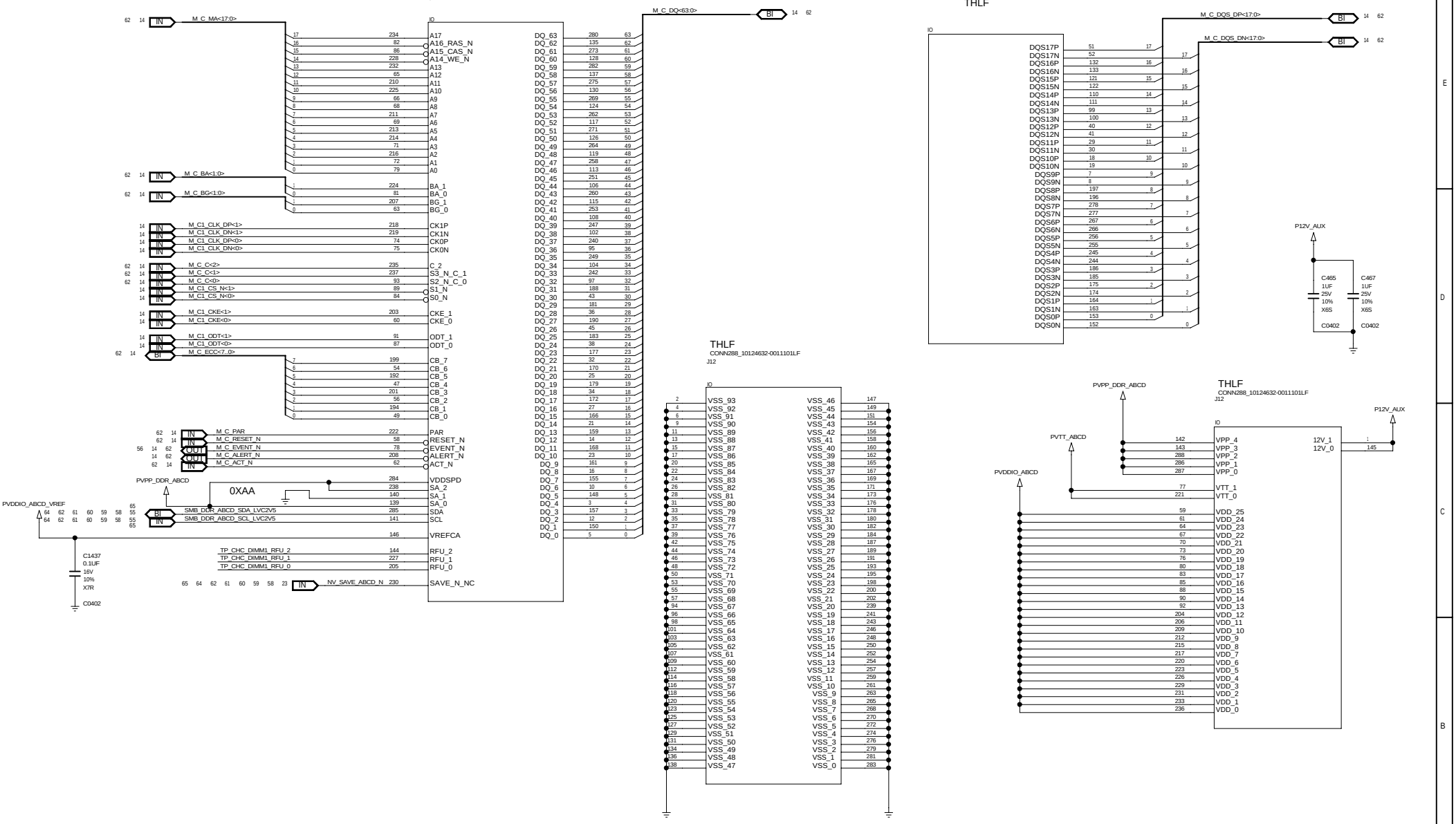
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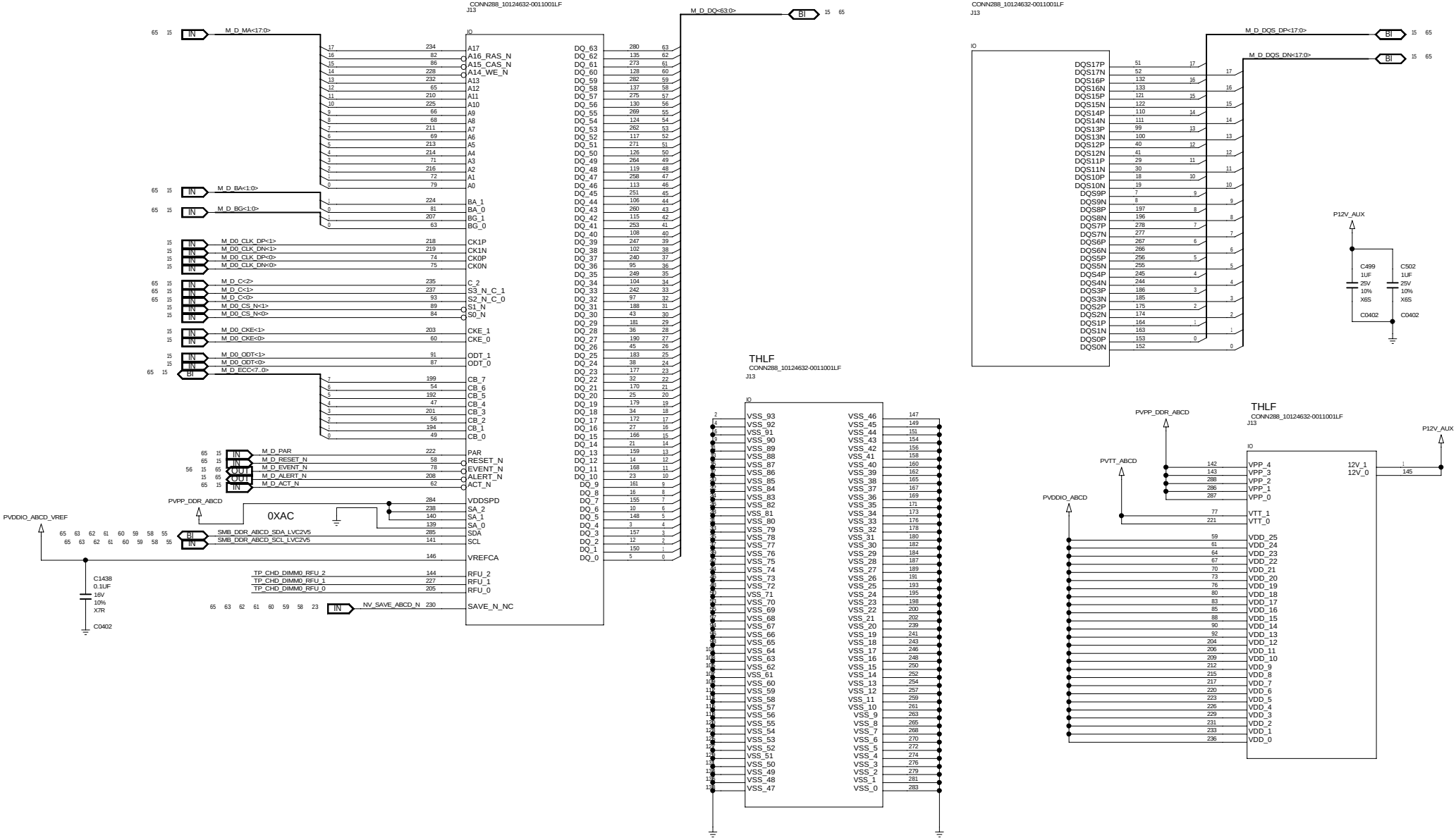
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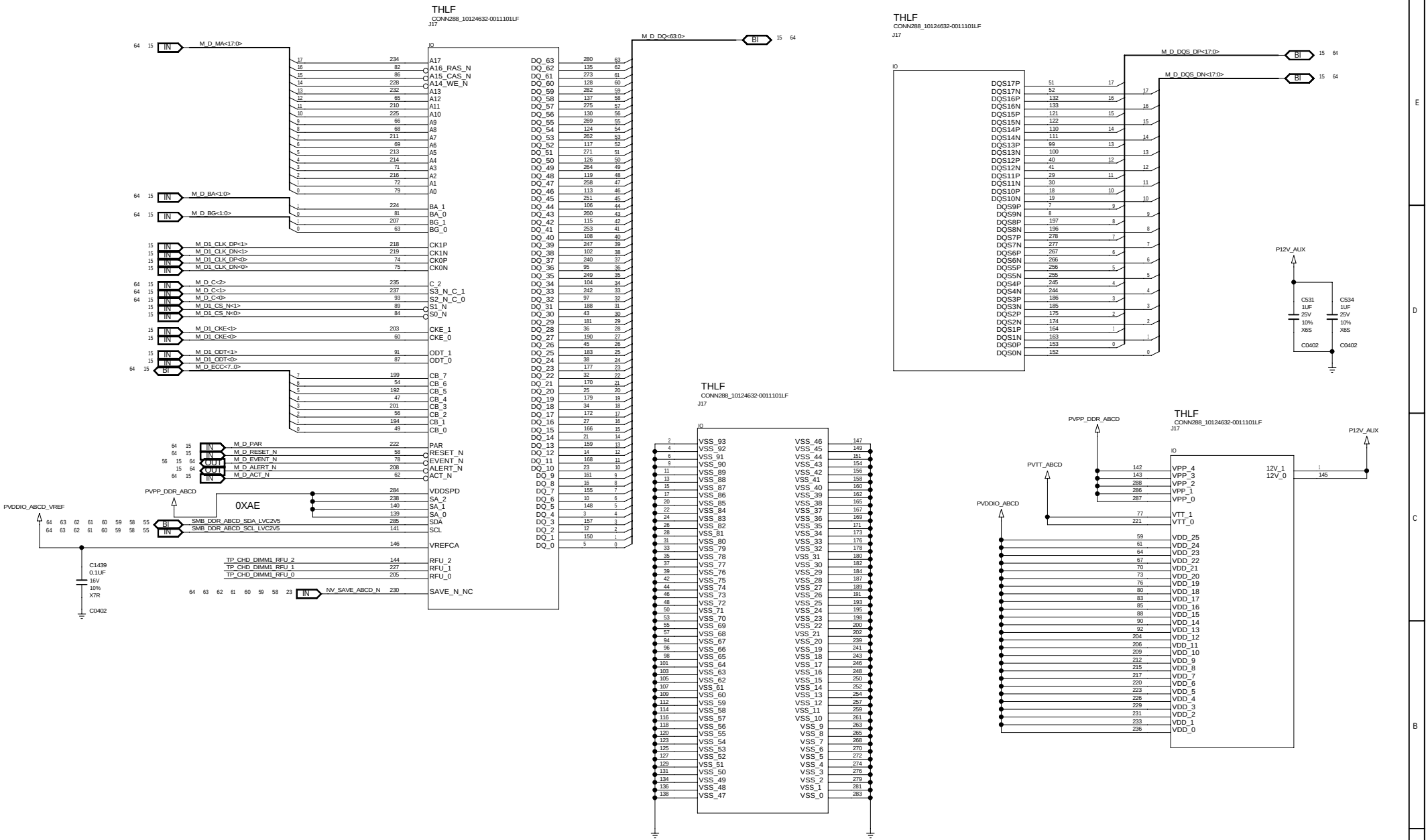
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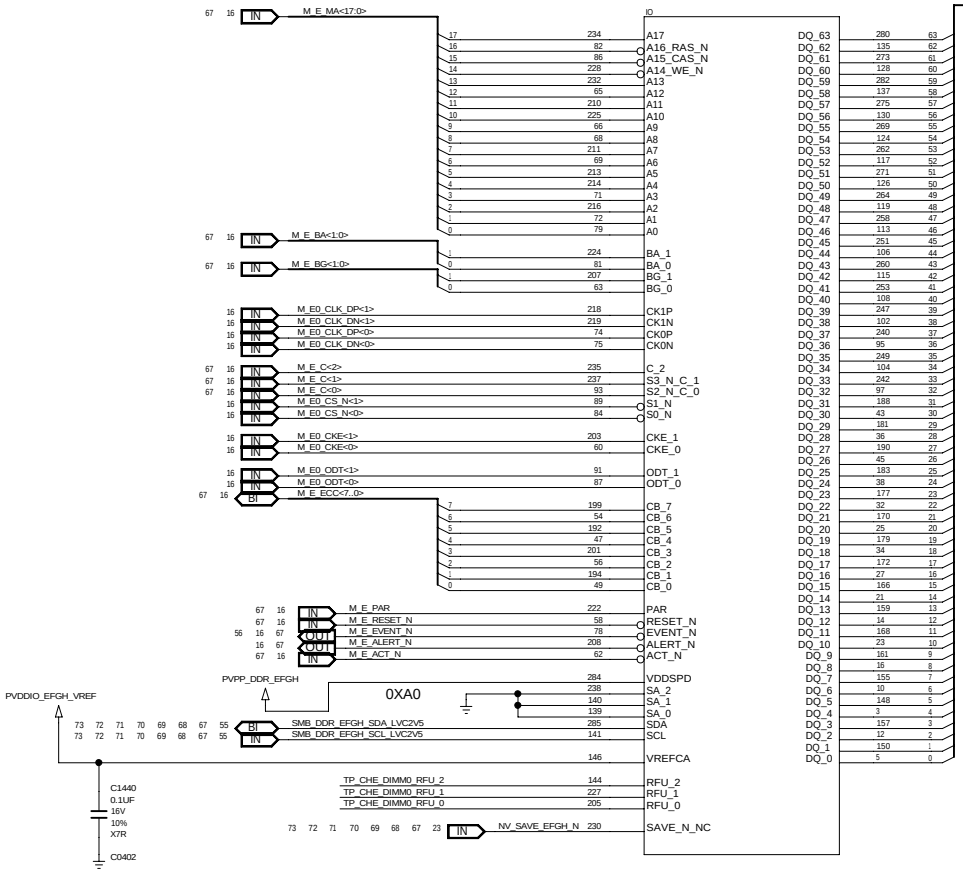
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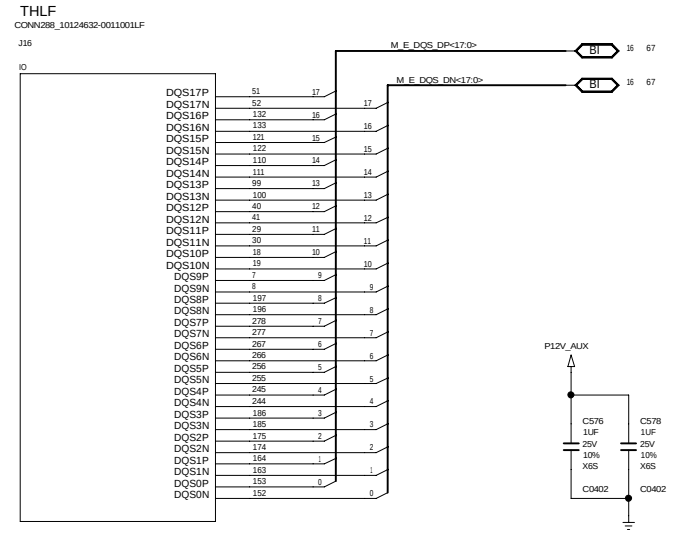
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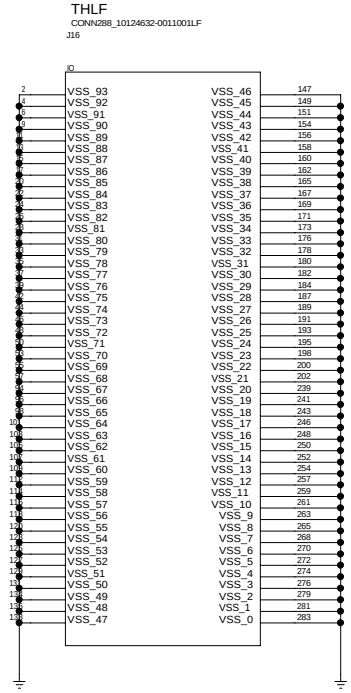


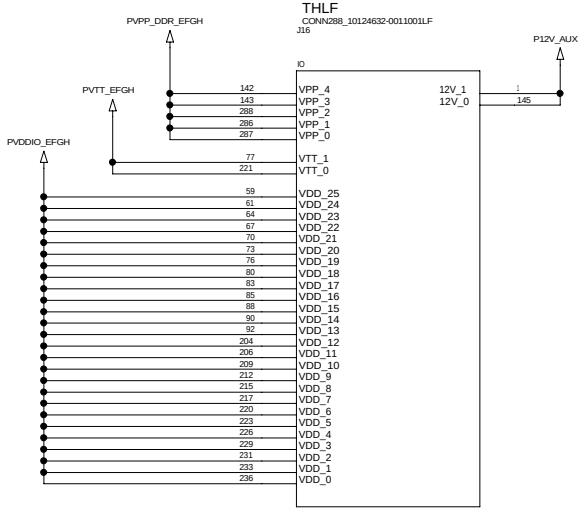
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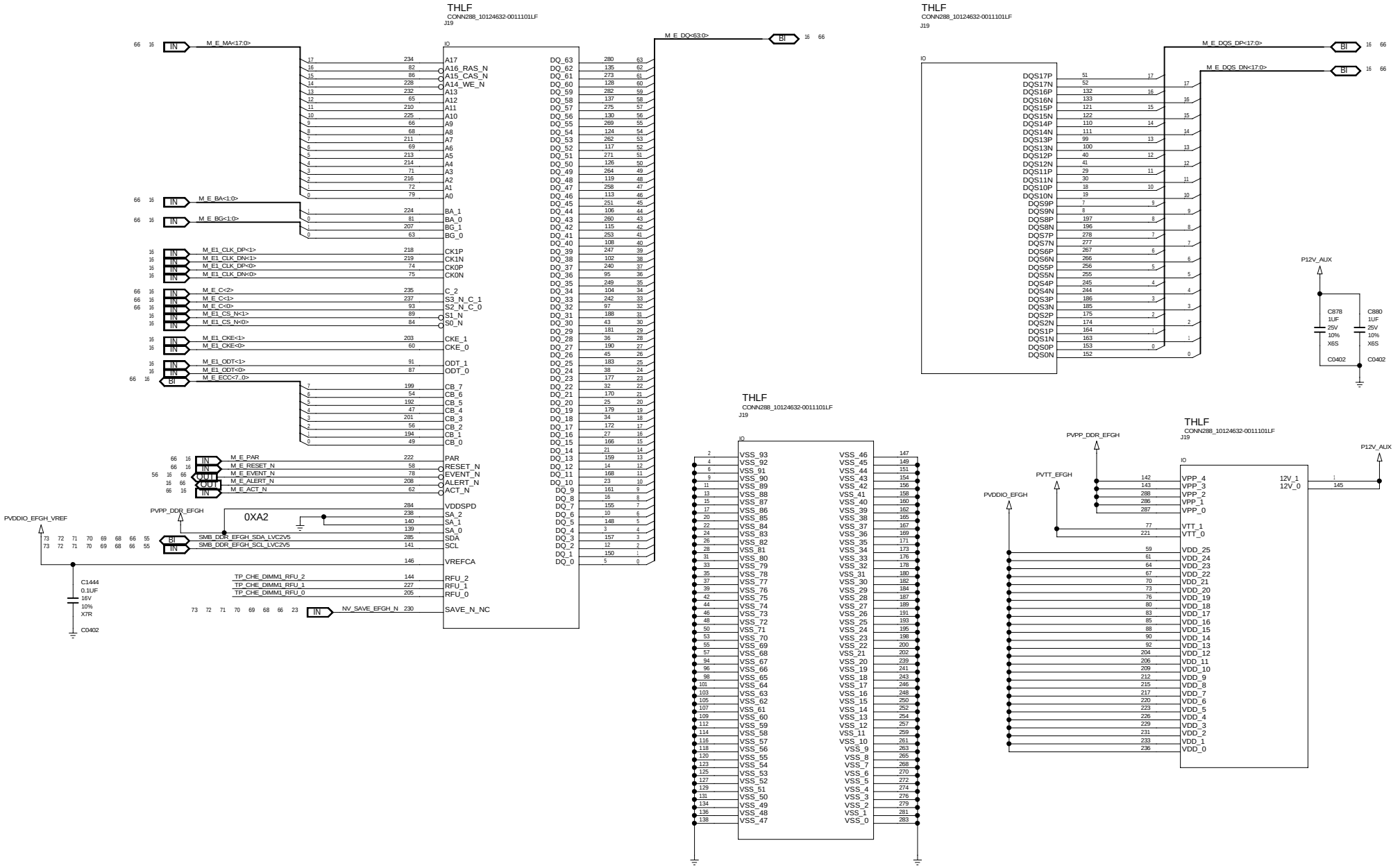






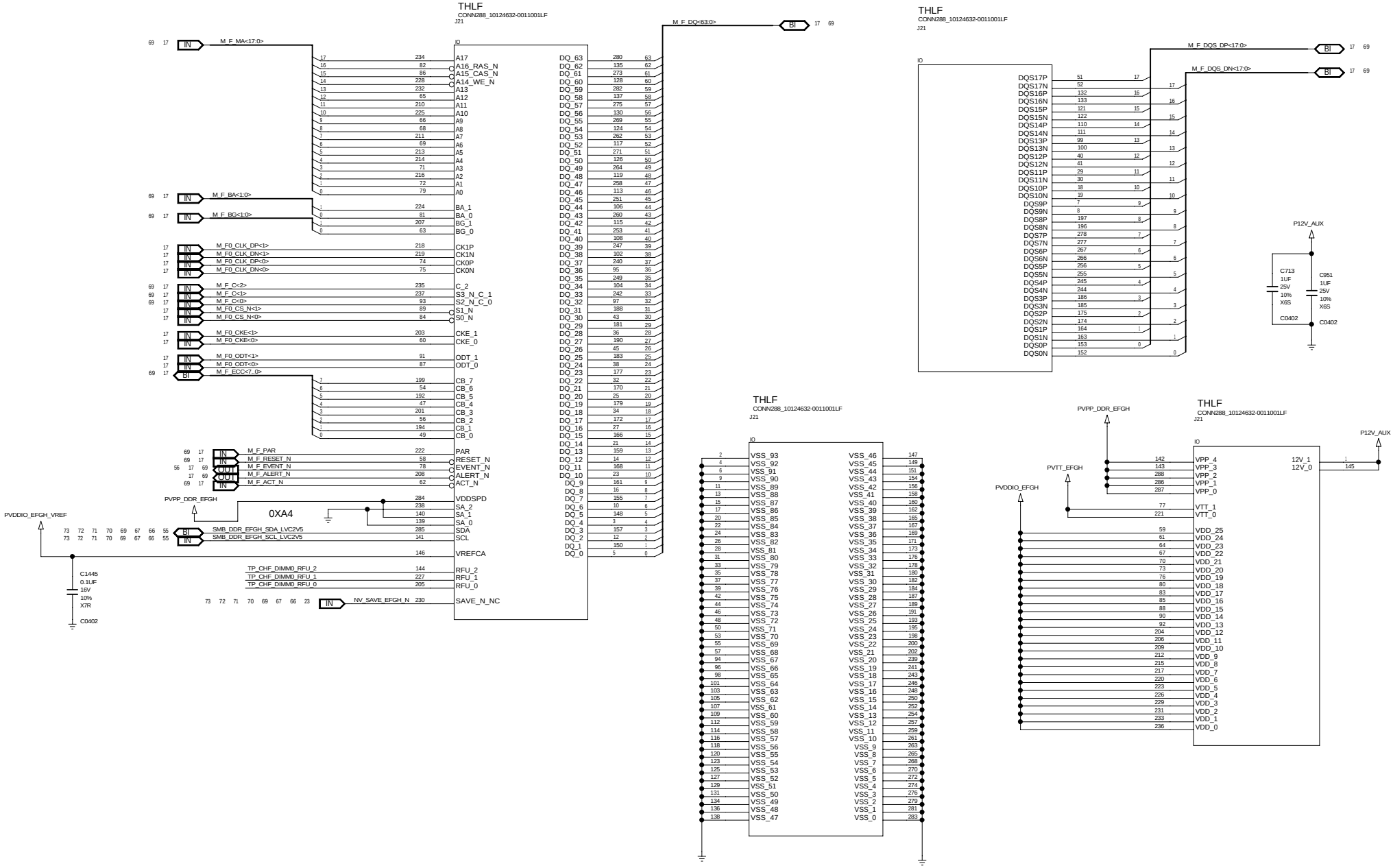
CPU0 DDR4 CH_E1(YELLOW)

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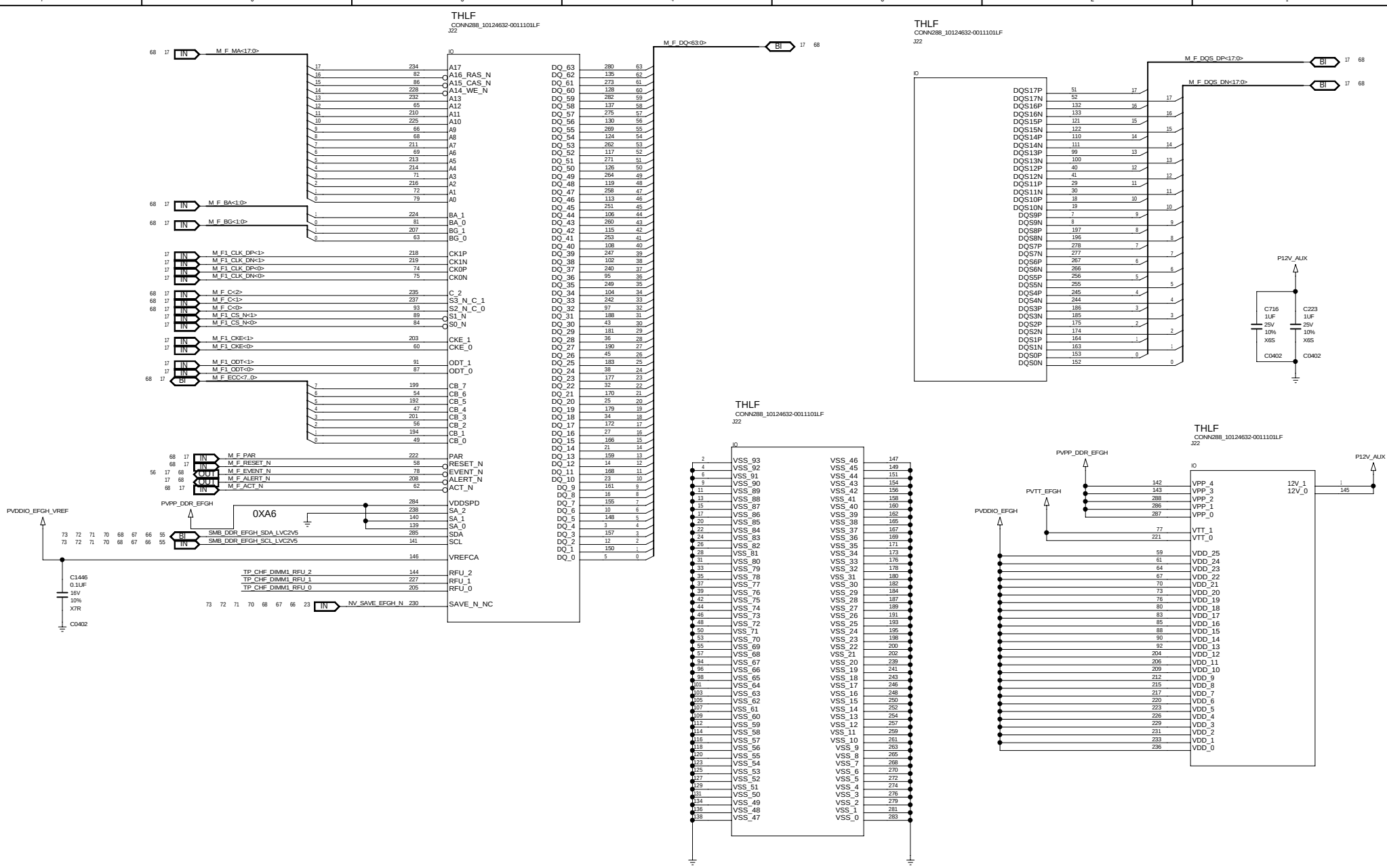
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			SHEET 67 OF 226



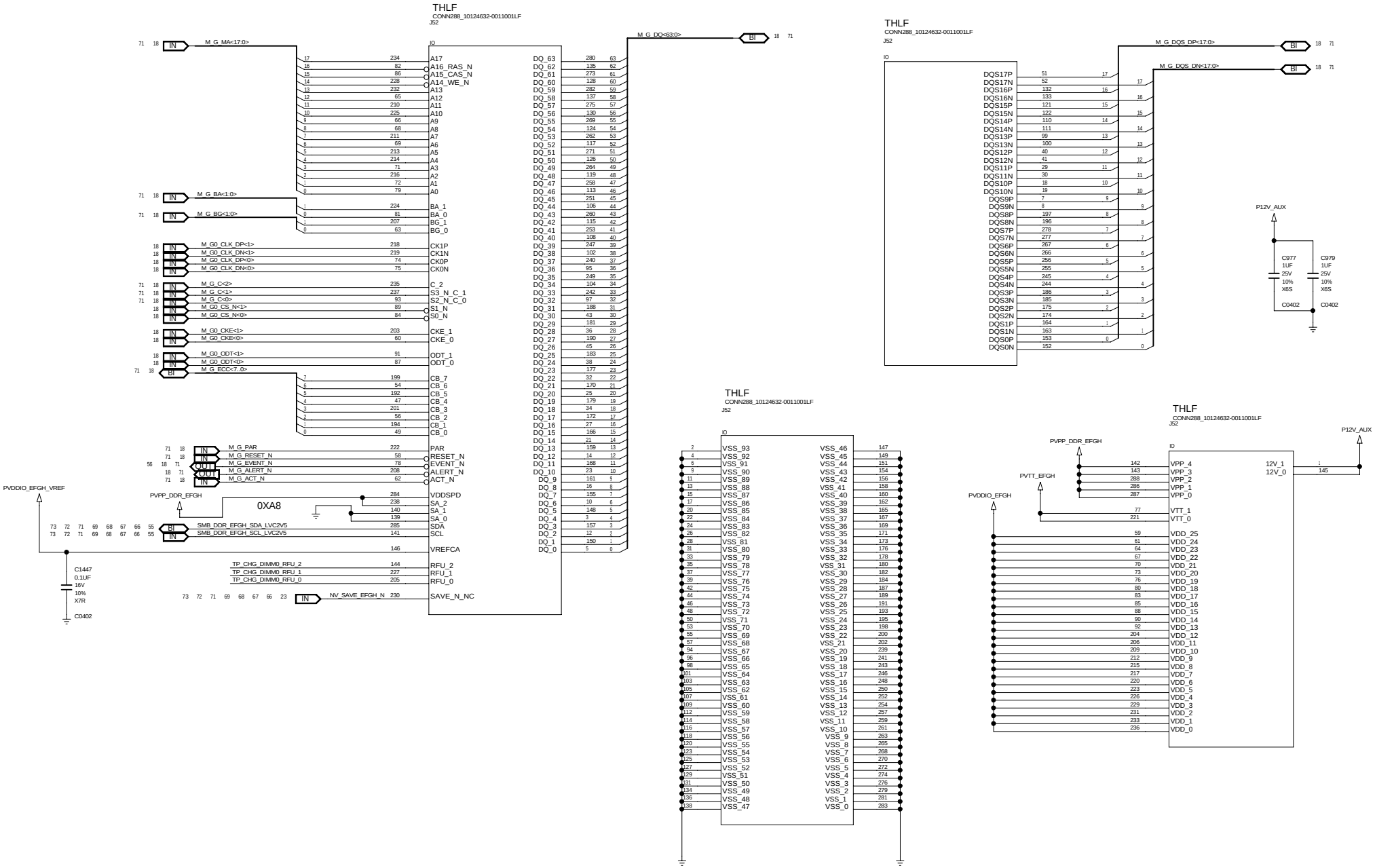
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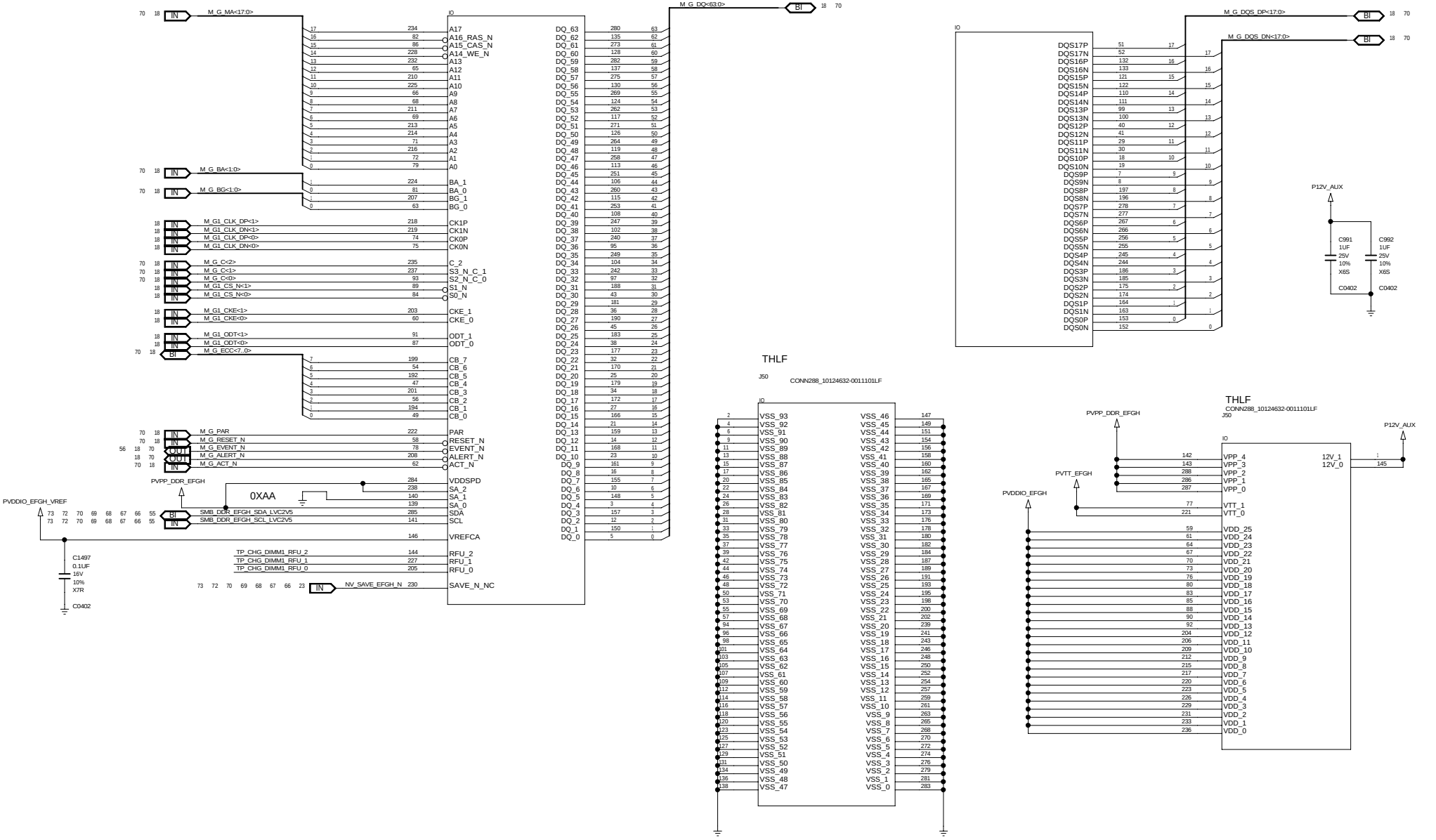
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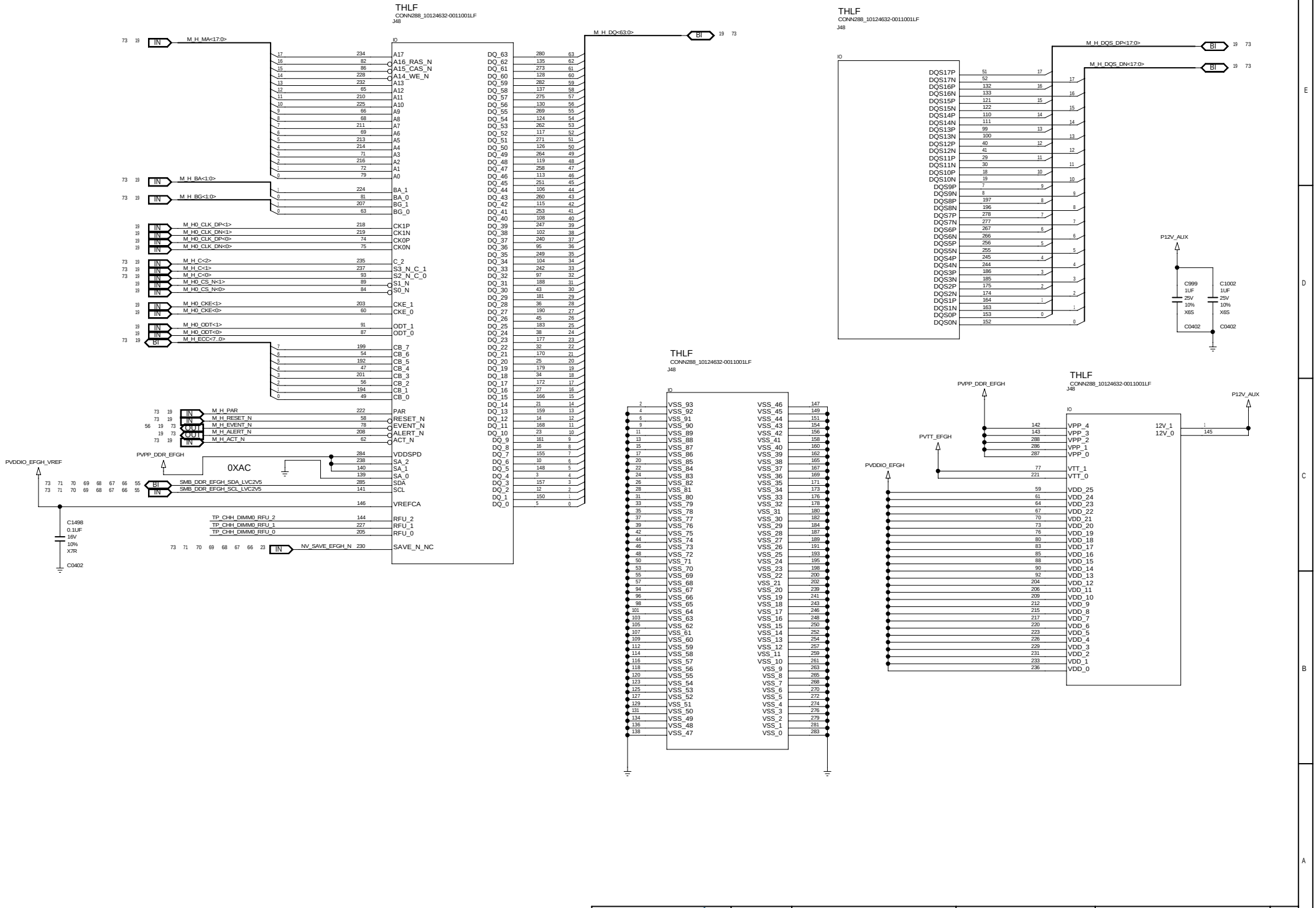
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		SIZE: C	DATE: Fri Dec 15 20:21:44 2017
			SHEET 70 OF 226



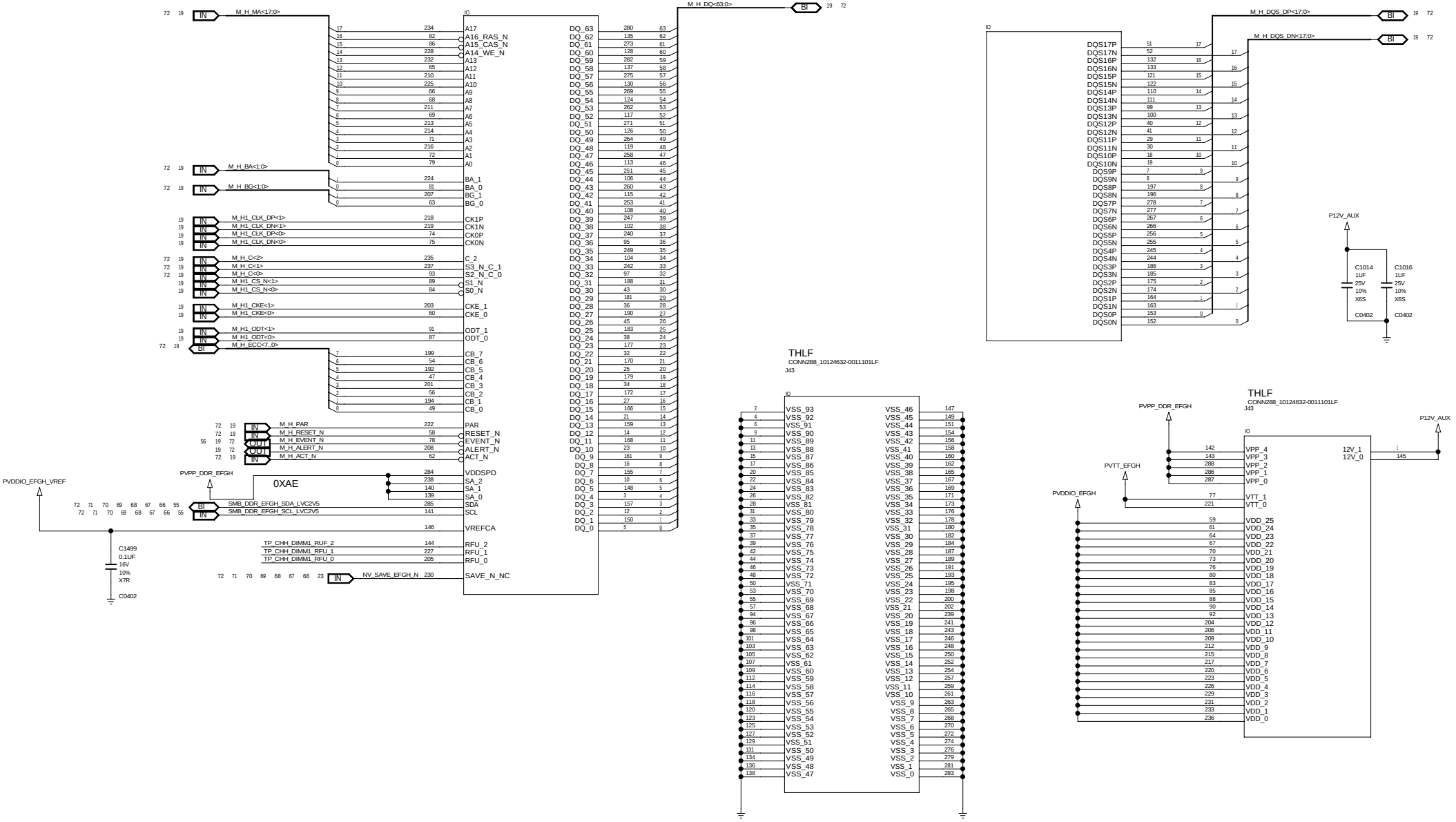
CPU0 DDR4 CH G2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
		REVIEWER:	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
		SIZE: C	DATE: Fri Dec 15 20:21:44 2017
			SHEET 71 OF 226



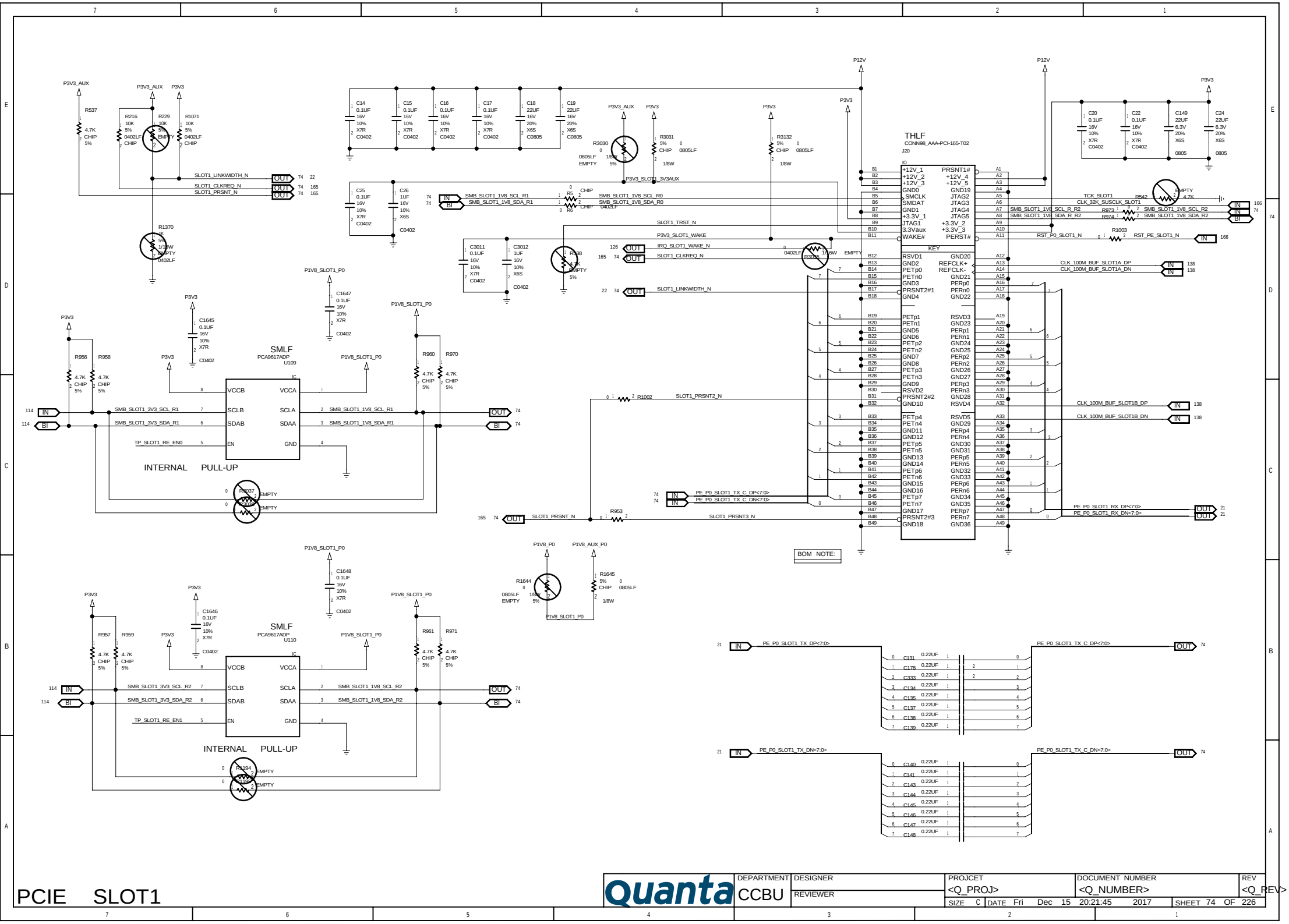
CPU0 DDR4 CH_H1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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			REV: <Q_REV>
		SIZE C	DATE Fri Dec 15 20:21:45 2017
			SHEET 72 OF 226



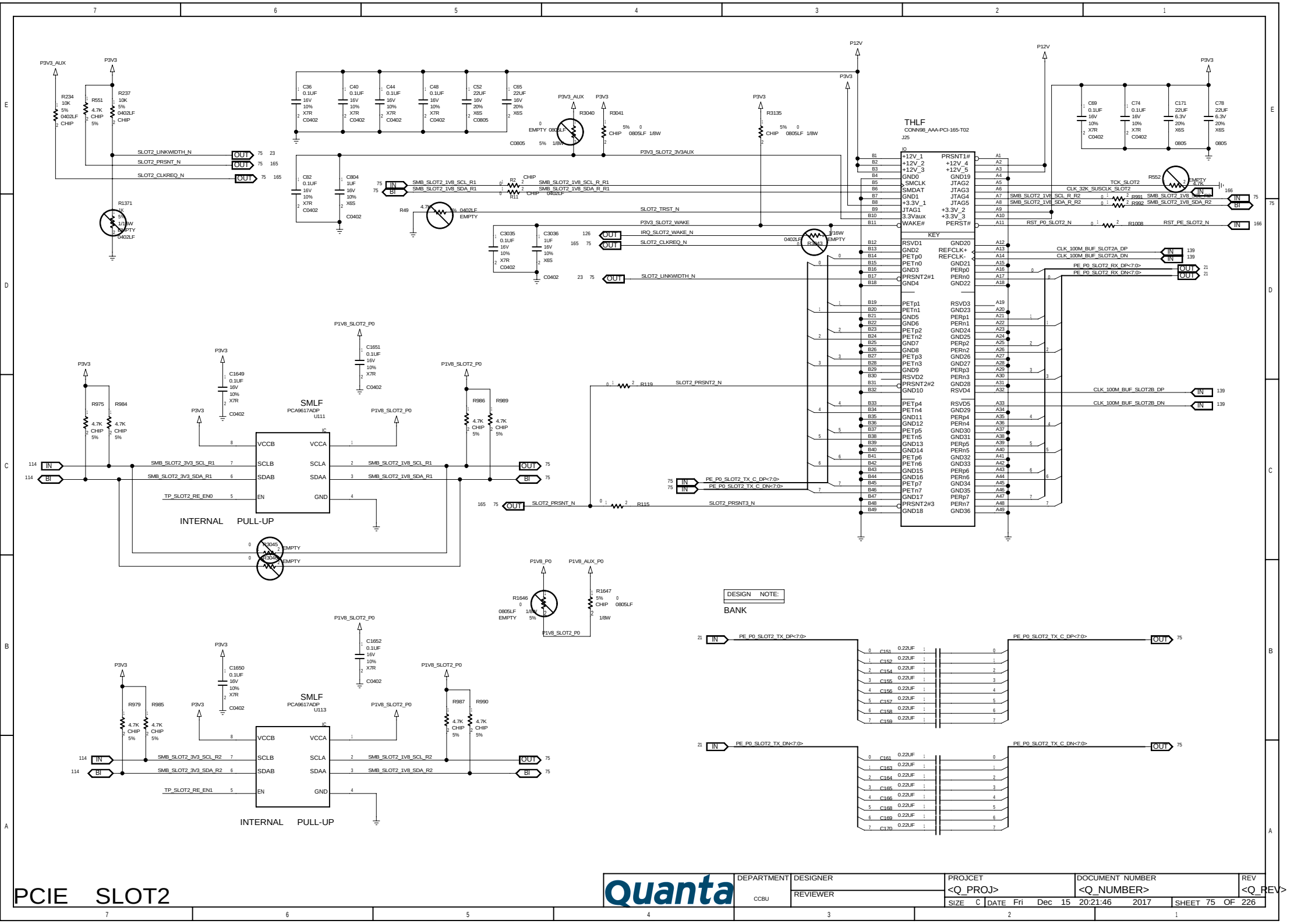
CPU0 DDR4 CH H2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
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		SIZE: C	DATE: Fri Dec 15 20:21:45 2017
			SHEET 73 OF 226



PCIE SLOT1

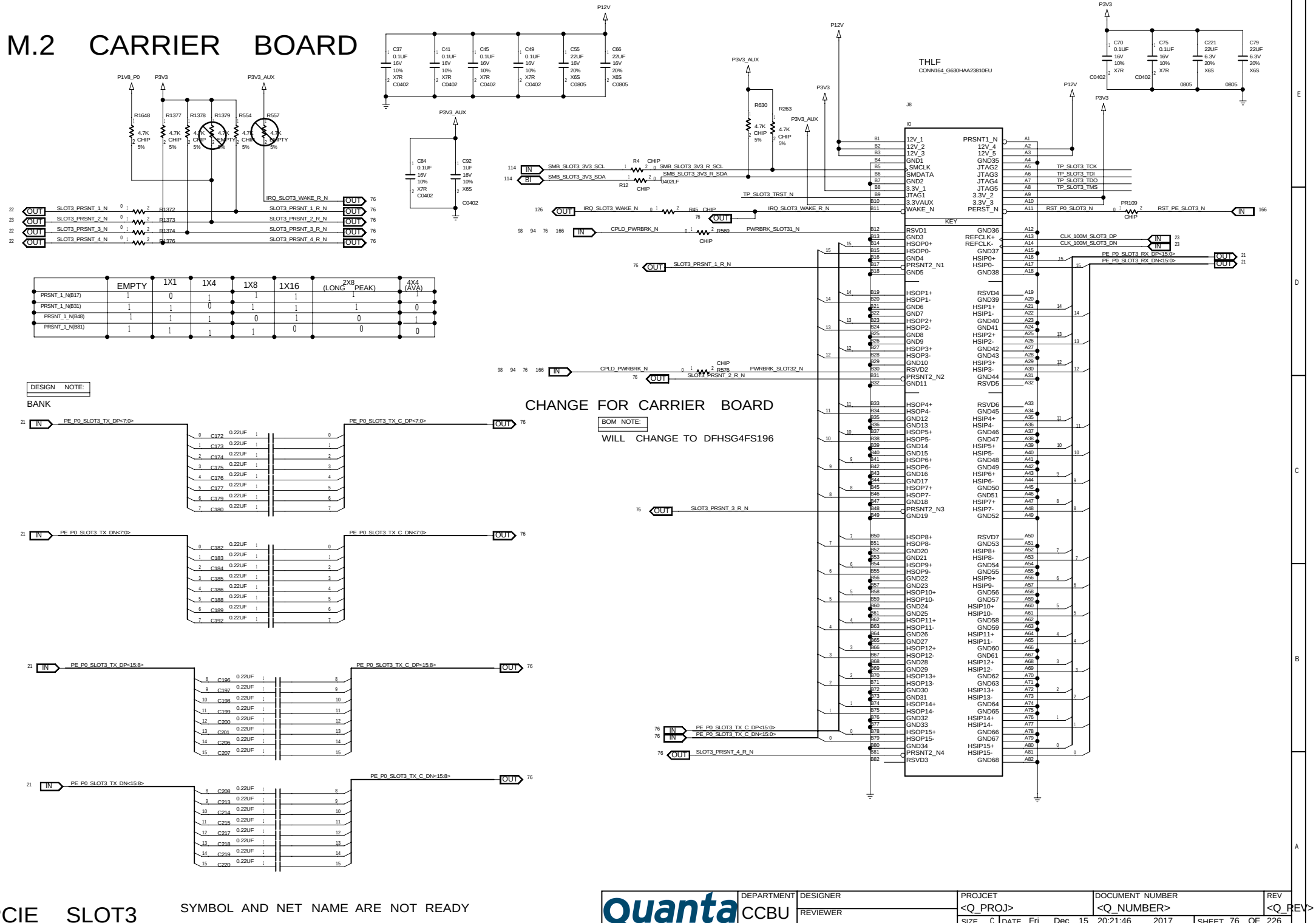
Quanta	DEPARTMENT: CCBU	DESIGNER:	REVIEWER:
PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>	
SIZE: C	DATE: Fri Dec 15 20:21:45 2017	SHEET 74 OF 226	



PCIE SLOT2

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>
DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>	SIZE: C	DATE: Fri Dec 15 20:21:46 2017
SHEET 75 OF 226			

M.2 CARRIER BOARD



	EMPTY	1X1	1X4	1X8	1X16	2X8 (LONG PEAK)	4X4 (AVA)
PRSNT_1_N(B17)	1	0	1	1	1	1	1
PRSNT_1_N(B31)	1	1	0	1	1	1	0
PRSNT_1_N(B48)	1	1	1	0	1	0	1
PRSNT_1_N(B81)	1	1	1	1	0	0	0

DESIGN NOTE:

BANK

CHANGE FOR CARRIER BOARD

BOM NOTE:

WILL CHANGE TO DFHSG4FS196

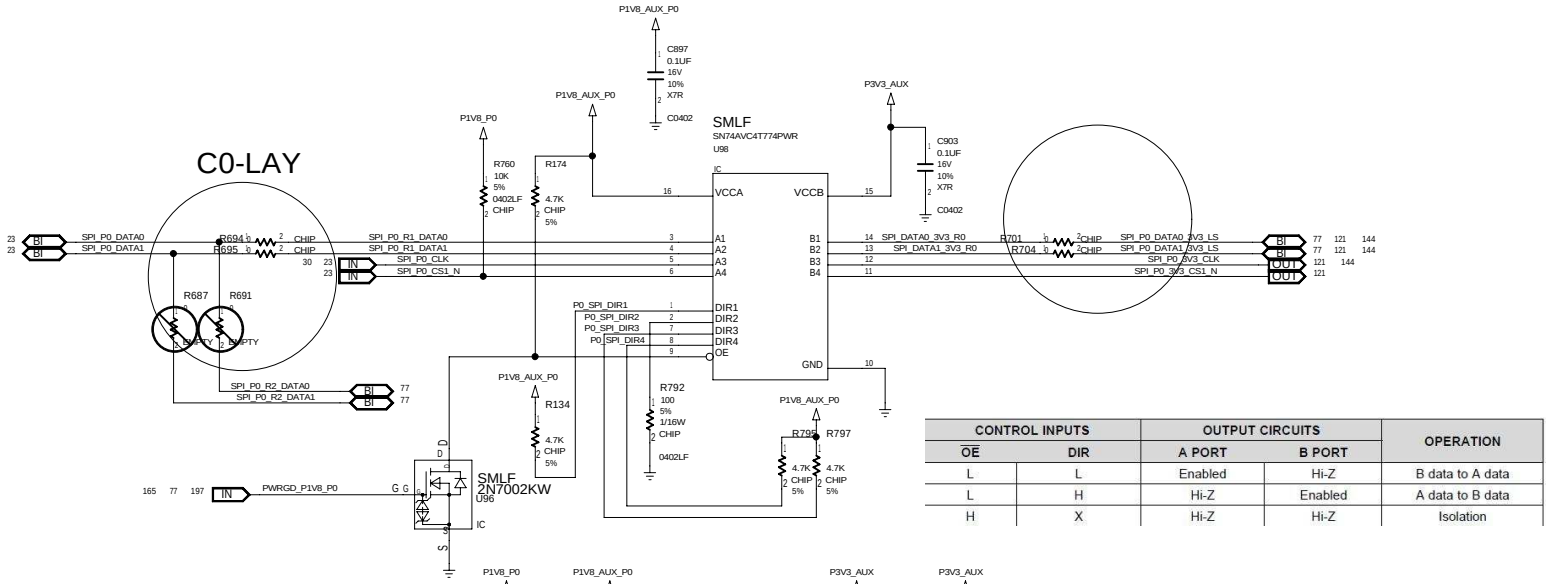
PCIE SLOT3

SYMBOL AND NET NAME ARE NOT READY

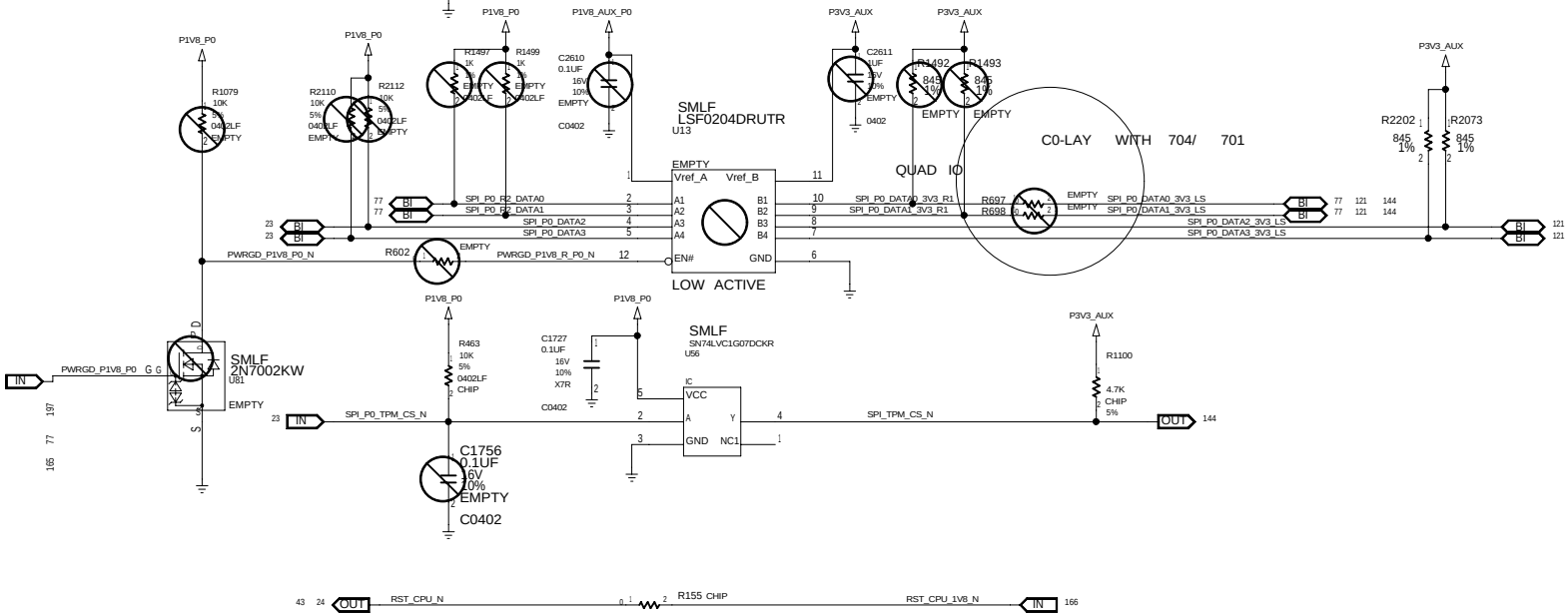
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:46 2017 SHEET 76 OF 226

1.8V/3.3V VOLTAGE TRANSLATION

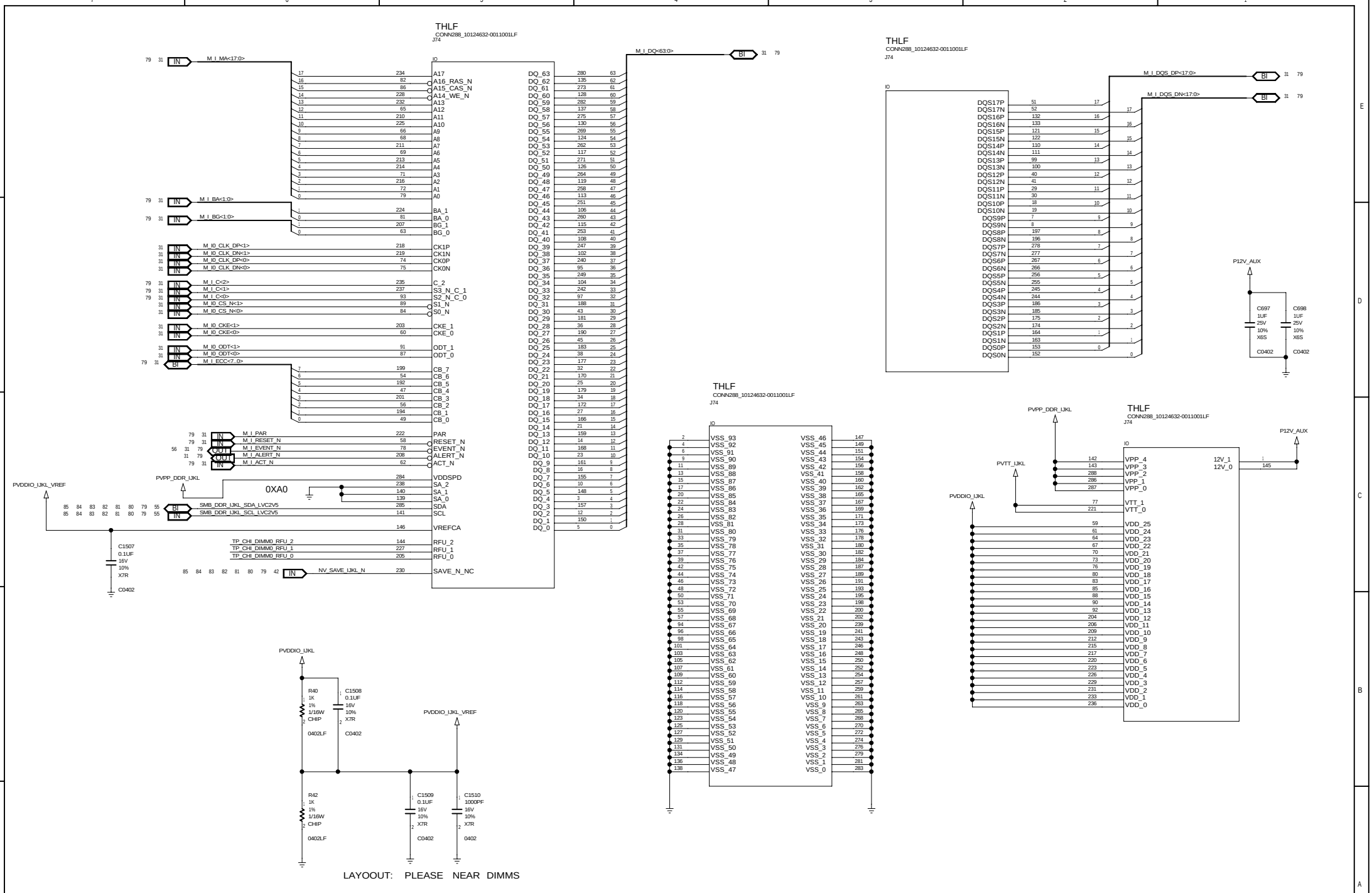


CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation



SPI TRANSLATION

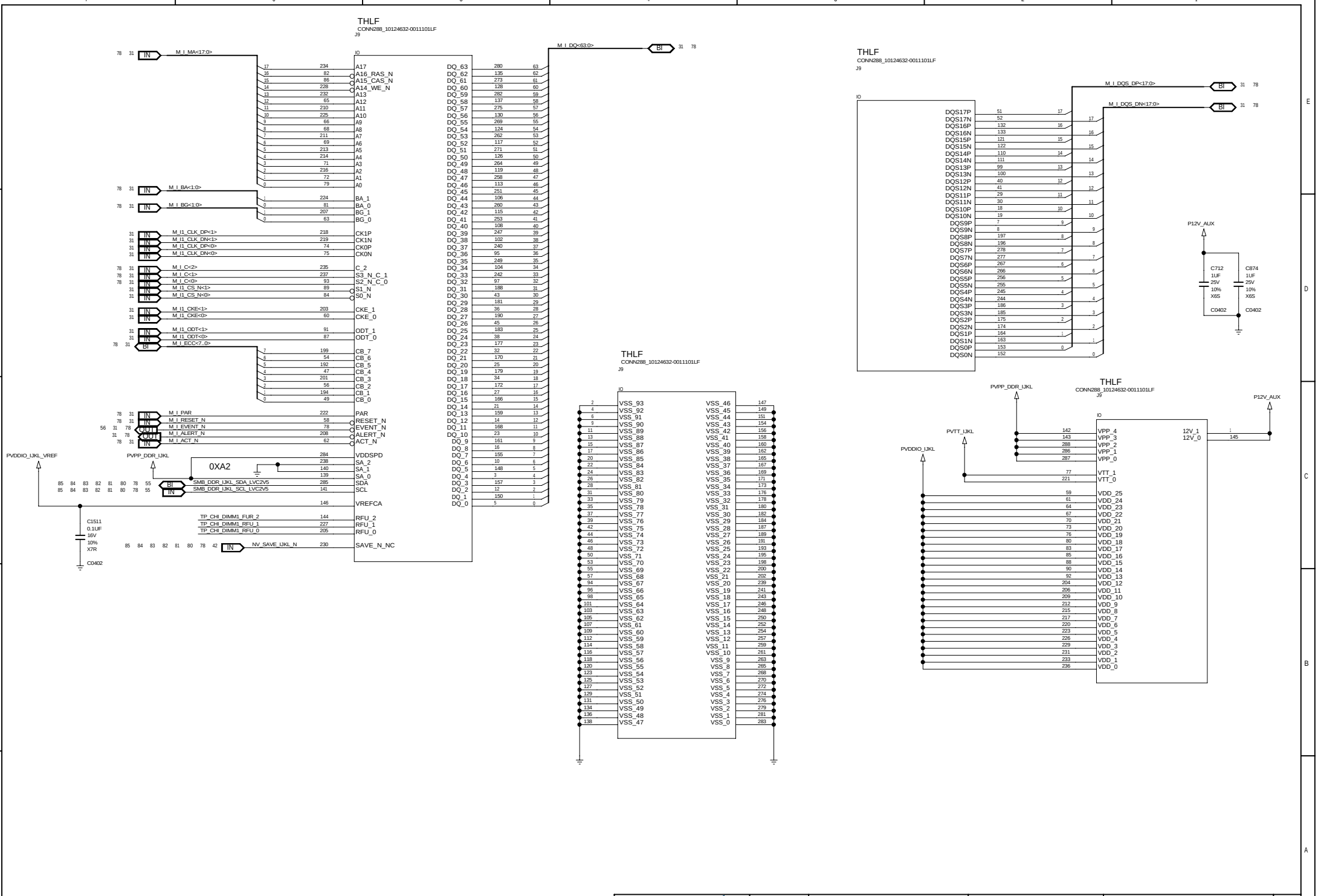
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		REVIEWER	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
		SIZE C	DATE Fri Dec 15 20:21:20 2017
			SHEET 77 OF 226



LAYOOUT: PLEASE NEAR DIMMS

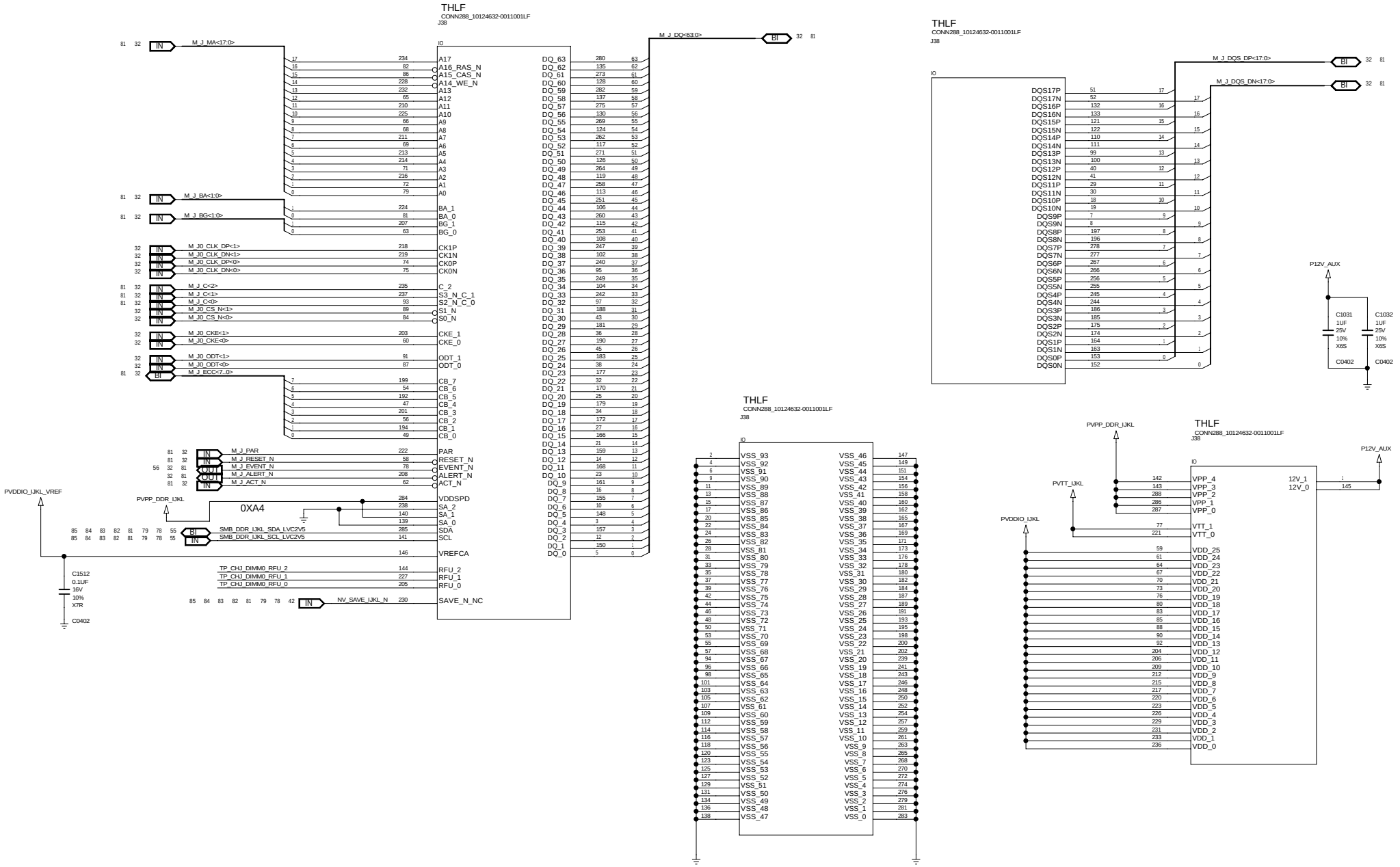
CPU1 DDR4 CH_I1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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			REV: <Q_REV>
	SIZE C	DATE Fri Dec 15 20:21:46 2017	SHEET 78 OF 226



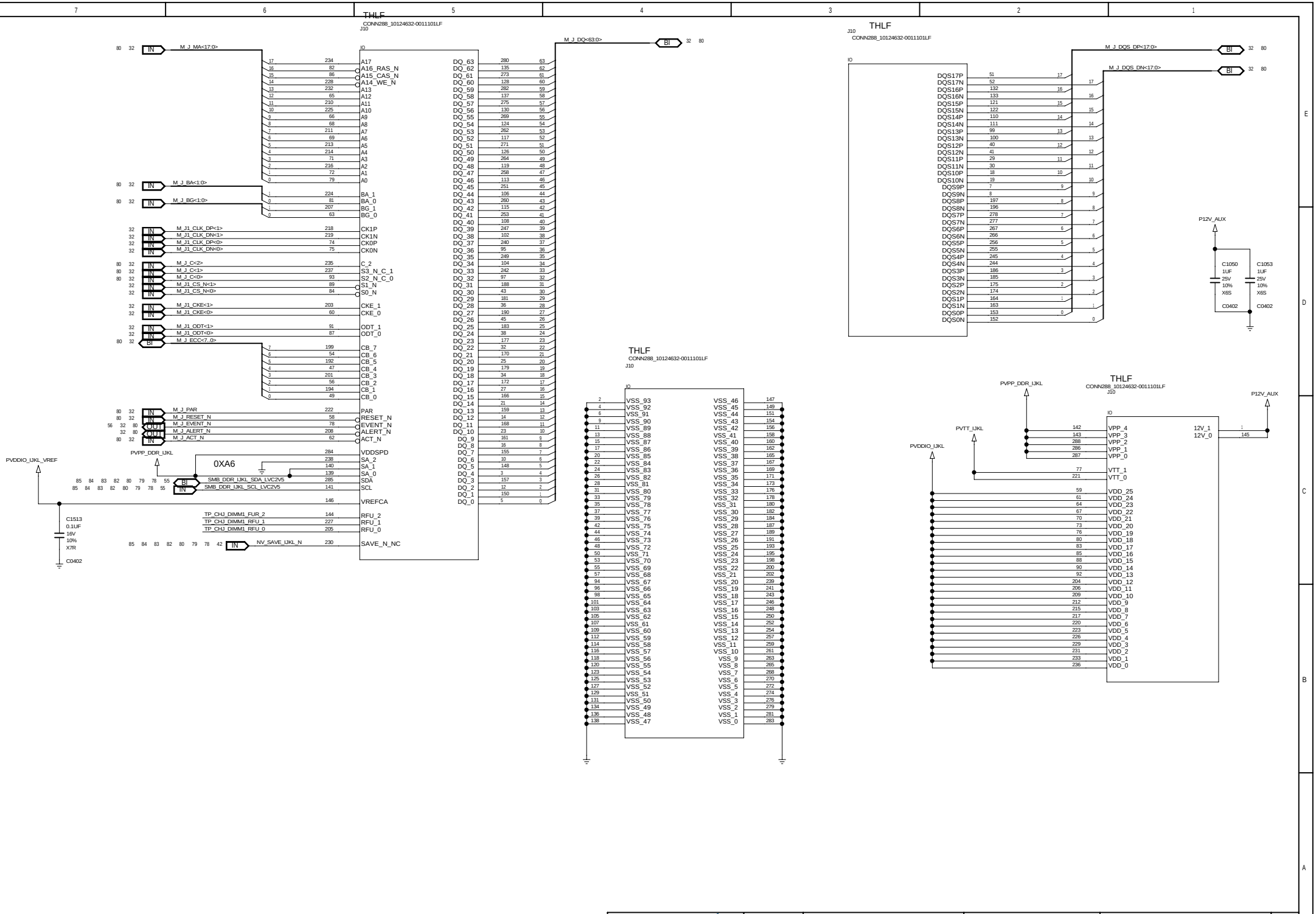
CPU1 DDR4 CH_I2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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			REV: <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:47 2017 SHEET 79 OF 226



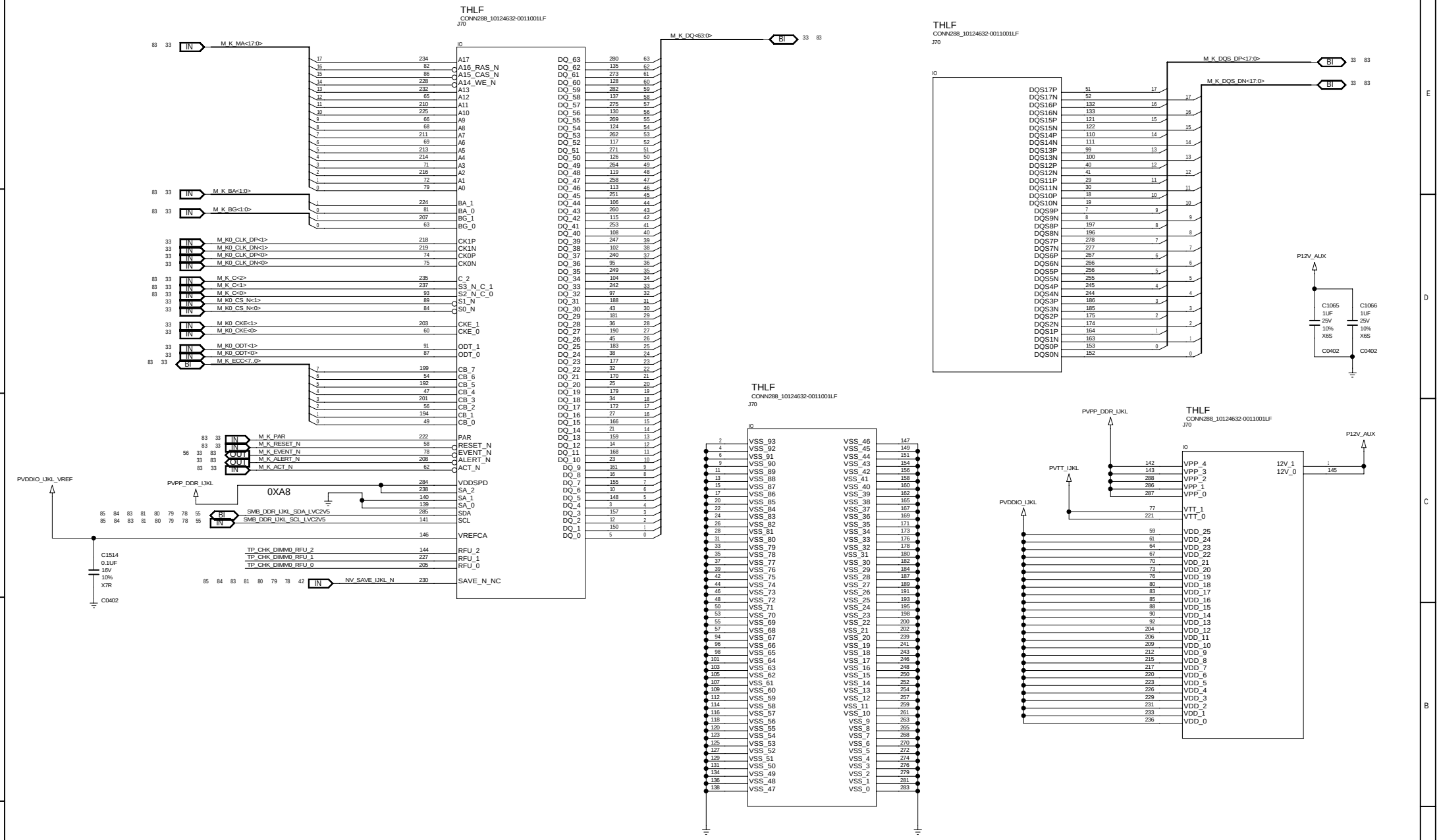
CPU1 DDR4 CH_J1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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		SIZE C	DATE Fri Dec 15 20:21:47 2017
			SHEET 80 OF 226



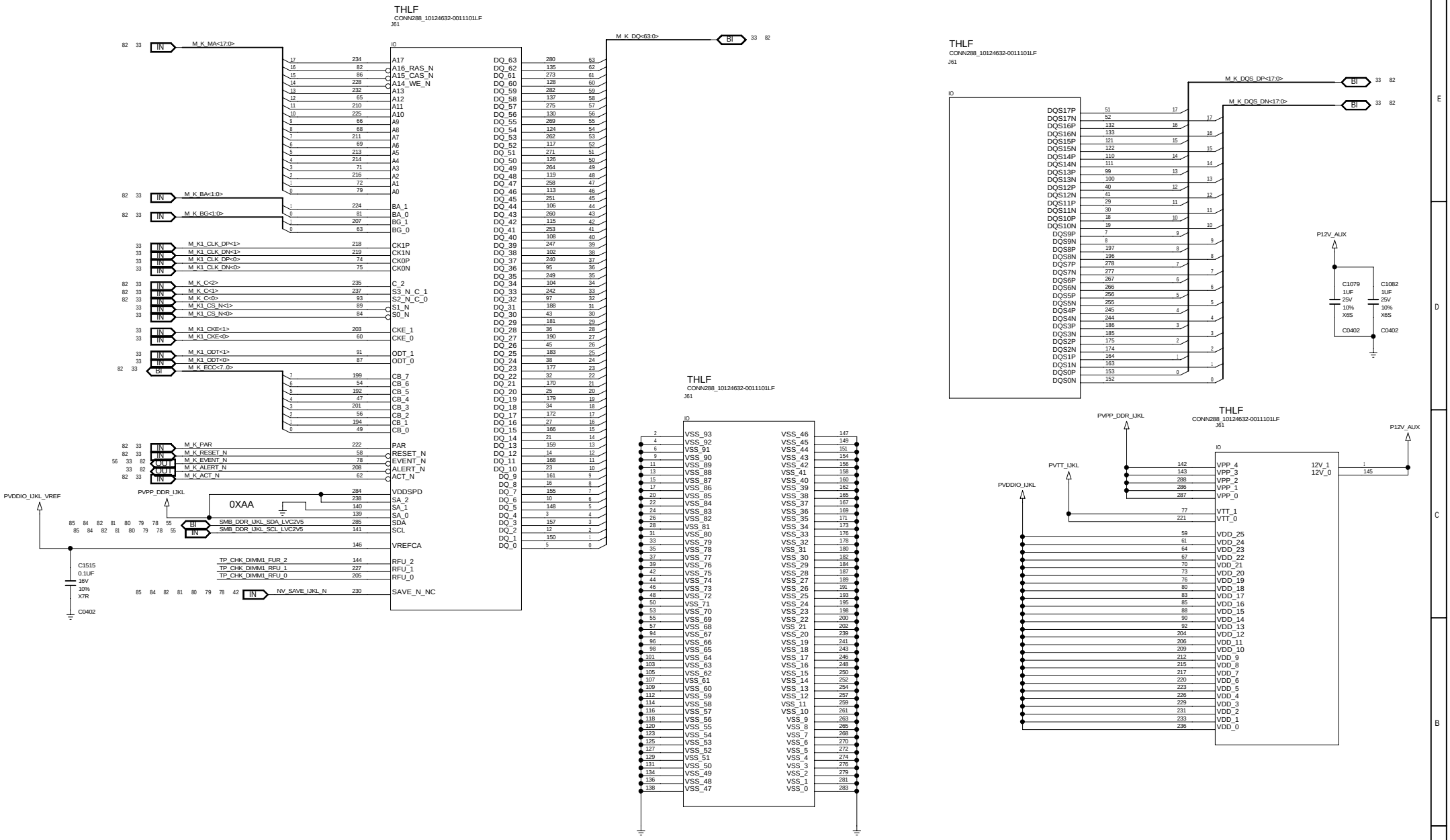
CPU1 DDR4 CH_J2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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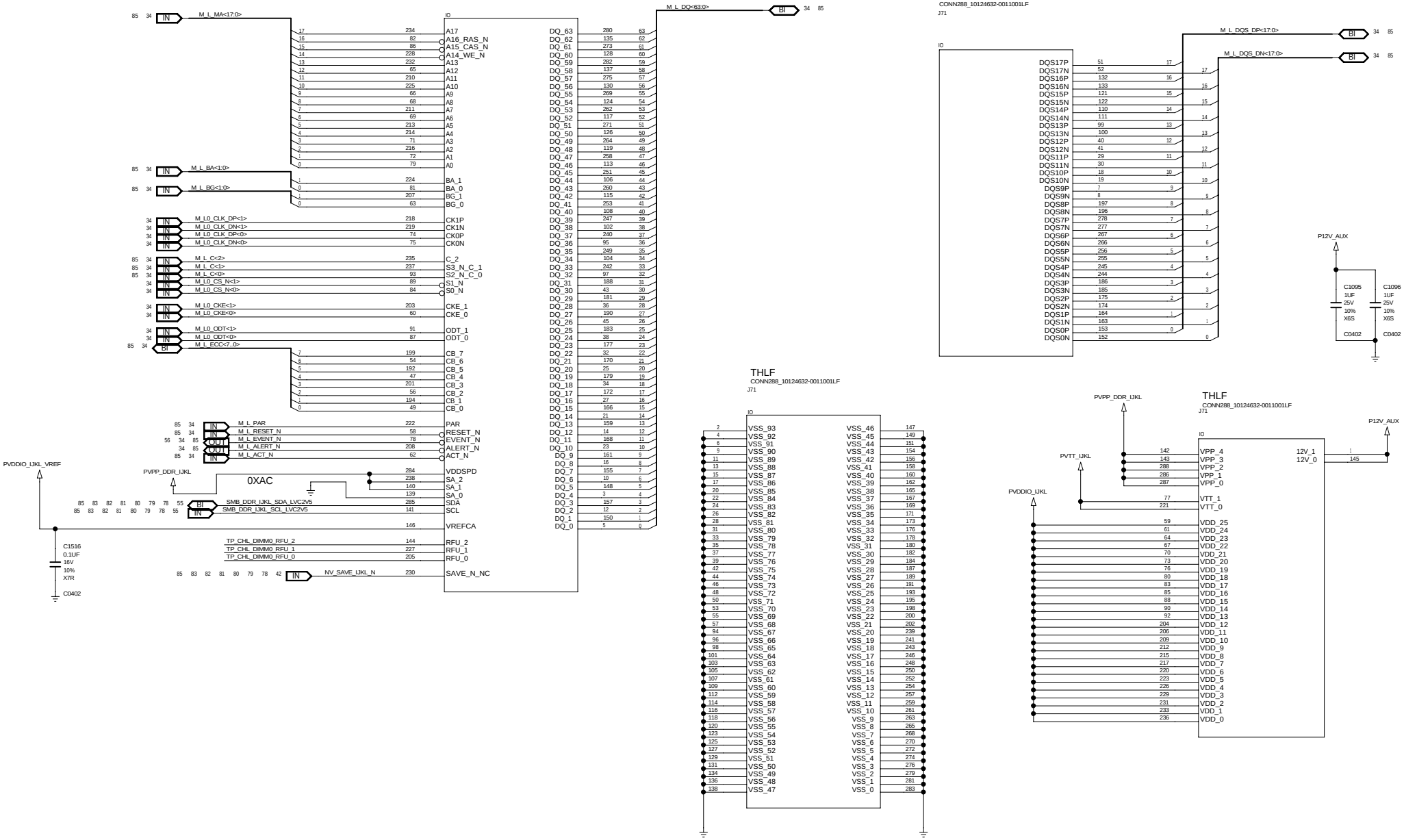
CPU1 DDR4 CH_K1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
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		SIZE: C	DATE: Fri Dec 15 20:21:48 2017
			SHEET 82 OF 226



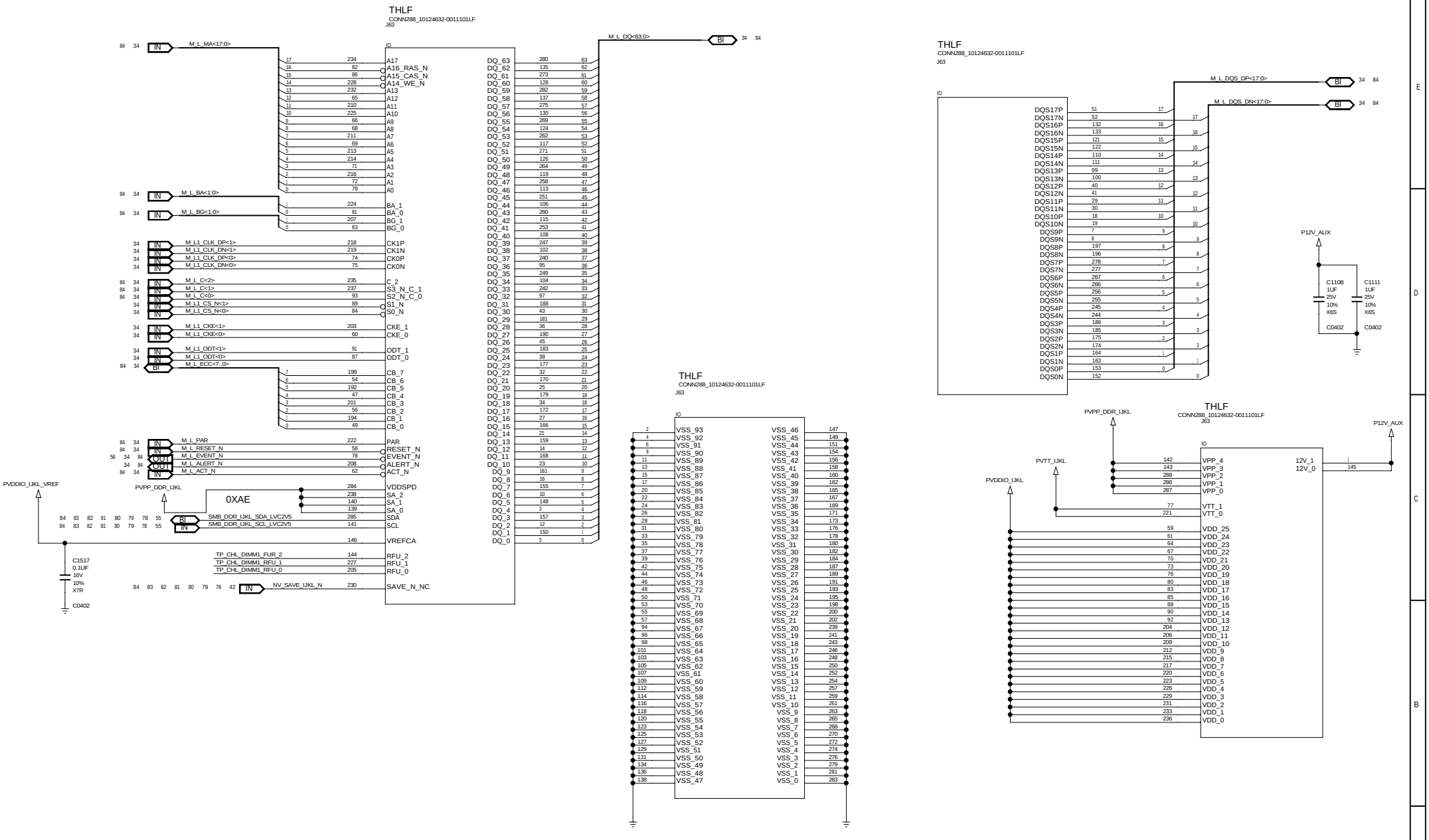
CPU1 DDR4 CH_K2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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			REV: <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:48 2017 SHEET 83 OF 226



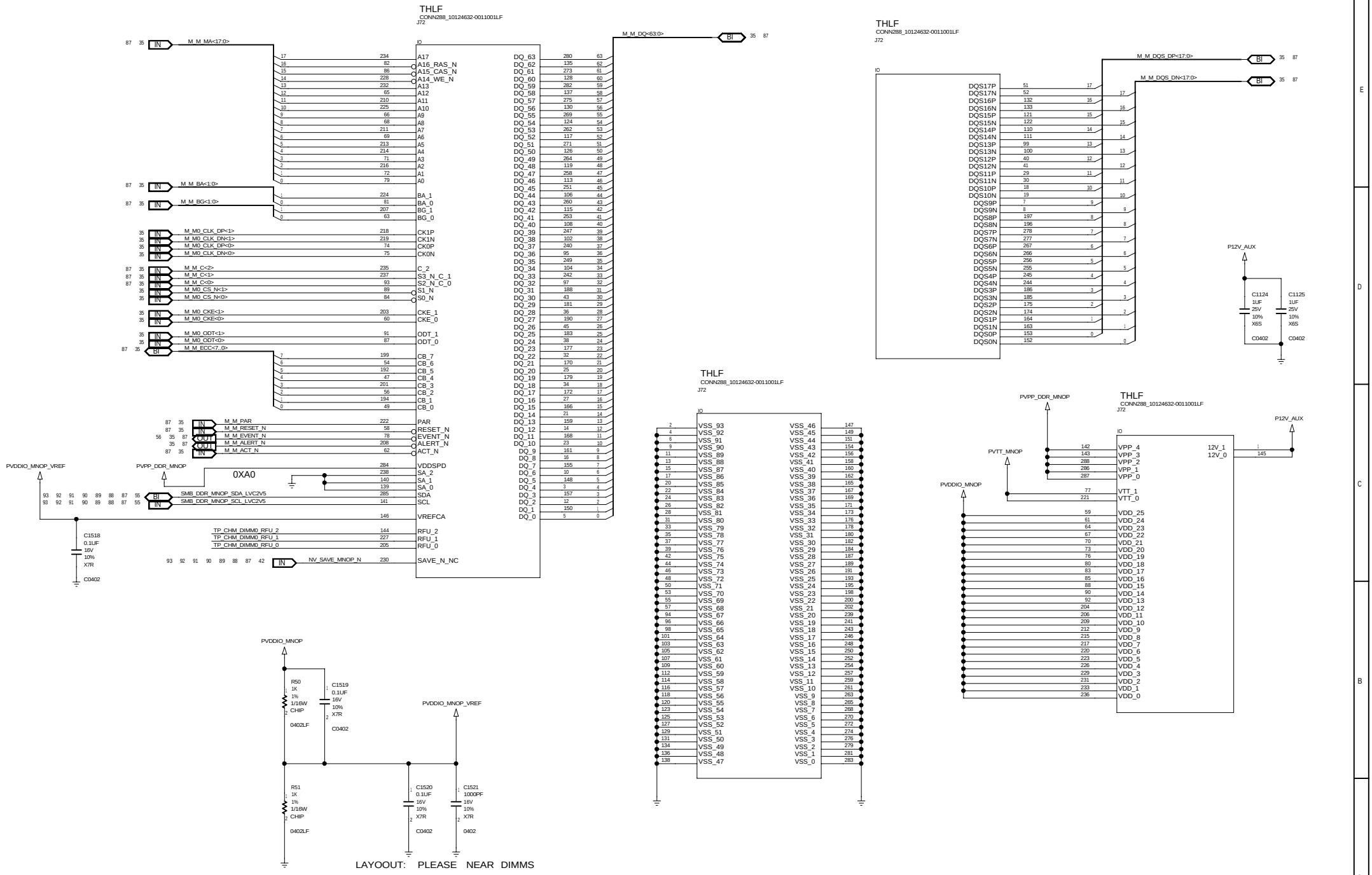
CPU1 DDR4 CH_L1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
		REVIEWER:	DOCUMENT NUMBER: <Q_NUMBER>
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		SIZE: C	DATE: Fri Dec 15 20:21:49 2017
			SHEET 84 OF 226



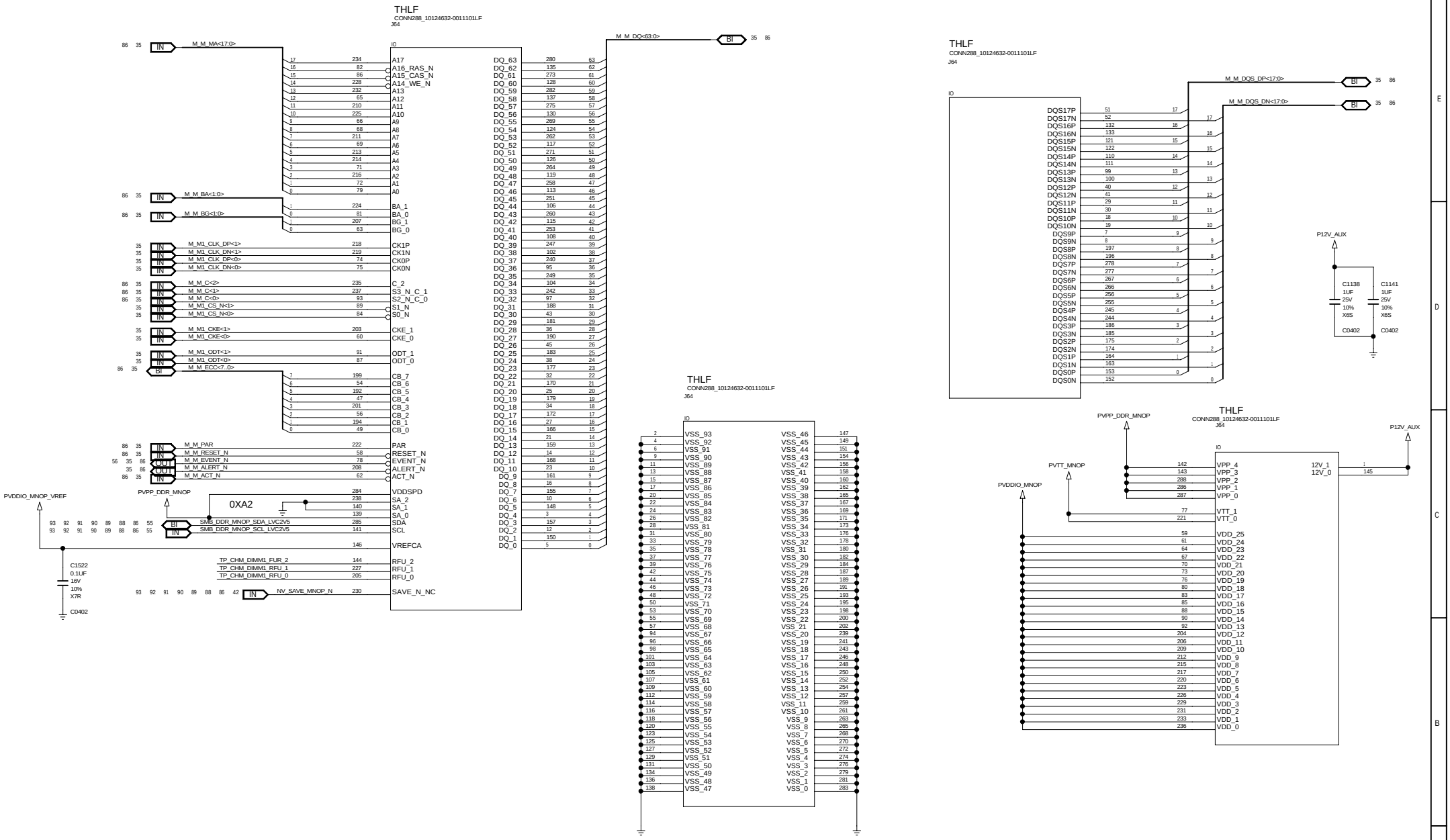
CPU1 DDR4 CH_L2(BLACK)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:49 2017
				SHEET 85 OF 226



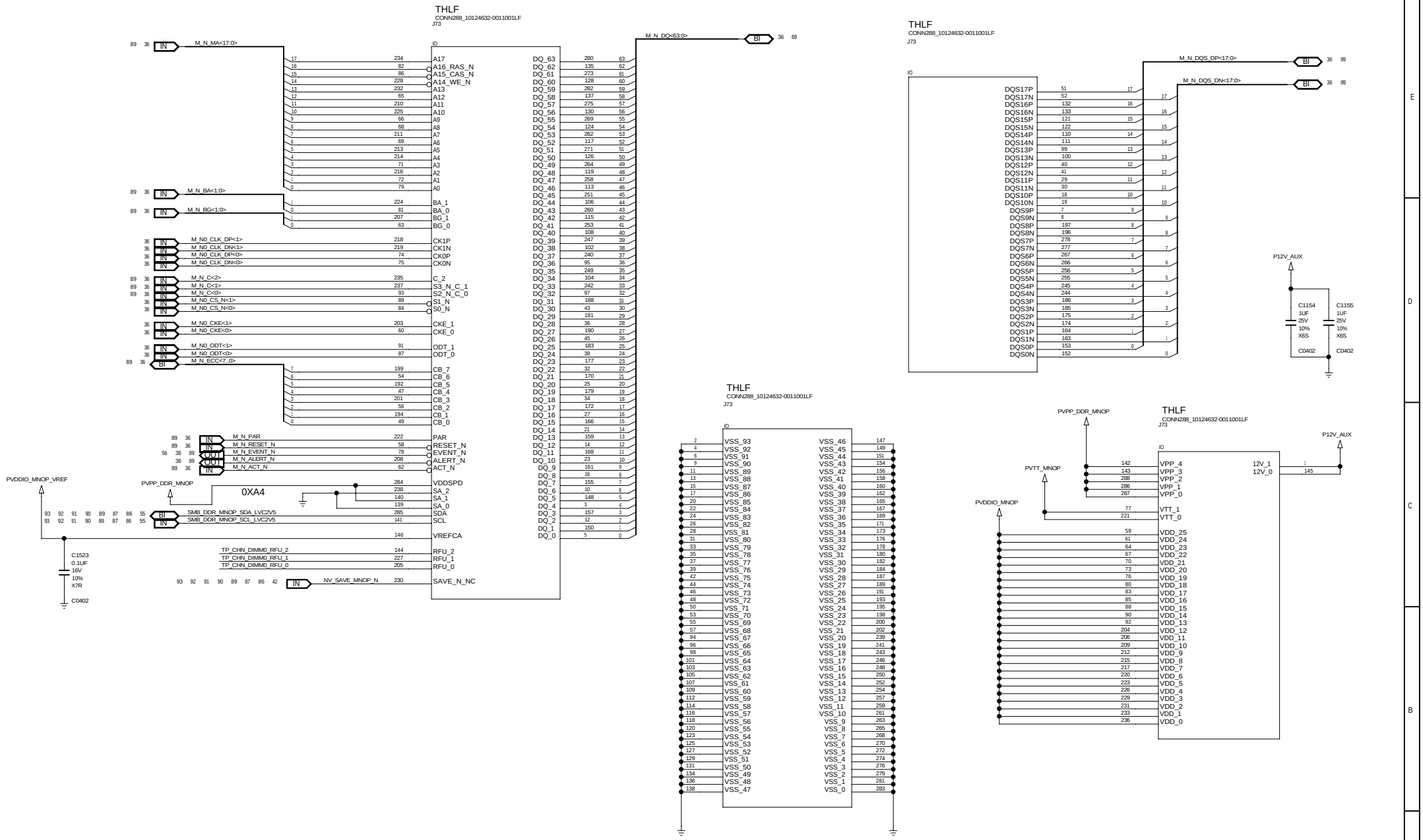
CPU1 DDR4 CH_M1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
			SIZE C · DATE Fri Dec 15 20:21:49 2017 · SHEET 86 OF 226



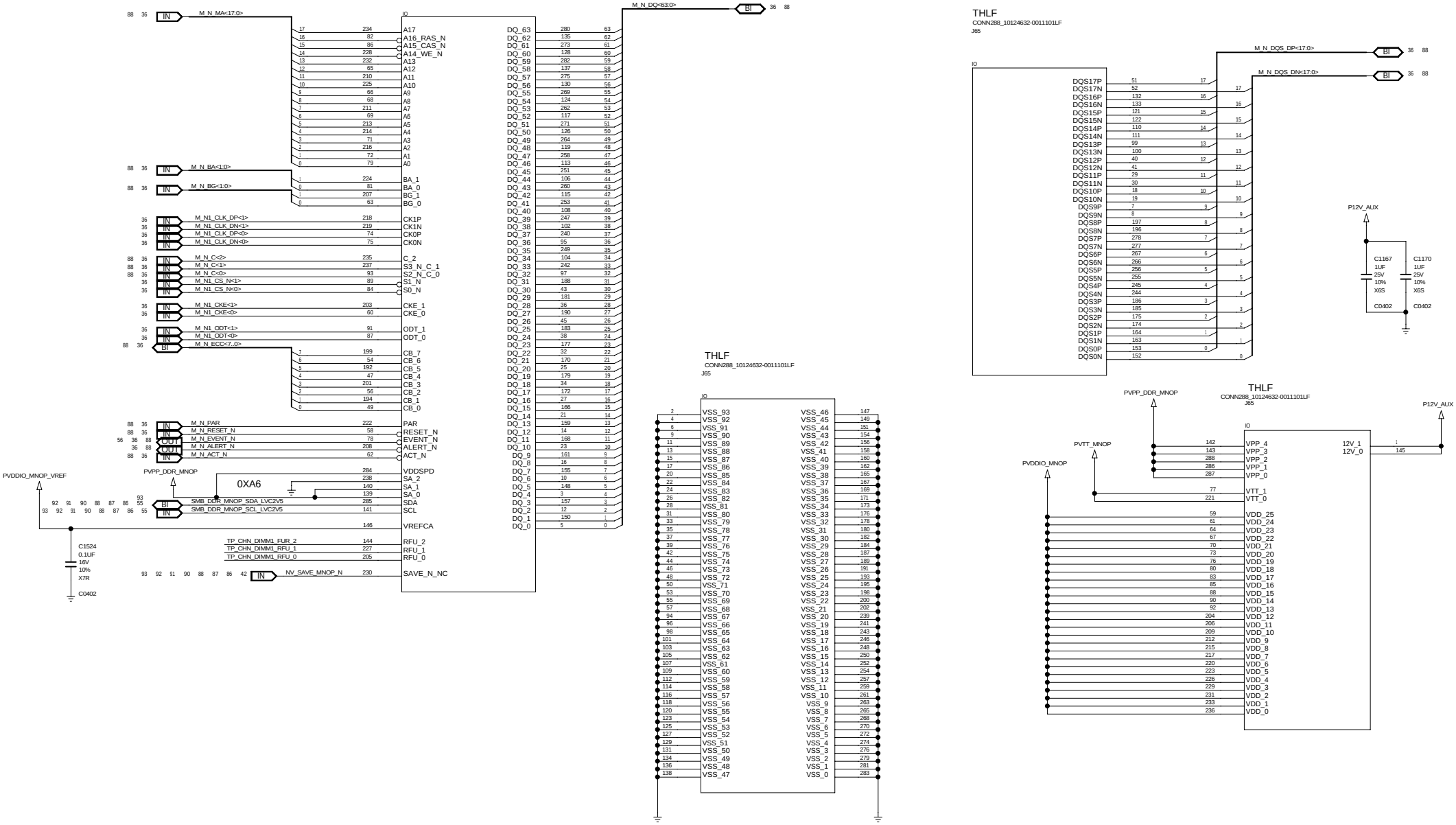
CPU1 DDR4 CH_M2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
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			REV: <Q_REV>
		SIZE: C	DATE: Fri Dec 15 20:21:50 2017
			SHEET 87 OF 226



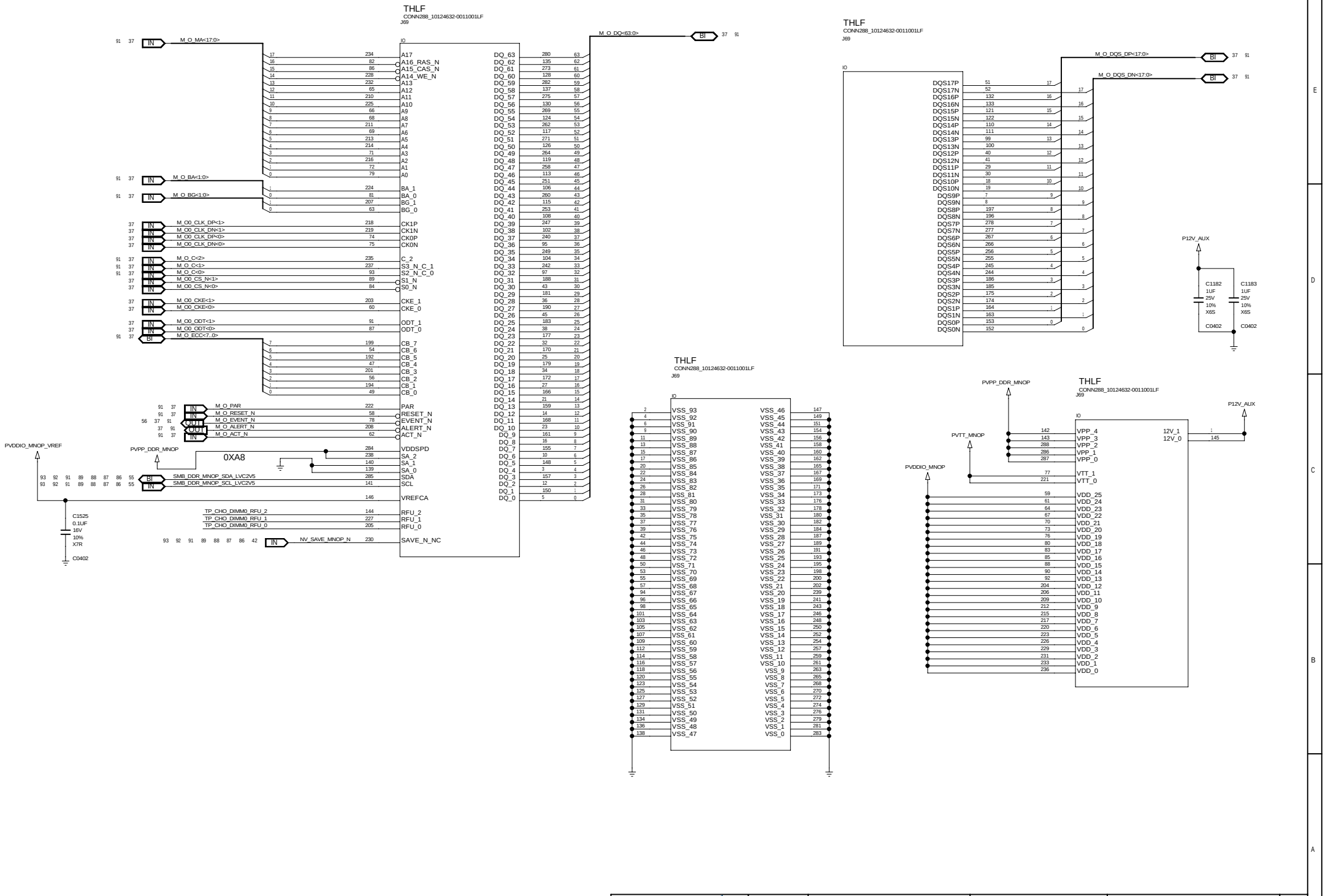
CPU1 DDR4 CH_N1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
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			SHEET 88 OF 226



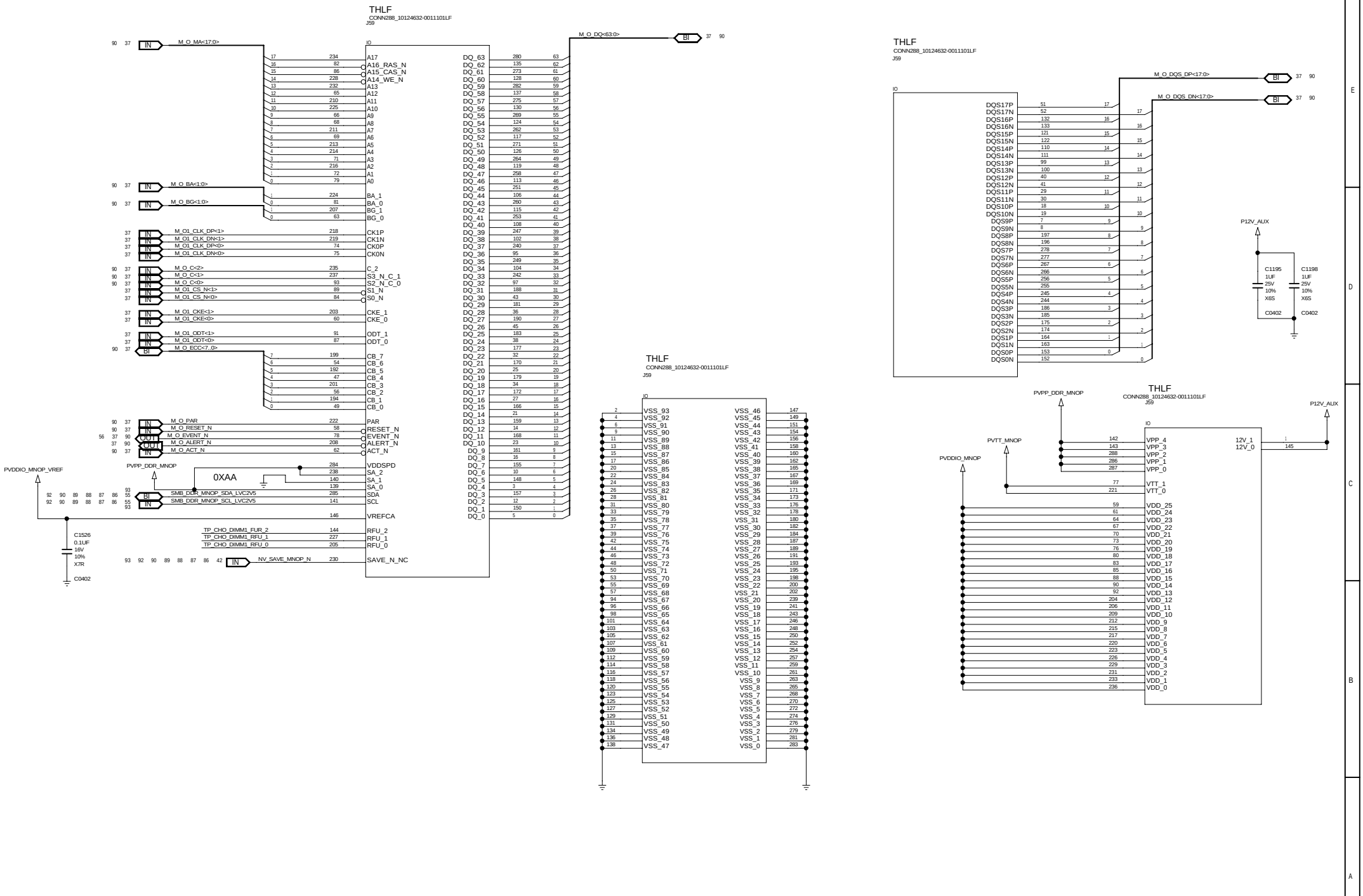
CPU1 DDR4 CH_N2(BLACK)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
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			REV: <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:51 2017 SHEET 89 OF 226



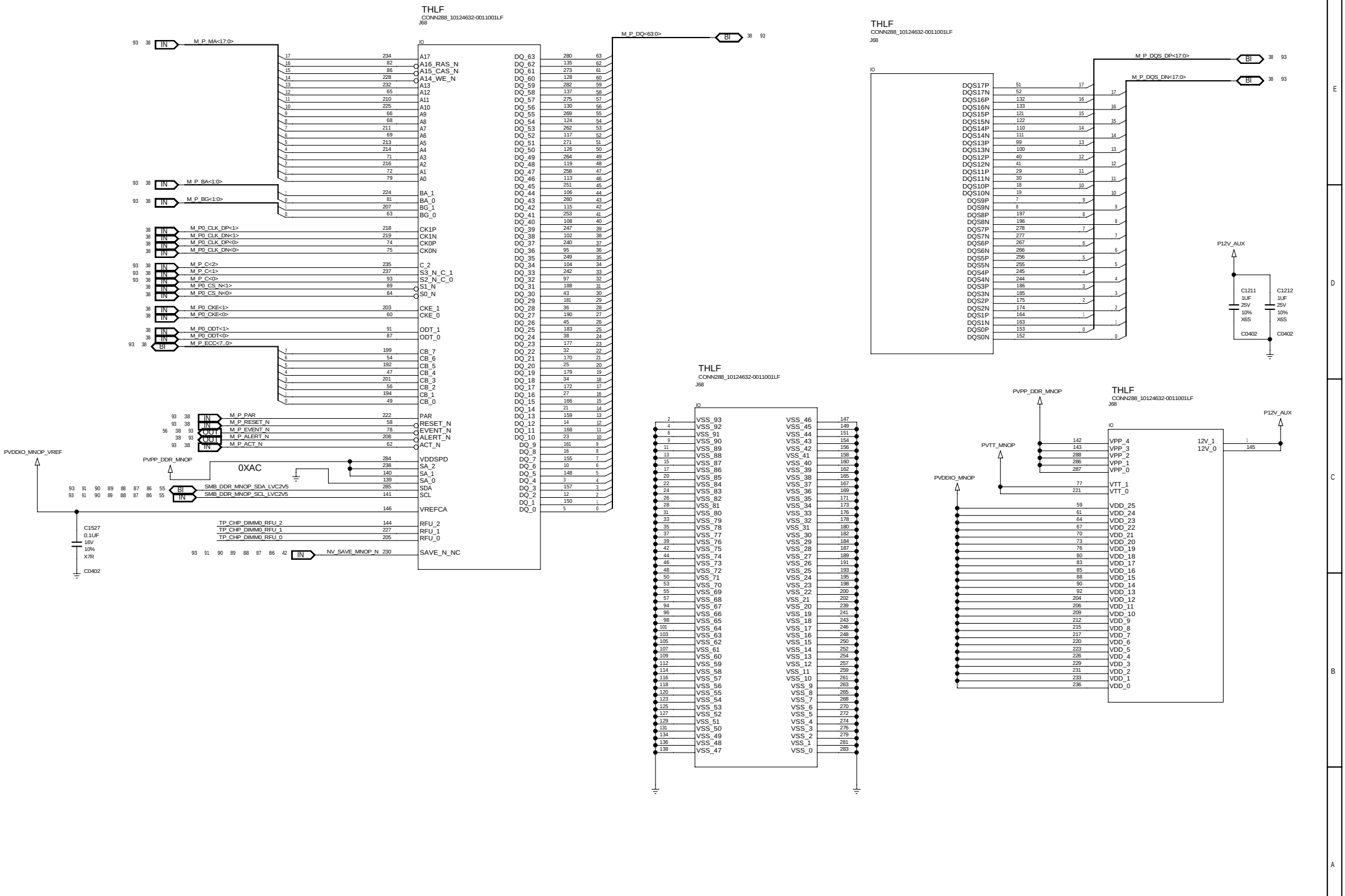
CPU1 DDR4 CH_O1(YELLOW)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
		REVIEWER:	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
		SIZE: C	DATE: Fri Dec 15 20:21:51 2017
			SHEET 90 OF 226



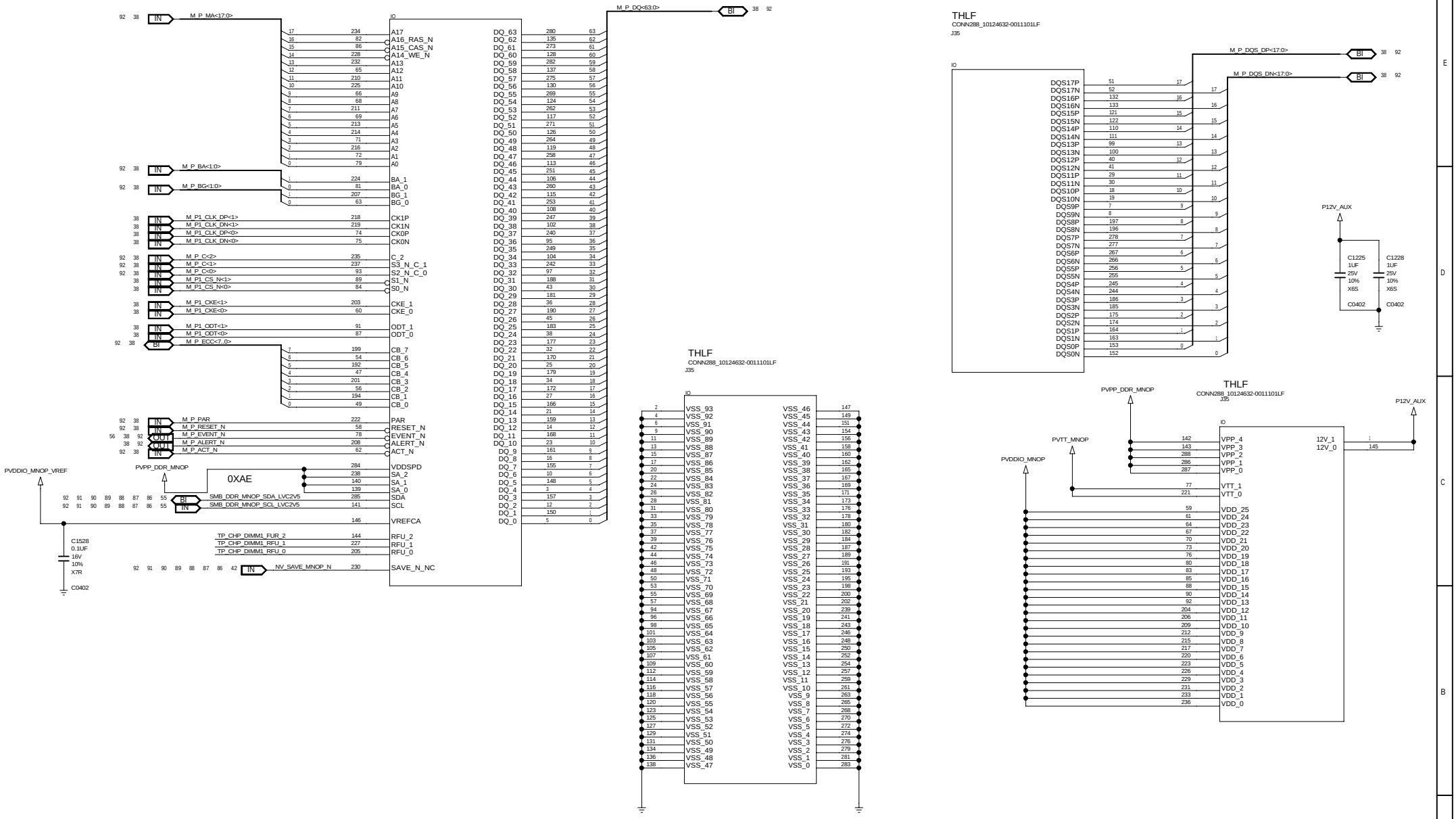
CPU1 DDR4 CH_O2(BLACK)

Quanta	DEPARTMENT: CCBU	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
	DESIGNER:	REVIEWER:	REV: <Q_REV>
	SIZE: C	DATE: Fri Dec 15 20:21:51 2017	SHEET 91 OF 226



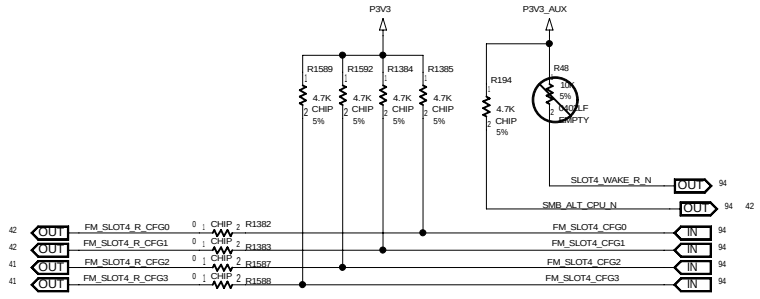
CPU1 DDR4 CH_P1(YELLOW)

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:21:52 2017
				SHEET 92 OF 226



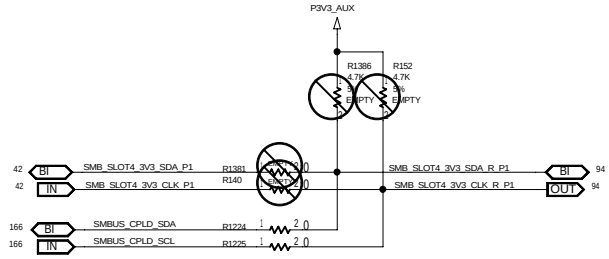
CPU1 DDR4 CH_P2(BLACK)

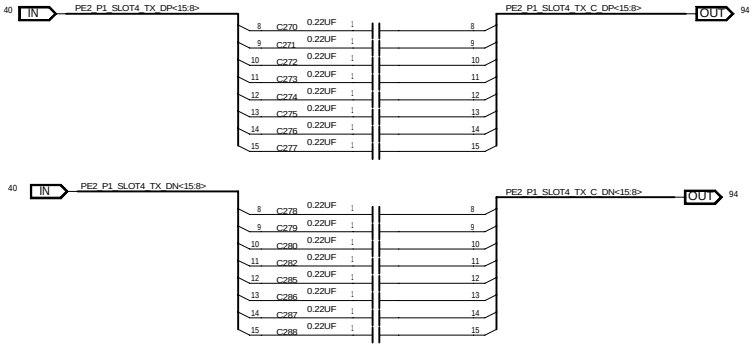
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		REVIEWER:	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
		SIZE: C	DATE: Fri Dec 15 20:21:52 2017
			SHEET 93 OF 226

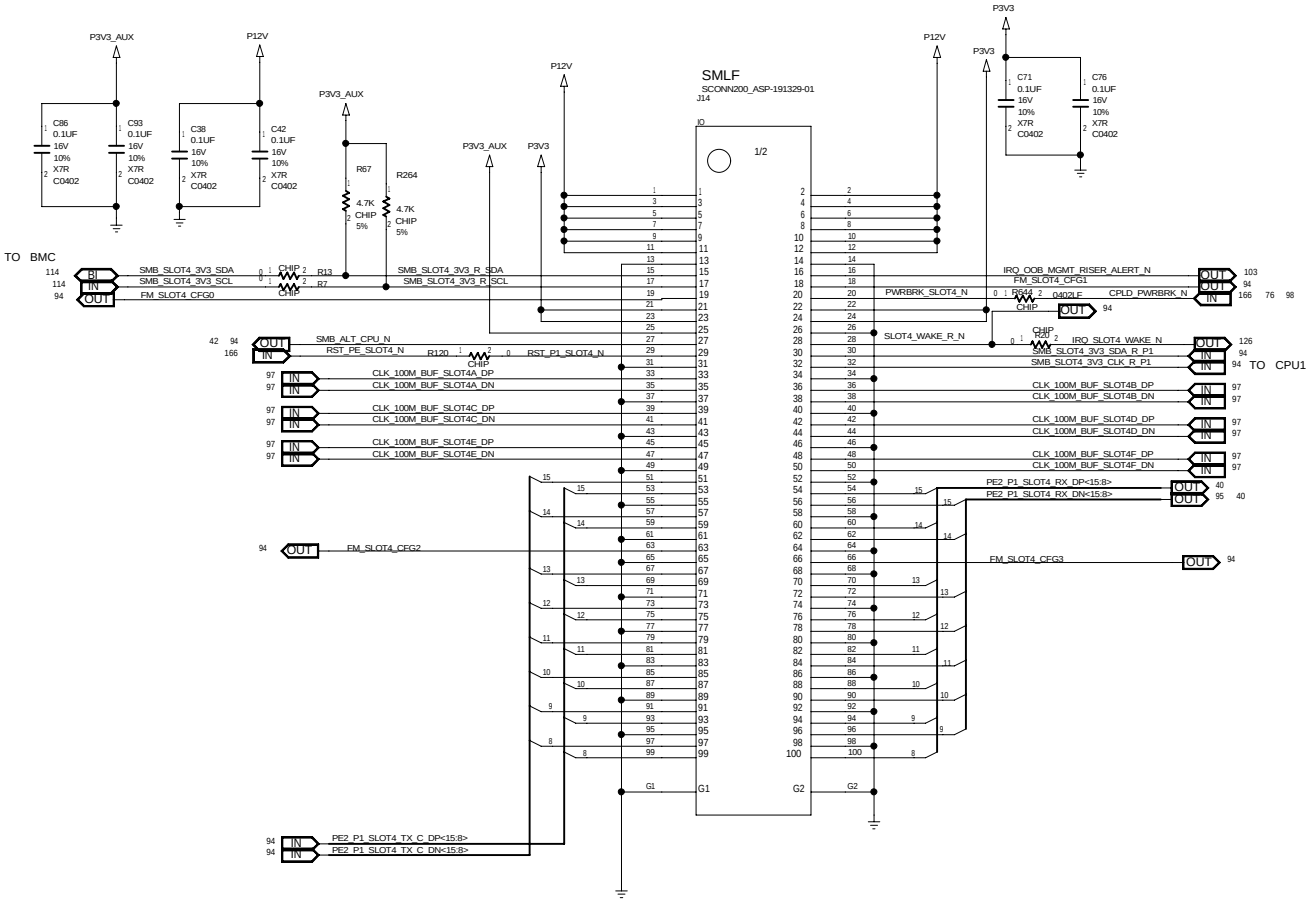


PCIE CONFIG SETTING

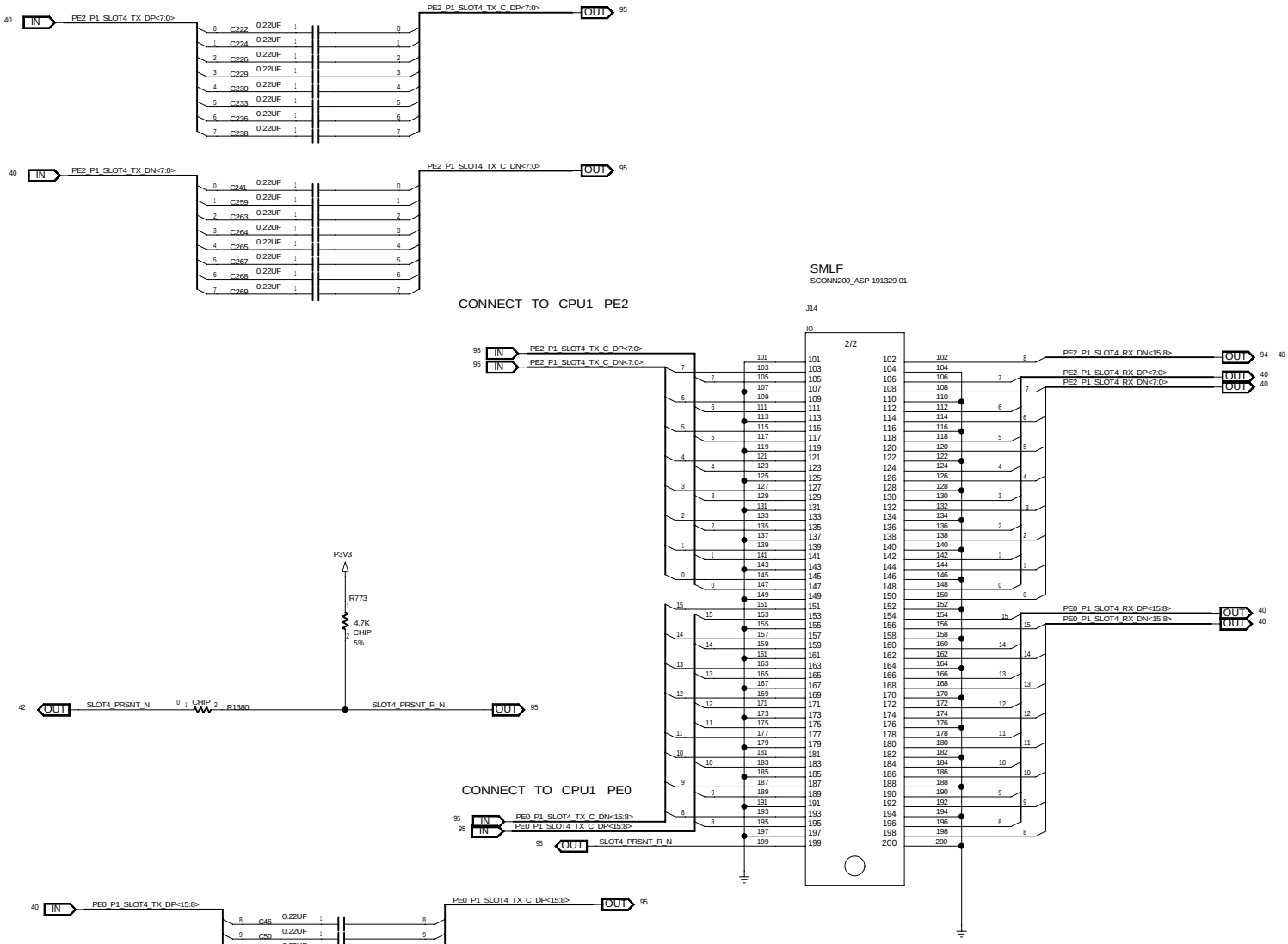
SLOT4_CFG0	SLOT4_CFG1	MB MAPPING TO RISER SLOTS
0	0	SS-2-SLOT PCIE RISER
0	1	SS-2-SLOT PCIE RISER
1	0	DS-2-SLOT PCIE RISER
1	1	RSVD





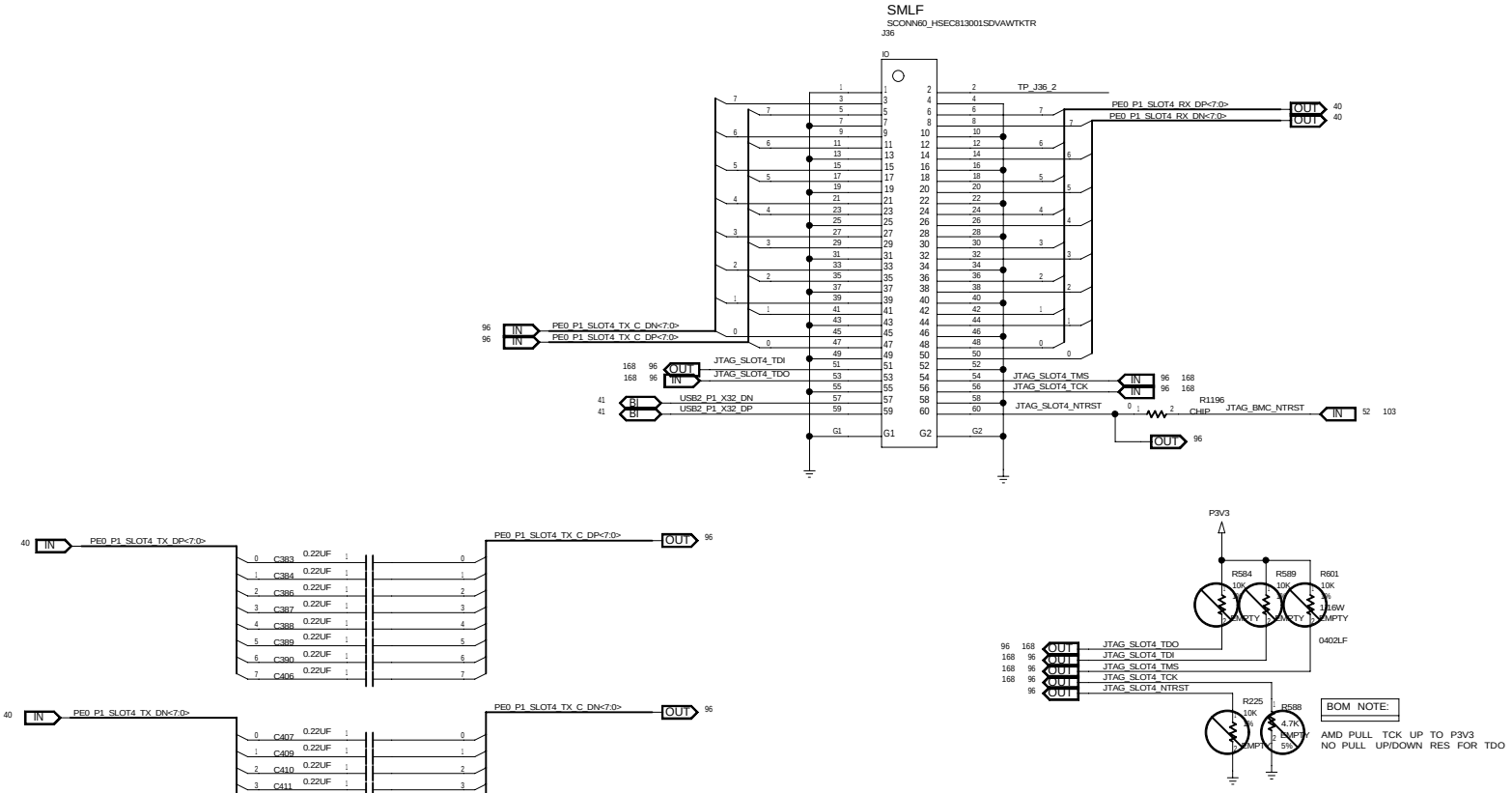


BOM NOTE:
N/A



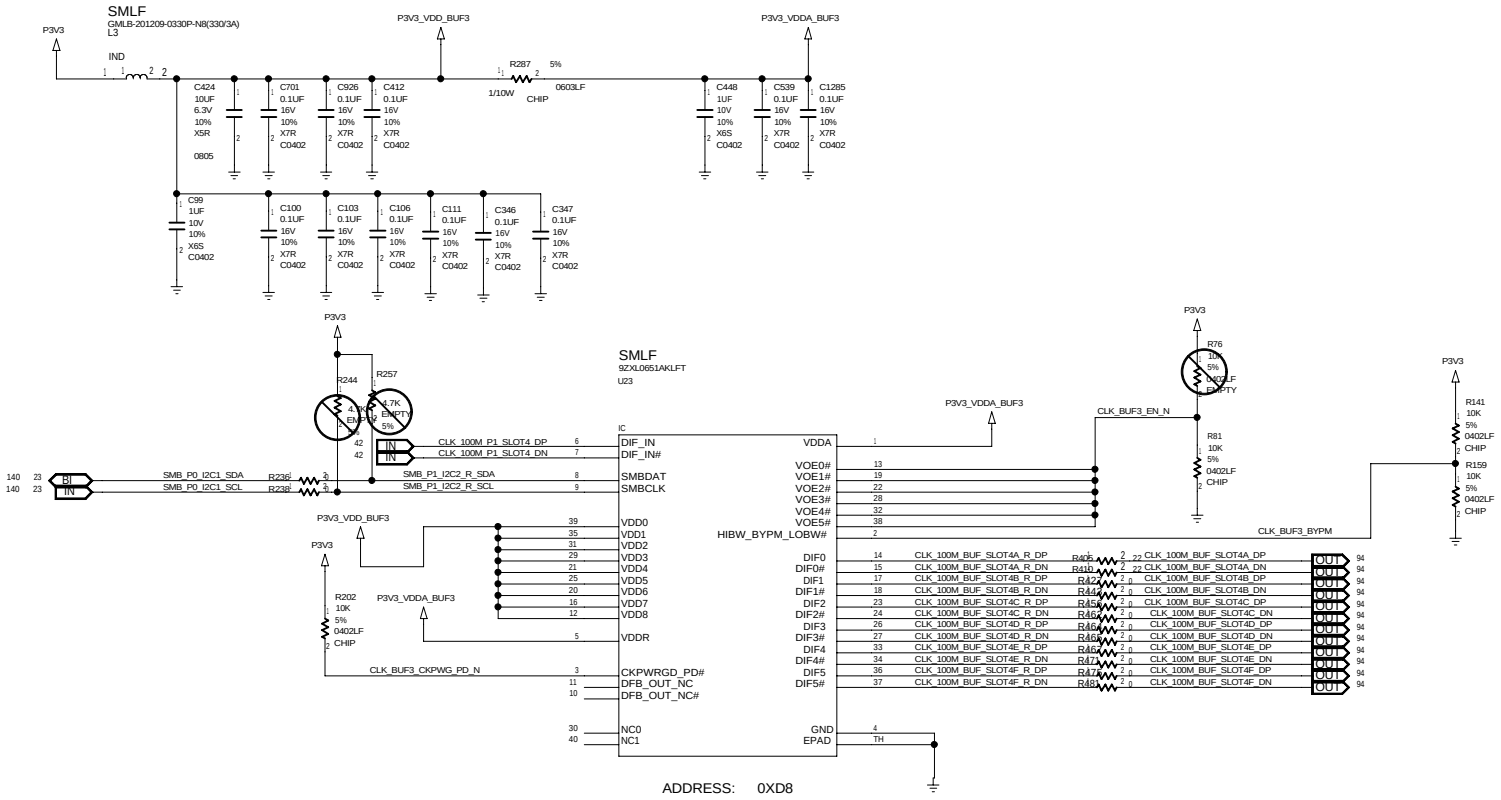
SLOT4 X32(2 OF 3)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
		REVIEWER:	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
		SIZE: C	DATE: Fri Dec 15 20:21:53 2017
			SHEET 95 OF 226



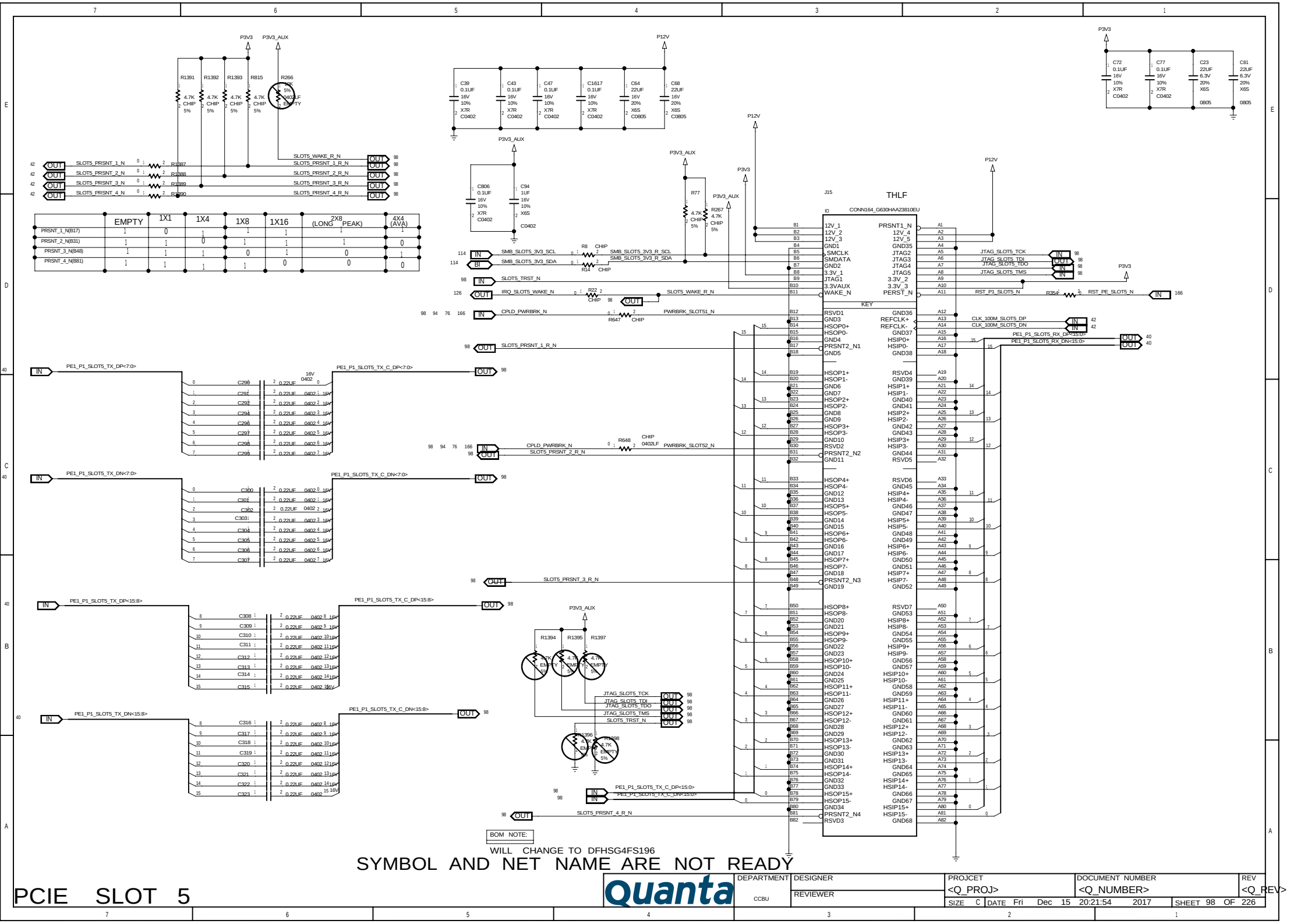
SLOT4 X32(3 OF 3)

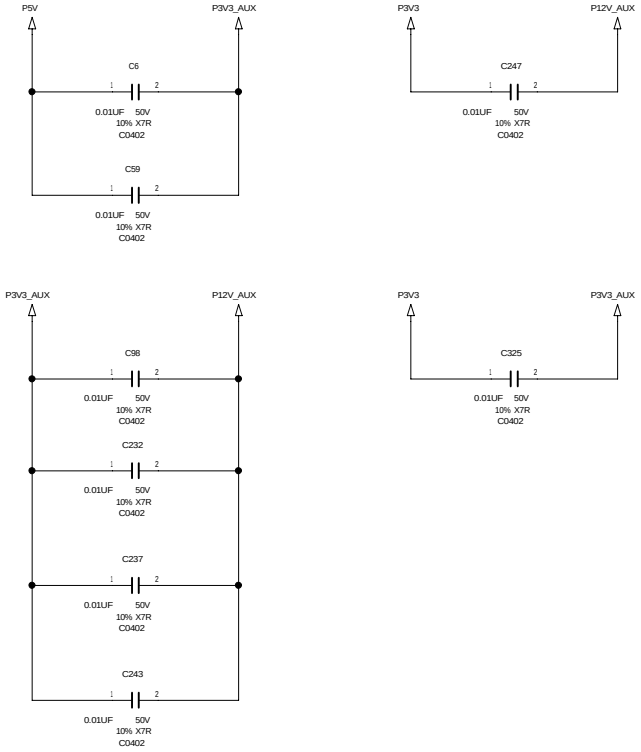
Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:53 2017	SHEET 96 OF 226



Clock BUFFER For Slot4

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER:	SIZE: C DATE: Fri Dec 15 20:21:53 2017	REV: <Q_REV>
				SHEET 97 OF 226

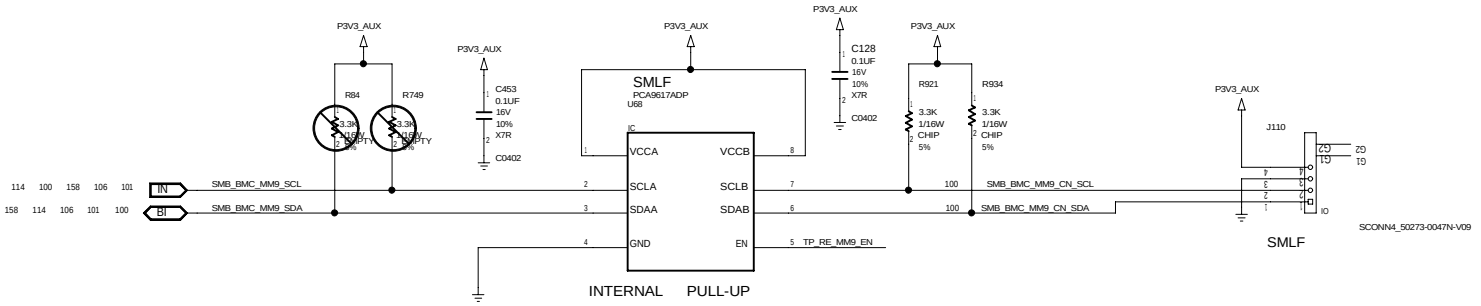

THLF
J15
CONN164_G630HAA23810EU
KEY
SYMBOL AND NET NAME ARE NOT READY
BOM NOTE:
WILL CHANGE TO DFHSG4FS196
PCIE SLOT 5
Quanta
DEPARTMENT
CCBU
DESIGNER
REVIEWER
PROJCET
<Q_PROJ>
DOCUMENT NUMBER
<Q_NUMBER>
REV
<Q_REV>
SIZE C
DATE Fri Dec 15 20:21:54 2017
SHEET 98 OF 226

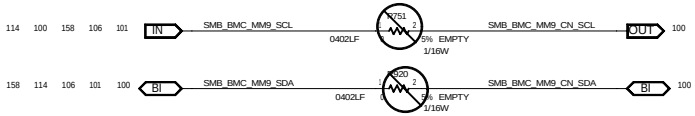


STITCHING CAP

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER	SIZE C DATE Fri Dec 15 20:21:54 2017	REV: <Q_REV>
				SHEET 99 OF 226

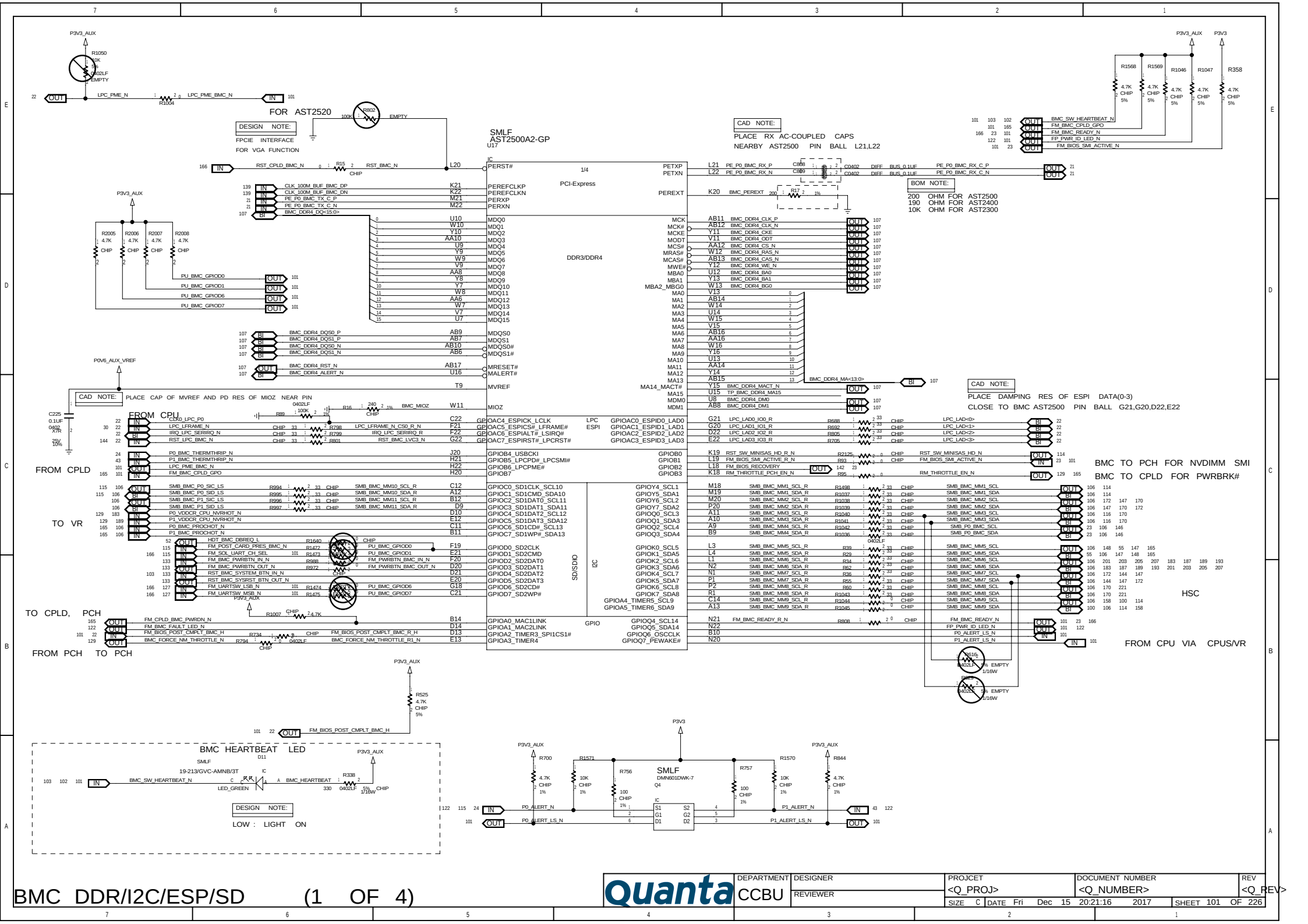
I2C REPEATER(FOR ESD)





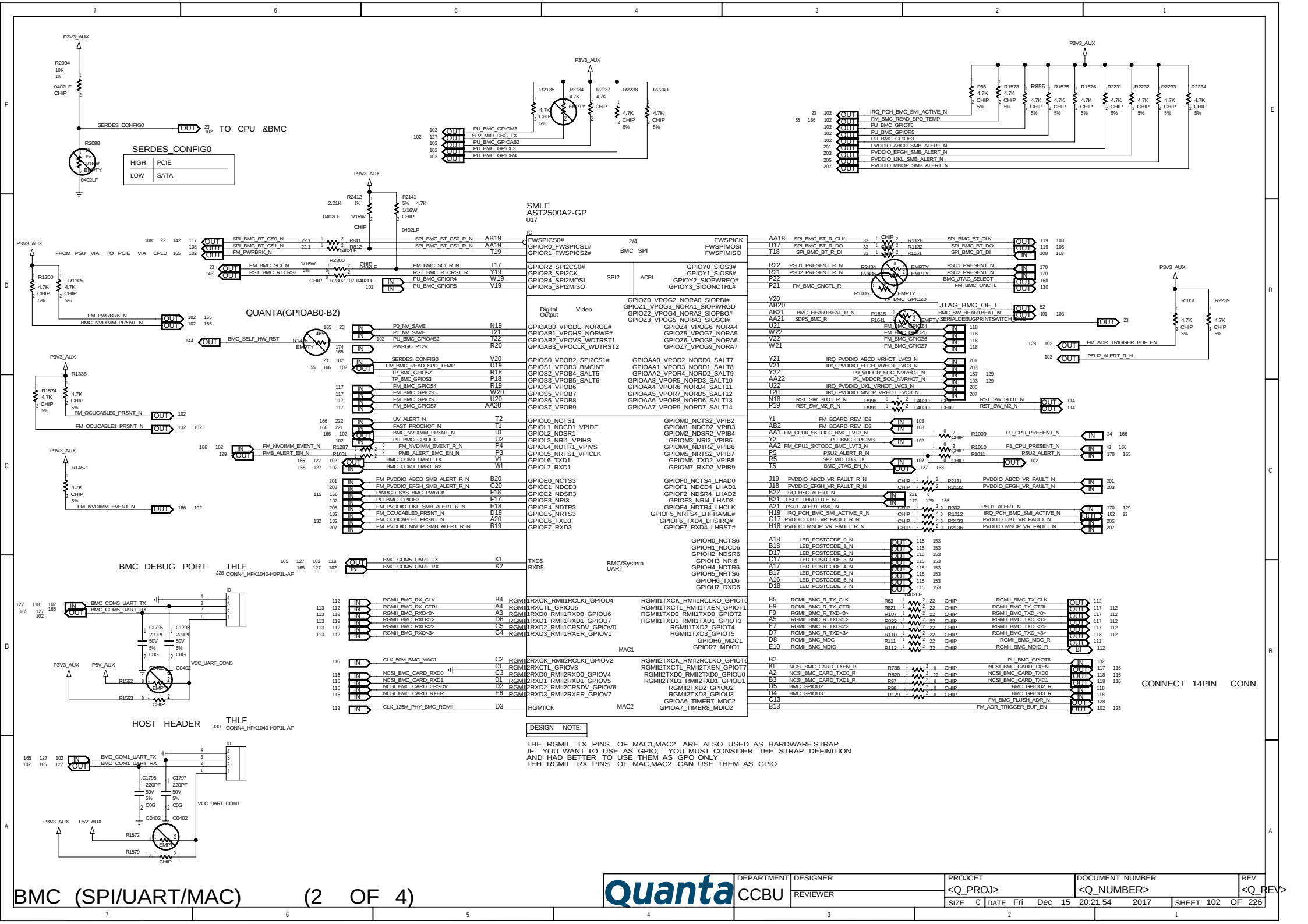
2U I2C EXPANDER

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
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			SIZE: C DATE: Fri Dec 15 20:21:54 2017	SHEET 100 OF 226



BMC DDR/I2C/ESP/SD (1 OF 4)

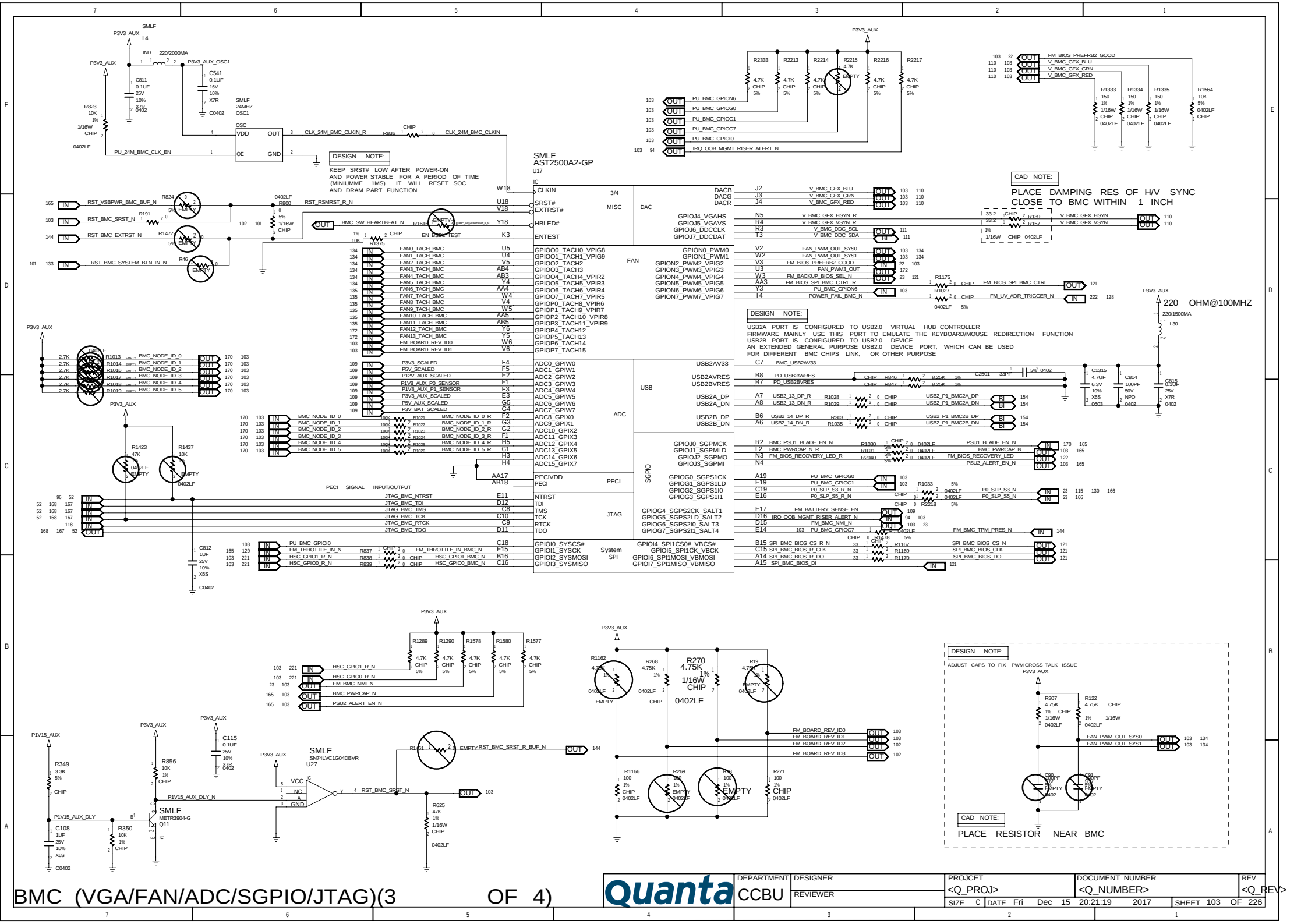
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REV: <Q_REV>	SIZE: C	DATE: Fri Dec 15 20:21:16 2017	SHEET 101 OF 226

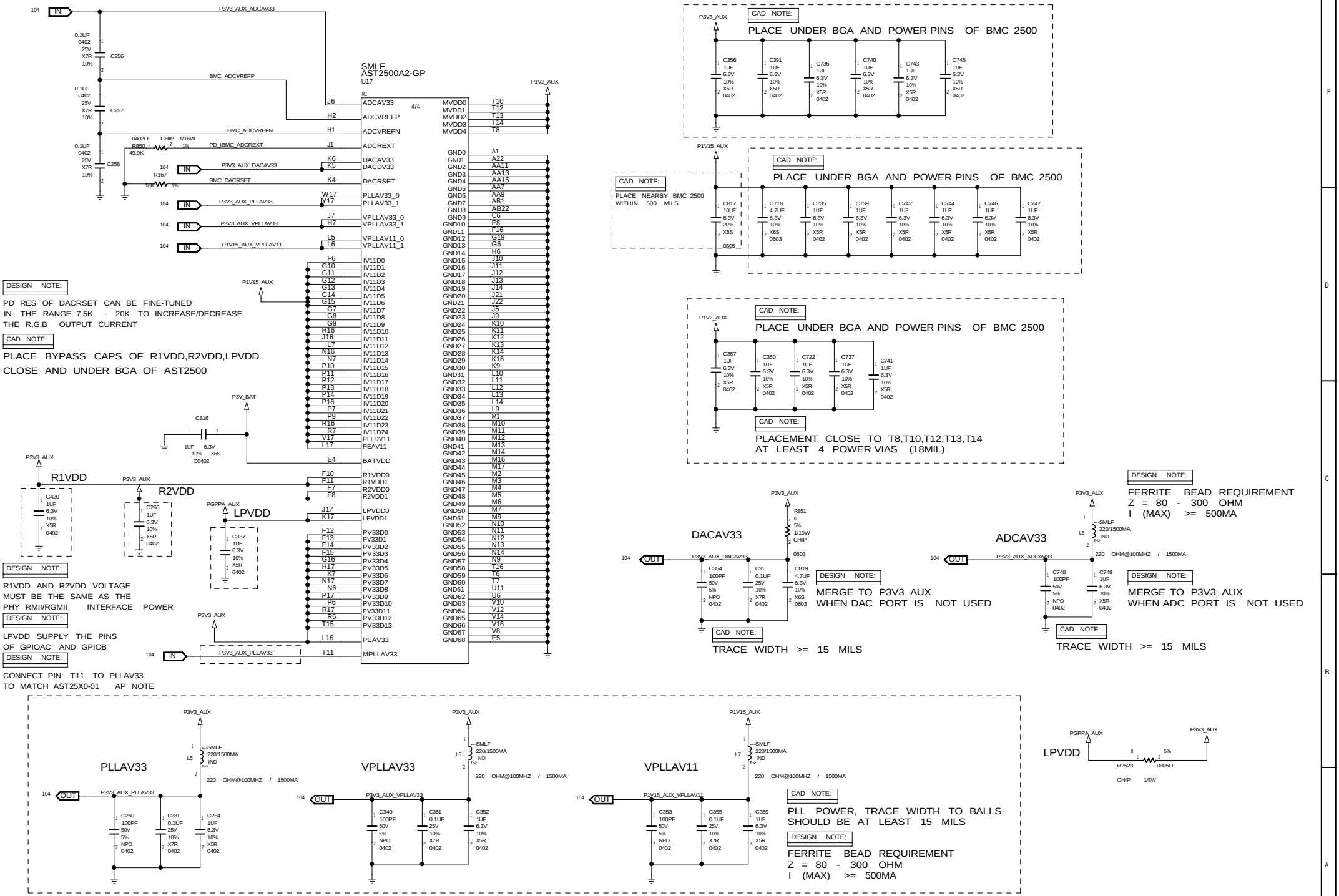


BMC (SPI/UART/MAC) (2 OF 4)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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SMLF
AST2500A2-GP
U17
DESIGN NOTE:
KEEP SRST# LOW AFTER POWER-ON AND POWER STABLE FOR A PERIOD OF TIME (MINIUMME 1MS). IT WILL RESET SOC AND DRAM PART FUNCTION
CAD NOTE:
PLACE DAMPING RES OF H/V SYNC CLOSE TO BMC WITHIN 1 INCH
DESIGN NOTE:
USB2A PORT IS CONFIGURED TO USB2.0 VIRTUAL HUB CONTROLLER
FIRMWARE MAINLY USE THIS PORT TO EMULATE THE KEYBOARD/MOUSE REDIRECTION FUNCTION
USB2B PORT IS CONFIGURED TO USB2.0 DEVICE
AN EXTENDED GENERAL PURPOSE USB2.0 DEVICE PORT, WHICH CAN BE USED FOR DIFFERENT BMC CHIPS LINK, OR OTHER PURPOSE
220 OHM@100MHZ
DESIGN NOTE:
ADJUST CAPS TO FIX PWM CROSS TALK ISSUE
CAD NOTE:
PLACE RESISTOR NEAR BMC
BMC (VGA/FAN/ADC/SGPIO/JTAG)(3 OF 4)
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
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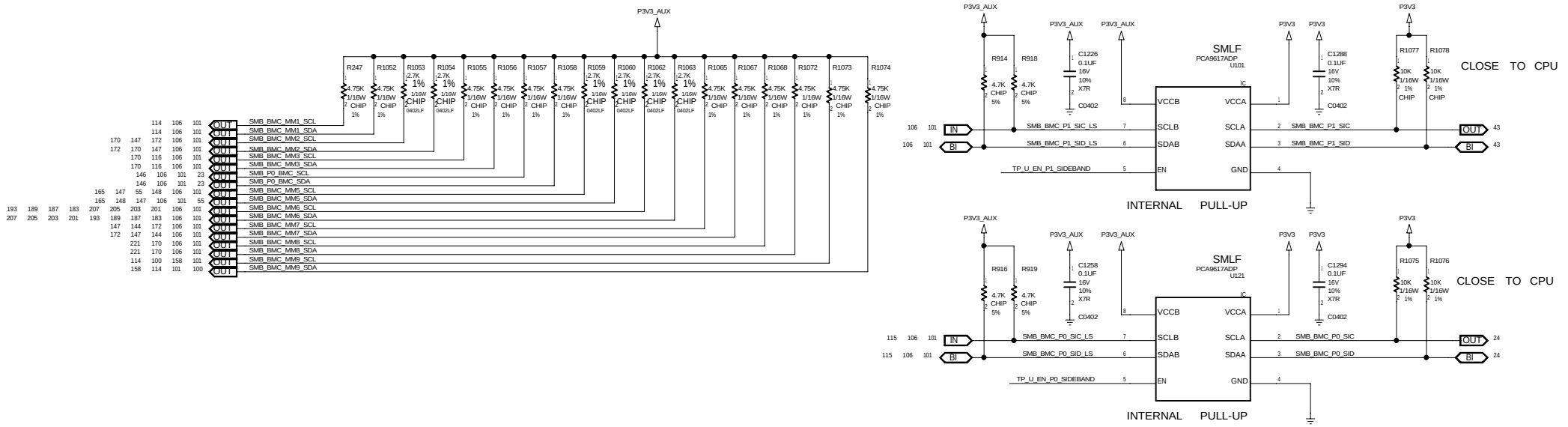


BMC POWER (4 OF 4)

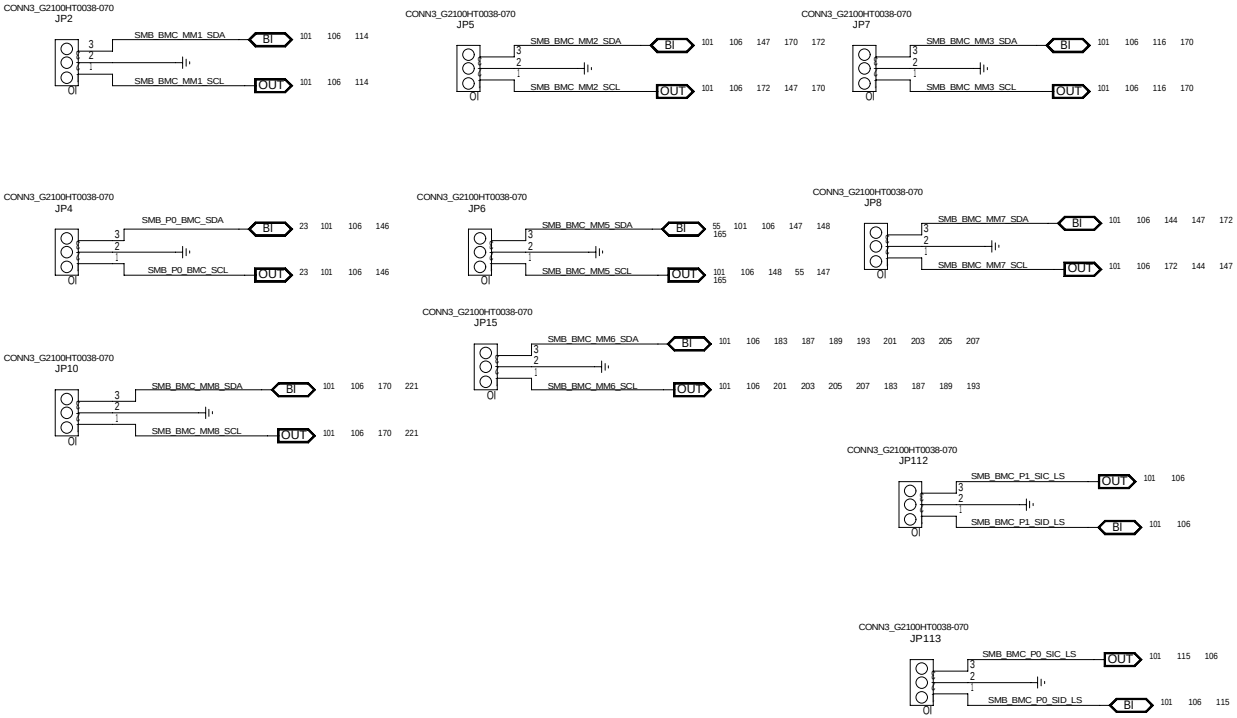
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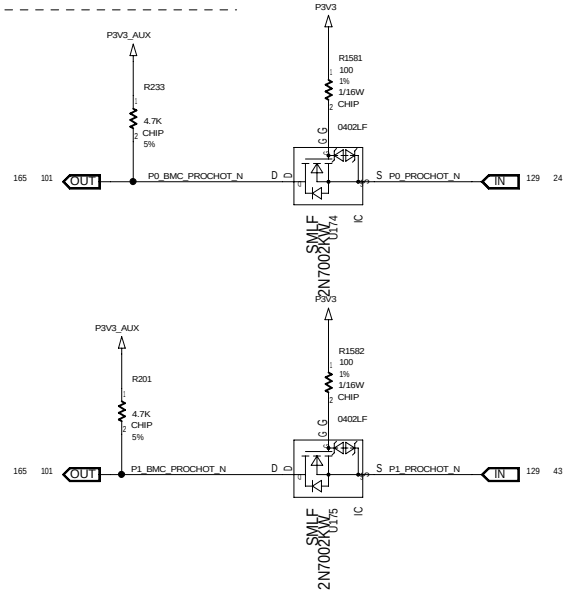
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			SIZE C	DATE Fri Dec 15 19:34:03 2017	SHEET 105 OF 226



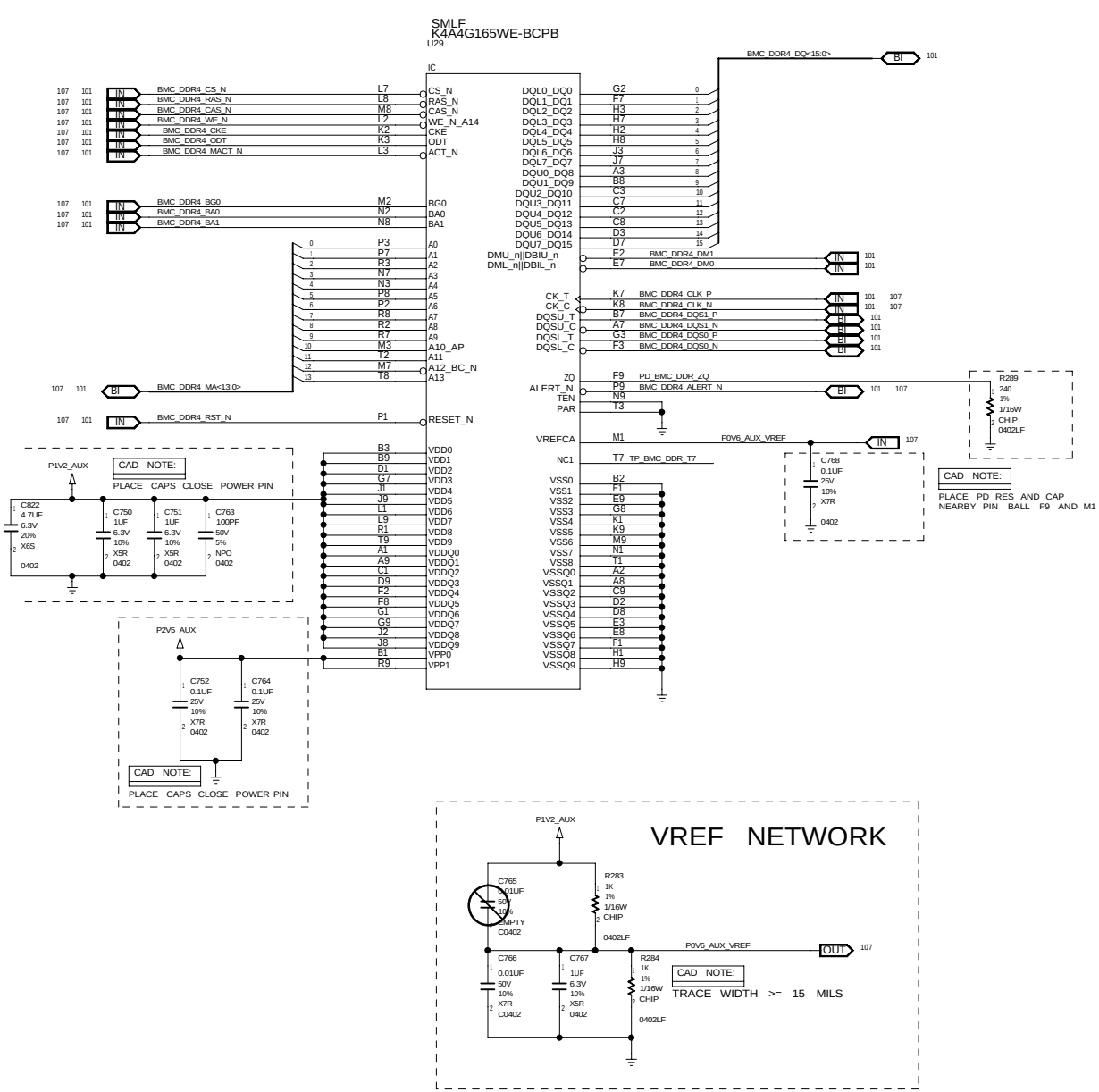
SMBUS PULL-UP RESISTORS

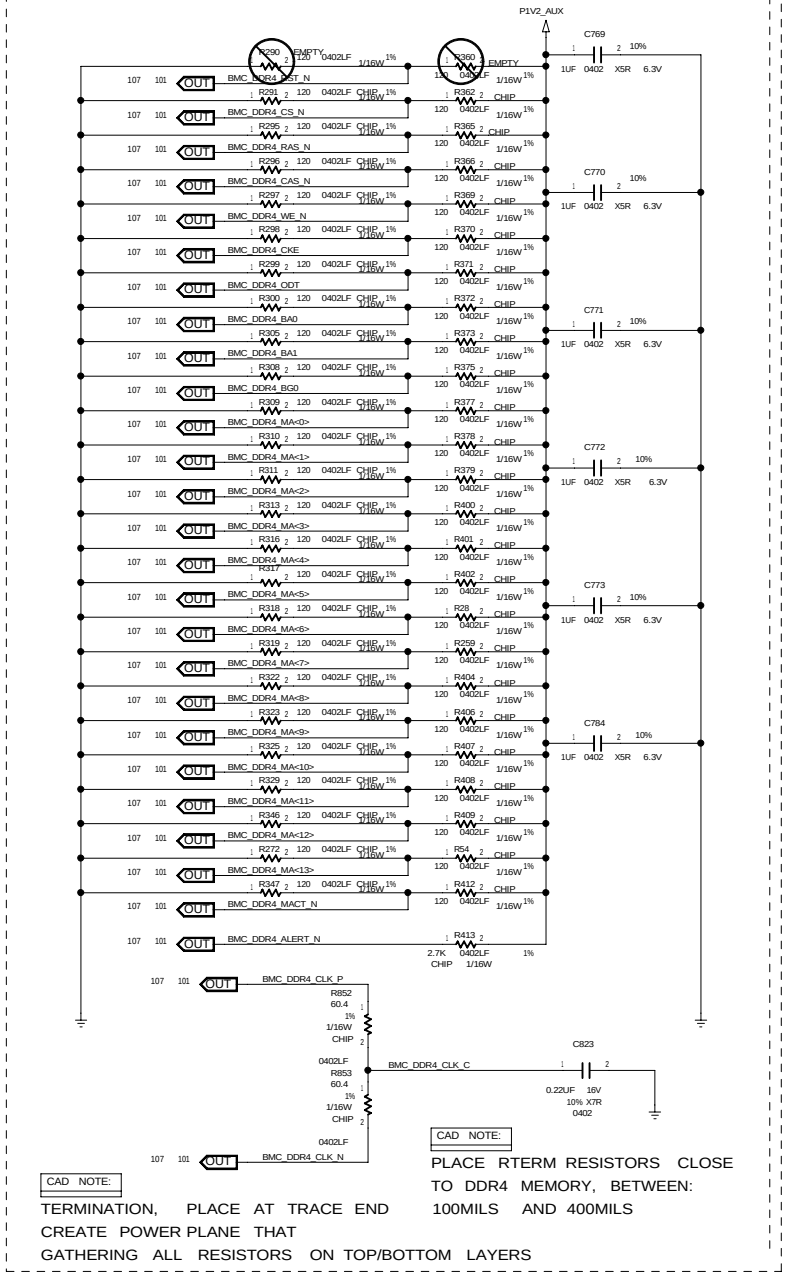




SMBus PULL UP/DOWN RES & Debug CONN

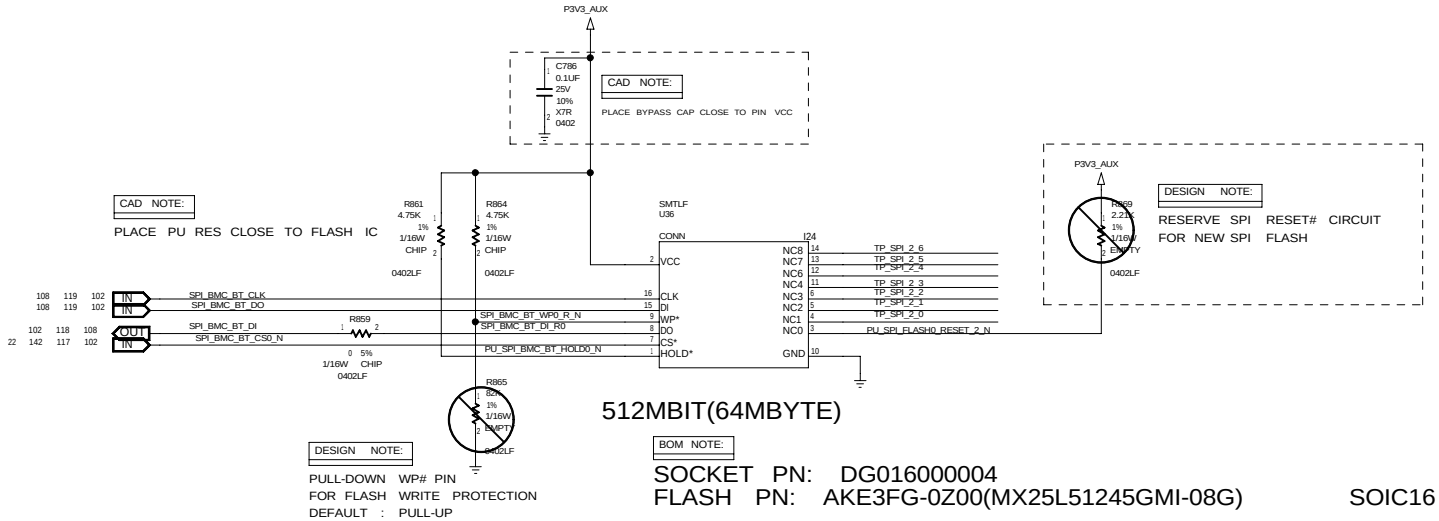
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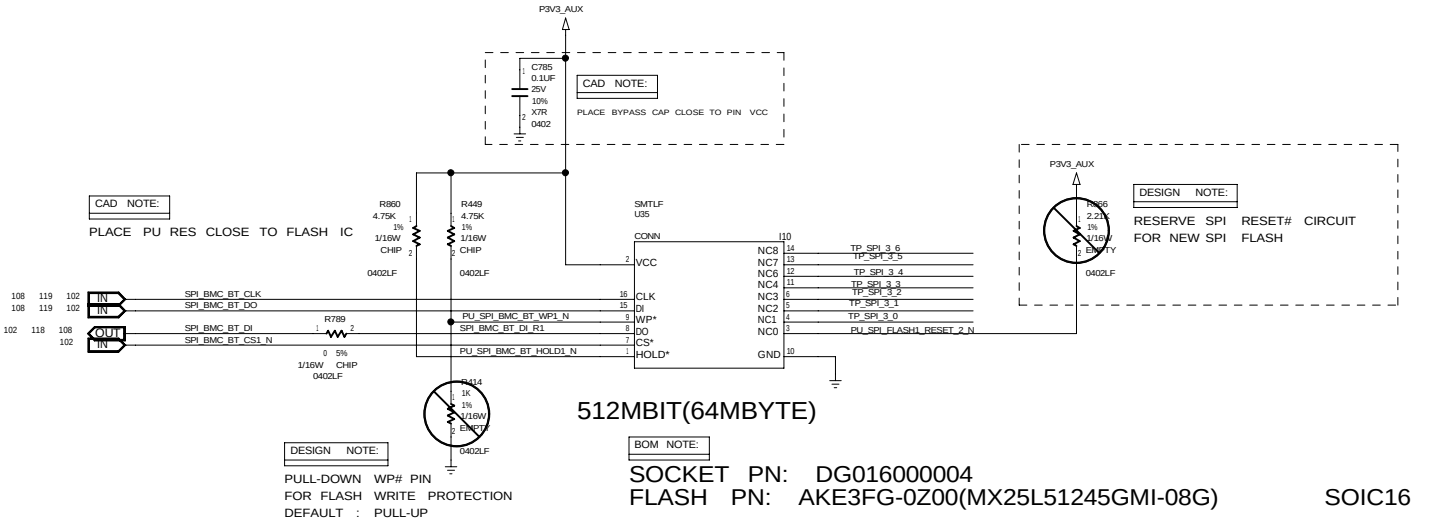




BMC DDR4 SDRAM

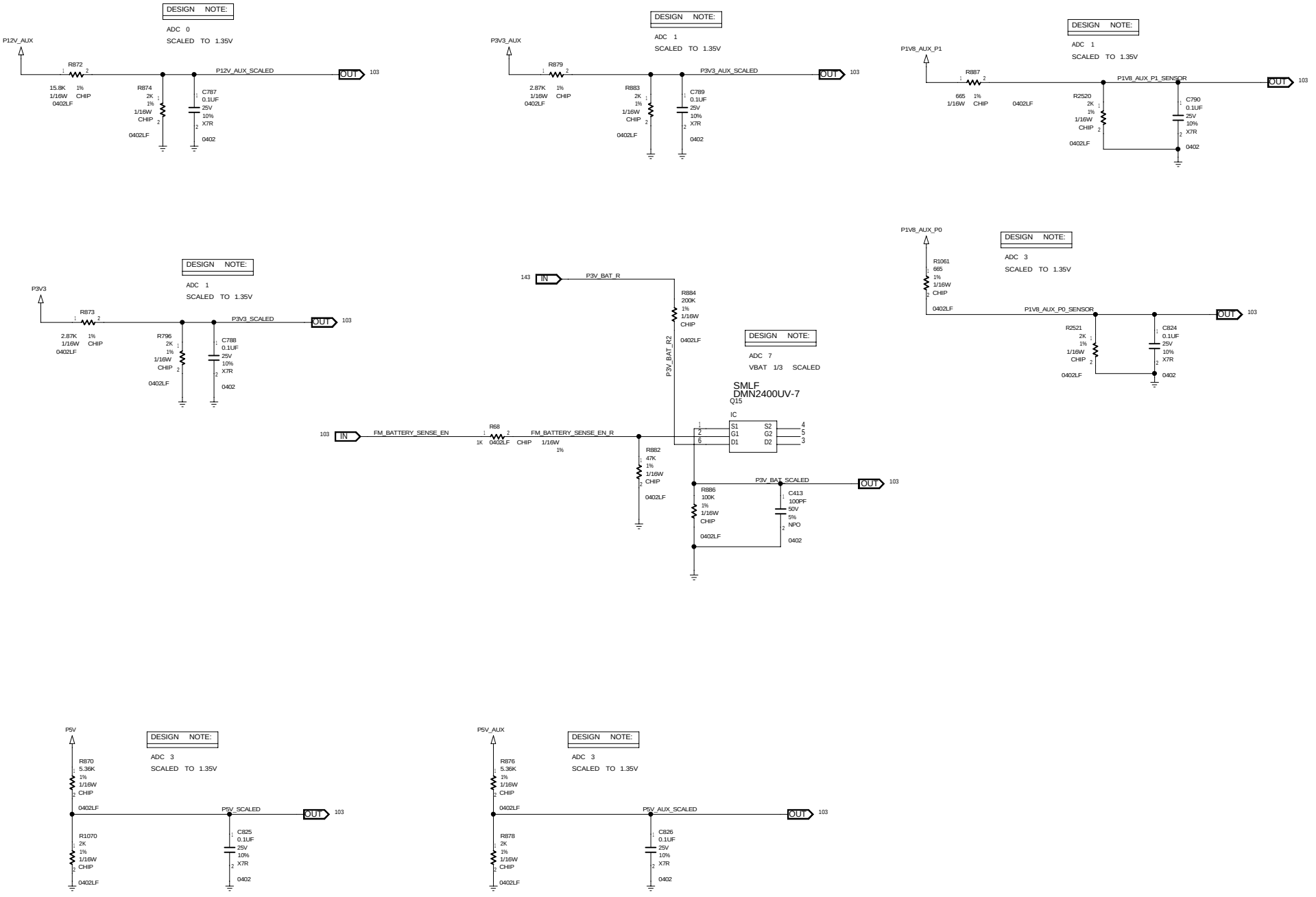
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		REVIEWER	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
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BMC BOOT FLASH(DUAL)

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CAD NOTE:

ROUTE ALL ADC NETS AT 6 MILS WIDE

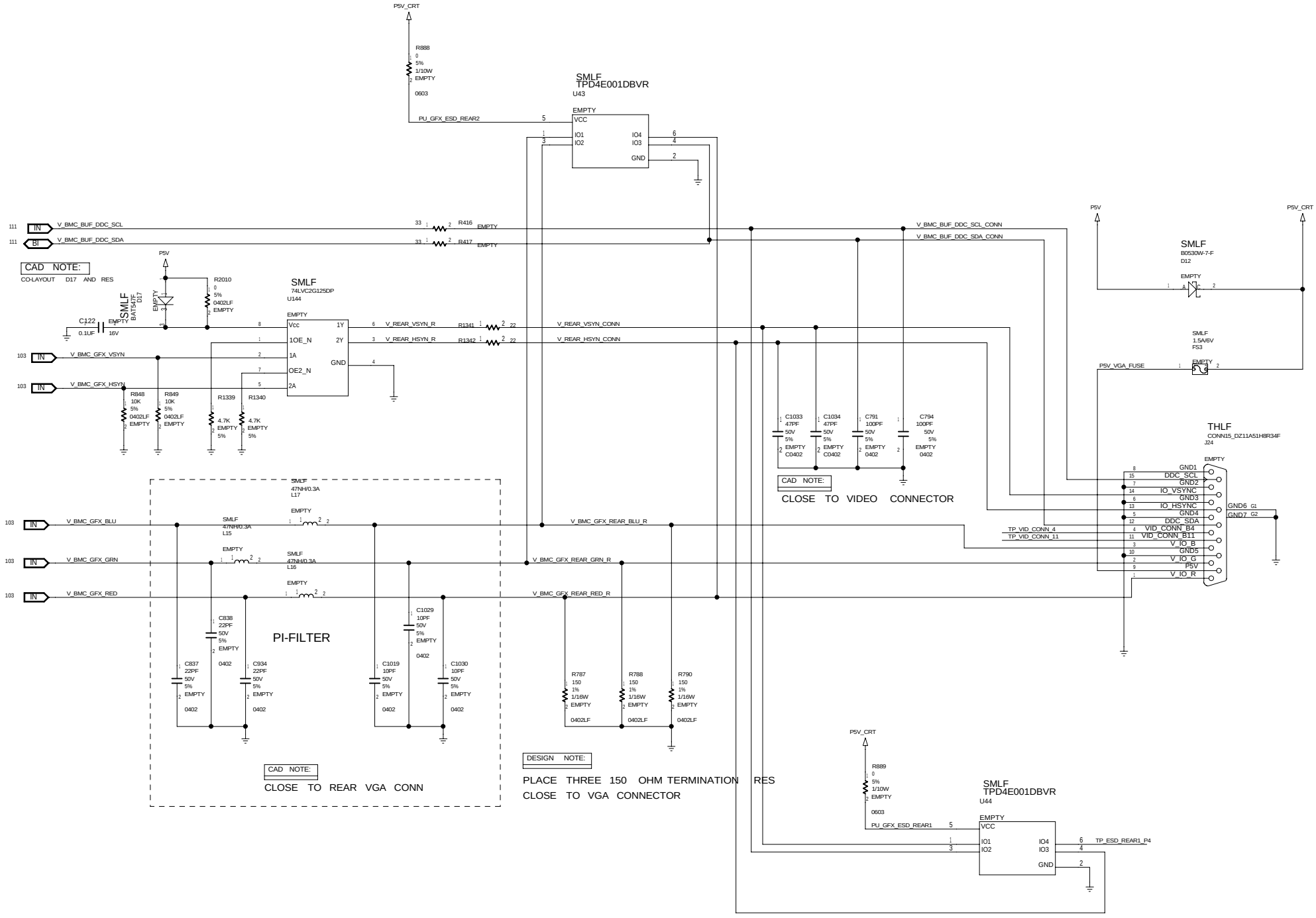
DESIGN NOTE:

ADC INPUT VOLTAGE RANGE : 0-1.8V

A GOOD NOMINAL INPUT VOLTAGE OF 3/4 VIN_MAX = 1.35V

BMC VOTAGE SENSOR

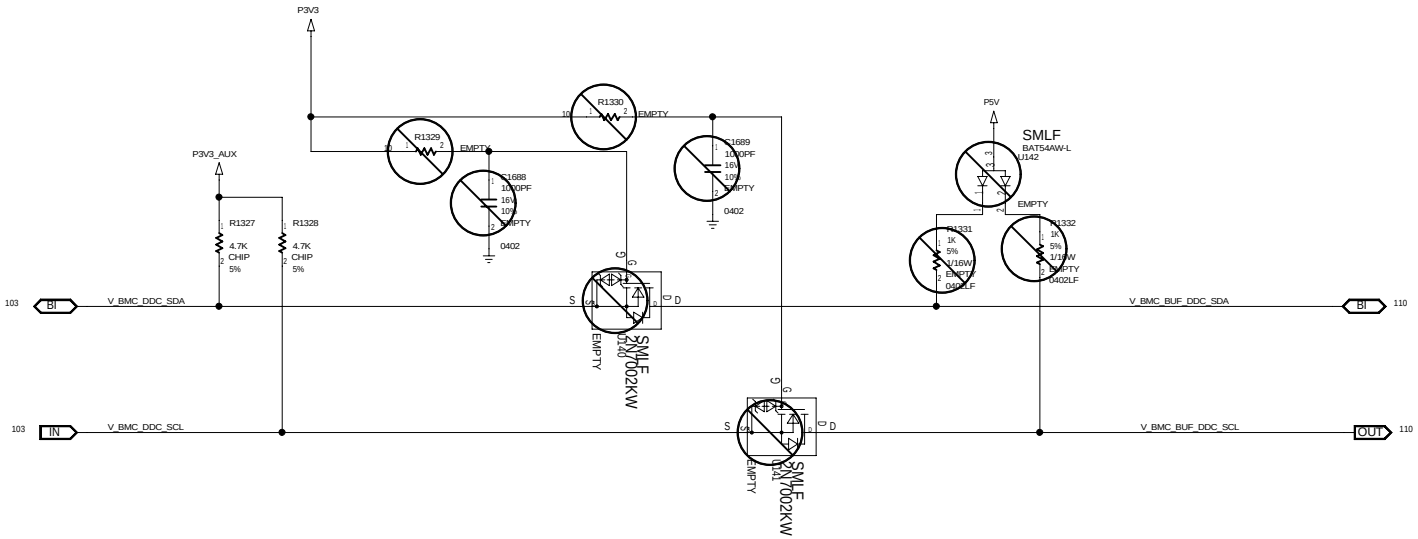
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		REVIEWER		REV: <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:55 2017	SHEET 109 OF 226



BMC VGA CONN

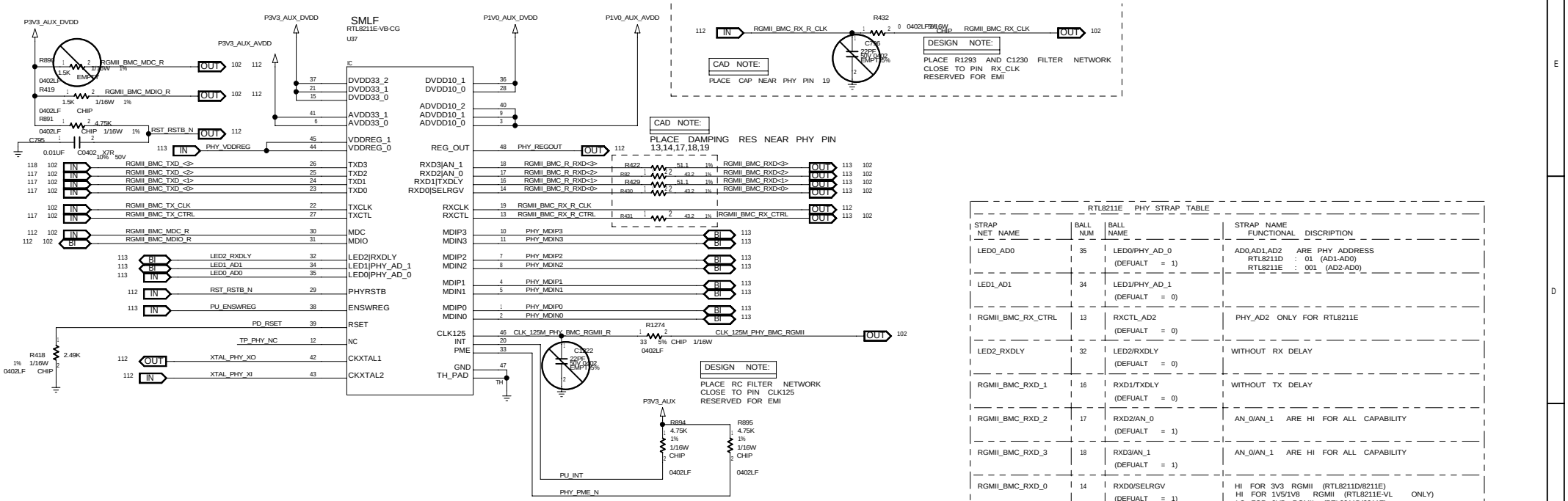
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		REVIEWER	SIZE: C DATE: Fri Dec 15 20:21:16 2017	SHEET 110 OF 226

REV: <Q_REV>



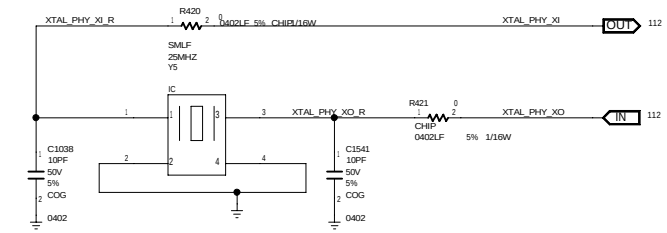
BMC DDC SMBUS ISOLATORS

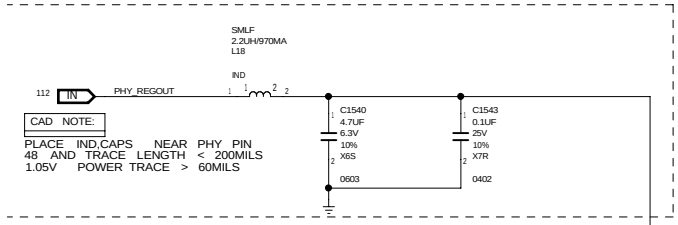
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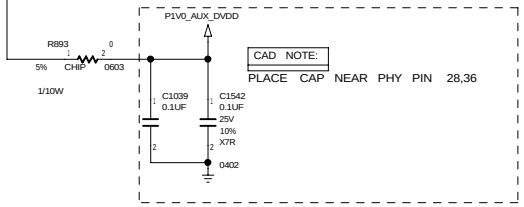


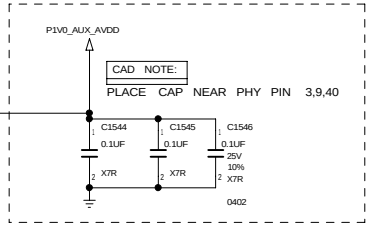
RTL8211E PHY STRAP TABLE

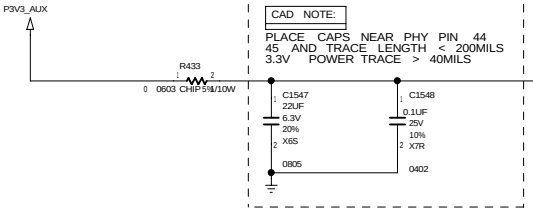
STRAP NET NAME	BALL NUM	BALL NAME	STRAP NAME FUNCTIONAL DISCRIPTION
LED0_AD0	35	LED0/PHY_AD_0 (DEFUALT = 1)	AD0,AD1,AD2 ARE PHY ADDRESS RTL8211D : 01 (AD1-AD0) RTL8211E : 001 (AD2-AD0)
LED1_AD1	34	LED1/PHY_AD_1 (DEFUALT = 0)	
RGMII_BMC_RX_CTRL	13	RXCTL_AD2 (DEFUALT = 0)	PHY_AD2 ONLY FOR RTL8211E
LED2_RXDLY	32	LED2/RXDLY (DEFUALT = 0)	WITHOUT RX DELAY
RGMII_BMC_RXD_1	16	RXD1/TXDLY (DEFUALT = 0)	WITHOUT TX DELAY
RGMII_BMC_RXD_2	17	RXD2/AN_0 (DEFUALT = 1)	AN_0/AN_1 ARE HI FOR ALL CAPABILITY
RGMII_BMC_RXD_3	18	RXD3/AN_1 (DEFUALT = 1)	AN_0/AN_1 ARE HI FOR ALL CAPABILITY
RGMII_BMC_RXD_0	14	RXD0/SELRGV (DEFUALT = 1)	HI FOR 3V3 RGMII (RTL8211D/8211E) HI FOR 1V5/1V8 RGMII (RTL8211E-VL ONLY) LO FOR 2V5 RGMII (RTL8211D/8211E)

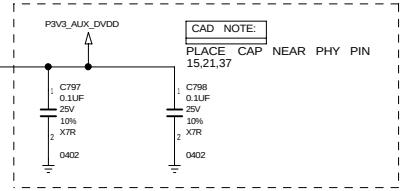


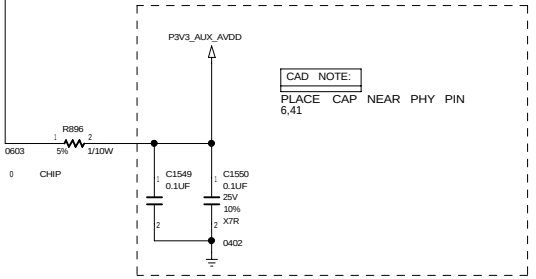


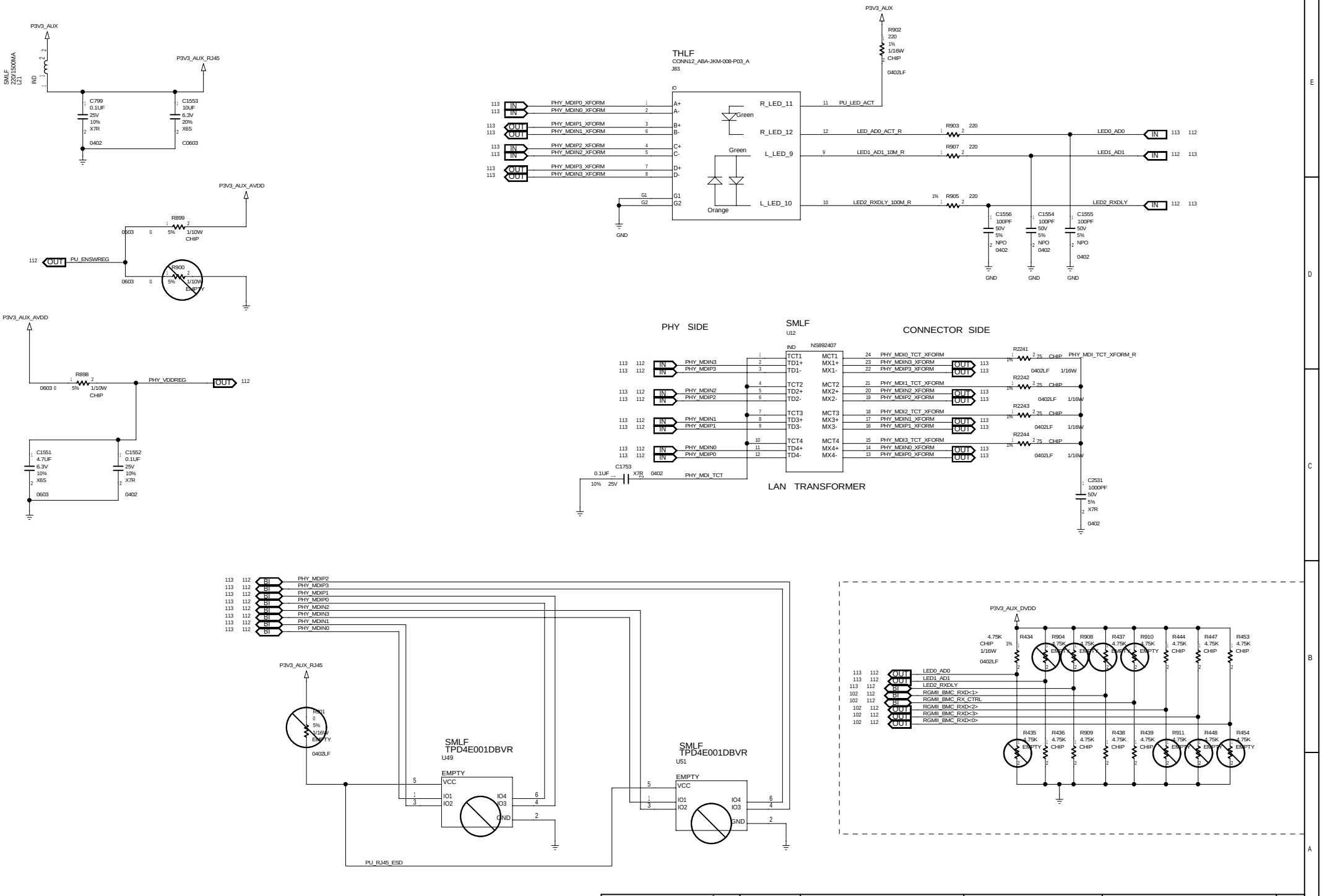






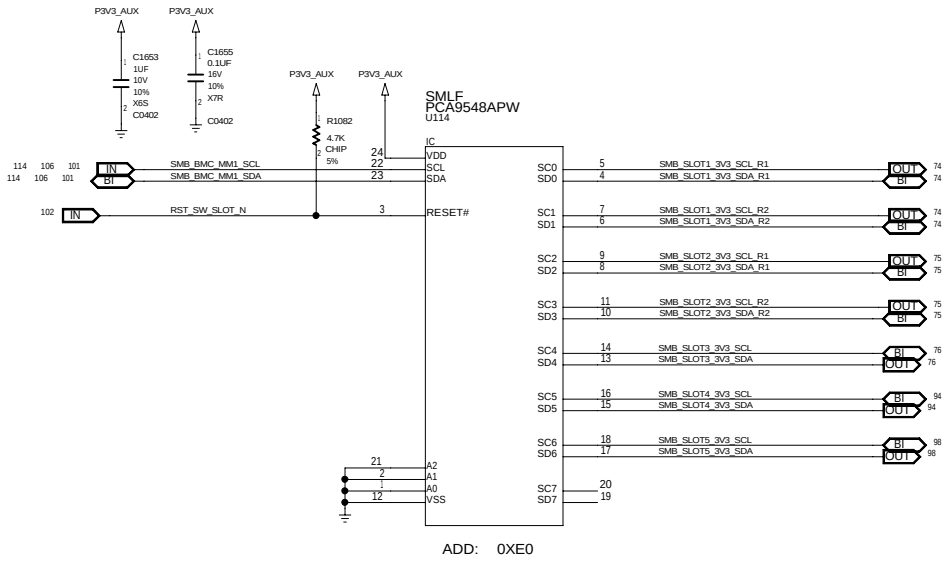


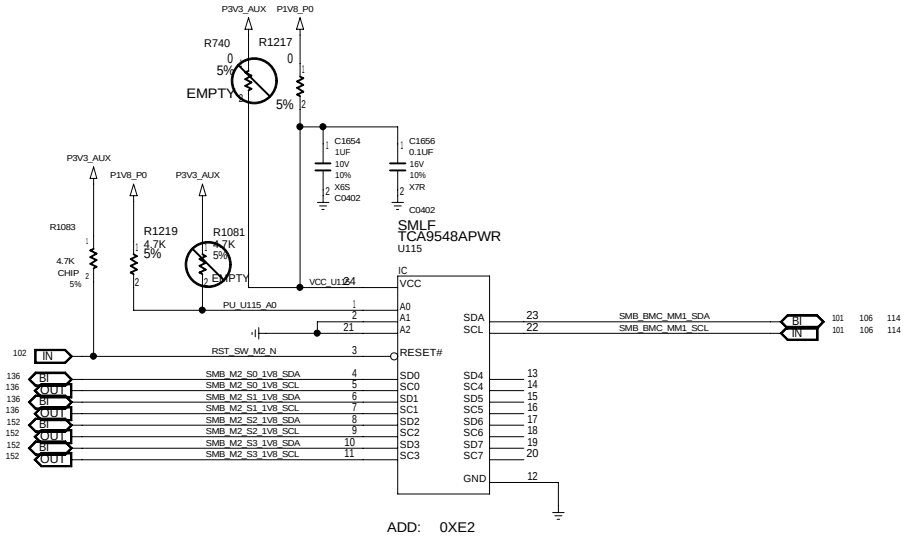


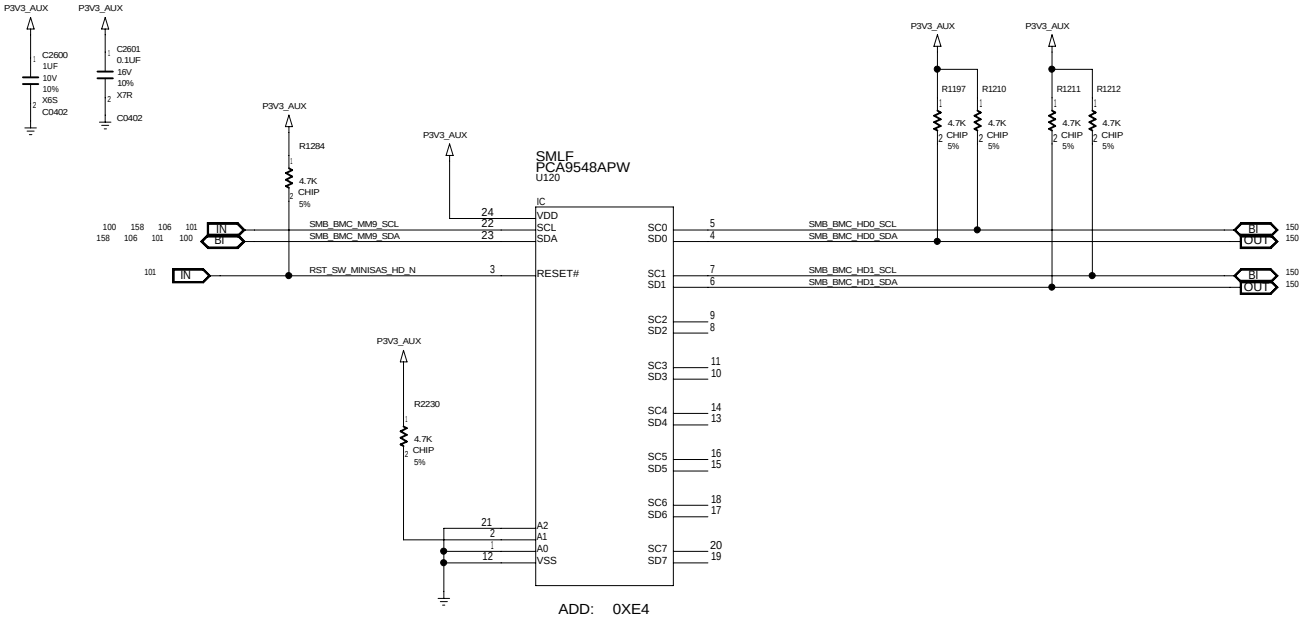


BMC 1GB PHY (2 OF 2)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>
		REVIEWER:	DOCUMENT NUMBER: <Q_NUMBER>
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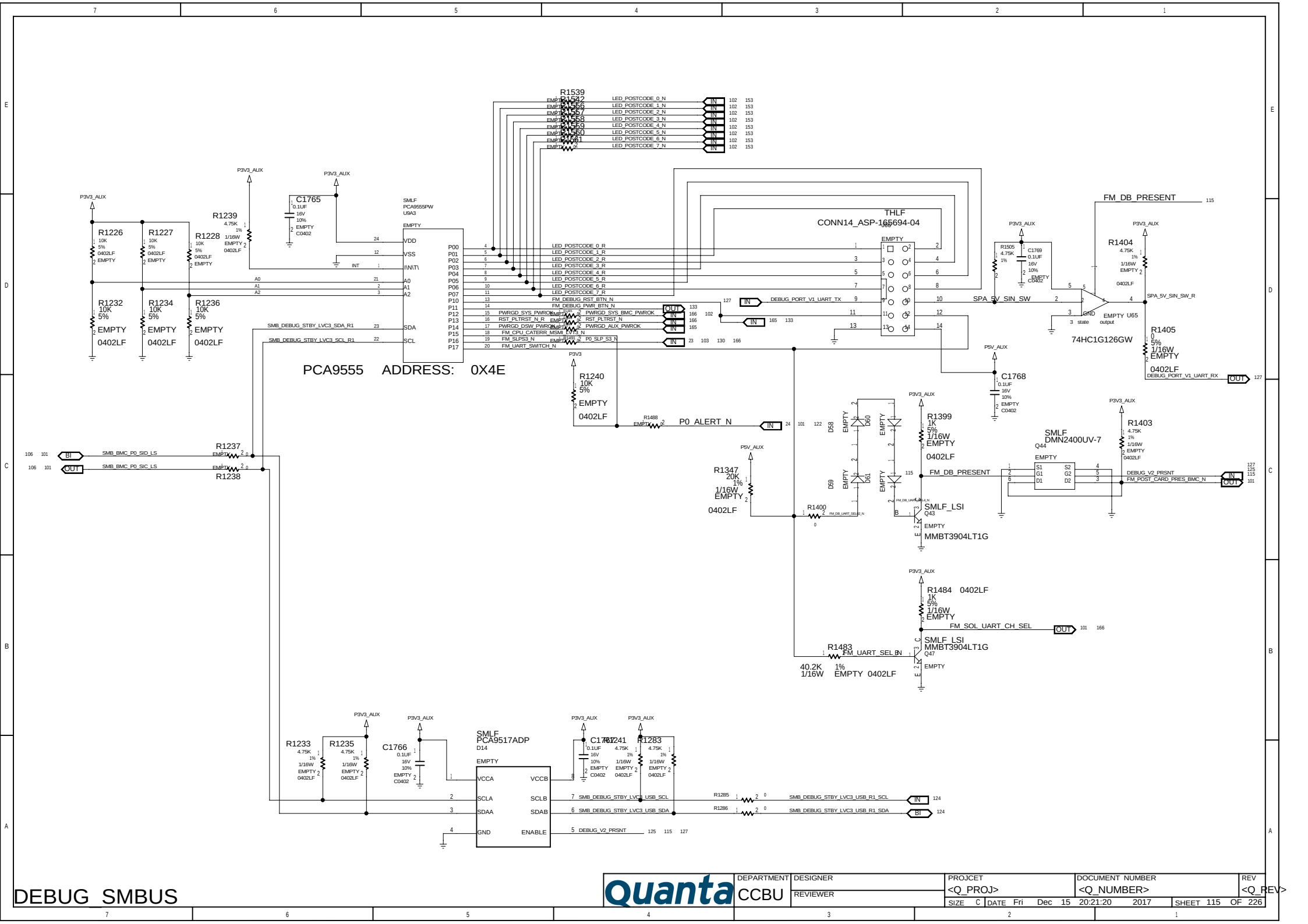






SMBUS SWITCH FOR PCIe slots

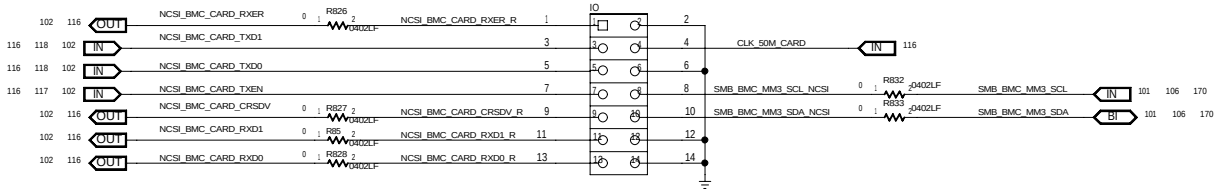
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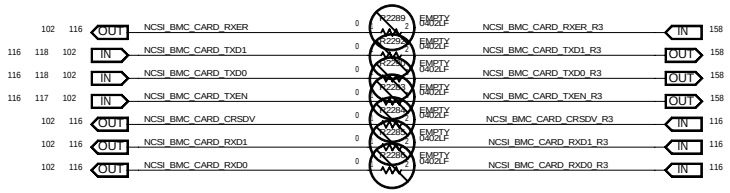
DEBUG_SMBUS

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>
DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>	SIZE: C	DATE: Fri Dec 15 20:21:20 2017
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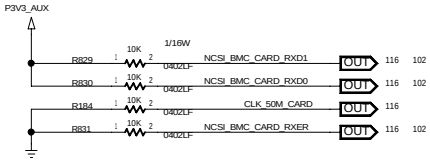
THLF
CONN14_52S-H90-14GBE0
J89

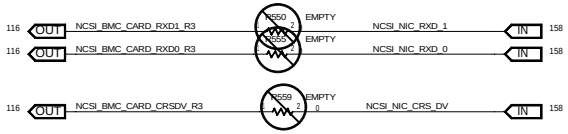


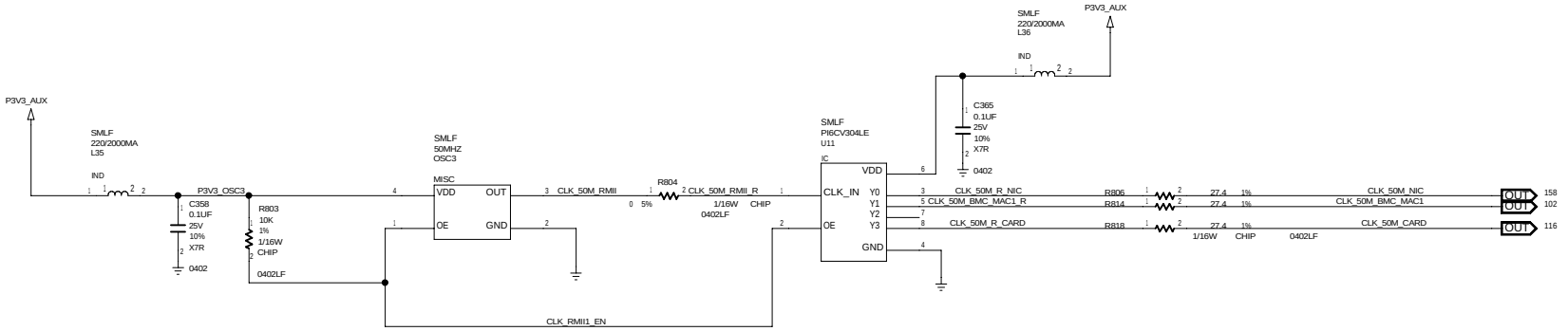
NCSI Connector				
Pin	Signal	I/O	Voltage	Description
1	RXER	O	3.3V	Enable signal from Rack Manager to HSC on the Blade
2	GND	I	0V	Ground
3	TXD1	I	3.3V	Transmit Data from BMC to NIC
4	CLK_50M	I	0V	50Mhz Clock
5	TXD0	I	3.3V	Transmit Data from BMC to NIC
6	GND	I	0V	Ground
7	TXEN	I	3.3V	Transmit Enable from BMC to NIC
8	GND	I	0V	Ground
9	CRSDV	O	3.3V	Receive carrier sense and data valid from NIC to BMC
10	GND	I	0V	Ground
11	RXD1	O	3.3V	Receive Data from NIC to BMC
12	GND	I	0V	Ground
13	RXD0	O	3.3V	Receive Data from NIC to BMC
14	GND	I	0V	Ground



CAD NOTE:
PLACE SEVEN RESISTORS CLOSE CONNECTOR WITHIN 0.5"







TO NIC
TO AST2500 MAC1
TO CONN

NCSI CONN

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DESIGN NOTE: BIT 0 (DEDICATED STRAP PIN)
BALL NAME: FWSPICS0#

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DISABLE CPU BOOT	AB19	SPI_BMC_FW_CS0_N	PU

STRAP VALUE = INVERSE OF INPUT	DESCRIPTION	INPUT LEVEL
STRAP VALUE= 0(DEFAULT)	ENABLE BMC	PU
STRAP VALUE= 1	DISABLE BMC	PD

P3V3_AUX — 0402LF R922 2.21K 1% 1/16W CHIP — SPI_BMC_BT_CS0_N — OUT 102 142 22 108

DESIGN NOTE:
TO PCH GPIO AND BIOS CONTROL, IF BMC DISABLE, BIOS IS HIGH ACTIVITY

DESIGN NOTE: BIT 12 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXD0
INTERNAL PD

DESIGN NOTE: BIT 13 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXD1
INTERNAL PD

RGMII_BMC_TXD_<0> — OUT 102 112 — R265 4.7K CHIP 5%
RGMII_BMC_TXD_<1> — OUT 102 112 — R275 4.7K CHIP 5%

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SPI MODE SELECTION	F9,A5	RMII_BMC_LOM_MEZZ_TXD<0> RMII_BMC_LOM_MEZZ_TXD<1>	PD PD

13:12	DESCRIPTION
00(DEFAULT)	DISABLE SPI INTERFACE
01	ENABLE SPI MASTER
10	ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11	ENABLE SPI PASS-THROUGH

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 1 (NOT IN HW STRAP)
RESERVED

DESIGN NOTE: -STRAP VALUE=0,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 2.2K OHM
-STRAP VALUE=1,PULL DOWN THE PIN TO GROUND BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — CAD NOTE: PLACE THE PU RES CLOSE BMC PIN R19, AND ON THE TRACE TO REDUCE STUB — R520 EMPTY 3.3K 0402LF 5% 1/16W — FM_BMC_GPIOS4 — OUT 102

DESIGN NOTE: BIT 3 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS4

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
VGA MEMORY SIZE SELECTION	R19	FM_BMC_GPIOS4	PD

00	SELECT 8MB VGA MEMORY
01(DEFAULT)	SELECT 16MB VGA MEMORY
10	SELECT 32MB VGA MEMORY
11	SELECT 64MB VGA MEMORY

DEFINED THE VGA MEMORY SIZE THAT WILL SHARE WITH SOC MEMORY
ASTPPED COMMENT:
FOR AST2500,IT ONLY REQUIRES 16MB TO SUPPORT ALL RESOLUTIONS.
THIS STRAPIS RESERVED FOR AST2510
WHICH IS VGA ONLY SKEW TO CHOOSE 64MB SIZE

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 4 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS5

P3V3_AUX — CAD NOTE: AND ON THE TRACE TO REDUCE STUB — R543 EMPTY 3.3K 0402LF 1/16W — FM_BMC_GPIOS5 — OUT 102

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
RESERVED (1)	W20	FM_BMC_GPIOS5	PD

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — CAD NOTE: PLACE THE PU RES CLOSE BMC PIN U20, AND ON THE TRACE TO REDUCE STUB — R521 EMPTY 3.3K — FM_BMC_GPIOS6 0402LF 1/16W — OUT 102 — R858 3.3K 5% 1/16W EMPTY 0402LF

DESIGN NOTE: BIT 5 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS6

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE DEDICATED VGA BIOS ROM	U20	FM_BMC_GPIOS6	PD

0(DEFAULT)	NO VGA BIOS ROM,VGA BIOS IS MERGED IN THE SYSTEM BIOS
1	ENABLE DEDICATED VGA BIOS ROM

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — CAD NOTE: PLACE THE PU RES CLOSE BMC PIN E9, AND ON THE TRACE TO REDUCE STUB — R580 CHIP 4.99K 0402LF 5% 1/16W — RGMII_BMC_TX_CTRL — OUT 102 112

DESIGN NOTE: BIT 6 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXCTL

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DEFINE MAC#1 INTERFACE	E9	RGMII_BMC_TX_CTRL	PD

0(DEFAULT)	RMII/NCSI
1	RGMII

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — CAD NOTE: PLACE THE PU RES CLOSE BMC PIN B1, AND ON THE TRACE TO REDUCE STUB — R536 EMPTY 4.99K 0402LF 1/16W 5% — NCSI_BMC_CARD_TXEN — OUT 102 116 — R912 4.7K CHIP 5%

DESIGN NOTE: BIT 7 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII2TXCTL

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DEFINE MAC#2 INTERFACE	B1	NCSI_BMC_CARD_TXEN	PD

0	RMII/NCSI
1(DEFAULT)	RGMII

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 8 (NOT IN HW STRAP)
ENABLE SOFTWARE SECURE-BOOT TEST MODE

0(DEFAULT)	NORMAL MODE (DEFAULT)
1	ENABLE SECURE BOOT TEST

DESIGN NOTE: BIT 11:9 (NOT IN HW STRAP)
AXI/AHB CLOCK FREQUENCY RATIO SELECTION

11:9	DESCRIPTION
000	UNDEFINED
001(DEFAULT)	SELECT AXI:AHB= 2:1
010	SELECT AXI:AHB= 3:1
011	SELECT AXI:AHB= 4:1
100	SELECT AXI:AHB= 5:1
101	SELECT AXI:AHB= 6:1
110	SELECT AXI:AHB= 7:1
111	SELECT AXI:AHB= 8:1

HCLK FREQ=H-PLL/(RATIO_OF_CPU-AXI)(RATIO_OF_AXI-AHB)

DESIGN NOTE: BIT 14 (NOT IN HW STRAP)
SELECT DEDICATED LPC RESET INPUT

0	LPC RESET IS SHARED WITH PCIE RESET PIN
1(DEFAULT)	LPC RESET IS LOCATED AT PIN NUMBER G22,SHARED WITH GPIOAC7

P3V3_AUX — CAD NOTE: PLACE THE PU RES CLOSE BMC PIN AA20, AND ON THE TRACE TO REDUCE STUB — R750 CHIP 1/16W 3.3K 0402LF 5% — FM_BMC_GPIOS7 — OUT 102

DESIGN NOTE: BIT 15 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS7

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
VGA CLASS CODE SELECTION	AA20	FM_BMC_GPIOS7	PD

0	SELECT THE CLASS CODE FOR VIDEO DEVICE
1(DEFAULT)	SELECT THE CLASS CODE FOR VGA DEVICE

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — CAD NOTE: PLACE THE PU RES CLOSE BMC PIN E7, AND ON THE TRACE TO REDUCE STUB — R760 EMPTY 3.3K 0402LF 1/16W — RGMII_BMC_TXD_<2> 5% — R1552 3.3K 5% — OUT 102 112

DESIGN NOTE: BIT 16 (DEDICATED STRAP PIN)
BALL NAME: RGMII1TXD2

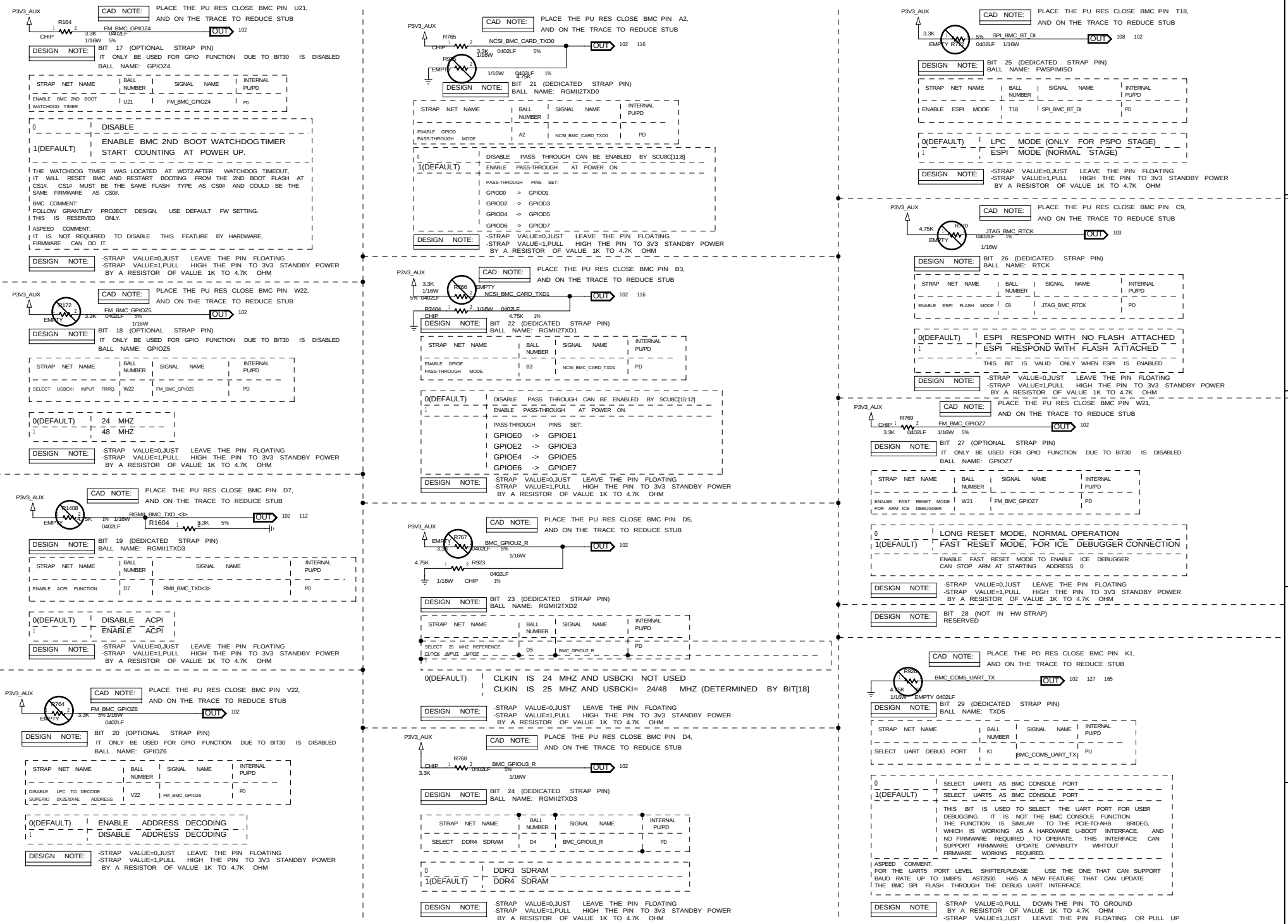
STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SUPERIO CONFIGURATION ADDRESS SELECTION	E7	RGMII_BMC_TXD_<2>	PD

0(DEFAULT)	DECODE 0X2E
1	DECODE 0X4E

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

BMC HW STRAPS (BIT 0-16)

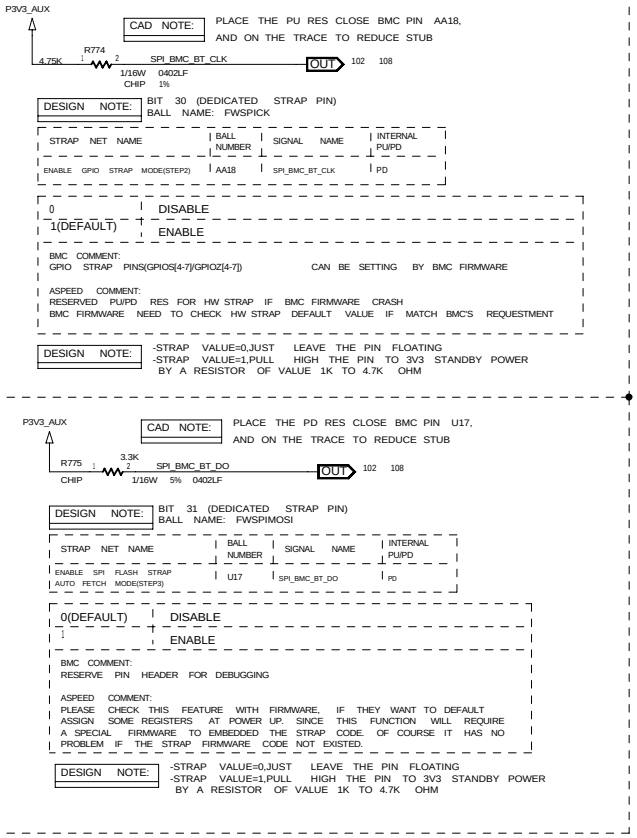
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
		REVIEWER	SIZE C DATE Fri Dec 15 20:21:56 2017	SHEET 117 OF 226



BMC HW STRAPS(BIT 17-29)

Quanta

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER	SIZE C	DATE Fri Dec 15 20:21:56 2017	SHEET 118 OF 226



DESIGN NOTE:

WHEN GPIO IS USED AS HARDWARE STRAP,
IT WILL CONSTRAIN THE ACTIVE LEVEL SELECTION OF THE GPIO APPLICATION.
EX.WHEN STRAP SETTING IS PULLED HIGH, THEN IT CAN BE USED AS A GPIO OF ACTIVE LOW
THAT HAVE A POWER UP STATE OF HIGH.

NOTE: IF GPIO PINS THAT ALSO WANT TO USED AS HARDWARE STRAP, HAD BETTER TO USE THEM AS GPO ONLY.

DESIGN NOTE:

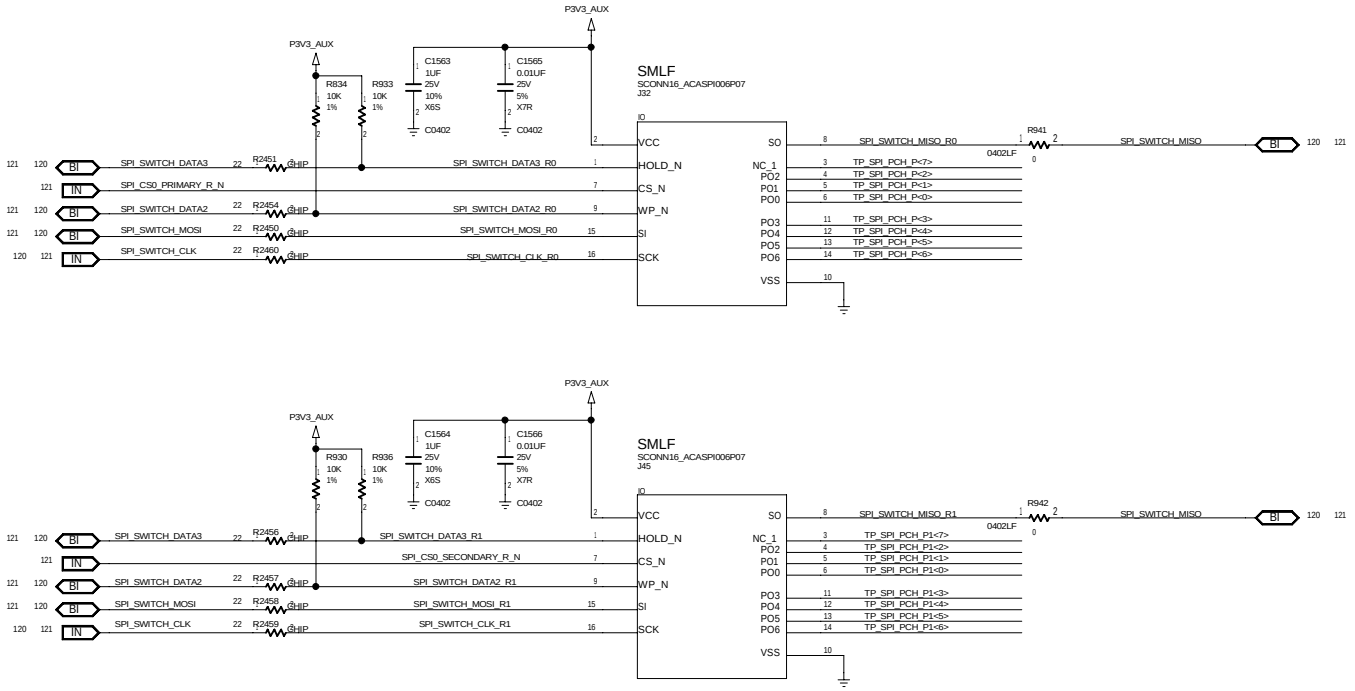
AST2500 DEFINES A 3 STEPS PROCEDURE FOR FUNCTIONAL STRAP SETTING INPUT.

1. STEP1:LOAD FROM DEDICATED STRAP PINS.
   - BASED ON THE SETTING AT STEP 1 TO LOAD STEP 2 OR STEP 3 STRAP INPUTS.
2. STEP2:HARDWARE STRAP: LOAD FROM THE OPTIONAL STRAP PINS WHEN SRST#(RST_RSMRST_N) ACTIVE.
3. STEP3:SOFTWARE STRAP: LOAD FROM THE FIRMWARE SPI FLASH WHEN SRST#(RST_RSMRST_N) INACTIVE.
   - THE STEP 2 AND STEP 3 STRAP INPUT MODES CAN BE ENABLED SIMUTANEOUSLY.
   BUT SOFTWARE STRAP EXECUTES LATER AND HAS HIGHER PRIORITY TO OVERWRITE HARDWARE STRAP.

THE HARDWARE STRAP REGISTERS LOAD THE EXTERNAL PIN VOLTAGE STATE
WHEN SRST#(RST_RSMRST_N) RESET INPUT IS LOW.
AND KEEP THE VALUE UNCHANGED AFTER SRST#(RST_RSMRST_N) GOEST HIGH.
THE STRAP REGISTER IS DEFINED AT ADDRESS 0X1E6E2070 IN THE SYSTEM CONTROL UNIT (SCU) MODULE.

BMC HW STRAPS (BIT 30-31)

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> REV: <Q_REV>
		REVIEWER:	SIZE C DATE Fri Dec 15 20:21:56 2017	SHEET 119 OF 226



CPU BIOS ROM

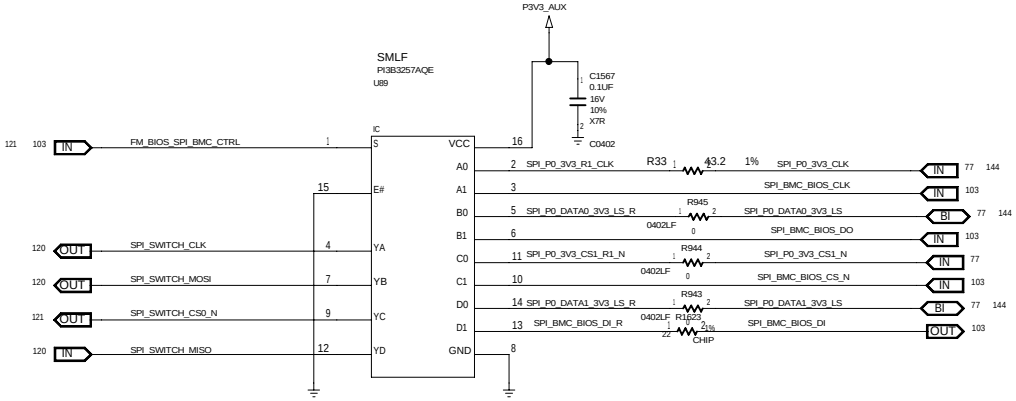
Quanta

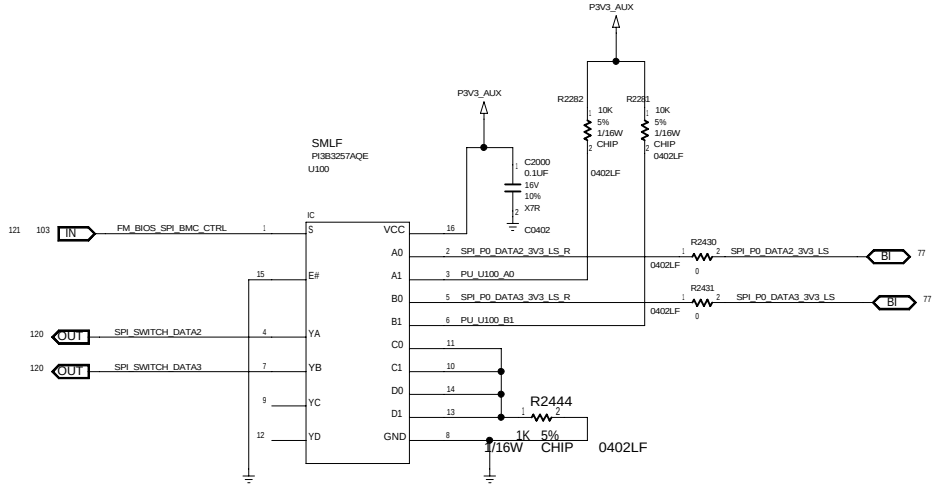
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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PI3B3257A TRUTH TABLE

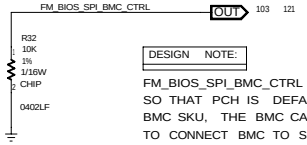
E#	S	Y_N	FUNCTION
H	X	HIZ	DISABLE
L	L	N_0	S=0
L	H	N_1	S=1





CAD NOTE:

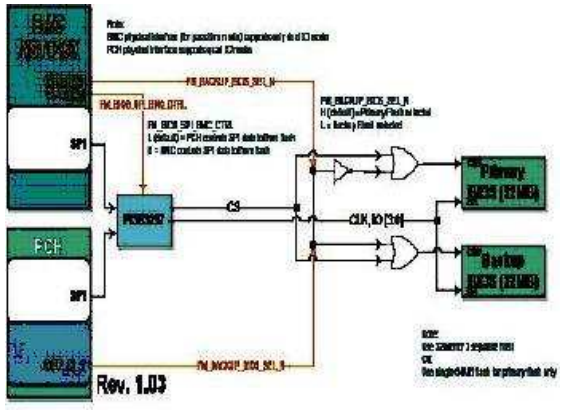
PLACE R8E18 CLOSE TO U8E6

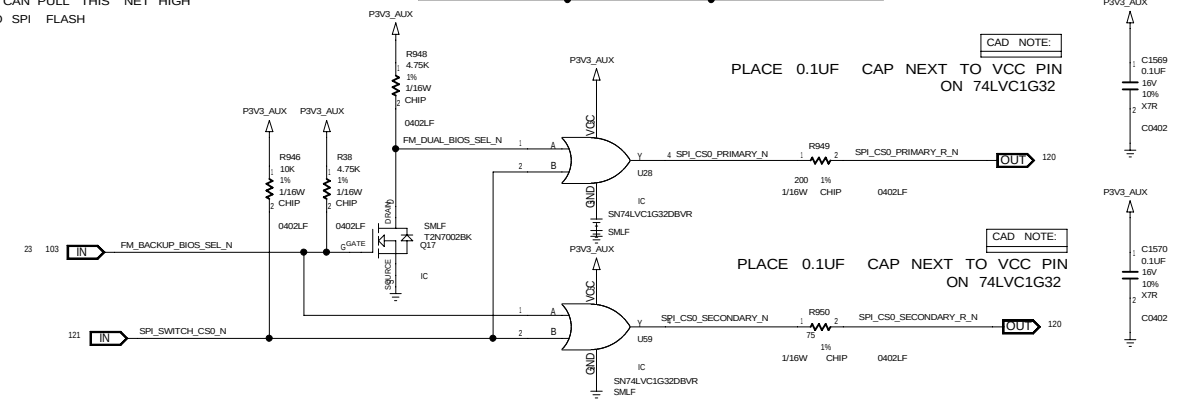


DESIGN NOTE:

FM_BIOS_SPI_BMC_CTRL NET SHOULD BE PULLED DOWN SO THAT PCH IS DEFAULT BUS AND FOR BMC SKU, THE BMC CAN PULL THIS NET HIGH TO CONNECT BMC TO SPI FLASH

FM_BACKUP_BIOS_SEL_N	SPI_SWITCH_CS0_N	BIOS	
H (DEFAULT)	L	PRIMARY (DEFAULT)	A1
L	L	SECONDARY	A0
X	H	X	





CAD NOTE:

PLACE 0.1UF CAP NEXT TO VCC PIN ON 74LVC1G32

CAD NOTE:

PLACE 0.1UF CAP NEXT TO VCC PIN ON 74LVC1G32

BMC SHARED SPI FLASH MUX

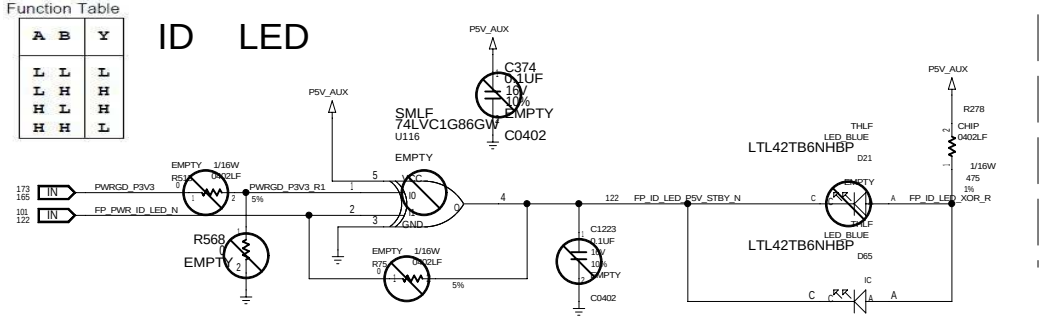
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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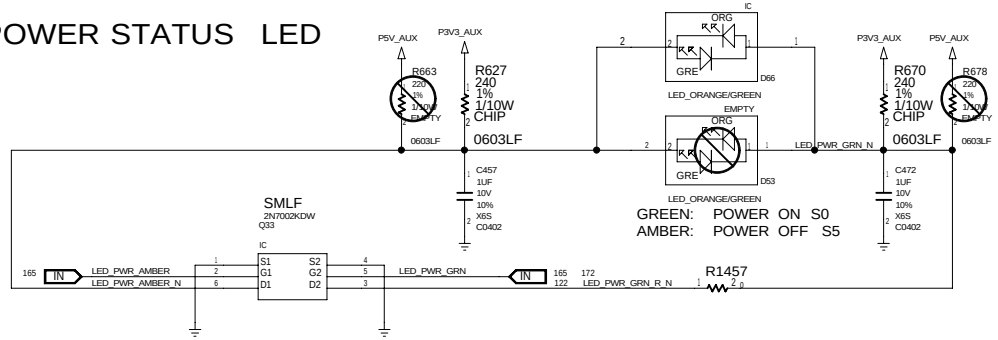
ID LED

Function Table

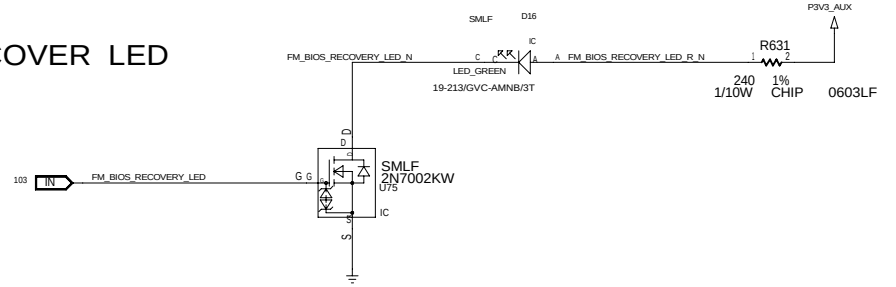
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



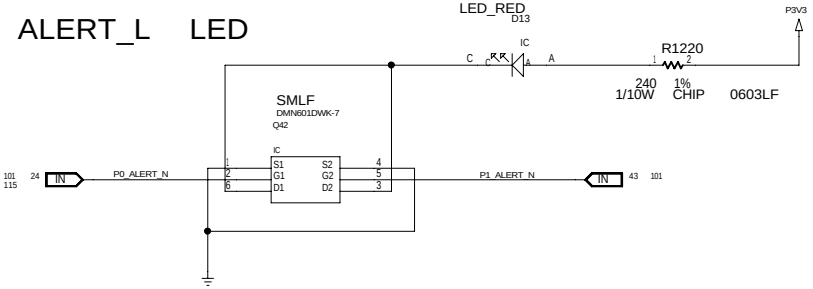
POWER STATUS LED



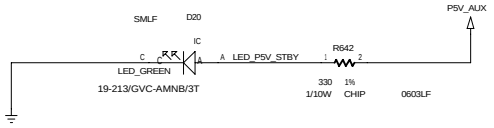
BIOS RECOVER LED



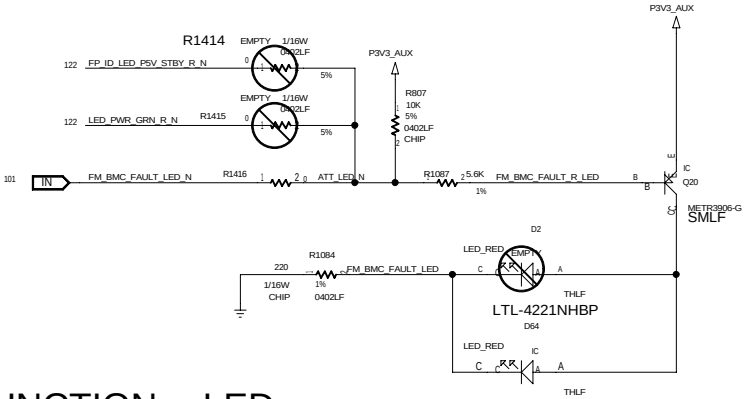
ALERT_L LED



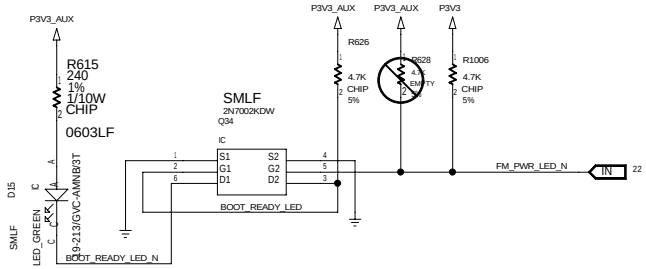
P5V_AUX STATUS LED



BLADE ATTENTION LED

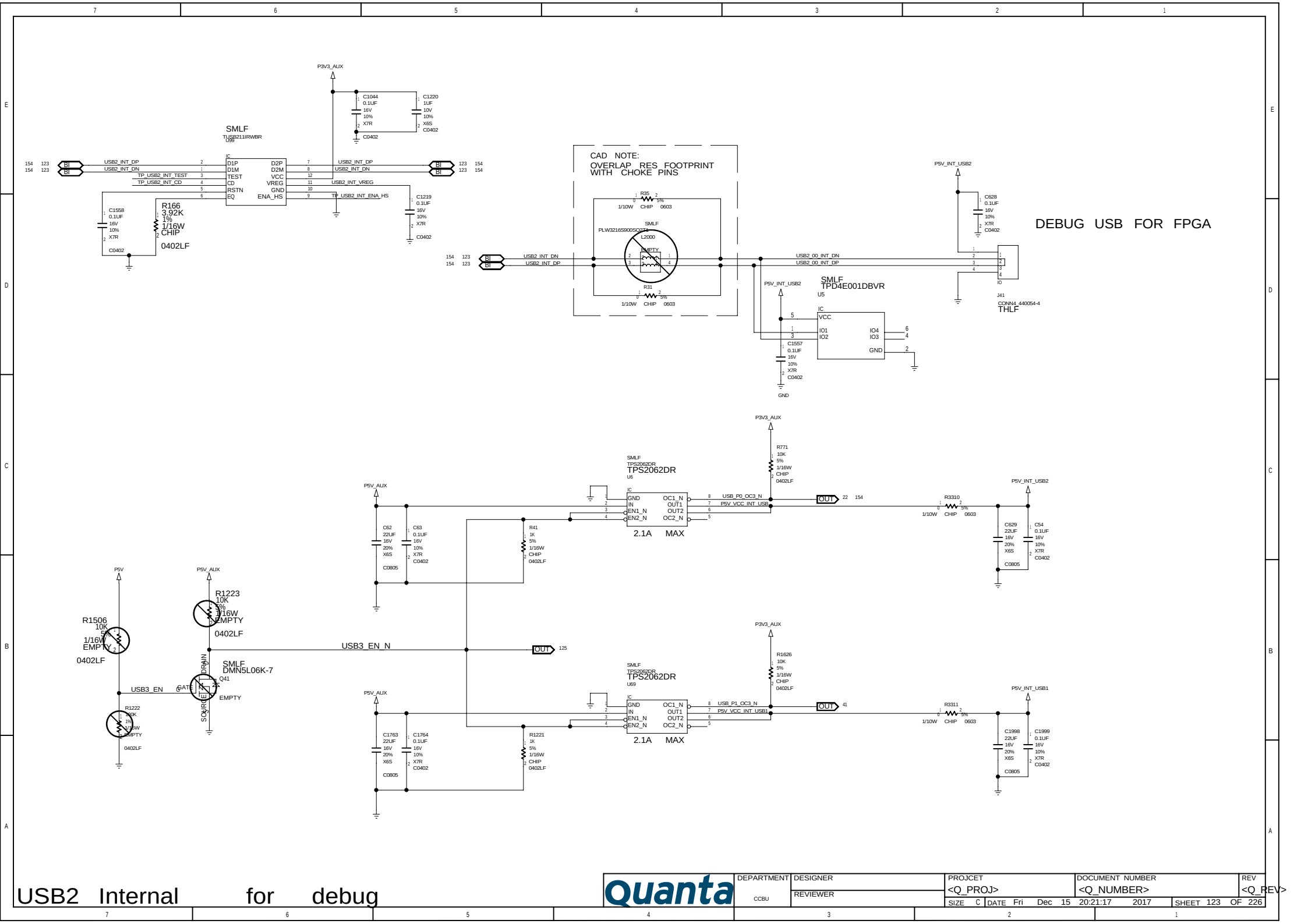


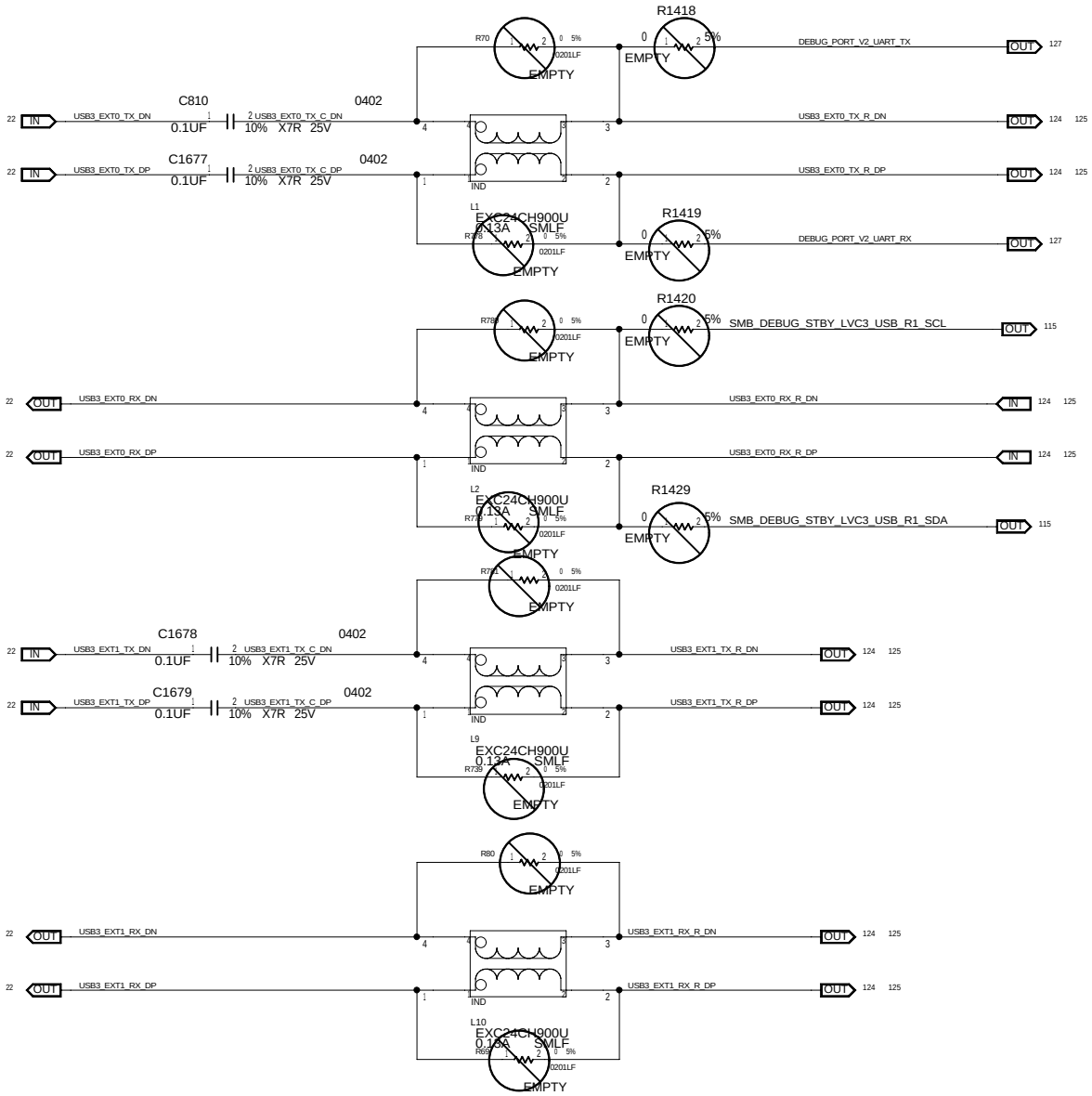
BOOT-UP READY LED

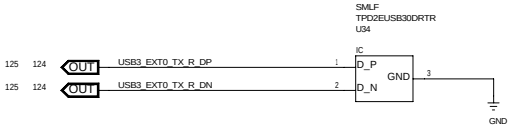


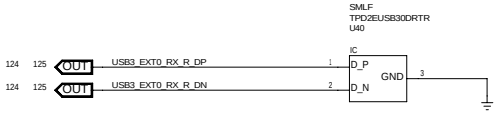
FUNCTION LED

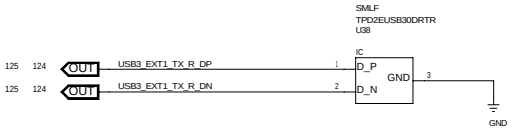
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			REV: <Q_REV>
		SIZE: C	DATE: Fri Dec 15 20:21:17 2017
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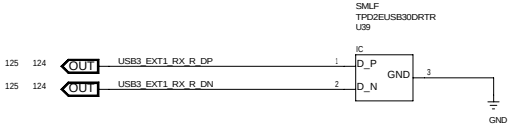

DEBUG USB FOR FPGA
CAD NOTE:
OVERLAP RES FOOTPRINT
WITH CHOKE PINS
SMLF
TUSB211IRWBR
U99
SMLF
TPD4E001DBVR
U5
SMLF
TPS2062DR
U6
SMLF
TPS2062DR
U69
SMLF
DMN5L06K-7
Q41
THLF
CONN4_440054-4
J41
USB2_INT_DP
USB2_INT_DN
TP_USB2_INT_TEST
TP_USB2_INT_CD
USB2_INT_VREG
TP_USB2_INT_ENA_HS
USB2_00_INT_DN
USB2_00_INT_DP
P3V3_AUX
P5V_INT_USB2
P5V_AUX
P5V
P5V_INT_USB1
USB_P0_OC3_N
USB_P1_OC3_N
P5V_VCC_INT_USB
USB3_EN_N
USB3_EN
2.1A MAX
R166 3.92K 1% 1/16W CHIP 0402LF
R1506 10K 5% 1/16W EMPTY 0402LF
R1223 10K 5% 1/16W EMPTY 0402LF
R1222 10K 1% 1/16W EMPTY 0402LF
R771 10K 5% 1/16W CHIP 0402LF
R1626 10K 5% 1/16W CHIP 0402LF
R41 1K 5% 1/16W CHIP 0402LF
R1221 1K 5% 1/16W CHIP 0402LF
R35 0 5% 1/10W CHIP 0603
R31 0 5% 1/10W CHIP 0603
R3310 0 5% 1/10W CHIP 0603
R3311 0 5% 1/10W CHIP 0603
L2000 EMPTY
PLW3216S900SQ2T1
C1044 0.1UF 16V 10% X7R C0402
C1220 1UF 10V 10% X6S C0402
C1558 0.1UF 16V 10% X7R C0402
C1219 0.1UF 16V 10% X7R C0402
C628 0.1UF 16V 10% X7R C0402
C1557 0.1UF 16V 10% X7R C0402
C62 22UF 16V 20% X6S C0805
C63 0.1UF 16V 10% X7R C0402
C629 22UF 16V 20% X6S C0805
C54 0.1UF 16V 10% X7R C0402
C1763 22UF 16V 20% X6S C0805
C1764 0.1UF 16V 10% X7R C0402
C1998 22UF 16V 20% X6S C0805
C1999 0.1UF 16V 10% X7R C0402
USB2 Internal for debug
Quanta
DEPARTMENT CCBU
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REVIEWER
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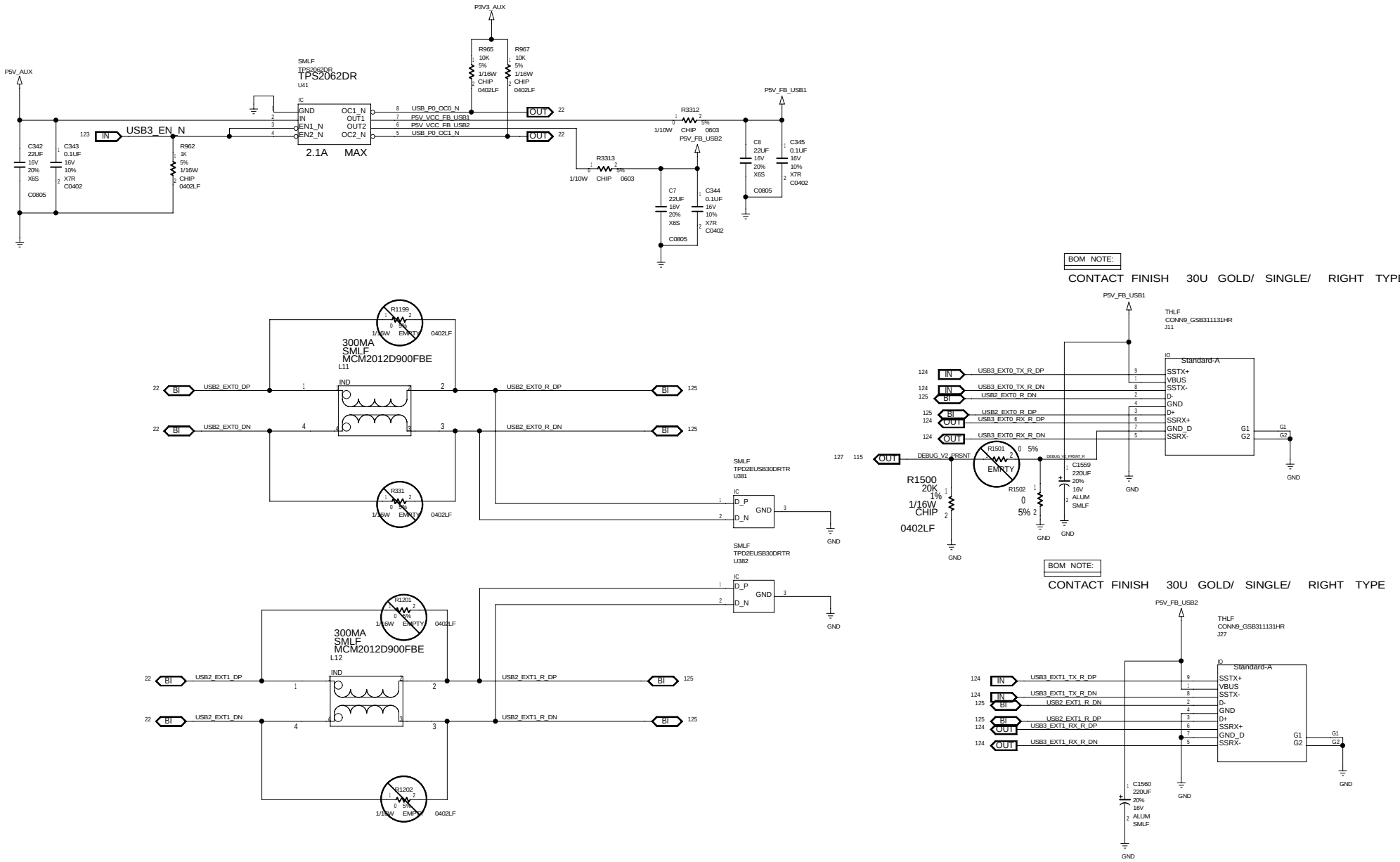






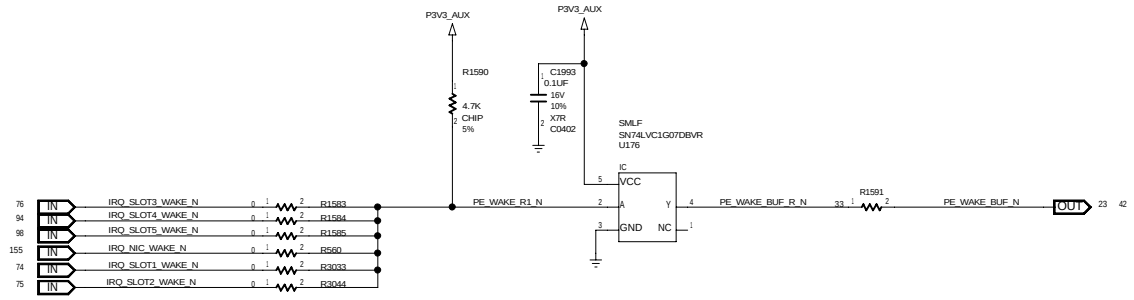
USB3 External (1 OF 2)

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:57 2017	SHEET 124 OF 226



USB3 External (2 OF 2)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:57 2017
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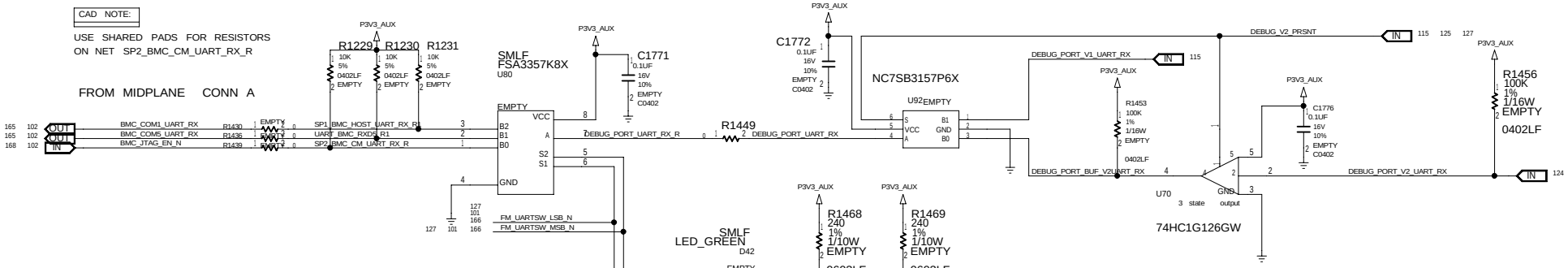
PCIE RESET & WAKEUP

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:57 2017	SHEET 126 OF 226

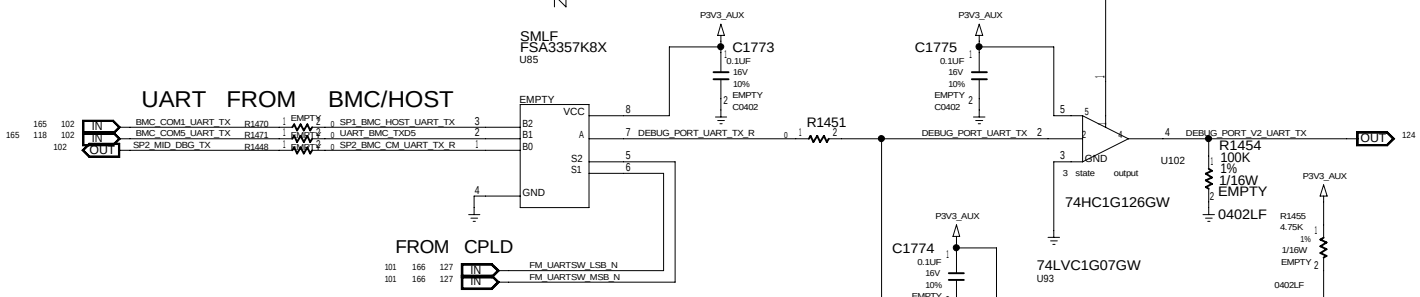
CAD NOTE:

USE SHARED PADS FOR RESISTORS
ON NET SP2_BMC_CM_UART_RX_R

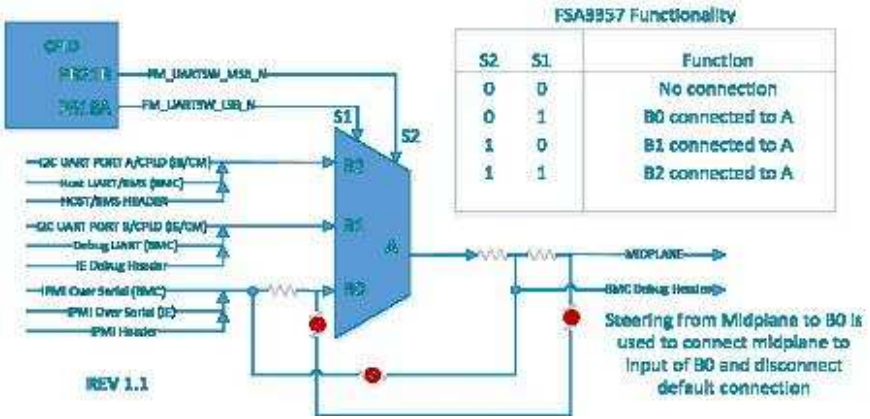
FROM MIDPLANE CONN A



UART FROM BMC/HOST

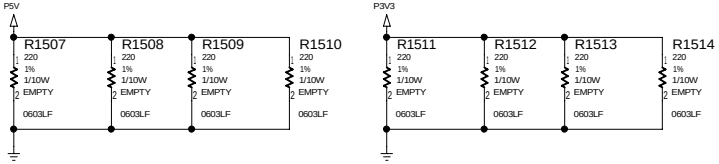


FROM CPLD



FSA9357 Functionality

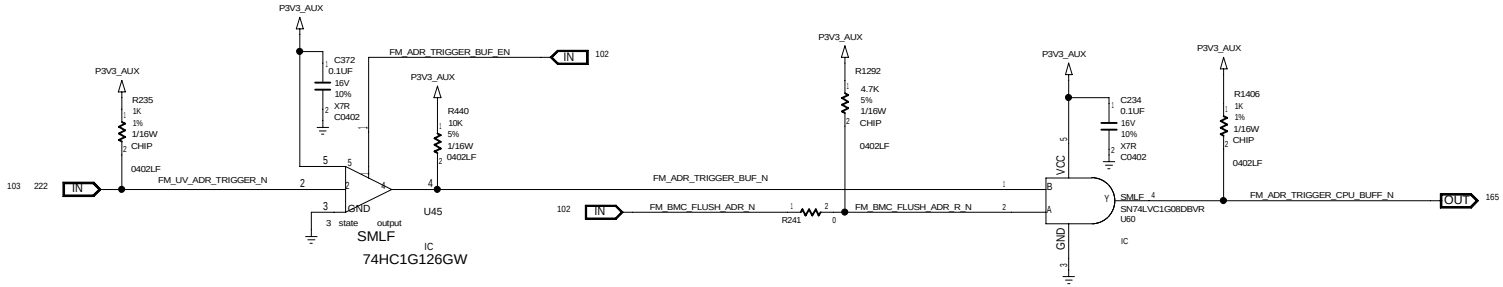
S2	S1	Function
0	0	No connection
0	1	B0 connected to A
1	0	B1 connected to A
1	1	B2 connected to A



DEBUG_UART

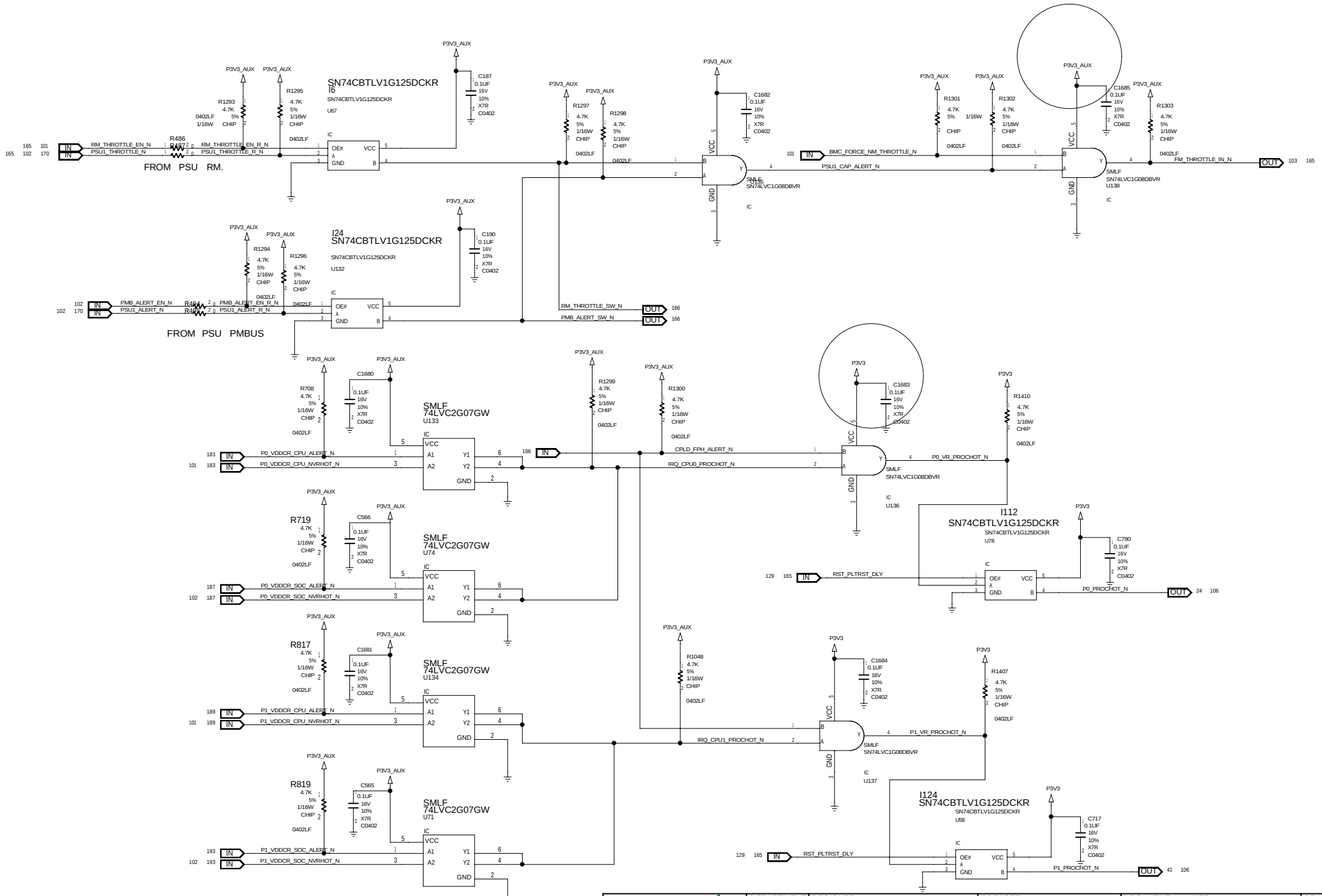
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			SIZE C	DATE Fri Dec 15 20:21:20 2017	SHEET 127 OF 226

NVDIMM SUPPORT



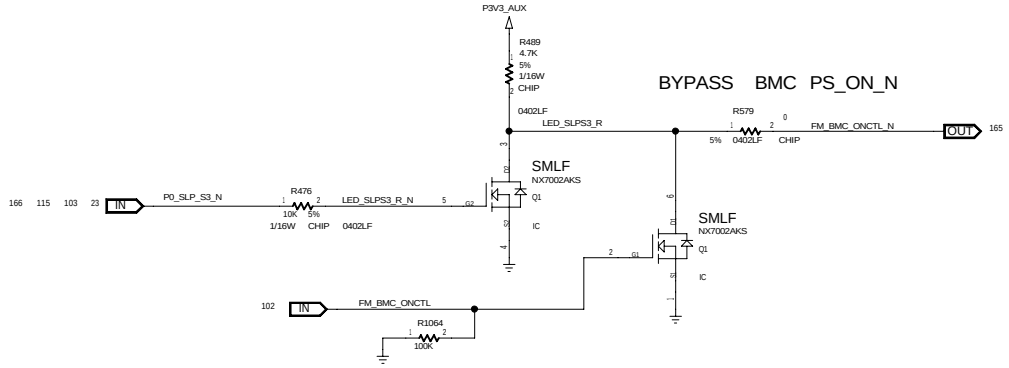
ADR SAVE & TRIGGER

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
		REVIEWER:	SIZE: C / DATE: Fri Dec 15 20:21:57 2017	SHEET 128 OF 226



PSU & VR ALERT

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
	SIZE: C	DATE: Fri Dec 15 20:21:57 2017	SHEET 129 OF 226



S3 CONTROL

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:58 2017	SHEET 130 OF 226

BLANK

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 19:34:33 2017	SHEET 131 OF 226

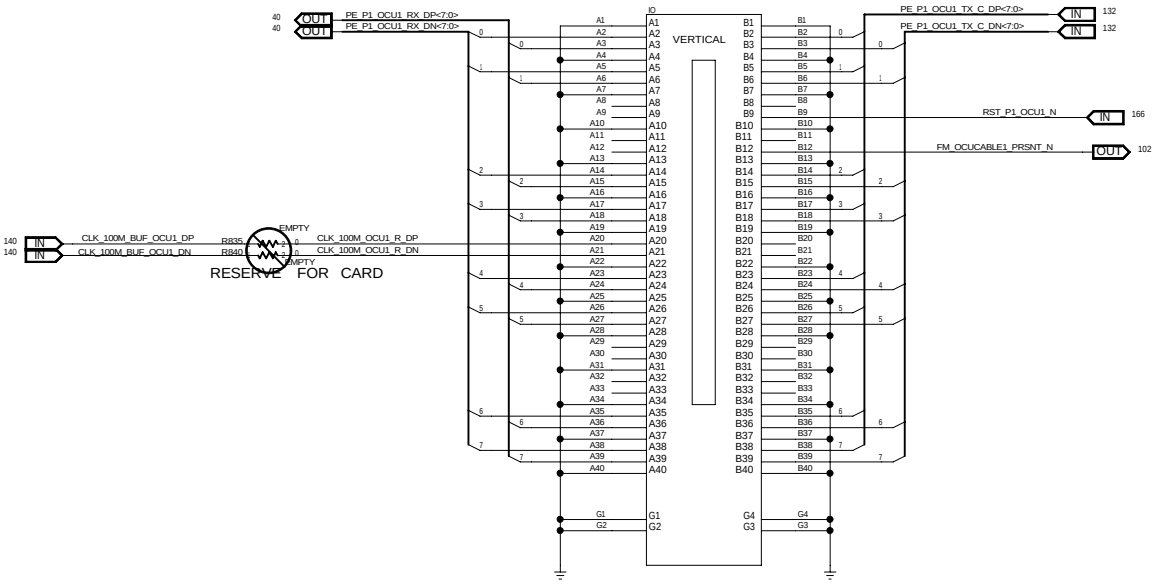
SMLF

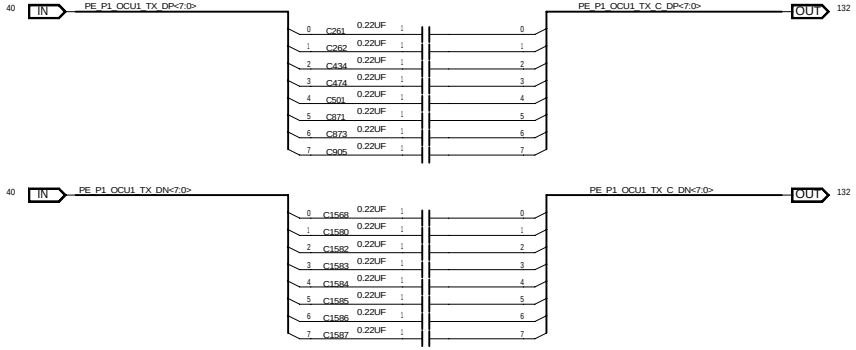
SCONN80_173162-0338

DESIGN NOTE:

NEED CHANGING TO OCULINK

J87

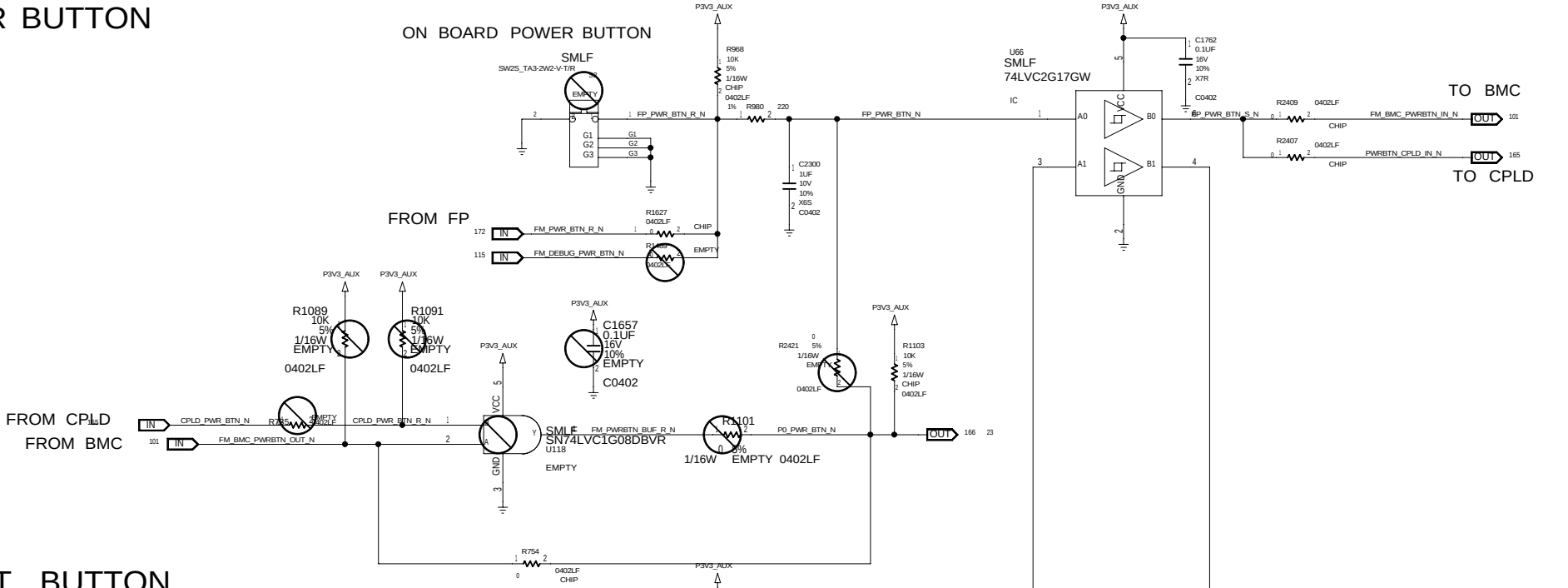




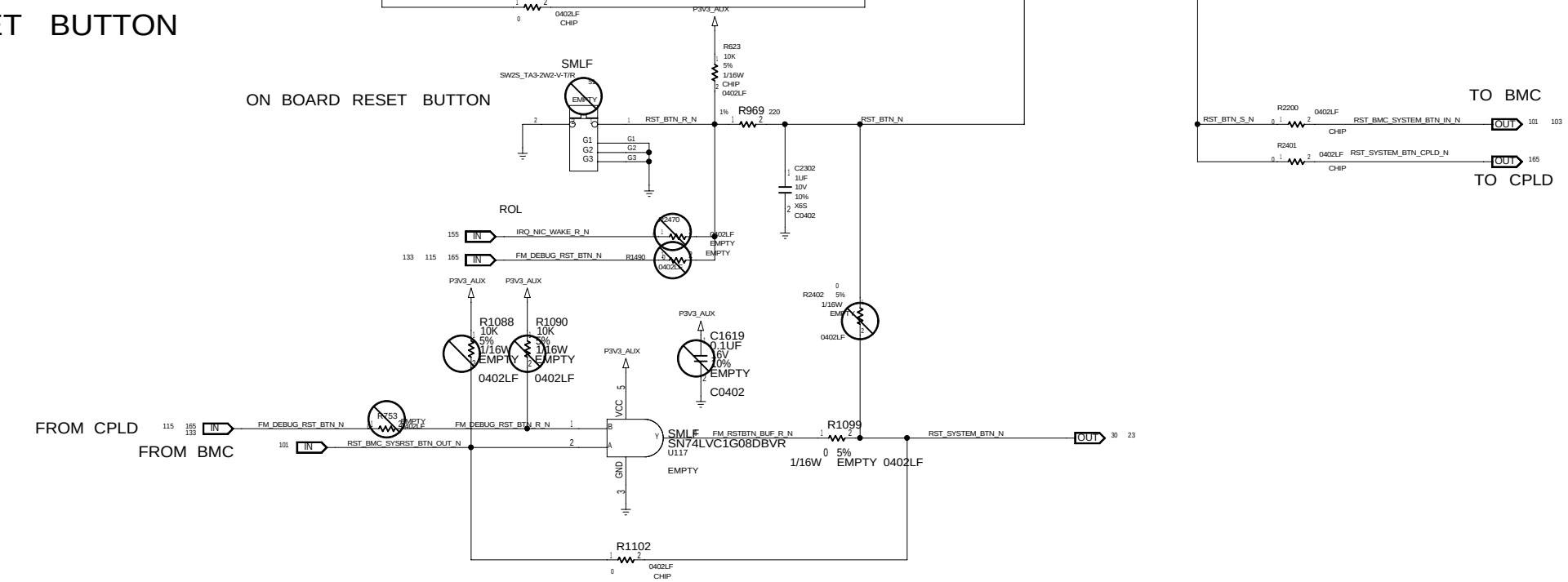
OCulink CONN1

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 20:21:58 2017	SHEET 132 OF 226

POWER BUTTON

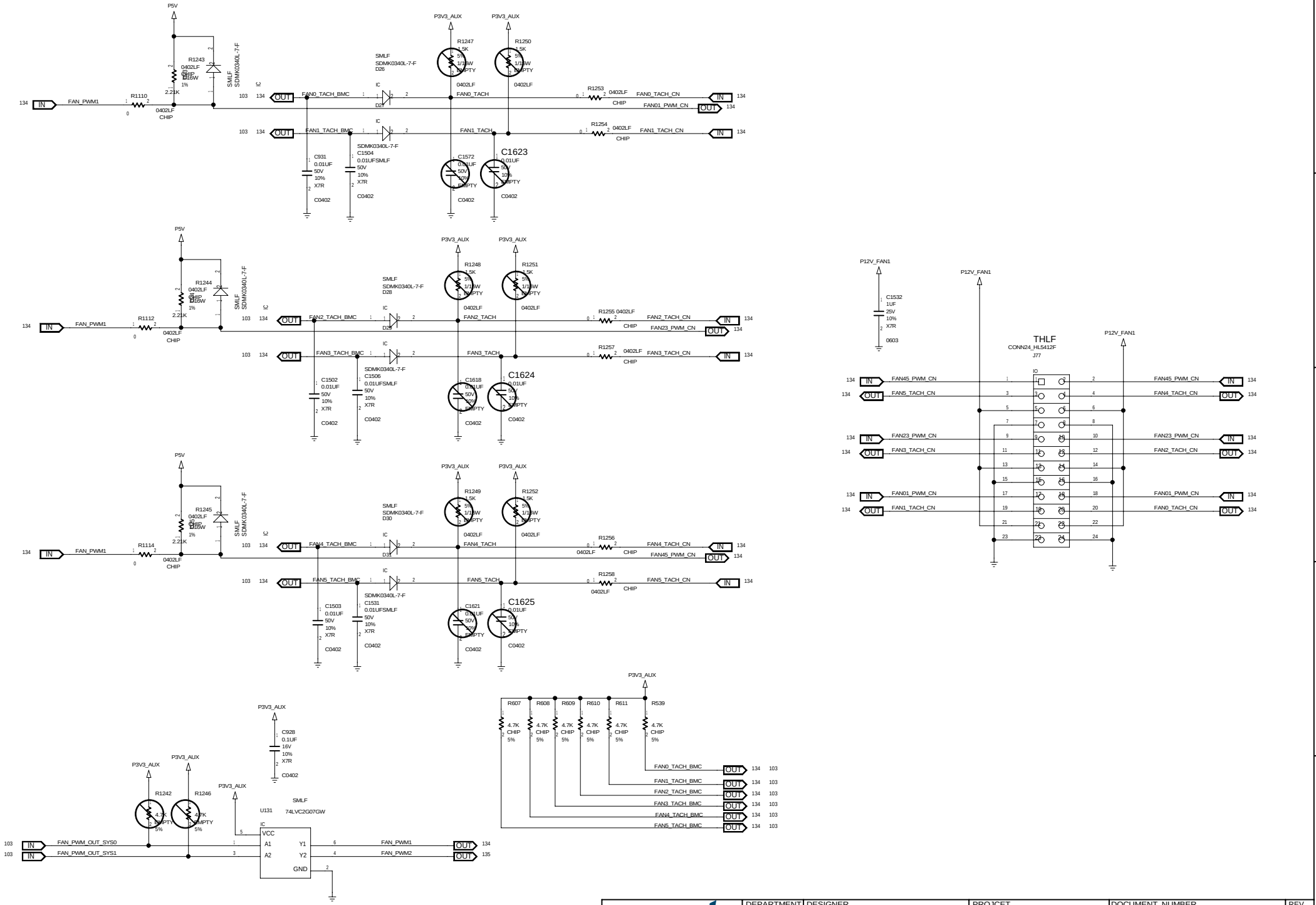


RESET BUTTON



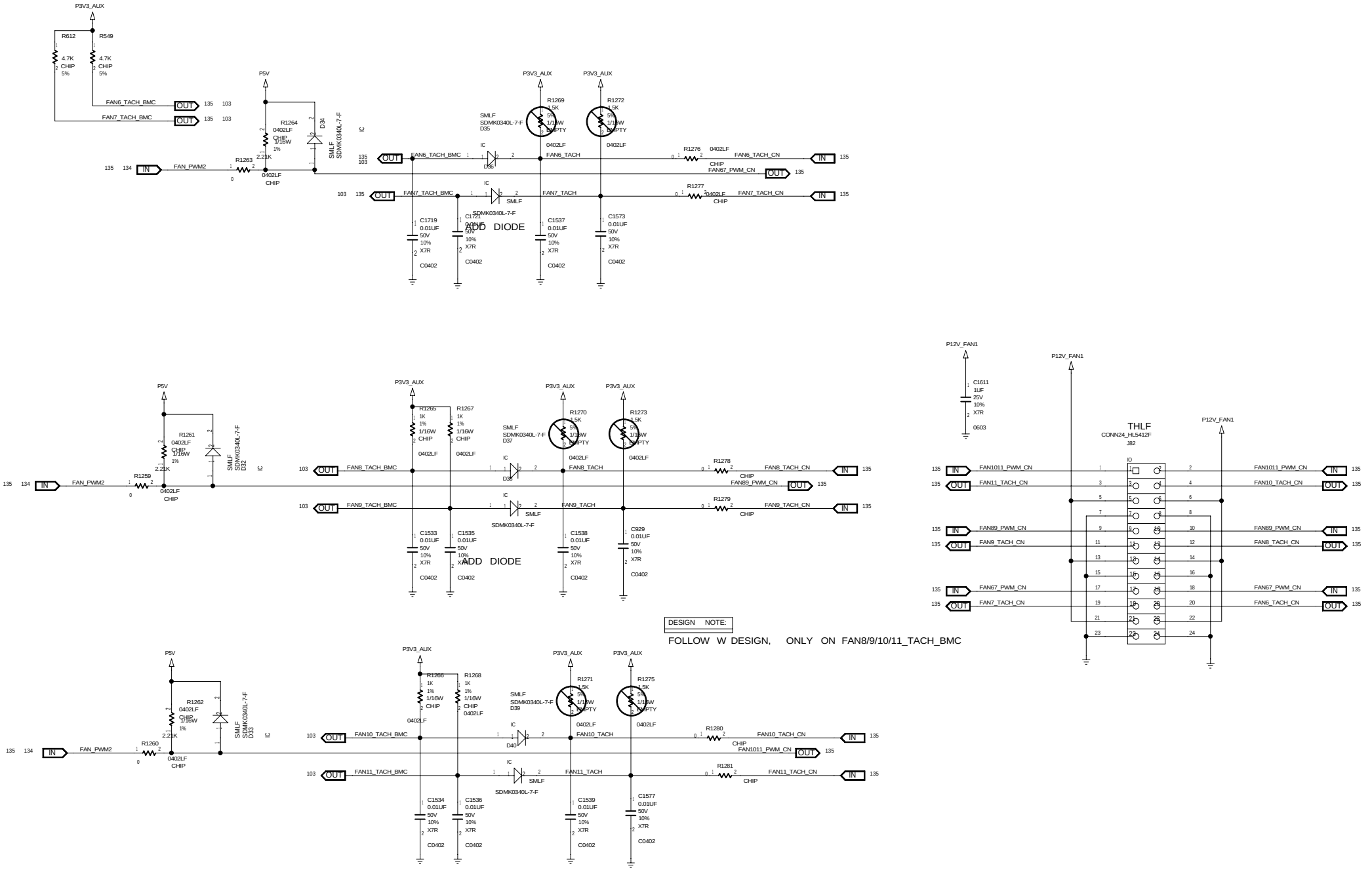
POWER & RESET BUTTON

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:58 2017
				SHEET 133 OF 226



FAN HEADER 1U

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE: C	DATE: Fri Dec 15 20:21:58 2017
				SHEET 134 OF 226



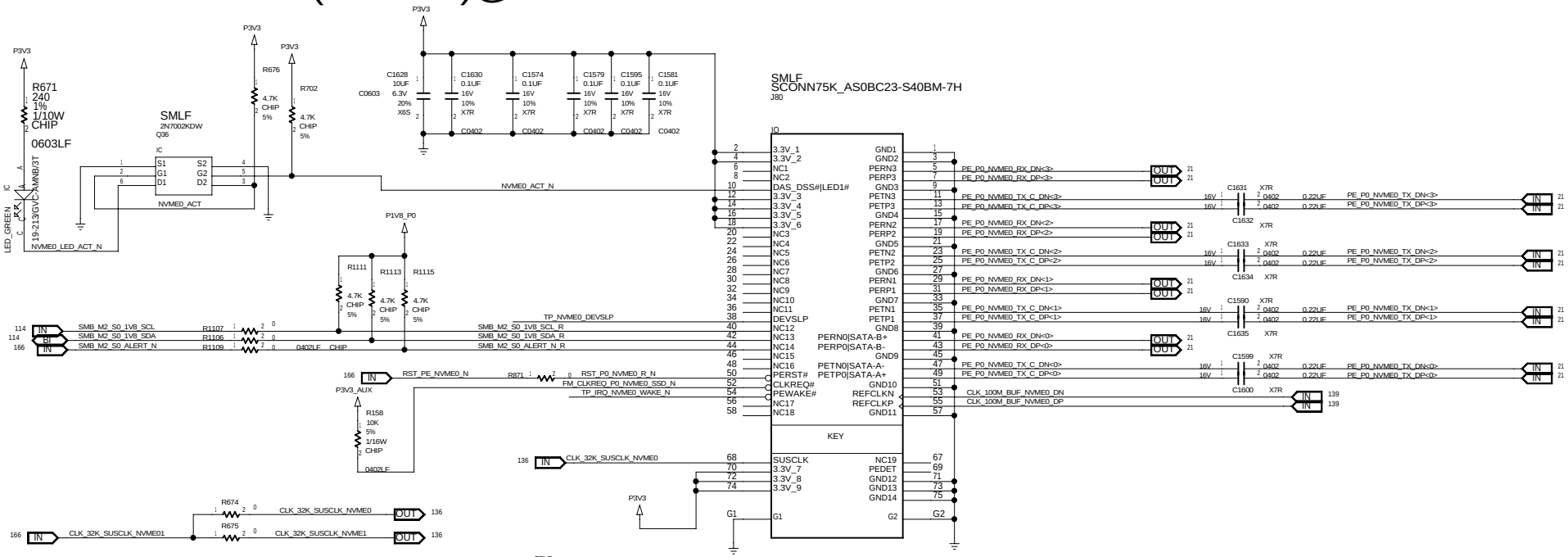
DESIGN NOTE:

FOLLOW W DESIGN, ONLY ON FAN8/9/10/11_TACH_BMC

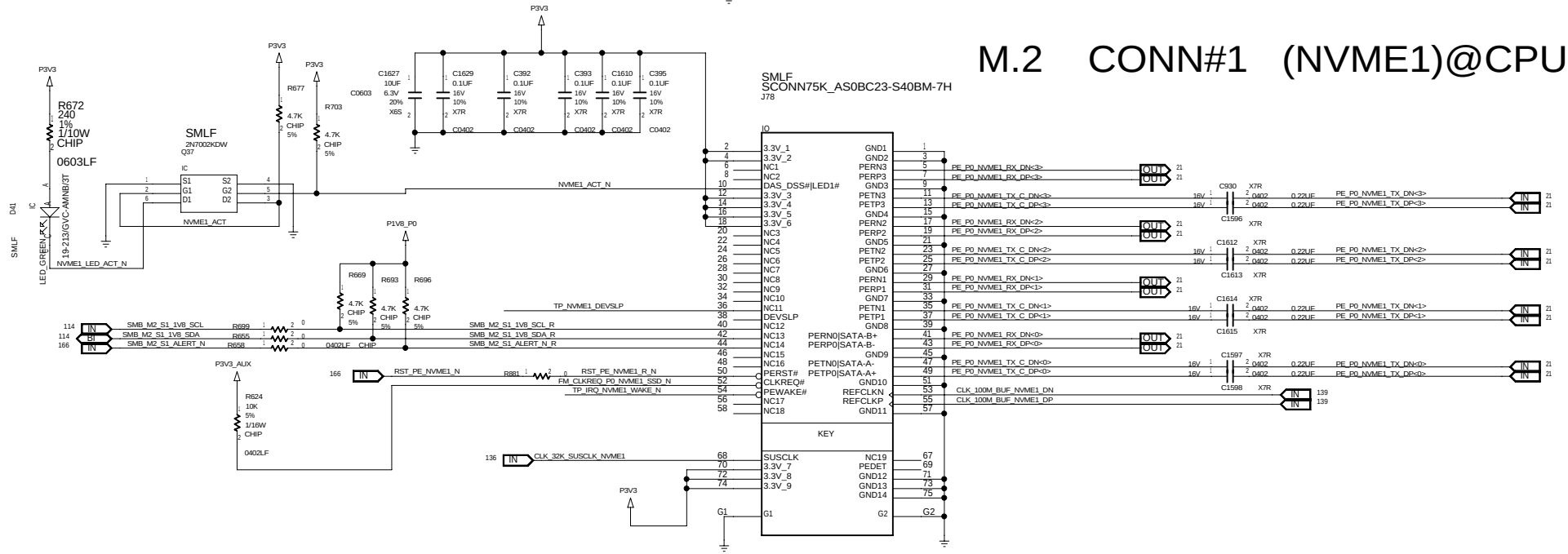
FAN HEADER 2U

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:58 2017
			REV: <Q_REV>	SHEET 135 OF 226

M.2 CONN#0 (NVME0)@CPU0



M.2 CONN#1 (NVME1)@CPU0

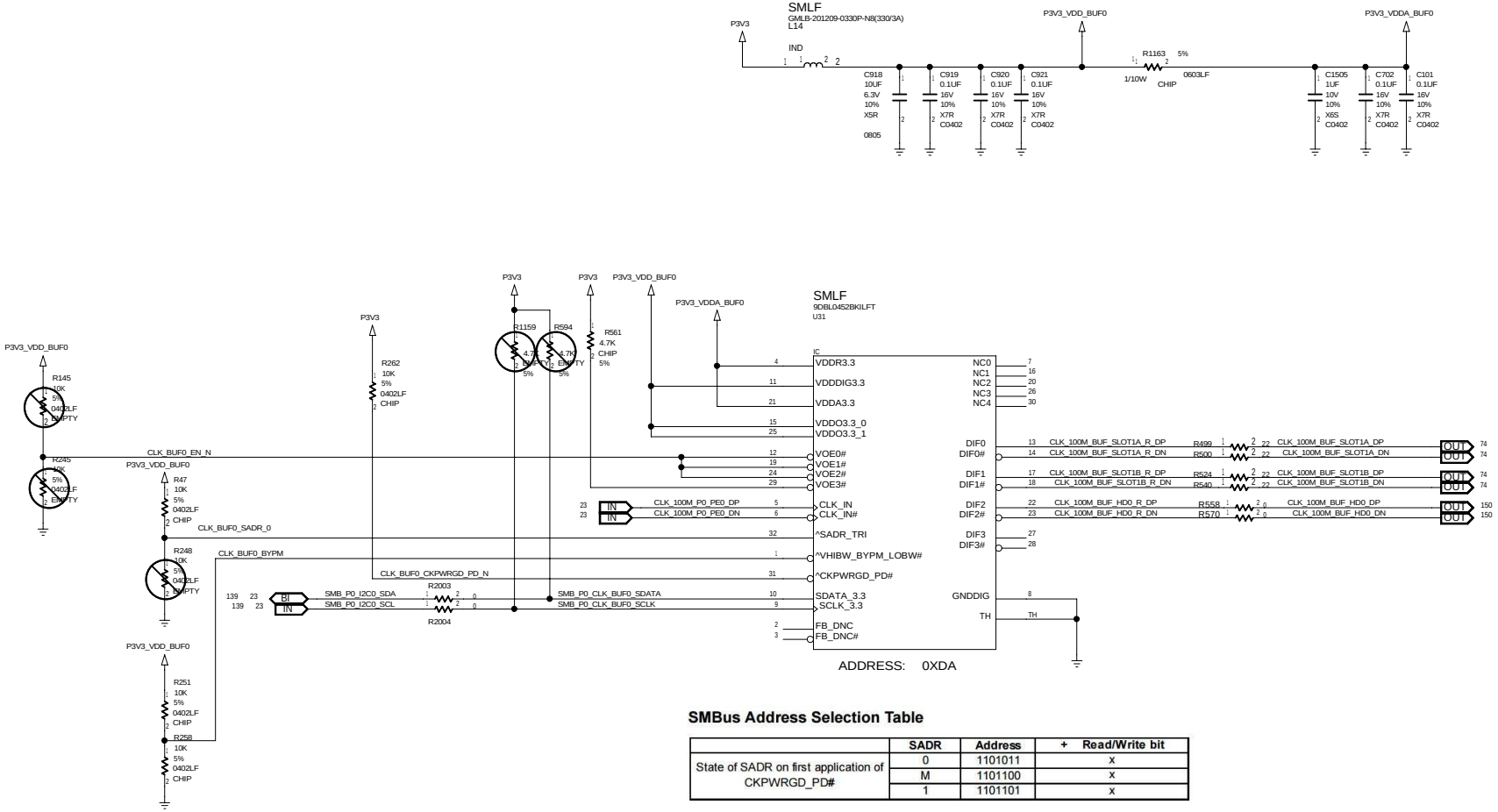


M.2 CPU0 CONN

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:17 2017	SHEET 136 OF 226

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Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 19:42:30 2017	SHEET 137 OF 226

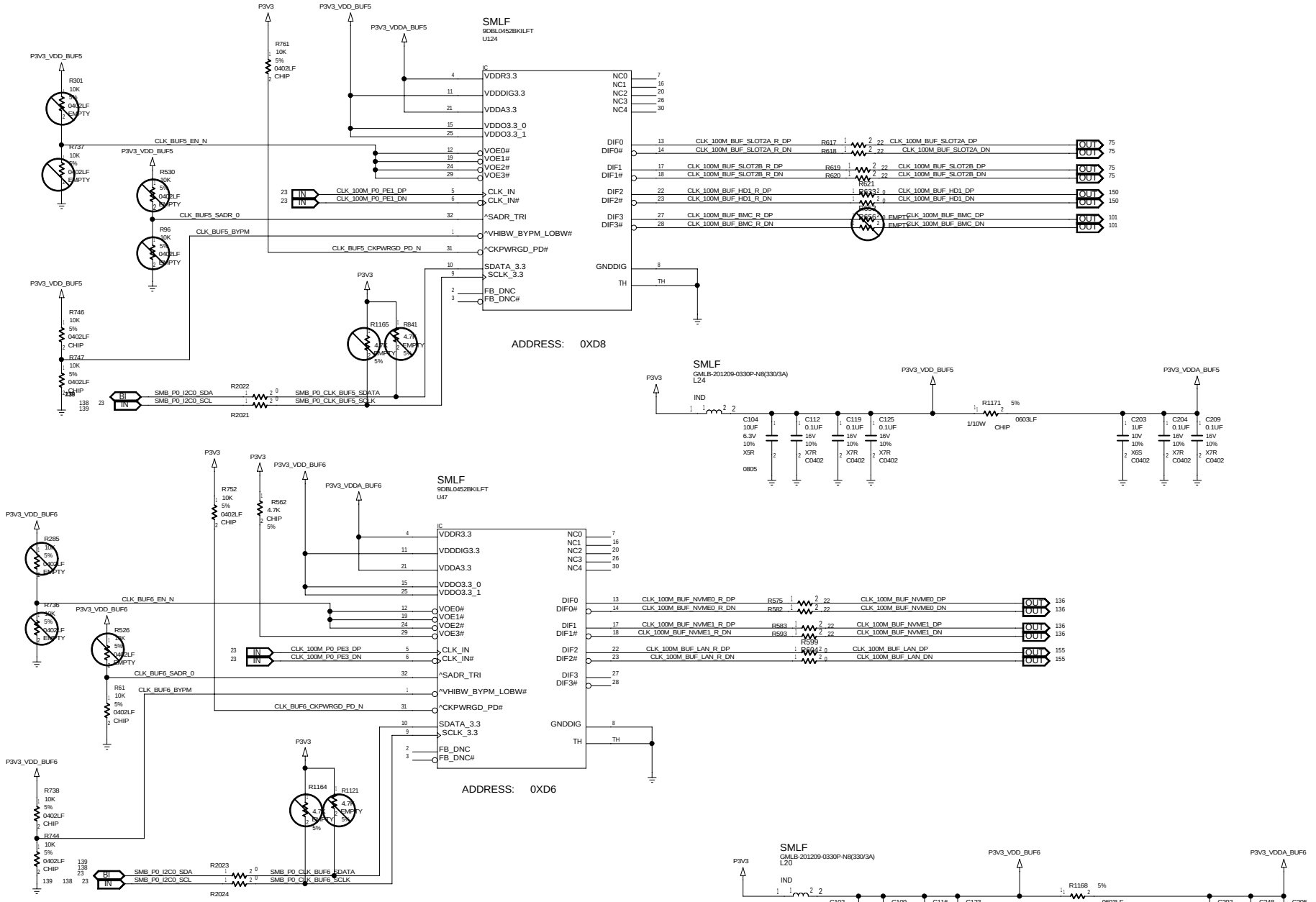


SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

CLOCK BUF FOR P0 1/2

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER	SIZE: C DATE: Fri Dec 15 20:21:18 2017	REV: <Q_REV> SHEET 138 OF 226



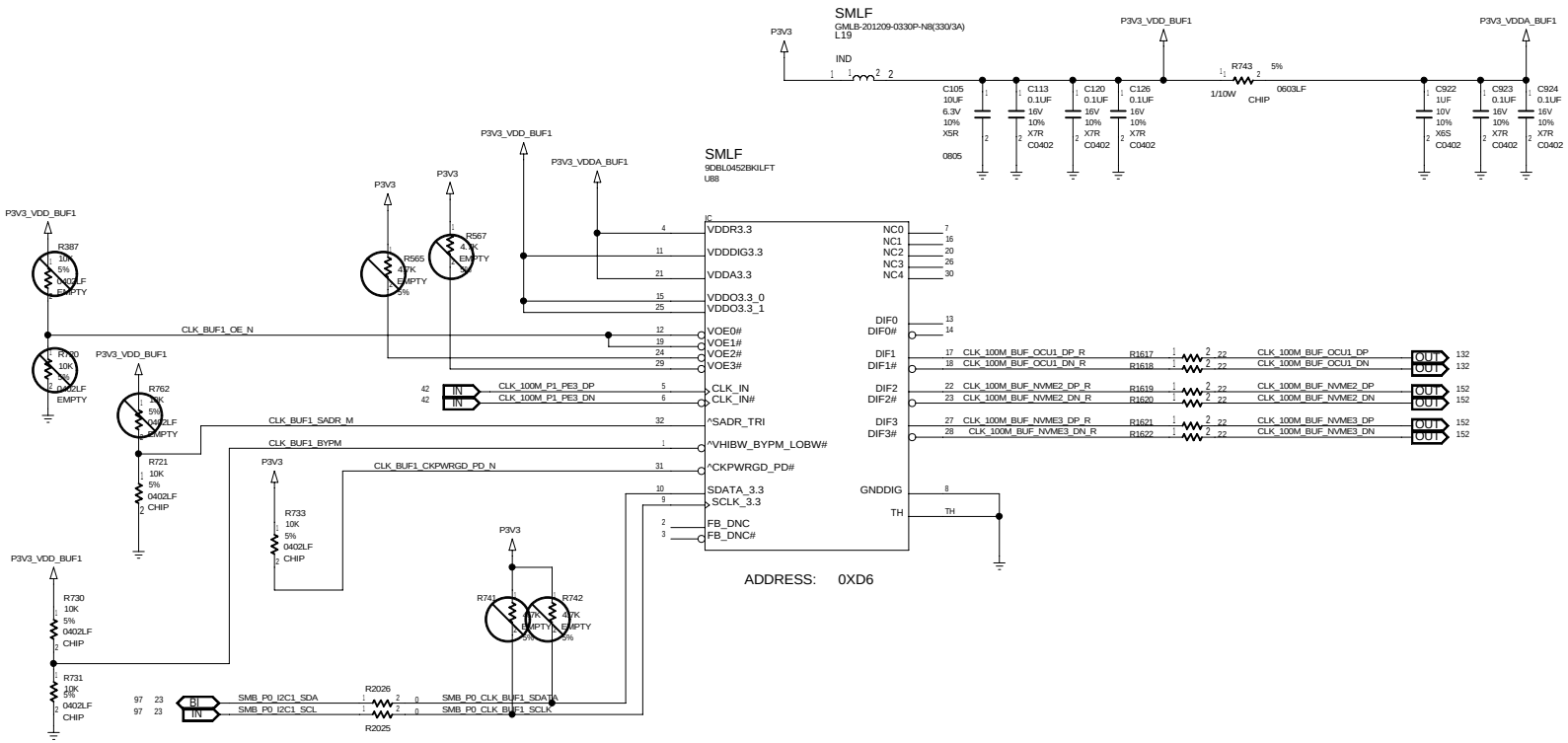
SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

CLOCK BUF FOR P0 2/2

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C | DATE Fri Dec 15 20:21:18 2017 | SHEET 139 OF 226



CLOCK BUFF FOR P1

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:18 2017	SHEET 140 OF 226

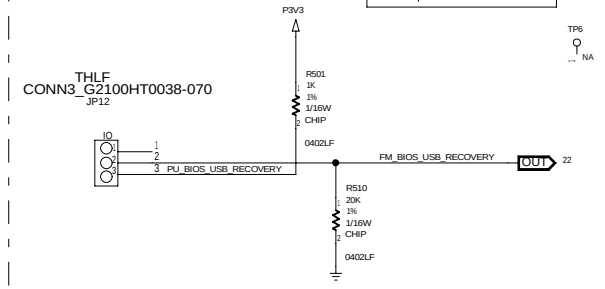
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Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 19:34:43 2017	SHEET 141 OF 226

JUMPER SETTING

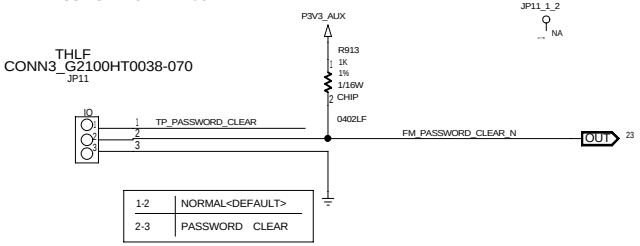
BIOS USB RECOVERY JUMPER

1-2	NORMAL<DEFAULT>
2-3	BIOS USB RECOVERY MODE



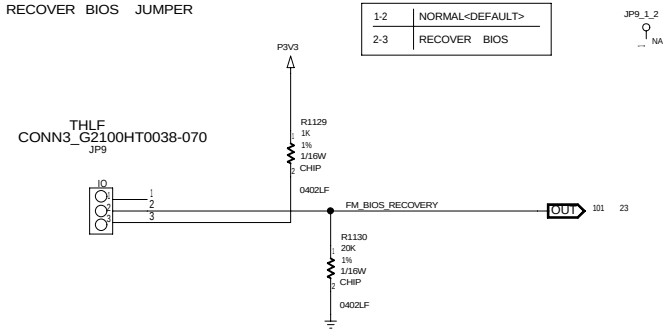
PASSWORD CLEAR JUMPER

1-2	NORMAL<DEFAULT>
2-3	PASSWORD CLEAR

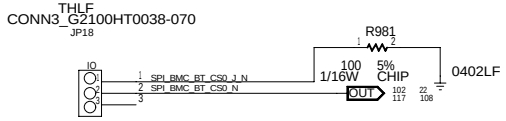


RECOVER BIOS JUMPER

1-2	NORMAL<DEFAULT>
2-3	RECOVER BIOS

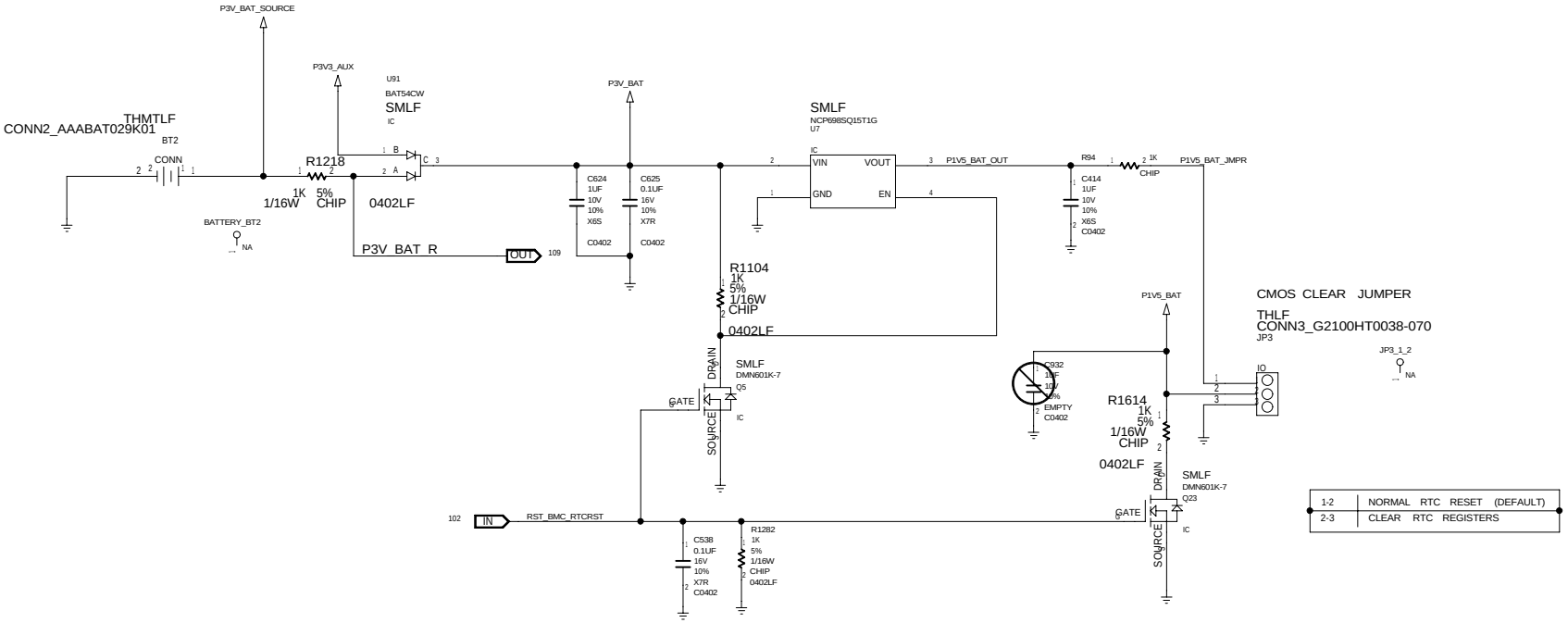


BMC DISABLE JUMPER



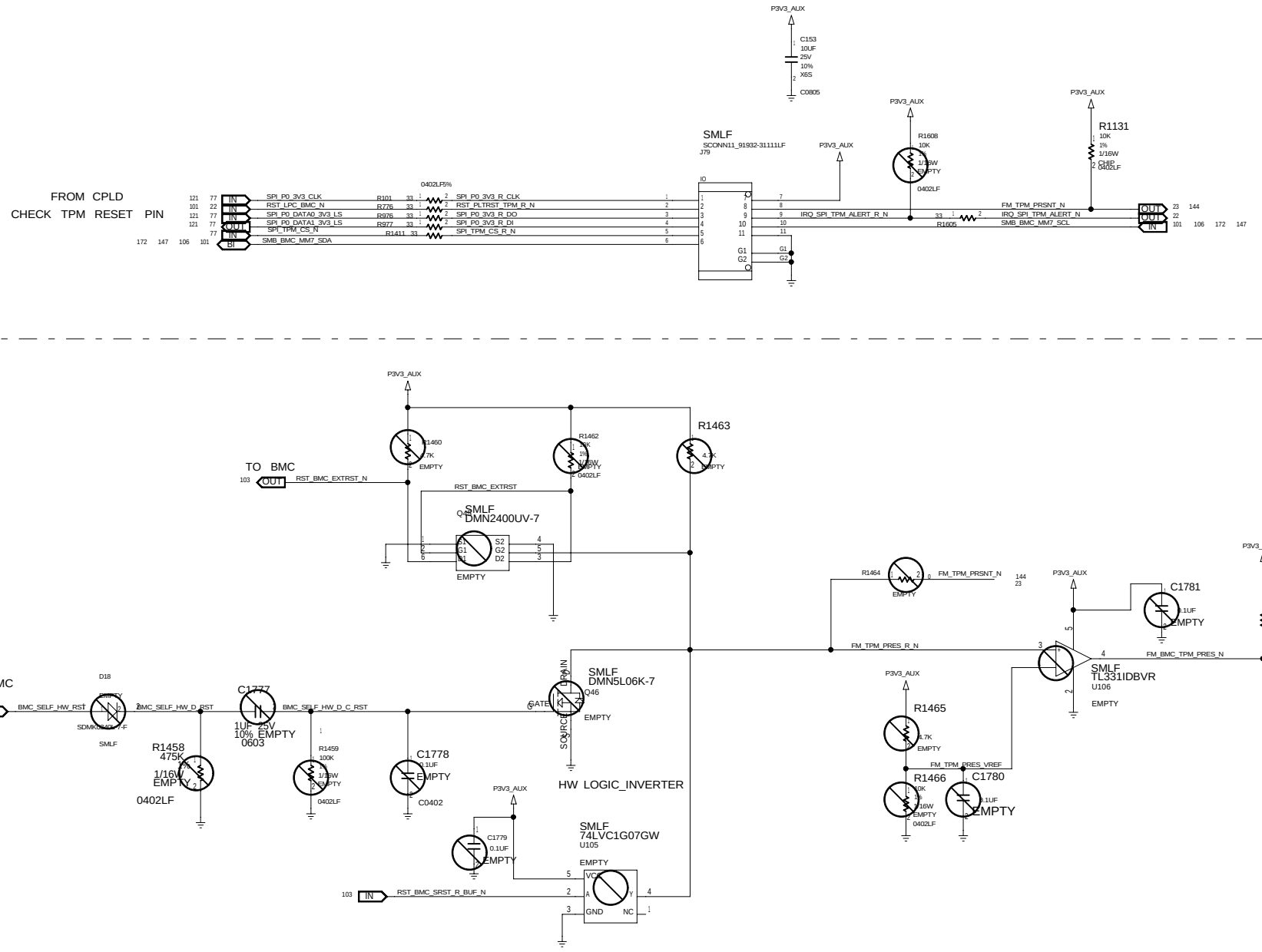
FWSPICS0# = 0, DISABLED

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:24 2017
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BATTERY & P1V5_BAT

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:18 2017	SHEET 143 OF 226



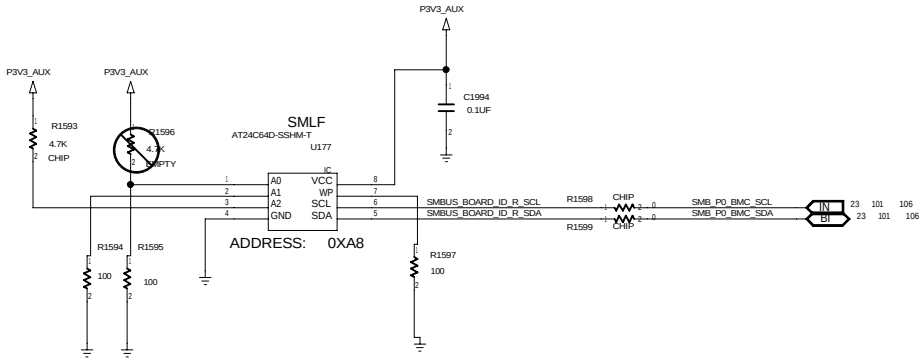
TPM CONN

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>
DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>	SIZE: C	DATE: Fri Dec 15 20:21:59 2017
SHEET 144 OF 226			

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Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 19:34:46 2017	SHEET 145 OF 226

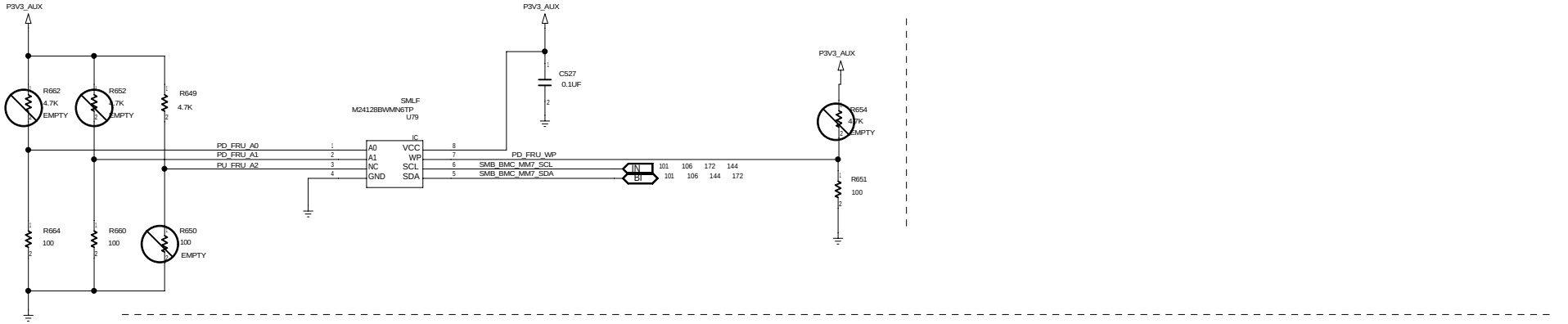
BOARD ID FOR BIOS



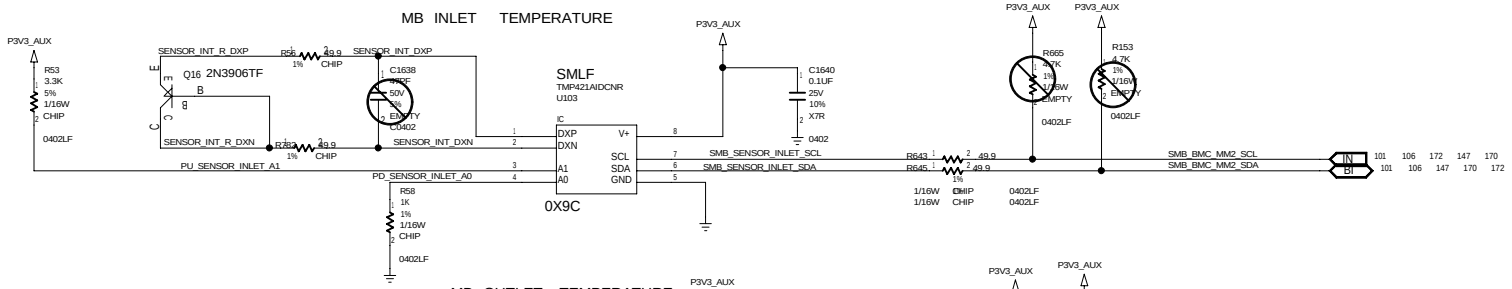
BOARD ID for BIOS

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:18 2017	SHEET 146 OF 226

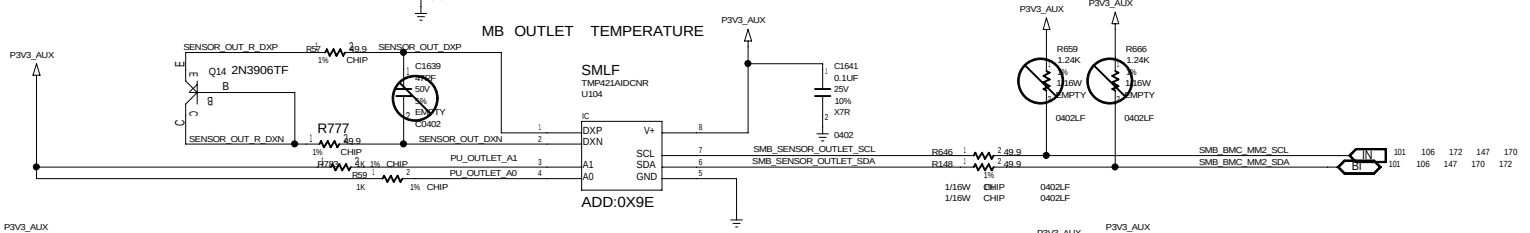
BOARD ID FRU EEPROM
SMBUS ADDRESS: 0XA8



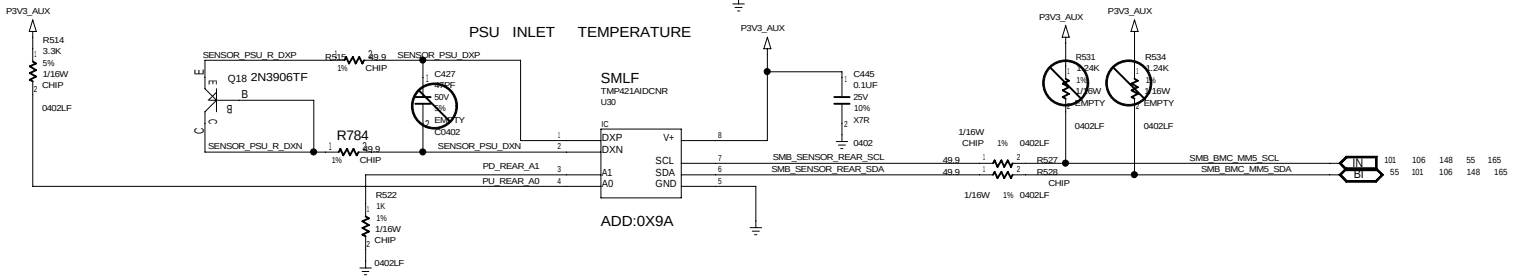
MB INLET TEMPERATURE



MB OUTLET TEMPERATURE

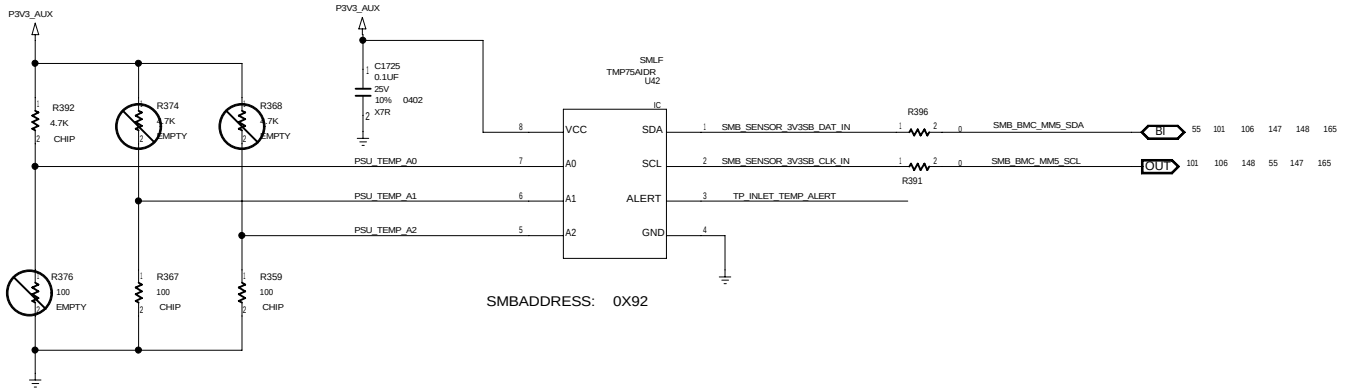


PSU INLET TEMPERATURE

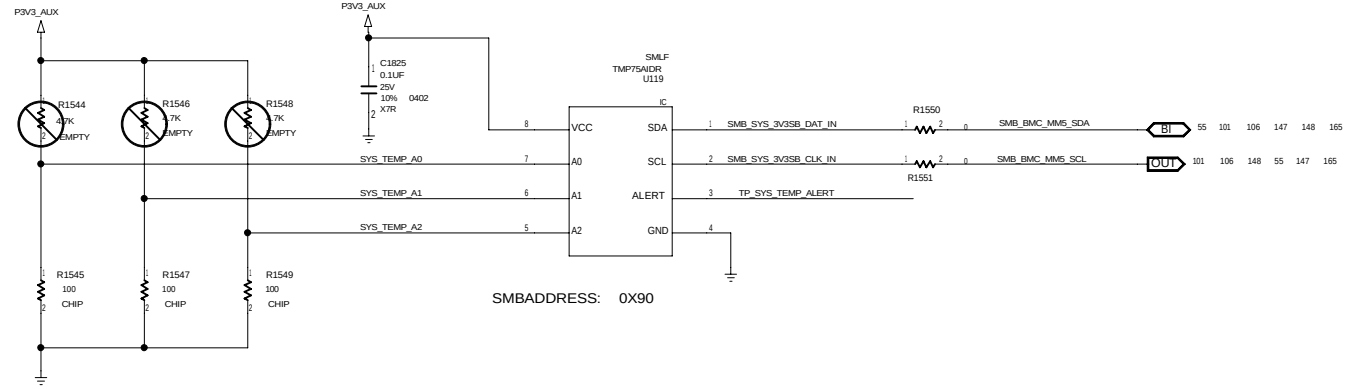


FRU & TEMP SENSOR

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:59 2017	SHEET 147 OF 226



SMBADDRESS: 0X92



SMBADDRESS: 0X90

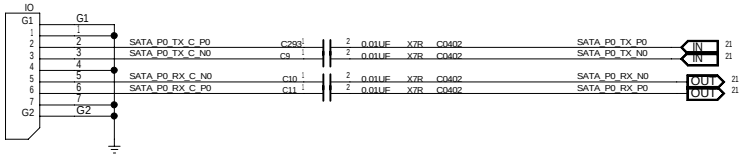
PSU TEMP SENSOR

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:59 2017	SHEET 148 OF 226

SATA0 CONN

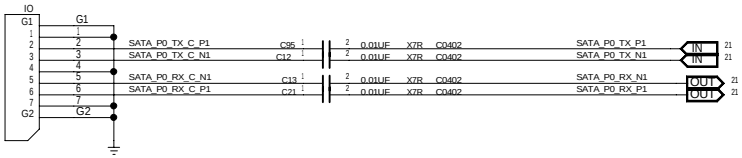
BOM NOTE:
WILL CHANGE TO DFHD07MS231

CONN7_ABA-SAT-054-KA4 THLF
J29



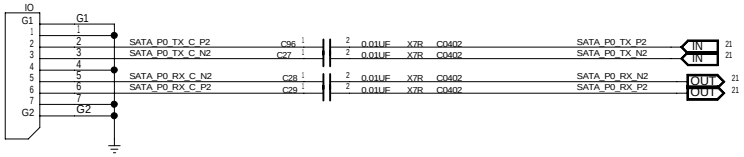
SATA1 CONN

CONN7_ABA-SAT-054-KA4 THLF
J31



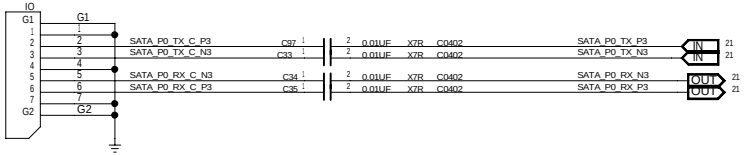
SATA2 CONN

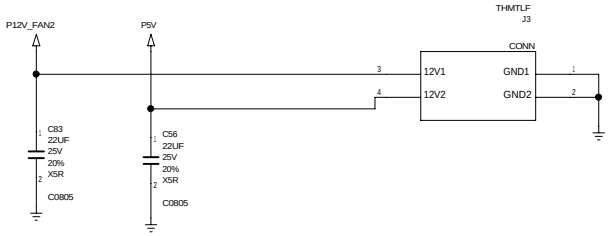
CONN7_ABA-SAT-054-KA4 THLF
J33

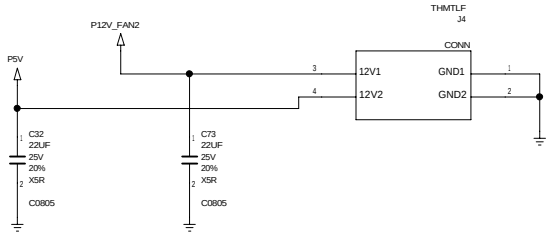


SATA3 CONN

CONN7_ABA-SAT-054-KA4 THLF
J34



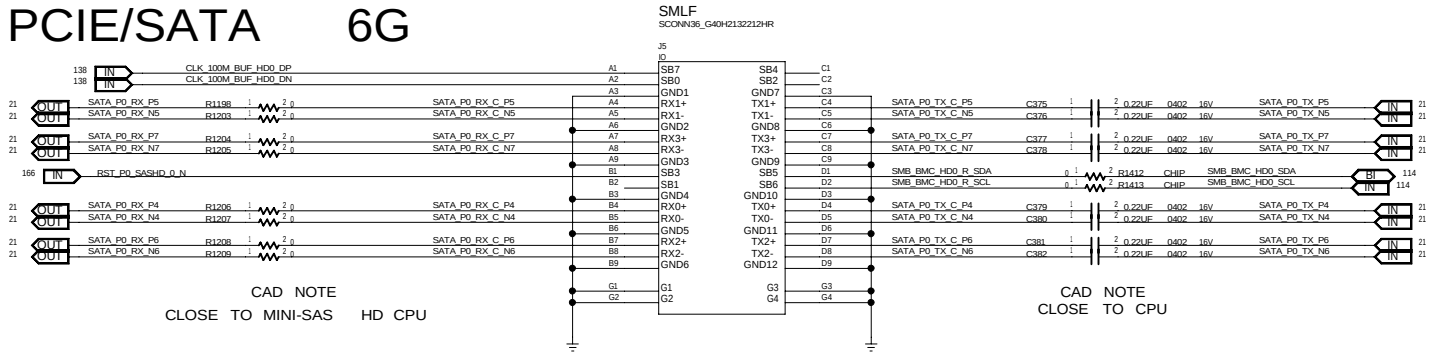




SATA CONN

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 20:21:59 2017	SHEET 149 OF 226

PCIE/SATA 6G

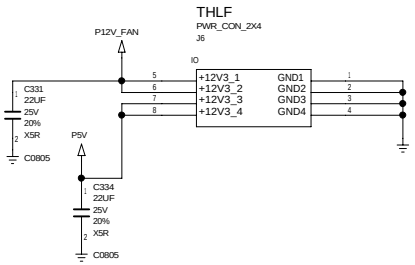


CAD NOTE
CLOSE TO MINI-SAS HD CPU

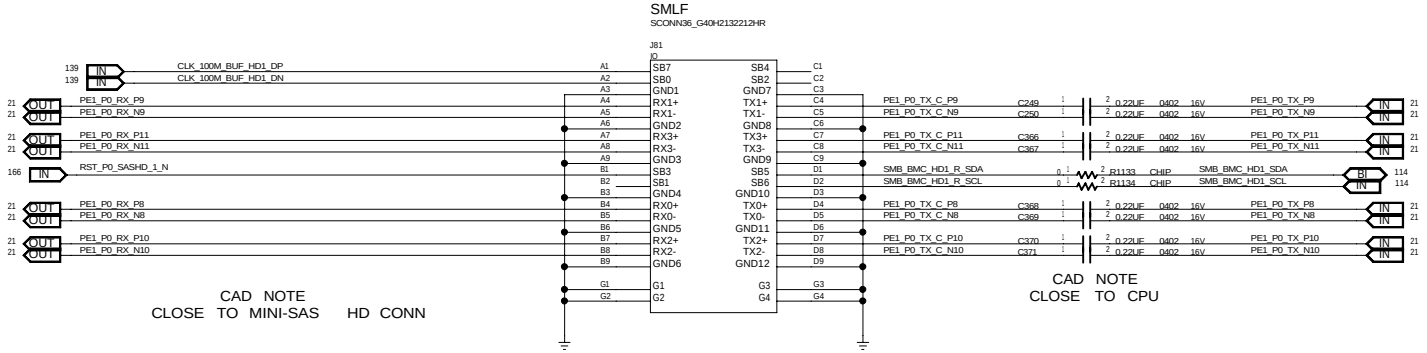
CAD NOTE
CLOSE TO CPU

MINI-SAS HD 0

BOM NOTE:
WILL CHANGE TO DFHS36FS109



PCIE ONLY

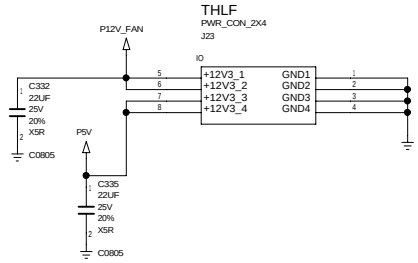


CAD NOTE
CLOSE TO MINI-SAS HD CONN

CAD NOTE
CLOSE TO CPU

MINI-SAS HD 1

BOM NOTE:
WILL CHANGE TO DFHS36FS109



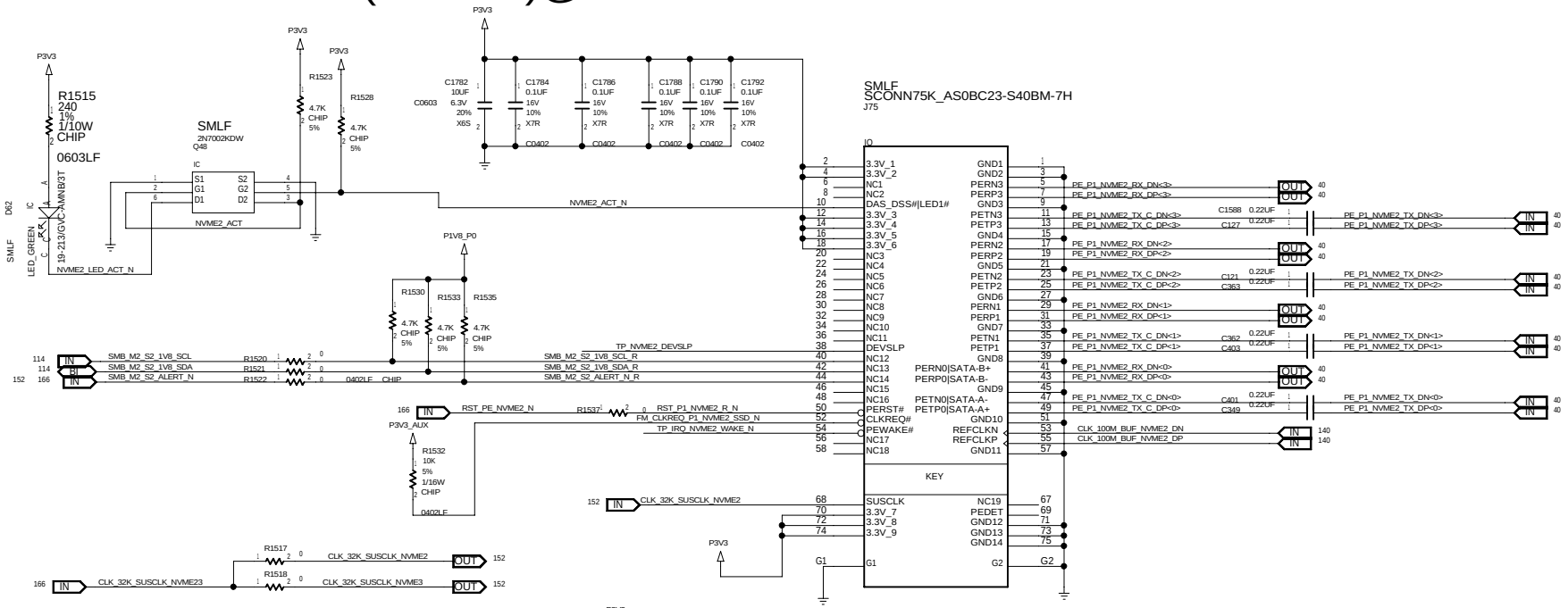
MINISAS HD FOR CPU0

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:59 2017
				SHEET 150 OF 226

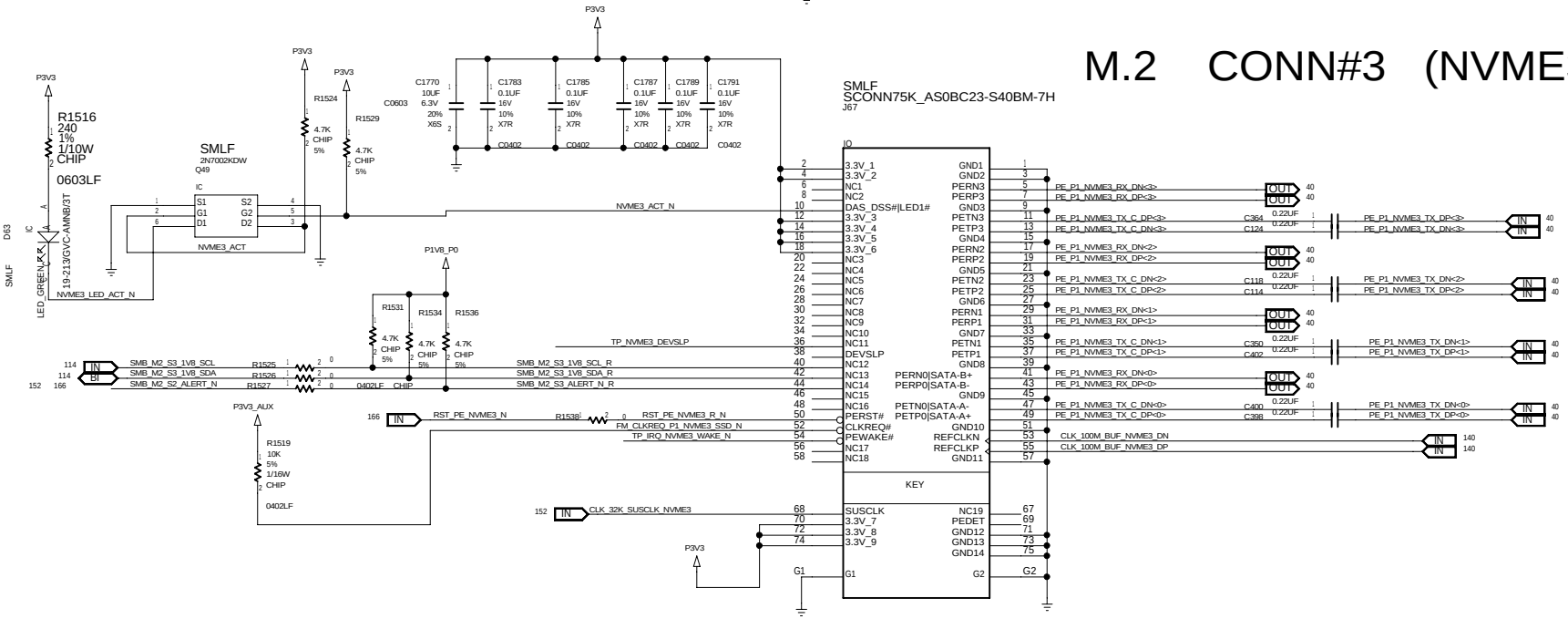
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Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:34:53 2017	SHEET 151 OF 226

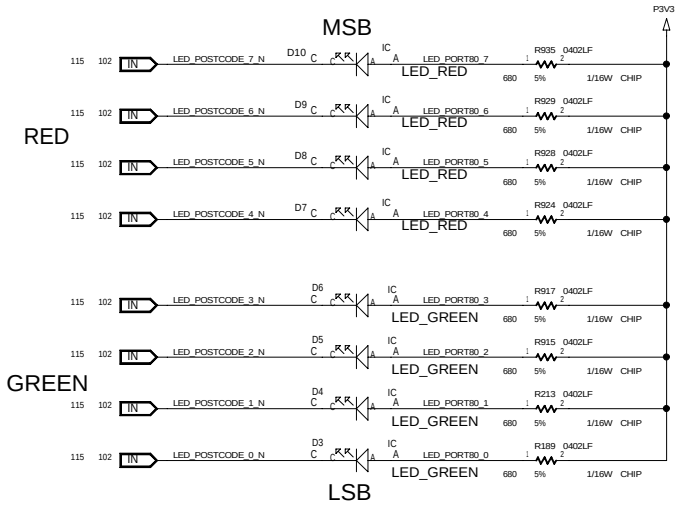
M.2 CONN#2 (NVME2)@CPU1



M.2 CONN#3 (NVME3)@CPU1

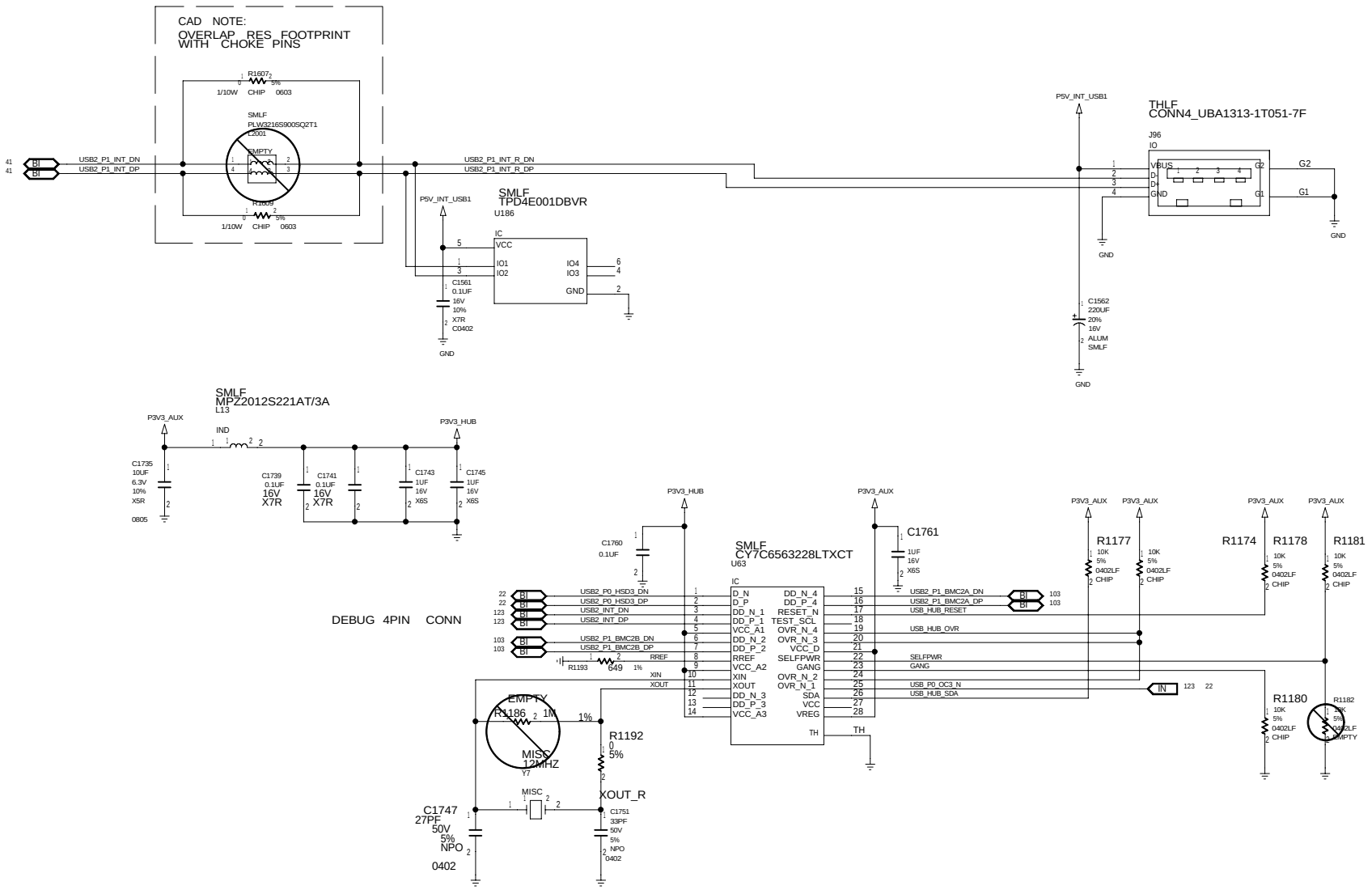


DEBUG PORT 80 LED



PORT80 LED

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:22:00 2017	SHEET 153 OF 226



USB2.0 INTERNAL

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER:		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:22:00 2017	SHEET 154 OF 226

SMLF
BCM57810SB0KFSBG
U24

EMPTY

1/9

P1V0_PCIERXVDDL IN 155

PCIE_RXVDDL_P03 P3
PCIE_RXVDDL_T03 T3
PCIE_RXVDDL_V03 V3
PCIE_RXVDDL_Y01 Y1
PCIE_RXVDDL_Y03 Y3
PCIE_RXVDDL_Y05 Y5
PCIE_RXVDDL_Y07 Y7
PCIE_RXVDDL_Y09 Y9

PCIE_TXVDDL_P20 P20
PCIE_TXVDDL_T20 T20
PCIE_TXVDDL_V20 V20
PCIE_TXVDDL_Y13 Y13
PCIE_TXVDDL_Y15 Y15
PCIE_TXVDDL_Y17 Y17
PCIE_TXVDDL_Y19 Y19
PCIE_TXVDDL_Y21 Y21

P1V0_PCIETXVDDL IN 155

IRQ_NIC_WAKE_R_N OUT 155 133 — R18 WAKE#
DL_ACTIVE_LED V18 TP_DL_ACTIVE_LED
PLAY_DEAD_NIC IN 155 — G3 PLAY_DEAD
PCIE_LINKUP_LED T19 TP_PCIE_LINK_LED
LAN_DISABLE IN 155 — L2 PCIE_DIS

EPIO_28|BSC_SEL_0 K16 SHARED_I2CSEL0 OUT 157
EPIO_29|BSC_SEL_1 M16 SHARED_I2CSEL1 OUT 157
BSC_SCL E3 SHARED_SCL OUT 157
BSC_SDA F3 SHARED_SDA OUT 157
P0_EXT_MDIO D2 TP_P0_EXT_MDIO
P0_EXT_MDC D1 TP_P0_EXT_MDC

CLK_100M_BUF_LAN_DN IN 139 — AB11 PCIEPLL_REFCLK_N
CLK_100M_BUF_LAN_DP IN 139 — AA11 PCIEPLL_REFCLK_P

RST_PE_NIC_N IN 166 — M21 CLKREQ#
TP_CLKREQ_N M22 PERST#

PE_P0_LAN_TX_C_DN<7:0> IN 155
PE_P0_LAN_TX_C_DP<7:0> IN 155

PCIE_RD0_N P1
PCIE_RD0_P P2
PCIE_RD1_N T1
PCIE_RD1_P T2
PCIE_RD2_N V1
PCIE_RD2_P V2
PCIE_RD3_N AB1
PCIE_RD3_P AA1
PCIE_RD4_N AB3
PCIE_RD4_P AA3
PCIE_RD5_N AB5
PCIE_RD5_P AA5
PCIE_RD6_N AB7
PCIE_RD6_P AA7
PCIE_RD7_N AB9
PCIE_RD7_P AA9

PCIE_TD7_P P21
PCIE_TD7_N P22
PCIE_TD6_P T21
PCIE_TD6_N T22
PCIE_TD5_P V21
PCIE_TD5_N V22
PCIE_TD4_P AA21
PCIE_TD4_N AB21
PCIE_TD3_P AA19
PCIE_TD3_N AB19
PCIE_TD2_P AA17
PCIE_TD2_N AB17
PCIE_TD1_P AA15
PCIE_TD1_N AB15
PCIE_TD0_P AA13
PCIE_TD0_N AB13

PE_P0_LAN_RX_DP<7:0> OUT 155
PE_P0_LAN_RX_DN<7:0> OUT 155

PE_P0_LAN_TX_DP<7:0> IN 21 — C1589–C1603 0.22UF 10% EMPTY 0402 16V — PE_P0_LAN_TX_C_DP<7:0> OUT 155
PE_P0_LAN_TX_DN<7:0> IN 21 — C1604–C1636 0.22UF EMPTY 0402 16V — PE_P0_LAN_TX_C_DN<7:0> OUT 155

PE_P0_LAN_RX_DP<7:0> IN 155 — C1637–C1666 0.22UF EMPTY 0402 10% 16V — PE_P0_LAN_RX_C_DP<7:0> OUT 21
PE_P0_LAN_RX_DN<7:0> IN 155 — C1667–C1674 0.22UF EMPTY 0402 16V — PE_P0_LAN_RX_C_DN<7:0> OUT 21

PD_FUNC_HIDE IN 155 — K2 FUNC_HIDE
K4 NC_K04
K6 NC_K06
PORT_SWAP IN 155 — A4 2PORT_SWAP
TP_XTAL_MON C10 XTAL_MON
XTAL_NIC_IN A8 XTAL_N
XTAL_NIC_OUT A9 XTAL_P

SI A1 EE_NIC_SI IN 156
SO A2 EE_NIC_SO_R OUT 156
CS# A3 EE_NIC_CS_N_R OUT 156
SCLK B1 EE_NIC_SCLK_R OUT 156

XTAL_BYPASS K5 XTAL_BYPASS — R1353 EMPTY 1/16W 5% 4.7K 0402LF

MISC
25MHZ
Y6 EMPTY
C336 27PF 50V 5% EMPTY 0402
C341 27PF 50V 5% EMPTY 0402
XTAL_NIC_R_IN — R1348 EMPTY 1/16W 0402LF 22 1%
XTAL_NIC_R_OUT — R1349 EMPTY 1/16W 0402LF 22 1%

BOM NOTE:
QNP CHANGE TO AJ578100T01(VENDOR CODE CHANGE FROM BCM TO QLG)
MPN KEEP BCM57810SB0KFSBG

SO - INTERNAL PULL-UP RESISTOR (IPU); 1
SI - INTERNAL PULL-DOWN RESISTOR (IPD); 0
CS# - INTERNAL PULL-UP RESISTOR (IPU); 1
SCLK - INTERNAL PULL-UP RESISTOR (IPU); 1

P3V3_AUX
R1343 4.7K EMPTY 5% — PORT_SWAP OUT 155
R1344 4.7K EMPTY 5%

P3V3_AUX
R1346 4.7K EMPTY 5%
0402LF
R1345 EMPTY — IRQ_NIC_WAKE_N OUT 126 — IRQ_NIC_WAKE_R_N IN 155 133

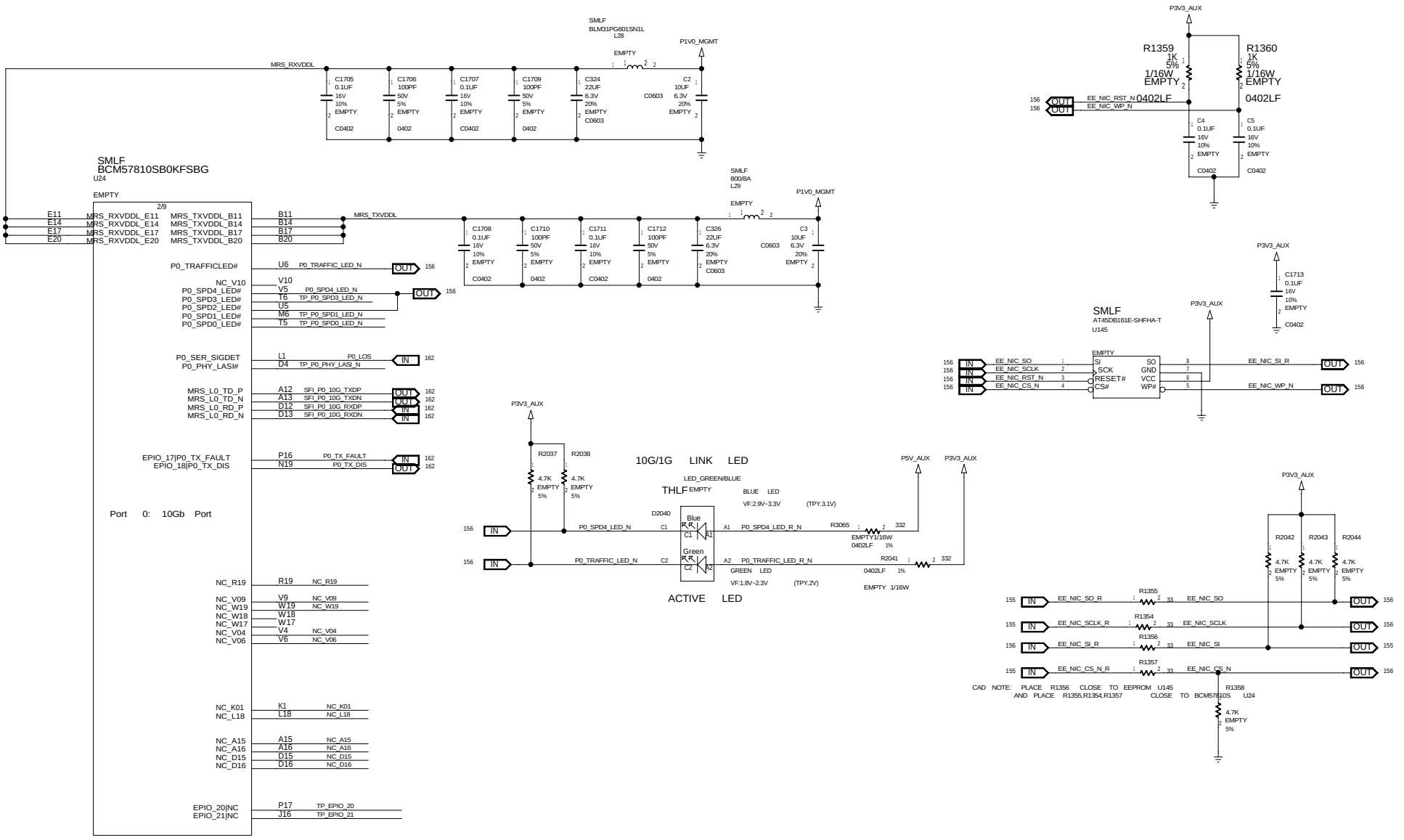
PLAY_DEAD_NIC OUT 155 — PLAY_DEAD INTERNAL PD
PD_FUNC_HIDE OUT 155 — FUNC_HIDE INTERNAL PD
LAN_DISABLE OUT 155 — LAN_DIS INTERNAL PD
R1350 R1351 4.7K EMPTY 5% R1352 4.7K EMPTY 5% 4.7K EMPTY 5%

P1V0_MGMT
SMLF 800/8A L26
EMPTY
C1686 10UF 6.3V 20% EMPTY C0603
C1687 22UF 6.3V 20% EMPTY C0603
C484 0.1UF 16V 10% EMPTY C0402
C1691 100PF 50V 5% EMPTY 0402
C1693 0.1UF 16V 10% EMPTY C0402
C1695 100PF 50V 5% EMPTY 0402
C1697 0.1UF 16V 10% EMPTY C0402
C1699 100PF 50V 5% EMPTY 0402
C1701 0.1UF 16V 10% EMPTY C0402
C1703 100PF 50V 5% EMPTY 0402
P1V0_PCIETXVDDL OUT 155

CAD NOTE: CLOSE TO U24

P1V0_MGMT
SMLF 800/8A L27
EMPTY
C1 10UF 6.3V 20% EMPTY C0603
C30 22UF 6.3V 20% EMPTY C0603
C1690 0.1UF 16V 10% EMPTY C0402
C1692 100PF 50V 5% EMPTY 0402
C1694 0.1UF 16V 10% EMPTY C0402
C1696 100PF 50V 5% EMPTY 0402
C1698 0.1UF 16V 10% EMPTY C0402
C1700 100PF 50V 5% EMPTY 0402
C1702 0.1UF 16V 10% EMPTY C0402
C1704 100PF 50V 5% EMPTY 0402
P1V0_PCIERXVDDL OUT 155

Quanta | DEPARTMENT CCBU | DESIGNER | REVIEWER | PROJCET <Q_PROJ> | DOCUMENT NUMBER <Q_NUMBER> | REV <Q_REV>
SIZE C | DATE Fri Dec 15 20:22:00 2017 | SHEET 155 OF 226



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SMLF
BCM57810SB0KFSBG
U24

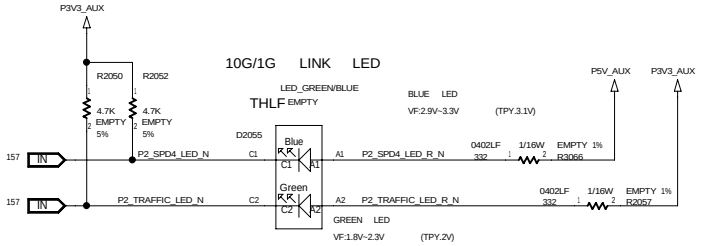
EMPTY

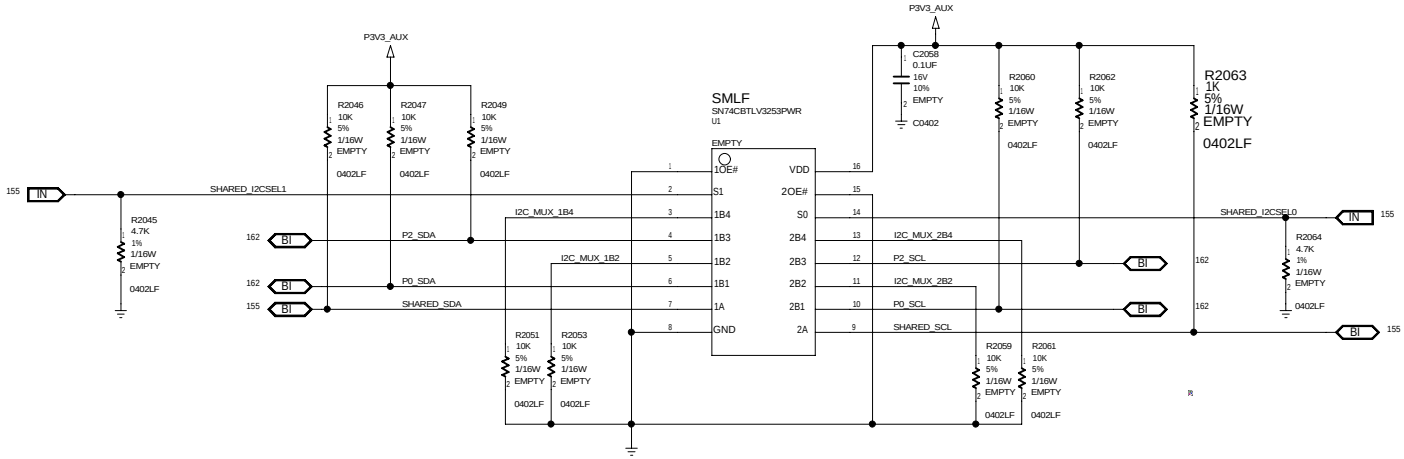
9/9

P2_TRAFFICLED#	C5	P2_TRAFFIC_LED_N	OUT	157
NC_B05	B5	NC_B05		
P2_SPD4_LED#	F7	P2_SPD4_LED_N	OUT	157
P2_SPD3_LED#	H6	TP_P2_SPD3_LED_N		
P2_SPD2_LED#	P5			
P2_SPD1_LED#	J6	TP_P2_SPD1_LED_N		
P2_SPD0_LED#	B6	TP_P2_SPD0_LED_N		
P2_SER_SIGDET	M1	P2_LOS	OUT	162
P2_PHY_LASI#	C3	TP_P2_PHY_LASI_N		
MRS_L2_TD_P	A18	SFI_P2_10G_TXDP	OUT	162
MRS_L2_TD_N	A19	SFI_P2_10G_TXDN	OUT	162
MRS_L2_RD_P	D18	SFI_P2_10G_RXDP	IN	162
MRS_L2_RD_N	D19	SFI_P2_10G_RXDN	IN	162
EPIO_23|P2_TX_FAULT	R16	P2_TX_FAULT	IN	162
EPIO_12|P2_TX_DIS	E5	P2_TX_DIS	OUT	162

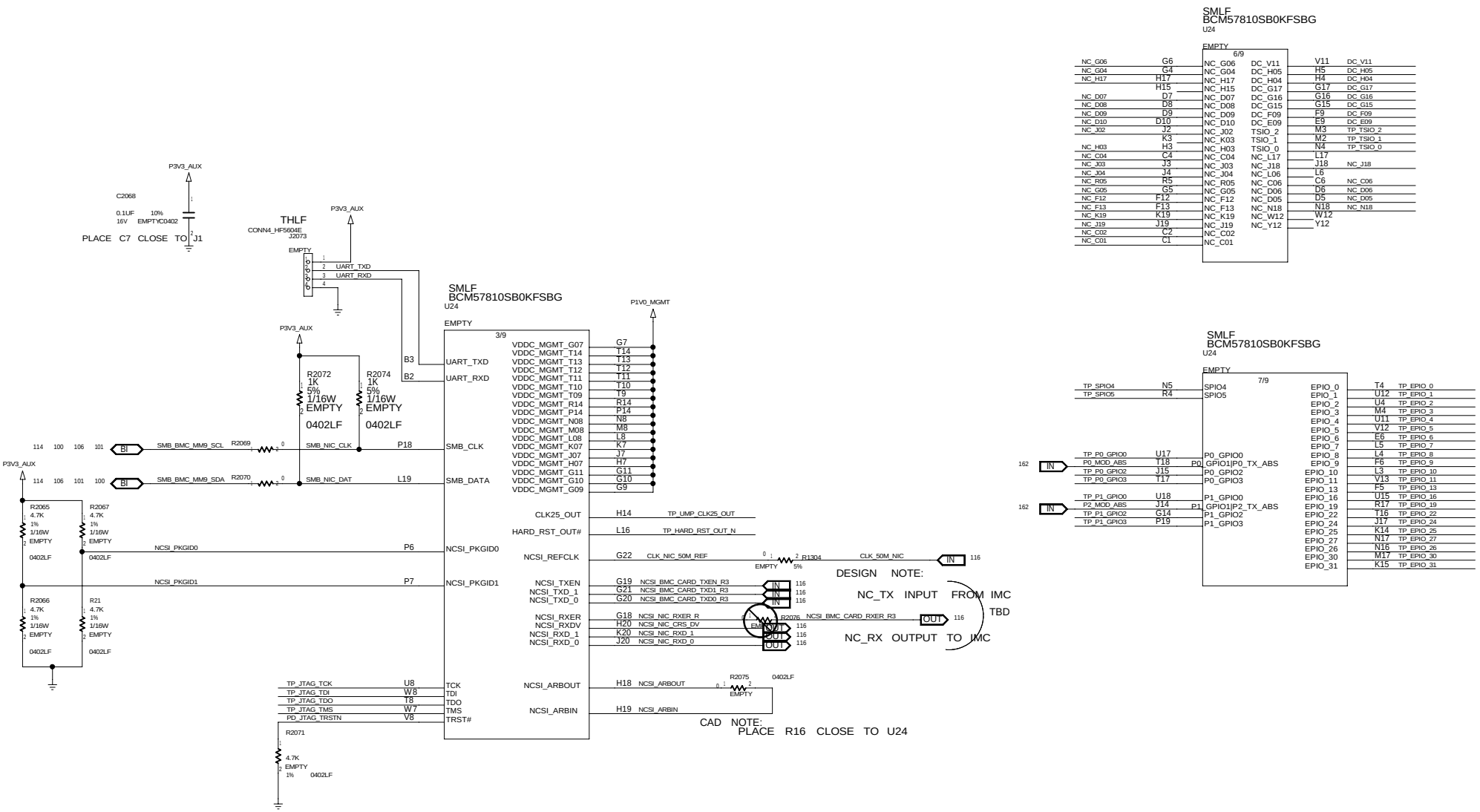
Port 1: 10Gb Port

NC_N06	N6	NC_N06	
TSIO_3	A6	TP_TSIO_3	
NC_A05	A5	NC_A05	
NC_M05	M5		
NC_H02	H2	NC_H02	
NC_E04	E4	NC_E04	
NC_F04	F4	NC_F04	
NC_H22	H22	NC_H22	
NC_K18	K18	NC_K18	
NC_A21	A21	NC_A21	
NC_A22	A22	NC_A22	
NC_D21	D21	NC_D21	
NC_D22	D22	NC_D22	
EPIO_14|NC	U9	TP_EPIO_14	
EPIO_15|NC	U10	TP_EPIO_15	

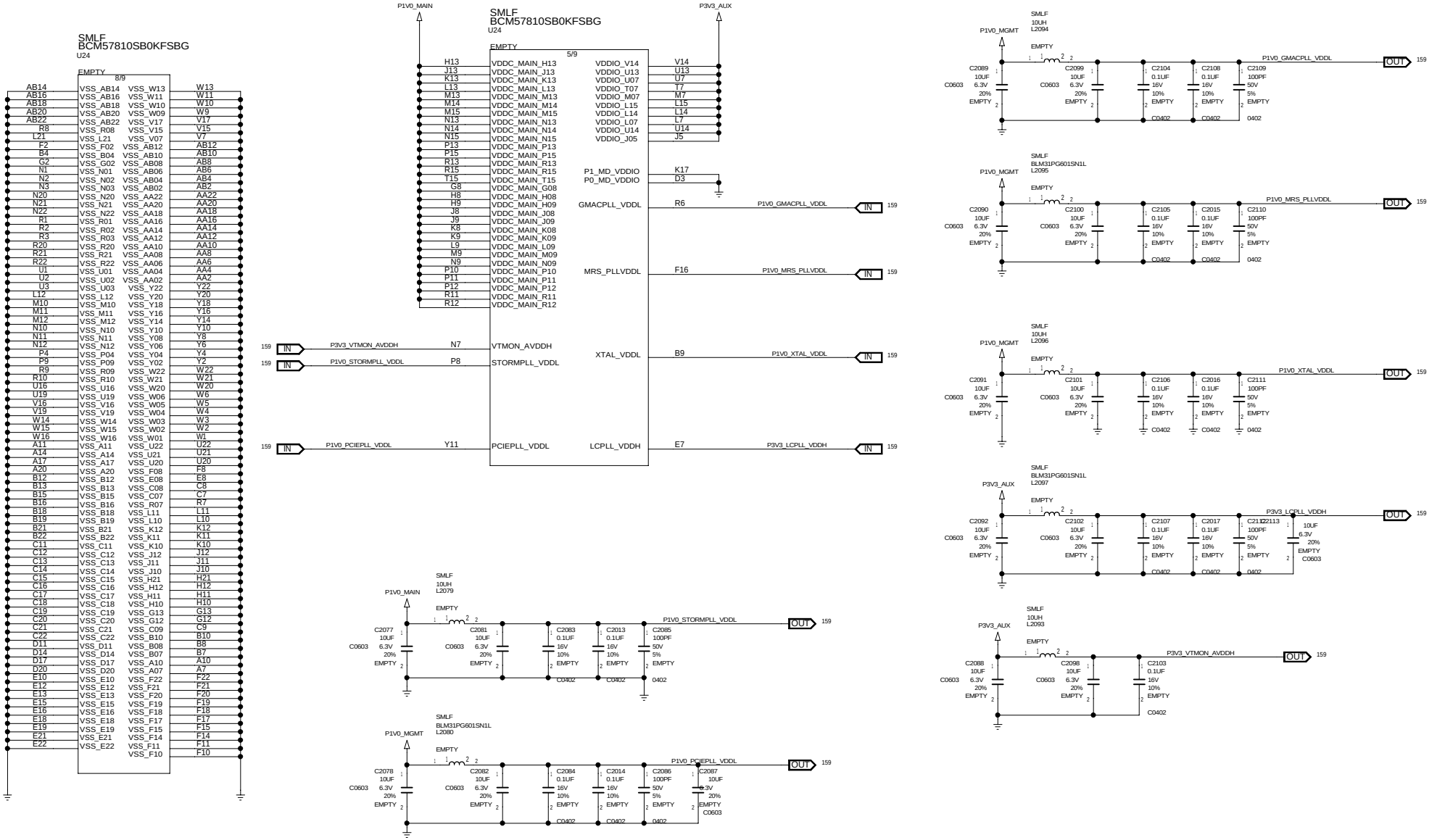




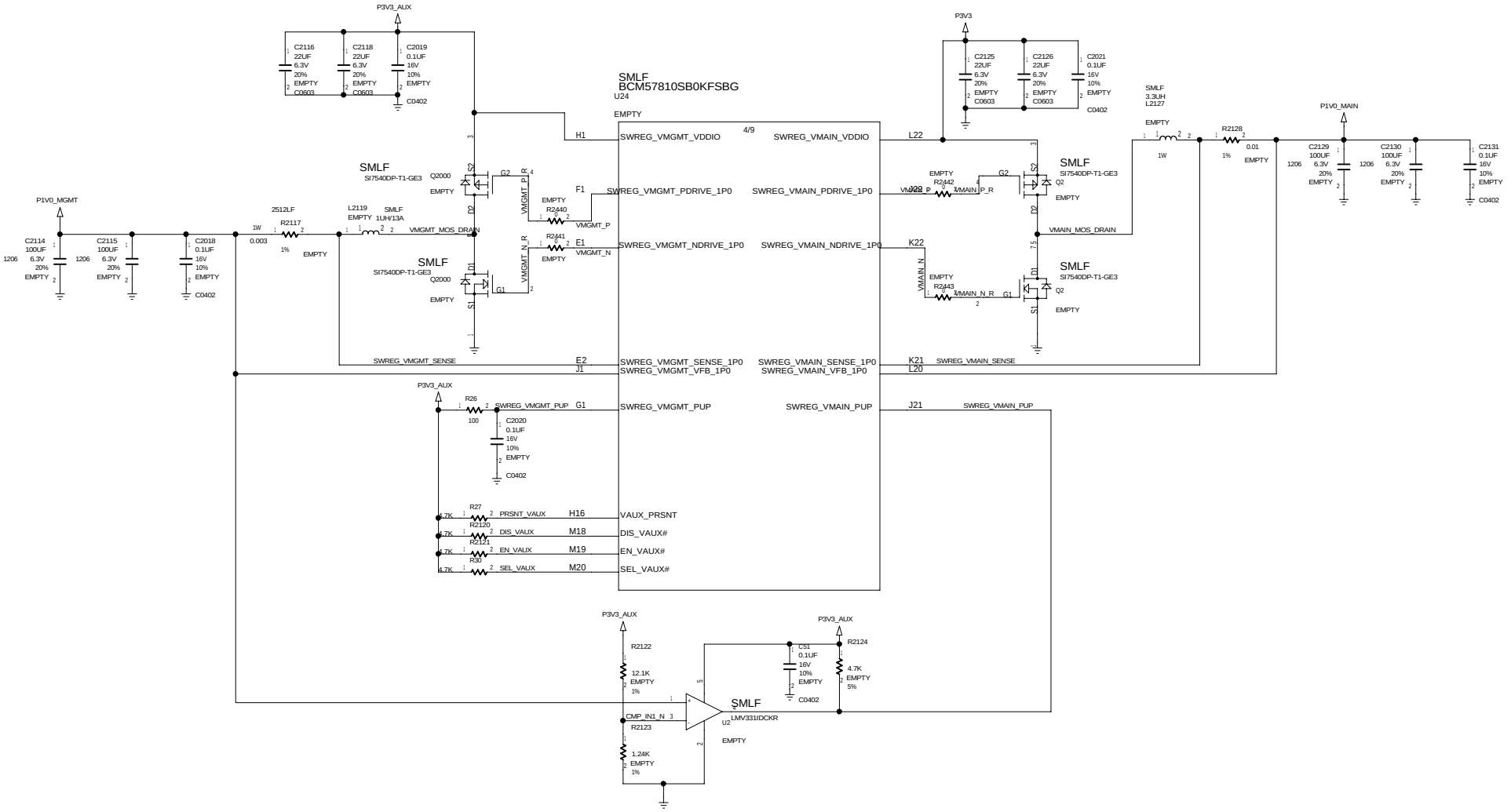
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		REVIEWER	SIZE C DATE Fri Dec 15 20:22:01 2017	SHEET 157 OF 226



Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER:		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:22:01 2017	SHEET 158 OF 226



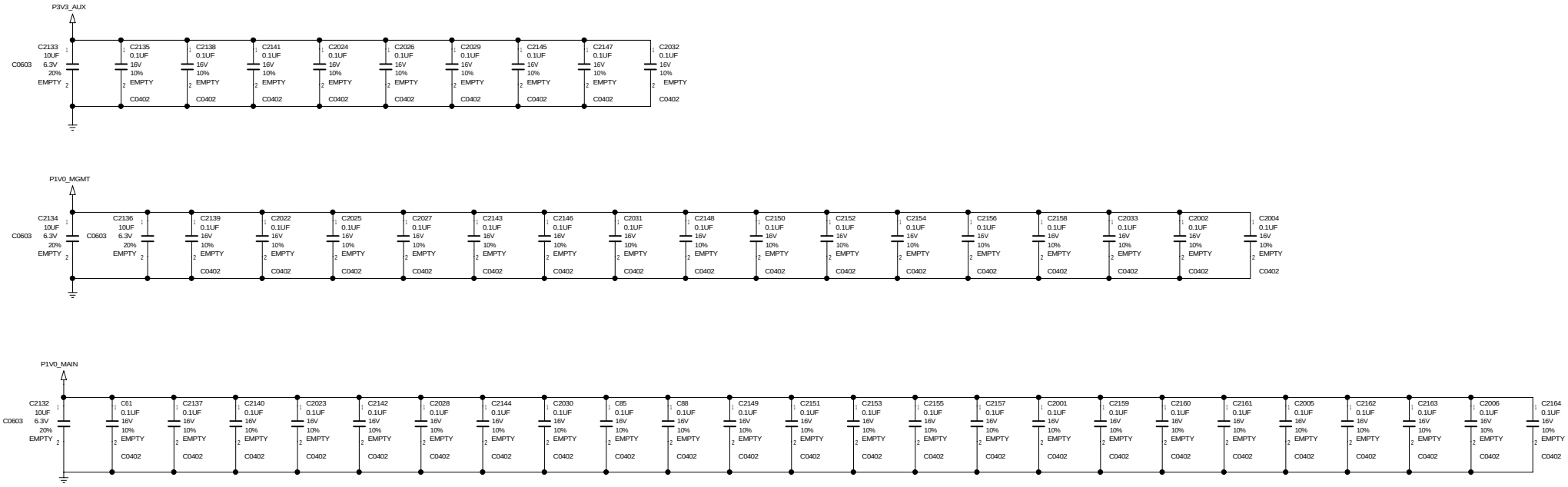
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:01 2017	SHEET 159 OF 226



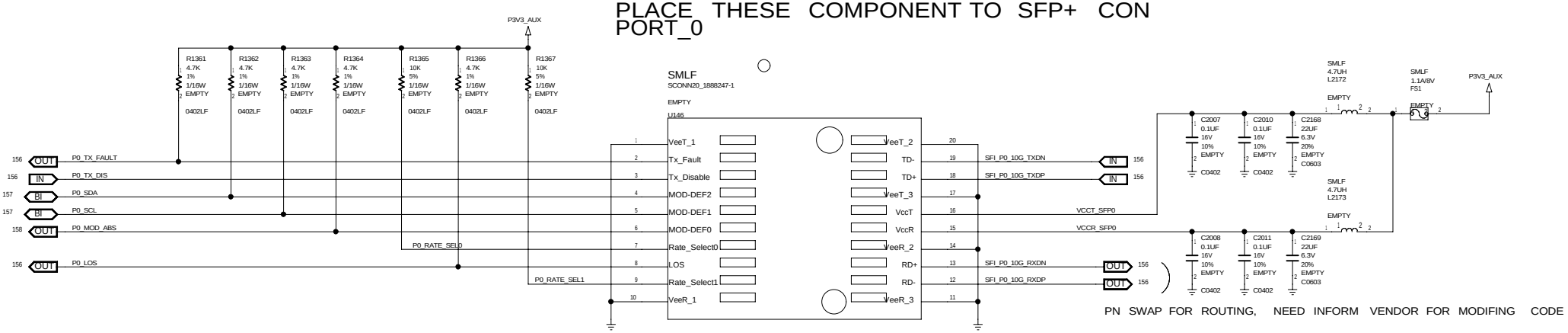
BCM57810 6 of 10

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:01 2017	SHEET 160 OF 226

CAD NOTE: PLACE THESE CAPACITORS IN THIS PAGE CLOSE TO U24

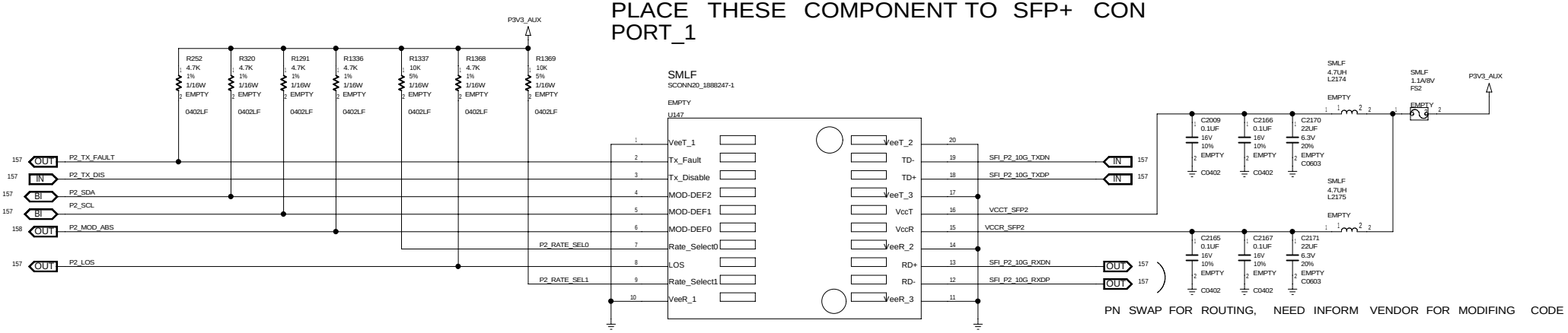


PLACE THESE COMPONENT TO SFP+ CON PORT_0



PN SWAP FOR ROUTING, NEED INFORM VENDOR FOR MODIFING CODE

PLACE THESE COMPONENT TO SFP+ CON PORT_1



PN SWAP FOR ROUTING, NEED INFORM VENDOR FOR MODIFING CODE

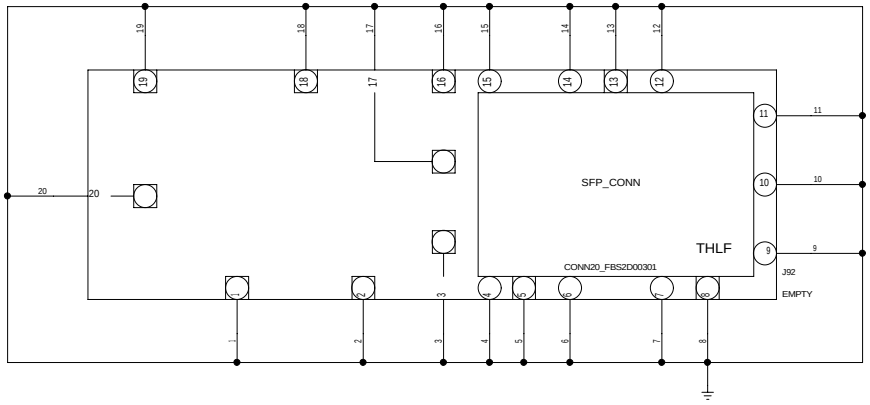
HEATSINK FOR BCM57810

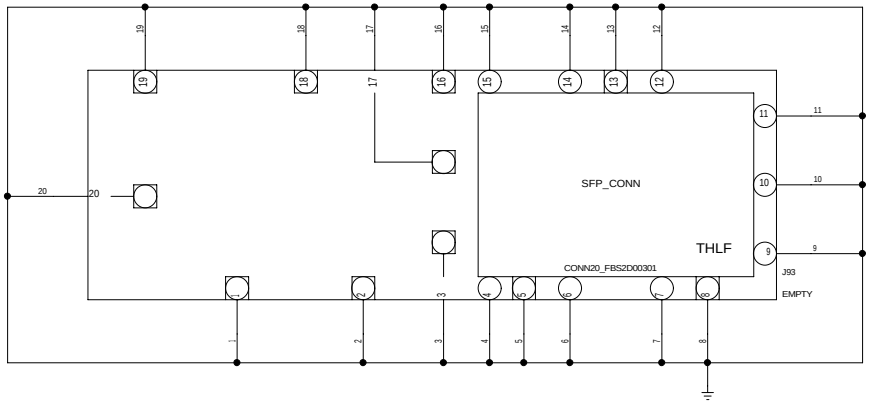
TP93
EMPTY

HEATSINK SCREW

TH
H2176
EMPTY

TH
H2179
EMPTY





Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:02 2017
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Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
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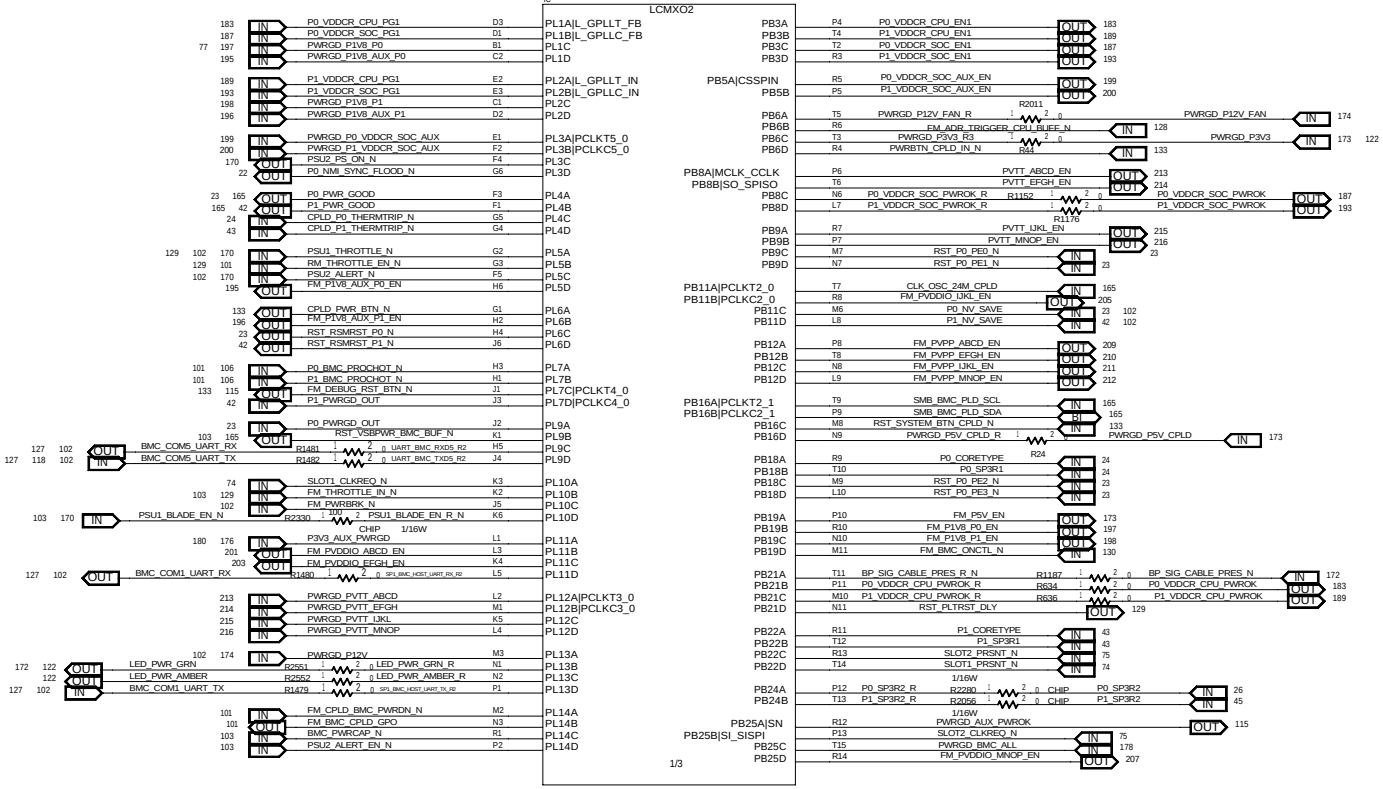
SMLF

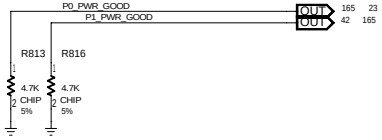
LCMXO2-1200UHC-4FTG256C

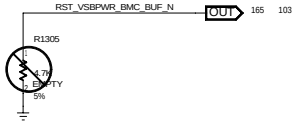
U32

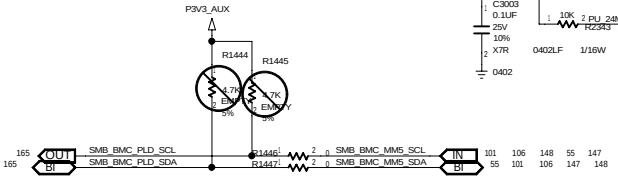
IC

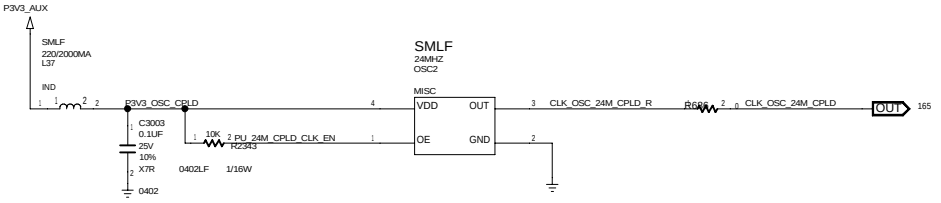
LCMXO2





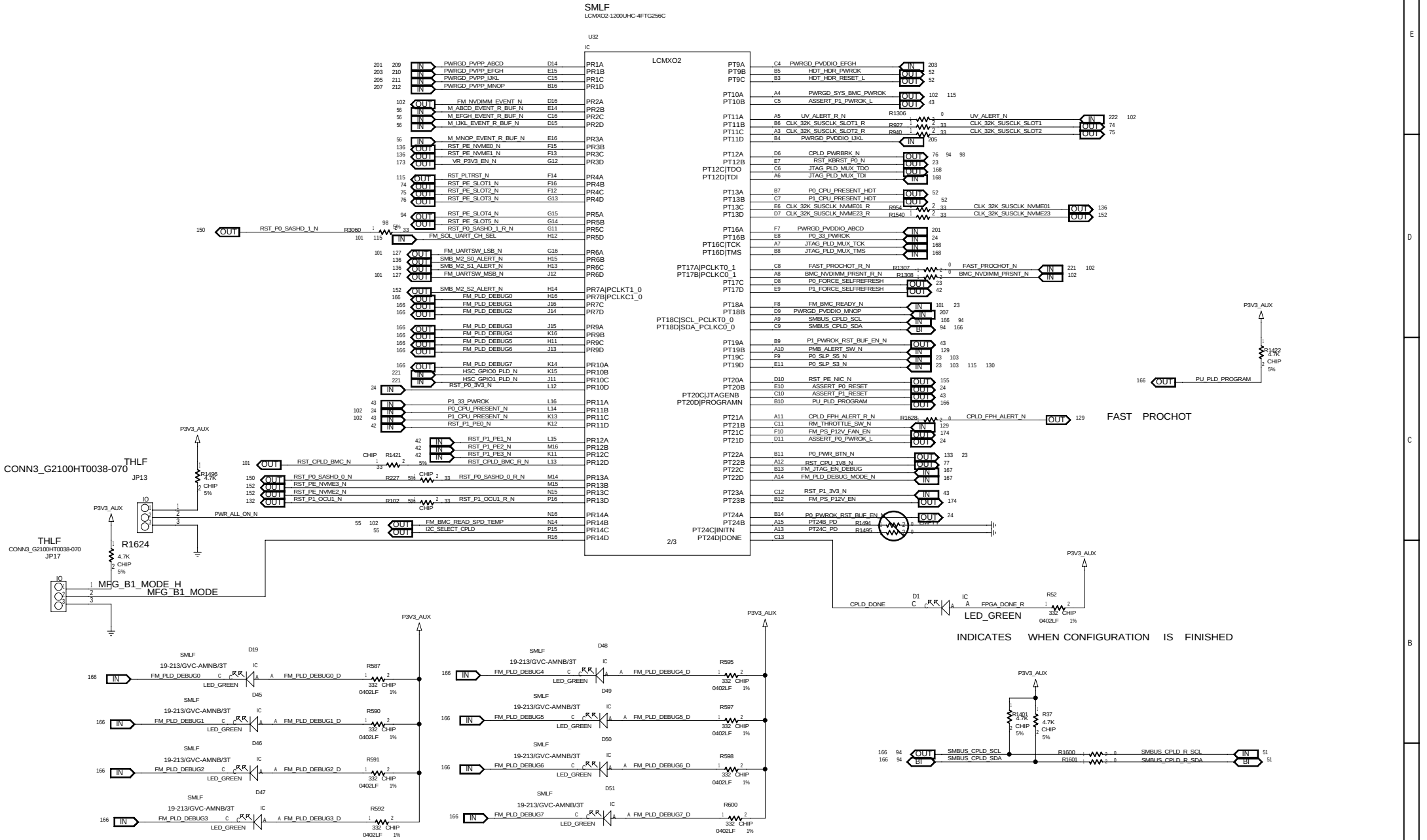






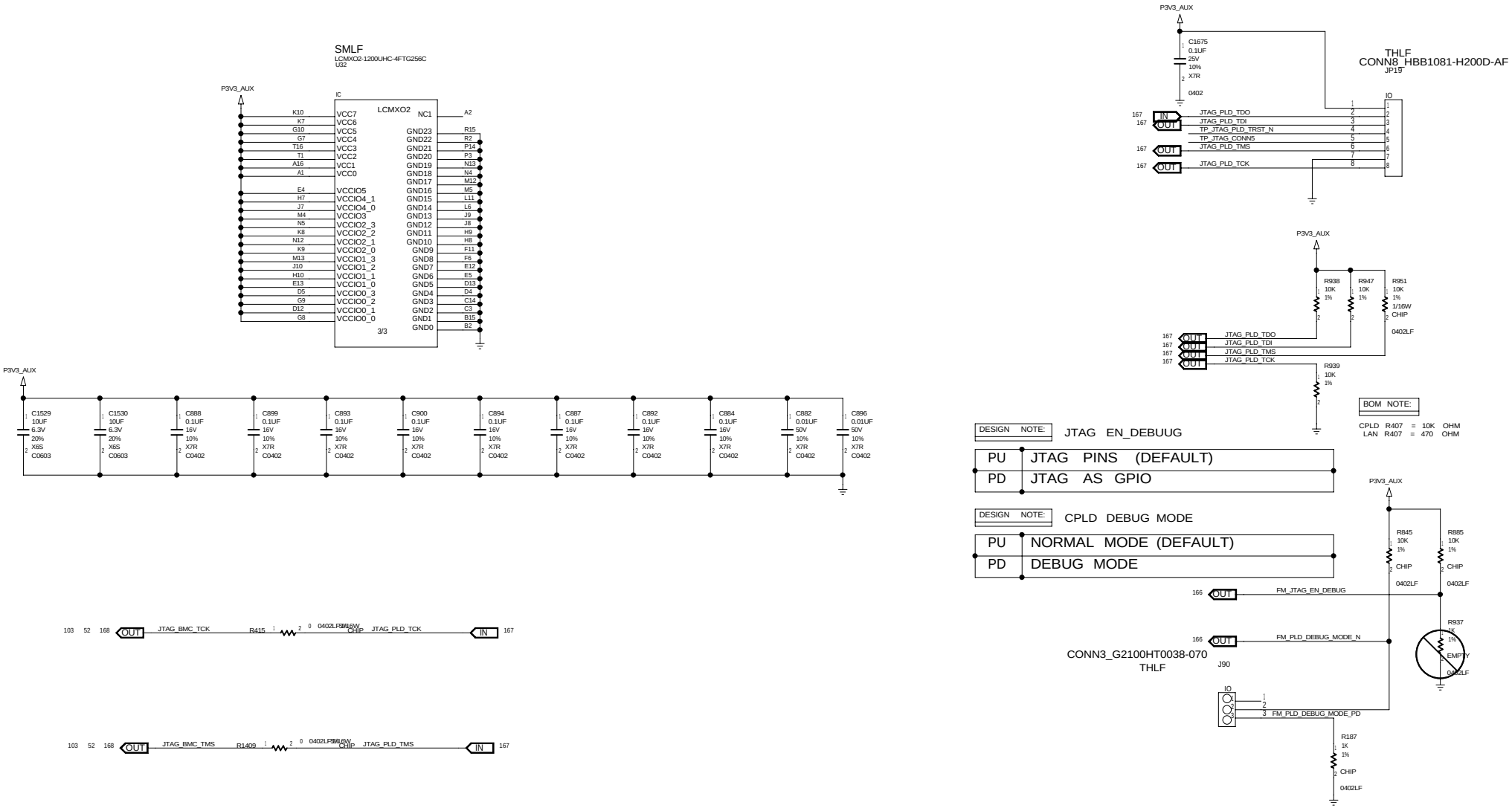
CPLD 1/3

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			REV: <Q_REV>
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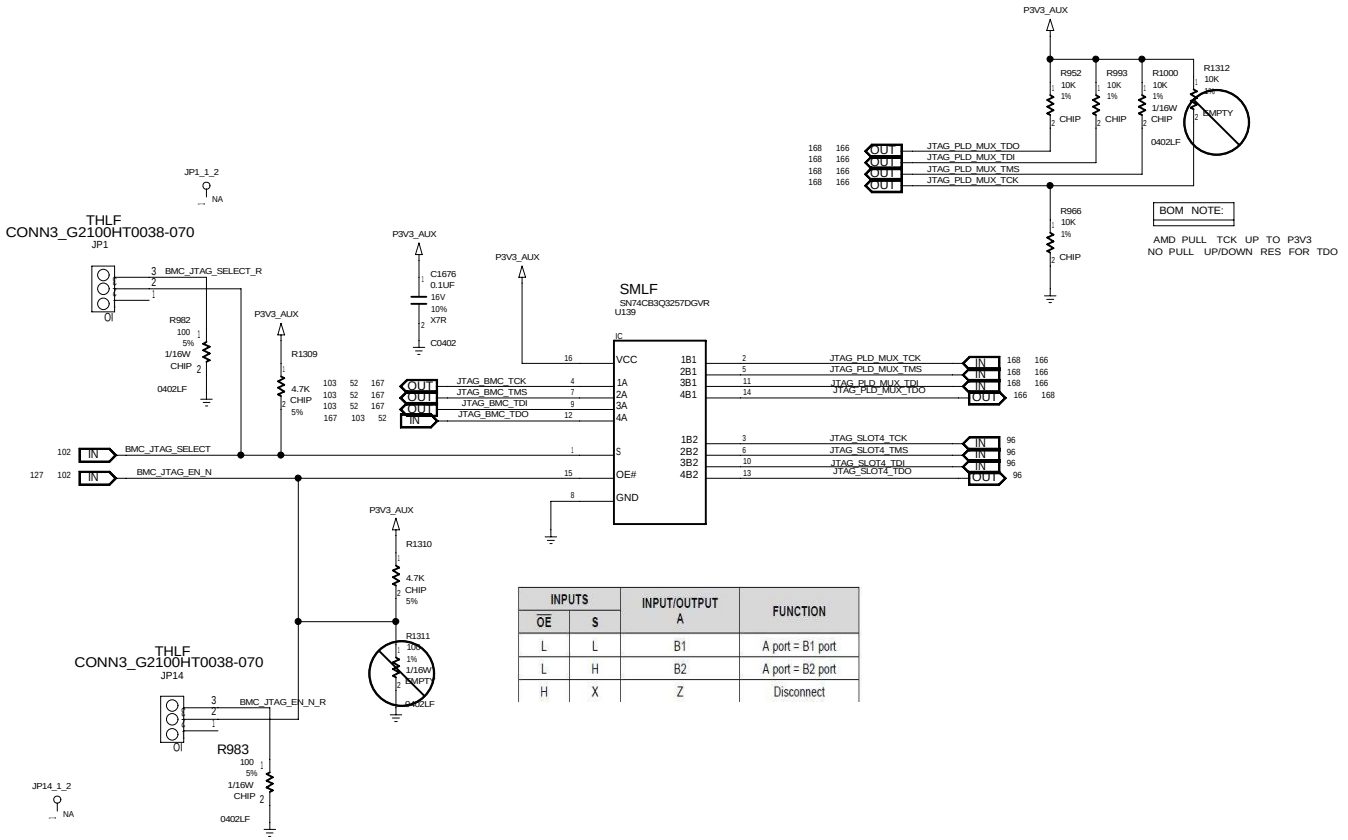
CPLD 2/3

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CPLD 3/3

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
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INPUTS		INPUT/OUTPUT	FUNCTION
$\overline{OE}$	S	A	
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

BMC JTAG

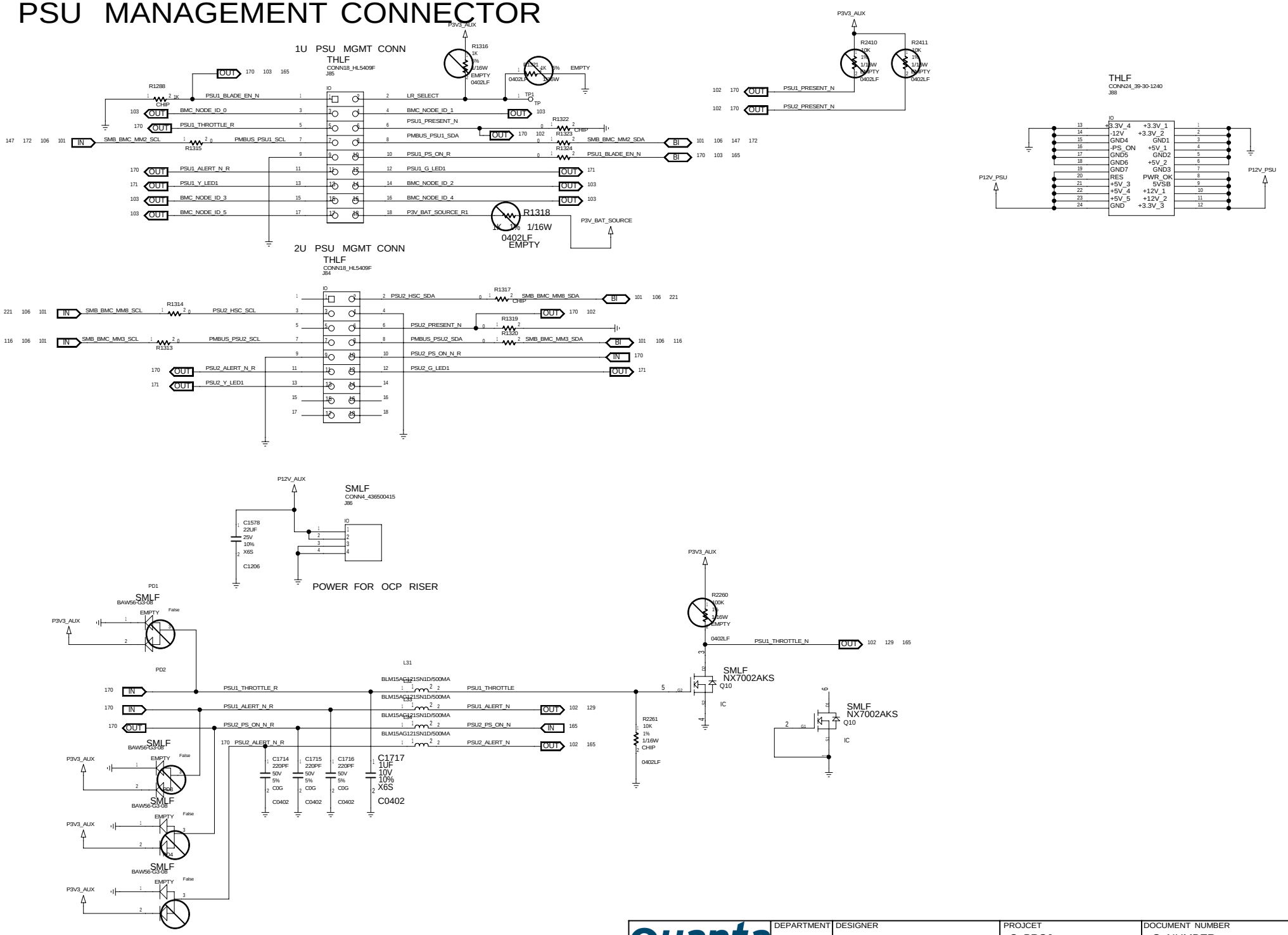
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		REVIEWER:	SIZE: C	DATE: Fri Dec 15 20:22:02 2017	SHEET 168 OF 226

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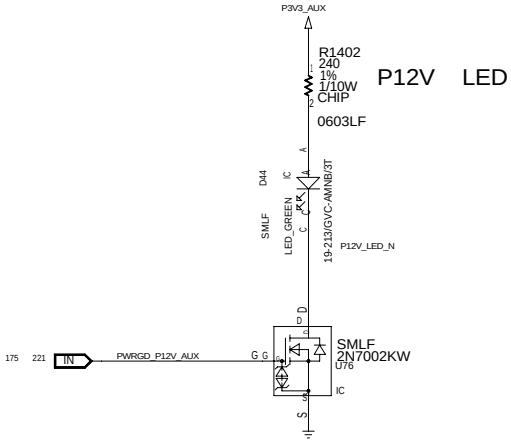
REV: <Q_REV>

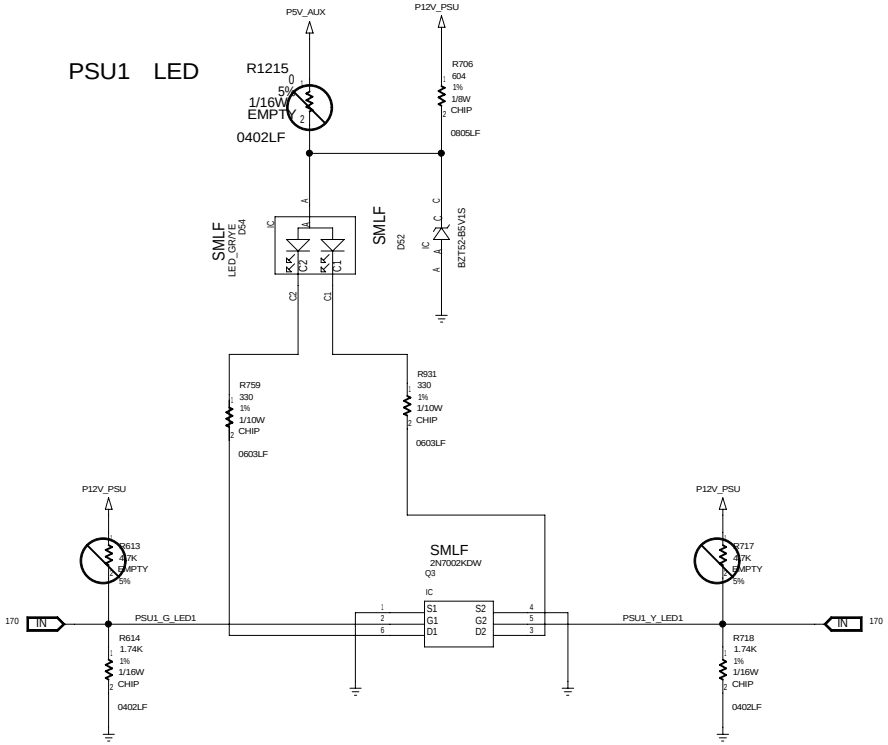
PSU MANAGEMENT CONNECTOR

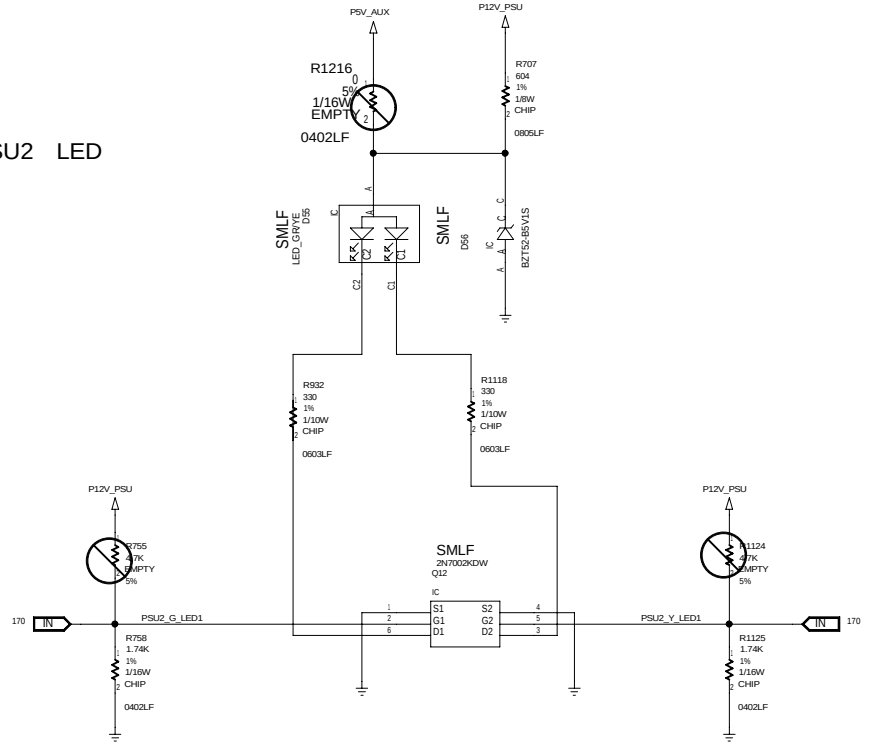


POWER CONNECTORS

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:22:03 2017
			REV: <Q_REV>	SHEET 170 OF 226

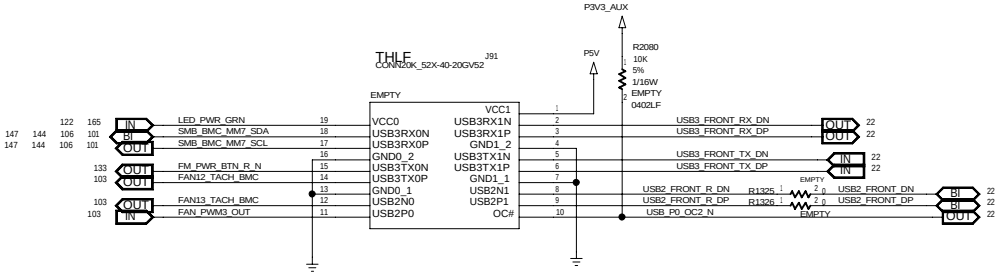


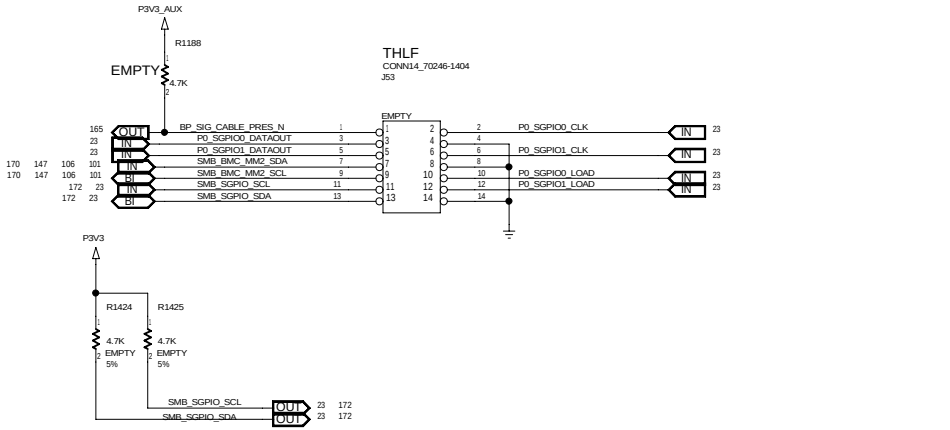




PSU & P12V LED

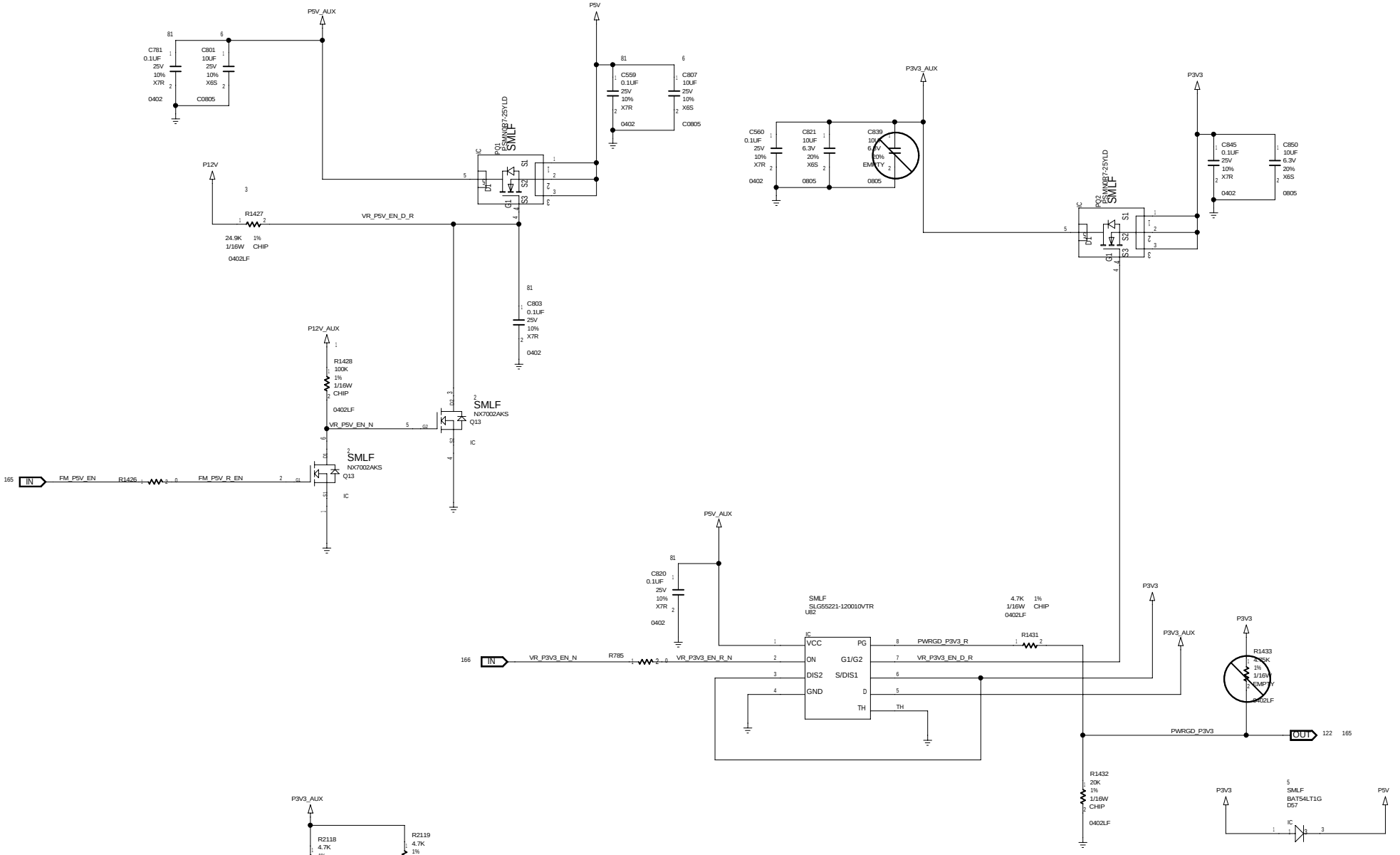
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		REVIEWER:	SIZE: C DATE: Fri Dec 15 20:21:19 2017	SHEET 171 OF 226





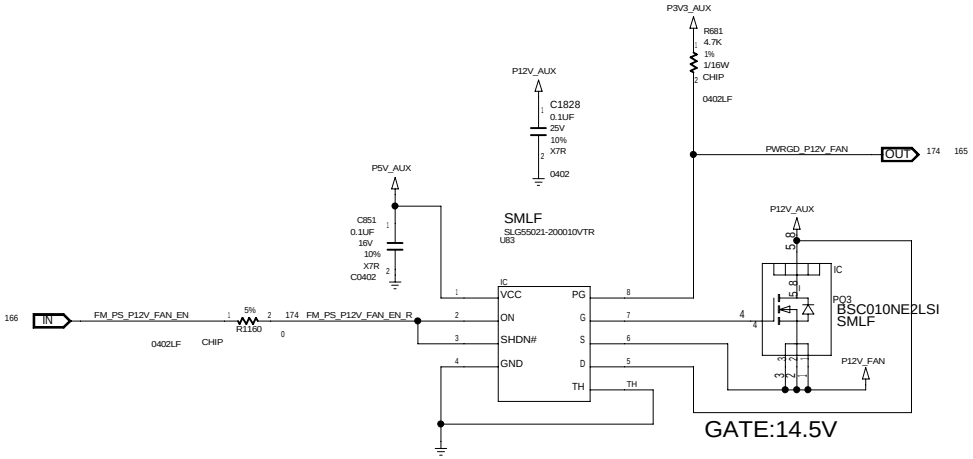
FRONT CONN

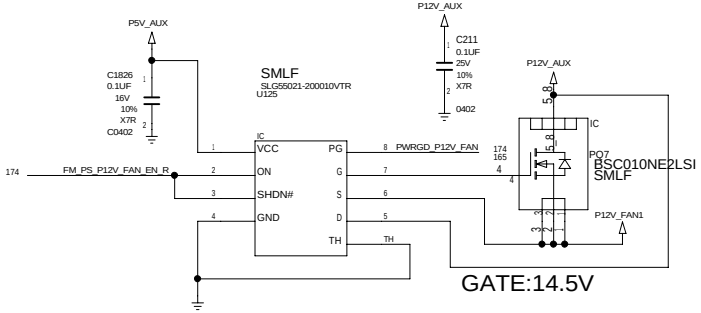
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				SHEET 172 OF 226

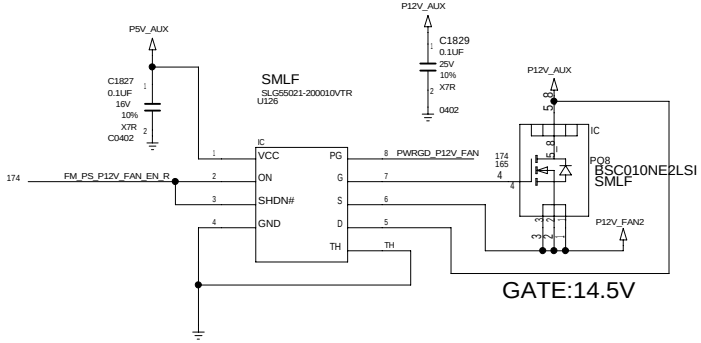


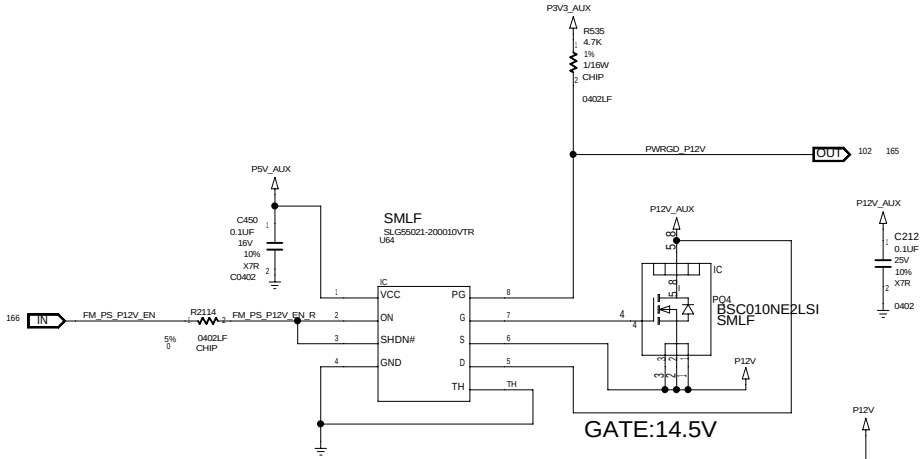
P5V & P3V3

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
	SIZE: C	DATE: Fri Dec 15 20:22:03 2017	SHEET 173 OF 226

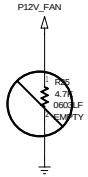












P12V & P12V_FAN

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:25 2017	SHEET 174 OF 226

DESIGN NOTE:
OUTPUT VOLTAGE = 5V+/-5%
OUTPUT RIPPLE&NOISE<50MV
TRANSIENT TOLERANCE=500MV
TDC = 19.2A
MAX CURRENT = 24A
OVER-CURRENT PROTECTION (MAX RATING*1.3)=31.2A
CURRENT STEP = 9A
SLEW RATE = 2.5A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 85% @ TDC

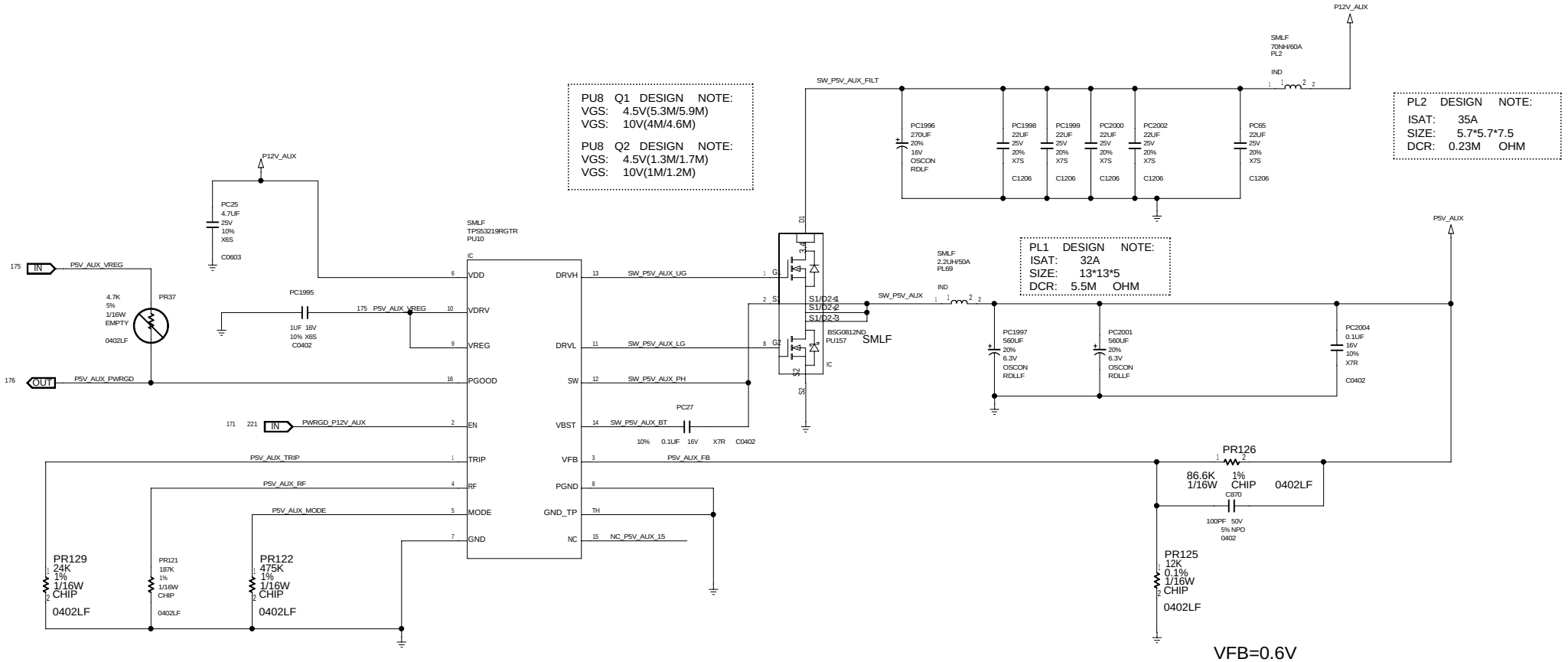
P5V_AUX VR

PU8 Q1 DESIGN NOTE:
VGS: 4.5V(5.3M/5.9M)
VGS: 10V(4M/4.6M)

PU8 Q2 DESIGN NOTE:
VGS: 4.5V(1.3M/1.7M)
VGS: 10V(1M/1.2M)

PL2 DESIGN NOTE:
ISAT: 35A
SIZE: 5.7*5.7*7.5
DCR: 0.23M OHM

PL1 DESIGN NOTE:
ISAT: 32A
SIZE: 13*13*5
DCR: 5.5M OHM

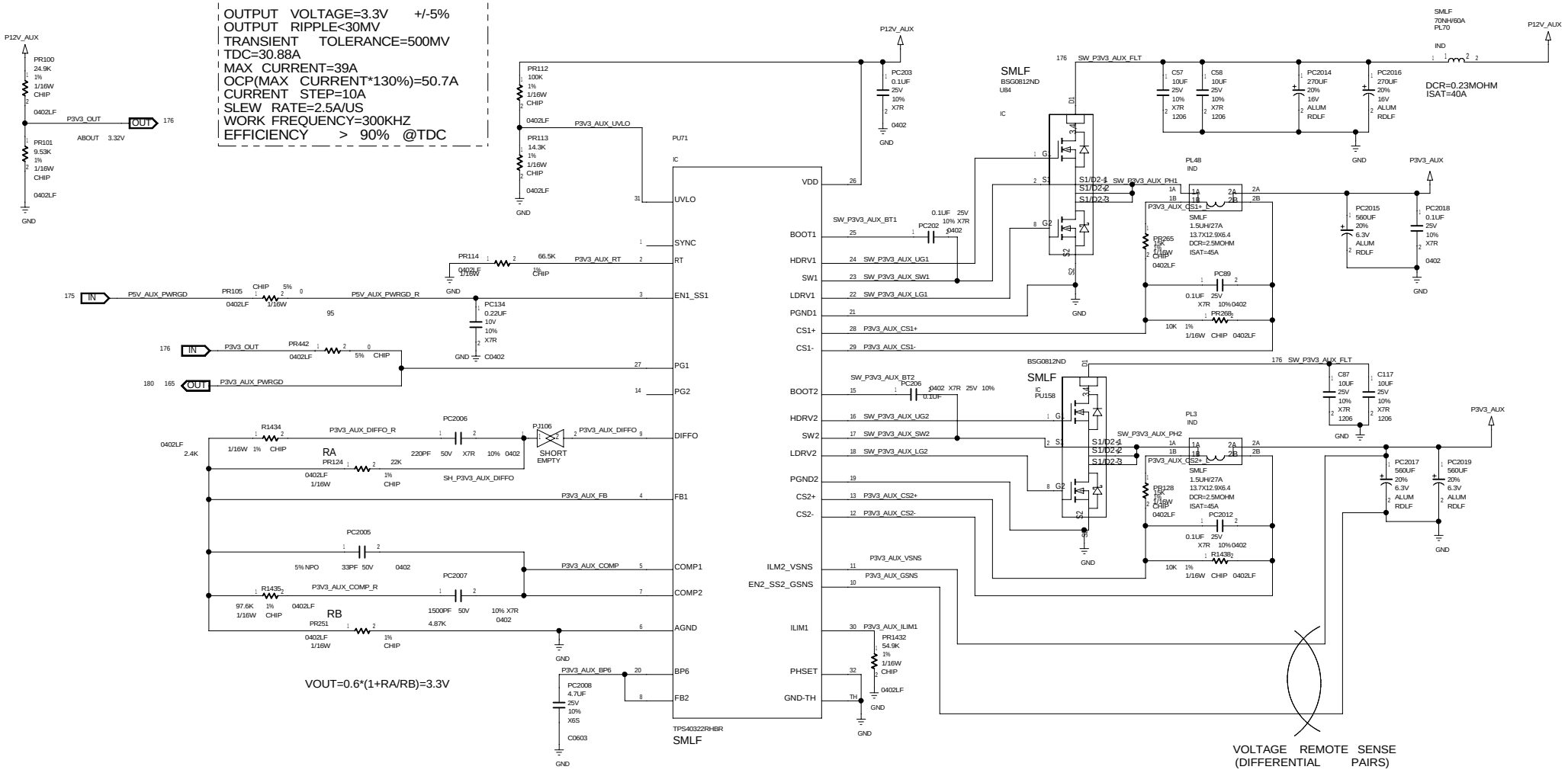


VFB=0.6V
VO=0.6(1+RA/RB)=4.93V
VOUT(REAL) = 4.98V

P3V3_AUX VR

DESIGN SPECIFICATION

OUTPUT VOLTAGE=3.3V +/-5%
OUTPUT RIPPLE<30MV
TRANSIENT TOLERANCE=500MV
TDC=30.88A
MAX CURRENT=39A
OCP(MAX CURRENT*130%)=50.7A
CURRENT STEP=10A
SLEW RATE=2.5A/US
WORK FREQUENCY=300KHZ
EFFICIENCY > 90% @TDC

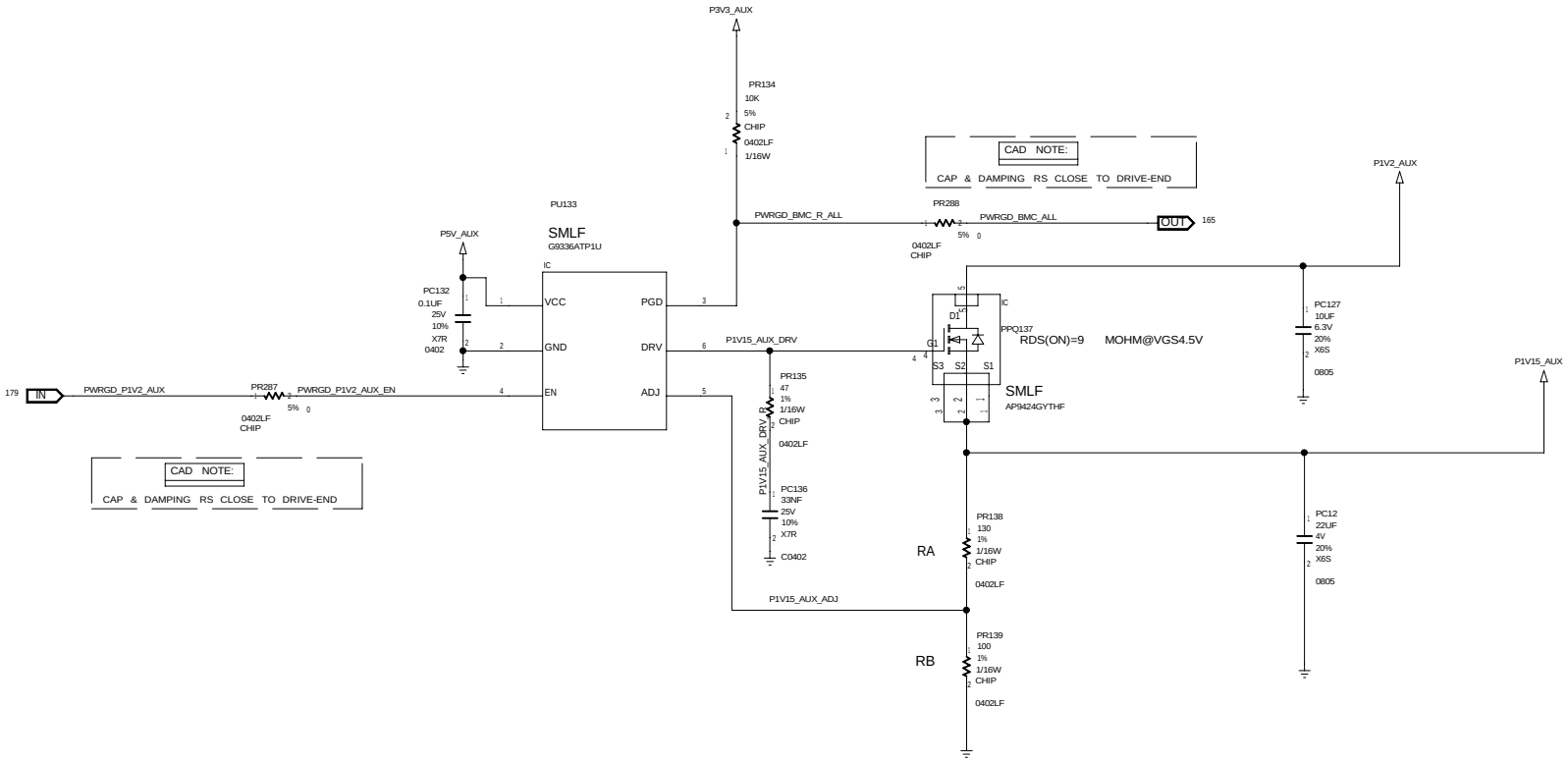


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Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 19:48:55 2017	SHEET 177 OF 226

P1V15_AUX

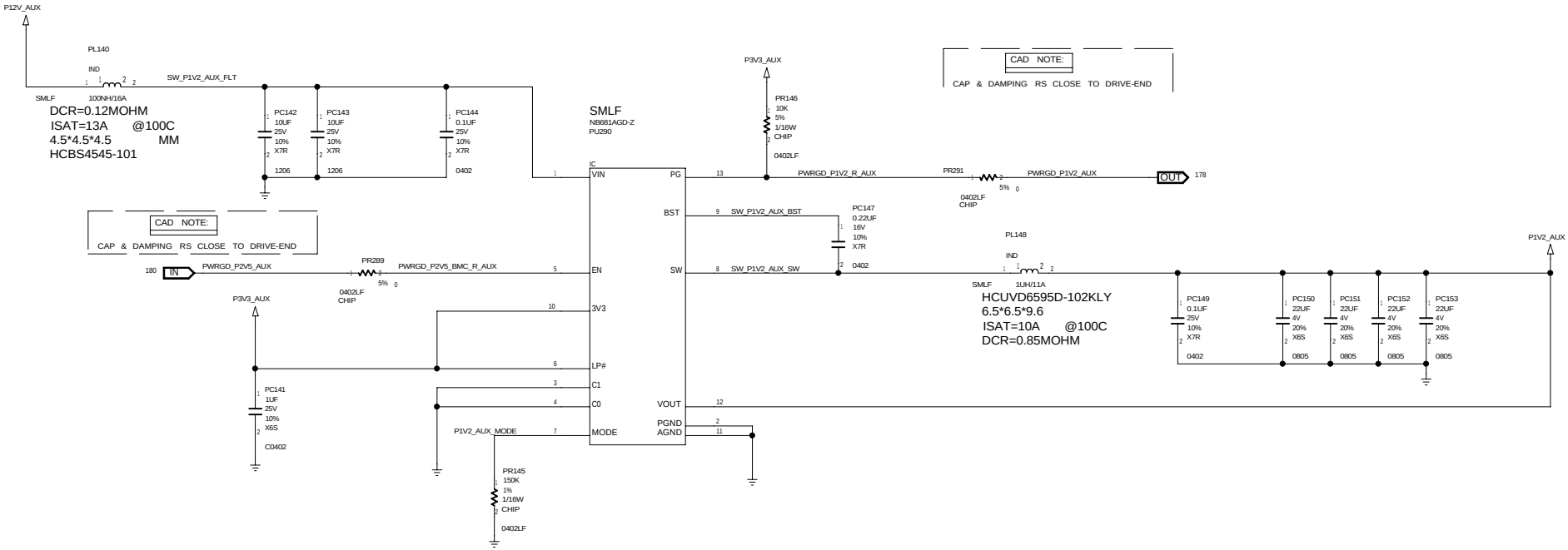
DESIGN SPECIFICATION
OUTPUT VOLTAGE=1.15V
OUTPUT RIPPLE<+/-11.5MV
TRANSIENT TOLERANCE=+/-51.75MV
TDC=0.75A
MAX CURRENT=0.75A



VOUT=0.5(1+RA/RB)=1.15V

DESIGN SPECIFICATION

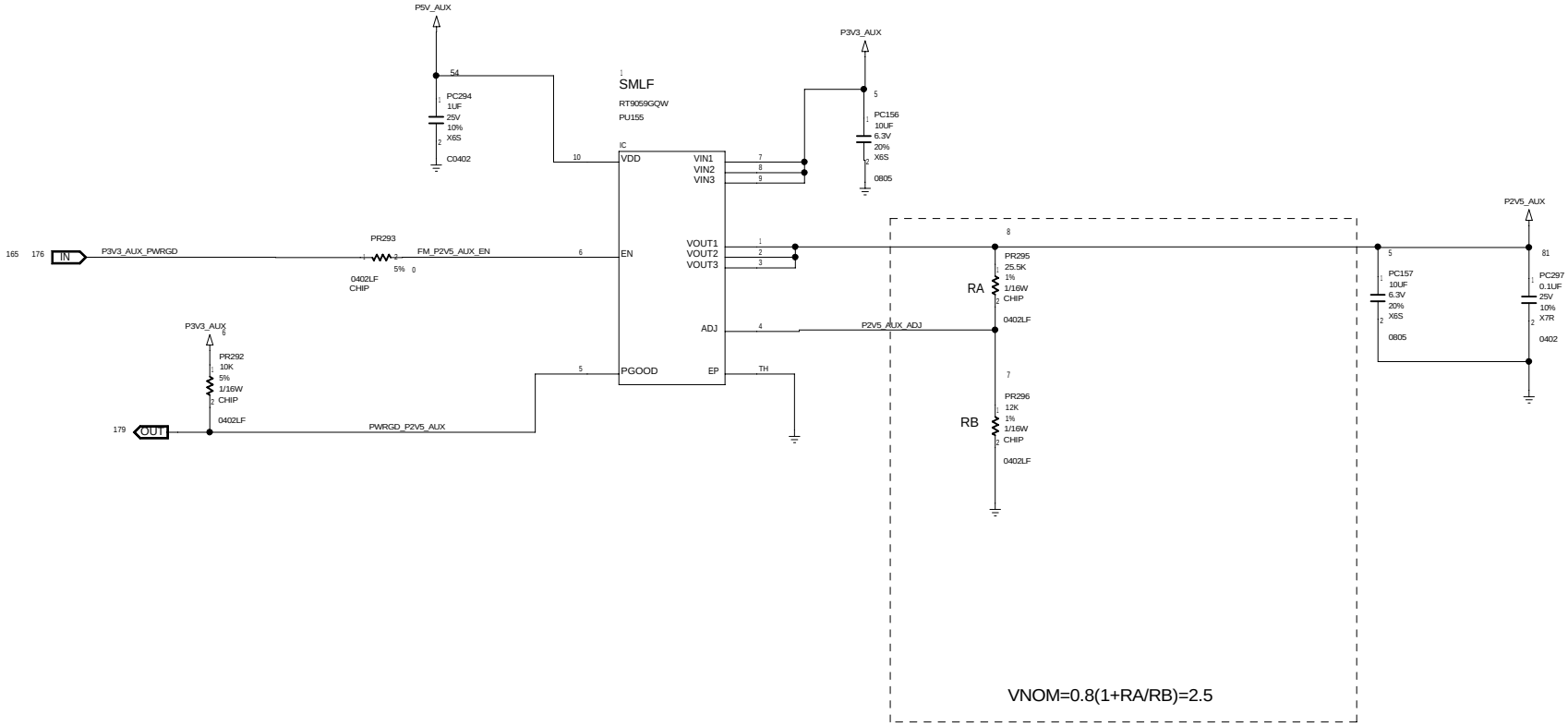
OUTPUT VOLTAGE=1.2V
OUTPUT RIPPLE<+/-12MV
TRANSIENT TOLERANCE=+/-54MV
TDC=1.2A
MAX CURRENT=2A
OVER CURRENT PROTECTION(IC RATING)=7A
CURRENT STEP=2A
SLEW RATE=2A/US
WORK FREQUENCY=750KHZ
EFFICIENCY>90%@TDC



P1V2_AUX

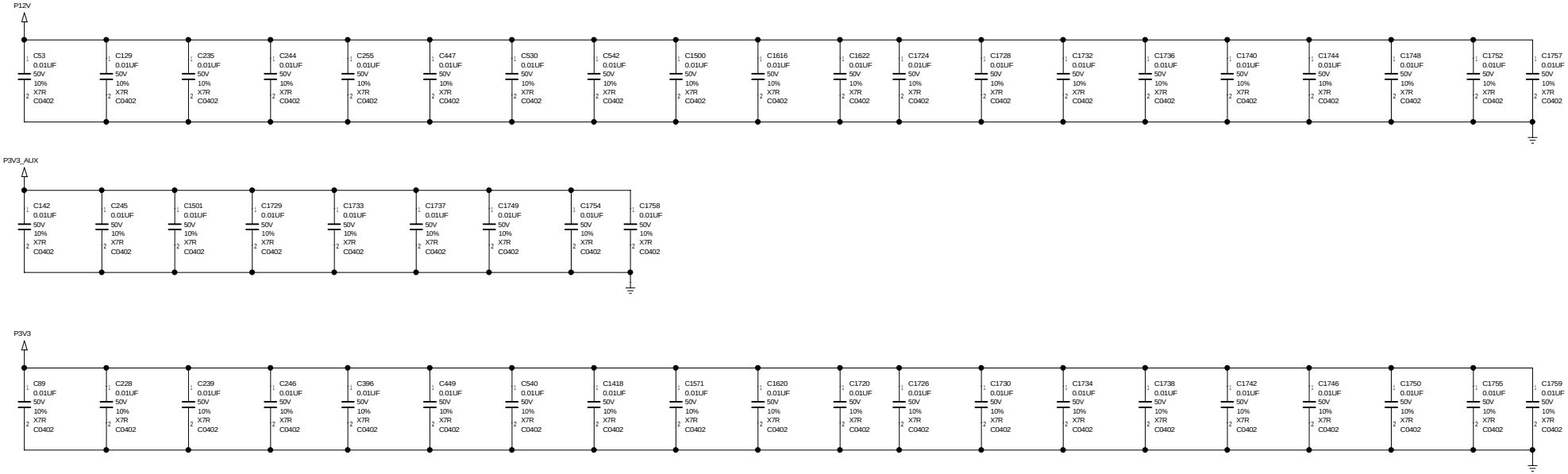
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:04 2017	SHEET 179 OF 226

OUTPUT VOLTAGE = 2.5V+/-5%
OUTPUT RIPPLE & NOISE < 50MV
TRANSIENT TOLERANCE = +/-137.5MV
TDC CURRENT = 0.3A
CURRENT STEP = 0.1A
SLEW RATE = 0.1A/US
MAX CURRENT = 0.5A
PD = (3.3V - 2.5V) * 0.5A =0.4W



P2V5_AUX

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:22:04 2017	SHEET 180 OF 226

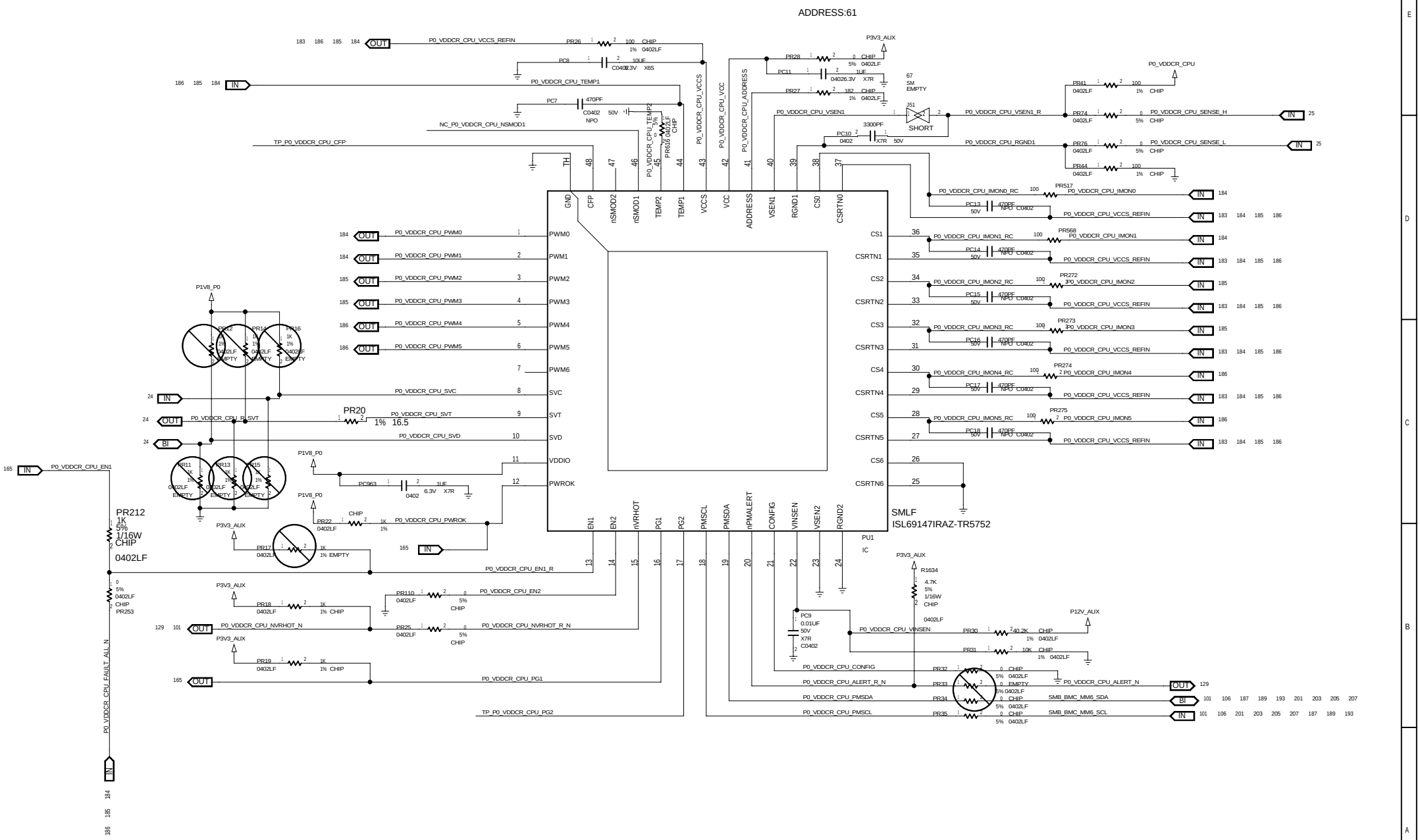


STITCHING CAP

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE C | DATE Fri Dec 15 20:22:04 2017	SHEET 181 OF 226

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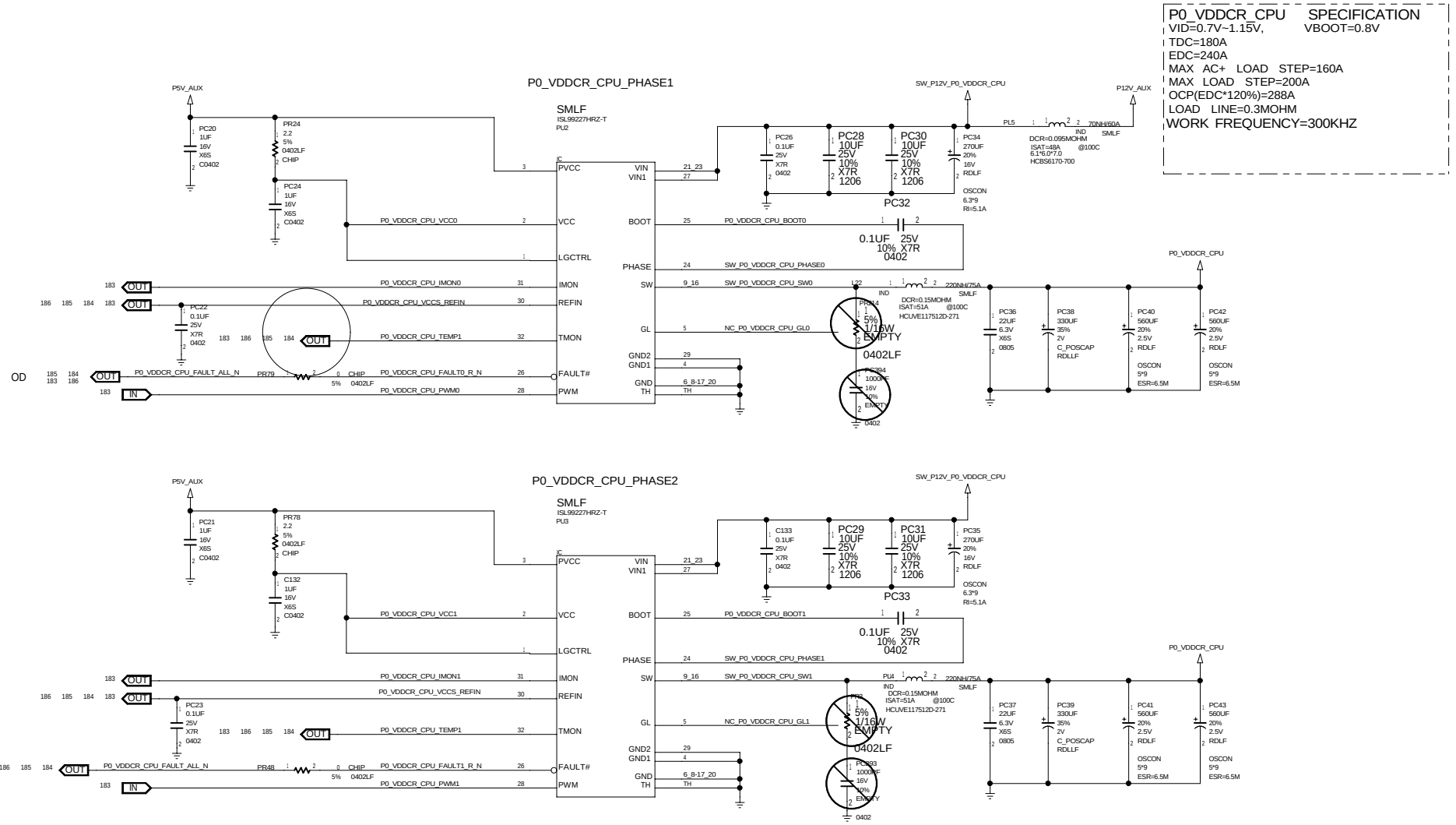
Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 19:37:01 2017	SHEET 182 OF 226

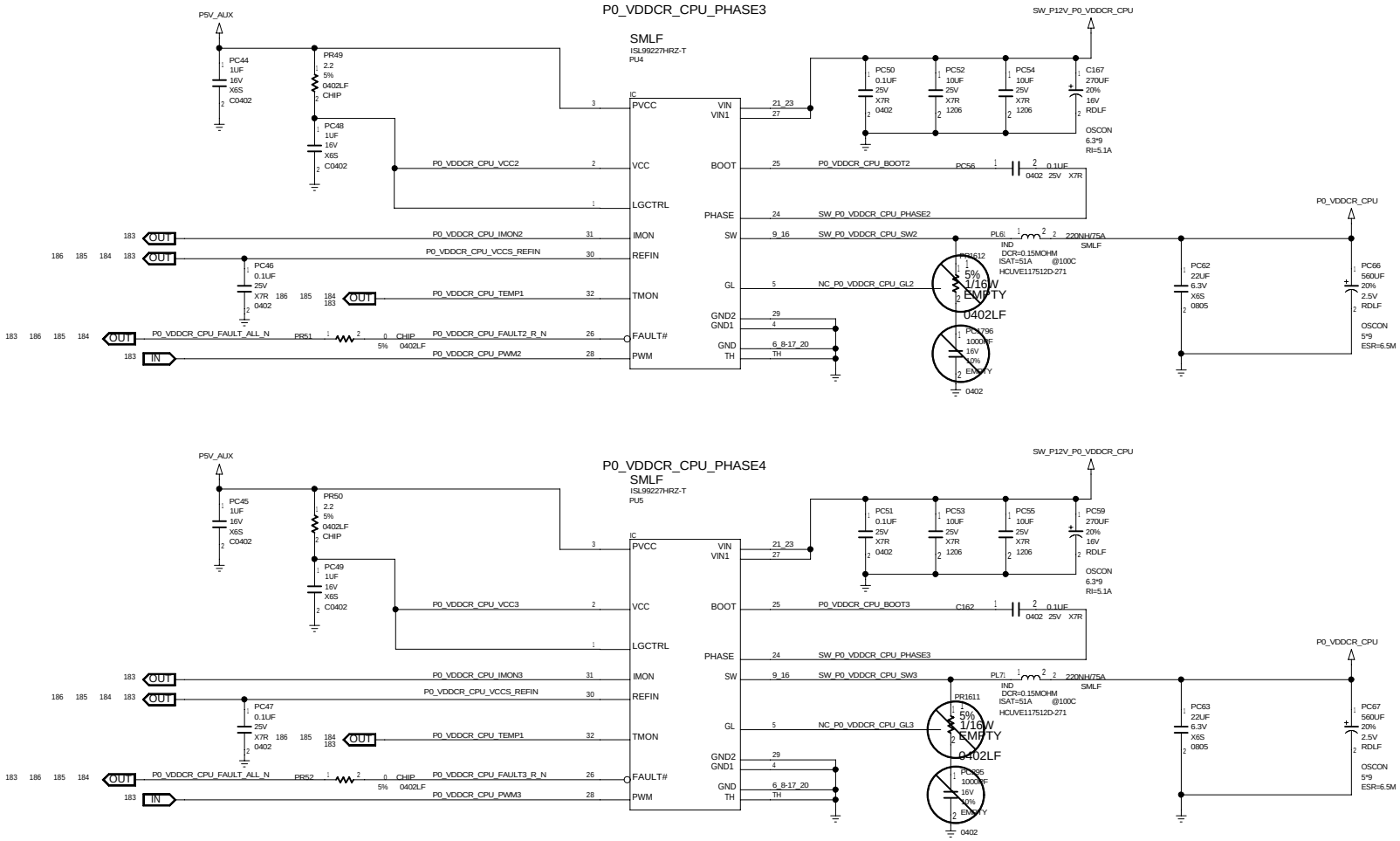


P0_VDDCR_CPU CONTROLLER

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

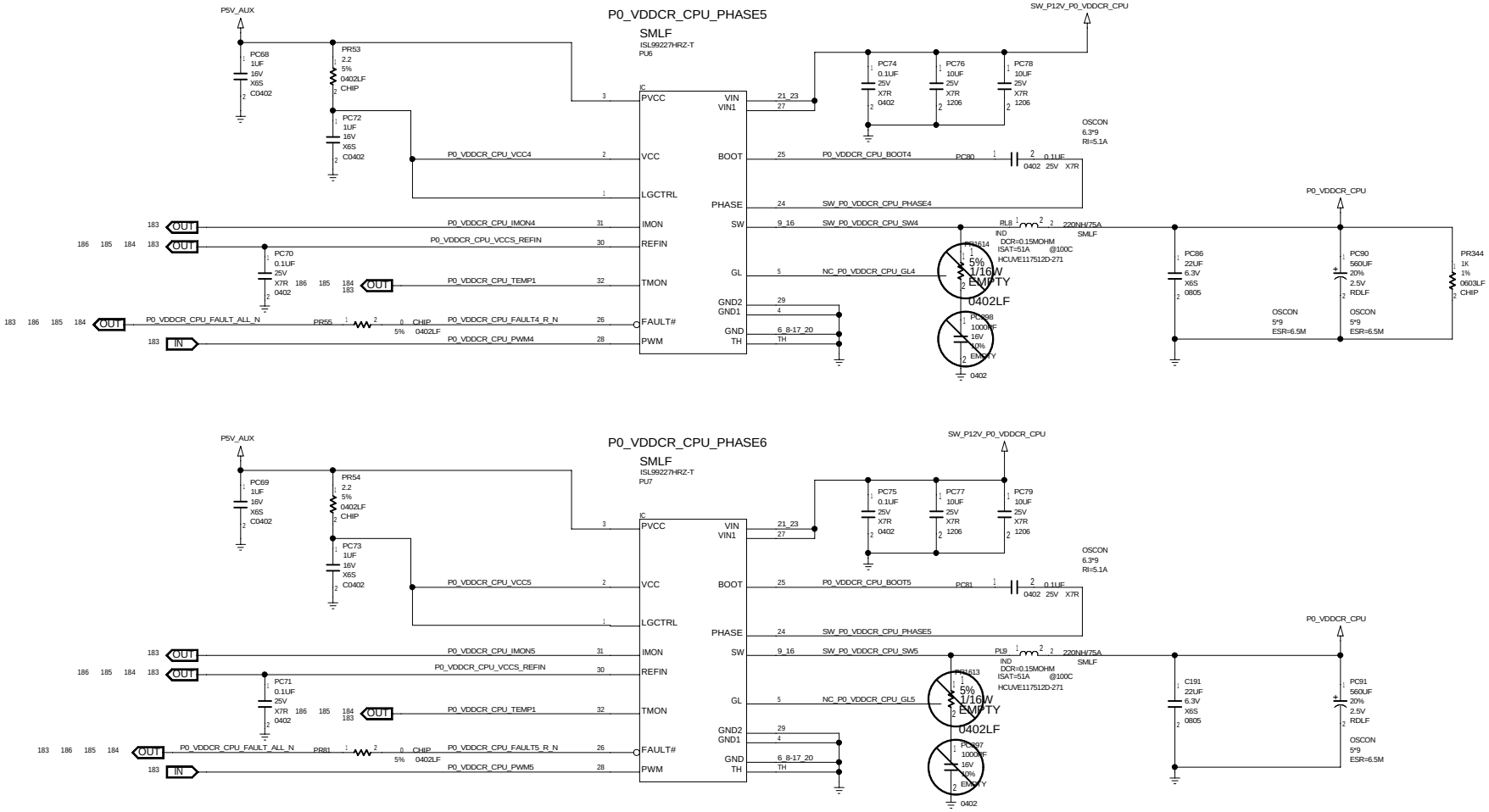
SIZE C | DATE Fri Dec 15 20:22:04 2017 | SHEET 183 OF 226


P0_VDDCR_CPU SPECIFICATION
VID=0.7V~1.15V, VBOOT=0.8V
TDC=180A
EDC=240A
MAX AC+ LOAD STEP=160A
MAX LOAD STEP=200A
OCP(EDC*120%)=288A
LOAD LINE=0.3MOHM
WORK FREQUENCY=300KHZ
P0_VDDCR_CPU_PHASE1
SMLF
ISL99227HRZ-T
PU2
P5V_AUX
P12V_AUX
SW_P12V_P0_VDDCR_CPU
PVCC
VIN
VIN1
VCC
BOOT
LGCTRL
PHASE
IMON
REFIN
TMON
SW
GL
FAULT#
PWM
GND2
GND1
GND
TH
P0_VDDCR_CPU_VCC0
P0_VDDCR_CPU_BOOT0
SW_P0_VDDCR_CPU_PHASE0
P0_VDDCR_CPU_IMON0
P0_VDDCR_CPU_VCCS_REFIN
P0_VDDCR_CPU_TEMP1
P0_VDDCR_CPU_FAULT_ALL_N
P0_VDDCR_CPU_FAULT0_R_N
P0_VDDCR_CPU_PWM0
SW_P0_VDDCR_CPU_SW0
NC_P0_VDDCR_CPU_GL0
PC32
0.1UF 25V 10% X7R 0402
220NH/75A SMLF
HCUVE117512D-271
0402LF EMPTY
P0_VDDCR_CPU_PHASE2
PU3
P0_VDDCR_CPU_VCC1
P0_VDDCR_CPU_BOOT1
SW_P0_VDDCR_CPU_PHASE1
P0_VDDCR_CPU_IMON1
P0_VDDCR_CPU_VCCS_REFIN
P0_VDDCR_CPU_TEMP1
P0_VDDCR_CPU_FAULT_ALL_N
P0_VDDCR_CPU_FAULT1_R_N
P0_VDDCR_CPU_PWM1
SW_P0_VDDCR_CPU_SW1
NC_P0_VDDCR_CPU_GL1
PC33



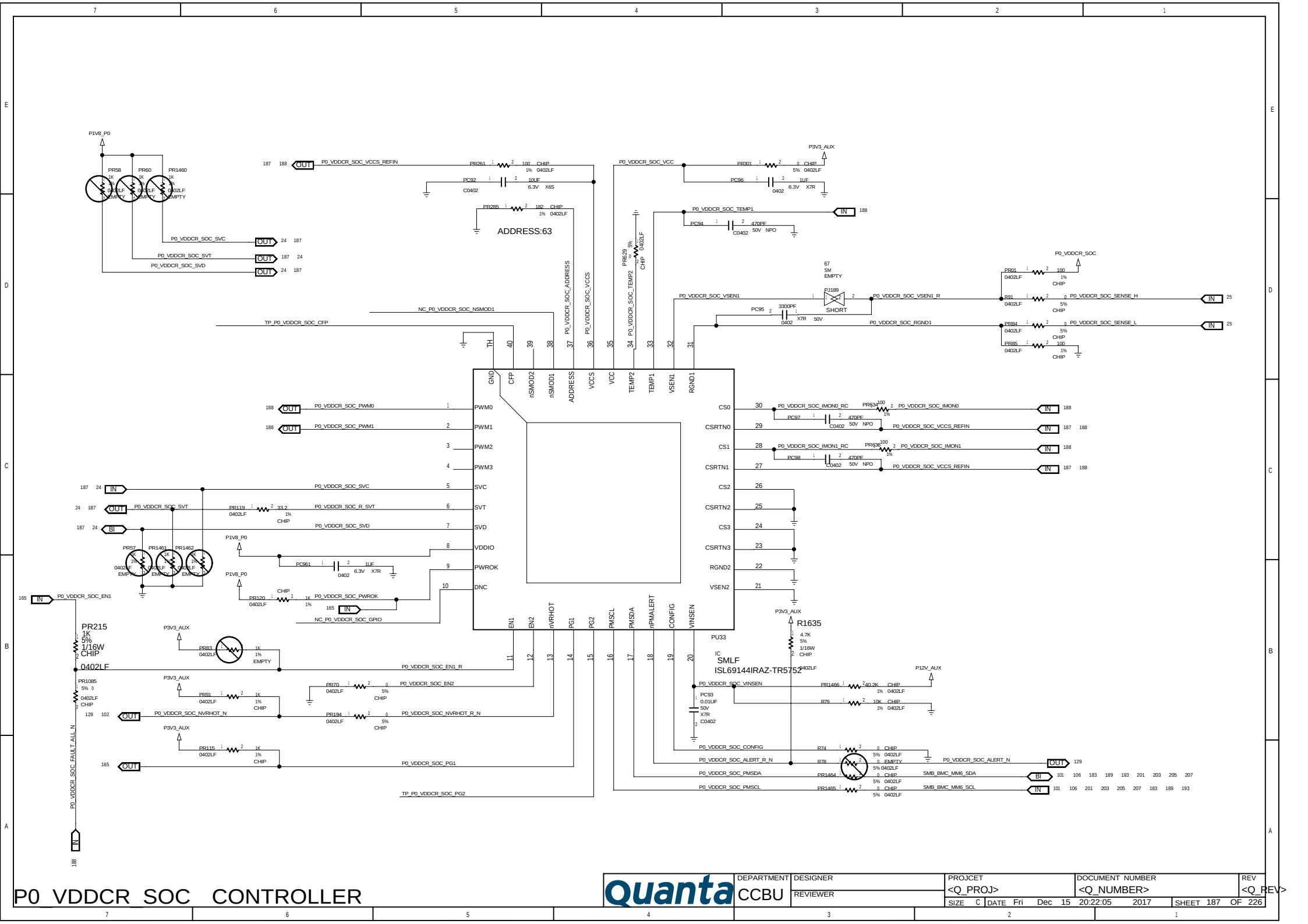
P0_VDDCR_CPU POWER STAGE_2

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE: C	DATE: Fri Dec 15 20:21:21 2017
				SHEET 185 OF 226



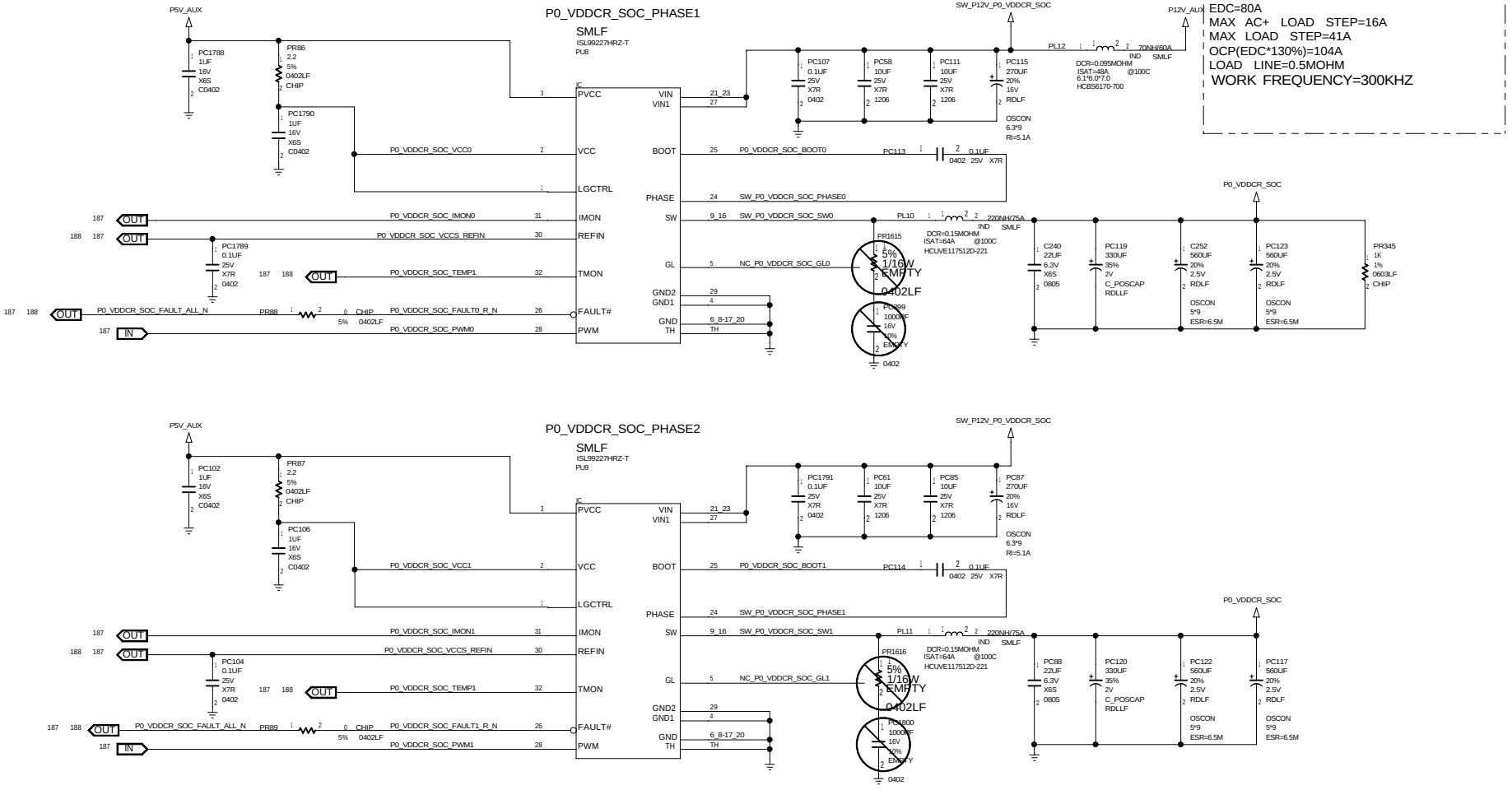
P0_VDDCR_CPU POWER STAGE_3

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:21:21 2017	SHEET 186 OF 226



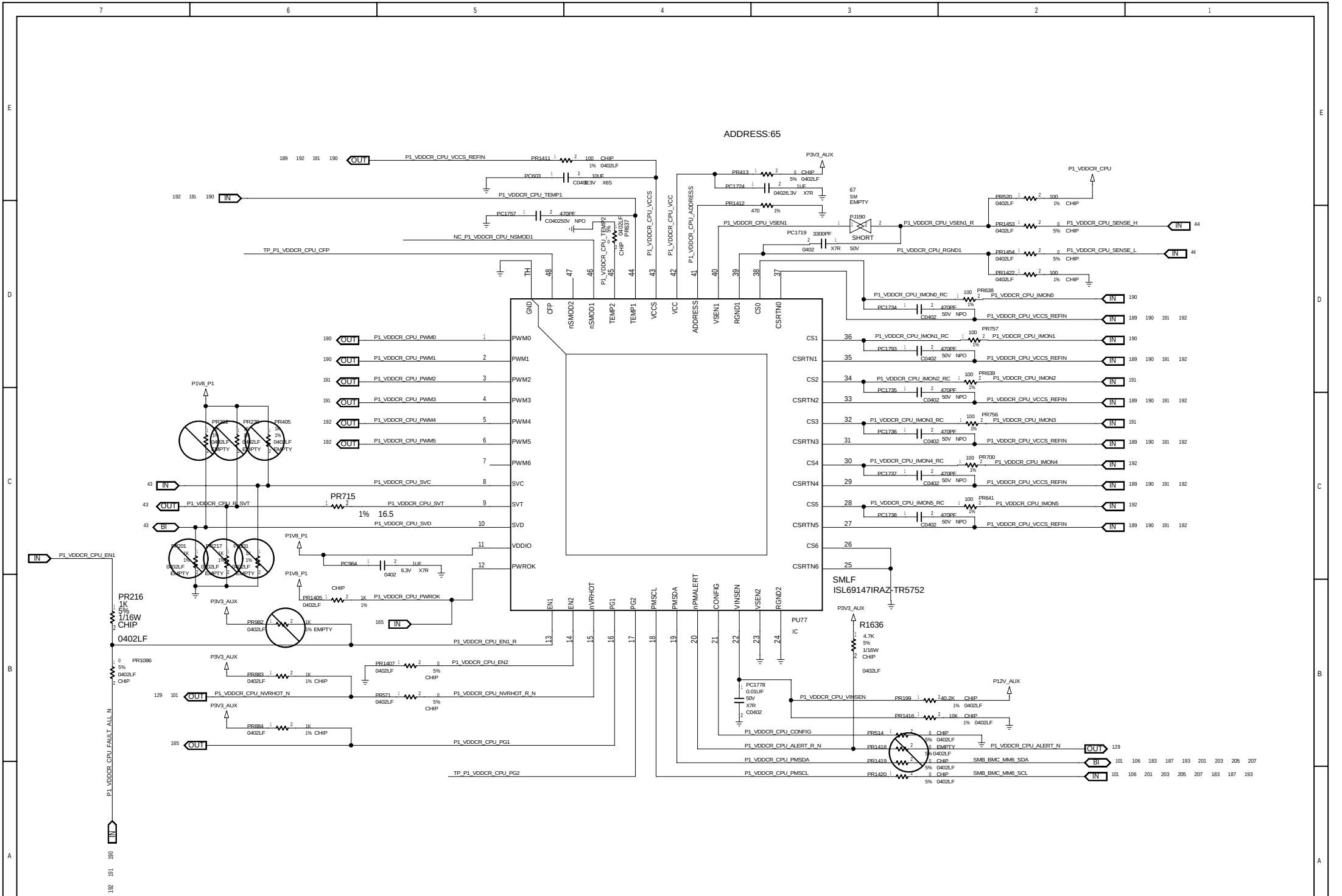
P0_VDDCR_SOC CONTROLLER

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:05 2017
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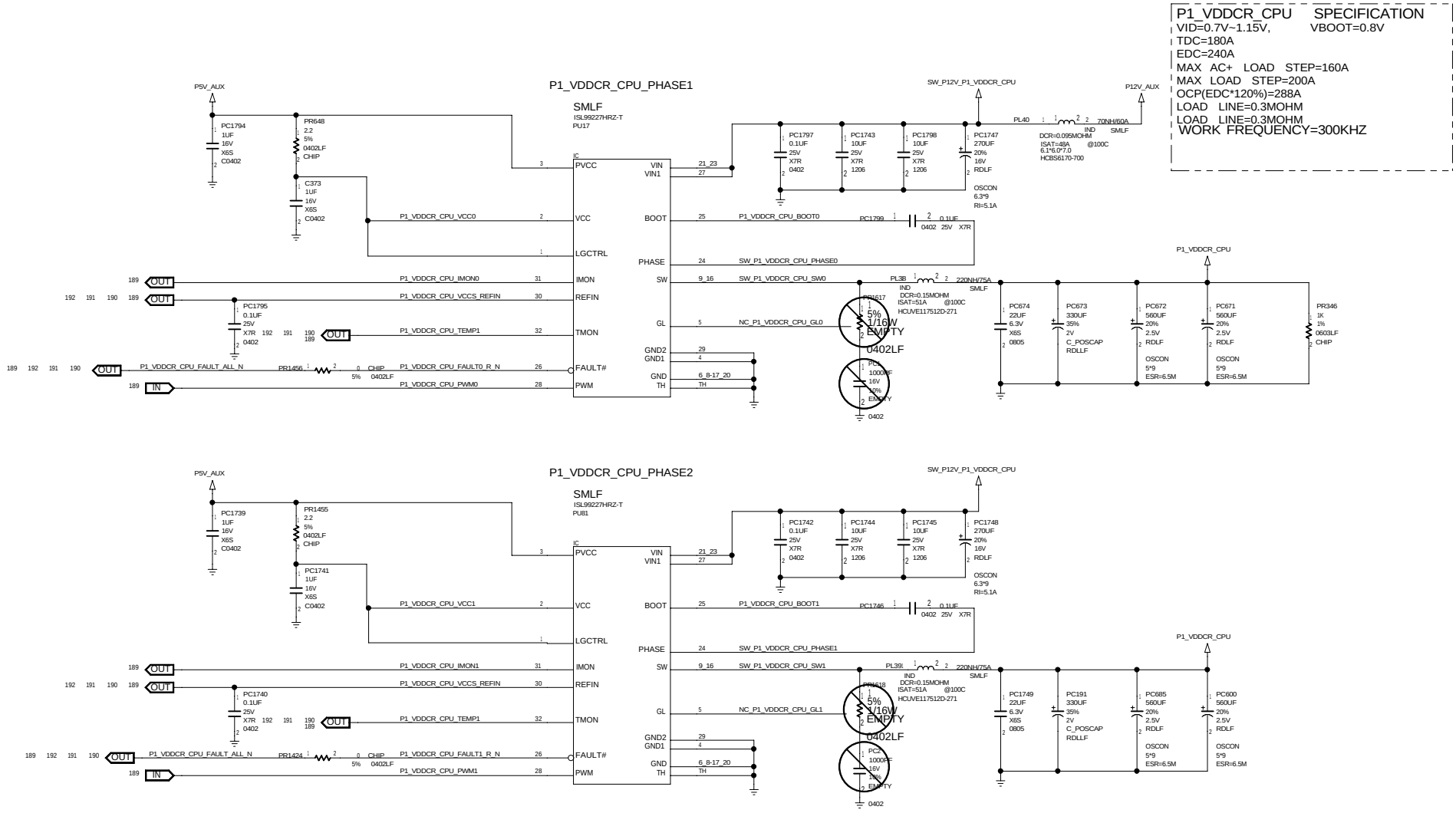
P0_VDDCR_SOC_POWER_STAGE_1

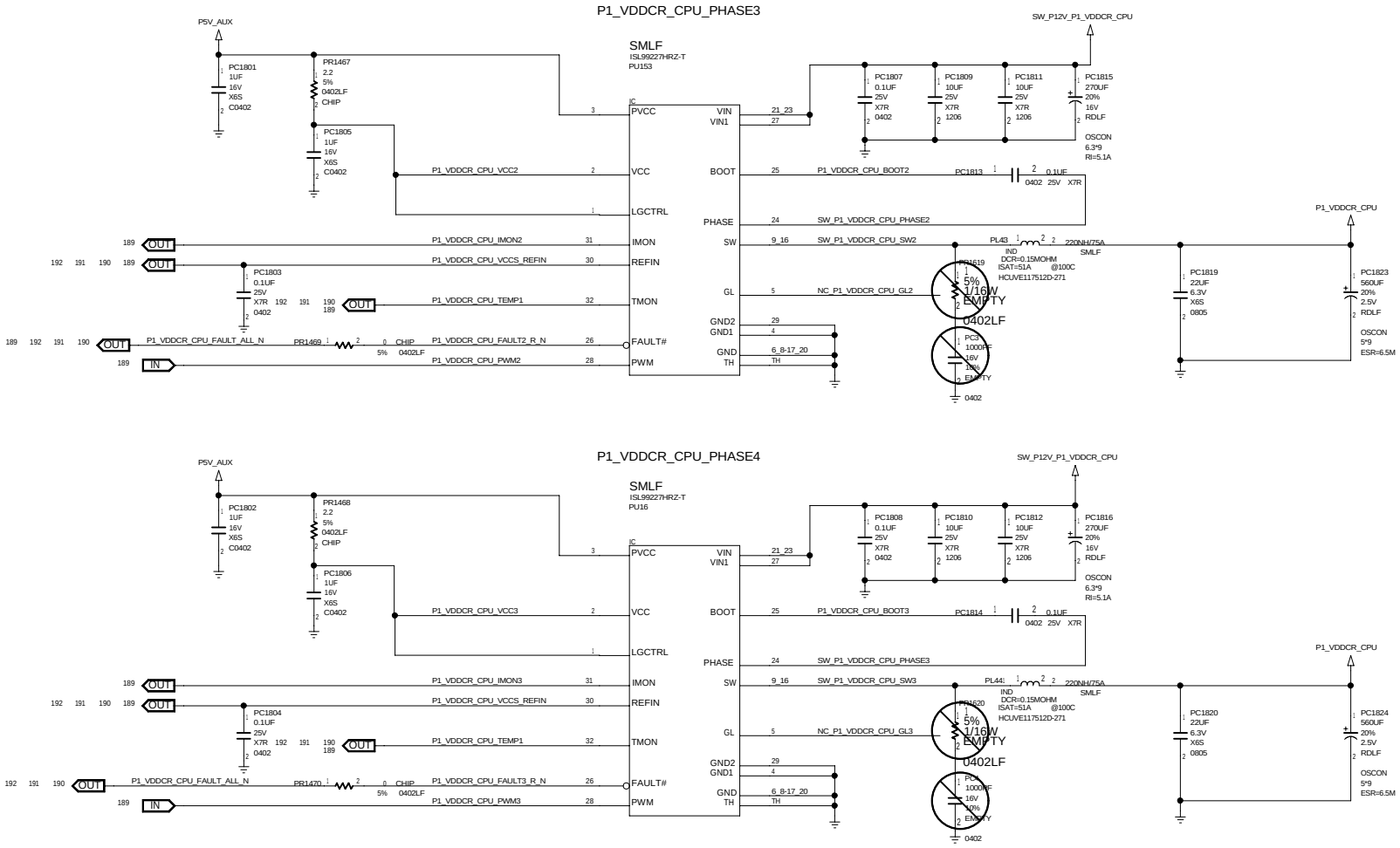
Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:22 2017	SHEET 188 OF 226



P1_VDDCR_CPU_CONTROLLER

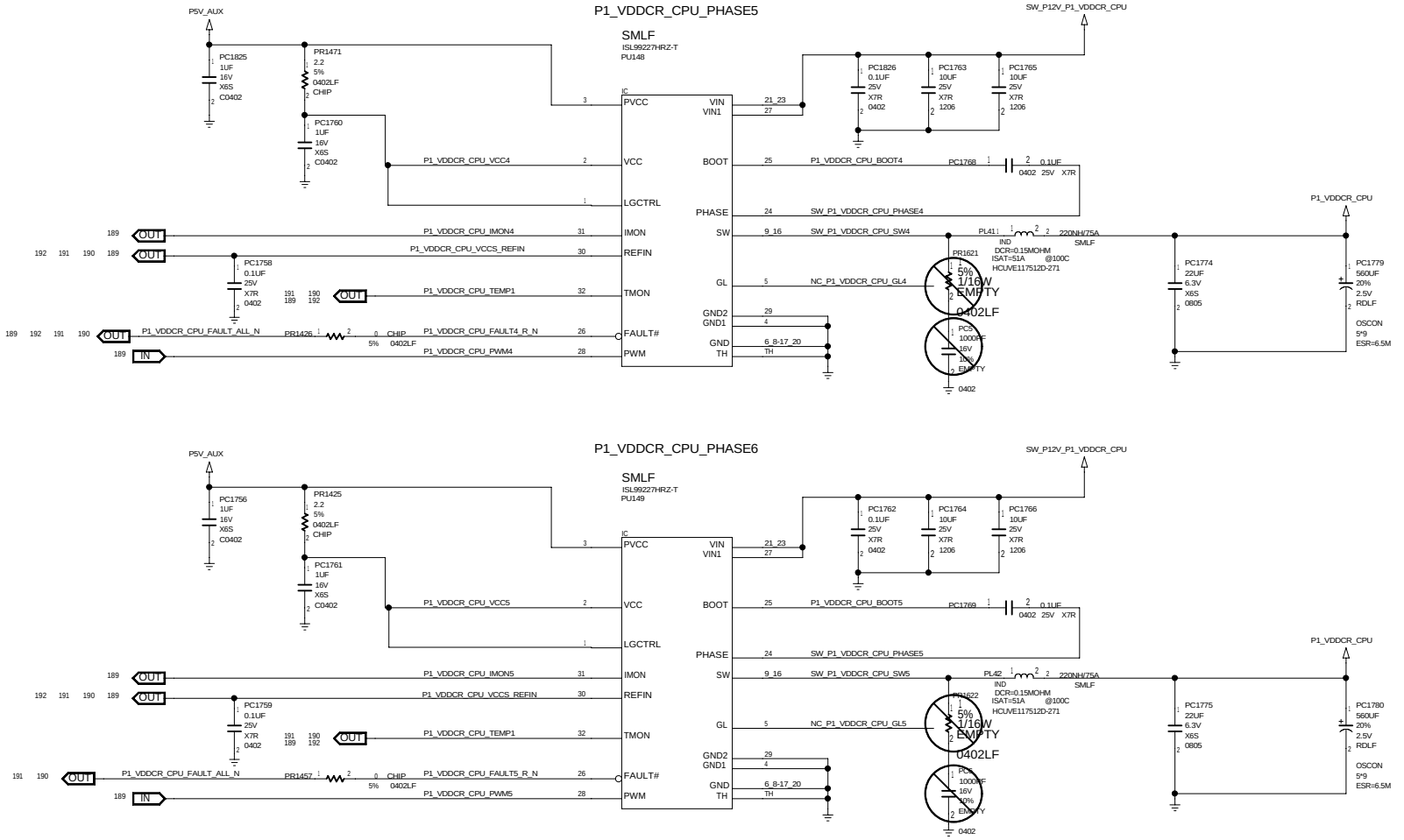
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C DATE Fri Dec 15 20:22:05 2017	SHEET 189 OF 226	


P1_VDDCR_CPU SPECIFICATION
VID=0.7V~1.15V, VBOOT=0.8V
TDC=180A
EDC=240A
MAX AC+ LOAD STEP=160A
MAX LOAD STEP=200A
OCP(EDC*120%)=288A
LOAD LINE=0.3MOHM
LOAD LINE=0.3MOHM
WORK FREQUENCY=300KHZ
P1_VDDCR_CPU_PHASE1
P1_VDDCR_CPU_PHASE2
SMLF
ISL99227HRZ-T
P5V_AUX
P12V_AUX
SW_P12V_P1_VDDCR_CPU
PVCC
VCC
LGCTRL
IMON
REFIN
TMON
FAULT#
PWM
VIN
VIN1
BOOT
PHASE
SW
GL
GND2
GND1
GND
TH
P1_VDDCR_CPU_VCC0
P1_VDDCR_CPU_VCC1
P1_VDDCR_CPU_IMON0
P1_VDDCR_CPU_IMON1
P1_VDDCR_CPU_VCCS_REFIN
P1_VDDCR_CPU_TEMP1
P1_VDDCR_CPU_FAULT_ALL_N
P1_VDDCR_CPU_FAULT0_R_N
P1_VDDCR_CPU_FAULT1_R_N
P1_VDDCR_CPU_PWM0
P1_VDDCR_CPU_PWM1
P1_VDDCR_CPU_BOOT0
P1_VDDCR_CPU_BOOT1
SW_P1_VDDCR_CPU_PHASE0
SW_P1_VDDCR_CPU_PHASE1
SW_P1_VDDCR_CPU_SW0
SW_P1_VDDCR_CPU_SW1
NC_P1_VDDCR_CPU_GL0
NC_P1_VDDCR_CPU_GL1
P1_VDDCR_CPU
OUT
IN
EMPTY
0402LF
CHIP
OSCON
C_FOSCAP
RDLLF



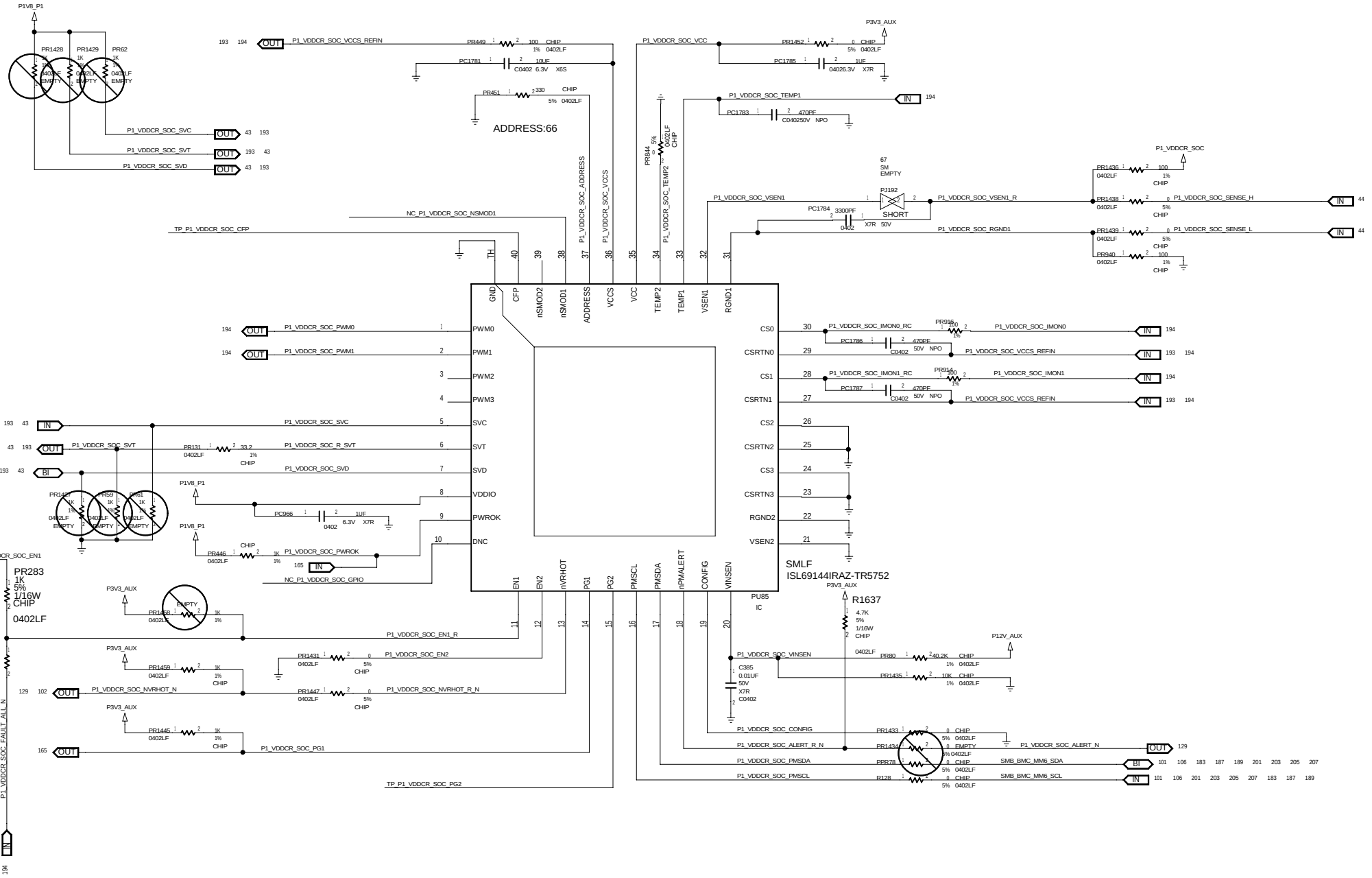
P1_VDDCR_CPU POWER STAGE_2

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:22 2017	SHEET 191 OF 226



P1_VDDCR_CPU POWER STAGE_3

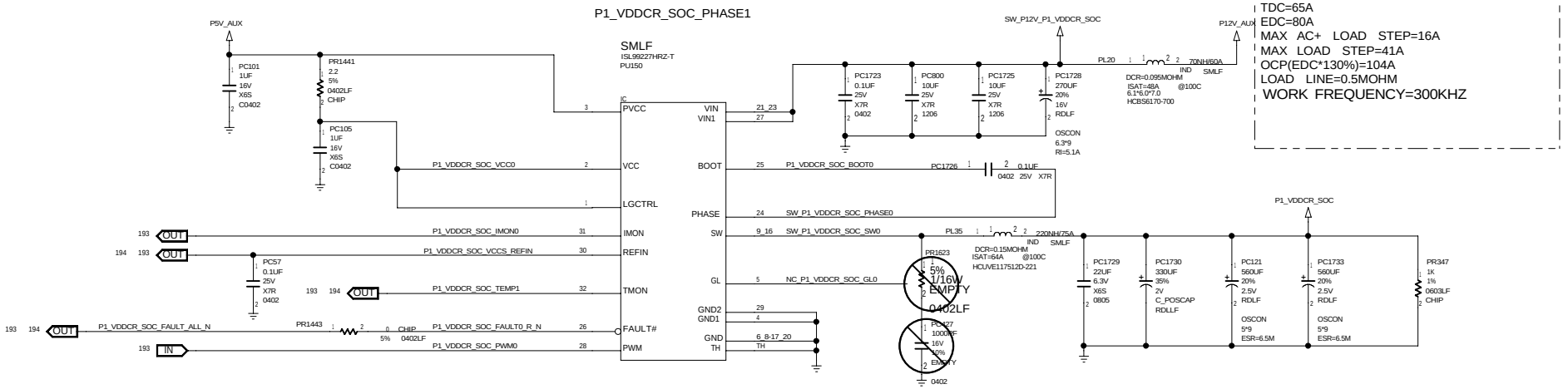
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C DATE Fri Dec 15 20:21:22 2017		SHEET 192 OF 226

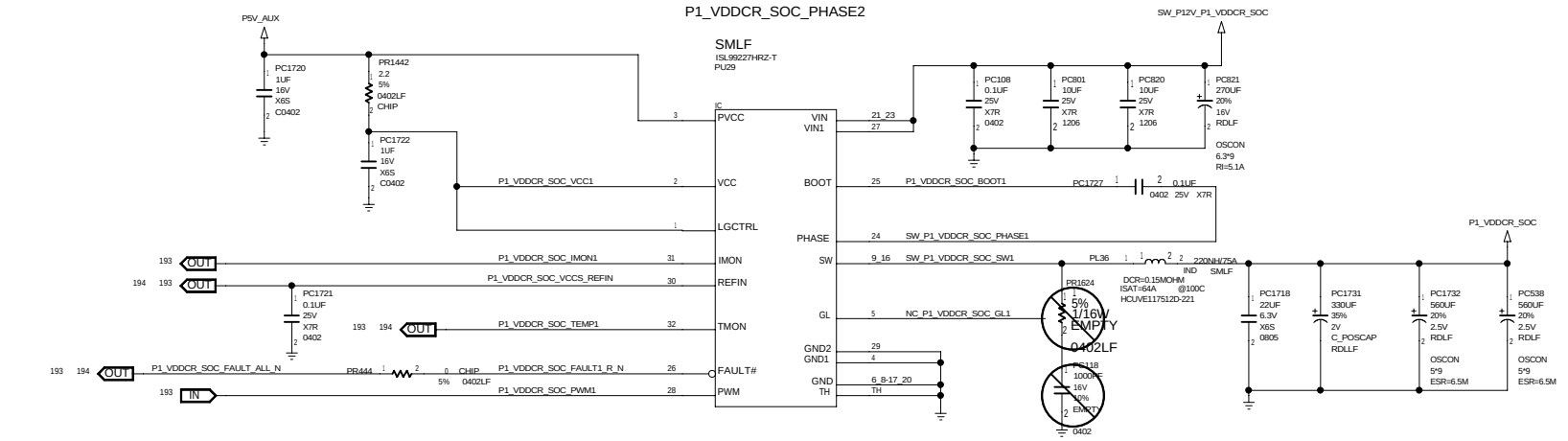


P1_VDDCR_SOC CONTROLLER

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE: C	DATE: Fri Dec 15 20:22:05 2017
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P1_VDDCR_SOC SPECIFICATION
VID=0.8V~0.9V, VBOOT=0.8V
TDC=65A
EDC=80A
MAX AC+ LOAD STEP=16A
MAX LOAD STEP=41A
OCP(EDC*130%)=104A
LOAD LINE=0.5MOHM
WORK FREQUENCY=300KHZ





P1_VDDCR_SOC_POWER_STAGE_1

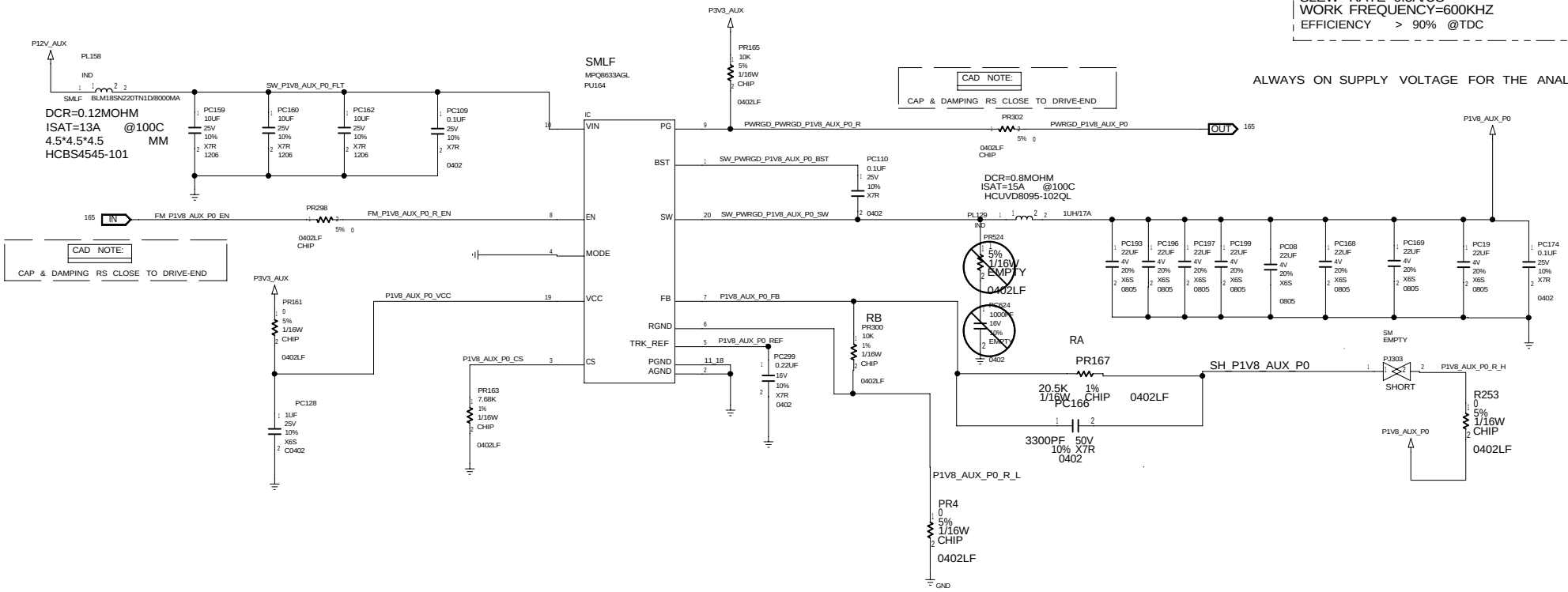
Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:22 2017	SHEET 194 OF 226

P1V8_AUX_P0

DESIGN SPECIFICATION

OUTPUT VOLTAGE=1.8V +/-5%
OUTPUT RIPPLE<+/-30MV
DC TOLERANCE = 180MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=5.6A
MAX CURRENT=7A
OCP(IMAX*130%)=9.1A
CURRENT STEP=0.5A
SLEW RATE=0.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC

ALWAYS ON SUPPLY VOLTAGE FOR THE ANALOG CIRCUITS



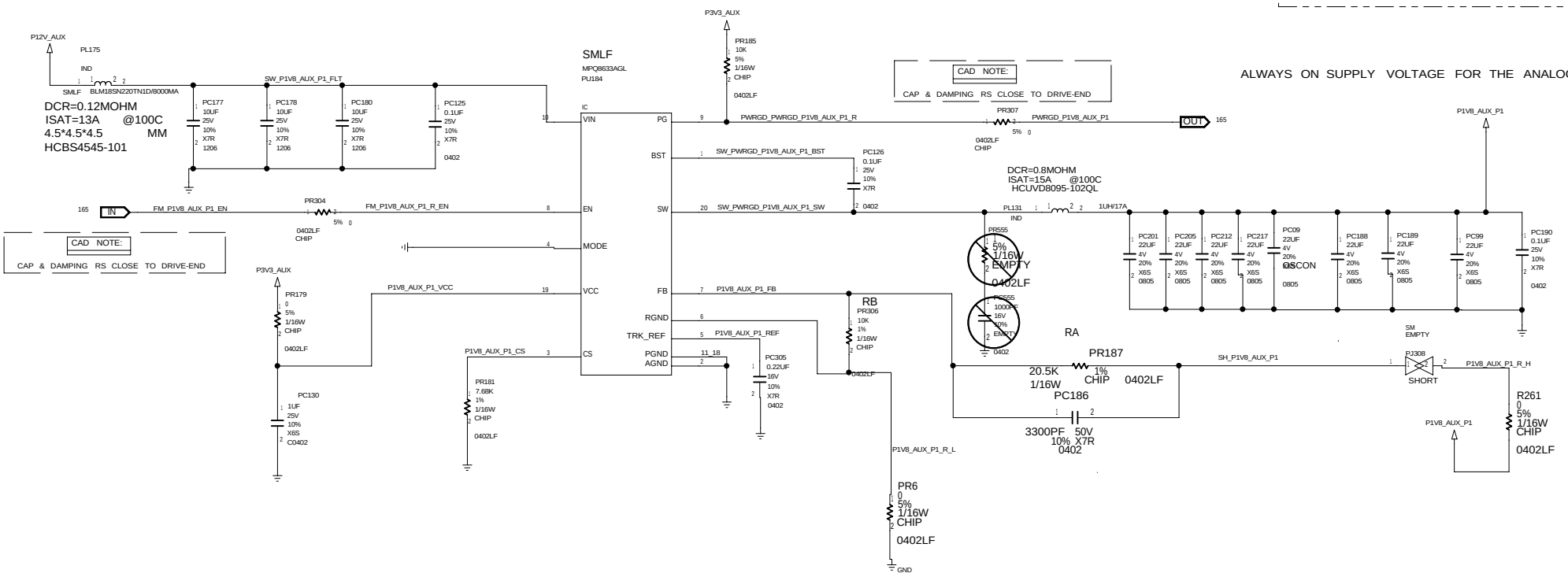
VOUT=0.6(1+RA/RB)=1.8V

P1V8_AUX_P1

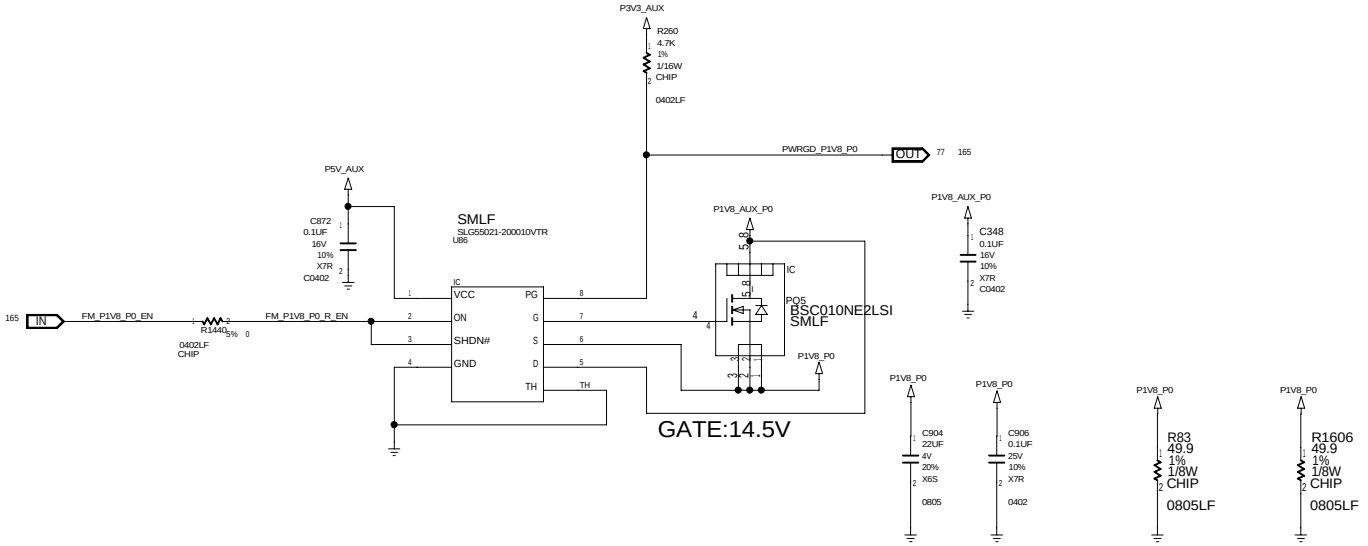
DESIGN SPECIFICATION

OUTPUT VOLTAGE=1.8V +/-5%
OUTPUT RIPPLE<+/-30MV
DC TOLERANCE = 180MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=5.6A
MAX CURRENT=7A
OCP(IMAX*130%)=9.1A
CURRENT STEP=0.5A
SLEW RATE=0.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC

ALWAYS ON SUPPLY VOLTAGE FOR THE ANALOG CIRCUITS

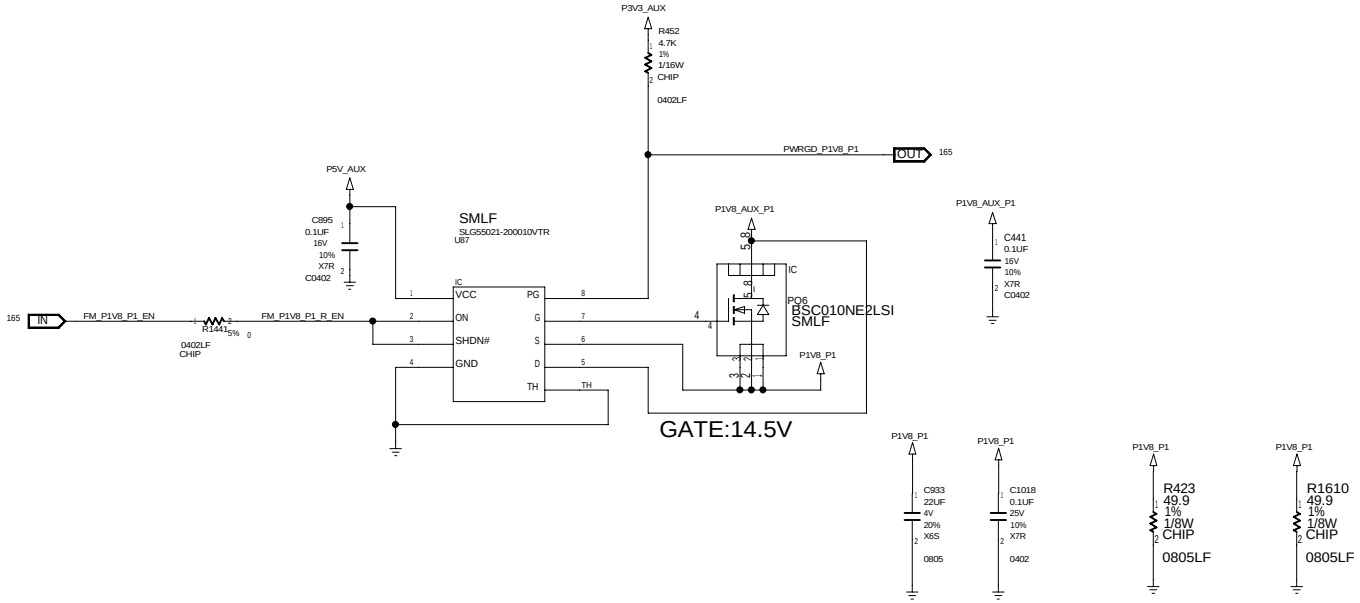


VOUT=0.6(1+RA/RB)=1.8V



P1V8_P0

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE: C DATE: Fri Dec 15 20:21:25 2017	SHEET 197 OF 226



P1V8_P1

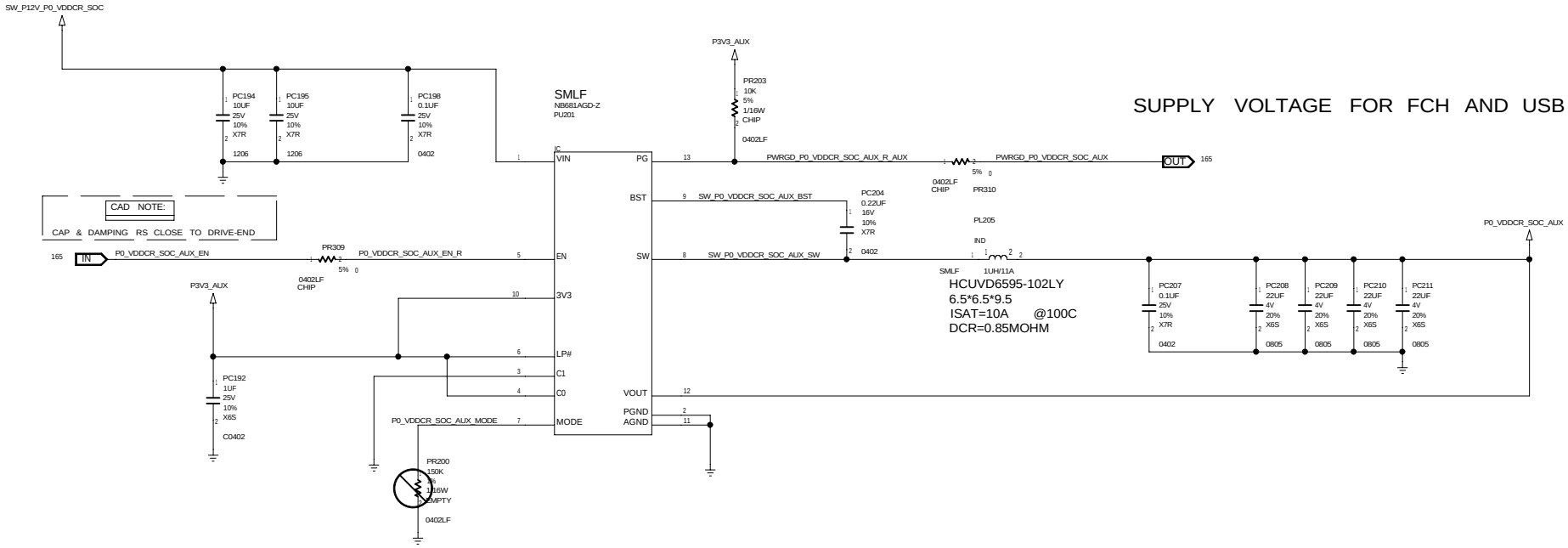
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		REVIEWER	SIZE: C	DATE: Fri Dec 15 20:21:25 2017
				SHEET 198 OF 226

REV: <Q_REV>

P0_VDDCR_SOC_AUX

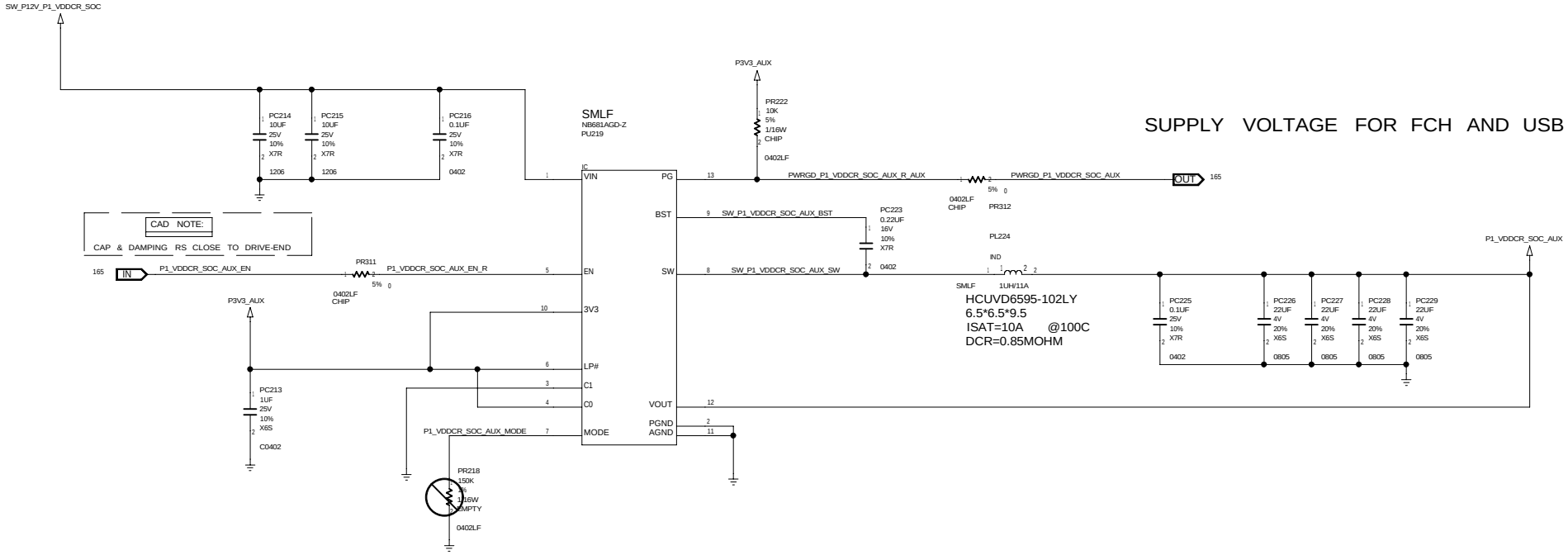
DESIGN SPECIFICATION
OUTPUT VOLTAGE=0.9V+/-5%
OUTPUT RIPPLE<+/-30MV
TRANSIENT TOLERANCE=+/-90MV
TDC=0.7A
MAX CURRENT=1.5A
OVER CURRENT PROTECTION(IC RATING)=7A
CURRENT STEP=0.25A
SLEW RATE=0.25A/US
WORK FREQUENCY=750KHZ
EFFICIENCY>85%@TDC

SUPPLY VOLTAGE FOR FCH AND USB



DESIGN SPECIFICATION
OUTPUT VOLTAGE=0.9V+/-5%
OUTPUT RIPPLE<+/-30MV
TRANSIENT TOLERANCE=+/-90MV
TDC=0.7A
MAX CURRENT=1.5A
OVER CURRENT PROTECTION(IC RATING)=7A
CURRENT STEP=0.25A
SLEW RATE=0.25A/US
WORK FREQUENCY=750KHZ
EFFICIENCY>85%@TDC

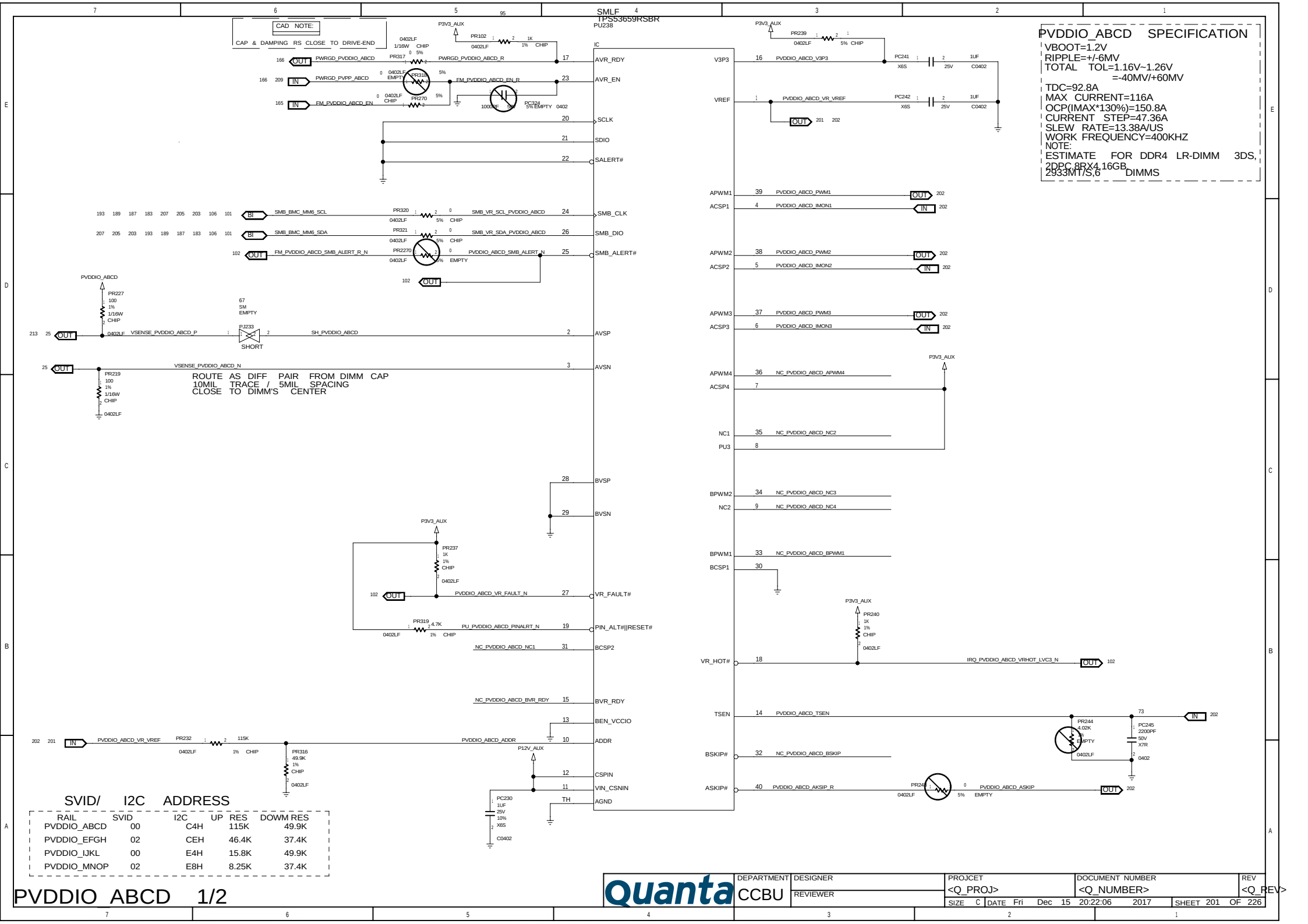
P1_VDDCR_SOC_AUX

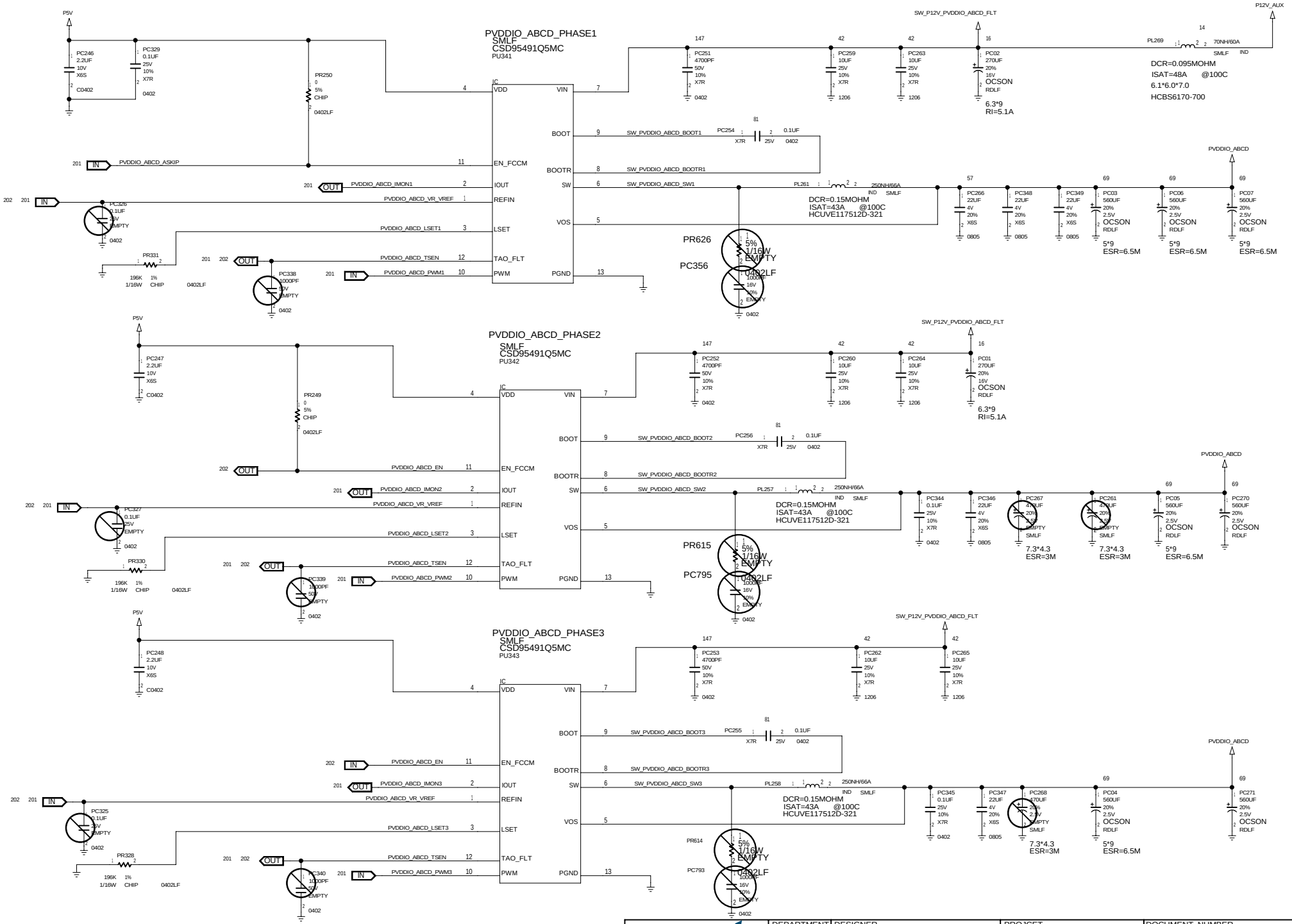


P1_VDDCR_SOC_AUX

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

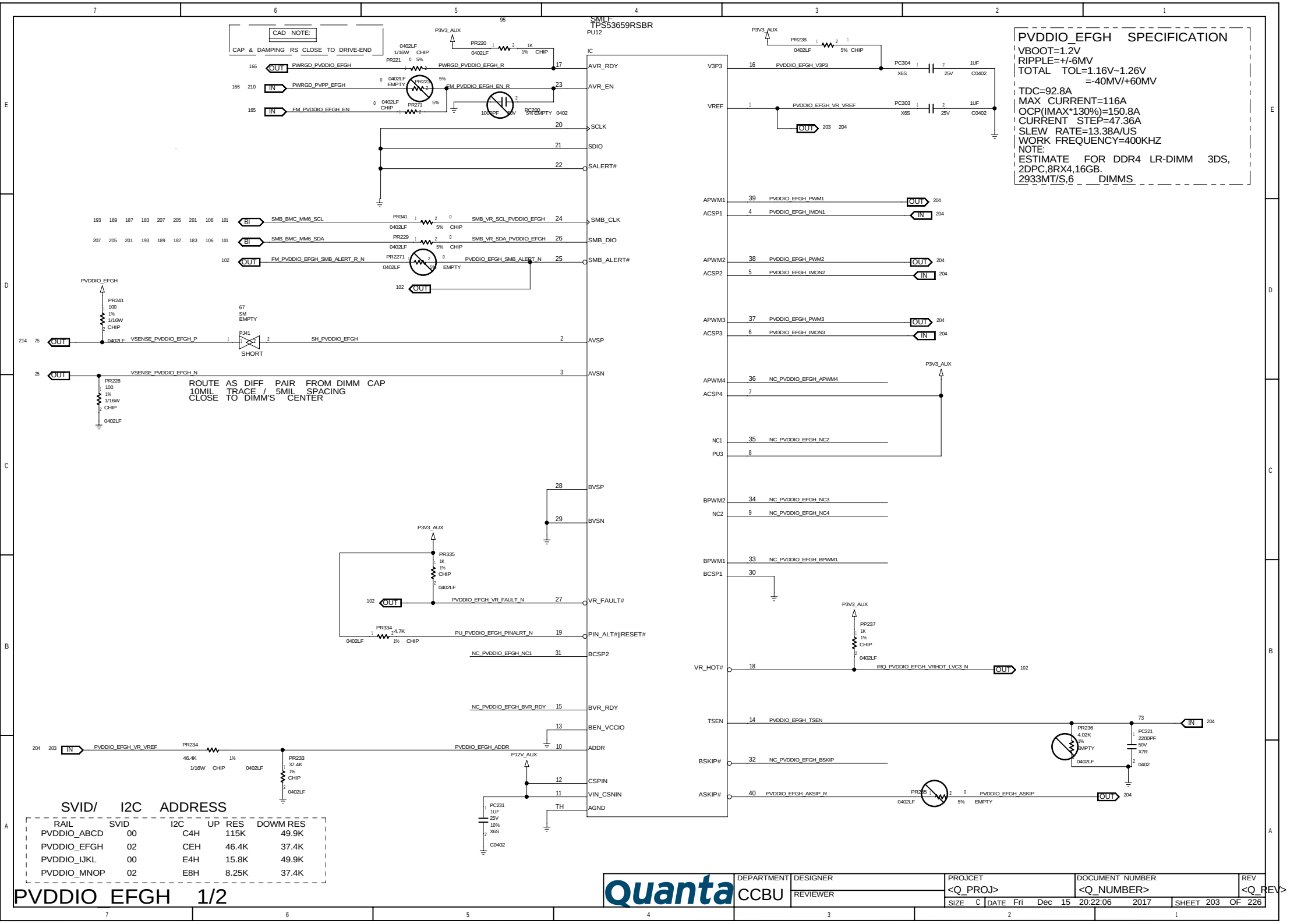
SIZE C | DATE Fri Dec 15 20:22:05 2017 | SHEET 200 OF 226

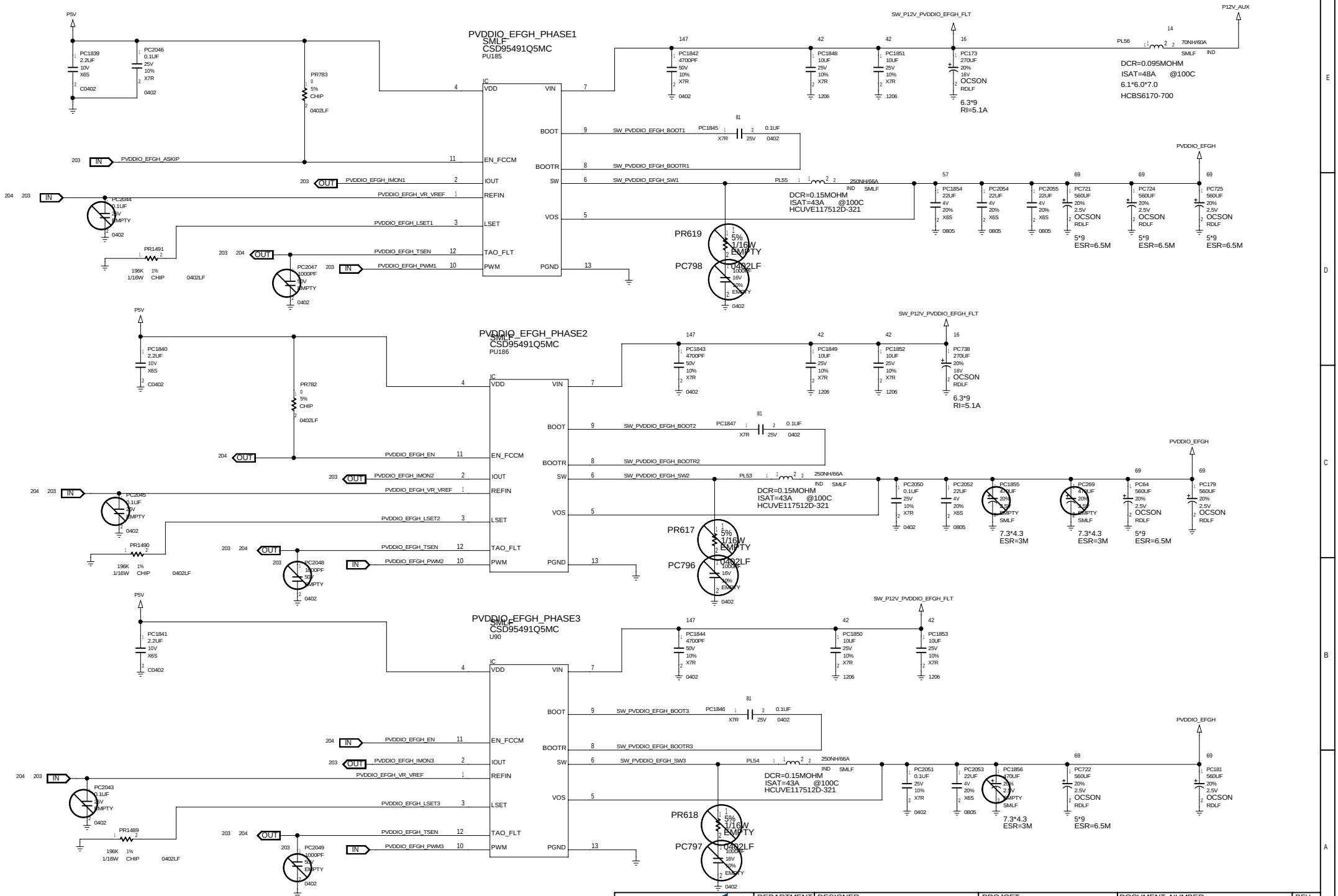

CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
SMLF
TPS53659RSBR
PU238
IC
AVR_RDY
AVR_EN
SCLK
SDIO
SALERT#
SMB_CLK
SMB_DIO
SMB_ALERT#
AVSP
AVSN
BVSP
BVSN
VR_FAULT#
PIN_ALT#||RESET#
BCSP2
BVR_RDY
BEN_VCCIO
ADDR
CSPIN
VIN_CSNIN
AGND
TH
APWM1
ACSP1
APWM2
ACSP2
APWM3
ACSP3
APWM4
ACSP4
NC1
PU3
BPWM2
NC2
BPWM1
BCSP1
VR_HOT#
TSEN
BSKIP#
ASKIP#
V3P3
VREF
P3V3_AUX
P12V_AUX
PVDDIO_ABCD
PVDDIO_ABCD SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB, 2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SHORT
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CEH 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_ABCD 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
SIZE C
DATE Fri Dec 15 20:22:06 2017
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PVDDIO_ABCD 2/2

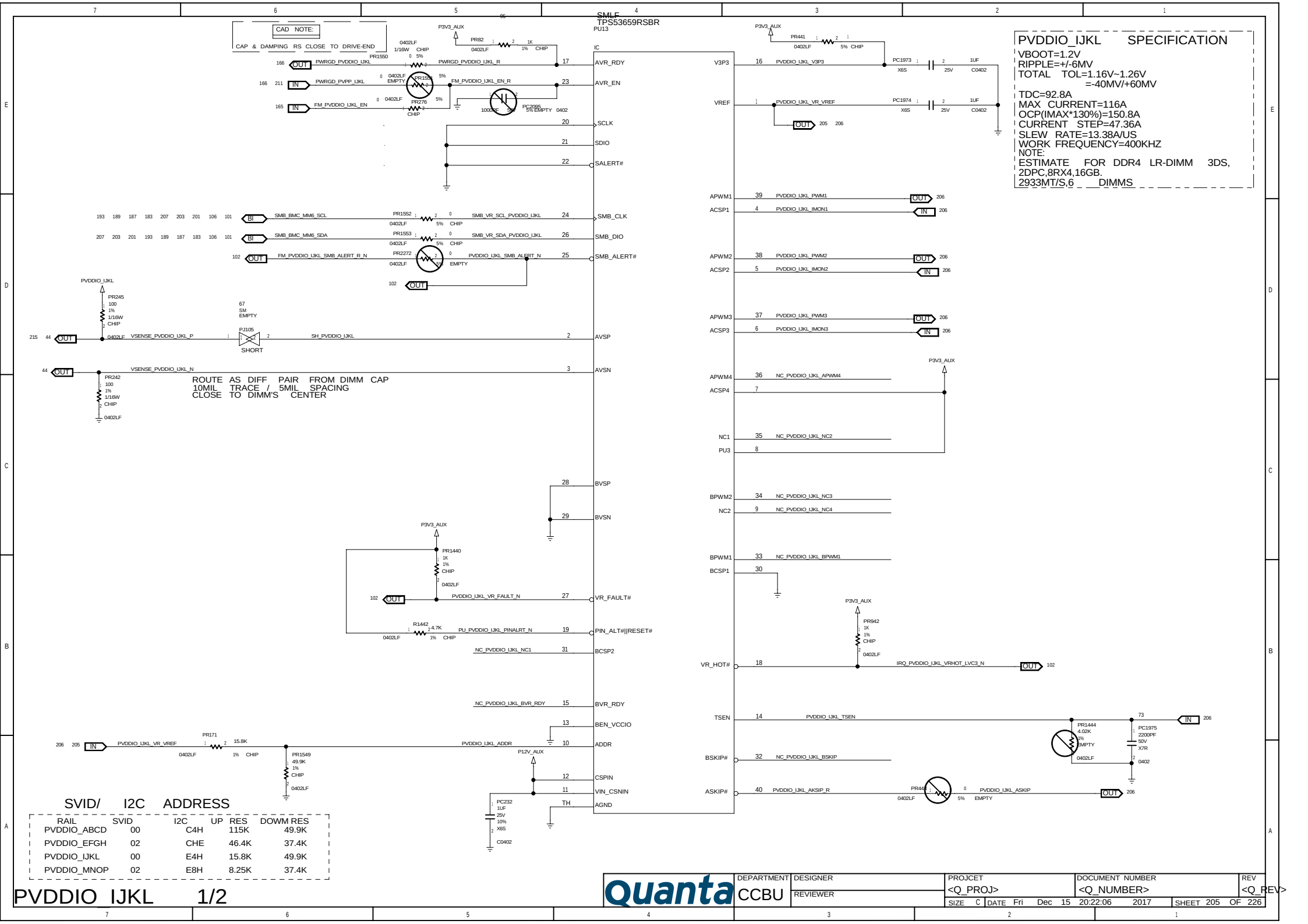
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DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:23 2017
SHEET 202 OF 226			

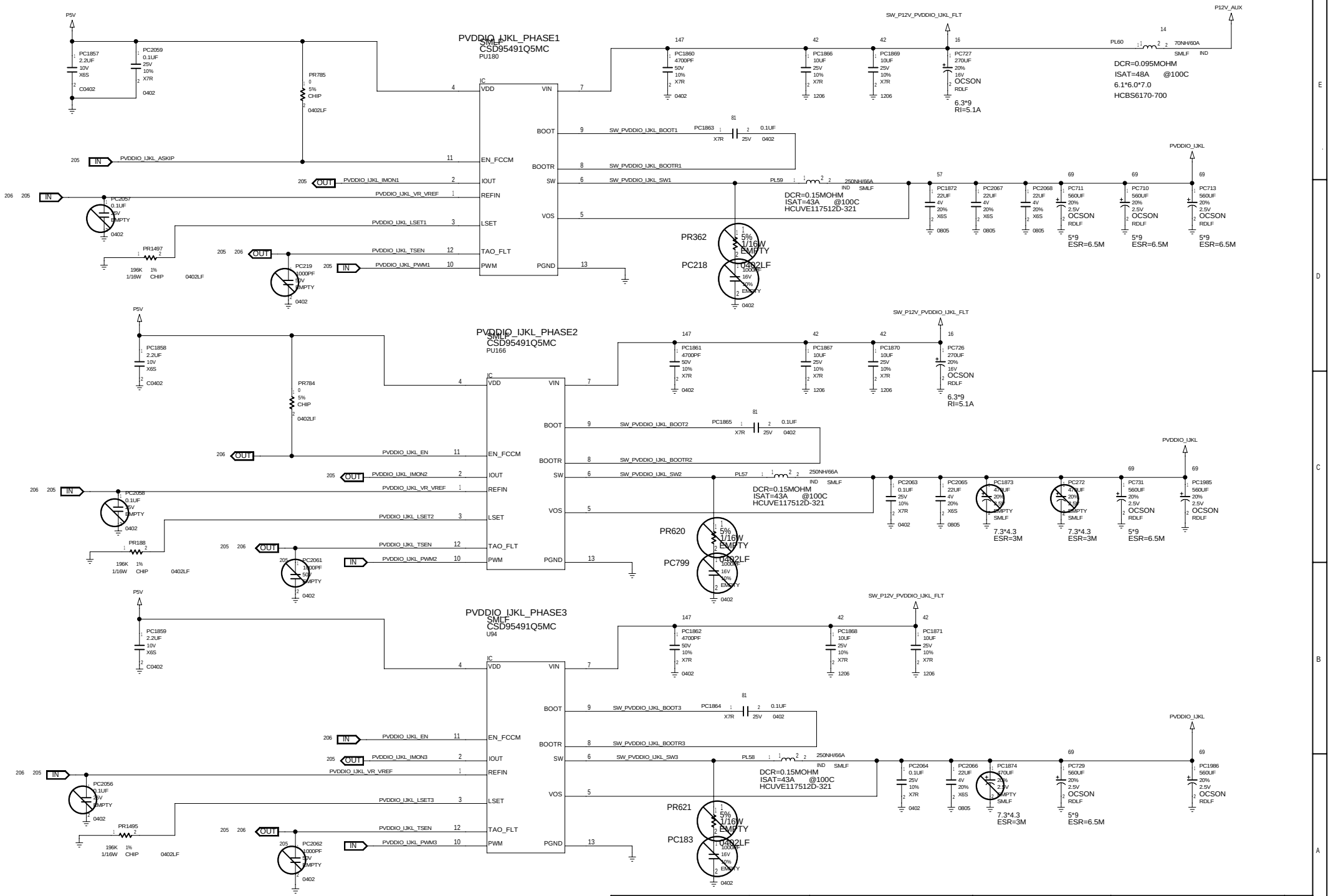

CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
SMLF
TPS53659RSBR
PU12
IC
PVDDIO_EFGH SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB.
2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CEH 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_EFGH 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
SIZE C
DATE Fri Dec 15 20:22:06 2017
SHEET 203 OF 226



PVDDIO_EFGH 2/2

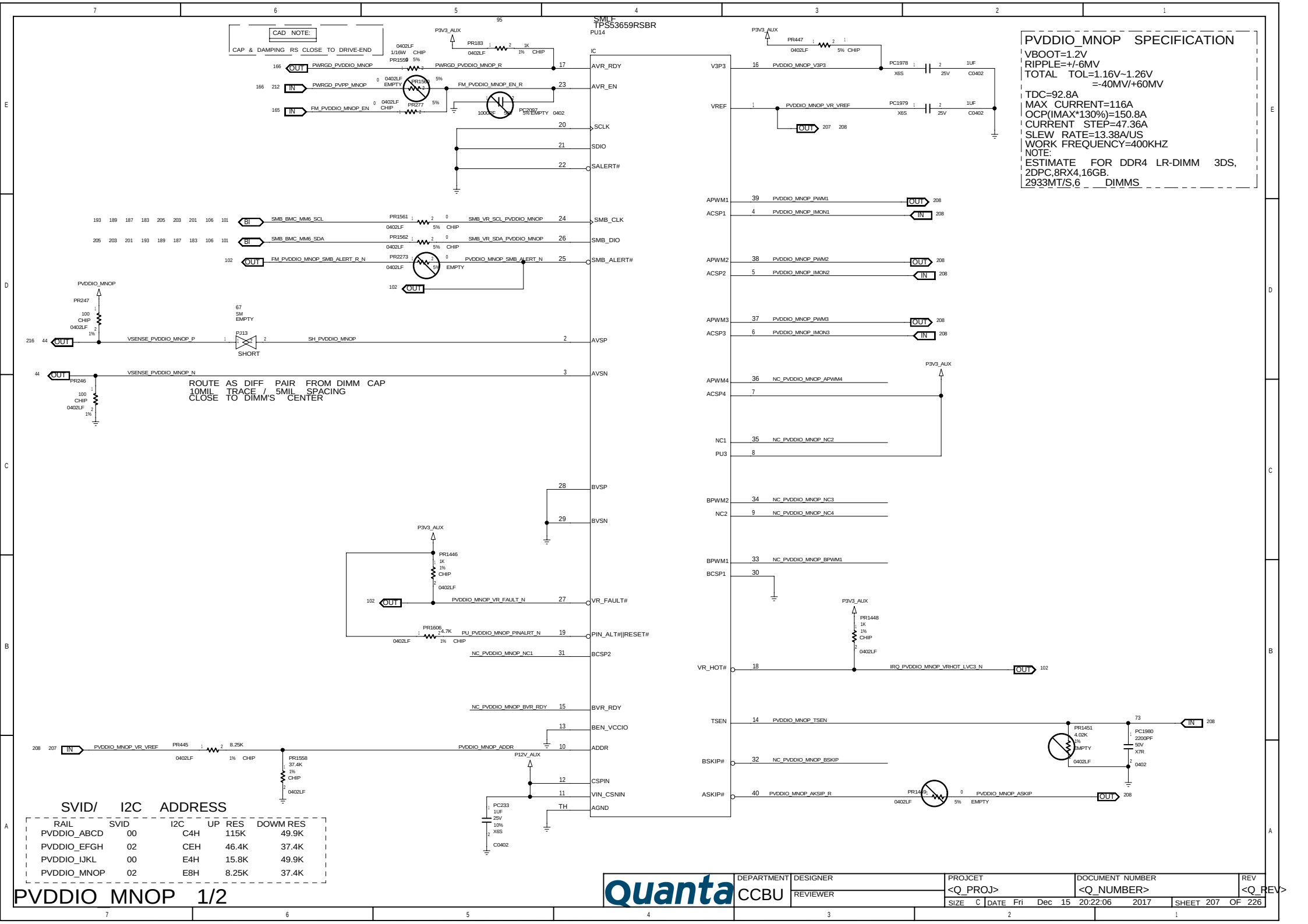
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>
		REVIEWER	SIZE C DATE Fri Dec 15 20:21:23 2017	REV <Q_REV> SHEET 204 OF 226

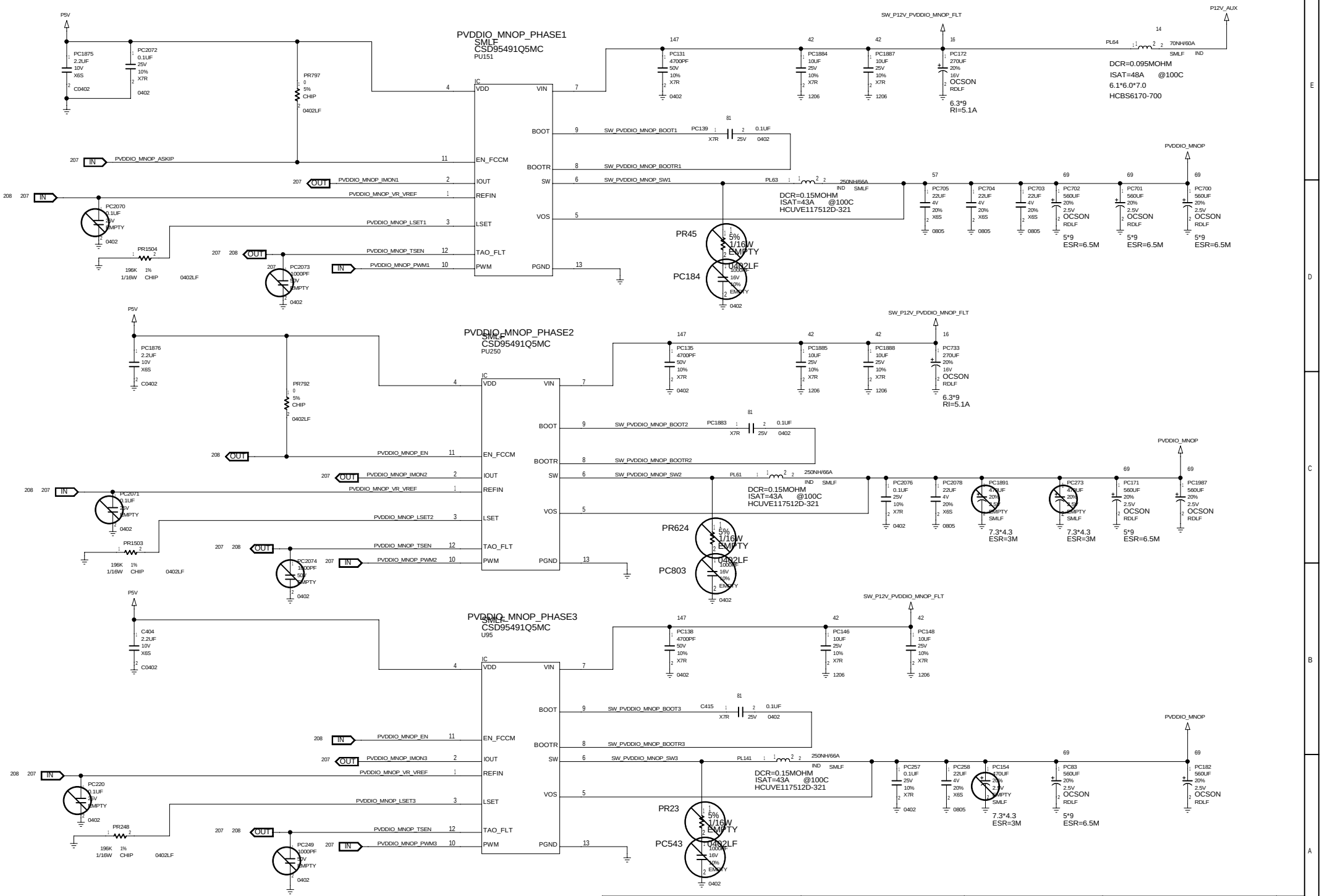

SMLF
TPS53659RSBR
PU13
CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
PVDDIO_IJKL SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB.
2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SHORT
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CHE 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_IJKL 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
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PVDDIO_IJKL 2/2

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CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
SMLF
TPS53659RSBR
PU14
IC
PVDDIO_MNOP SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB.
2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CEH 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_MNOP 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
SIZE C
DATE Fri Dec 15 20:22:06 2017
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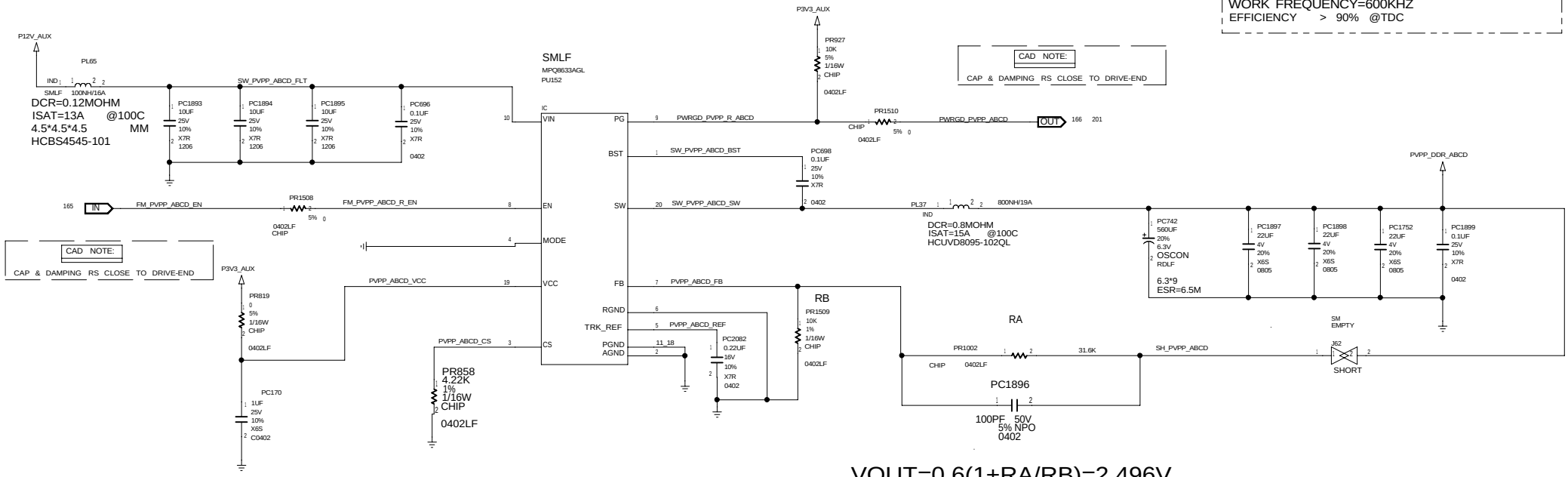
PVDDIO_MNOP 2/2

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:23 2017
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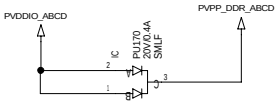
PVPP_DDR_ABCD

PVPP_DDR_ABCD SPECIFICATION

OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.6A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



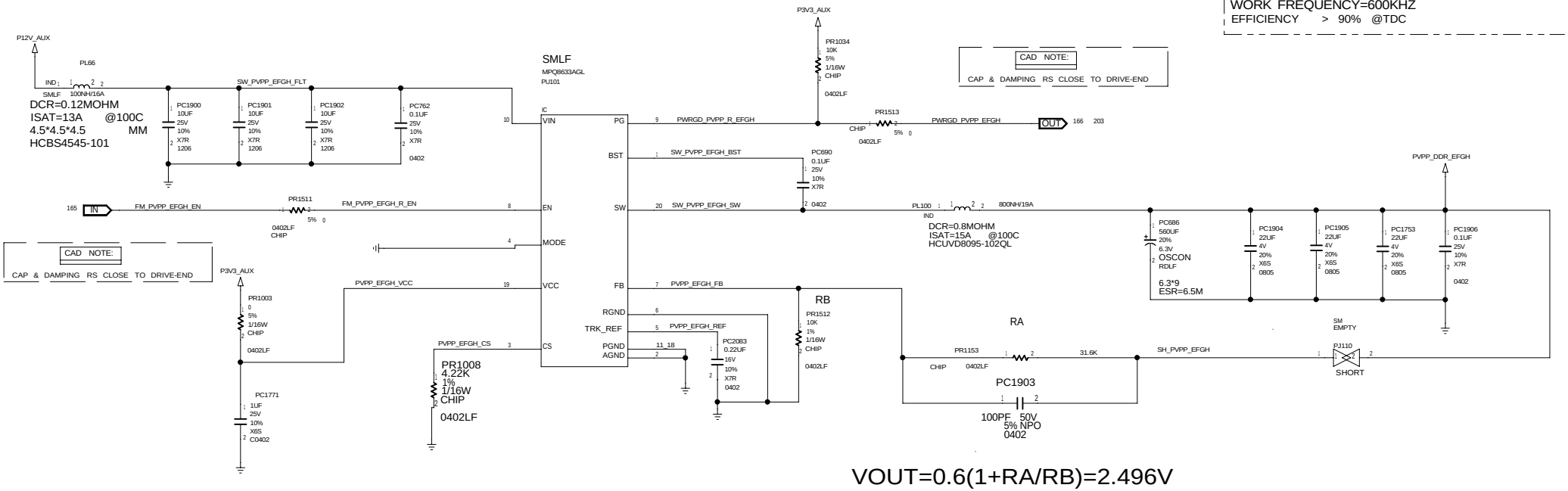
VOUT=0.6(1+RA/RB)=2.496V



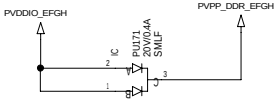
PVPP_DDR_EFGH

PVPP_DDR_EFGH SPECIFICATION

OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.2A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC

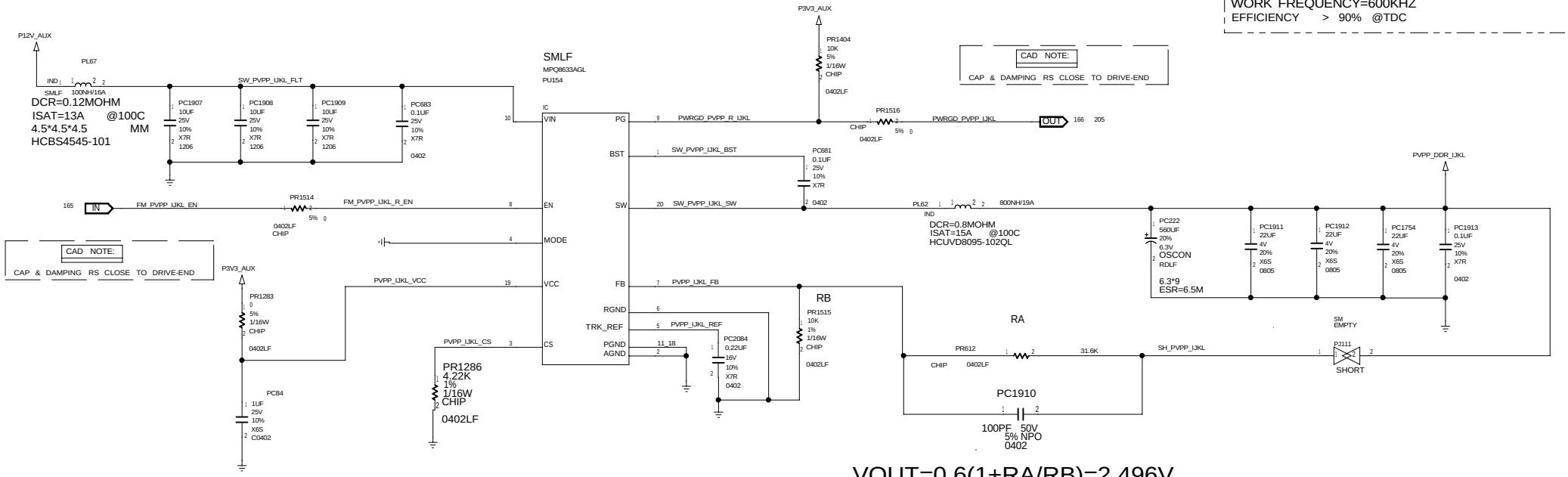


VOUT=0.6(1+RA/RB)=2.496V

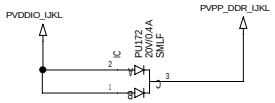


PVPP_DDR_IJKL

PVPP_DDR_IJKL SPECIFICATION
OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.6A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



VOUT=0.6(1+RA/RB)=2.496V



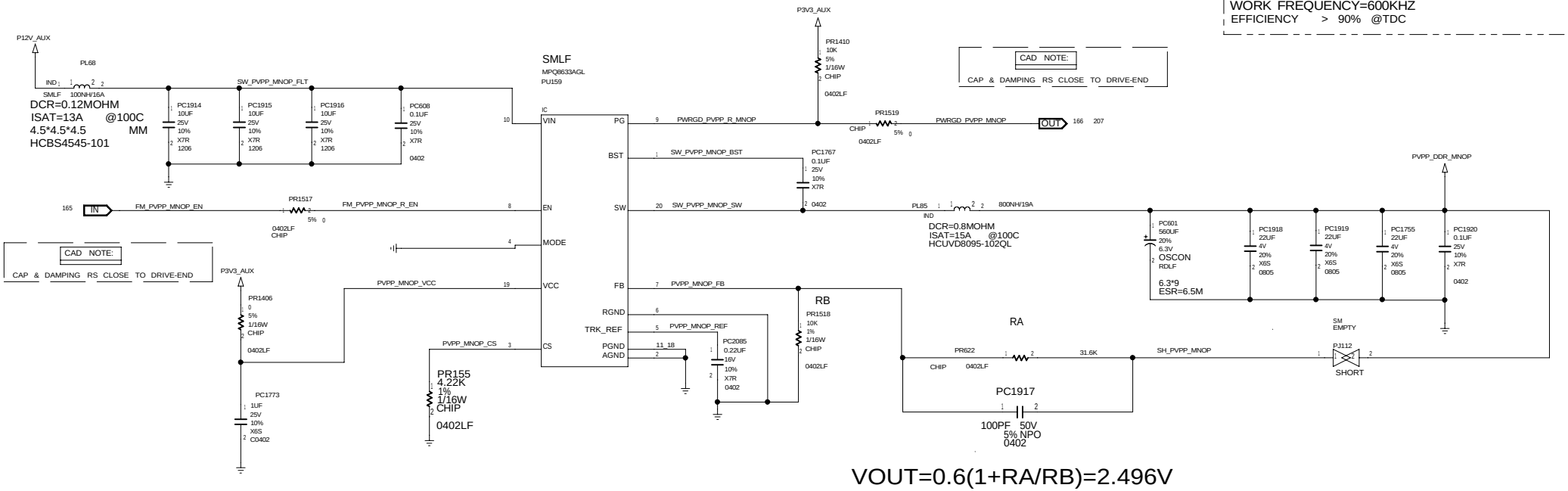
PVPP_DDR_IJKL

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
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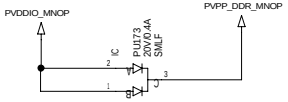
PVPP_DDR_MNOP

PVPP_DDR_MNOP SPECIFICATION

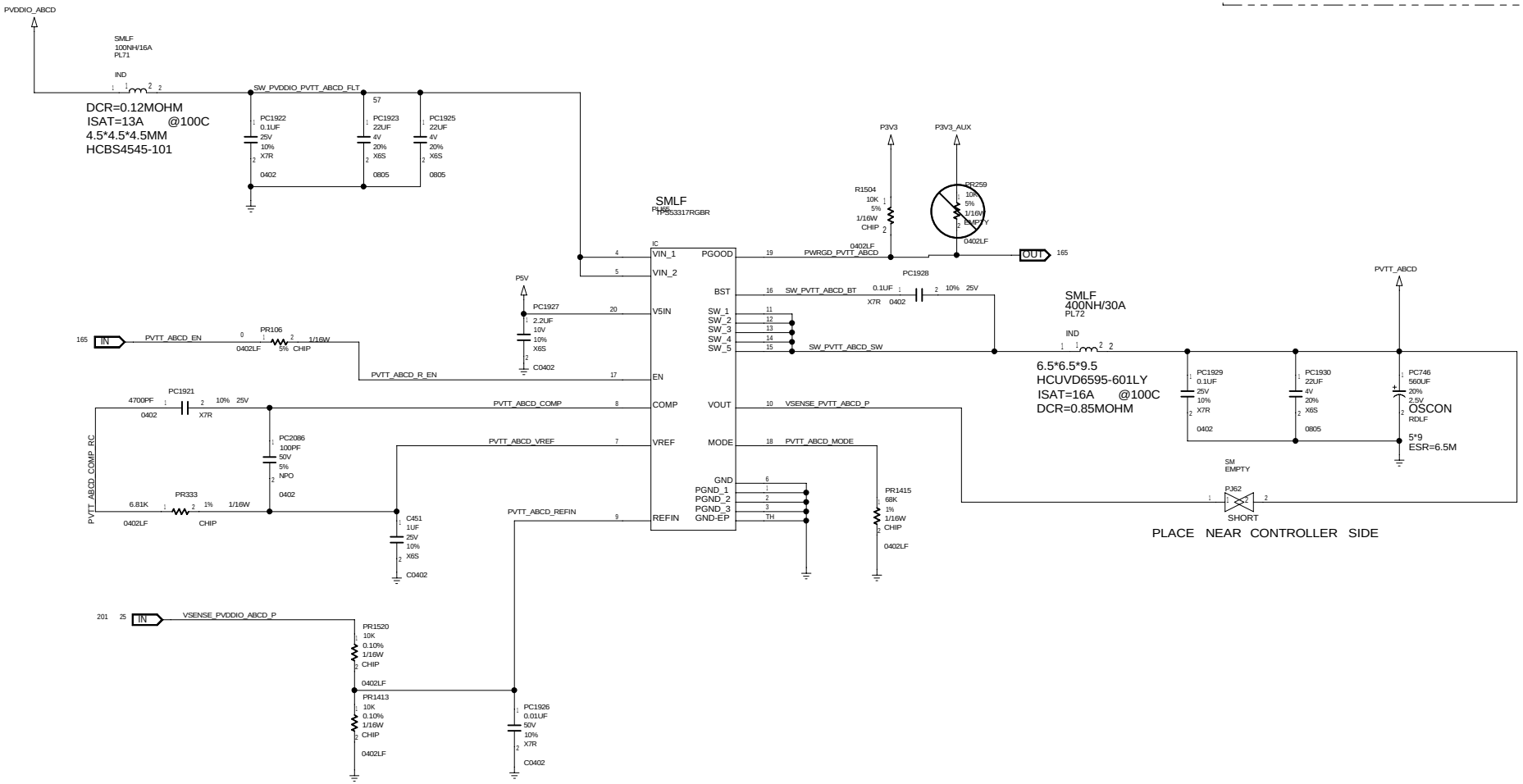
OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.6A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



VOUT=0.6(1+RA/RB)=2.496V



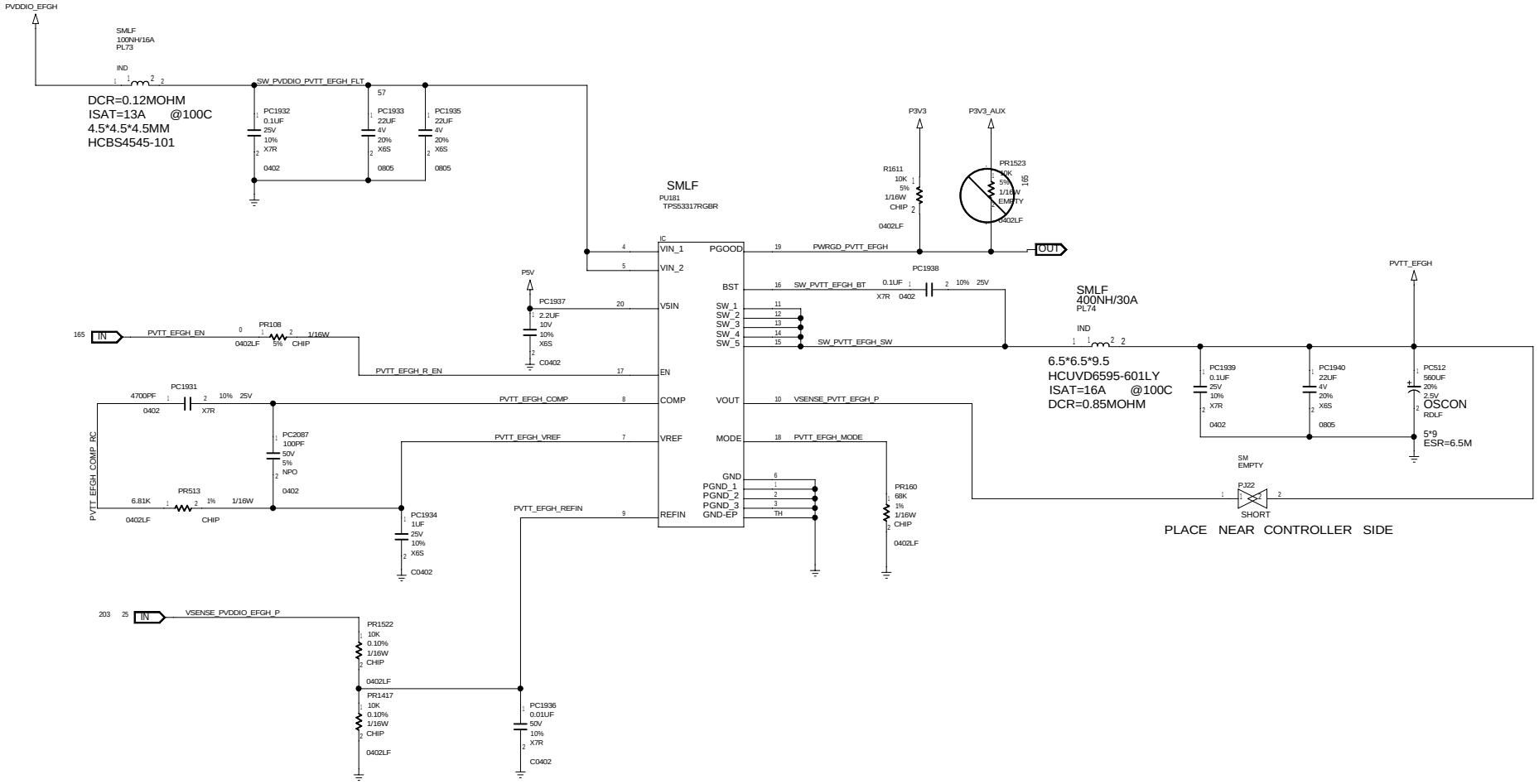
PVTT_ABCD SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_ABCD

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>
DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>	SIZE: C	DATE: Fri Dec 15 20:22:07 2017
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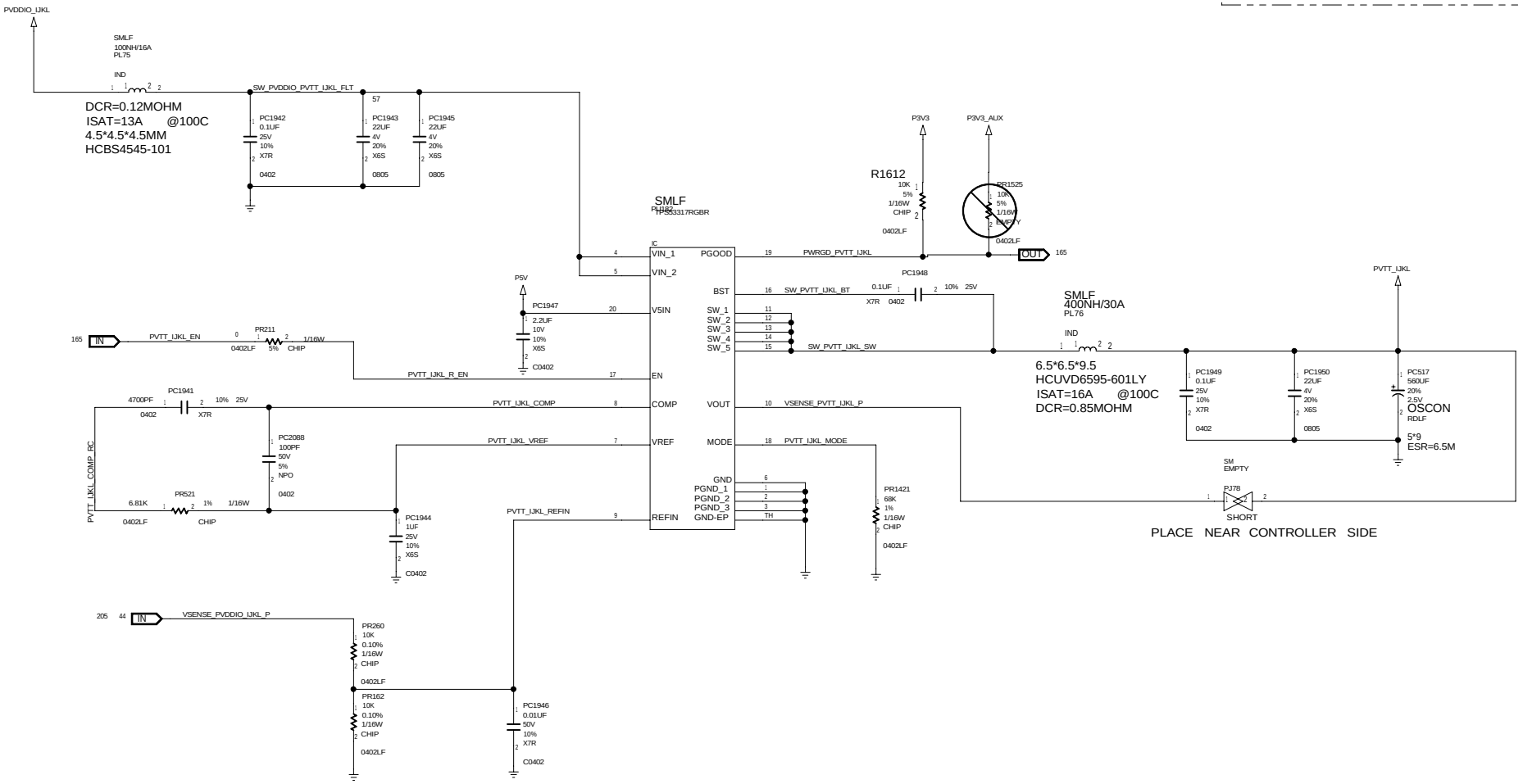
PVTT_EFGH SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_EFGH

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:07 2017	SHEET 214 OF 226

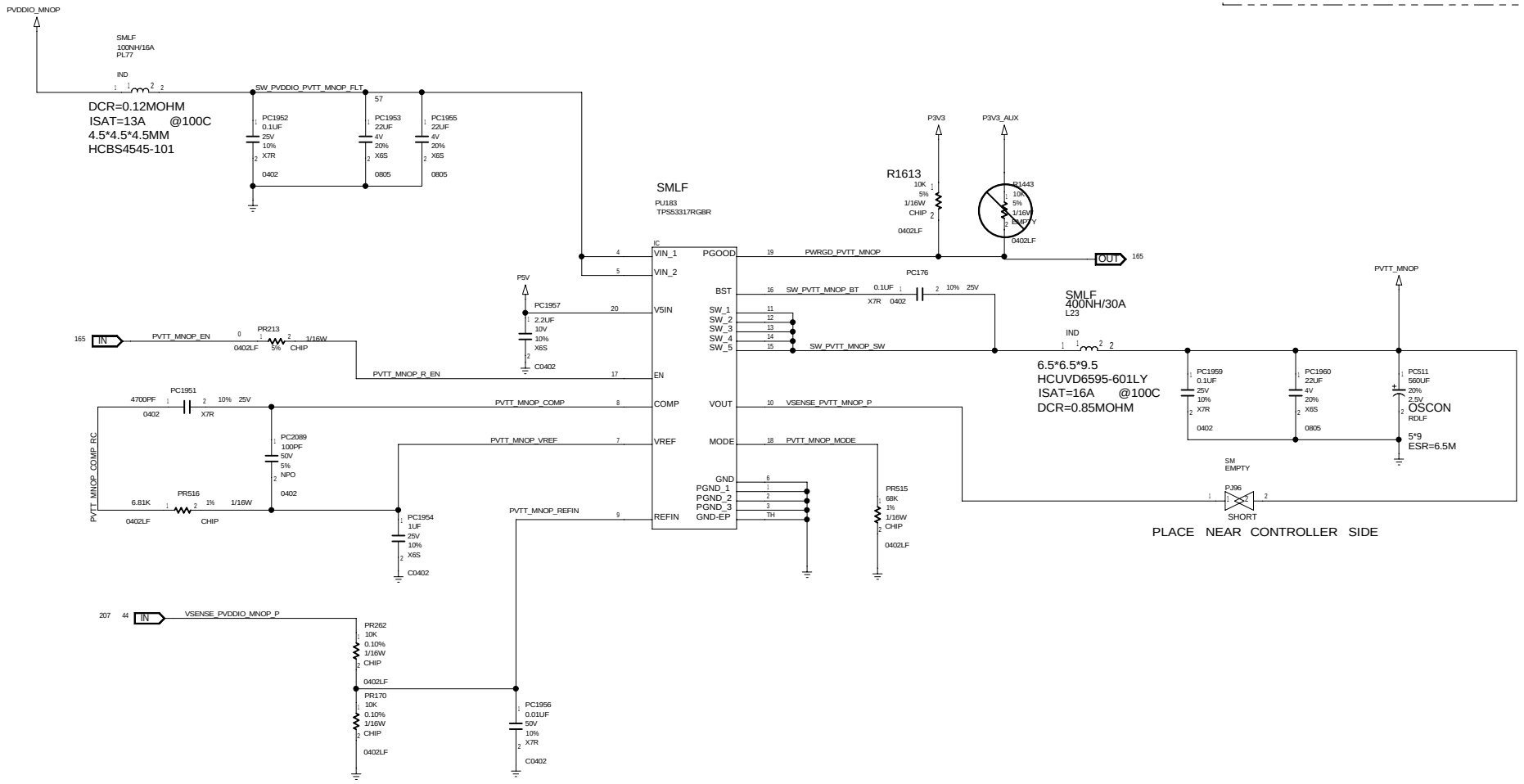
PVTT_IJKL SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_IJKL	Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>
				DOCUMENT NUMBER: <Q_NUMBER>
				REV: <Q_REV>
			SIZE: C	DATE: Fri Dec 15 20:22:07 2017
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PVTT_MNOP SPECIFICATION

VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



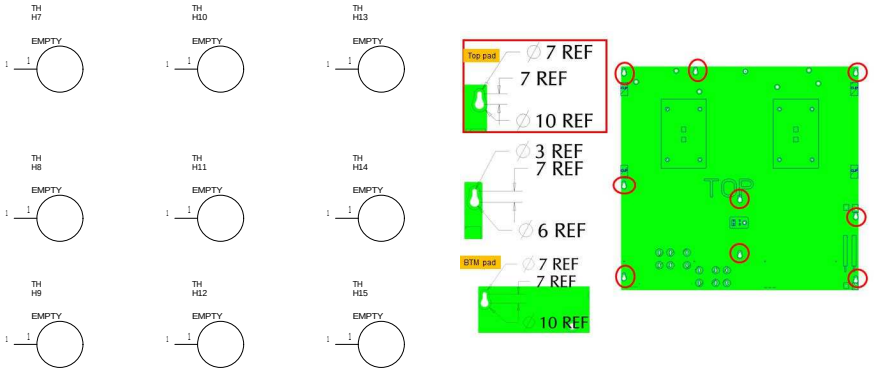
PVTT_MNOP

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
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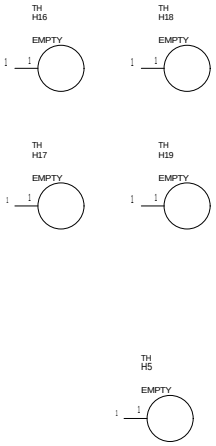
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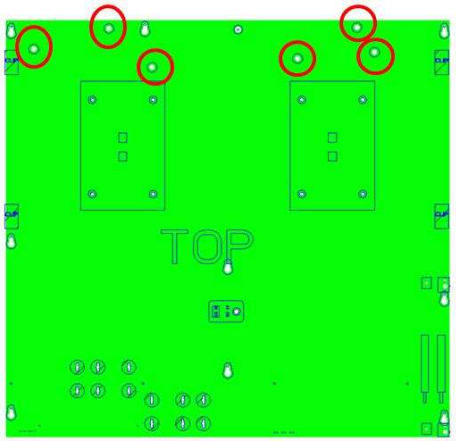
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			SIZE C	DATE Fri Dec 15 19:43:00 2017	SHEET 217 OF 226

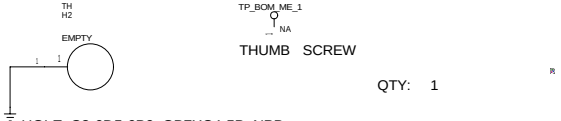
MLB SCREW HOLE
HOLE_C7D3_6B7_OB7XC5N_NPM
QTY: 9



AIR DEFLECTOR AND HS HOLE
HOLE_C7D5B9_NPM
QTY: 6



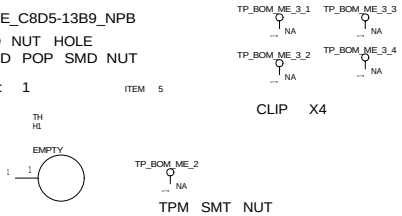




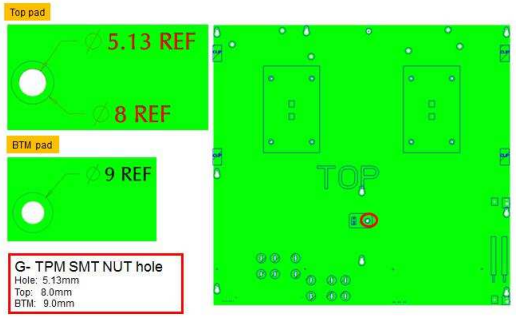
THUMB SCREW
QTY: 1

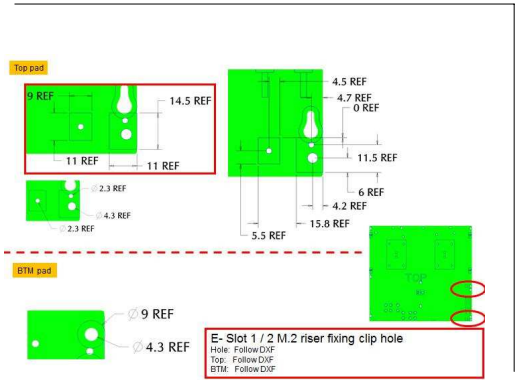
HOLE_C8-6D5-6B9_OB7XC4-5B_NPB
FOR THUMB SCREW
QTY: 1 ITEM 2

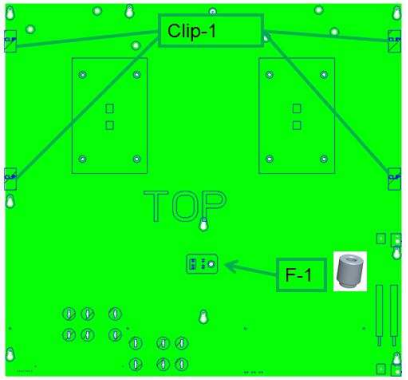
HOLE_C8D5-13B9_NPB
SMD NUT HOLE
NEED POP SMD NUT
QTY: 1 ITEM 5



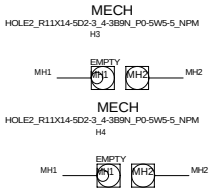
QTY: 1



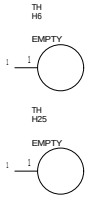




G-1 : MBT6M020010 (1pcs / per MB)
Clip 1 : JXS2V013010 (4pcs / per MB)



HOLE2_R11X14-5D2-3_4-3B9N_P0-5W5-5_NPM
HOLE FOR SLOT 1 / 2 M.2 RISER FIXING CLIP HOLE
QTY: 4



HOLE_R9X11D2-3TN_NPM
FOR M.2 RISER OF SLOT2
QTY: 2

SCREW HOLES

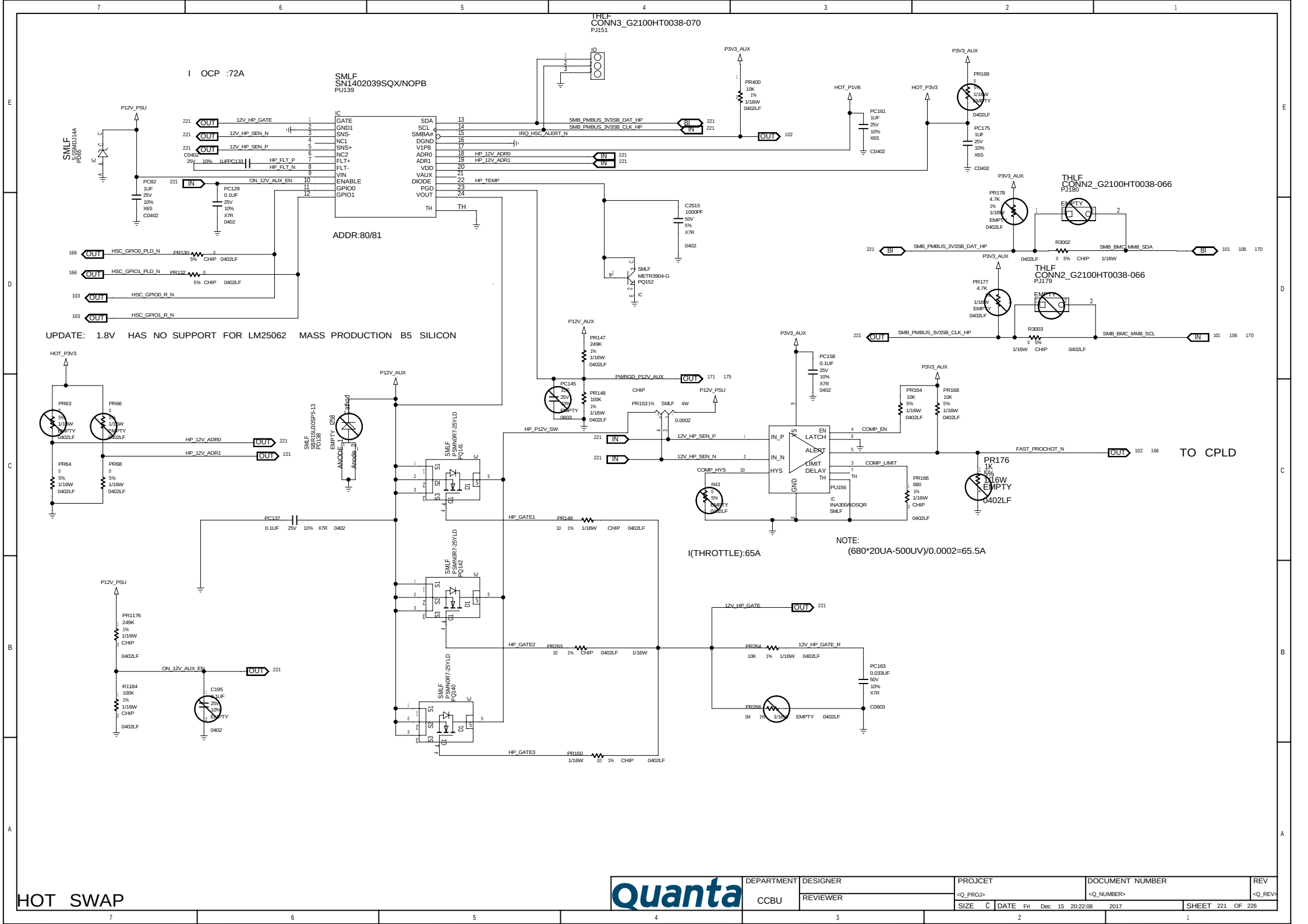
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:08 2017	SHEET 218 OF 226

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			SIZE C	DATE Fri Dec 15 19:37:13 2017	SHEET 219 OF 226

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Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE: C	DATE: Fri Dec 15 19:37:14 2017	SHEET 220 OF 226


THLF
CONN3_G2100HT0038-070
PJ151
I OCP :72A
SMLF
SN1402039SQX/NOPB
PU139
ADDR:80/81
UPDATE: 1.8V HAS NO SUPPORT FOR LM25062 MASS PRODUCTION B5 SILICON
THLF
CONN2_G2100HT0038-066
PJ180
PJ179
TO CPLD
I(THROTTLE):65A
NOTE:
(680*20UA-500UV)/0.0002=65.5A
HOT SWAP
Quanta
DEPARTMENT
CCBU
DESIGNER
REVIEWER
PROJCET
<Q_PROJ>
DOCUMENT NUMBER
<Q_NUMBER>
REV
<Q_REV>
SIZE C
DATE Fri Dec 15 20:22:08 2017
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UV CIRCUIT

	MIN	NORMAL	MAX
R2	17.82	18	18.18
R1	4.94	4.99	5.04
2.5_DIODE	2.48	2.5	2.52

P12V TRIP POINT IS 11.52V

$11.52*(R1/R1+R2)=2.5$

11VMAX

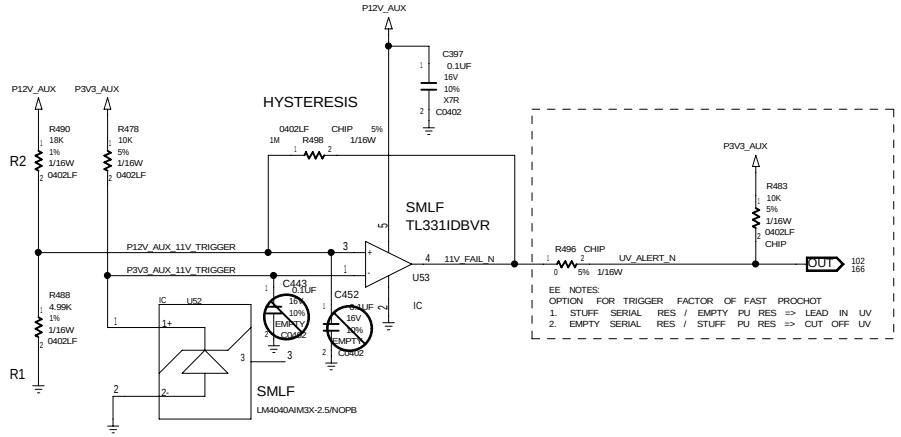
$$V=\frac{(R1_{MIN}+R2_{MAX})*2.5_DIODE}{R1_{MIN}}\ MAX$$

=11.79V

11VMIN

$$V=\frac{(R1_{MAX}+R2_{MIN})*2.5_DIODE}{R1_{MAX}}\ MIN$$

=11.25V



UV FOR ADR

	MIN	NORMAL	MAX
R2	16.73	16.9	17.07
R1	4.9401	4.99	5.04
2.5_DIODE	2.48	2.5	2.52

P12V TRIP POINT IS 10.967V

$10.967*(R1/R1+R2)=2.5$

10.5VMAX

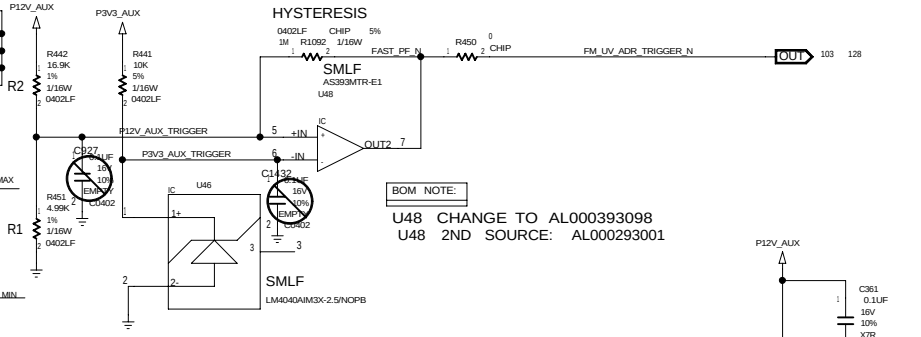
$$V=\frac{(R1_{MIN}+R2_{MAX})*2.5_DIODE}{R1_{MIN}}\ MAX$$

=11.23V

10.5VMIN

$$V=\frac{(R1_{MAX}+R2_{MIN})*2.5_DIODE}{R1_{MAX}}\ MIN$$

=10.71V

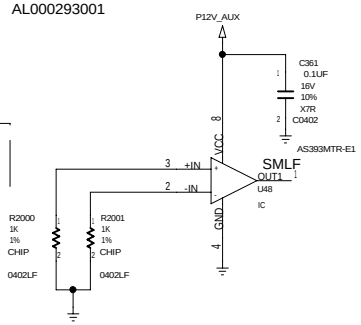


BOM NOTE:

U48 CHANGE TO AL000393098

U48 2ND SOURCE: AL000293001

BOM NOTE:U46,U52 CHANGE TO AL404025013 TO IMPROVE DERATING TEMPERATURE



VOLTAGE MONITOR

Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:25 2017
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MECH
WEEE
DM2

EMPTY
DUMMY_SYMBOL

MECH
PB-E1_SMALL
DM3

EMPTY
DUMMY_SYMBOL

MECH
PCB_VENDOR_LOGO_15X8
DM4

EMPTY
DUMMY_SYMBOL

BACKPLATE X2

TP2
NA

TP3
NA

SAM BRACKET X2

TP4
NA

TP5
NA

CARRIER FRAME X2

-> NO NEED, AMD WILL WHIP CPU WITH CARRIER FRAME

DUMMY SYMBOL

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> REV: <Q_REV>
		REVIEWER	SIZE C DATE Fri Dec 15 20:22:09 2017	SHEET 223 OF 226

PCB PN

PCB
NA

MAC LABEL

MAC_LABEL
NA

PN LABEL

HCS09004010
MECH
PCBA_LABEL_15X5
PN_LABEL

MECH
DUMMY_SYMBOL

BIOS LABEL

BMC LABEL

SN LABEL

HCS67003010
MECH
BARCODE
SN_LABEL

MECH
DUMMY_SYMBOL

AIRDUCT_RIGHT

AIRDUCT_LEFT

LASER MARK

COMPONENT SIDE(TOP)

MECH
LASER_MARK_LABELS_10X10B
DM5

EMPTY
DUMMY_SYMBOL

SOLDER SIDE(BOT)

MECH
LASER_MARK_LABELS_10X10B
DM6

EMPTY
DUMMY_SYMBOL

SCREW FOR M.2

SCREW FOR M.2

SCREW HLOE

TH
H23
EMPTY

TH
H24
EMPTY

TH
H28
EMPTY

TH
H30
EMPTY

NUT FOR LAN MEZZ

DUMMY SYMBOL

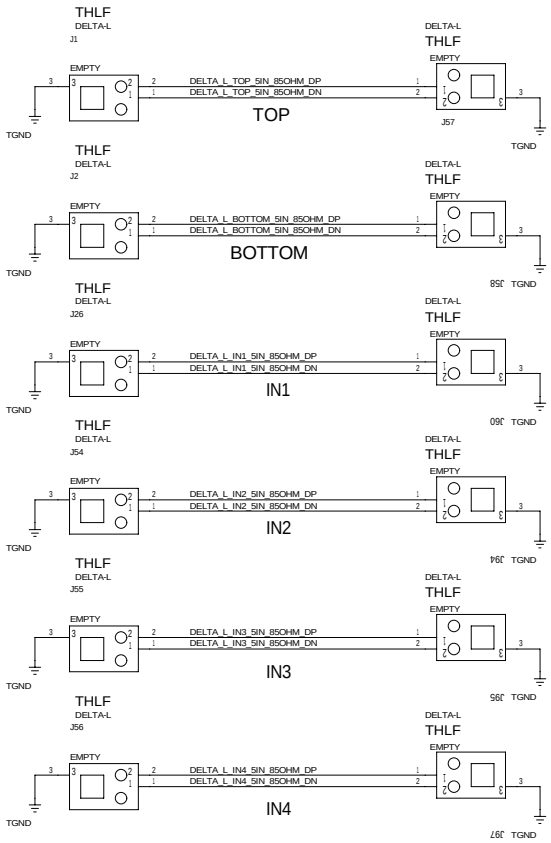
Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:09 2017
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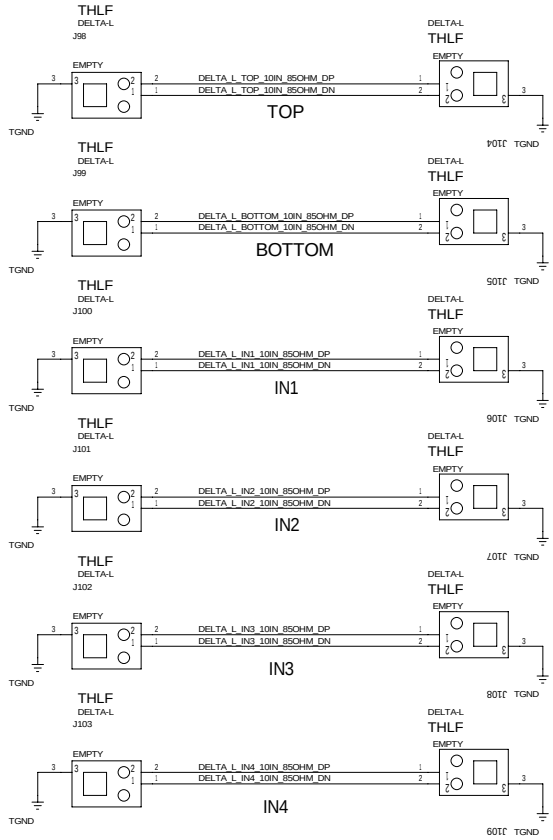
Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
		REVIEWER:	SIZE C	DATE Fri Dec 15 19:37:18 2017	SHEET 225 OF 226

DELTA-L: CONTROL PCB LOSS

85 OHM, 5INCH



85 OHM, 10INCH



DELTA L

Quanta	DEPARTMENT: CCBU	DESIGNER:	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER> / REV: <Q_REV>
		REVIEWER:	SIZE: C / DATE: Fri Dec 15 20:22:10 2017	SHEET 226 OF 226