OPEN EDGE RMC

FAB: A
REV: 1.15
PCB: DAS9NMD18A0
PCBA:3AS9NMA0010

COVER

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 13:57:32 2018	REV: 1.15
				SHEET: 1 OF 41

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27	BMC MEM DDR4
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29	FT2232
30	RTC
31	SCREW HOLE
32	COUPON-DELTA-L
33	TPS259261DRCR/HotSwap/P12V_STBY
34	MPQ8626GD-Z/P3V3_RMC_STBY
35	RT2518GQW/P2V5_AUX
36	RT7251BZQW/P1V2_AUX
37	RT7251BZQW/P1V15_AUX
38	MPQ8628GD-Z/P1V_VDD_AUX
39	NB682/P1V_AVDD_AUX
40	RT7251BZQW/P5V_STBY

PAGE(S)	CONTENTS
41	P3V3_RMC_AUX

PAGE(S)	CONTENTS

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NOKIA

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	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 13:57:43 2018		SHEET 2 OF 41

MECH
WEEE
DM2
DUMMY2
EMPTY
DUMMY_SYMBOL 1

MECH
PB-E1_SMALL
DM3
DUMMY3
EMPTY
DUMMY_SYMBOL 1

MECH
PCBA_LABEL_15X5
DM4
DUMMY4
MECH
DUMMY_SYMBOL 1

MECH
EFI BIOS LABEL
DM1
DUMMY28_HCLU2002010
EMPTY
DUMMY_SYMBOL 1

MECH
BARCODE_20X6
DM8
DUMMY15
MECH
DUMMY_SYMBOL 1

MECH
BARCODE_20X6
DM7
DUMMY15
MECH
DUMMY_SYMBOL 1

MECH
PCB_VENDOR_LOGO_15X8
DM6
DUMMY7
EMPTY
DUMMY_SYMBOL 1

MECH
BMC_FLASH
DM5
DUMMY8
MECH
DUMMY_SYMBOL 1

MECH
BMC_FLASH
DM10
DUMMY8
MECH
DUMMY_SYMBOL 1

BOM NOTE:

BOM ADD
P/N:AKE3EFZ0Z00
P/N:AKE3LF-0Z00

MECH
BATTERY_SYMBOL
DM9
DUMMY12
MECH
DUMMY_SYMBOL 1

BOM NOTE:

BOM ADD
P/N:FBS5S23901

BOM NOTE:

BOM ADD
P/N:AHL03003003

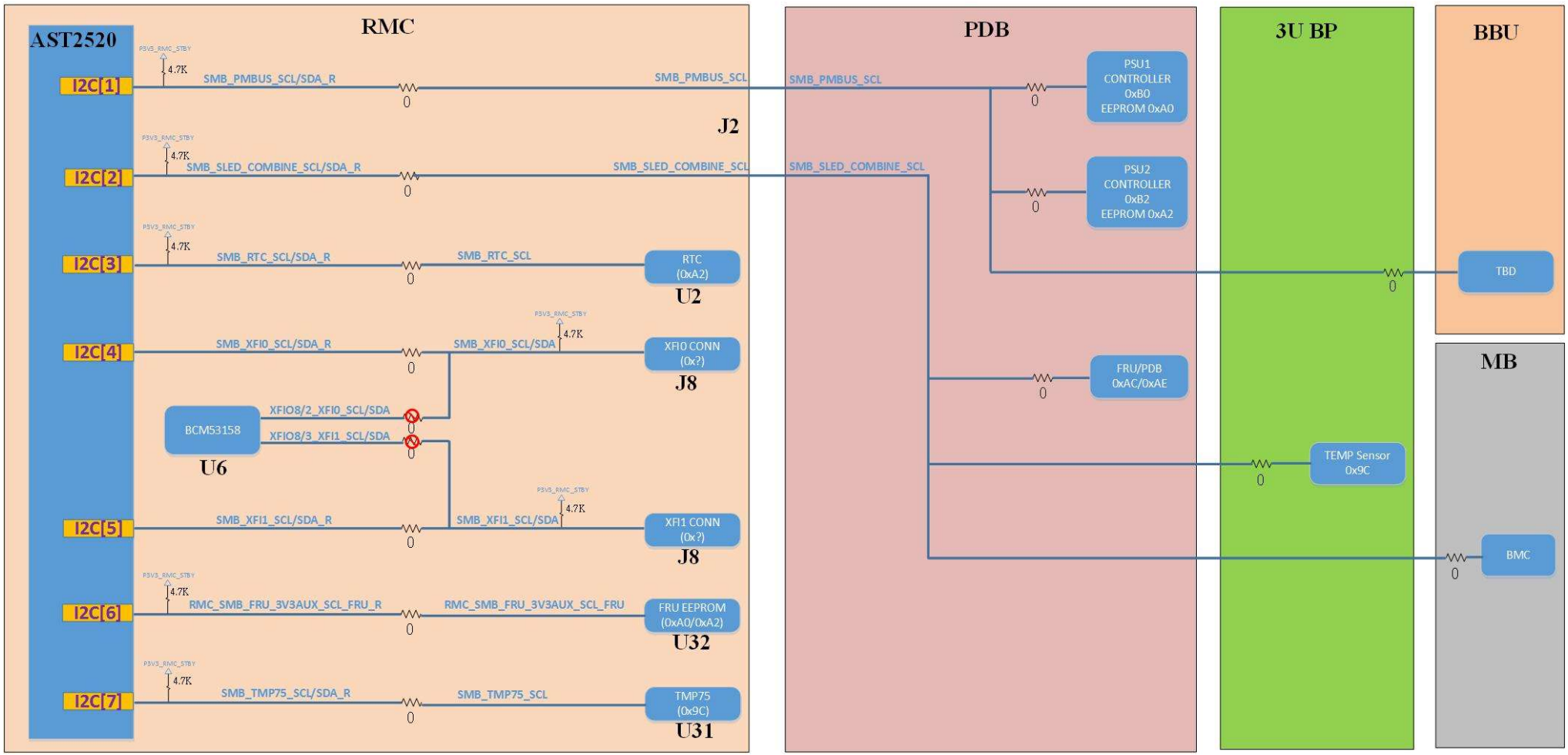
LASER_MARK

UNTITLED

NOKIA

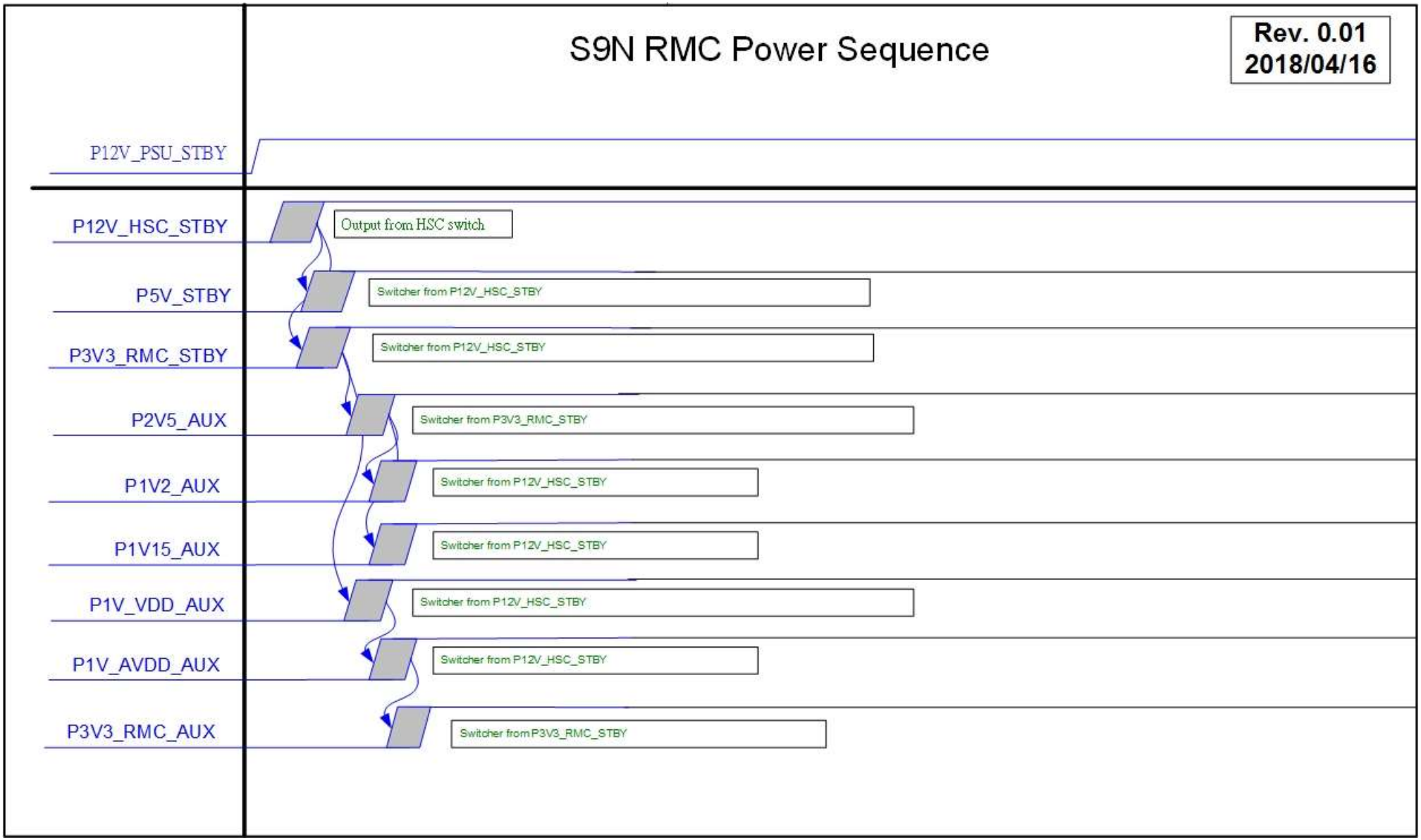
DEPARTMENT	DESIGNER NAME	PROJCET	DOCUMENT NUMBER	REV
BU9	REVIEWER NAME	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:29:41 2018	SHEET 3 OF 41	

S9N RMC SMbus Block Diagram
FAB2 v01



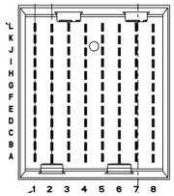
SMBUS DIAGRAM

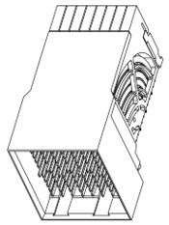
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		REVIEWER	SIZE: C	DATE: Wed Nov 21 14:19:37 2018	SHEET: 4 OF 41

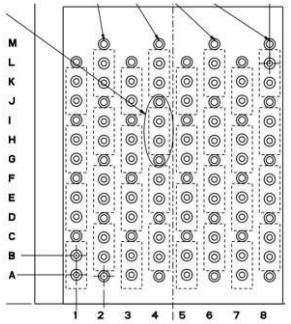


POWER SEQUENCE

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:01:04 2018	REV: 1.15
				SHEET: 5 OF 41







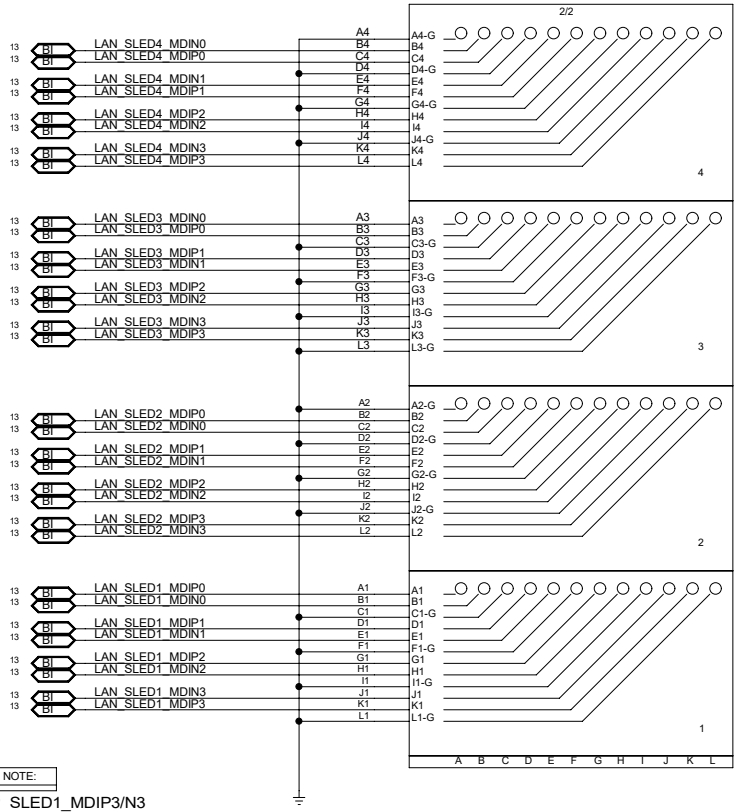
BOM NOTE:

MFR: 10136593-102LF

TO PDB

J2
THLF
CONN96_10136593-102LF
PART_NUMBER
IO

2/2



DESIGN NOTE:

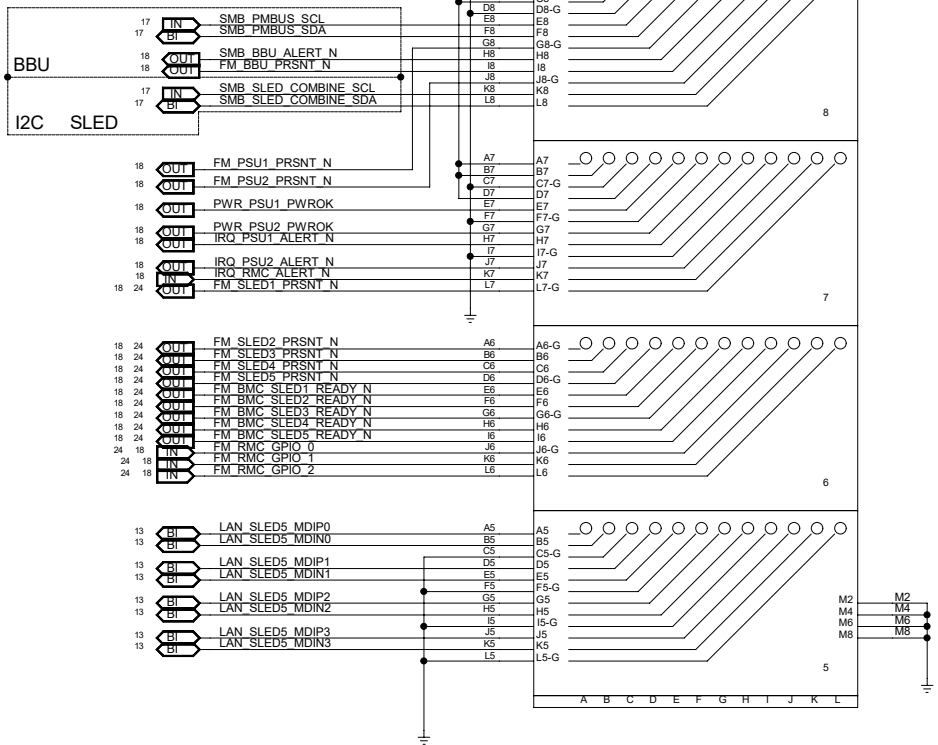
SWAP SLED1_MDIP3/N3
SWAP SLED3_MDIN0/P0
SWAP SLED3_MDIN3/P3
SWAP SLED4_MDIN3/P3
SWAP SLED4_MDIN1/P1
SWAP SLED4_MDIN0/P0

P3V3_RMC_STBY BY
RMC PROVIDED

THLF
CONN96_10136593-102LF
J2
PART_NUMBER
IO

P3V3_RMC_STBY
P12V_PSU_STBY

1/2

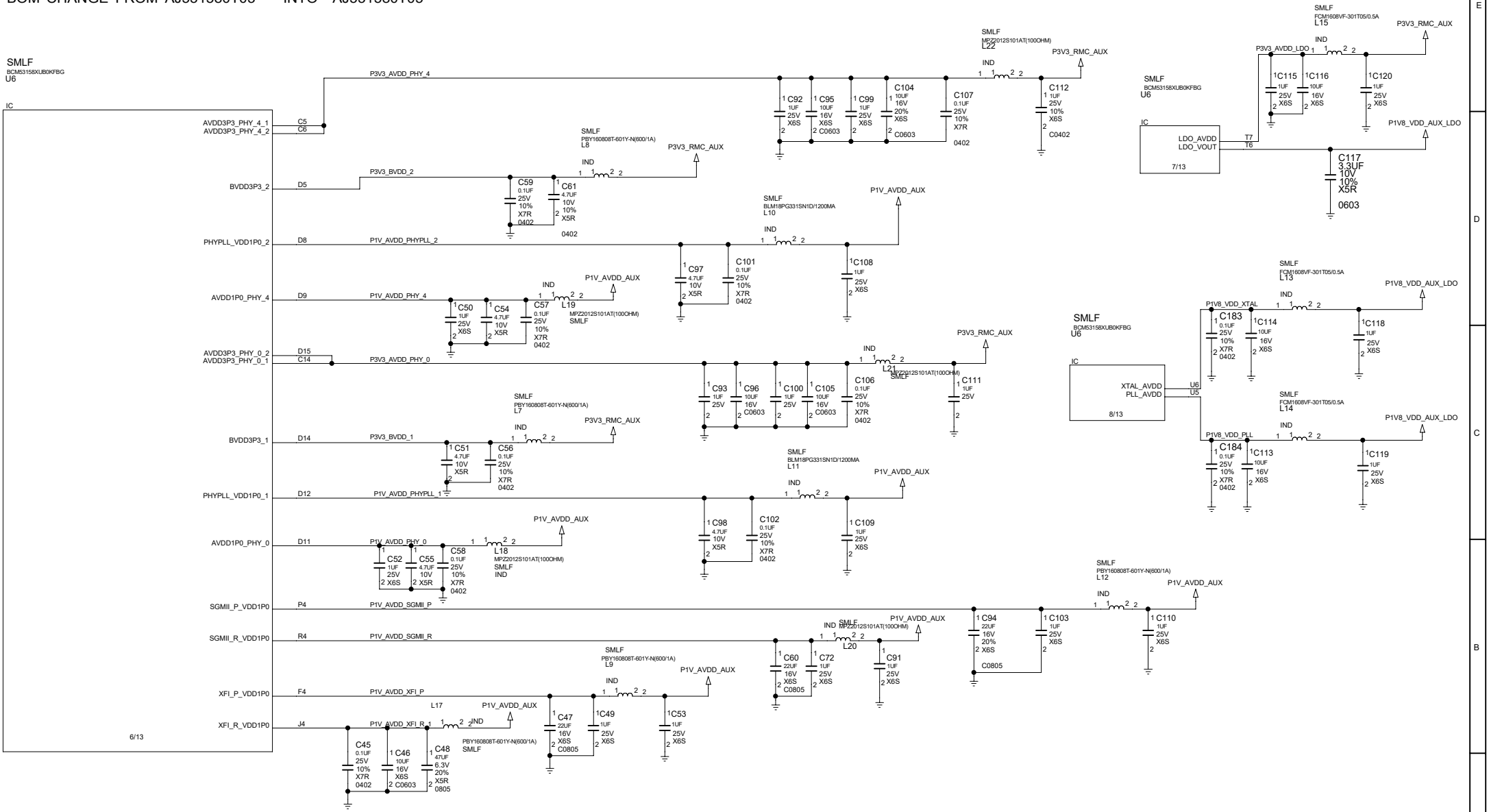


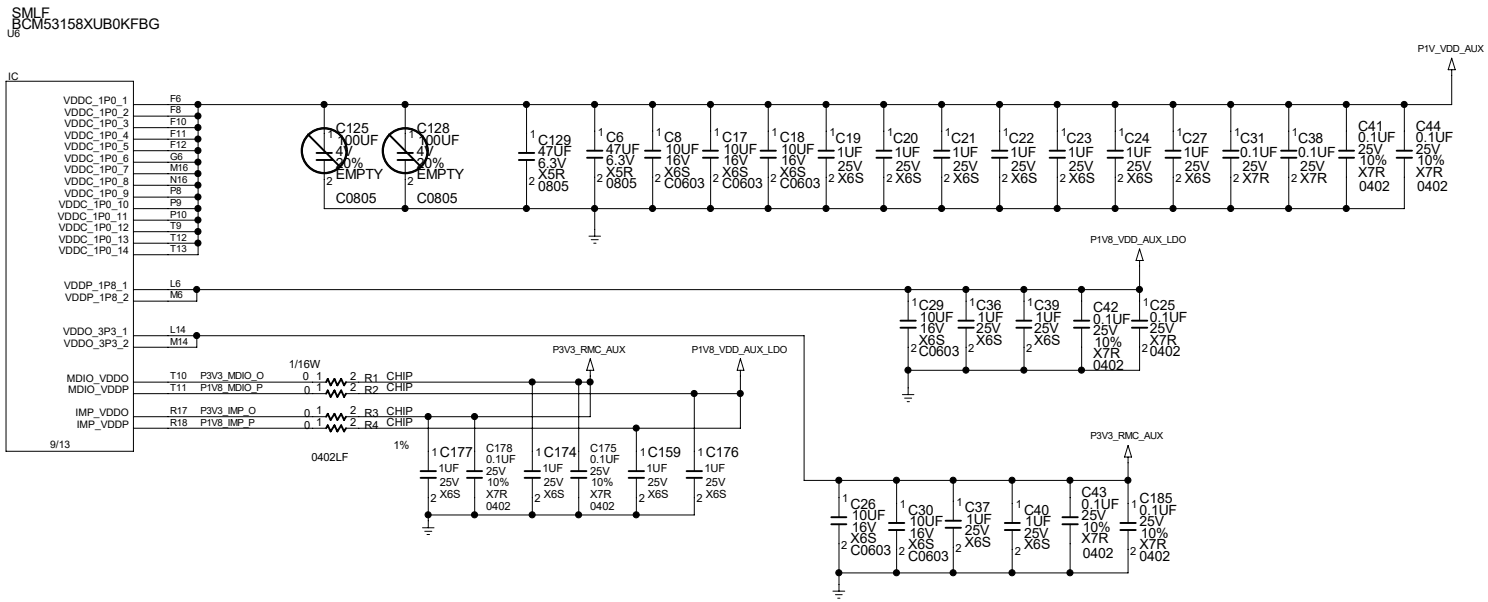
AIRMAX VS2 RAR (TO PDB)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:01:13 2018		SHEET 6 OF 41

BOM NOTE:

BOM CHANGE FROM AJ531580T03 INTO AJ531580T05





BCM53158 POWER2

NOKIA	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
		REVIEWER	OPEN EDGE RMC	N/A	1.15
			SIZE C DATE Wed Nov 21 14:03:18 2018		SHEET 8 OF 41

SMLF
BCM53158XUB0KFBG
U6

IC

VSS_1	F1
VSS_2	F2
VSS_3	F3
VSS_4	F7
VSS_5	F9
VSS_6	F13
VSS_7	F14
VSS_8	G7
VSS_9	G8
VSS_10	G9
VSS_11	G10
VSS_12	G11
VSS_13	G12
VSS_14	G13
VSS_15	H6
VSS_16	H7
VSS_17	H8
VSS_18	H9
VSS_19	H10
VSS_20	H11
VSS_21	H12
VSS_22	H13
VSS_23	J6
VSS_24	J7
VSS_25	J8
VSS_26	J9
VSS_27	J10
VSS_28	J11
VSS_29	J12
VSS_30	J13
VSS_31	J14
VSS_32	K6
VSS_33	K7
VSS_34	K8
VSS_35	K9
VSS_36	K10
VSS_37	K11
VSS_38	K12
VSS_39	K13
VSS_40	K14
VSS_41	L7
VSS_42	L8
VSS_43	L9
VSS_44	L10
VSS_45	L11
VSS_46	L12
VSS_47	L13
VSS_48	M7
VSS_49	M8
VSS_50	M9
VSS_51	M10
VSS_52	M11
VSS_53	M12
VSS_54	M13
VSS_55	N6
VSS_56	N7
VSS_57	N8
VSS_58	N9
VSS_59	N10
VSS_60	N11
VSS_61	N12
VSS_62	N13
VSS_63	N14
VSS_64	P7
VSS_65	P11
VSS_66	P14
VSS_67	T5

10/13

SMLF
BCM53158XUB0KFBG
U6

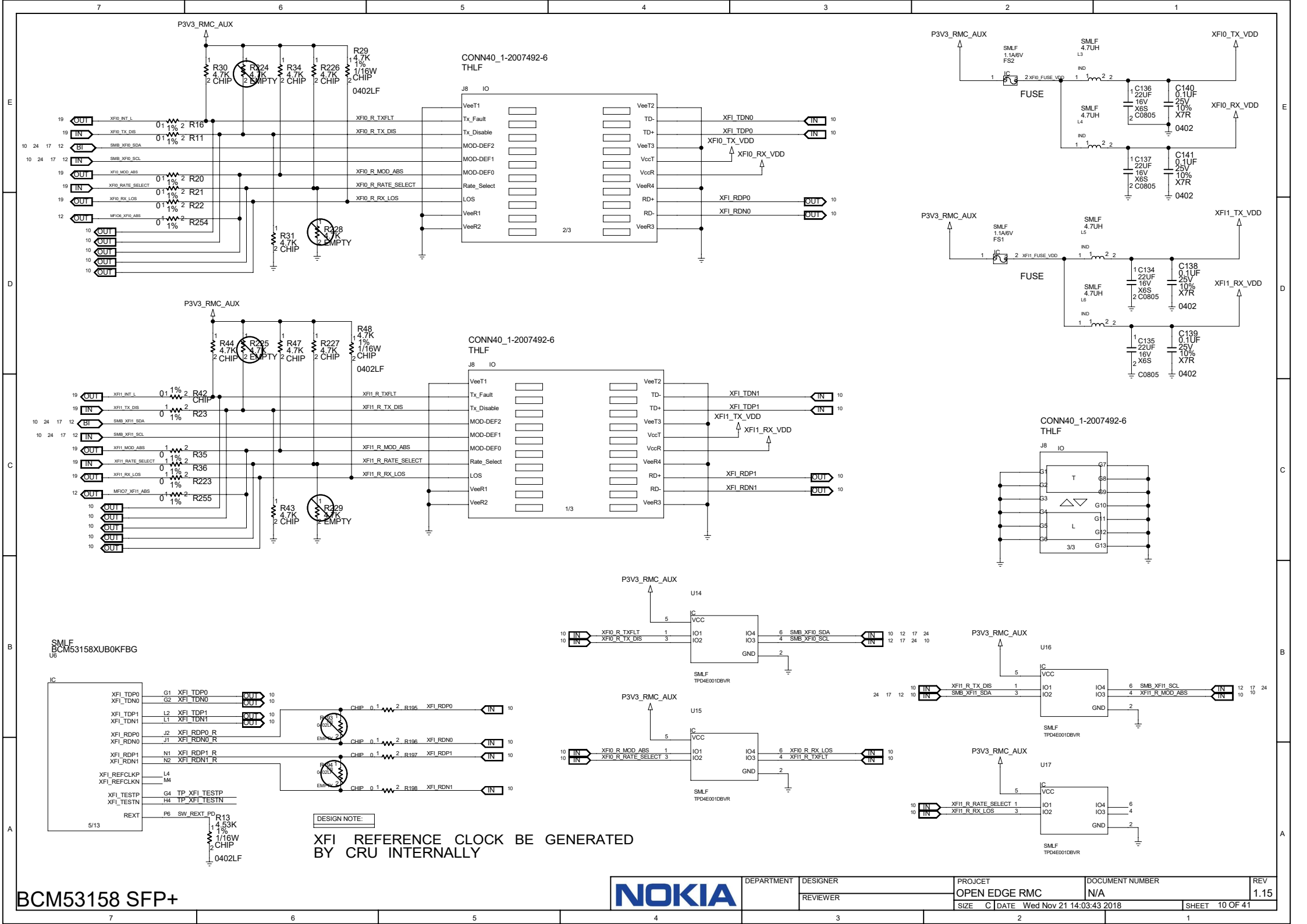
IC

VSS_68	T8
VSS_69	W19
VSS_70	T1
VSS_71	T2
VSS_72	U3
VSS_73	V1
VSS_74	V2
VSS_75	G3
VSS_76	H1
VSS_77	H2
VSS_78	H3
VSS_79	J3
VSS_80	K1
VSS_81	K2
VSS_82	K3
VSS_83	K4
VSS_84	L3
VSS_85	M1
VSS_86	M2
VSS_87	M3
VSS_88	N3
VSS_89	P1
VSS_90	P2
VSS_91	P3
VSS_92	W1
VSS_93	V3
VSS_94	V5
VSS_95	V6
VSS_96	W4
VSS_97	W7
VSS_98	E5
VSS_99	A1
VSS_100	A19
VSS_101	C7
VSS_102	C8
VSS_103	C9
VSS_104	C10
VSS_105	C11
VSS_106	C12
VSS_107	C13
VSS_108	C15
VSS_109	D4
VSS_110	D6
VSS_111	D7
VSS_112	D10
VSS_113	D13
VSS_114	D16
VSS_115	E3
VSS_116	E4
VSS_117	F16
VSS_118	L17
VSS_119	L18

11/13

BCM53158 POWER3

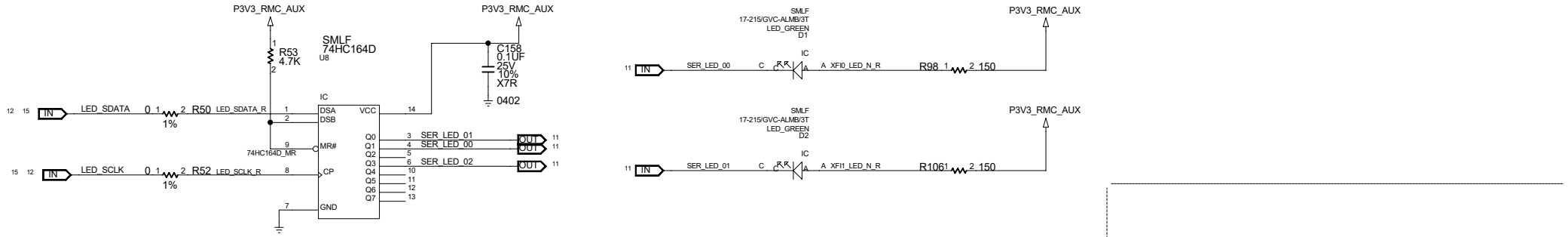
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		REVIEWER	OPEN EDGE RMC	N/A	1.15
			SIZE C	DATE Wed Nov 21 14:03:27 2018	SHEET 9 OF 41



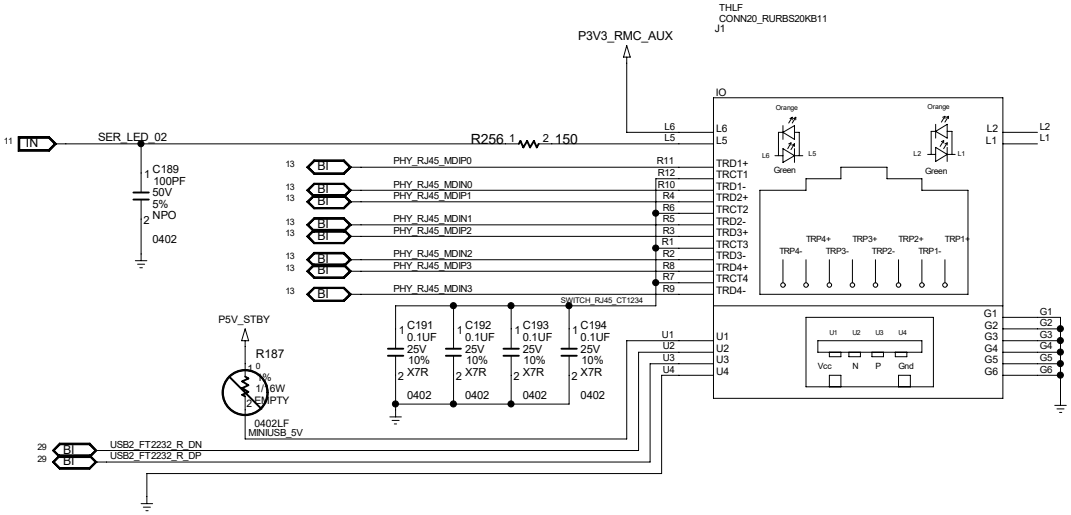
BCM53158 SFP+

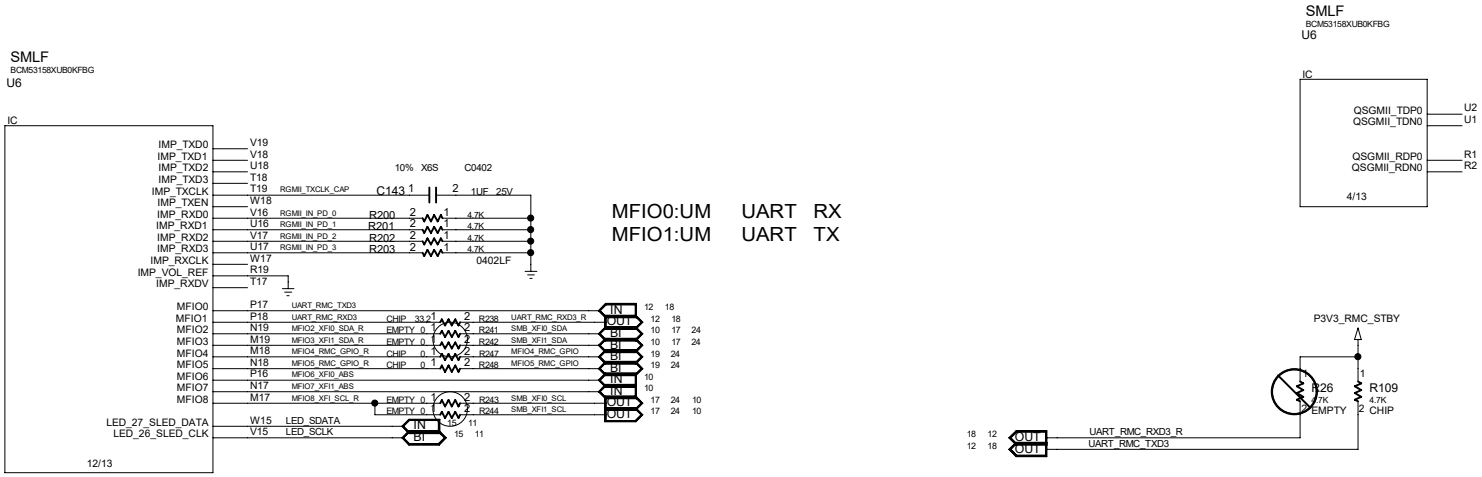
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				SHEET: 10 OF 41

LAN STATUS LED



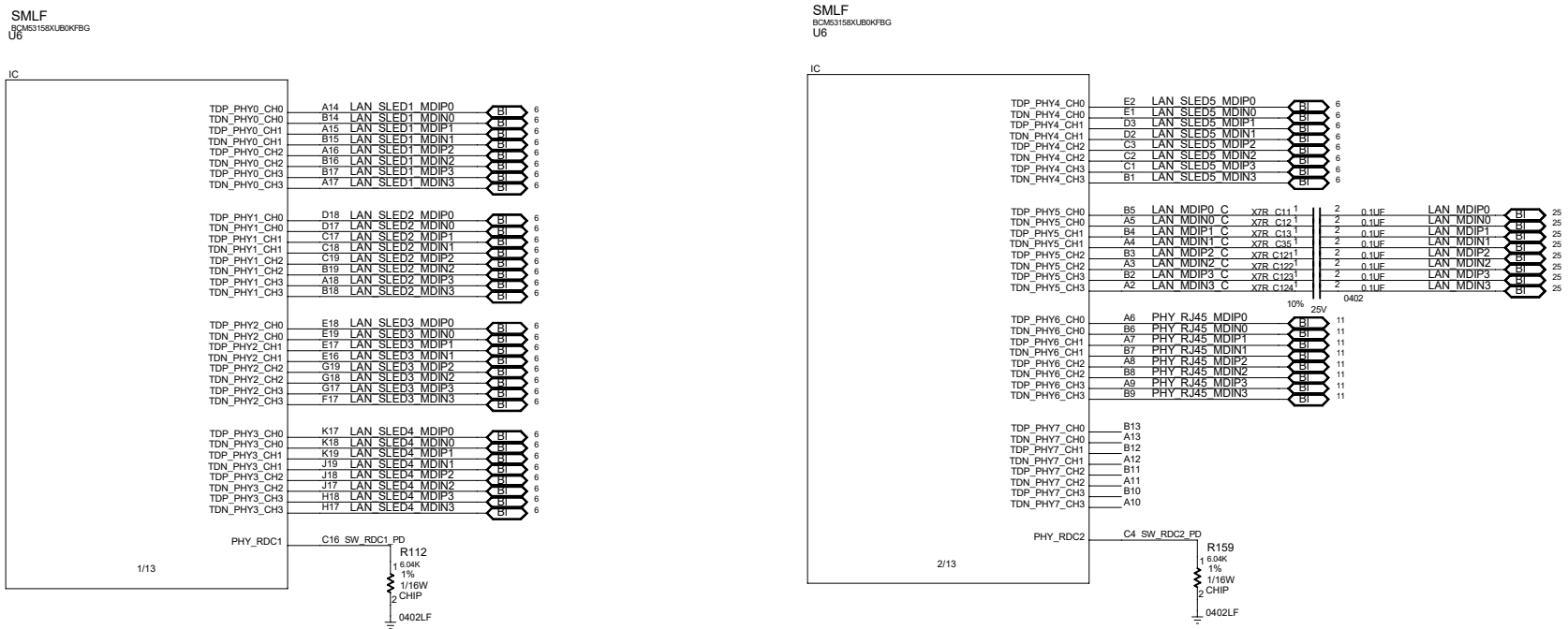
RJ45





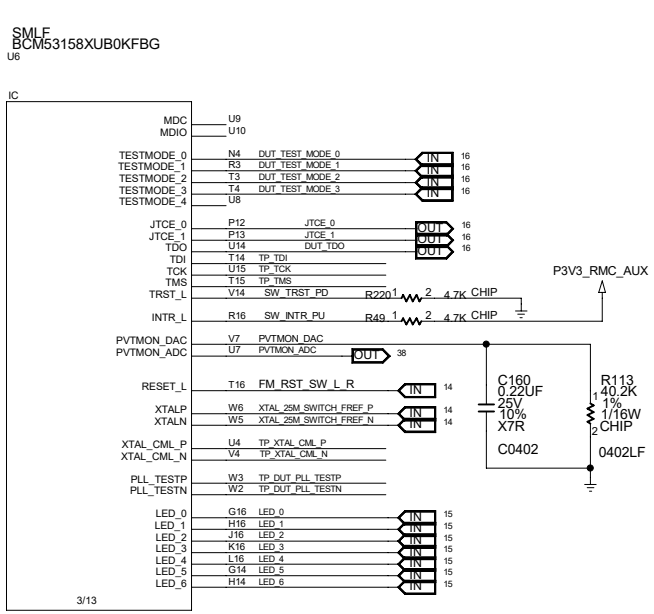
BCM53158 RGMII

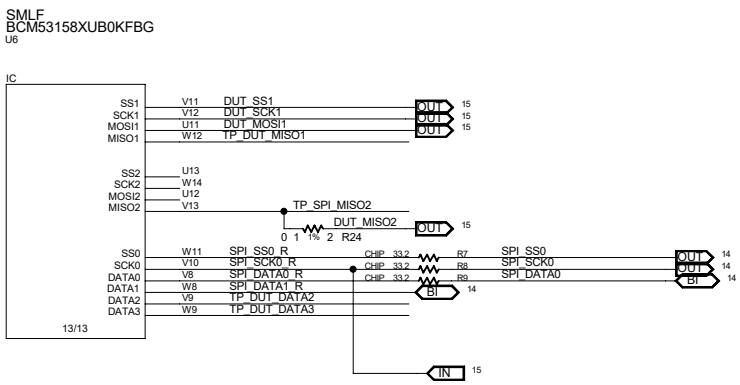
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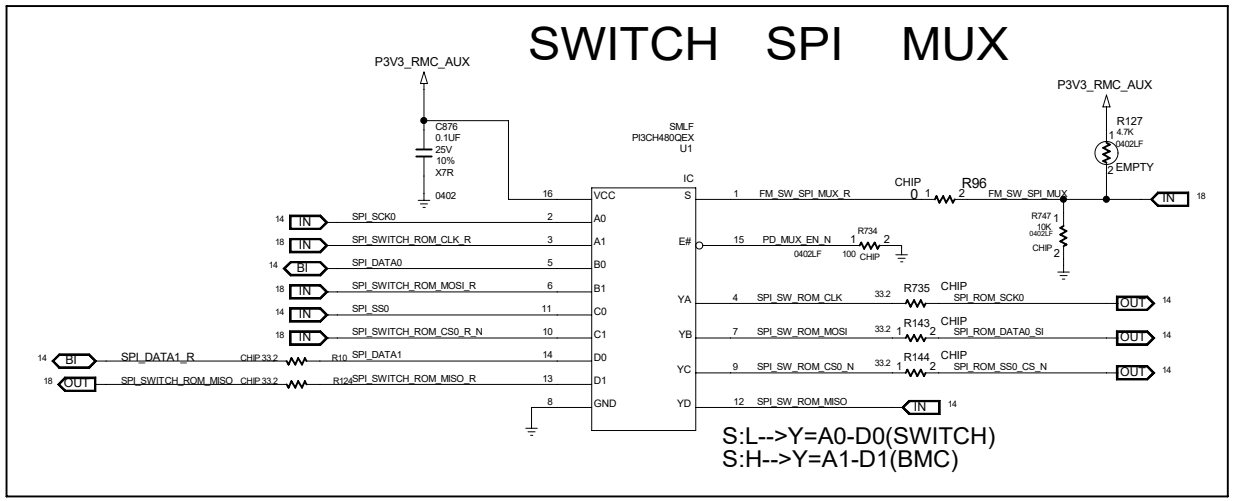


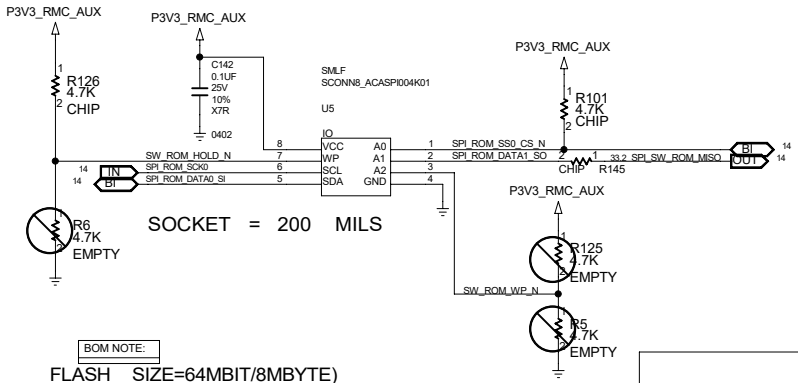
BCM53158 PHY

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:04:16 2018	REV: 1.15
				SHEET: 13 OF 41



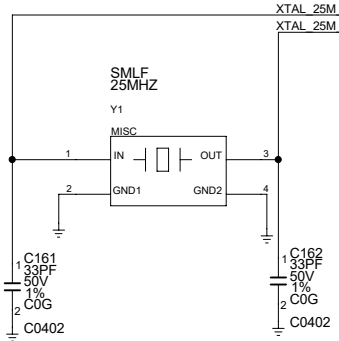




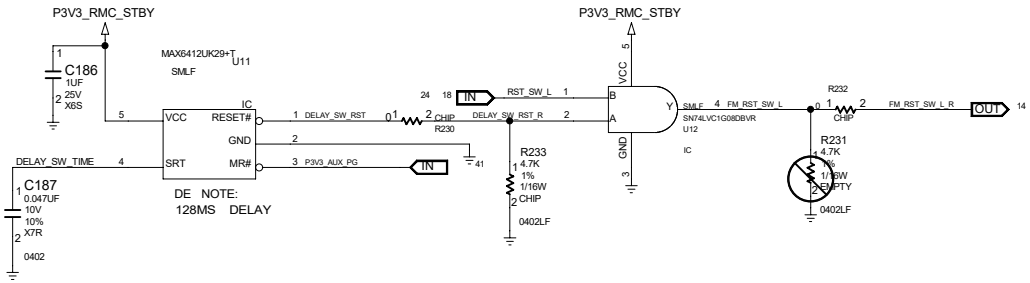


BOM NOTE:

FLASH SIZE=64MBIT/8MBYTE)
BMC FLASH 8-SOP
P/N:AKE3EFZ0Z00 (MX25L6433FM2I-08G)

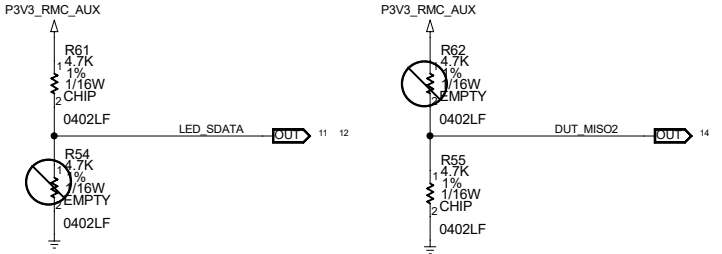


CHANGE BOM
CH0336J0B08



BCM53158 FLASH

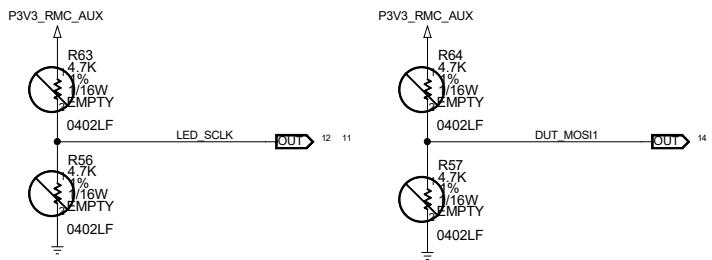
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	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:04:22 2018		SHEET 14 OF 41



DESIGN NOTE:

TO SET THE BOOT SOURCE, USE THE VALUES BELOW:
(:FLOATING)

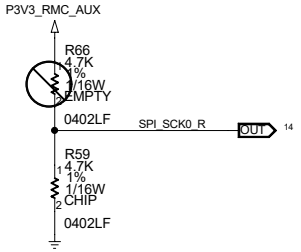
2'B00 8051 ROM BOOT
2'B01 8051 BOOT FROM FLASH (STARTS WITH ROM;JUMPS TO FLASH)
2'B10 M7 BOOT FROM FLASH
2'B11 BOOT M7 FROM INTERNAL MEMORY



DESIGN NOTE:

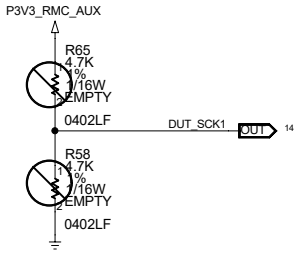
CASCADING_CONFIG[1:0]TO BELOW OPERATION MODE
(:FLOATING)

2'B00 AVR STANDALONE;HARDWARE FORWARDING(UNMANAGED)
2'B01 AVR CASCADING ENABLED;PRIMARY
2'B10 AVR CASCADING ENABLED;SECONDARY
2'B11 AVR STANDALONE;NO HARDWARE FORWARDING



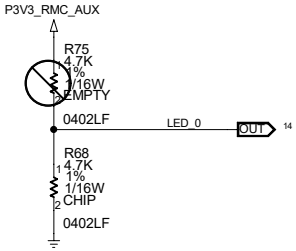
FOR IMP PORT VOLTAGE SELECTION.

0(PD) IMP PORT WORKS AT 3.3V
1(PU) IMP PORT WORKS AT V



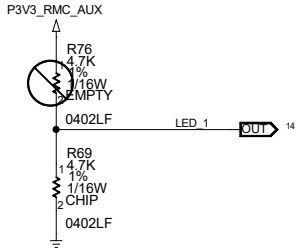
FOR EN_EEE(ENERGY EFFICIENT ETHERNET)

0(PD) DISABLE EEE FEATURE FOR SWITCH MAC
1(PU) ENABLE EEE FEATURE FOR SWITCH MAC(DEFAULT)



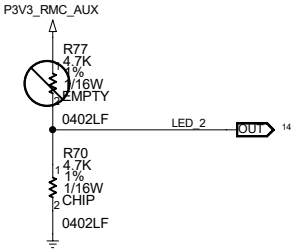
FOR XTAL BYPASS CONFIGURATION

1(PU) EXTERNAL CLOCK IS DRIVEN IN XTAL PADS
0(PD) CRYSTAL IS PRESENT ON BOARD TO DRIVE THE XTAL PADS
THIS STRAP GOES TO I_BYPASS PIN OF XTAL IP.



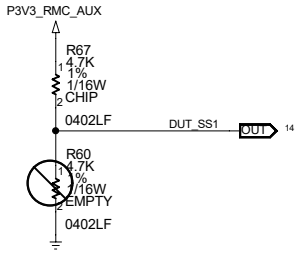
FOR ATE TIME CONFIGURATION

1(PU) ENABLES FIXED ATE TIME.
0(PD) DISABLES FIXED ATE TIME.



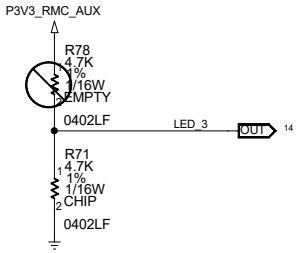
FOR XTAL FREQUENCY SELECTION.

1(PU) 50 MHZ XTAL CLOCK
0(PD) 25 MHZ XTAL CLOCK



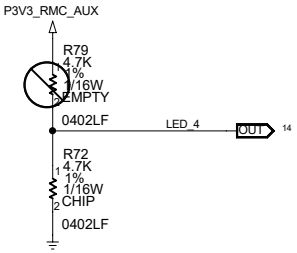
FOR CM7DAP OPERATION.

1(PU) CM7DAP IS IN JTAG MODE
0(PD) CM7DAP IS IN SW MODE



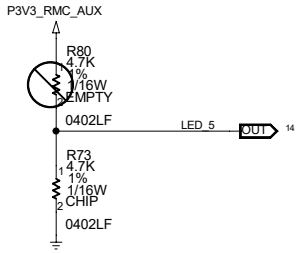
FOR QSPI SELECTION.

1(PU) RESERVED
0(PD) QSPI IS CONNECTED OR NO CONNECTION IN SPI0



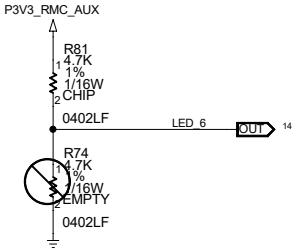
MDIO VOLTAGE SELECTION.

0(PD) 3.3V MODE MDIO
1(PU) 1.2V MODE MDIO



FOR BISR OPERATION
0(PD) BISR IS RUN AT POWER UP

1(PU) BYPASSES BISR OPERATION AT POWER-UP
0(PD) BISR IS RUN AT POWER UP



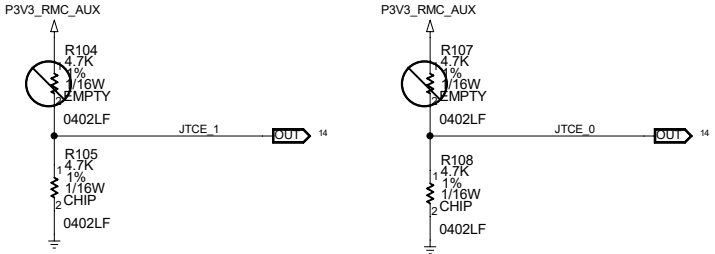
FOR MDIO MODE SELECTION.

1(PU) AVENGER IS MDIO MASTER
0(PD) AVENGER IS MDIO SLAVE

Strap Pin and Test Mode (1/2)

NOKIA

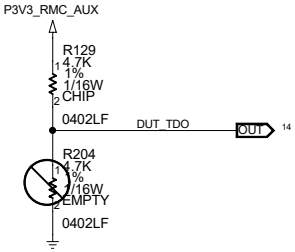
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:04:30 2018		SHEET 15 OF 41



DESIGN NOTE:

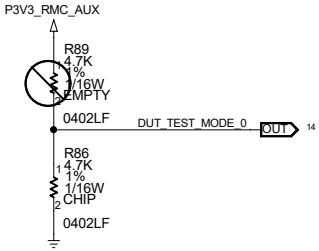
SELECT AS SHOWN BELOW:
(00:DFT LVTAP)

2B'00 DFT LVTAP
2B'01 AVS
2B'10 8051 DEBUG
2B'11 M7 DAP



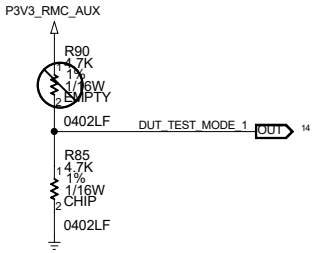
FOR IMP PORT VOLTAGE SELECTION.
1(PU):ENABLED

0(PD) = DISABLED
1(PU) = ENABLED



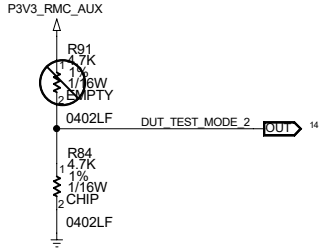
TEST MODE CONTROL BIT 0
0(PD):

0(PD) =
1(PU) =



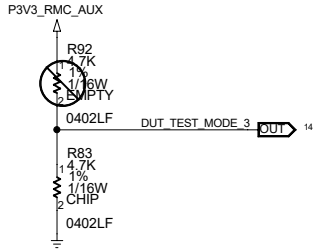
TEST MODE CONTROL BIT 1
0(PD):

0(PD) =
1(PU) =



TEST MODE CONTROL BIT 2
0(PD):

0(PD) =
1(PU) =

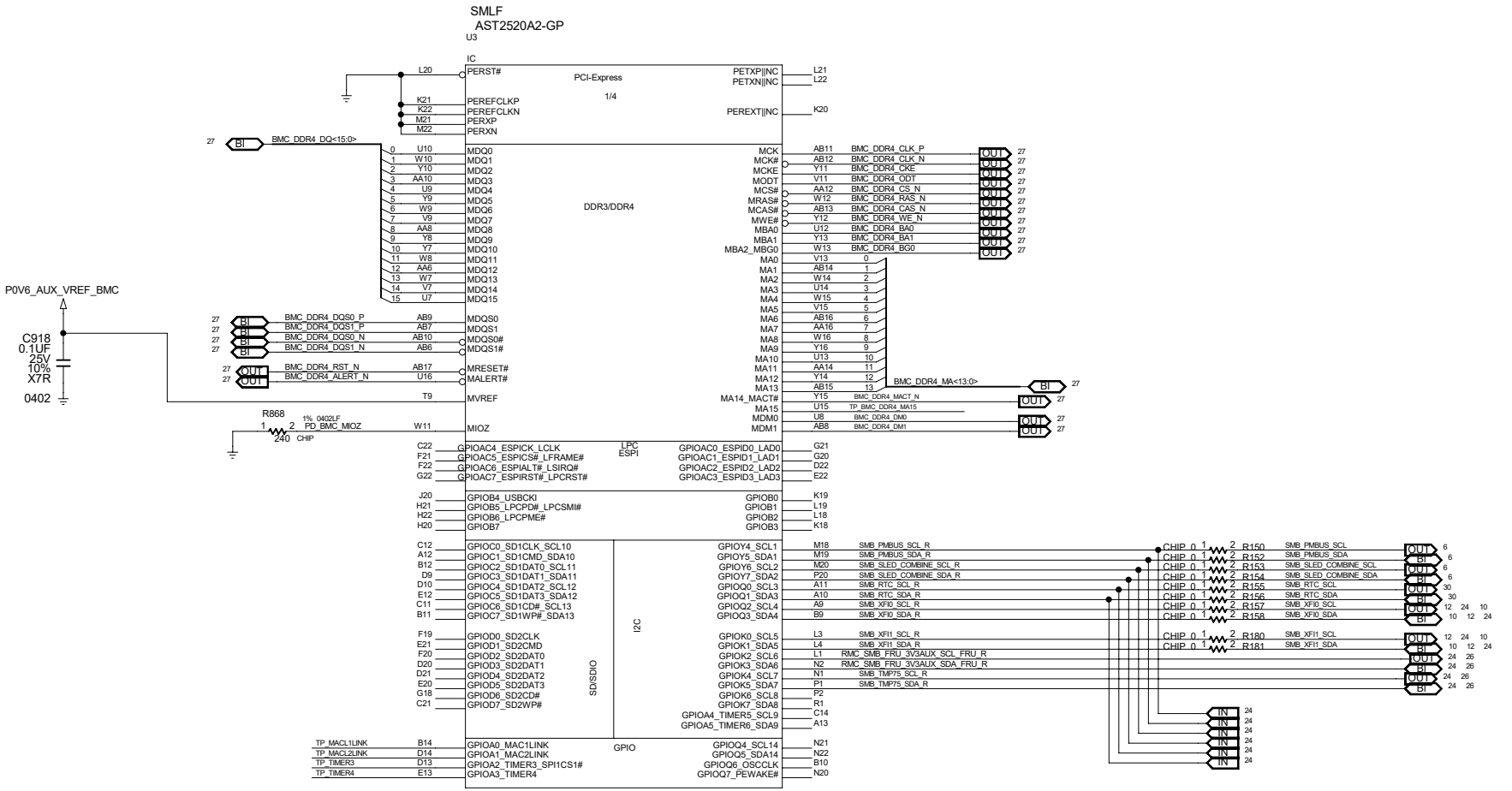


TEST MODE CONTROL BIT 3
0(PD):

0(PD) =
1(PU) =

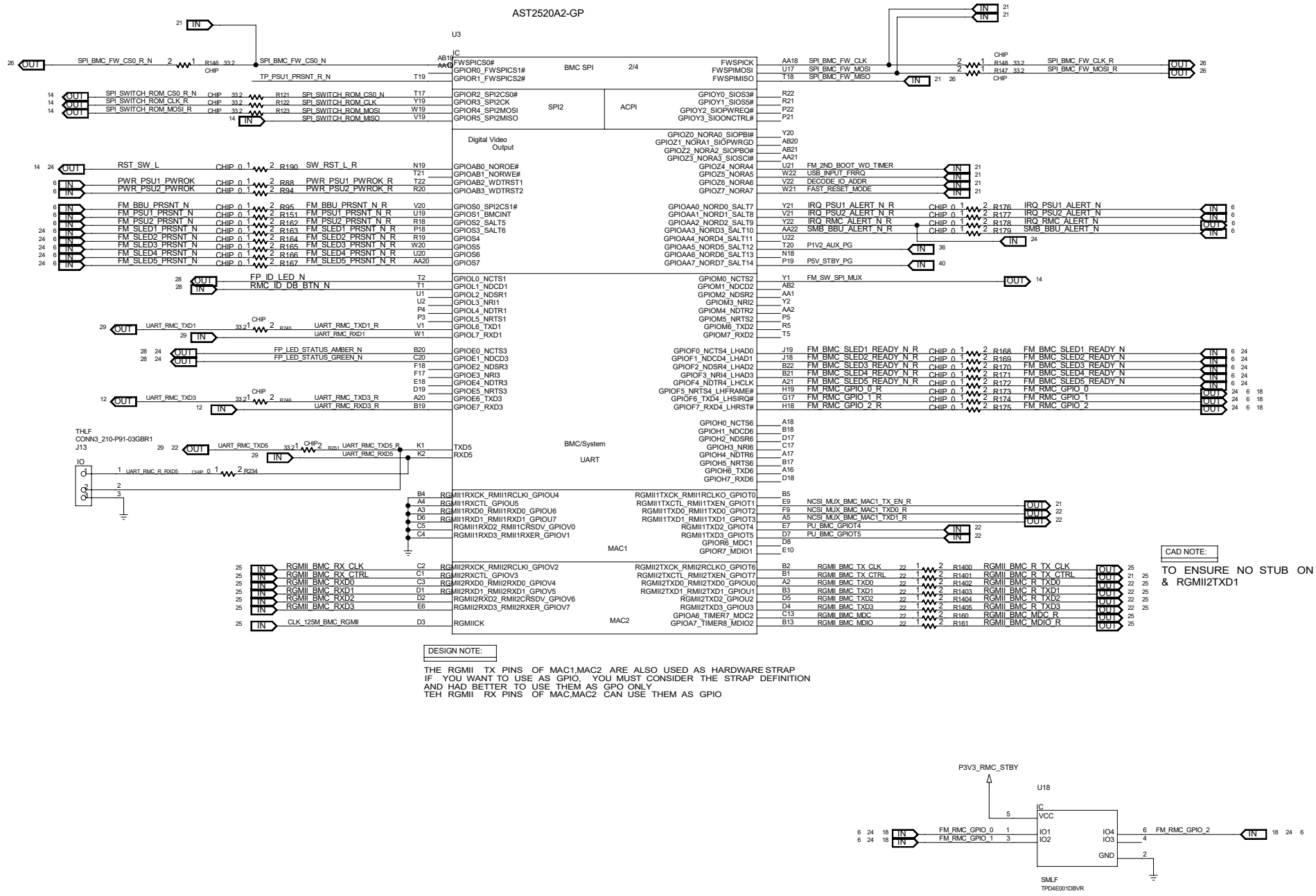
Strap Pin and Test Mode (2/2)

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A / REV: 1.15
		REVIEWER	SIZE: C / DATE: Wed Nov 21 14:05:28 2018	SHEET: 16 OF 41



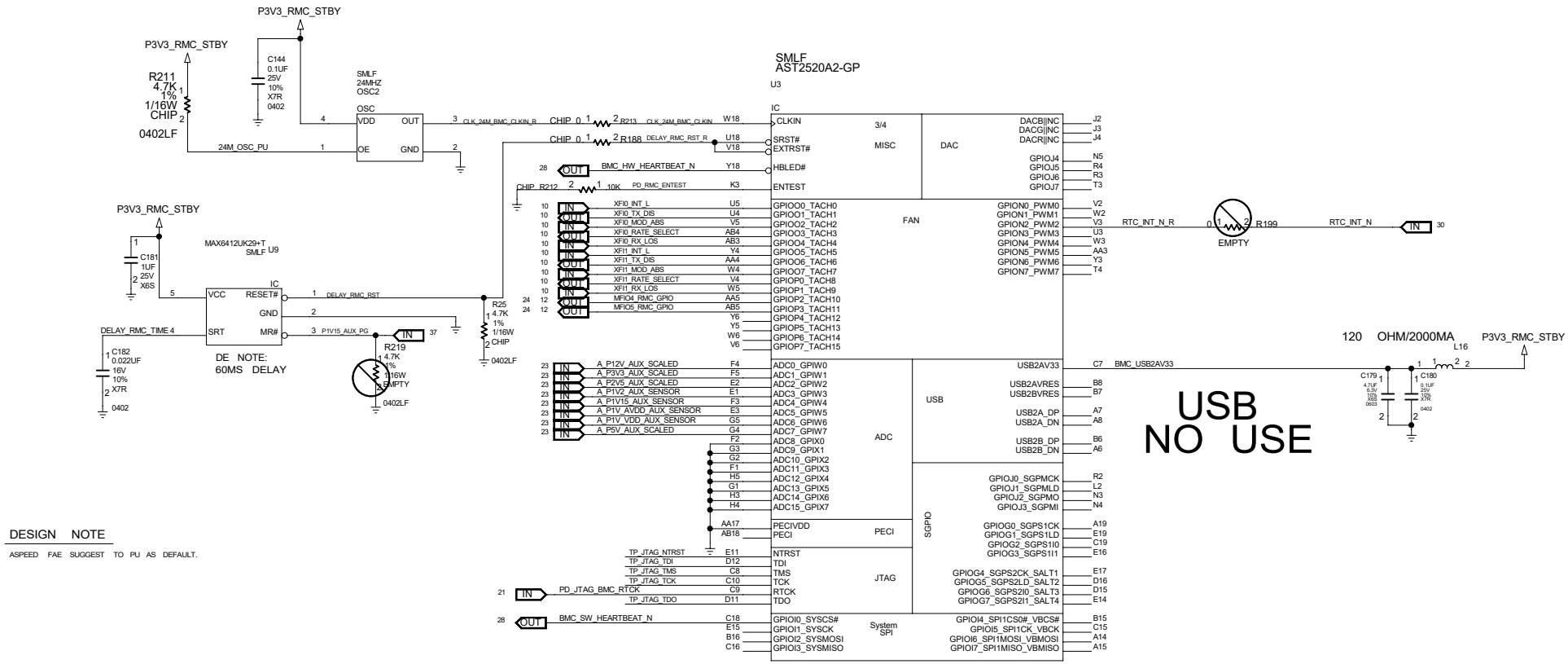
BMC:AST2520 1/4

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:05:44 2018	REV: 1.15
				SHEET: 17 OF 41



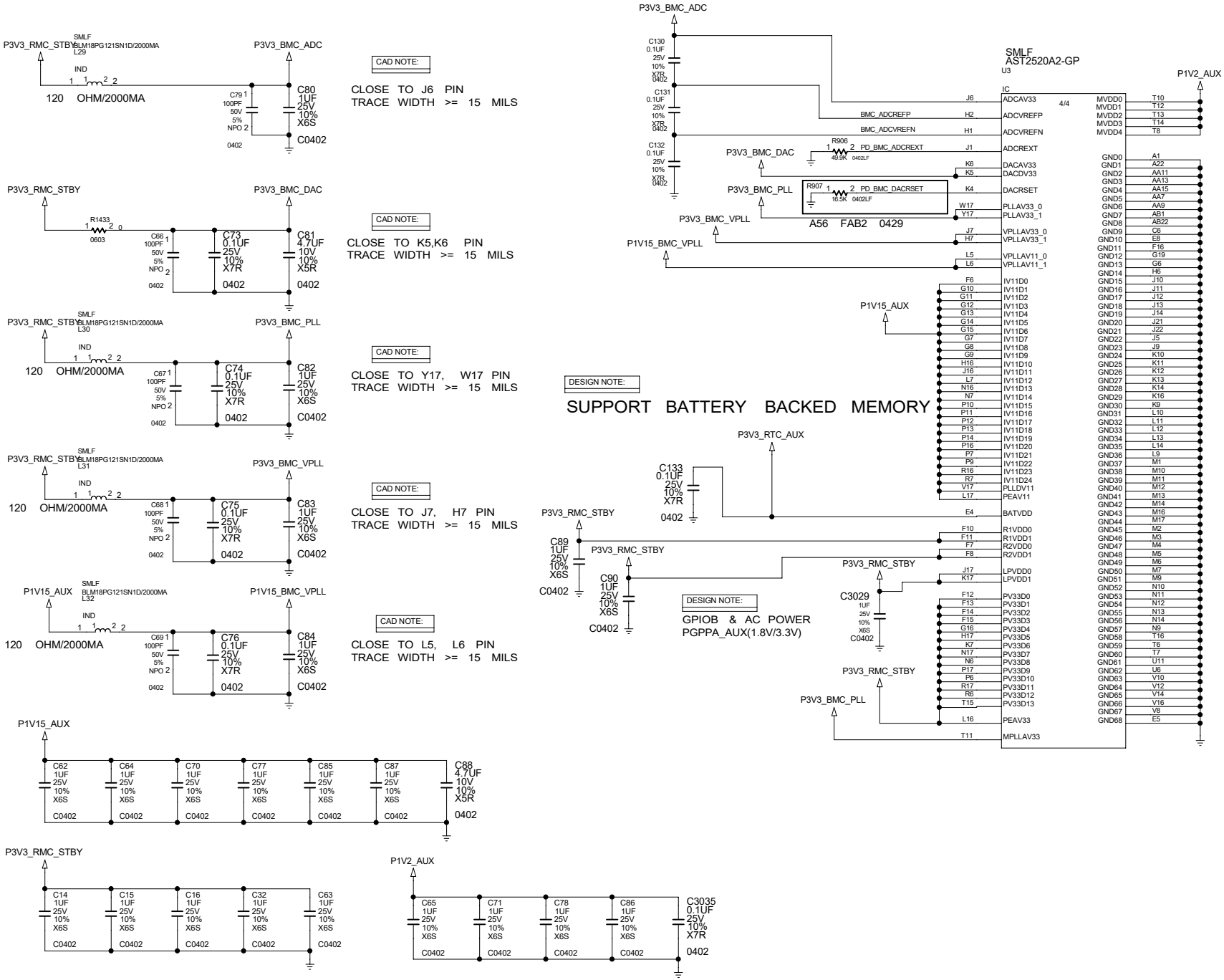
BMC:AST2520 2/4

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC
		REVIEWER	DOCUMENT NUMBER: N/A
			REV: 1.15
	SIZE: C	DATE: Wed Nov 21 14:12:19 2018	SHEET: 18 OF 41



BMC:AST2520 3/4

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:06:29 2018		SHEET 19 OF 41



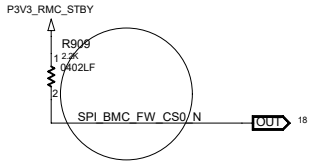
BMC:AST2520 4/4

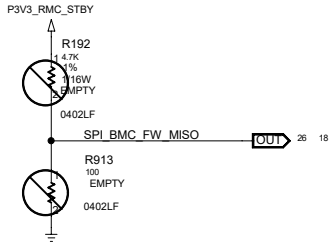
NOKIA

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:06:54 2018		SHEET 20 OF 41

DESIGN NOTE:

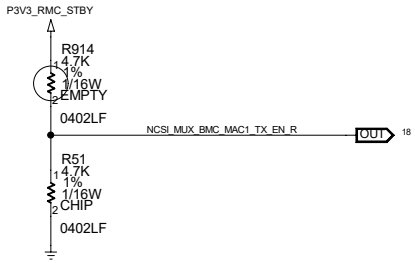
ENABLE CPU RUNNING(0:PU:2.2K OHM)
0: ENABLE BOOT
1: DISABLE CPU OPERATION, WHEN NO FIRMWARE EXIST





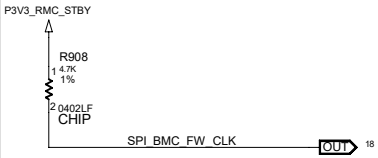
DESIGN NOTE:

ENABEL ESPI BUS(1:PU)
0(FLOATING): LPC MODE
1(PU):ESPI MODE



DESIGN NOTE:

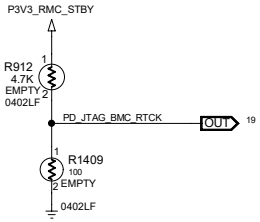
DEFINE MAC#1 INTERFACE TYPE(0:PD)
0(PD):RMII/NCSI
1(PU):RGMII



DESIGN NOTE:

ENABLE GPIO STRAP MODE(STEP 2)(1:PU AS DEFAULT)
0(FLOATING):DISABLE
1(PU):ENABLE

AP NOTE : A2500-03



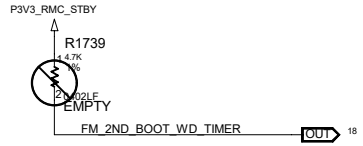
DESIGN NOTE:

ENABLE ESPI FLASH MODE(0:FLOATING)
0(FLOATING): ESPI RESPOND WITH NO FLASH ATTACHED
1(PU): ESPI RESPOND WITH FLASH ATTACHED
THIS BIT IS VALID ONLY WHEN ESPI IS ENABLED



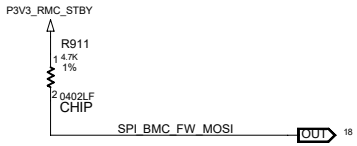
DESIGN NOTE:

DEFINE MAC#2 INTERFACE TYPE(1:PU)
0(FLOATING):RMII/NCSI
1(PU):RGMII



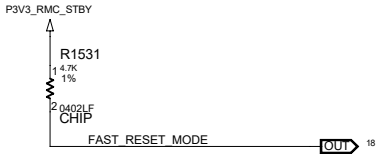
DESIGN NOTE:

ENABLE BMC 2ND BOOT WATCHDOG TIMER
(0:FLOATING)
0(FLOATING):DISABLE
1(PU):ENABLE BMC 2ND BOOT WATCHDOGTIMER.
START COUNTING AT POWER UP.



DESIGN NOTE:

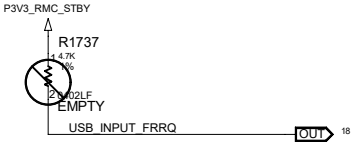
ENABLE SPI FLASH STRAP AUTO FETCH MODE(STEP3)
1(PU):ENABLE
0(FLOATING):DISABLE
1(PU):ENABLE



DESIGN NOTE:

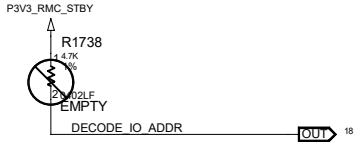
ENABLE FAST RESET MODE (1:PU AS DEFAULT)
0(FLOATING):LONG RESET MODE
1(PU):FAST RESET MODE

AP NOTE : A2500-03



DESIGN NOTE:

SELECT USBCKI INPUT FRRQ.
(0:FLOATING)
0(FLOATING):24 MHZ
1(PU):48 MHZ



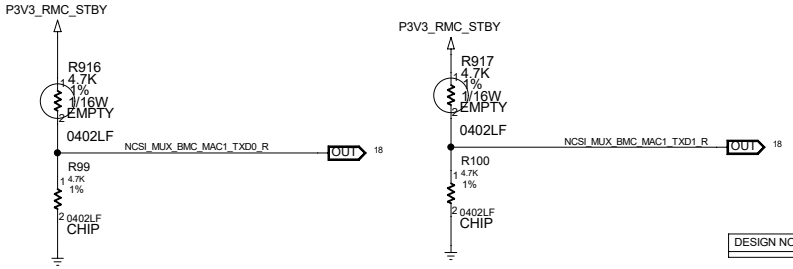
DESIGN NOTE:

DISABLE LPC TO DECODE SUPERIO 0X2E/0X4E ADDRESS
(0:FLOATING)
0(FLOATING):ENABLE ADDRESS DECODING
1(PU):DISABLE ADDRESS DECODING

BMC HW STRAPPING(DEDICATED) 1/2

NOKIA

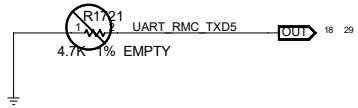
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:07:33 2018		SHEET 21 OF 41



DESIGN NOTE:

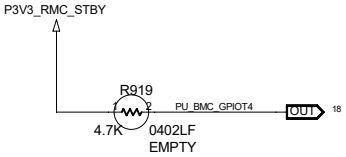
SPI1 INTERFACE MODE SELECTION [1:0](00:FLOAITNG)
00: DISABLE SPI INTERFACE
01: ENABLE SPI MASTER
10: ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11: ENABLE SPI PASS-THROUGH

0:PD
1:PU



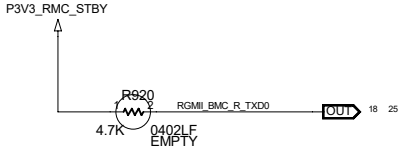
DESIGN NOTE:

SELECT UART DEBUG PORT(1)
(1:FLOATING)
0(PD):SELECT UART1 AS BMC CONSOLE PORT
1(FLOATING):SELECT UART5 AS BMC CONSOLE PORT



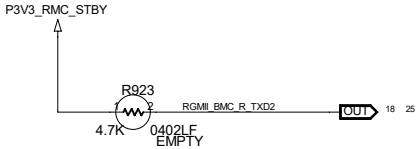
DESIGN NOTE:

SUPER IO CONFIGURATION ADDRESS SELECTION(0:FLOATING)
0(FLOATING):DECODE 0X2E
1(PU):DECODE 0X4E



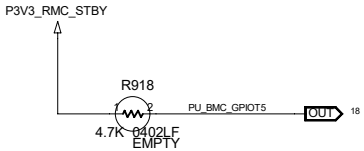
DESIGN NOTE:

ENABLE GPIOD PASS-THROUGH MODE(0:FLOATING)
0(FLOATING):DISABLE, PASS THROUGH CAN BE ENABLED BY SCU8C[11:8]
1(PU):ENABLE PASS-THROUGH AT POWER ON PASS-THROUGH PINS SET:



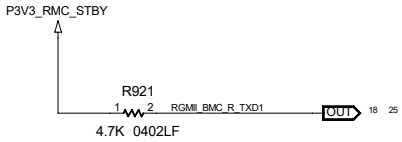
DESIGN NOTE:

SELECT 25MHZ REFERENCE CLOCK INPUT MODE(0:FLOATING)
0(FLOATING): CLKIN IS 24 MHZ AND USBCK NOT USED
1(PU): CLKIN IS 25MHZ AND USBCKI =24/48 MHZ(DETERMINED BY BIT[18]



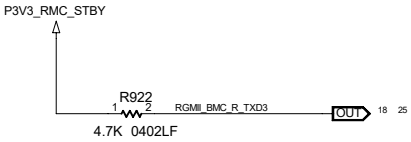
DESIGN NOTE:

ENABLE ACPI FUNCTION(0:FLOATING)
0(FLOAITNG):DISABLE ACPI
1(PU):ENABLE ACPI



DESIGN NOTE:

ENABLE GPIOE PASS-THROUGH MODE(1:PU)
0(FLOATING): DISABLE, PASS THROUGH CAN BE ENABLED BY SCU8C[15:12]
1(PU):ENABLE PASS-THROUGH AT POWER ON

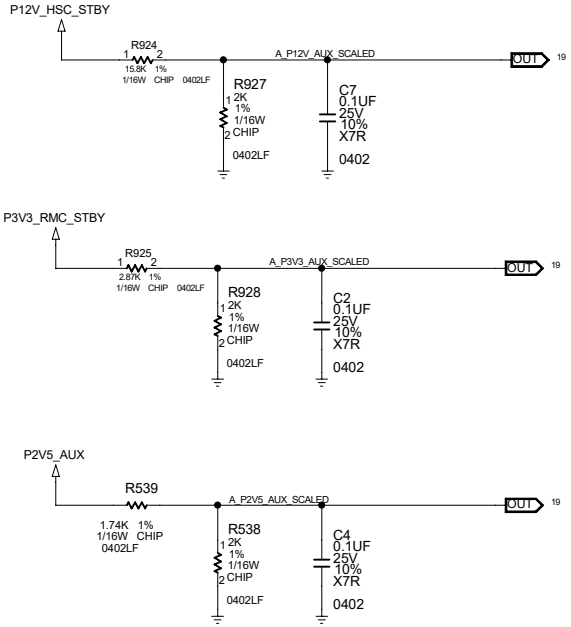


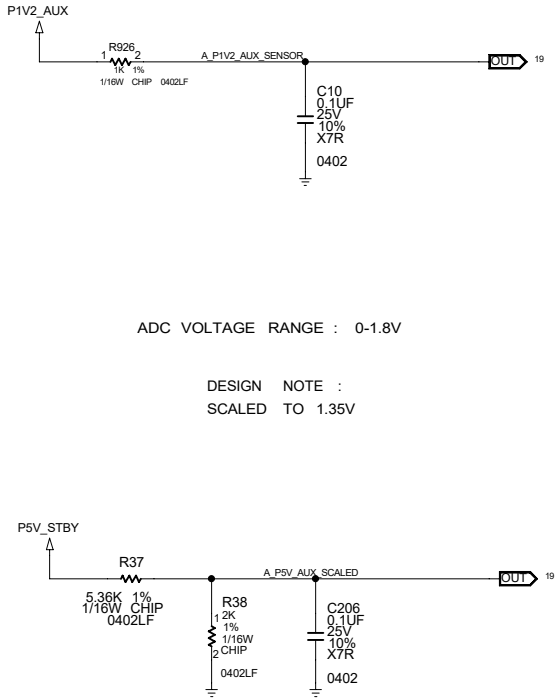
DESIGN NOTE:

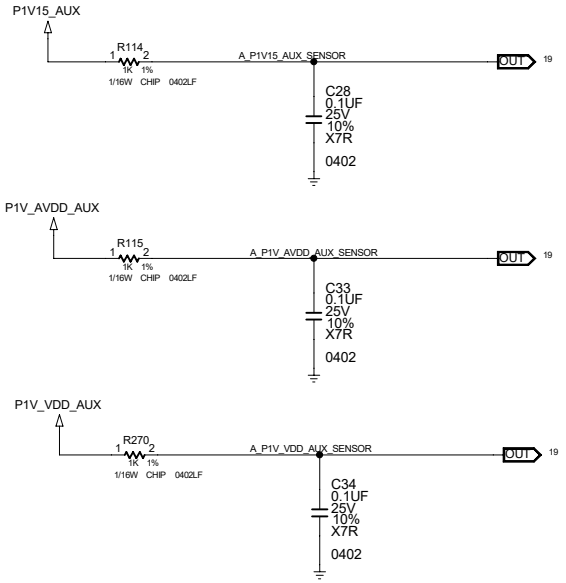
SELECT DDR4 SDRAM(1:PU)
0(FLOATING): DDR3 SDRAM
1(PU): DDR4 SDRAM

BMC HW STRAPPING(DEDICATED) 2/2

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A / REV: 1.15
		REVIEWER	SIZE: C / DATE: Wed Nov 21 14:07:43 2018	SHEET: 22 OF 41







ADC VOLTAGE RANGE : 0-1.8V

DESIGN NOTE :
SCALED TO 1.35V

CAD NOTE:

ROUTE ALL ADC NETS AT 6 MILS WIDE

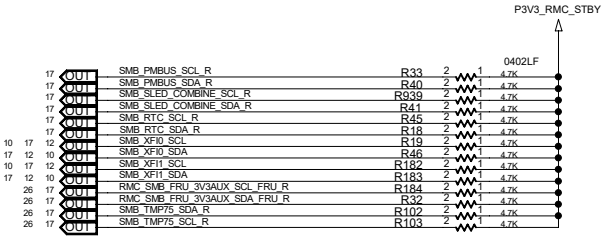
DESIGN NOTE:

ADC INPUT VOLTAGE RANGE:0~1.8V
1.35V IS PREFFERD

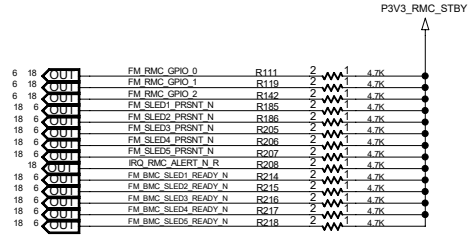
BMC VOLTAGE SENSOR

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:07:56 2018	REV: 1.15
				SHEET: 23 OF 41

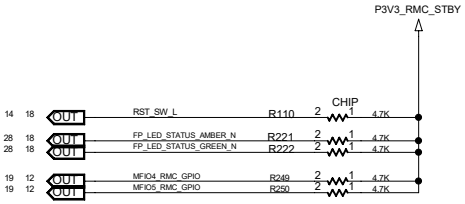
RMC I2C PU



TO AIRMAX GPIO PU

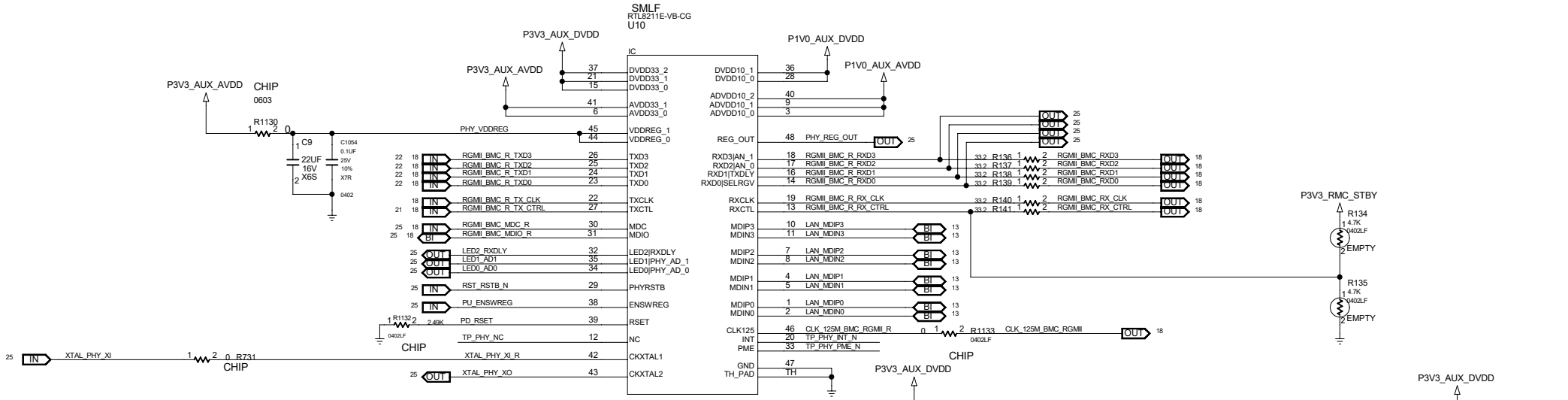


RMC GPIO PU

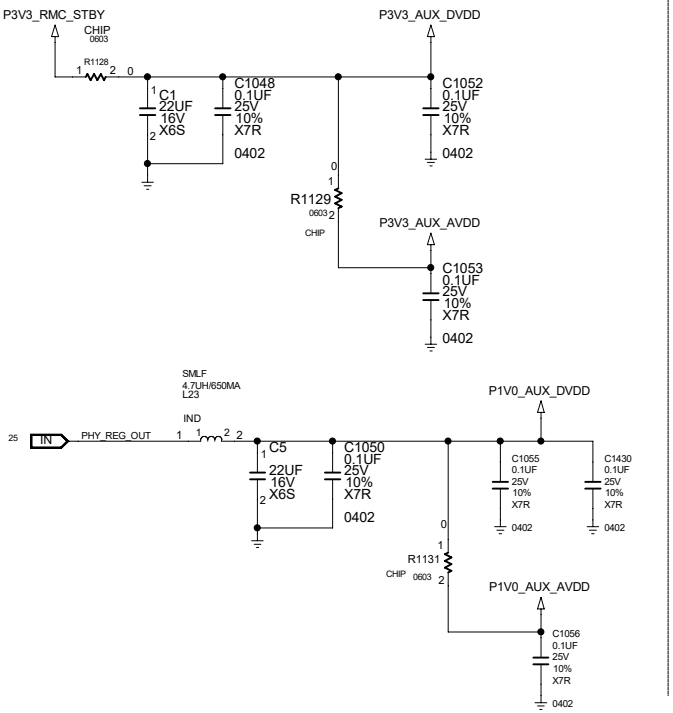


BMC PU & PD

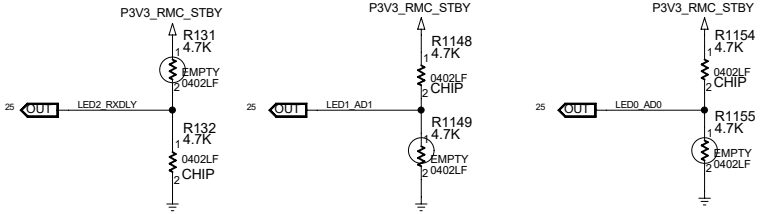
NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A / REV: 1.15
		REVIEWER	SIZE: C / DATE: Wed Nov 21 14:08:07 2018	SHEET: 24 OF 41



POWER RAIL DECOUPLING



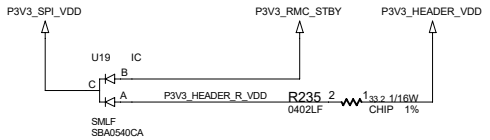
LED & PHY ADDRESS CONFIG

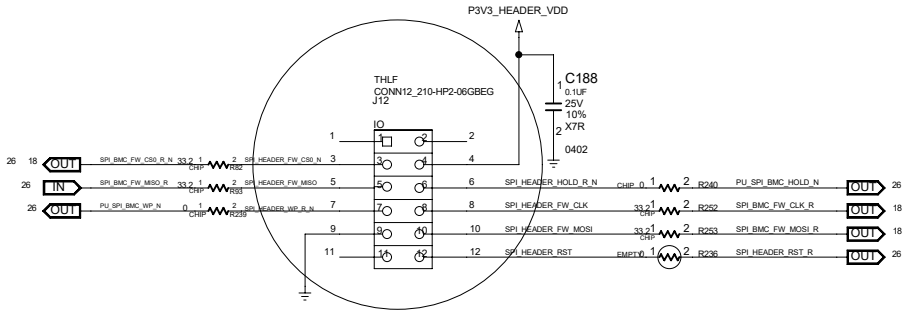


BMC MANAGEMENT PORT-RTL8211E

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:08:19 2018	REV: 1.15
				SHEET: 25 OF 41

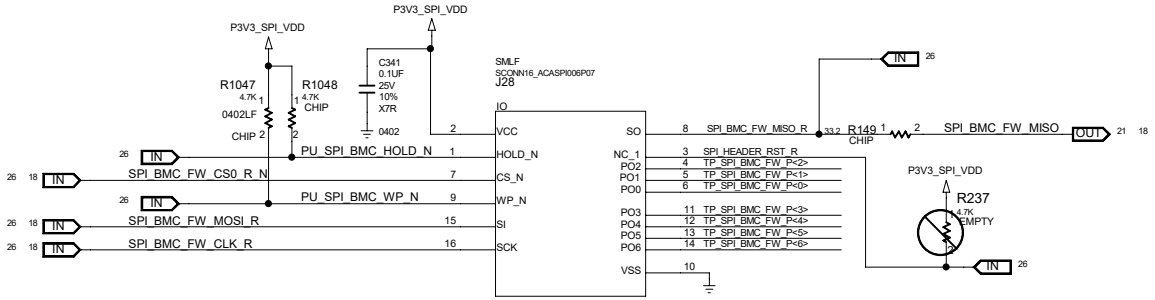
RECOVERY HEADER





1	Vpp	CS2	2
3	CS1	Vcc	4
5	MISO/DQ1	Hold/DQ3	6
7	Wp/DQ2	CLK	8
9	GND	MOSI/DQ0	10
11	NC	Reset	12

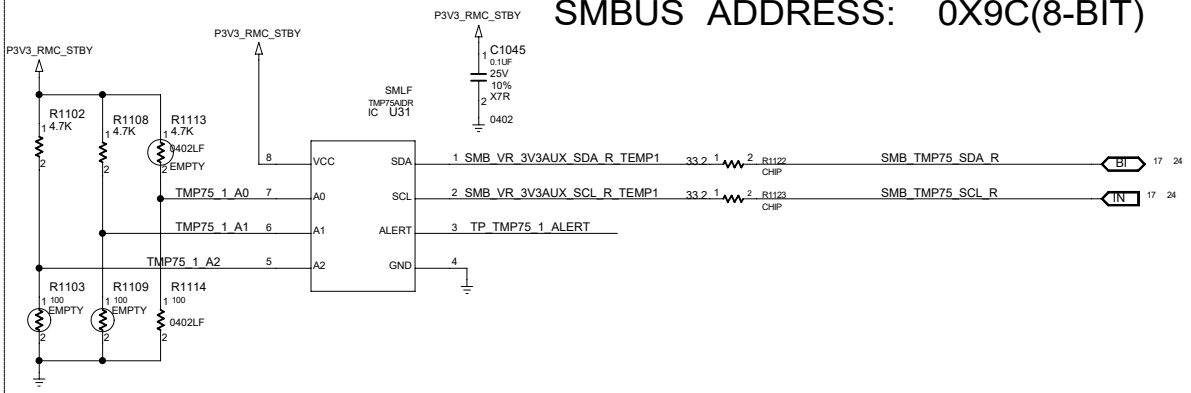
BMC FIRMWARE



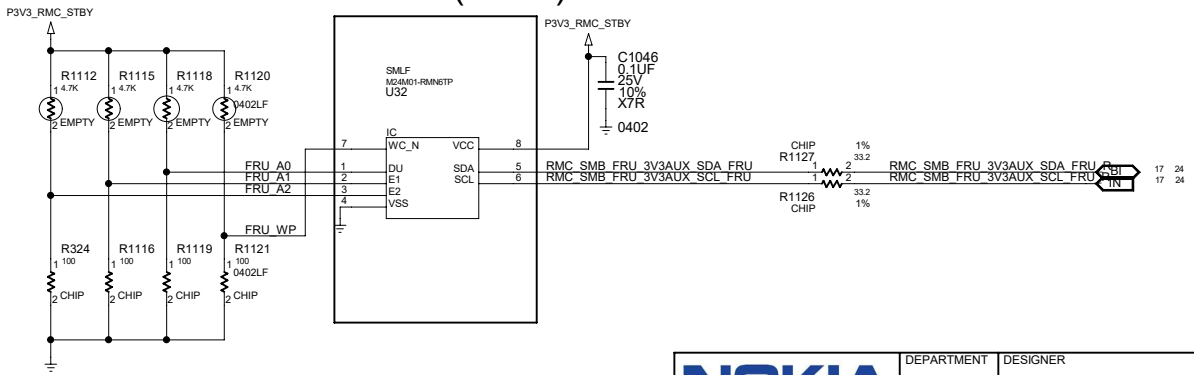
BOM NOTE:

FLASH SIZE=1GBIT/128MBYTE)
BMC FLASH SOIC16
P/N:AKE3LF-0Z00 (MX66L1G45GMI-08G)

THERMAL SENSOR
SMBUS ADDRESS: 0X9C(8-BIT)

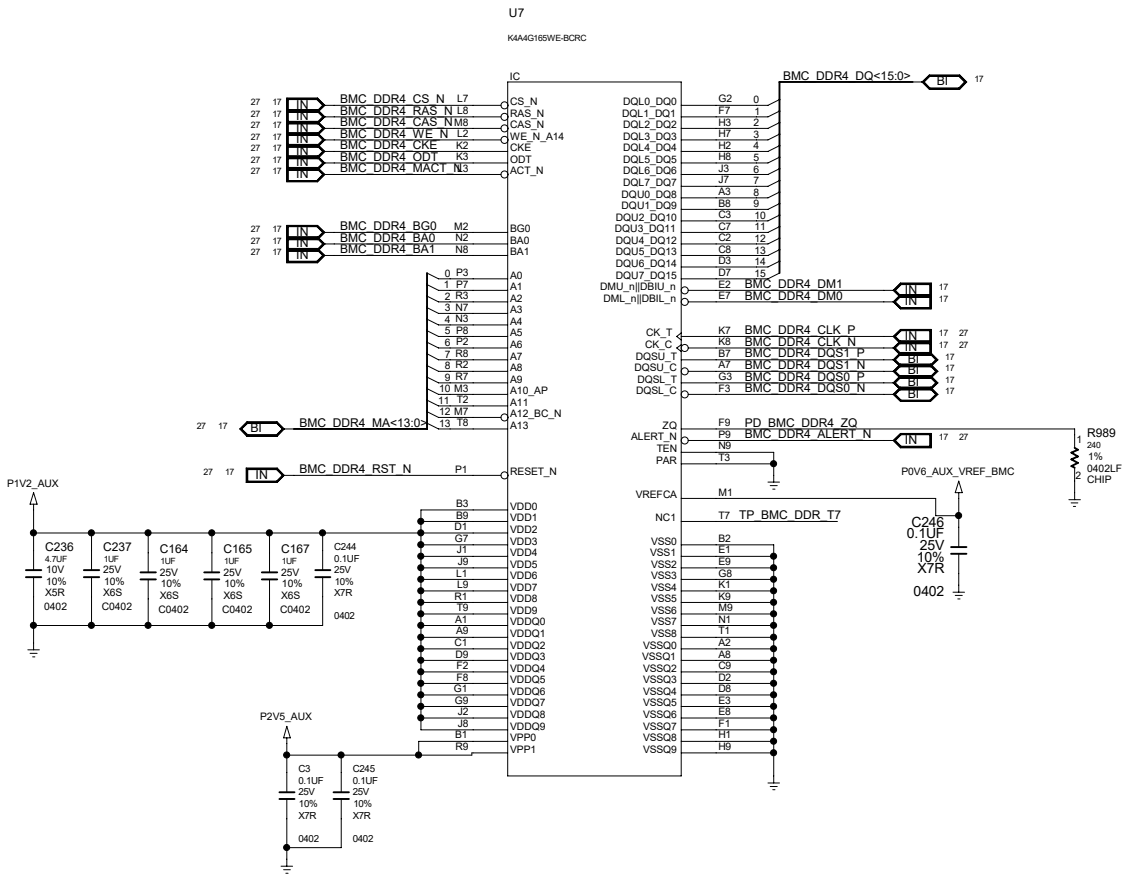


BASEBOARD FRU EEPROM
SMBUS ADDRESS: 0XA0/0XA2(8-BIT)

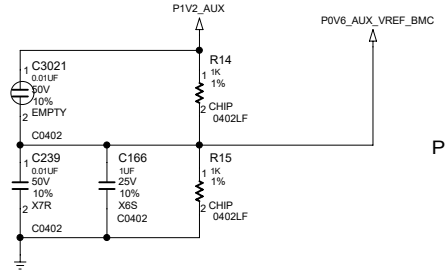


BMC FLASH ROM& THERMAL SENSOR

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A	REV: 1.15
		REVIEWER	SIZE: C	DATE: Wed Nov 21 14:27:23 2018	SHEET: 26 OF 41

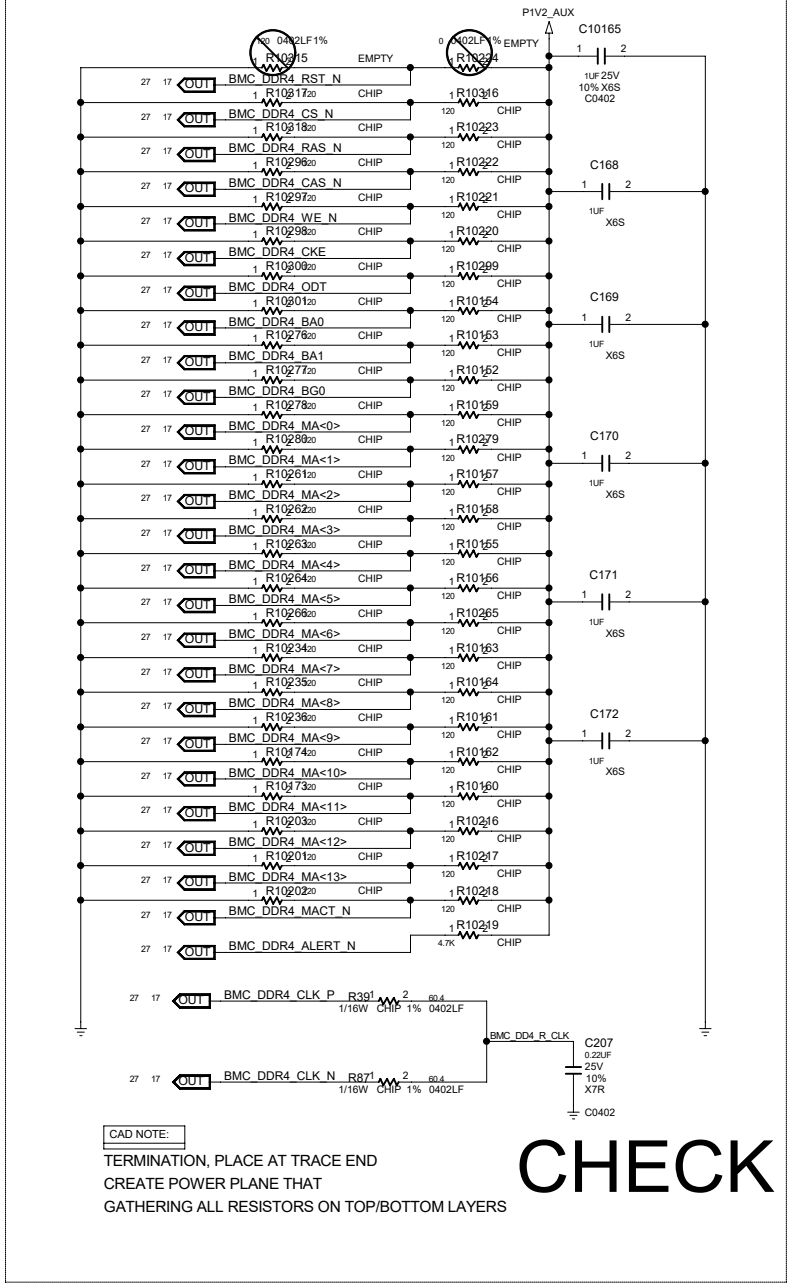


P1V2_AUX DIVIDE TO P0V6_AUX_VREF_BMC



CAD NOTE:

P0V6_AUX_REF_BMC TRACE WIDTH >= 15 MILS



CAD NOTE:

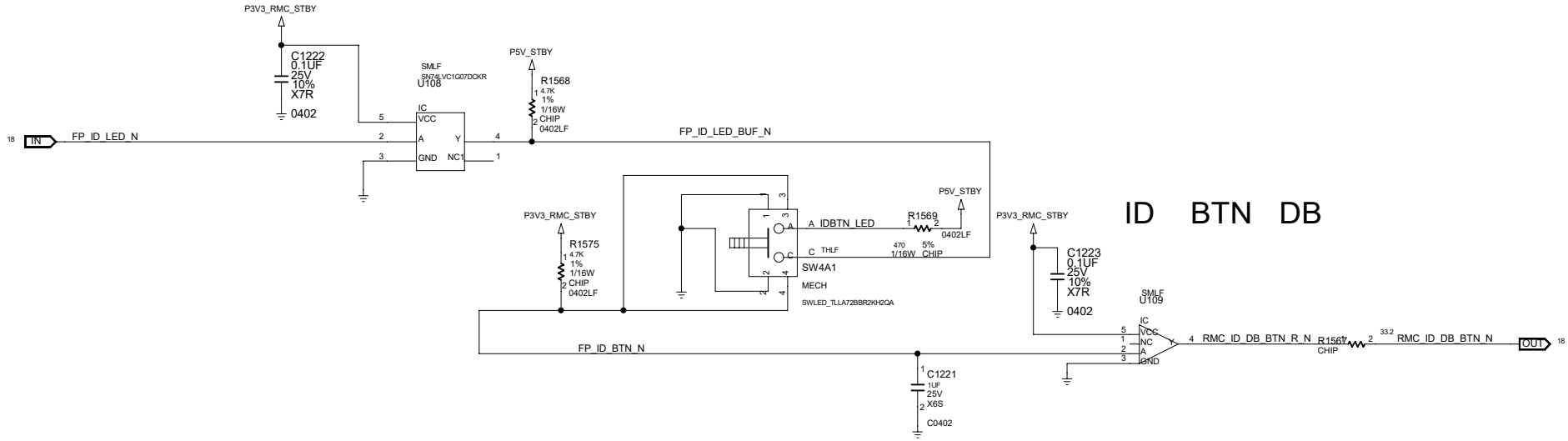
TERMINATION, PLACE AT TRACE END
CREATE POWER PLANE THAT
GATHERING ALL RESISTORS ON TOP/BOTTOM LAYERS

CHECK

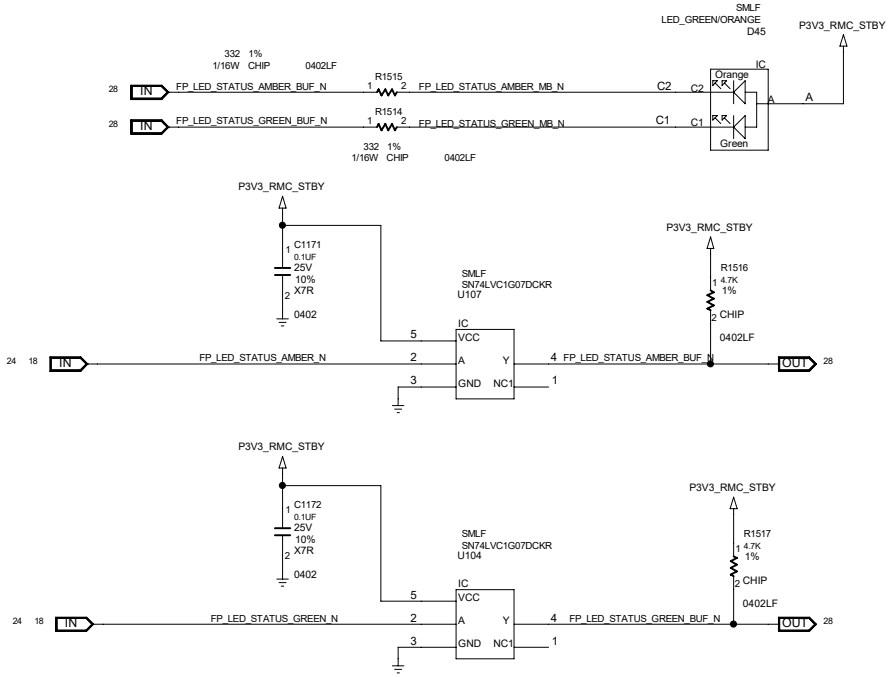
BMC MEM DDR4

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	REVIEWER	OPEN EDGE RMC	N/A	1.15
		SIZE C DATE Wed Nov 21 14:08:41 2018		SHEET 27 OF 41

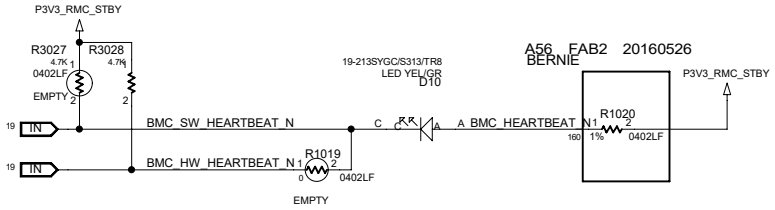
FP ID LED BUFFER



BMC STATUS LED



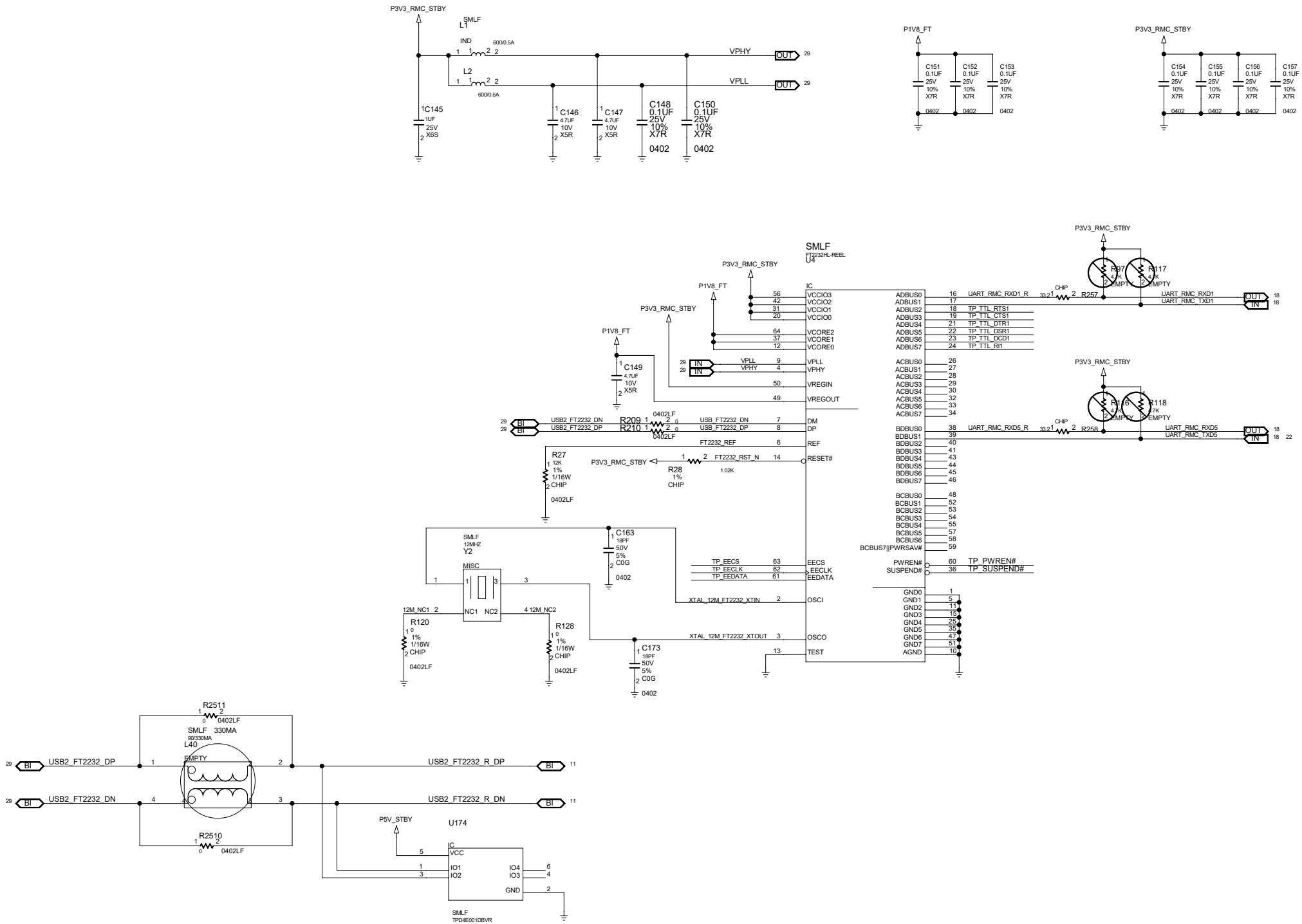
BMC HEARTBEAT LED



COLOR:YELLOW GREEN

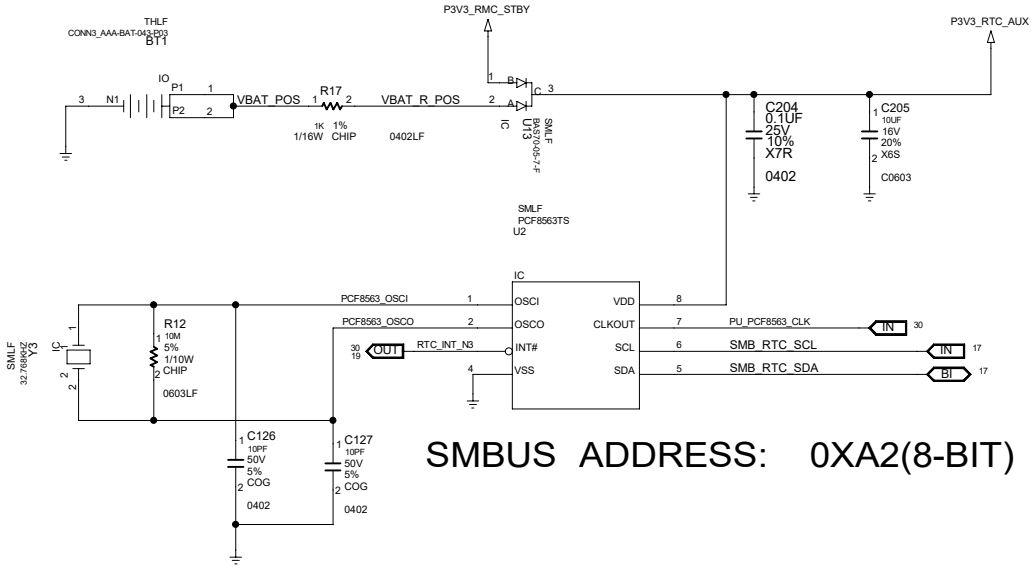
ID BTN & DEBUG LED

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:08:51 2018	REV: 1.15
				SHEET: 28 OF 41

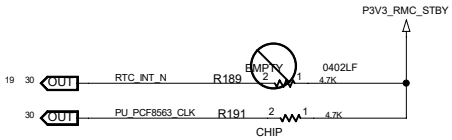


FT2232

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A / REV: 1.15
		REVIEWER	SIZE: C / DATE: Wed Nov 21 14:09:03 2018	SHEET: 29 OF 41



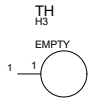
SMBUS ADDRESS: 0XA2(8-BIT)

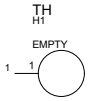


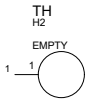
RTC

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A	REV: 1.15
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:09:17 2018	SHEET: 30 OF 41	

FBF06263010 * 1PC
NODE PDB THUMB SCW S2P(FBS2P096,3D)BLUE

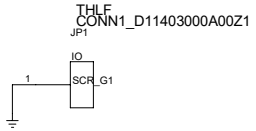




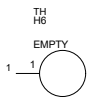




GUIDE



SWITCH HEATSINK HOLE



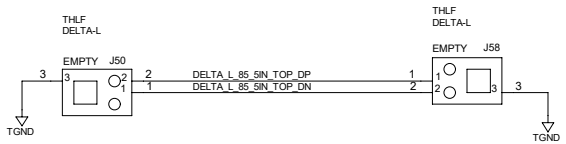


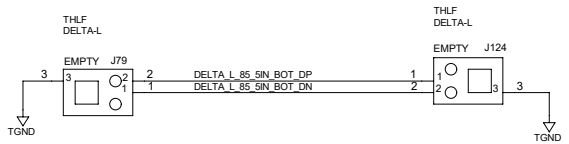
SCREW HOLE

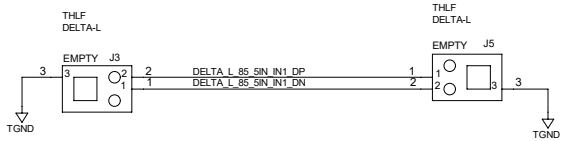
NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:09:29 2018	REV: 1.15
				SHEET: 31 OF 41

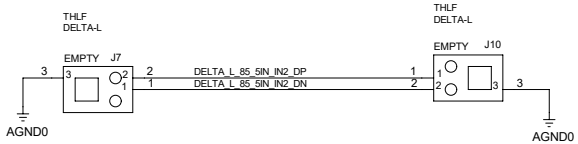
DELTA-L

5 INCH

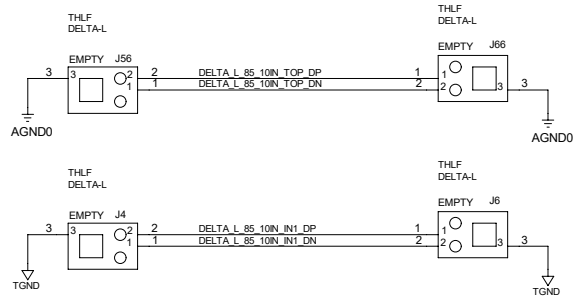


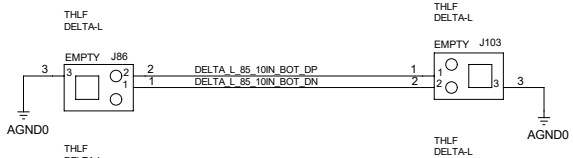


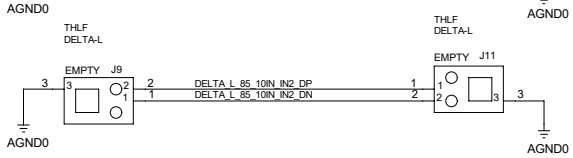




10 INCH



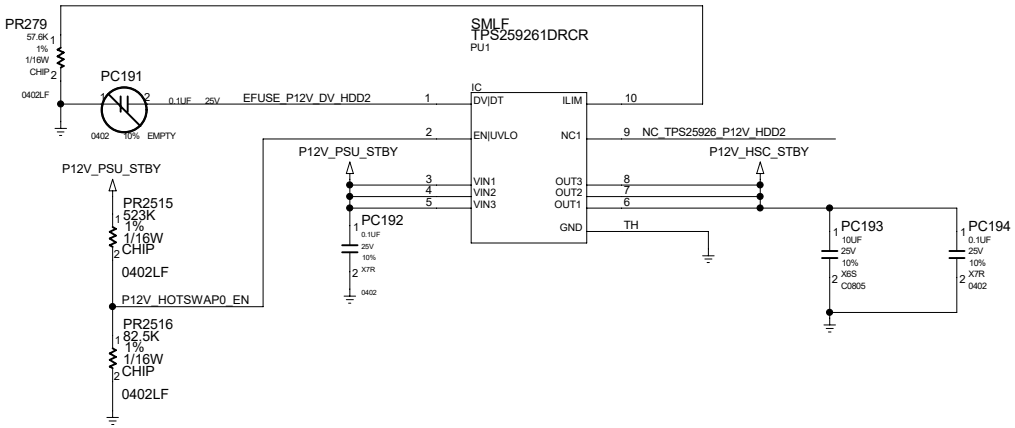




COUPON-DELTA-L

NOKIA	DEPARTMENT BU9	DESIGNER NAME	PROJCET OPEN EDGE RMC	DOCUMENT NUMBER N/A	REV 1.15
		REVIEWER NAME	SIZE C	DATE Wed Nov 21 14:10:04 2018	SHEET 32 OF 41

HOT SWAP
P12V_STBY

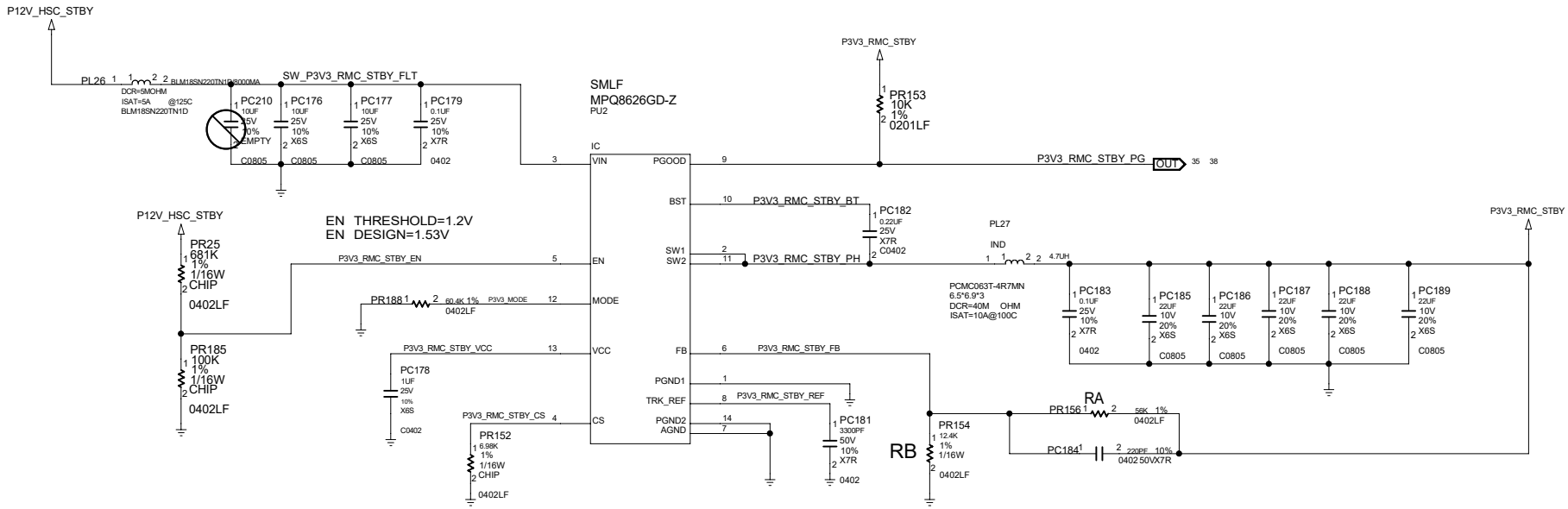


TPS259261DRCR/HotSwap/P12V_STBY

NOKIA	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
		REVIEWER	OPEN EDGE RMC	N/A	1.15
			SIZE C	DATE Wed Nov 21 14:10:21 2018	SHEET 33 OF 41

P3V3_RMC_STBY SPECIFICATION
VOUT=3.3V +/-5%
OUTPUT RIPPLE & NOISE < +/-50MV
TRANSIENT TOLERANCE=300MV
TDC =3.6A
MAX CURRENT =3.6A
OCP(IMAX*130%) =4.72A
CURRENT STEP=1.8A
SLEW RATE=2.5/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC

P3V3_RMC_STBY

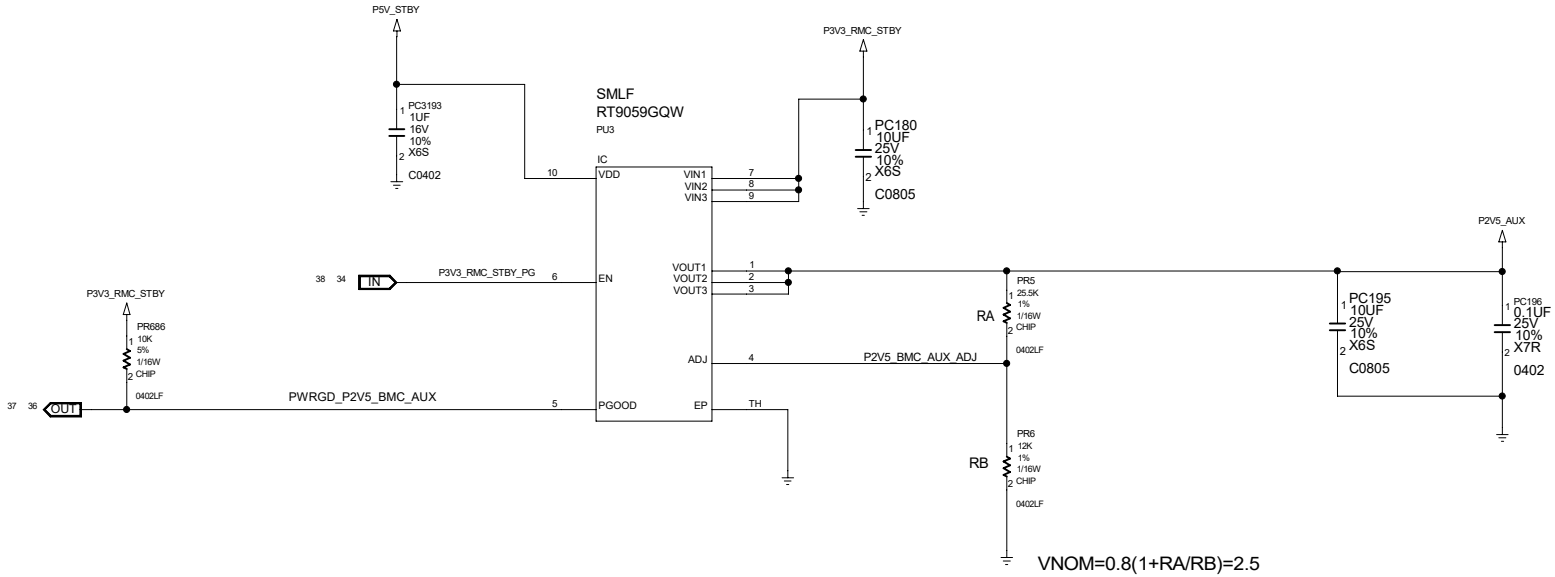


VOUT=0.6(1+RA/RB)=3.309V

MPQ8626GD-Z/P3V3_RMC_STBY

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A / REV: 1.15
		REVIEWER	SIZE: C / DATE: Wed Nov 21 14:10:32 2018	SHEET: 34 OF 41

P2V5_AUX SPECIFICATION
VOUT=2.5V +/-5%
OUTPUT RIPPLE & NOISE < +/-30MV
TRANSIENT TOLERANCE=250MV
TDC =0.3A
MAX CURRENT =0.3A
PD=(3.3V-2.5V)*0.3A=0.15W

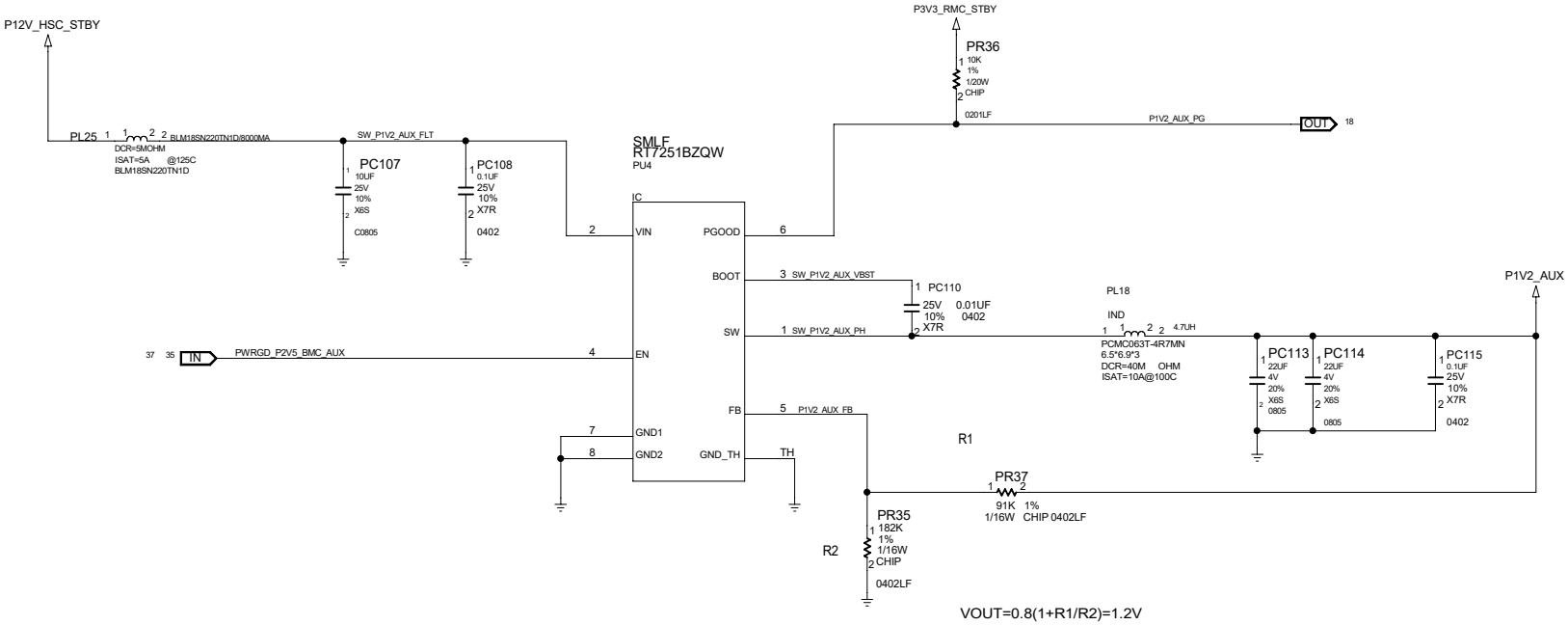


RT2518GQW/P2V5_AUX

NOKIA	DEPARTMENT	DESIGNER / REVIEWER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A / REV: 1.15
			SIZE: C DATE: Wed Nov 21 14:10:45 2018	SHEET: 35 OF 41

P1V2_AUX SPECIFICATION
VOUT=1.2V +/-5%
OUTPUT RIPPLE & NOISE < +/-30MV
TRANSIENT TOLERANCE=120MV
TDC =0.75A
MAX CURRENT =0.75A
OCP(IC RATING)=2.6A
CURRENT STEP=0.37A
SLEW RATE=2.5/US
WORK FREQUENCY=800KHZ
EFFICIENCY > 85% @TDC

P1V2_AUX

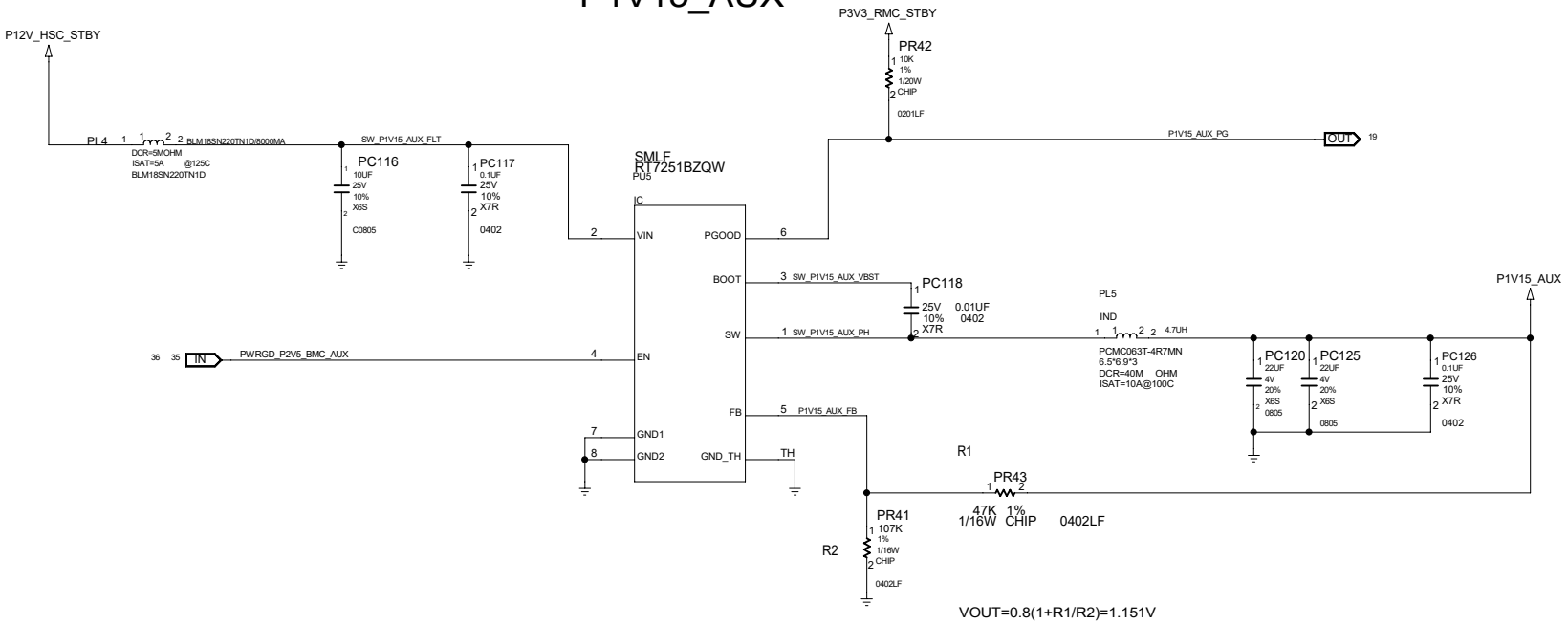


RT7251BZQW/P1V2_AUX

NOKIA	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
		REVIEWER	OPEN EDGE RMC	N/A	1.15
			SIZE C DATE Wed Nov 21 14:11:00 2018		SHEET 36 OF 41

P1V15_AUX SPECIFICATION
VOUT=1.15V +/-5%
OUTPUT RIPPLE & NOISE < +/-30MV
TRANSIENT TOLERANCE=120MV
TDC =0.75A
MAX CURRENT =0.75A
OCP(IC RATING)=2.6A
CURRENT STEP=0.37A
SLEW RATE=2.5/US
WORK FREQUENCY=800KHZ
EFFICIENCY > 80% @TDC

P1V15_AUX

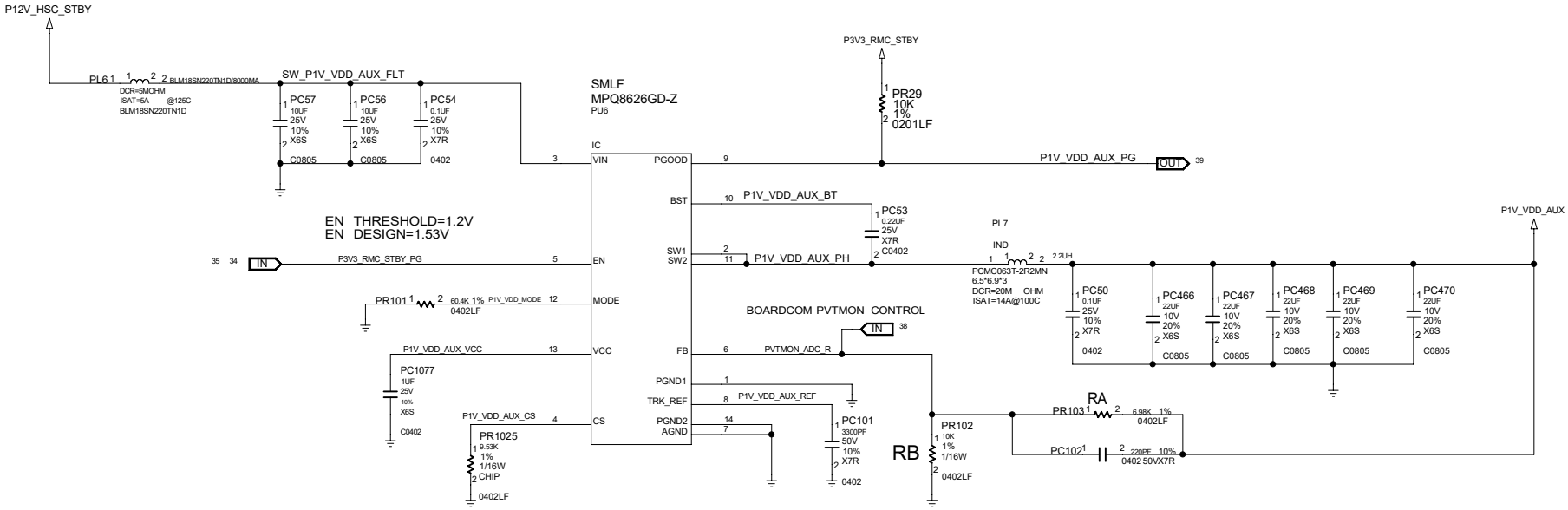


RT7251BZQW/P1V15_AUX

NOKIA	DEPARTMENT	DESIGNER	PROJCET: OPEN EDGE RMC	DOCUMENT NUMBER: N/A
		REVIEWER	SIZE: C DATE: Wed Nov 21 14:11:16 2018	REV: 1.15
				SHEET: 37 OF 41

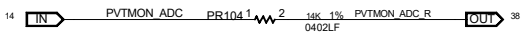
P1V_VDD_AUX SPECIFICATION
VOUT=1.0V +/-5%
OUTPUT RIPPLE & NOISE < +/-20MV
TRANSIENT TOLERANCE=100MV
TDC =2.7A
MAX CURRENT =2.7A
OCP(IMAX*130%) =3.5A
CURRENT STEP=1.35A
SLEW RATE=2.5/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 85% @TDC

P1V_VDD_AUX



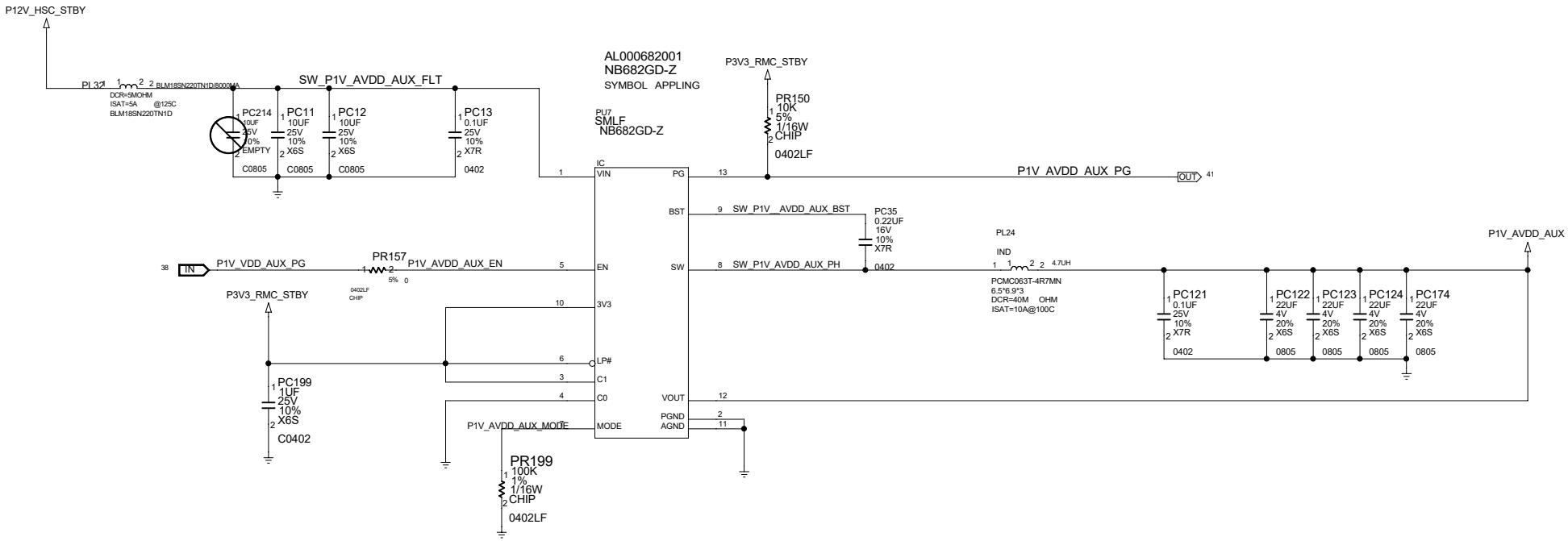
VOUT=0.6(1+RA/RB)=1.0188V

BROADCOM PVTMON CONTROL



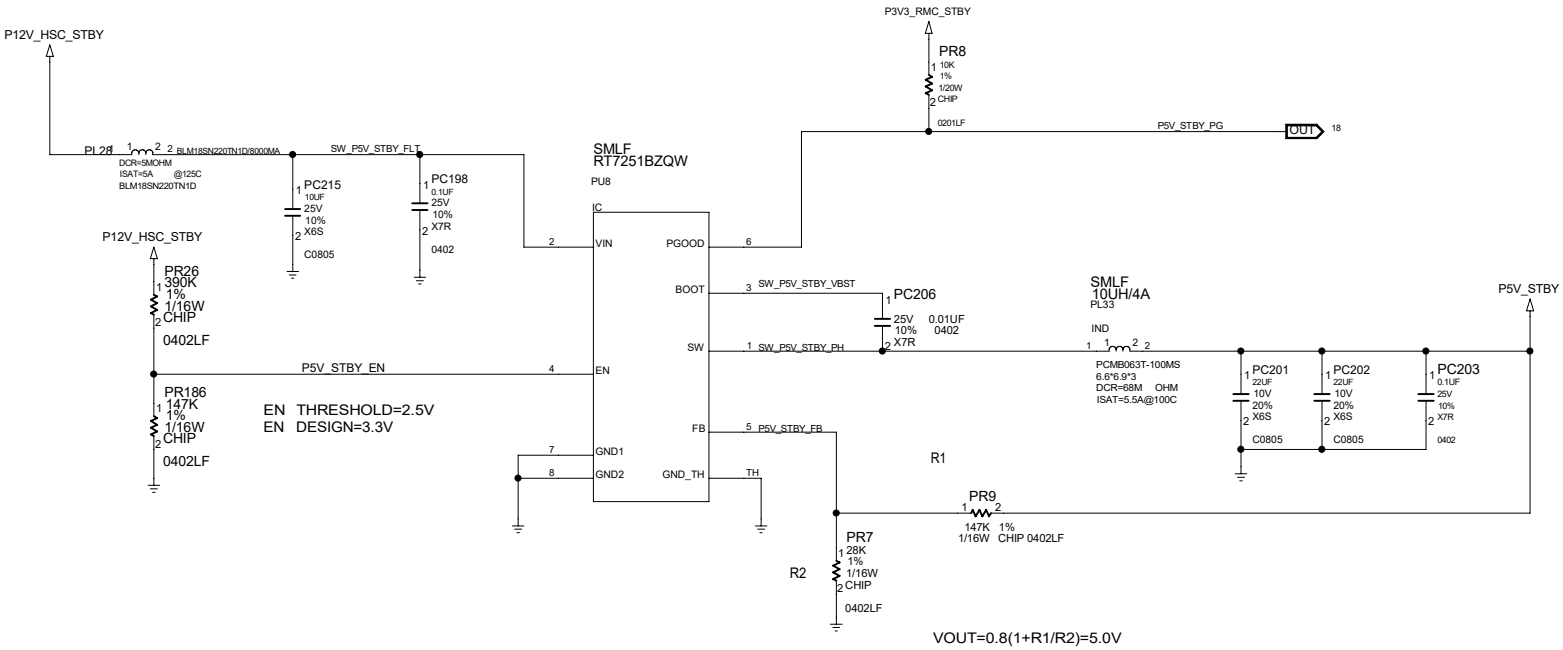
P1V_AVDD_AUX SPECIFICATION
VOUT=1.0V +/-5%
OUTPUT RIPPLE & NOISE < +/-20MV
TRANSIENT TOLERANCE=100MV
TDC =1.0A
MAX CURRENT =1.0A
OCP(IC RATING)=7A
CURRENT STEP=0.5A
SLEW RATE=2.5/US
WORK FREQUENCY=750KHZ
EFFICIENCY > 85% @TDC

P1V_AVDD_AUX



P5V_STBY SPECIFICATION
VOUT=5V +/-5%
OUTPUT RIPPLE & NOISE < +/-30MV
TRANSIENT TOLERANCE=500MV
TDC =0.7A
MAX CURRENT =0.7A
OCP(IC RATING)=2.6A
CURRENT STEP=0.35A
SLEW RATE=2.5/US
WORK FREQUENCY=800KHZ
EFFICIENCY > 85% @TDC

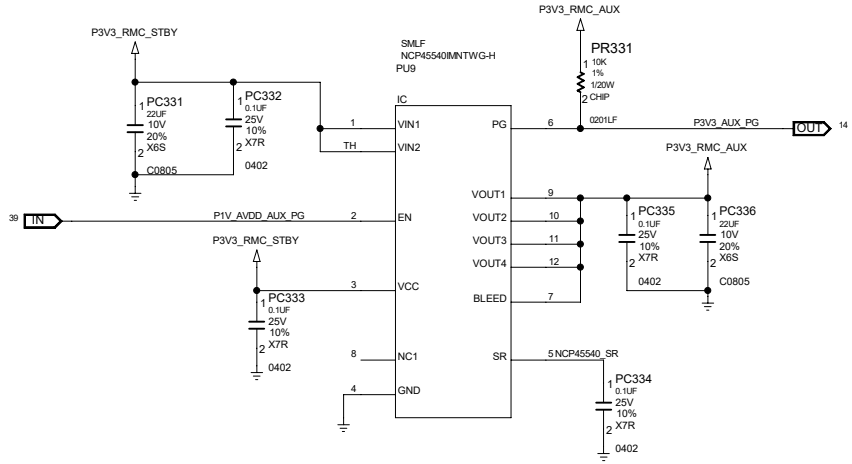
P5V_STBY



RT7251BZQW/P5V_STBY

NOKIA	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
		REVIEWER	OPEN EDGE RMC	N/A	1.15
			SIZE C DATE Wed Nov 21 14:12:00 2018		SHEET 40 OF 41

P3V3_RMC_AUX


P3V3_RMC_STBY
PC331
22UF
10V
20%
X6S
C0805
PC332
0.1UF
25V
10%
X7R
0402
SMLF
NCP45540IMNTWG-H
PU9
IC
VIN1
VIN2
EN
VCC
NC1
GND
VOUT1
VOUT2
VOUT3
VOUT4
BLEED
PG
SR
P3V3_RMC_AUX
PR331
10K
1%
1/20W
CHIP
0201LF
P3V3_AUX_PG
OUT
IN
P1V_AVDD_AUX_PG
PC333
PC334
PC335
PC336
NCP45540_SR