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Compute Project

Mt. Jade

Ampere Altra® /AltraMax™

Motherboard Specification

v1.0

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1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

Wiwynn Corporation

2. OCP Tenets Compliance

2.1. Openness

The Mt. Jade Design Specification exemplifies openness by providing a design for a server CPU which can be used to support numerous use cases ranging from general compute to storage to accelerators. This server design can be used as a standalone device in a standard 19” rack.

2.2. Efficiency

The form factor of the Mt. Jade server allows for better air flow and more efficient cooling for a higher powered CPU.

2.3. Impact

Mt. Jade is designed to dramatically reduce time to market for additional card and drive configurations. This server board can connect directly to custom risers and different NVMe drives on the backplane.

2.4. Scale

3. Revision Table

Date	Revision #	Author	Description
Aug 31, 2021	0.50	Yoon Chae	Draft
Sept 2, 2021	0.75	Jayesh Shah	Review Draft
Sept 17, 2021	1.0	Yoon Chae	Updated physical specifications

4. Scope

This specification describes the design of the Mt. Jade server board based on Ampere® Altra® and Altra Max™ processors.

5. Overview

All processor names mentioned in this specification refer to Ampere® Altra® and Altra Max™ processors (formerly codenamed Quicksilver and Mystique processors). Details on Ampere processors can be found at https://amperecomputing.com/altra/
This document describes a dual socket server design based on Ampere® Altra® and Altra Max® processors, which is referred to hereinafter as Mt. Jade server motherboard.

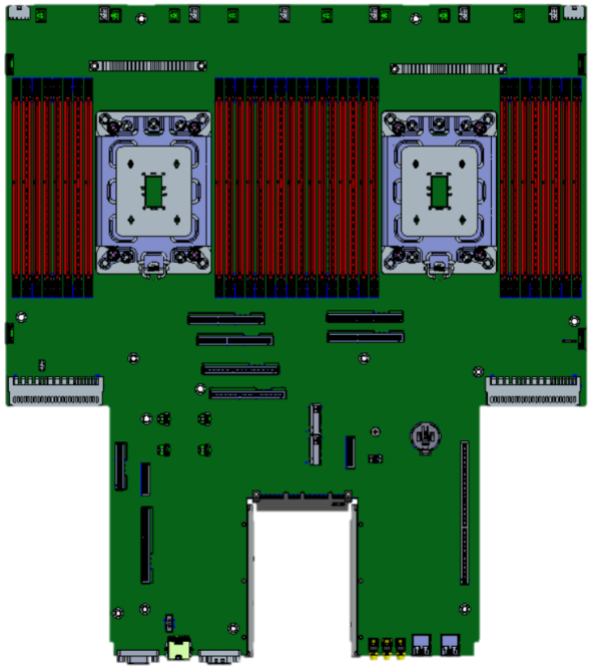

Figure 1: Mt. Jade Server Motherboard

Mt. Jade server motherboard is designed with dual sockets, 32 DDR4 DIMMs for 2DPC-3200 configuration, 4C+ connector for x16 PCIE Gen4 OCPv3 NIC, riser connectors for PCIe riser cards, onboard ASPEED AST2500 BMC, and two CRPS PSU connectors.

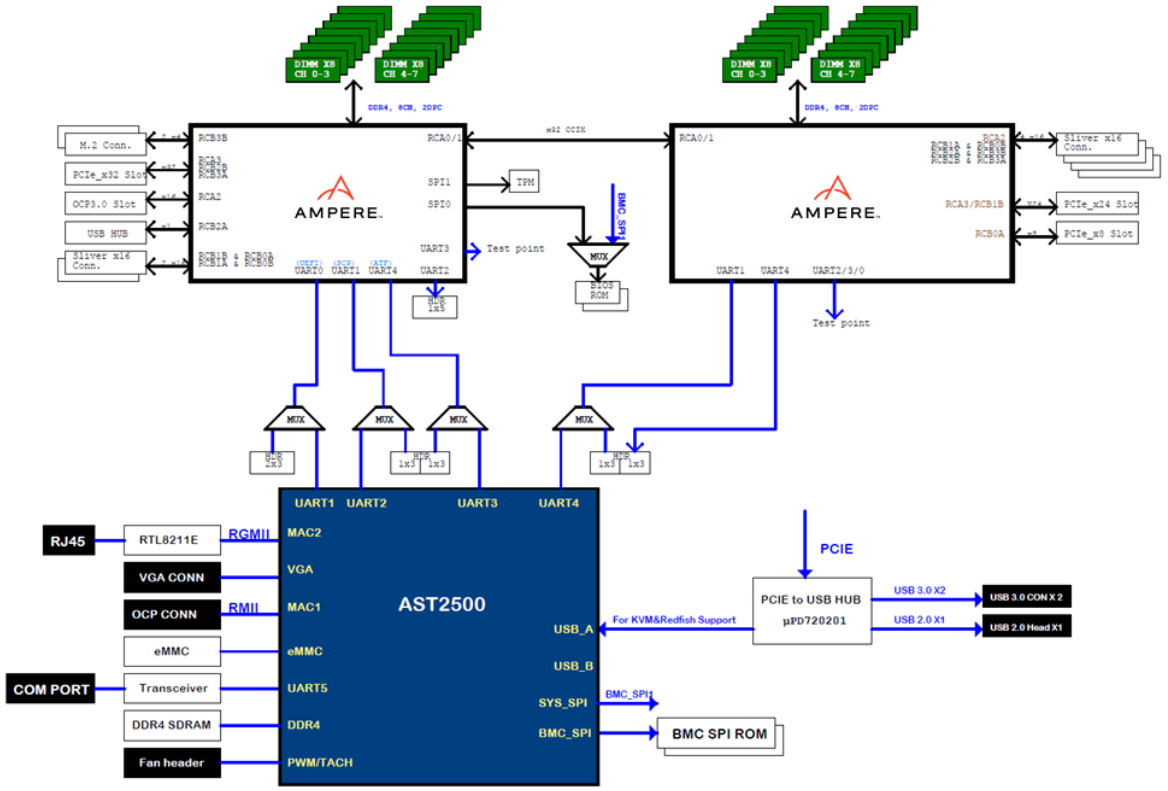

Figure 2: Mt. Jade Block Diagram

The server motherboard has the option to support two M.2 SSD drives. One can be used as boot drive and the other can be used as data drive or backup boot drive. Both the x4 PCIe link to the boot drive and the data drive shall be connected to the CPU. The recommended minimum capacity of the boot drive is 256GB. The system can support M.2 drives of 22110 or 2280 form factor.

Mt. Jade 2S server shall connect to an OCP v3.0 NIC on the platform through its PCIe. The server will utilize the remaining PCIe lanes to enable high bandwidth connections to 1U and 2U system boards such as risers and backplane.

This document covers MB block diagram, features, BMC sub-system, power management, and miscellaneous physical specification of the motherboard.

6. Rack Compatibility

[Note to author of this specification: This section should document the incremental features in the product implementation. The product must be 100% compliant with any and all features or requirements described in this baseline specification.]

7. Physical Specifications

7.1. Motherboard Features

Mt. Jade motherboard supports for the following features:

Processor		
	CPU	Ampere Altra®/AltraMax™ processors
	Sockets	Dual LGA sockets
	TDP	210W (1U) / 250W (2U)
Memory		
	DIMM Slots	32 DIMM slots total, 2 DIMMs per channel
	DIMM Type	DDR4 RDIMM/LRDIMM with ECC
	DIMM Speed	DDR4-3200 (2DPC)
	DIMM Size	16GB, 32GB, 64GB, 128GB, 256GB
	Capacities	Up to 8TB (4TB per CPU)
Storage		
	NVMe M.2	2x on-board 2280/22110 slots, x4 Gen3/Gen4
	NVMe U.2	6x Sliver connectors for NVMe BP, 24x 2.5” x4 Gen3/Gen4 U.2 NVMe drives with hot plug support
	SAS/SATA	PCIe-HBA with SATA BP, 24x 2.5” or 12x 3.5” SAS/SATA drives with hot plug support
PCI-Express Expansion		
	PCIe Risers	1x Gen4 x32 vertical connector, two x8 + one x16 port 1x Gen4 x8/x16 vertical connector, one x8 + one x16 port 1x Gen4 x8 vertical connector
	OCPv3.0	1x x16 Gen4 OCP3.0 connector
Networking		
	LOM	OCP3.0 NIC PCIe x16 Gen4

	MGMT	1x 1GbE from BMC to Rear RJ45 Connector
MISC		
	Front Panel	PWR / RST / UID buttons One USB 2.0 port One VGA connector
	Rear Panel	VGA, RJ-45, Serial Port, 2x USB 2.0/3.0, UID/Reset/Power Buttons
	FAN	6x 6056 dual-rotor fan connectors 8x 4056 dual-rotor fan connectors Hot plug support
	PSU	Dual CRPS PSU with 1+1 redundancy, hot plug support
Server Management		
	Chipset	BMC ASPEED AST2500
System Firmware		
	BIOS	AMI Aptio® V, EDK-II
	BMC	AMI MegaRAC®, OpenBMC
	Security	TPM 2.0

7.2. Motherboard Placement

Mt. Jade is a spread-core motherboard design. The motherboard is 428mm wide x 479.36mm deep and will fit in an EIA-19" 1U/2U rack mount chassis. There are two sets of fan connectors which are placed in the top side of the board to support six 6056 dual rotor fans for 2U chassis and eight 4056 dual rotor fans for 1U chassis. The master CPU socket is placed in the right side of the motherboard which is required to boot the system when a single CPU is populated.

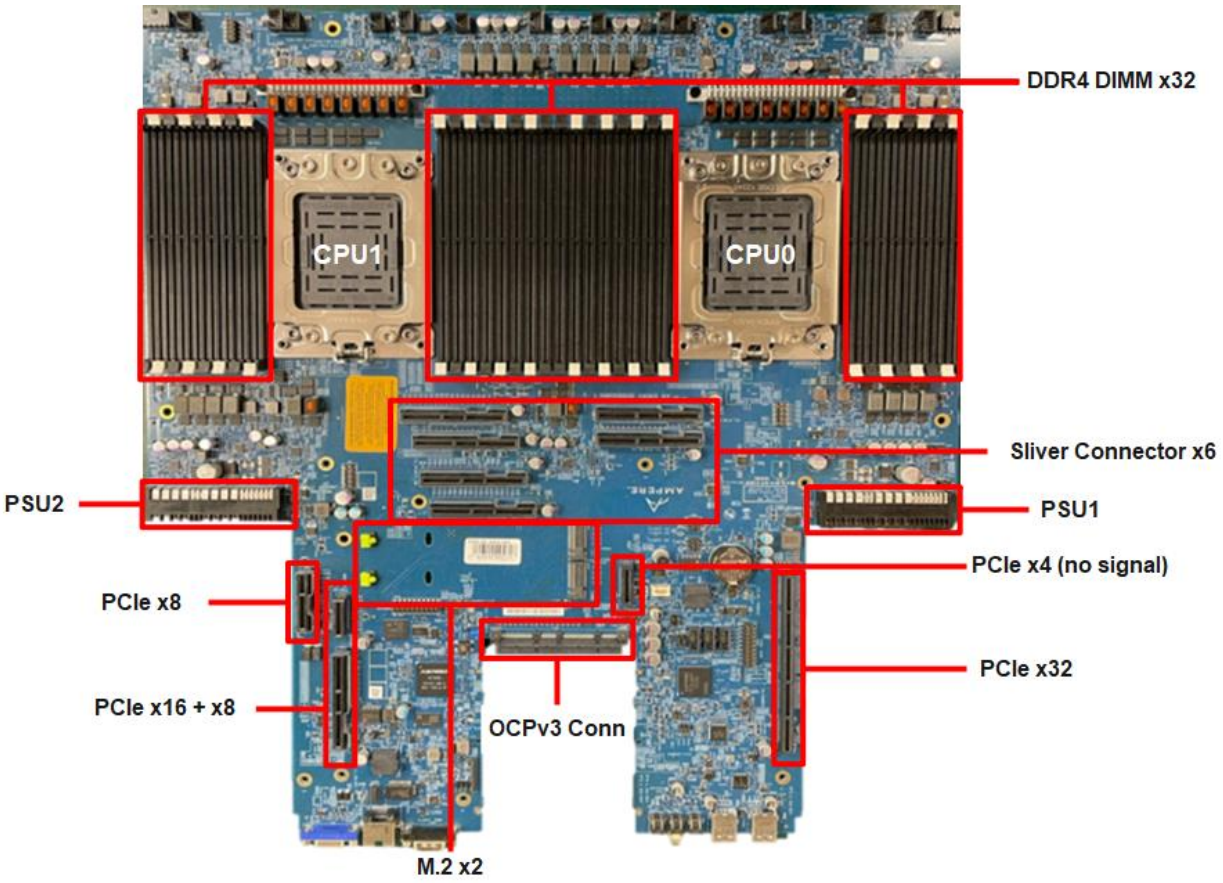

Figure 3: Mt. Jade Motherboard Placement

There are six sliver connectors which are placed in the center of the motherboard. The sliver connectors are used to connect Altra®/Altra Max™ PCIe lanes to the NVMe backplane through cables. There are two connectors for CPU0 PCIe ports and the other four connectors for CPU1 PCIe ports. One sliver connector, SLV3, can be connected to riser card through cable to support x16 PCIe card.

Two M.2 on-board connectors support 2280/22110 NVMe M.2 NVMe SSDs as system boot drives. However, the Mt. Jade system can boot from SAS/SATA drives connected to a PCIe SAS/SATA HBA card.

There are several custom PCIe connectors on Mt. Jade. One x32 lane vertical connector in the right bottom side and one x16 lane OCPv3 connector in the middle side are for CPU0 PCIe ports. There are three connectors in the left side. Two of them, x16 and x8, are vertically aligned for x24 riser card. And the other x8 connector is for x8/x16 combo riser card.

7.3. CPUs

Ampere Altra processor supports up to 80 ARMv8 CPU cores, max 3.0 GHz, and 210W TDP. Altra Max supports up to 128 ARMv8 CPU cores, max 3.2GHz, and 250W TDP. Both processors have same processor interfaces, 8 channel DDR4, 128 lanes of Gen4 PCIe, and miscellaneous processor interfaces for system management and control.

Altra processor has 4 native x16 PCIe ports, configurable as CCIX, and 8 native x8 PCIe ports. Altra Max processor has 8 native x16 ports of which 4 x16 ports can be configured as CCIX. The detail PCIe configurations of Mt. Jade board for Altra/Altra Max are described in PCIe Configuration section.

Package of Altra/Altra Max processors is LGA in 77mm x 67mm with 4926 pins. Altra and AltraMax are pin-to-pin compatible.

Mt. Jade motherboard supports single or dual Ampere Altra/Altra Max processors. 1U Mt. Jade system supports Altra/Altra Max processor SKU’s up to 210W TDP and 2U system supports them up to 250W TDP.

7.4. DIMMs

Mt. Jade motherboard has total 32 DDR4 DIMM connectors, 16 per socket, 2 DIMMs per channel. The Figure 4 shows the labels of 32 DIMM sockets which is used for DIMM installation order.

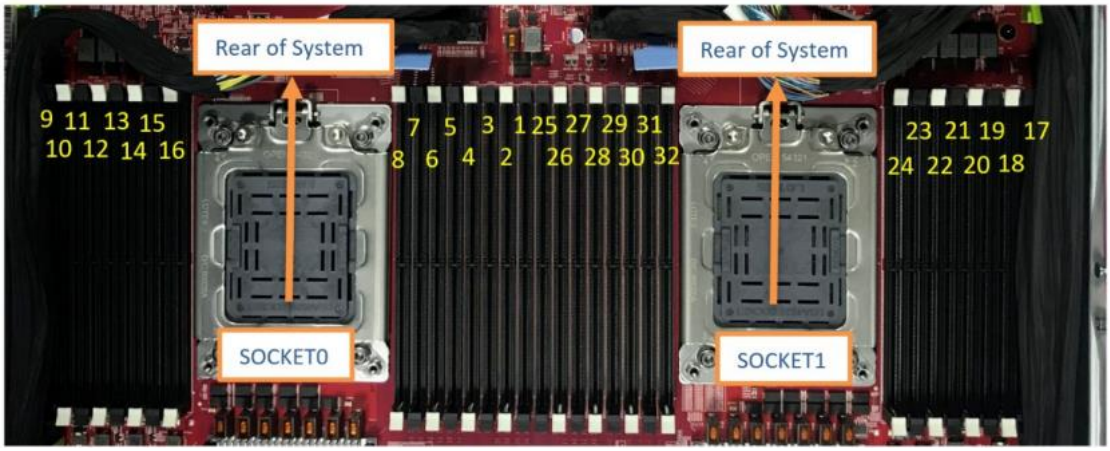

Figure 4 Mt.Jade DIMM Socket Label

The Table 1 & Table 2 show DIMM installation sequence for 2 DIMM-Per-Channel configurations for each socket, Master and Slave.

DIMM Configurations (Socket0-2DPC)	MCU4		MCU5		MCU6		MCU7		MCU3		MCU2		MCU1		MCU0	
	9	10	11	12	13	14	15	16	8	7	6	5	4	3	2	1
2 DIMM_MCU0															V	V
2 DIMM_MCU1													V	V		
2 DIMM_MCU2											V	V				
2 DIMM_MCU3									V	V						
2 DIMM_MCU4	V	V														
2 DIMM_MCU5			V	V												
2 DIMM_MCU6					V	V										
2 DIMM_MCU7							V	V								
4 DIMM_MCU04	V	V													V	V
8 DIMM_MCU0145	V	V	V	V									V	V	V	V
8 DIMM_MCU0246	V	V			V	V					V	V			V	V
8 DIMM_MCU0347	V	V					V	V	V	V					V	V
8 DIMM_MCU1357			V	V			V	V	V	V			V	V		
8 DIMM_MCU0267					V	V	V	V			V	V			V	V
12 DIMM_MCU012456	V	V	V	V	V	V					V	V	V	V	V	V
12 DIMM_MCU013457	V	V	V	V			V	V	V	V			V	V	V	V
12 DIMM_MCU023467	V	V			V	V	V	V	V	V	V	V			V	V
12 DIMM_MCU123567			V	V	V	V	V	V	V	V	V	V	V	V		
16 DIMM_MCU01234567	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Table 1 2DPC Installation Sequence for DIMMs in Socket0 (Master) side

DIMM Configurations (Socket1-2DPC)	MCU4		MCU5		MCU6		MCU7		MCU3		MCU2		MCU1		MCU0	
	25	26	27	28	29	30	31	32	24	23	22	21	20	19	18	17
2 DIMM_MCU0															V	V
2 DIMM_MCU1													V	V		
2 DIMM_MCU2											V	V				
2 DIMM_MCU3									V	V						
2 DIMM_MCU4	V	V														
2 DIMM_MCU5			V	V												
2 DIMM_MCU6					V	V										
2 DIMM_MCU7							V	V								
4 DIMM_MCU04	V	V													V	V
8 DIMM_MCU0145	V	V	V	V									V	V	V	V
8 DIMM_MCU0246	V	V			V	V					V	V			V	V
8 DIMM_MCU0347	V	V					V	V	V	V					V	V
8 DIMM_MCU1357			V	V			V	V	V	V			V	V		
8 DIMM_MCU0267					V	V	V	V			V	V			V	V
12 DIMM_MCU012456	V	V	V	V	V	V					V	V	V	V	V	V
12 DIMM_MCU013457	V	V	V	V			V	V	V	V			V	V	V	V
12 DIMM_MCU023467	V	V			V	V	V	V	V	V	V	V			V	V
12 DIMM_MCU123567			V	V	V	V	V	V	V	V	V	V	V	V		
16 DIMM_MCU01234567	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Table 2 2DPC Installation Sequence for DIMMs in Socket1 (Slave) side

Altra / AltraMax supports mixed DIMM configuration listed in Table 3. Most of mixed DIMM configurations are supported when the different DIMMs are installed in different channels. When different DIMMs are installed in same channel, only RCD or SDRAM Die variations are allowed.

MIXING DIMM SUPPORT	Different RCD	Different DRAM DIES	Mixing x4 & x8	Different Density	Different Speed	Different Vendor	Mixing 1R & 2R
Different Channel	Yes	Yes	Yes	Yes	Yes	Yes	TBD
Same Channel	Yes	Yes	No	No	Not Preferred	Not Preferred	No

Table 3 Supported Mixed DIMM Configurations

7.5. PCIe Configuration

Mt. Jade motherboard supports both Altra/Altra Max processors which are same in terms of number of Gen4 lanes but are different in terms of PCIe port configurations.

Altra processor has 4 x16 and 8 x8 Gen4 PCIe ports. The x16 Gen4 PCIe port is called as RCA (Root Complex – TypeA) and it can be bifurcated to 2 x8 Gen4 or 4 x4 Gen4 ports or configured as x16 CCIX port. The x8 Gen4 PCIe port is called as RCB (Root Complex – TypeB) and it can be bifurcated to 2 x4 ports.

Altra Max process has 8 x16 PCIe ports which are all RCA. Each x16 RCA port can be bifurcated to 2 x8 or 4 x4 ports.

The Table 4 shows the PCIe configurations supported by Altra/Altra Max.

PCIE Port Mapping			
Altra		**AltraMax**	
RCA0	PCIE4 or CCIX	RCA0	PCIE4 or CCIX
RCA1		RCA1	
RCA2		RCA2	
RCA3		RCA3	
RCB0A	PCIE4	RCA4[15:8]	PCIE4
RCB1B		RCA4[7:0]	
RCB0B		RCA5[15:8]	
RCB1A		RCA5[7:0]	
RCB3B		RCA6[15:8]	
RCB2A		RCA6[7:0]	
RCB3A		RCA7[15:8]	
RCB2B		RCA7[7:0]	

PCIE Bifurcation	
RCA	**RCB**
x16	x8
x8/x8	x4/x4
x8/x4/x4	
x4/x4/x4/x4	

Table 4 Altra/AltraMax PCIE ports mapping & valid bifurcation configuration

Note: ‘x8/x4/x4’ configuration means the lower 8 lanes, RCA[7:0], are mapped to x8 port, other two x4 lanes, RCA[11:8] & RCA[15:12], are mapped to two x4 ports. And the ‘x4/x4/x8’ configuration is not supported.

7.5.1. Mt.Jade PCIE Configuration

The Table 5 shows the Mt.Jade PCIE ports configuration, device connectivity, and the port mapping between Altra and AltraMax. And Figure 5 shows the same as block diagram with 2U PCIE riser cards.

Mt.Jade PCIE Configuration			
Altra	**AltraMax**	**PCIE Port Connectors**	**PCIE Port Connectivity**
S0_RCA2	S0_RCA2	SFF-TA-1002 4C Right Angle Connector	OCPv3 NIC
S0_RCA3	S0_RCA3	SFF-TA-1002 4C+ (280 pins) Vertical Connector	Riser_x32 - CN2
S0_RCB3A	S1_RCA7[15:8]		Riser_x32 - CN3
S0_RCB2B	S1_RCA7[7:0]		Riser_x32 - CN1
S0_RCB0B	S0_RCA5[15:8]	SFF-TA-1002 4C (140 pins) Vertical Connector	Backplane - 2 x4 U.2
S0_RCB1A	S0_RCA5[7:0]		Backplane - 2 x4 U.2
S0_RCB0A	S0_RCA4[15:8]	SFF-TA-1002 4C (140 pins) Vertical Connector	Backplane - 2 x4 U.2
S0_RCB1B	S0_RCA4[7:0]		Backplane - 2 x4 U.2
S0_RCB3B	S0_RCA6[15:8]	2x M.2 NGFF Connectors	2 x4 M.2 NVMe SSDs
S0_RCB2A	S0_RCA6[7:0]	No Connectors	BMC VGA (x1 PCIE2) PCIE2USB adapter (x1 PCIE2)
S1_RCA2	S1_RCA2	SFF-TA-1002 4C (140 pins) Vertical Connector	Backplane - 4 x4 U.2 or Riser_x8 CN1 (x16)
S1_RCA3	S1_RCA3	SFF-TA-1002 4C (140 pins) Vertical Connector	Riser_x24 - CN2 (x8) and CN3 (x8)
S1_RCB1B	S1_RCA4[7:0]	SFF-TA-1002 EDSFF (56 pins) Vertical Connector	Riser_x24 - CN1 (x8)
S1_RCB0A	S1_RCA4[15:8]	SFF-TA-1002 2C (84 pins) Vertical Connector	Riser_x8 - CN2
S1_RCB0B	S1_RCA5[15:8]	SFF-TA-1002 4C (140 pins) Vertical Connector	Backplane - 2 x4 U.2
S1_RCB1A	S1_RCA5[7:0]		Backplane - 2 x4 U.2
S1_RCB3B	S1_RCA6[15:8]	SFF-TA-1002 4C (140 pins) Vertical Connector	Backplane - 2 x4 U.2
S1_RCB2A	S1_RCA6[7:0]		Backplane - 2 x4 U.2
S1_RCB3A	S1_RCA7[15:8]	SFF-TA-1002 4C (140 pins) Vertical Connector	Backplane - 2 x4 U.2
S1_RCB2B	S1_RCA7[7:0]		Backplane - 2 x4 U.2

Table 5 Mt.Jade MB PCIE Ports Configuration & Mapping between Altra and AltraMax

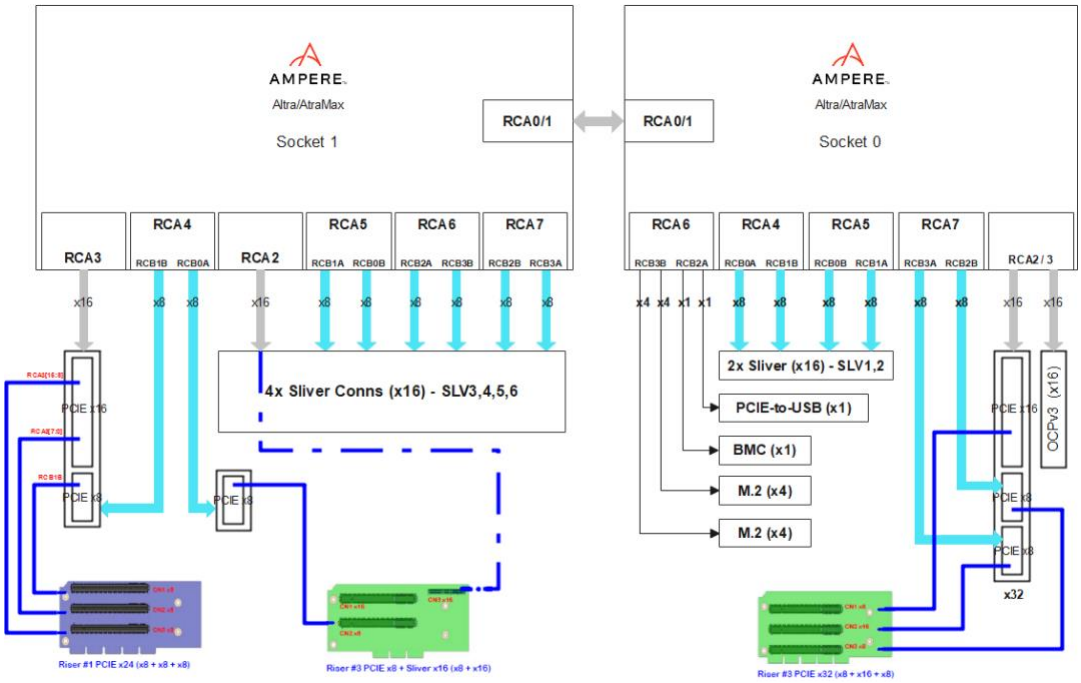

Figure 5 Mt.Jade PCIE port configuration and mapping between Altra and AltraMax

7.5.2. PCIE connectors

Mt.Jade MB uses the five different SFF-TA-1002 connectors to support Gen4 PCIe interfaces and M.2 NGFF connector for onboard M.2 NVMe SSD devices:

- SFF-TA-1002 4C+ vertical connector for x32 PCIe riser card
- SFF-TA-1002 4C right angle connector for OCPv3 network card
- SFF-TA-1002 4C vertical connectors for U.2 NVMe SSD backplane
- SFF-TA-1002 4C and EDSFF vertical connectors for x24 PCIe riser card
- SFF-TA-1002 2C connector for x8 PCIe riser card
- M.2 NGFF connector for M.2 NVMe SSD devices

7.5.2.1. PCIe x32 Riser Connector and Pin definition

Figure 6 TE: 2328461-2 Pin:280

Pin #	Pin Definition	Pin #	Pin Definition
A1	GND	A71	S0_PCIERCA3_RX_12_N
A2	GND	A72	GND
A3	GND	A73	S0_PCIERCA3_RX_13_P
A4	GND	A74	S0_PCIERCA3_RX_13_N
A5	GND	A75	GND
A6	GND	A76	S0_PCIERCA3_RX_14_P
A7	GND	A77	S0_PCIERCA3_RX_14_N
A8	GND	A78	GND
A9	GND	A79	S0_PCIERCA3_RX_15_P
A10	GND	A80	S0_PCIERCA3_RX_15_N
A11	+3V3	A81	GND
A12	+3V3	A82	CON_S0_RCA32_PERST_L
A13	+3V3	A83	S0_PCIERCA3_WAKE_L
A14	+3V3	A84	GND
A15	GND	A85	GND
A16	GND	A86	S0_PCIERCB_2B_PRSNT_1C_L
A17	GND	A87	S0_PCIERCB_3A_PRSNT_1C_L
A18	GND	A88	GND
A19	GND	A89	S0_PCIERCB2B_RX_0_P
A20	S0_PCIERCB_3A_SCL	A90	S0_PCIERCB2B_RX_0_N
A21	S0_PCIERCB_3A_SDA	A91	GND
A22	GND	A92	S0_PCIERCB2B_RX_1_P
A23	S0_PCIERCB_2B_SCL	A93	S0_PCIERCB2B_RX_1_N
A24	S0_PCIERCB_2B_SDA	A94	GND
A25	GND	A95	S0_PCIERCB2B_RX_2_P
A26	CLK100M_S0_RCA3_1_REF_P	A96	S0_PCIERCB2B_RX_2_N
A27	CLK100M_S0_RCA3_1_REF_N	A97	GND
A28	GND	A98	S0_PCIERCB2B_RX_3_P
A29	GND	A99	S0_PCIERCB2B_RX_3_N
A30	S0_PCIERCA3_RX_0_P	A100	GND
A31	S0_PCIERCA3_RX_0_N	A101	S0_PCIERCB2B_RX_4_P
A32	GND	A102	S0_PCIERCB2B_RX_4_N
A33	S0_PCIERCA3_RX_1_P	A103	GND
A34	S0_PCIERCA3_RX_1_N	A104	S0_PCIERCB2B_RX_5_P
A35	GND	A105	S0_PCIERCB2B_RX_5_N
A36	S0_PCIERCA3_RX_2_P	A106	GND
A37	S0_PCIERCA3_RX_2_N	A107	S0_PCIERCB2B_RX_6_P
A38	GND	A108	S0_PCIERCB2B_RX_6_N
A39	S0_PCIERCA3_RX_3_P	A109	GND
A40	S0_PCIERCA3_RX_3_N	A110	S0_PCIERCB2B_RX_7_P
A41	GND	A111	S0_PCIERCB2B_RX_7_N
A42	S0_PCIERCA3_RX_4_P	A112	GND
A43	S0_PCIERCA3_RX_4_N	A113	GND
A44	GND	A114	S0_PCIERCB_3A_PRSNT_2C_L
A45	S0_PCIERCA3_RX_5_P	A115	CON_S0_RCB3A_PERST_L
A46	S0_PCIERCA3_RX_5_N	A116	GND
A47	GND	A117	S0_PCIERCB3A_RX_0_P
A48	S0_PCIERCA3_RX_6_P	A118	S0_PCIERCB3A_RX_0_N
A49	S0_PCIERCA3_RX_6_N	A119	GND
A50	GND	A120	S0_PCIERCB3A_RX_1_P
A51	S0_PCIERCA3_RX_7_P	A121	S0_PCIERCB3A_RX_1_N
A52	S0_PCIERCA3_RX_7_N	A122	GND
A53	GND	A123	S0_PCIERCB3A_RX_2_P
A54		A124	S0_PCIERCB3A_RX_2_N
A55		A125	GND
A56	GND	A126	S0_PCIERCB3A_RX_3_P
A57	GND	A127	S0_PCIERCB3A_RX_3_N
A58	S0_PCIERCA3_RX_8_P	A128	GND
A59	S0_PCIERCA3_RX_8_N	A129	S0_PCIERCB3A_RX_4_P
A60	GND	A130	S0_PCIERCB3A_RX_4_N
A61	S0_PCIERCA3_RX_9_P	A131	GND
A62	S0_PCIERCA3_RX_9_N	A132	S0_PCIERCB3A_RX_5_P
A63	GND	A133	S0_PCIERCB3A_RX_5_N
A64	S0_PCIERCA3_RX_10_P	A134	GND
A65	S0_PCIERCA3_RX_10_N	A135	S0_PCIERCB3A_RX_6_P
A66	GND	A136	S0_PCIERCB3A_RX_6_N
A67	S0_PCIERCA3_RX_11_P	A137	GND
A68	S0_PCIERCA3_RX_11_N	A138	S0_PCIERCB3A_RX_7_P
A69	GND	A139	S0_PCIERCB3A_RX_7_N
A70	S0_PCIERCA3_RX_12_P	A140	GND

Pin #	Pin Definition	Pin #	Pin Definition
B1	+12V	B71	S0_PCIERCA3_TX_12_N
B2	+12V	B72	GND
B3	+12V	B73	S0_PCIERCA3_TX_13_P
B4	+12V	B74	S0_PCIERCA3_TX_13_N
B5	+12V	B75	GND
B6	+12V	B76	S0_PCIERCA3_TX_14_P
B7	+12V	B77	S0_PCIERCA3_TX_14_N
B8	+12V	B78	GND
B9	+12V	B79	S0_PCIERCA3_TX_15_P
B10	+3V3_SB	B80	S0_PCIERCA3_TX_15_N
B11	+3V3	B81	GND
B12	+3V3	B82	CON_S0_RCA30_PERST_L
B13	+3V3	B83	S0_PCIERCA3_PWR_BRK_L_R
B14	+3V3	B84	S0_PCIERCA3_PRSNT_4C_L
B15	+3V3	B85	GND
B16	GND	B86	S0_PCIERCB_2B_PWR_BRK_L_R
B17	GND	B87	CON_S0_RCB2B_PERST_L
B18	GND	B88	GND
B19	GND	B89	S0_PCIERCB2B_TX_0_P
B20	S0_PCIERCA3_SCL	B90	S0_PCIERCB2B_TX_0_N
B21	S0_PCIERCA3_SDA	B91	GND
B22	GND	B92	S0_PCIERCB2B_TX_1_P
B23	CLK100M_S0_RCB3A_0_REF_P	B93	S0_PCIERCB2B_TX_1_N
B24	CLK100M_S0_RCB3A_0_REF_N	B94	GND
B25	GND	B95	S0_PCIERCB2B_TX_2_P
B26	CLK100M_S0_RCB3B_0_REF_P	B96	S0_PCIERCB2B_TX_2_N
B27	CLK100M_S0_RCB3B_0_REF_N	B97	GND
B28	GND	B98	S0_PCIERCB2B_TX_3_P
B29	GND	B99	S0_PCIERCB2B_TX_3_N
B30	S0_PCIERCA3_TX_0_P	B100	GND
B31	S0_PCIERCA3_TX_0_N	B101	S0_PCIERCB2B_TX_4_P
B32	GND	B102	S0_PCIERCB2B_TX_4_N
B33	S0_PCIERCA3_TX_1_P	B103	GND
B34	S0_PCIERCA3_TX_1_N	B104	S0_PCIERCB2B_TX_5_P
B35	GND	B105	S0_PCIERCB2B_TX_5_N
B36	S0_PCIERCA3_TX_2_P	B106	GND
B37	S0_PCIERCA3_TX_2_N	B107	S0_PCIERCB2B_TX_6_P
B38	GND	B108	S0_PCIERCB2B_TX_6_N
B39	S0_PCIERCA3_TX_3_P	B109	GND
B40	S0_PCIERCA3_TX_3_N	B110	S0_PCIERCB2B_TX_7_P
B41	GND	B111	S0_PCIERCB2B_TX_7_N
B42	S0_PCIERCA3_TX_4_P	B112	GND
B43	S0_PCIERCA3_TX_4_N	B113	GND
B44	GND	B114	S0_PCIERCB_2B_PRSNT_2C_L
B45	S0_PCIERCA3_TX_5_P	B115	S0_PCIERCB_3A_PWR_BRK_L_R
B46	S0_PCIERCA3_TX_5_N	B116	GND
B47	GND	B117	S0_PCIERCB3A_TX_0_P
B48	S0_PCIERCA3_TX_6_P	B118	S0_PCIERCB3A_TX_0_N
B49	S0_PCIERCA3_TX_6_N	B119	GND
B50	GND	B120	S0_PCIERCB3A_TX_1_P
B51	S0_PCIERCA3_TX_7_P	B121	S0_PCIERCB3A_TX_1_N
B52	S0_PCIERCA3_TX_7_N	B122	GND
B53	GND	B123	S0_PCIERCB3A_TX_2_P
B54	S0_PCIERCA3_PRSNT_1C_L	B124	S0_PCIERCB3A_TX_2_N
B55	S0_PCIERCA3_PRSNT_2C_L	B125	GND
B56	GND	B126	S0_PCIERCB3A_TX_3_P
B57	GND	B127	S0_PCIERCB3A_TX_3_N
B58	S0_PCIERCA3_TX_8_P	B128	GND
B59	S0_PCIERCA3_TX_8_N	B129	S0_PCIERCB3A_TX_4_P
B60	GND	B130	S0_PCIERCB3A_TX_4_N
B61	S0_PCIERCA3_TX_9_P	B131	GND
B62	S0_PCIERCA3_TX_9_N	B132	S0_PCIERCB3A_TX_5_P
B63	GND	B133	S0_PCIERCB3A_TX_5_N
B64	S0_PCIERCA3_TX_10_P	B134	GND
B65	S0_PCIERCA3_TX_10_N	B135	S0_PCIERCB3A_TX_6_P
B66	GND	B136	S0_PCIERCB3A_TX_6_N
B67	S0_PCIERCA3_TX_11_P	B137	GND
B68	S0_PCIERCA3_TX_11_N	B138	S0_PCIERCB3A_TX_7_P
B69	GND	B139	S0_PCIERCB3A_TX_7_N
B70	S0_PCIERCA3_TX_12_P	B140	GND

Table 6 x32 Riser Connector Pin Definition

7.5.2.2. PCIe x24 Riser Connector and Pin definition

Figure 7 TE: 2332139-3 Pin:140 + TE:2327679-3 Pin:56

TE: 2332139-3			
Pin #	Pin Definition	Pin #	Pin Definition
B1	+12V	A1	GND
B2	+12V	A2	GND
B3	+12V	A3	GND
B4	+12V	A4	GND
B5	+12V	A5	GND
B6	+12V	A6	GND
B7	+3V3_SB	A7	GND
B8	+3V3	A8	+3V3
B9	+3V3	A9	+3V3
B10	+3V3	A10	+3V3
B11	+3V3	A11	+3V3
B12	+3V3	A12	GND
B13	GND	A13	GND
B14	CON_S1_RCA30_PERST_L	A14	GND
B15	S1_PCIERCA3_WAKE_L	A15	GND
B16	GND	A16	GND
B17	S1_PCIERCA3_TX_15_N	A17	S1_PCIERCA3_RX_15_N
B18	S1_PCIERCA3_TX_15_P	A18	S1_PCIERCA3_RX_15_P
B19	GND	A19	GND
B20	S1_PCIERCA3_TX_14_N	A20	S1_PCIERCA3_RX_14_N
B21	S1_PCIERCA3_TX_14_P	A21	S1_PCIERCA3_RX_14_P
B22	GND	A22	GND
B23	S1_PCIERCA3_TX_13_N	A23	S1_PCIERCA3_RX_13_N
B24	S1_PCIERCA3_TX_13_P	A24	S1_PCIERCA3_RX_13_P
B25	GND	A25	GND
B26	S1_PCIERCA3_TX_12_N	A26	S1_PCIERCA3_RX_12_N
B27	S1_PCIERCA3_TX_12_P	A27	S1_PCIERCA3_RX_12_P
B28	GND	A28	GND
B29	GND	A29	GND
B30	S1_PCIERCA3_TX_11_N	A30	S1_PCIERCA3_RX_11_N
B31	S1_PCIERCA3_TX_11_P	A31	S1_PCIERCA3_RX_11_P
B32	GND	A32	GND
B33	S1_PCIERCA3_TX_10_N	A33	S1_PCIERCA3_RX_10_N
B34	S1_PCIERCA3_TX_10_P	A34	S1_PCIERCA3_RX_10_P
B35	GND	A35	GND
B36	S1_PCIERCA3_TX_9_N	A36	S1_PCIERCA3_RX_9_N
B37	S1_PCIERCA3_TX_9_P	A37	S1_PCIERCA3_RX_9_P
B38	GND	A38	GND
B39	S1_PCIERCA3_TX_8_N	A39	S1_PCIERCA3_RX_8_N
B40	S1_PCIERCA3_TX_8_P	A40	S1_PCIERCA3_RX_8_P
B41	GND	A41	GND
B42	S1_PCIERCA3_1_PRSNT_2C_L	A42	CON_S1_RCA32_PERST_L
B43	GND	A43	GND
B44	S1_PCIERCA3_TX_7_N	A44	S1_PCIERCA3_RX_7_N
B45	S1_PCIERCA3_TX_7_P	A45	S1_PCIERCA3_RX_7_P
B46	GND	A46	GND
B47	S1_PCIERCA3_TX_6_N	A47	S1_PCIERCA3_RX_6_N
B48	S1_PCIERCA3_TX_6_P	A48	S1_PCIERCA3_RX_6_P
B49	GND	A49	GND
B50	S1_PCIERCA3_TX_5_N	A50	S1_PCIERCA3_RX_5_N
B51	S1_PCIERCA3_TX_5_P	A51	S1_PCIERCA3_RX_5_P
B52	GND	A52	GND
B53	S1_PCIERCA3_TX_4_N	A53	S1_PCIERCA3_RX_4_N
B54	S1_PCIERCA3_TX_4_P	A54	S1_PCIERCA3_RX_4_P
B55	GND	A55	GND
B56	S1_PCIERCA3_TX_3_N	A56	S1_PCIERCA3_RX_3_N
B57	S1_PCIERCA3_TX_3_P	A57	S1_PCIERCA3_RX_3_P
B58	GND	A58	GND
B59	S1_PCIERCA3_TX_2_N	A59	S1_PCIERCA3_RX_2_N
B60	S1_PCIERCA3_TX_2_P	A60	S1_PCIERCA3_RX_2_P
B61	GND	A61	GND
B62	S1_PCIERCA3_TX_1_N	A62	S1_PCIERCA3_RX_1_N
B63	S1_PCIERCA3_TX_1_P	A63	S1_PCIERCA3_RX_1_P
B64	GND	A64	GND
B65	S1_PCIERCA3_TX_0_N	A65	S1_PCIERCA3_RX_0_N
B66	S1_PCIERCA3_TX_0_P	A66	S1_PCIERCA3_RX_0_P
B67	GND	A67	GND
B68	S1_PCIERCA3_A2_SCL	A68	CLK100M_S1_RCA3_A2_REF_N
B69	S1_PCIERCA3_A2_SDA	A69	CLK100M_S1_RCA3_A2_REF_P
B70	S1_PCIERCA3_2_PRSNT_4C_L	A70	GND

TE: 2327679-3			
Pin #	Pin Definition	Pin #	Pin Definition
B1	GND	A1	GND
B2	S1_PCIERCA2_TX_0_P	A2	S1_PCIERCA2_RX_0_P
B3	S1_PCIERCA2_TX_0_N	A3	S1_PCIERCA2_RX_0_N
B4	GND	A4	GND
B5	S1_PCIERCA2_TX_1_P	A5	S1_PCIERCA2_RX_1_P
B6	S1_PCIERCA2_TX_1_N	A6	S1_PCIERCA2_RX_1_N
B7	GND	A7	GND
B8	S1_PCIERCA2_TX_2_P	A8	S1_PCIERCA2_RX_2_P
B9	S1_PCIERCA2_TX_2_N	A9	S1_PCIERCA2_RX_2_N
B10	GND	A10	GND
B11	S1_PCIERCA2_TX_3_P	A11	S1_PCIERCA2_RX_3_P
B12	S1_PCIERCA2_TX_3_N	A12	S1_PCIERCA2_RX_3_N
B13	GND	A13	GND
B14	S1_PCIERCA2_1_PRSNT_L	A14	S1_PCIERCA2_RX_4_P
B15	CON_S1_RCA20_PERST_L	A15	S1_PCIERCA2_RX_4_N
B16	GND	A16	GND
B17	S1_PCIERCA2_TX_4_P	A17	S1_PCIERCA2_RX_5_P
B18	S1_PCIERCA2_TX_4_N	A18	S1_PCIERCA2_RX_5_N
B19	GND	A19	GND
B20	S1_PCIERCA2_TX_5_P	A20	S1_PCIERCA2_RX_6_P
B21	S1_PCIERCA2_TX_5_N	A21	S1_PCIERCA2_RX_6_N
B22	GND	A22	GND
B23	S1_PCIERCA2_TX_6_P	A23	S1_PCIERCA2_RX_7_P
B24	S1_PCIERCA2_TX_6_N	A24	S1_PCIERCA2_RX_7_N
B25	GND	A25	GND
B26	S1_PCIERCA2_TX_7_P	A26	GND
B27	S1_PCIERCA2_TX_7_N	A27	S1_PCIERCA2_1_PRSNT_1C_L
B28	GND	A28	GND

Table 7 PCIE x24 Riser Connector Pin Definition

7.5.2.3. Sliver connector for PCIe U.2 NVMe backplane and Pin Definition

Figure 8 TE: 2332139-3 Pin:140

SLIV 1, 2, 3, 4			
Pin #	Pin Definition	Pin #	Pin Definition
B1	+12V	A1	GND
B2	+12V	A2	GND
B3	+12V	A3	GND
B4	+12V	A4	GND
B5	+12V	A5	GND
B6	+12V	A6	GND
B7	+12V	A7	PCIE_SCL
B8	+12V	A8	PCIE_SDA
B9	PCIE_WAKE_L	A9	+3V3
B10	PERST_L	A10	+3V3
B11	+3V3_SB	A11	PERST_L
B12	SLIV_X_INT_L	A12	PCIE_PRSNT_1C_L
B13	GND	A13	GND
B14	CLK100M_P	A14	BACKPLANE_HP_1_SCL
B15	CLK100M_N	A15	BACKPLANE_HP_1_SDA
B16	GND	A16	GND
B17	PCIE_TX_0_P	A17	PCIE_RX_0_P
B18	PCIE_TX_0_N	A18	PCIE_RX_0_N
B19	GND	A19	GND
B20	PCIE_TX_1_P	A20	PCIE_RX_1_P
B21	PCIE_TX_1_N	A21	PCIE_RX_1_N
B22	GND	A22	GND
B23	PCIE_TX_2_P	A23	PCIE_RX_2_P
B24	PCIE_TX_2_N	A24	PCIE_RX_2_N
B25	GND	A25	GND
B26	PCIE_TX_3_P	A26	PCIE_RX_3_P
B27	PCIE_TX_3_N	A27	PCIE_RX_3_N
B28	GND	A28	GND
B29	GND	A29	GND
B30	PCIE_TX_4_P	A30	PCIE_RX_4_P
B31	PCIE_TX_4_N	A31	PCIE_RX_4_N
B32	GND	A32	GND
B33	PCIE_TX_5_P	A33	PCIE_RX_5_P
B34	PCIE_TX_5_N	A34	PCIE_RX_5_N
B35	GND	A35	GND
B36	PCIE_TX_6_P	A36	PCIE_RX_6_P
B37	PCIE_TX_6_N	A37	PCIE_RX_6_N
B38	GND	A38	GND
B39	PCIE_TX_7_P	A39	PCIE_RX_7_P
B40	PCIE_TX_7_N	A40	PCIE_RX_7_N
B41	GND	A41	GND
B42	PCIE_PRSNT_2C_L	A42	PERST_L
B43	GND	A43	GND
B44	PCIE_TX_0_P	A44	PCIE_RX_0_P
B45	PCIE_TX_0_N	A45	PCIE_RX_0_N
B46	GND	A46	GND
B47	PCIE_TX_1_P	A47	PCIE_RX_1_P
B48	PCIE_TX_1_N	A48	PCIE_RX_1_N
B49	GND	A49	GND
B50	PCIE_TX_2_P	A50	PCIE_RX_2_P
B51	PCIE_TX_2_N	A51	PCIE_RX_2_N
B52	GND	A52	GND
B53	PCIE_TX_3_P	A53	PCIE_RX_3_P
B54	PCIE_TX_3_N	A54	PCIE_RX_3_N
B55	GND	A55	GND
B56	PCIE_TX_4_P	A56	PCIE_RX_4_P
B57	PCIE_TX_4_N	A57	PCIE_RX_4_N
B58	GND	A58	GND
B59	PCIE_TX_5_P	A59	PCIE_RX_5_P

SLIV 5, 6			
Pin #	Pin Definition	Pin #	Pin Definition
B1	+12V	A1	GND
B2	+12V	A2	GND
B3	+12V	A3	GND
B4	+12V	A4	GND
B5	+12V	A5	GND
B6	+12V	A6	GND
B7	+12V	A7	PCIE_SCL
B8	+12V	A8	PCIE_SDA
B9	PCIE_WAKE_L	A9	+3V3
B10	PERST_L	A10	+3V3
B11	+3V3_SB	A11	PERST_L
B12	SLIV_X_INT_L	A12	PCIE_PRSNT_1C_L
B13	GND	A13	GND
B14	CLK100M_P	A14	BACKPLANE_HP_1_SCL
B15	CLK100M_N	A15	BACKPLANE_HP_1_SDA
B16	GND	A16	GND
B17	PCIE_TX_7_N	A17	PCIE_RX_7_N
B18	PCIE_TX_7_P	A18	PCIE_RX_7_P
B19	GND	A19	GND
B20	PCIE_TX_6_N	A20	PCIE_RX_6_N
B21	PCIE_TX_6_P	A21	PCIE_RX_6_P
B22	GND	A22	GND
B23	PCIE_TX_5_N	A23	PCIE_RX_5_N
B24	PCIE_TX_5_P	A24	PCIE_RX_5_P
B25	GND	A25	GND
B26	PCIE_TX_4_N	A26	PCIE_RX_4_N
B27	PCIE_TX_4_P	A27	PCIE_RX_4_P
B28	GND	A28	GND
B29	GND	A29	GND
B30	PCIE_TX_3_N	A30	PCIE_RX_3_N
B31	PCIE_TX_3_P	A31	PCIE_RX_3_P
B32	GND	A32	GND
B33	PCIE_TX_2_N	A33	PCIE_RX_2_N
B34	PCIE_TX_2_P	A34	PCIE_RX_2_P
B35	GND	A35	GND
B36	PCIE_TX_1_N	A36	PCIE_RX_1_N
B37	PCIE_TX_1_P	A37	PCIE_RX_1_P
B38	GND	A38	GND
B39	PCIE_TX_0_N	A39	PCIE_RX_0_N
B40	PCIE_TX_0_P	A40	PCIE_RX_0_P
B41	GND	A41	GND
B42	PCIE_PRSNT_2C_L	A42	PERST_L
B43	GND	A43	GND
B44	PCIE_TX_7_N	A44	PCIE_RX_7_N
B45	PCIE_TX_7_P	A45	PCIE_RX_7_P
B46	GND	A46	GND
B47	PCIE_TX_6_N	A47	PCIE_RX_6_N
B48	PCIE_TX_6_P	A48	PCIE_RX_6_P
B49	GND	A49	GND
B50	PCIE_TX_5_N	A50	PCIE_RX_5_N
B51	PCIE_TX_5_P	A51	PCIE_RX_5_P
B52	GND	A52	GND
B53	PCIE_TX_4_N	A53	PCIE_RX_4_N
B54	PCIE_TX_4_P	A54	PCIE_RX_4_P
B55	GND	A55	GND
B56	PCIE_TX_3_N	A56	PCIE_RX_3_N
B57	PCIE_TX_3_P	A57	PCIE_RX_3_P
B58	GND	A58	GND
B59	PCIE_TX_2_N	A59	PCIE_RX_2_N

B60	PCIE_TX_5_N	A60	PCIE_RX_5_N
B61	GND	A61	GND
B62	PCIE_TX_6_P	A62	PCIE_RX_6_P
B63	PCIE_TX_6_N	A63	PCIE_RX_6_N
B64	GND	A64	GND
B65	PCIE_TX_7_P	A65	PCIE_RX_7_P
B66	PCIE_TX_7_N	A66	PCIE_RX_7_N
B67	GND	A67	GND
B68		A68	PERST_L
B69		A69	
B70	PCIE_PRSNT_4C_L	A70	

B60	PCIE_TX_2_P	A60	PCIE_RX_2_P
B61	GND	A61	GND
B62	PCIE_TX_1_N	A62	PCIE_RX_1_N
B63	PCIE_TX_1_P	A63	PCIE_RX_1_P
B64	GND	A64	GND
B65	PCIE_TX_0_N	A65	PCIE_RX_0_N
B66	PCIE_TX_0_P	A66	PCIE_RX_0_P
B67	GND	A67	GND
B68		A68	PERST_L
B69		A69	
B70	PCIE_PRSNT_4C_L	A70	

Table 8 Sliver Connector Pin Definitions

7.5.2.4. PCIe x8 Riser Connector and Pin definition

Figure 9 TE: 2331813-3 PIN: 84

7.5.2.5. OCPv3 NIC Connector and Pin definition

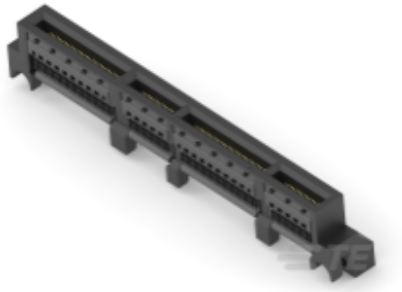

Figure 10 TE: 1-2340321-2 PIN: 168

7.5.2.6. PCIe M.2 NGFF Connector and Pin definition

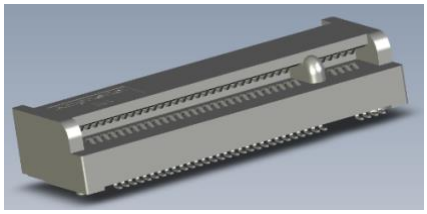

Figure 11 AMPHENOL: MDT420M01001 PIN: 75

7.5.3. Mt.Jade PCIE Riser Cards

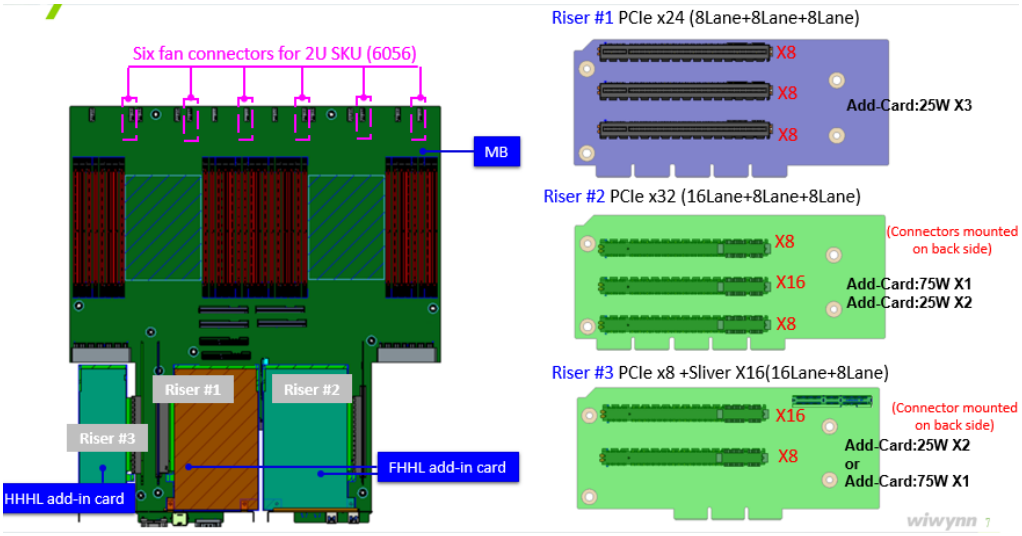

Figure 12 Mt. Jade 2U Riser Cards

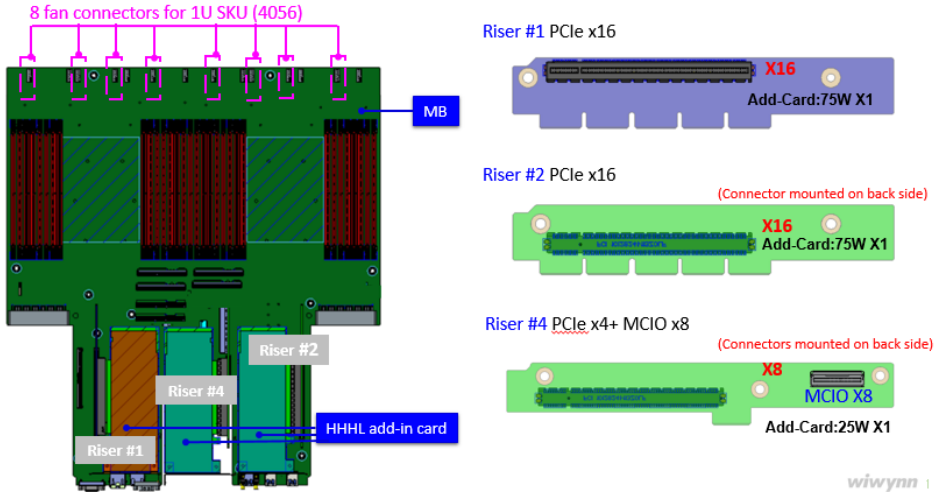

Figure 13 Mt. Jade 1U Riser Cards

7.6. Management Subsystem

7.6.1. BMC

The primary functions of BMC on Mt.Jade Motherboard are:

- IPMI2.0 support for remote management
- IPMB support for chassis management
- System power control
- System Event Log
- Sensor monitoring (voltage/power, temperature, PSU)
- Fan control (fail detection, speed monitor & control)
- Serial Over Lan
- Asset Information (FRU)
- Auto recovery from hang (Watchdog)
- Remote KVM and Media

Mt.Jade BMC is designed with AST2500 of which system is configured with 512MB DDR4-2400 SDRAM, two 64MB SPI flash memories for BMC boot, 32GB eMMC storage, x1 Gen2 PCIE port for VGA, ten I2C ports and GPIO pins for system management, 1GbE management ETH port for network, UARTs for console and debug, USB for KVM/Redfish support, PWM/TACH for FAN control, and ADC for power fail monitoring. The Table 9 shows BMC configuration.

INTERFACES	BMC CONFIGURATION
Memory	512MB DDR4 memory with ECC support
PCIe	1x PCIe x1 Gen2 port for VGA control
VGA	1x VGA port with 1920x1028 resolution
SPI	2x 256Mb SPI flash for BMC boot, one for main and the other for fail-save, BMC's SYS_SPI is connected to MB to program/upgrade Altra / AltraMax FW
Storage	1x 32GB eMMC device (optional use)
I2C	2x I2C ports (I2C3: Master, I2C1: Slave) for in-band/out-of-band communication with CPU 1x I2C port (I2C2) for access program/upgrade system boot EEPROM 1x I2C port (I2C4) for current, temperature monitoring, FRU access 1x I2C port (I2C5) for RTC access 1x I2C port (I2C6) for PCIe sideband signals 1x I2C port (I2C7) for PSU access 1x I2C port (I2C9) for TPM 2x I2C ports (I2C12/I2C13) for DDR4 SPD EEPROM access
Network	- x1 10/100/1000Mbps management LAN from BMC's ETH - x1 10/100 RMII interface as NCSI for OCPv3 NIC
UART	x1 DB9 (TX/RX) for BMC's console (BMC_UART5) BMC_UART1 is connected to S0_UART0 for Altra / AltraMax system console (UEFI/OS) BMC_UART2 is connected to S0_UART3 for Altra / AltraMax SCP FW console output BMC_UART3 is connected to S0_UART4 for Altra / AltraMax ATF FW console output BMC_UART4 is connected to S1_UART3 for Altra / AltraMax SCP FW console output
USB	USB2A is connected directly to PCIe-USB bridge chip for KVM & Redfish support
GPIO	Refer ***section*** for GPIO pin assignments.

INTERFACES	BMC CONFIGURATION
ADC	Monitors 15 power rails of motherboard
PWM/TACH	8 fans for 1U & 6 fans for 2U systems
JTAG	x1 BMC's JTAG slave port for AST2500 debug. x1 BMC's JTAG master port to program CPLD or to debug Altra / AltraMax

Table 9 BMC AST2500 Configuration

7.6.2. I2C Network

Mt.Jade MB has many I2C devices onboard such as voltage regulator devices, EEPROMs (boot, DDR4 SPD, FRU), Temperature sensors, RTC, PSU, and PCIe backplane controllers & PCIe I2C side band signals. Also, Altra/AltraMax processor uses I2C interfaces to communicate with BMC.

There are several groups of I2C devices are connected to Altra/AltraMax and/or BMC:

- Voltage Regulator Devices
- EEPROMs (Boot, DDR4-DIMM SPD, FRU)
- CPU and BMC IPMI communication
- PCIe IO-expanders, and NVMe drives for OOB management
- Temperature sensors, PSU, RTC, and TPM

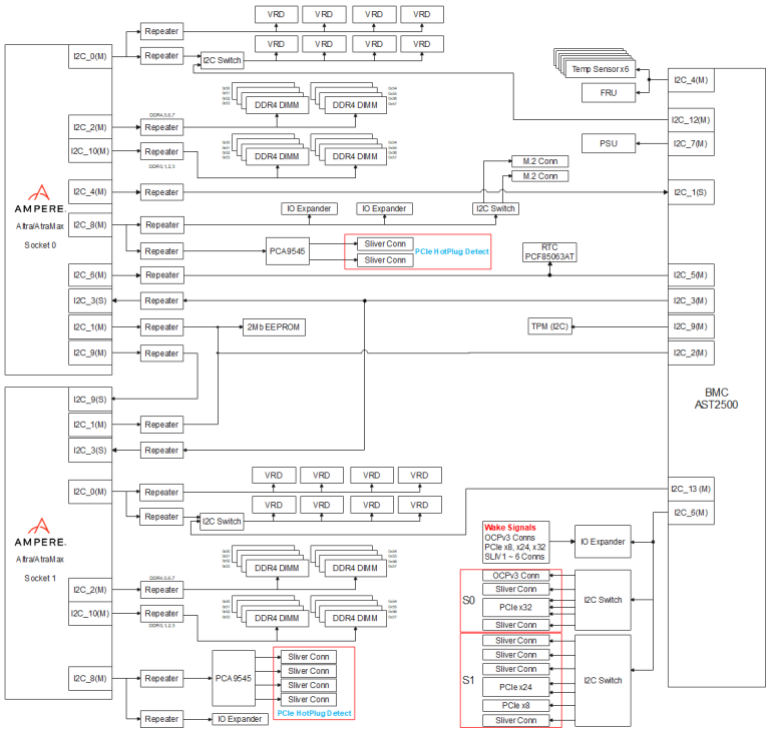

Figure 14 Mt.Jade I2C Network Diagram

7.6.2.1. I2C connection of voltage regulator devices

Altra / AltraMax processor uses I2C_0 controller to access VRDs via PMBus commands. BMC uses I2C_12 and I2C_13 controllers to access on VRDs for high power rails, VDD_PCP / VDDQ_0123 / VDDQ_4567 / VDD_SOC / VDD_RCA, through I2C switch. However, BMC is allowed to access the VRDs only when Altra / AltraMax processor is in power-down state. BMC FW should manage the VRD access control.

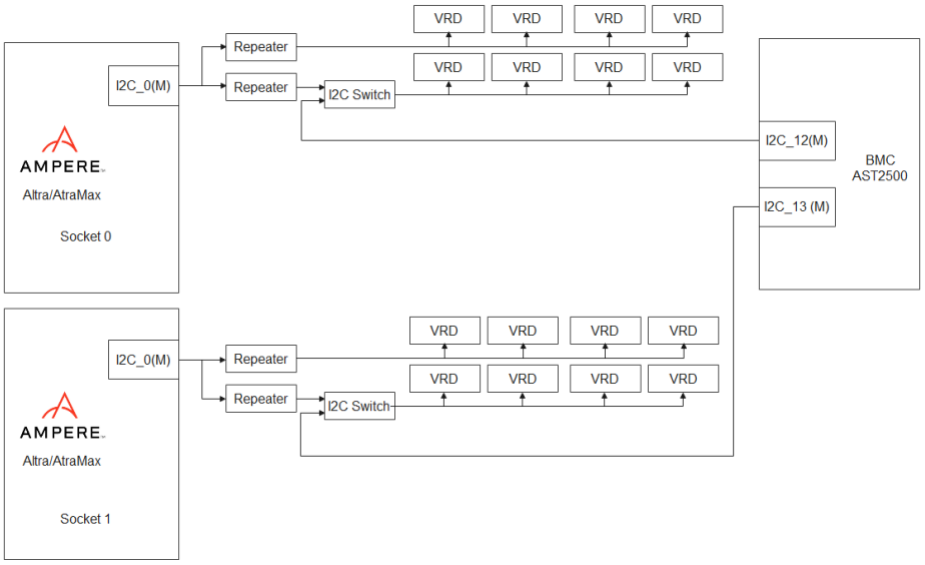

Figure 15 Mt.Jade I2C network of voltage regulators

7.6.2.2. I2C connection of Altra/AltraMax Boot EEPROM

I2C Boot EEPROM is accessed by Altra/AltraMax processors in Master/Slave socket as well as BMC. The BMC accesses the EEPROM only when the FW needs to be updated after BMC powers off both processors in Master/Slave sockets. When system powers on, the processor in Master socket will access the boot EEPROM first and the processor in Slave socket will wait for the processor in Master socket to send message to the processor in Slave socket through I2C_9 bus after the FW loading is done by the processor in Master socket. The processor in Master socket will proceed the 2P boot process after the message from the processor in Slave socket received.

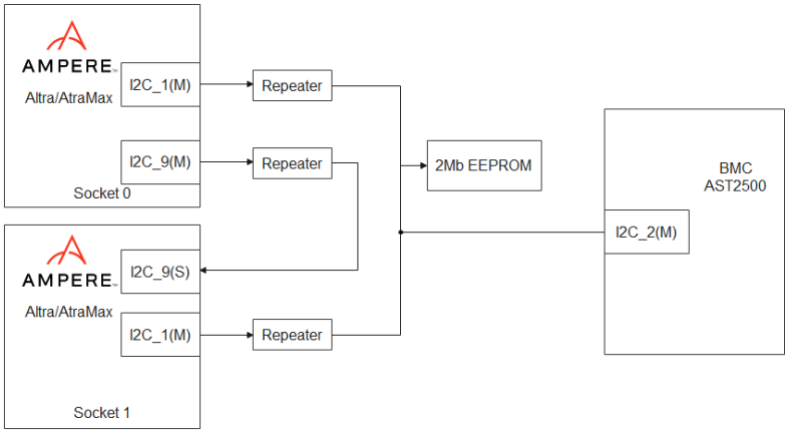

Figure 16 Mt.Jade I2C network of Boot EEPROM

7.6.2.3. I2C connection of DIMM SPDs

Two I2C controllers, I2C_2 and I2C_10, in Altra/AltraMax processor are used to access the DIMM SPD EEPROMs. 4 DDR channels form a group of which SPD EEPROMs are attached to dedicated I2C controller, which allows to use same I2C addresses for the SPD EEPROM on each DIMM groups, S0_DDR4_0/1/2/3, S0_DDR4_4/5/6/7, S1_DDR4_0/1/2/3, S1_DDR4_4/5/6/7.

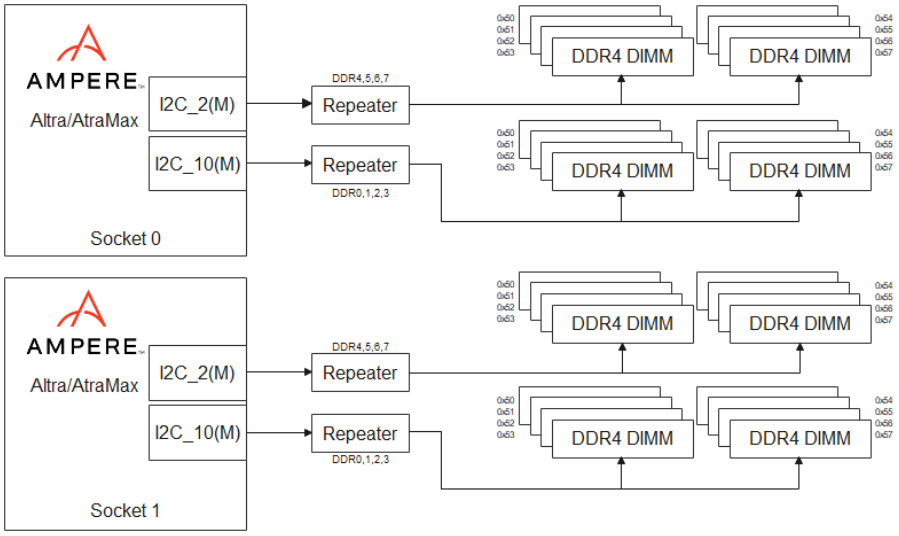

Figure 17 Mt.Jade I2C network of DIMM SPDs

7.6.2.4. I2C connection between CPU and BMC

Altra/AltraMax and BMC communicates via asymmetric I2C connectivity. When CPU sends requests to BMC, the requests will be sent from the I2C_4 of the CPU

in socket 0 as master port to the I2C_1 of the BMC as slave port. However, when BMC sends requests to CPU, the requests will be sent from the I2C_3 of the BMC as master port to the I2C_3 slave port, either the one in Socket 0 or the other in Socket 1.

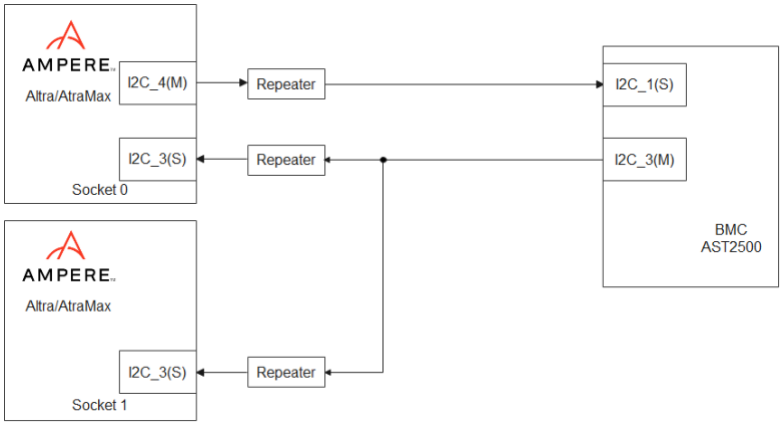

Figure 18 Mt.Jade I2C connection between CPU and BMC

7.6.2.5. I2C connections for PCIe NVMe hot plug & OOB management, PCIE sideband signals

Figure 19 shows I2C connections for PCIE NVMe hot-plug and sideband signals for PCIE devices. The I2C_8 interface of Altra/AltraMax processor is connected to I/O expander on NVMe backplane to support hot-plug feature. And BMC I2C_6 interface is connected to PCIe sideband signals to support Wake signals and NVMe OOB management.

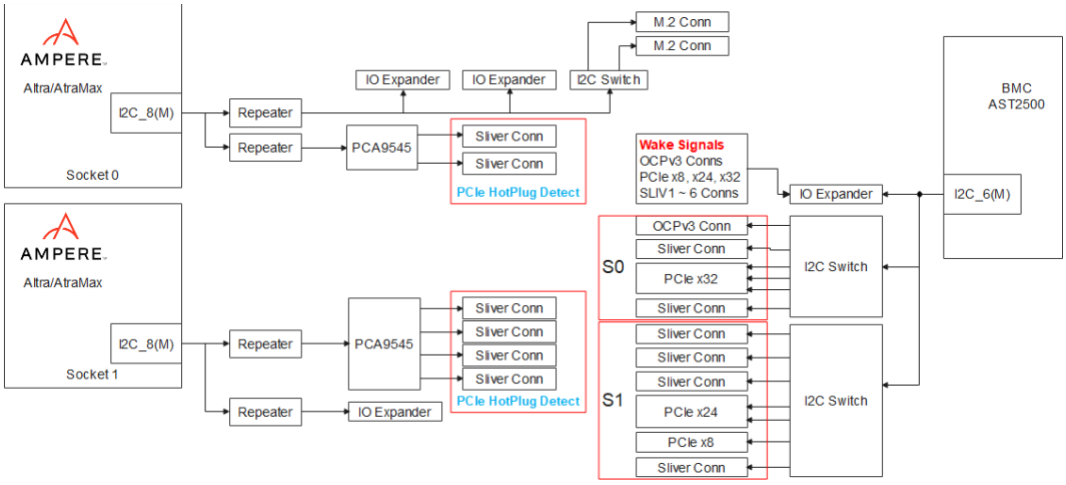

Figure 19 Mt.Jade I2C connections for PCIE NVMe hot-plug and management

7.6.2.6. Miscellaneous I2C devices

Temperature sensors, FRU, and PSU devices are connected to BMC. The RTC device is connected to Altra/AltraMax processor and BMC.

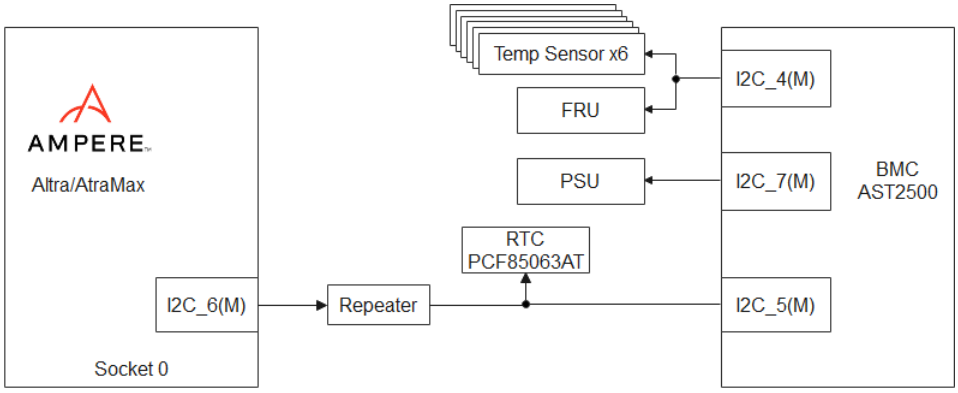

Figure 20 Mt.Jade Miscellaneous I2C devices such as temp-sensors, FRU, PSU, and RTC

7.7. Debug Interfaces

Mt.Jade MB has several dedicated JTAG headers:

- 2x10 header for BMC JTAG port for BMC FW debug
- 1x8 header for CPLD JTAG port, debug & CPLD image update purpose
- 2x10 and 2x5 header for Altra/AltraMax JTAG ports, JTAG_DAP and JTAG_SOC

By default, the CPLD JTAG slave port is connected to 1x8 header for CPLD Programmer, the BMC JTAG port is configured as slave and connected to 2x10 header for BMC JTAG debugger. BMC FW can configure the JTAG port as master and set GPIOM2 pin to connect the BMC JTAG port to CPLD JTAG slave port for updating CPLD image.

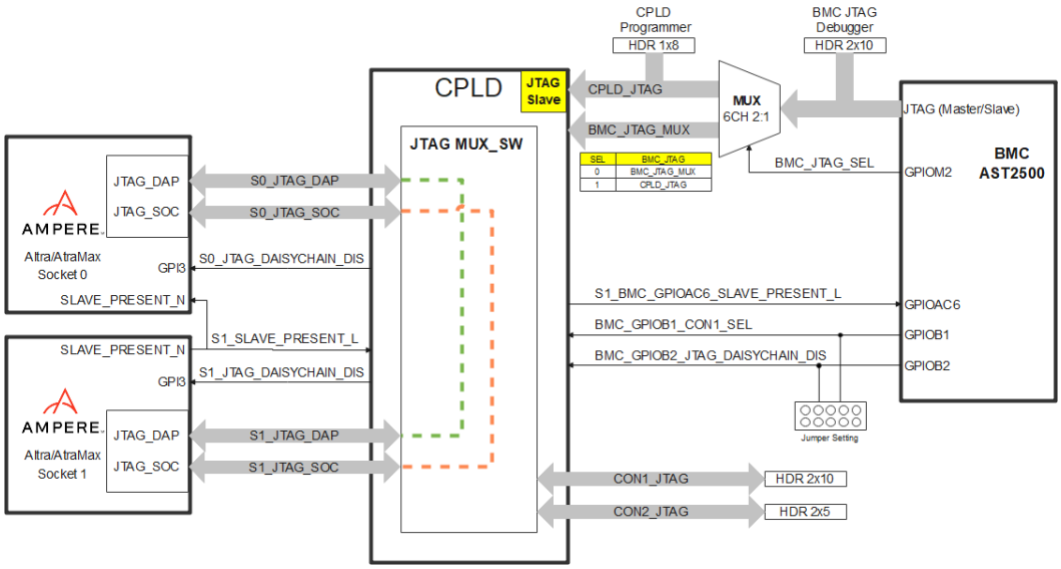

Figure 21 Mt.Jade JTAG Connectivity among CPU/CPLD/BMC

Altra/AltraMax JTAG ports are daisy-chained through internal mux and switches in CPLD and mapped to two external headers for JTAG debugger connection when the CPUs are populated on both sockets though S1_SLAVE_PRESENT_L signal. When CPU is installed only on Socket 0, CPLD will break the daisy-chain and connect Altra/AltraMax JTAG ports on Socket 0 to two external headers.

7.8. GPIOs

Figure 22 shows the connections between Altra / AltraMax and BMC GPIO pins. The CPLD provides simple voltage isolation since they're in different power rails. The detail definition of GPIO pins can be found in Table 10 and Table 11.

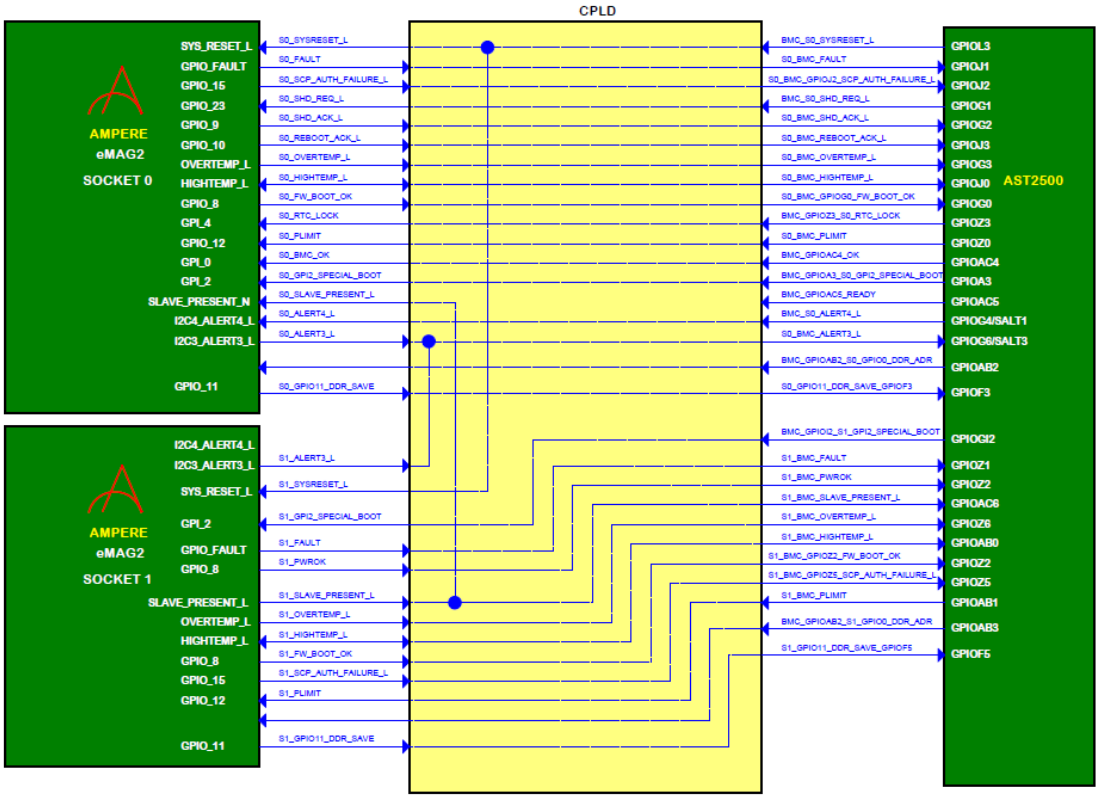

Figure 22 Mt.Jade GPIO mapping between Altra / AltraMax and BMC

Group	Pin name	Pin #	I/O	Signal Name	Description
GPIO	GPIO_0	AK2	I, FLOATING	S0_GPIO_0	TEST POINT
	GPIO_1	AJ3	I, PU 4.7K	S0_GPIO_1	TEST POINT
	GPIO_2	AK4	I, PU 4.7K	S0_GPIO2_RTC_INT_L	Interrupt from RTC to S0 , active LOW
	GPIO_3	AJ5	I/O, FLOATING	S0_SPARE_S_GPIO	Connect to BMC via CPLD - Reserved for future use
	GPIO_4	AJ7	I, PD 10K	S0_GPIO4_BIOS_RECOVER	S0 BIOS Recovery - Reserved for future use
	GPIO_5	AK8	I/O, FLOATING	S0_GPIO5_RSVD	Connected to CPLD - Reserved for future use
	GPIO_6	AJ9	I/O, FLOATING	S0_GPIO6_RSVD	Connected to CPLD - Reserved for future use
	GPIO_7	AK10	I/O, FLOATING	CPU0_SPI_AUTH_FAIL_L	S0 SPI Authorization Fail
	GPIO_8	AJ11	O, PD 10K	S0_FW_BOOT_OK	S0 SMpro boot OK, active HIGH connect to BMC via CPLD
	GPIO_9	AJ13	O, PU 4.7K	S0_SHD_ACK_L	S0 acknowledge " graceful shutdown ", active LOW connected to BMC via CPLD
	GPIO_10	AK14	O, PU 4.7K	S0_REBOOT_ACK_L	S0 software reboot acknowledge, active LOW connected to BMC via CPLD

	GPIO_11	AJ15	O, PD 10K	S0_GPIO11_DDR_SAVE	S0 memory SAVE mode control by CPU, active HIGH Connected to DIMM&BMC - Reserved for future use
	GPIO_12	AK16	I, PD 10K	S0_PLIMIT	S0 power limit, active HIGH Request from BMC
	GPIO_13	AJ17	I, PD 10K	CPLD_S0_GPIO13_DDR_ADR	S0_DDR_ADR connected to CPLD
	GPIO_14	AJ19	I, PU 4.7K	S0_TPM_ALERT_L	TPM0,1 module alert, active LOW
	GPIO_15	AK32	O, PU 4.7K	S0_SCP_AUTH_FAILURE_L	S0 secure-boot authentication failure, active LOW connected to BMC via CPLD
	GPIO_16	AL33	O, PU 4.7K	S0_GPIO16_PCIE_RST_L	S0 PCIE reset bit 0, decode by CPLD
	GPIO_17	AL31	O, PU 4.7K	S0_GPIO17_PCIE_RST_L	S0 PCIE reset bit 1, decode by CPLD
	GPIO_18	AM30	O, PU 4.7K	S0_GPIO18_PCIE_RST_L	S0 PCIE reset bit 2, decode by CPLD
	GPIO_19	AN31	O, PU 4.7K	S0_GPIO19_PCIE_RST_L	S0 PCIE reset bit 3, decode by CPLD
	GPIO_20	AP32	O, PU 4.7K	S0_GPIO20_PCIE_RST_L	S0 PCIE reset bit 4, decode by CPLD
	GPIO_21	AT32	O, PU 4.7K	S0_GPIO21_PCIE_RST_L	S0 PCIE reset bit 5, decode by CPLD
	GPIO_22	AR31	I, PU 4.7K	S0_GPIO22_PCIE_PRSNT_L	S0 PCIE card present interrupt from IO expander, active LOW
	GPIO_23	AU31	I, PU 4.7K	S0_SHD_REQ_L	BMC request S0 a " graceful shutdown ", active LOW connected to BMC via CPLD
GPI	GPI_0	AM44	I, PU 10K	S0_BMC_OK	BMC ready, active HIGH Connect to BMC via CPLD
	GPI_1	AN45	I, PU 4.7K	S0_TPM_PRSNT_L	TPM0,1 module present, active LOW
	GPI_2	AL45	I, PD 10K	S0_GPI2_SPECIAL_BOOT	Jump to special boot mode Control by BMC
	GPI_3	AM46	I, FLOATING	S0_JTAG_DSYCHN_DIS_R	This signal disable internal daisy chain of the JTAG DAPs (SMPro , PMPro , ARMv8/SOC)
	GPI_4	AN47	I., PD 10K	S0_RTC_LOCK	This signal indicates to the eMAG2 that the RTC access will be temporary restricted BMC output this signal HIGH to indicates that it needs to access the RTC
	GPI_5	AL47	I, FLOATING	S0_GPI_5	TEST POINT
	GPI_6	AL49	I, FLOATING	S0_GPI_6	TEST POINT
	GPI_7	AN49	I, FLOATING	S0_GPI_7	TEST POINT
ALERT	HIGHTEMP_N	AP40	O, PU 4.7K	S0_HIGHTEMP_L	S0 high temperature alert, active LOW connected to BMC via CPLD
	OVERTEMP_N	AN39	O, PU 4.7K	S0_OVERTEMP_L	S0 over temperature alert, BMC shutdown power immediately, active LOW connected to BMC via CPLD
	GPIO_FAULT	AM56	O, PD 4.7K	S0_FAULT_ALERT	S0 fault alert, RED LED blinking , active HIGH connected to BMC via CPLD

Table 10 GPIO Assignment Table for Master Socket

Group	Pin name	Pin #	I/O	Signal Name	Description
GPIO	GPIO_0	AK2	I, FLOATING	S1_GPIO_0	TEST POINT
	GPIO_1	AJ3	I, PU 4.7K	S1_GPIO_1	TEST POINT
	GPIO_2	AK4	I/O, FLOATING	S1_GPIO_2	TEST POINT
	GPIO_3	AJ5	I/O, FLOATING	S1_SPARE_S_GPIO	Connect to BMC via CPLD - Reserved for future use
	GPIO_4	AJ7	I, PD 10K	S1_GPIO4_BIOS_RECOVER	S1 BIOS Recovery - Reserved for future use
	GPIO_5	AK8	I/O, FLOATING	S1_GPIO_5	TEST POINT
	GPIO_6	AJ9	I/O, FLOATING	S1_GPIO_6	TEST POINT
	GPIO_7	AK10	I/O, FLOATING	S1_GPIO_7	TEST POINT
	GPIO_8	AJ11	O, PD 10K	S1_FW_BOOT_OK	S1 SMpro boot OK, active HIGH connected to BMC via CPLD
	GPIO_9	AJ13	I/O, FLOATING	S1_SHD_ACK_L	TEST POINT
	GPIO_10	AK14	I/O, FLOATING	S0_REBOOT_ACK_L	TEST POINT

	GPIO_11	AJ15	O, PD 10K	S1_GPIO11_DDR_SAVE	S1 memory SAVE mode control by CPU, active HIGH Connected to DIMM&BMC - Reserved for future use
	GPIO_12	AK16	I, PD 10K	S1_PLIMIT	S1 power limit, active HIGH Request from BMC
	GPIO_13	AJ17	I, PD 10K	CPLD_S1_GPIO13_DDR_ADR	BMC force S1 assert DDR_SAVE when detect AC power loss - Reserved for future use
	GPIO_14	AJ19	I/O, FLOATING	S1_GPIO_14	TEST POINT
	GPIO_15	AK32	O, PU 4.7K	S1_SCP_AUTH_FAILURE_L	S1 secure-boot authentication failure, active LOW connected to BMC via CPLD
	GPIO_16	AL33	O, PU 4.7K	S1_GPIO16_PCIE_RST_L	S1 PCIE reset bit 0, decode by CPLD
	GPIO_17	AL31	O, PU 4.7K	S1_GPIO17_PCIE_RST_L	S1 PCIE reset bit 1, decode by CPLD
	GPIO_18	AM30	O, PU 4.7K	S1_GPIO18_PCIE_RST_L	S1 PCIE reset bit 2, decode by CPLD
	GPIO_19	AN31	O, PU 4.7K	S1_GPIO19_PCIE_RST_L	S1 PCIE reset bit 3, decode by CPLD
	GPIO_20	AP32	O, PU 4.7K	S1_GPIO20_PCIE_RST_L	S1 PCIE reset bit 4, decode by CPLD
	GPIO_21	AT32	O, PU 4.7K	S1_GPIO21_PCIE_RST_L	S1 PCIE reset bit 5, decode by CPLD
	GPIO_22	AR31	I, PU 4.7K	S1_GPIO22_PCIE_PRSNT_L	S1 PCIE card present interrupt from IO expander, active LOW
	GPIO_23	AU31	I/O, FLOATING	S1_GPIO_23	TEST POINT
GPI	GPI_0	AM44	I, FLOATING	S1_GPI_0	TEST POINT
	GPI_1	AN45	I, FLOATING	S1_GPI_1	TEST POINT
	GPI_2	AL45	I, PD 10K	S1_GPI2_SPECIAL_BOOT	Jump to special boot mode Control by BMC
	GPI_3	AM46	I, FLOATING	S1_JTAG_DSYCHN_DIS_R	This signal disable internal daisy chain of the JTAG DAPs (SMPro , PMPro , ARMv8/SOC)
	GPI_4	AN47	I., PD 10K	S1_GPI_4	TEST POINT
	GPI_5	AL47	I, FLOATING	S1_GPI_5	TEST POINT
	GPI_6	AL49	I, FLOATING	S1_GPI_6	TEST POINT
	GPI_7	AN49	I, FLOATING	S1_GPI_7	TEST POINT
ALERT	HIGHTEMP_N	AP40	O, PU 4.7K	S1_HIGHTEMP_L	S1 high temperature alert, active LOW connected to BMC via CPLD
	OVERTEMP_N	AN39	O, PU 4.7K	S1_OVERTEMP_L	S1 over temperature alert, BMC shutdown power immediately, active LOW connected to BMC via CPLD
	GPIO_FAULT	AM56	O, PD 4.7K	S1_FAULT_ALERT	S1 fault alert, RED LED blinking , active HIGH connected to BMC via CPLD

Table 11 GPIO Assignment Table for Slave Socket

7.9. Boot Devices

The below three devices are used for the system boot:

- Microchip AT24CM02 2Mbit I2C EEPROM for Altra/AltraMax SCP FW
- Macronix MX25L25673G 256Mbit QSPI flash for Altra/AltraMax ATF/BIOS FW
- Macronix MX66L51235FMI-10G 512Mbit SPI flash for BMC AST2500 FW

The Figure 23 shows the boot devices connectivity between Altra / AltraMax processors and BMC. Two single bit SPI flash memories are attached to BMC, one for main boot device and the other for failover one.

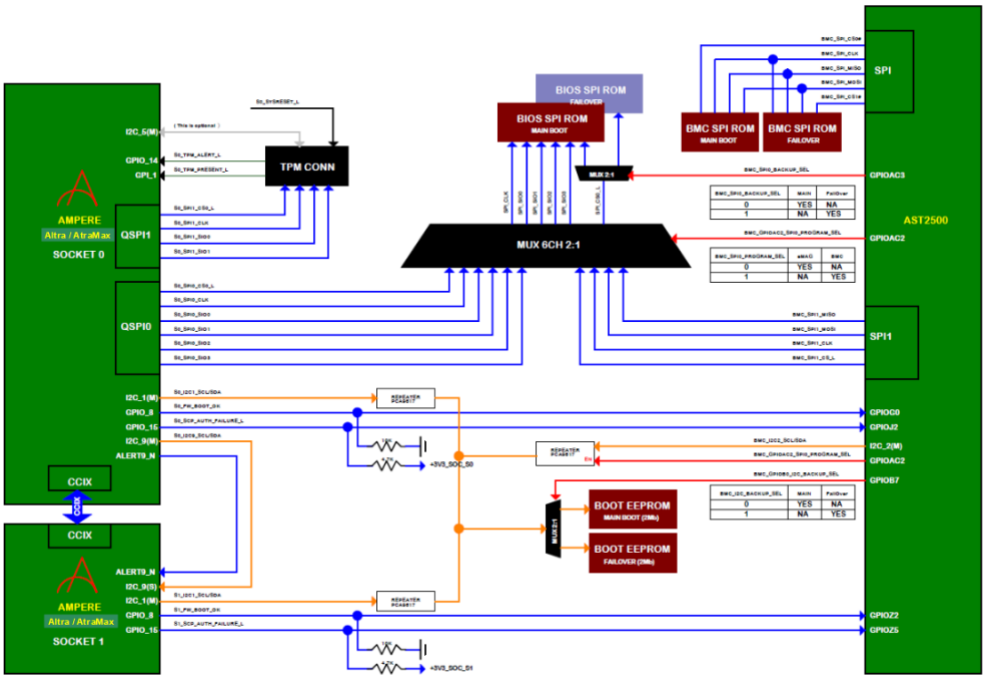

Figure 23 Boot EEPROM, SPI Flash, and TPM for Altra / AltraMax and BMC

Two I2C EEPROMs are connected to both Altra / AltraMax processors and BMC through the 2:1 MUX. Both processors in master/slave sockets share the I2C bus to access the boot EEPROM. The processor in master socket accesses the I2C EEPROM first at power-on and release the I2C bus for the processor in slave socket to access the I2C EEPROM after sending the message to the processor in slave socket through the dedicated I2C connection between the processors.

BMC monitors Altra / AltraMax processor boot process. If boot process fails, BMC uses GPIO pin to switch I2C boot EEPROM from main-boot device to failover one and reboot the processors. BMC also accesses the I2C boot EEPROM for FW update after both processors in master/slave sockets power off.

Not like I2C EEPROM, two QSPI flash memories, main-boot and failover devices, are shared between Altra / AltraMax processor in master socket and BMC. While Altra / AltraMax processor fetches codes from flash memory in QSPI mode, BMC updates FW to flash memory in single bit SPI mode. Similar like I2C boot EEPROM, BMC switches the SPI flash CS signal from main-boot device to failover one though MUX controlled by GPIO pin. Also, BMC uses GPIO and MUX to gain access to the SPI flash memory for FW update.

7.10. Clocks, Reset, and Power-on Sequence

7.10.1. Clocks

Figure 24 shows clock sources on Mt.Jade motherboard.

Renesas (IDT) 9FGV1006B 2-output clock generator chip provides Altra / AltraMax processors 100MHz PCIE Gen4 compliant clock without SSC as system reference clock and serdes reference clock for 25G CCIX 2P link.

Renesas (IDT) 9FGL0841 8-output clock generator and 92XL1231 12-output clock buffer chip provide 100MHz PCIE Gen4 compliant clock for Altra / AltraMax processors, onboard PCIE devices, PCIE riser cards, OCPv3 NIC connector, and Sliver connectors for NVMe drives as common reference clock.

Renesas (IDT) 5P35023 programmable clock generator provides the several reference clocks, 50MHz/24MHz/125MHz, for BMC and 50MHz for OCPv3 NIC connector.

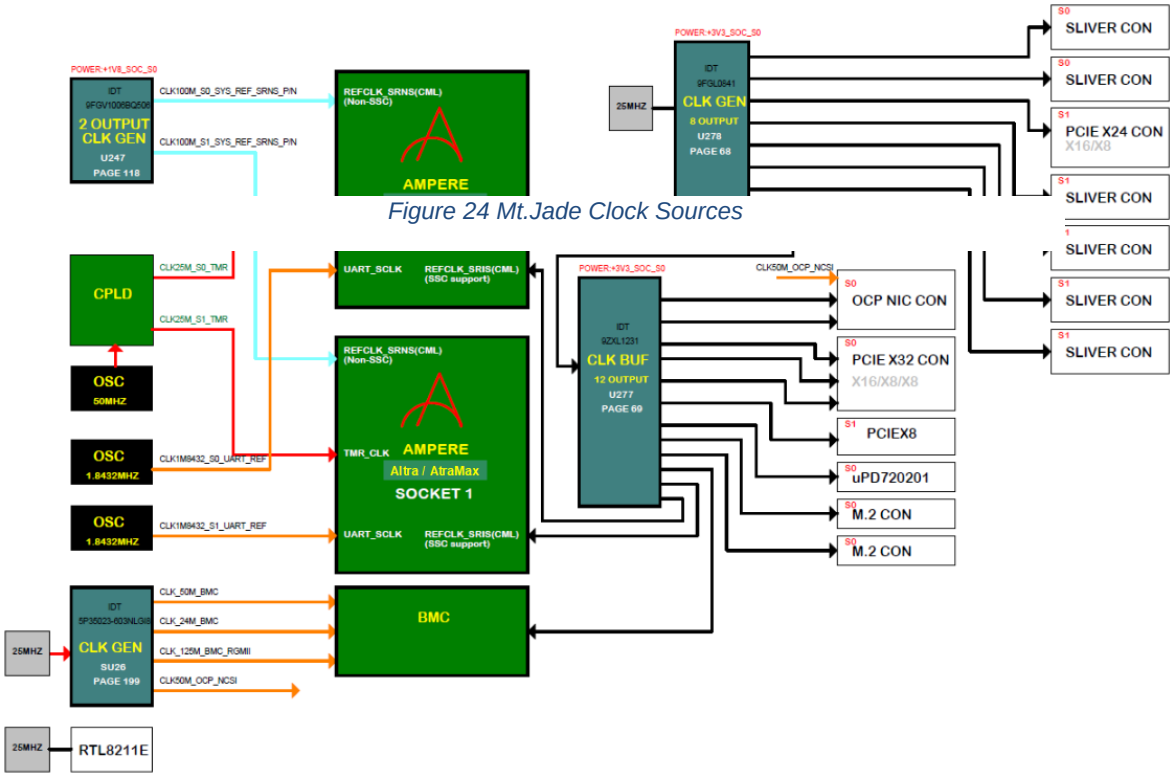

Figure 24 Mt.Jade Clock Sources

CPLD takes 50MHz clock from oscillator and generates two 25MHz synchronous clocks to feed the processors in Master/Slave sockets as global timer clock.

Two 1.8432MHz oscillators are connected to Altra / AltraMax processors as UART serial clock sources to set UART baud rate to 115200 bps.

25MHz crystals are used as input clock sources for Renesas (IDT) 5P35023, Renesas (IDT) 9FGL0841, and RTL8211E BMC Ethernet PHY chip.

7.10.2. Reset

Several reset signals are connected between Altra / AltraMax processors, BMC, and PCIE devices on Mt.Jade MB:

- SYS_RESET_L – Input reset signal for Altra / AltraMax processor which will reset entire chip. This signal is controlled by BMC FW through BMC_GPIO and CPLD. The BMC FW will toggle the SYS_RESET signal for Altra / AltraMax processors either by IPMI command or by SYS_RESET button on board
- SRST_L – Input reset signal for BMC AST2500 which can be triggered by BMC_RESET button on board. The BMC_REST signal resets Ethernet PHY and eMMC devices attached to BMC
- DDR[7:0]_RESET_L – output reset signal generated by Altra / AltraMax processor to reset DDR4 devices. This reset signal is directly connected to DIMM connectors
- MRESET_L – output reset signal generated by BMC to reset DDR4 SDRAM attached to BMC
- PERST signals – output signals to reset the PCIE devices. PERST signal for specific PCIE port is generated through CPLD from the 6 GPIO pins controlled by Altra / AltraMax FW

Figure 25 shows the reset signal connections among Altra / AltraMax processors, BMC, and CPLD.

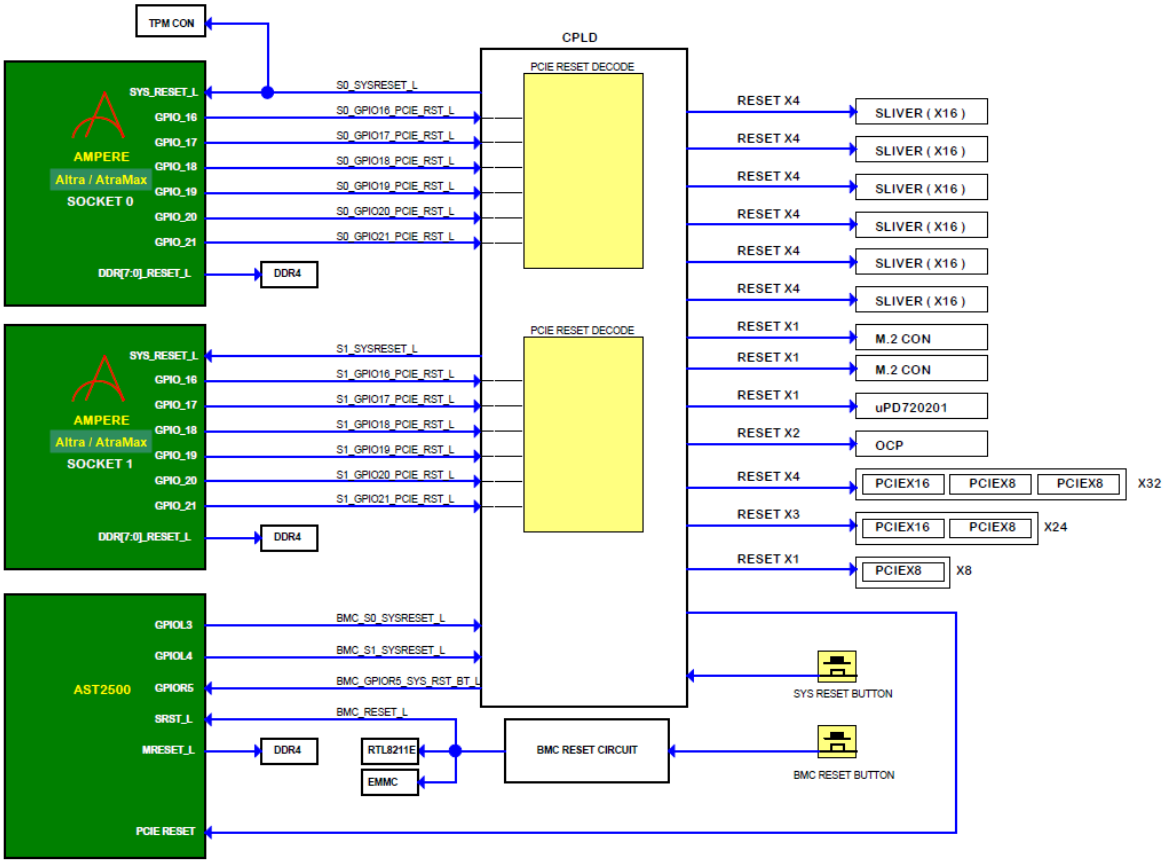

Figure 25 Mt.Jade Reset Signals

7.10.3. Power-on Sequence

Figure 26 shows the Altra / AltraMax processor power-on sequence for 2 socket platform where ALERT9_N signal, which is supposed to trigger the execution of socket1 FW, is directly connected between processors in master/slave sockets.

First, socket0 (master socket) power rails will be turned on in order of VDD_SOC, VDD_RCAx, VDD1V8_SOC, VDDH_RCAx, VDDH_RCBx, VDDQ_DDR0123/4567, VDD3V3_SOC. The SOC_PWRGD of socket0, S0_SOC_PWRGD, will be asserted after more than 32 system clock cycles. The same power-on sequence should be applied to socket1 (slave socket).

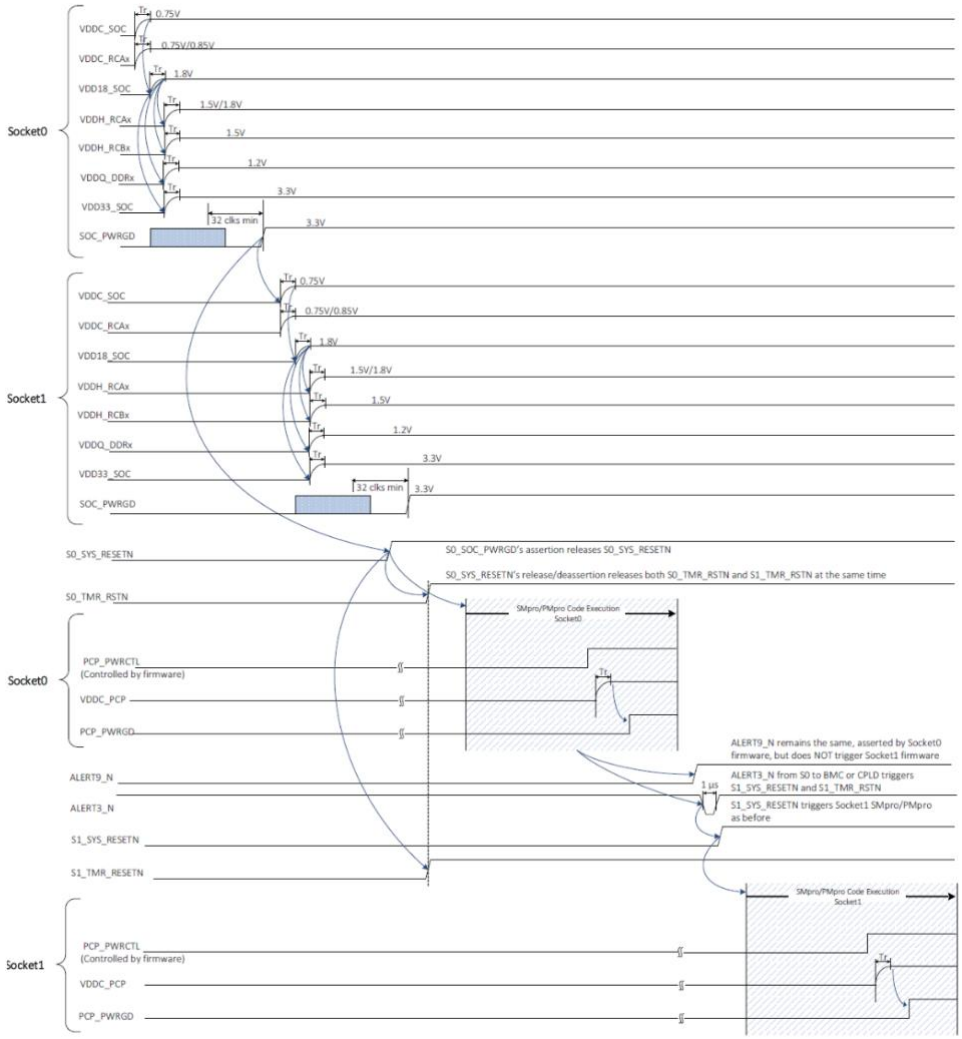

Figure 26 Altra / AltraMax Power-on Sequence

The S0_SOC_PWRGD signal assertion will release S0_SYS_RESETN signal and the S0_SYS_RESETN signal will release both S0_TMR_RESETN and S1_TMR_RESETN signals. Once S0_SYS_RESETN signal is released, socket0 FW starts and turns on the S0_VDD_PCP power rail. After the S0_PCP_PWRGD signal is detected, socket0 FW will assert S0_ALERT9_N signal and toggle S0_ALERT3_N signal with 1usec delay so that CPLD will release the S1_SYS_RESETN after detecting ALERT9_N assertion and 1usec pulse in ALERT3_N signal which will make the socket1 FW start reliably to turn on S1_VDD_PCP power rail.

8. Thermal Design Requirements

Table 12 lists the thermal resistance values for the package along with the maximum operating junction temperature, the thermal throttling and shutdown temperature for Altra and AltraMax processors. The θ_{JC}, T_{CJ}, TM1, and TM2 values in the table are varied depending on SKU.

Parameter	Symbol	Altra	AltraMax
Junction-to-case thermal resistance[1,2]	θ_{JC}	0.12	0.075
Maximum continuous operating junction temperature[3]	T_{CJ} (C)	100	100
SoC thermal throttling temperature[3]	TM1 (C)	105	105
SoC thermal shut down temperature[3]	TM2 (C)	120	
Storage temperature range[4]	T_{STG}	-55 to +150	
Operating junction temperature range[4]	T_J	0 to +125	

Notes:
1. Case temperature TC is measured at top center of lid with device seated in ILM4926 socket.
2. θ_{JC} is measured based on boundary conditions of the reference thermal solution and all power is assumed to dissipate from package to thermal solution.
3. TCJ as specified in this table is for use as a system thermal design guideline. The SoC can run continuously at this temperature. To achieve maximum performance, ensure that the thermal solution can maintain TCJ at this value.
In case of operational or cooling failures, the following built-in mechanism in firmware will protect the SoC from a thermal runaway or getting damaged:
   – HIGHTEMP_N (TM1): The SoC temperature at which thermal throttling will be triggered. The CPU frequency is throttled down in steps of 50 MHz.
   – OVERTEMP_N (TM2): The SoC temperature at which a shutdown will be triggered. The entire SoC is powered off under this condition.
4. This value is not a specification of the operational temperature range; it is a stress rating only.

Table 12 Altra / AltraMax Thermal Specification

9. I/O System

10. Rear Side Power, I/O and Midplane

Figure 27 shows the rear side power and I/O when Mt.Jade MB is installed in 1U chassis and Figure 28 shows the same when the Mt.Jade MB is installed in 2U chassis.

The power supply and bottom side I/O are common between 1U and 2U chassis where BMC UART/ETH/VGA ports, OCPv3 NIC connector, PWR/RST/UID buttons and 2x USB3.0 type-A connectors are located.

1U system has 3 riser cards available for three x16 Gen4 low-profile PCIE devices while 2U system has 8 riser cards available for two low-profile PCIE devices and six FHHL PCIE devices.

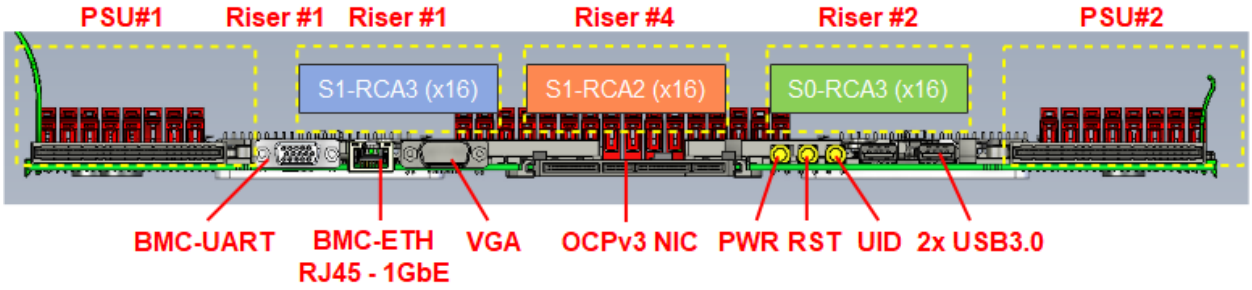

Figure 27 Mt.Jade 1U Rear Side I/O

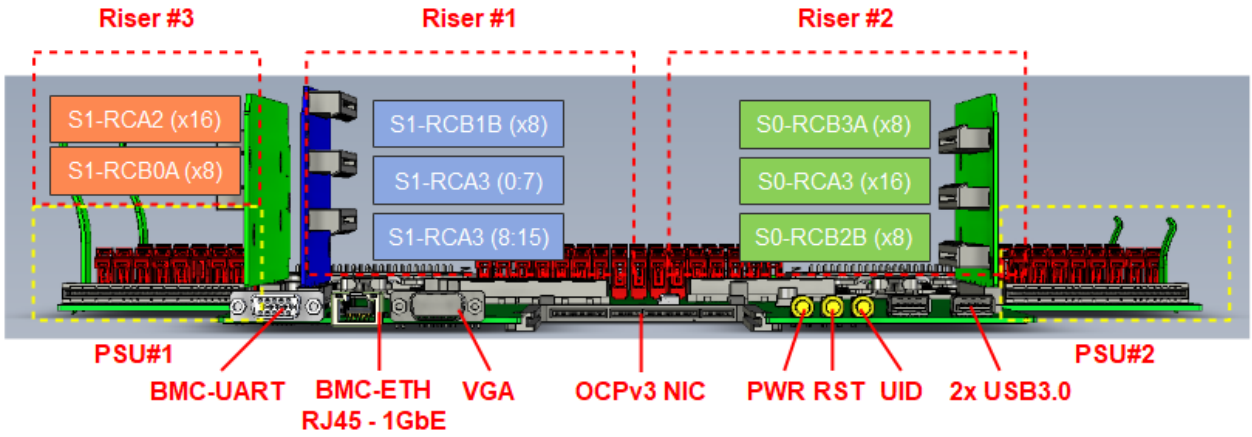

Figure 28 Mt.Jade 2U Rear Side I/O

11. Rack Implementation

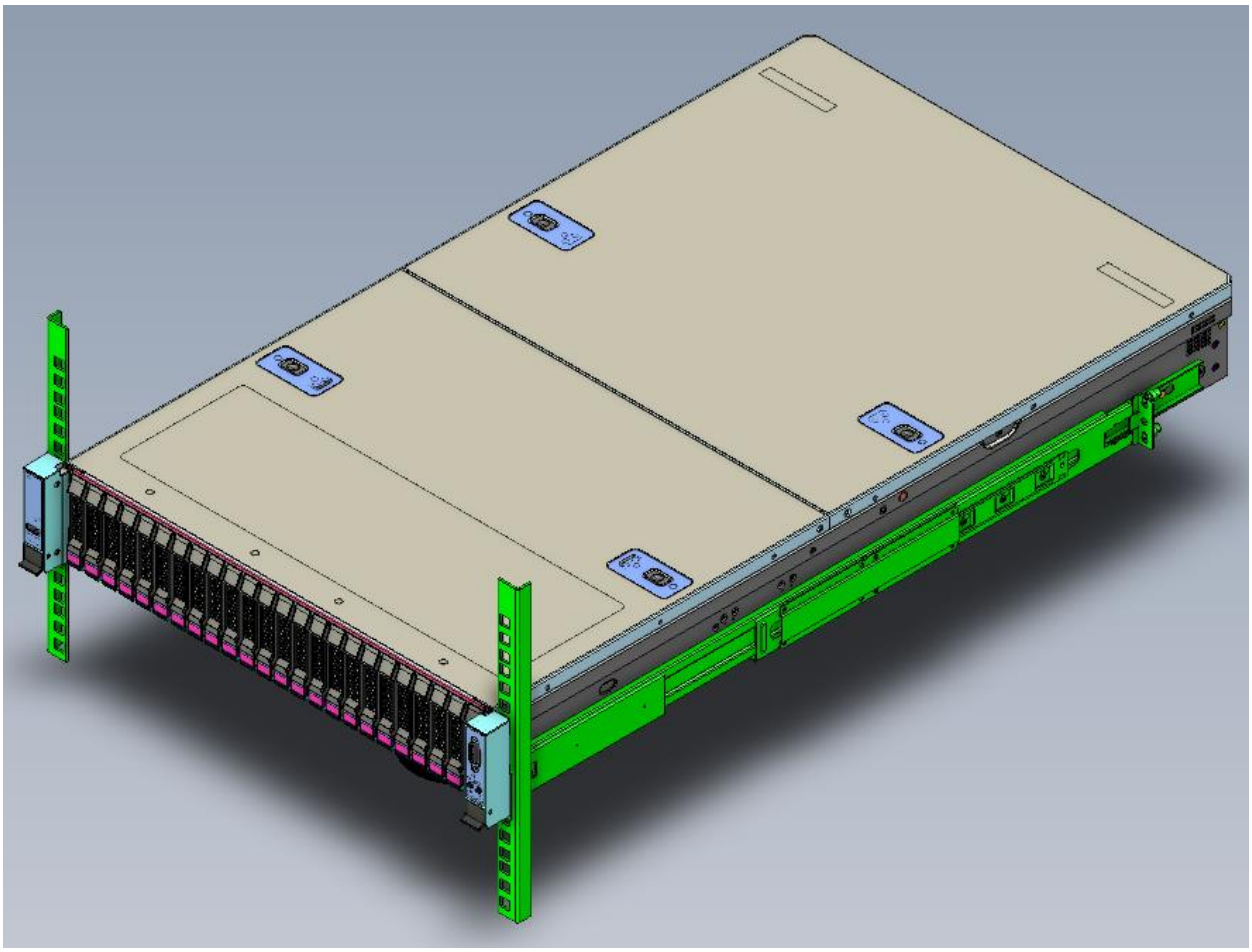

Figure 29 Mt.Jade 3D - 2U System Rack Mount View

12. Mechanical

Figure 30 is 3D isometric view of Mt.Jade motherboard and the below is the high lights of Mt.Jade in mechanical point of view.

- CPU and heat sink
  - ILM4926 socket is soldered on Mt.Jade motherboard to hold CPU
  - 1U & 2U heat sink can be mounted on top of the socket
- DIMMs
  - Standard DDR4 DIMM connectors
- OCPv3 NIC
  - Two guard rails to hold the OCPv3 NIC card along with 4C connector
  - Chassis supports latch or screw based
- PCIE riser cards
  - There are cages with latch and screw to hold the riser cards
- FAN
  - Two sets of FAN connectors which are aligned with hot-swappable FAN cage connectors
- CPRS PSU
  - Two connectors are located left and right side
  - PSU is supported by latch on chassis
- Cable clips
  - Two long cable clips for 4 Sliver cables on the edge of motherboard near slave socket
  - Two short cable clips for 2 Sliver cables on edge of motherboard near master socket side

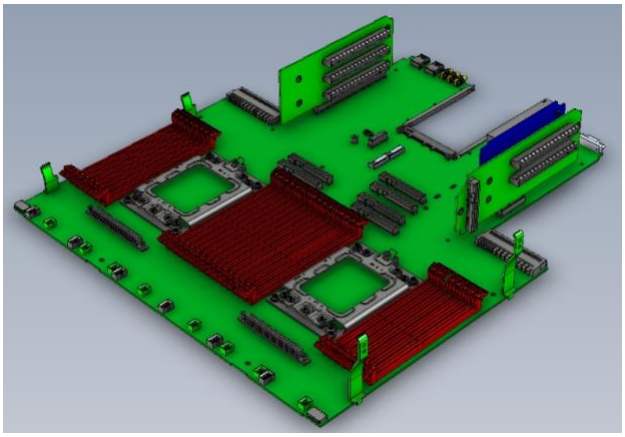

Figure 30 Mt.Jade Motherboard 3D - Isometric View

Figure 31, Figure 32, Figure 33 shows the mechanical connection of x32/x24/x8 2U riser cards on Mt.Jade MB. There are mechanical cages to provide mechanical support for the riser cards as chassis accessories. The details of mechanical specification of the riser card cages won't be covered in this document since it belongs to chassis specification.

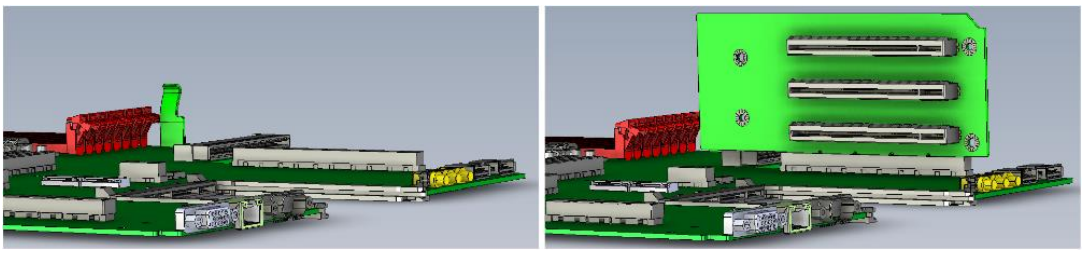

Figure 31 Mt.Jade Motherboard 3D - x32 Riser Card

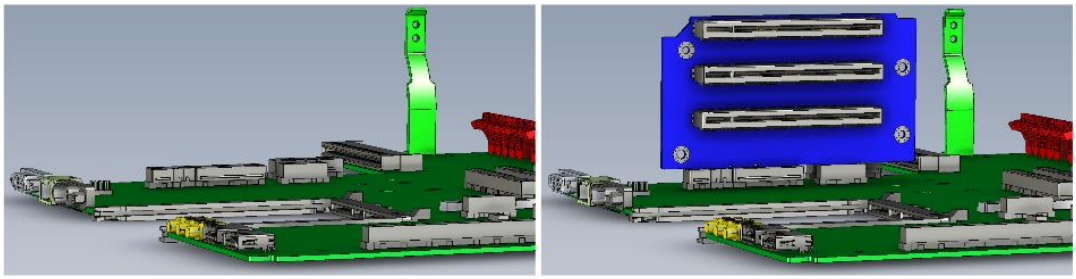

Figure 32 Mt.Jade Motherboard 3D - x24 Riser Card

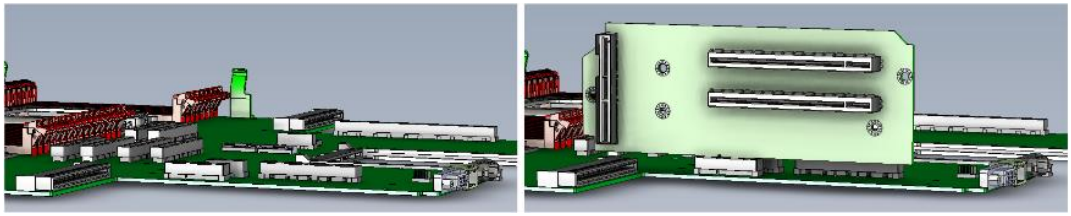

Figure 33 Mt.Jade Motherboard 3D - x8 Riser Card

13. Motherboard Power System

13.1. Altra / AltraMax Power Specification

The Table 13 contains estimated power and currents for the Altra and AltraMax processors. The TDP, I_{PCP}, $I_{PCP(Max)}$ values in the table are varied depending on SKU.

Parameter	Symbol	Altra	AltraMax
Thermal Design Power[1]	TDP (W)	210	250
PCP active (continuous) operating current[2]	I_{PCP} (A)	200	240
PCP maximum operating current[3]	$I_{PCP(Max)}$ (A)	300	420
0.75V SoC (VDD_SOC) active operating current	I_{SOC} (A)	22.17	24
0.75 V RCB active operating current (VDDC_RCB[0:3]/VDDC_RCA[4:7])	I_{C_RCB} (A)	4	
0.90 V RCA active operating current (VDDC_RCA[0:3])	I_{C_RCA} (A)	16	16
1.5 V RCB active operating current (VDDH_RCB[0:3]/VDDC_RCA[4:7])	I_{H_RCB} (A)	4	4
1.8 V RCA active operating current (VDDH_RCA[0:3])	I_{H_RCA} (A)	5	5
1.2 V DDR4 active operating current (VDDQ_DDR0123, VDDQ_DDR4567)	I_{DDRQ} (A)	10	10
1.8 V DDR4 supply active operating current (VDD18_DDR_AVDD)	I_{DDR} (A)	0.5	1
1.8 V SerDes active operating current (VDD18_SERDES_AVDD)	I_{SERDES} (A)	0.5	0.5
1.8 V SOC active operating current (VDD18_SOC)	I_{O18} (A)	0.5	1
1.8 V PCP active operating current (VDD18_PCP_AVDD)	I_{PCP18} (A)	0.5	1
3.3 V SOC active operating current (VDD33_SOC)	I_{O33} (A)	1	1

Notes:
1. Power measured at nominal voltage and max recommended operating temperature.
2. PCP active (continuous) operating current is estimated at the highest frequency with TDP and TCJ per SKU as specified in *Table 12* with best-case process part.
3. PCP maximum operating current is estimated at the maximum frequency per SKU, with TCJ per SKU as specified in *Table 12* with best-case process part (which drives worst-case power). For hot-swap controller OCP calculations, use VDDC_PCP = 1.1 V.

Table 13 Altra / AtraMax DC Power Supply Loads

13.2. Mt.Jade Power Delivery Block Diagram

Mt.Jade power system is designed to support the Altra / AltraMax processors, based on the power specification described in the Table 13, BMC sub-system including fans, and the PCIe devices which are connected to PCIe riser cards, OCPv3 connectors, and M.2 connectors. The Figure 34 shows the detail connections of Mt.Jade power rails.

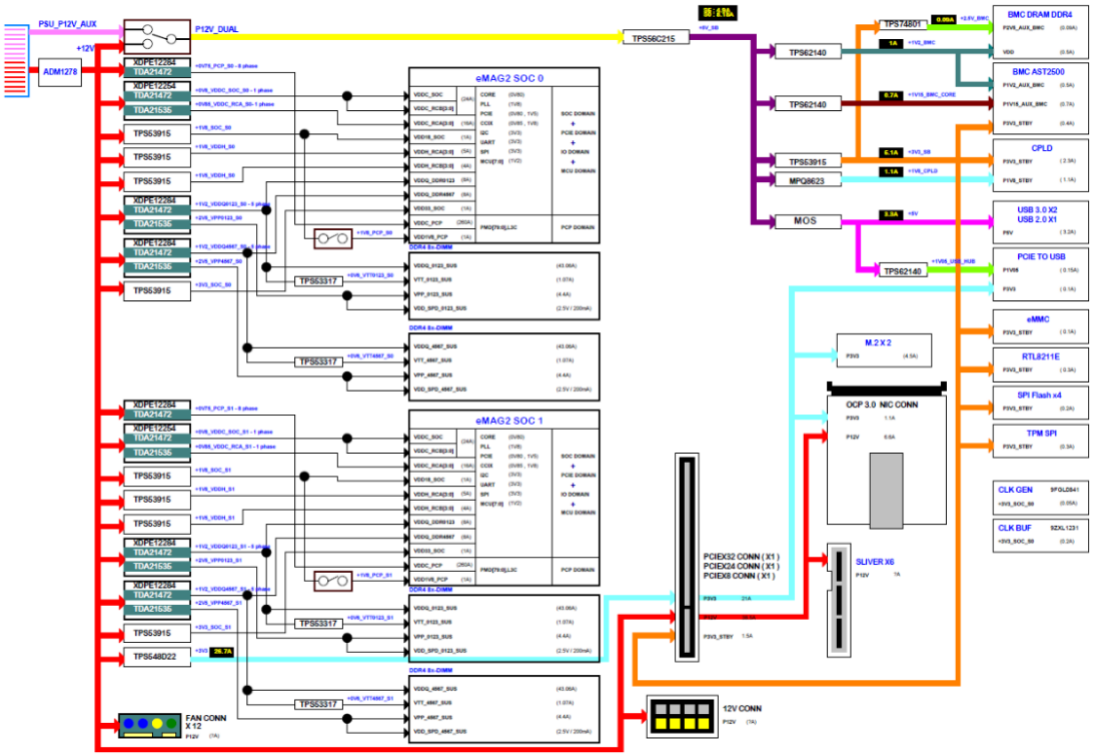

Figure 34 Mt.Jade Power Delivery Block Diagram

There are four high power domains for Altra / AltraMax processors:

- PCP power domain for CPU cores and mesh interconnects
- SoC power domain for SoC blocks, memory and PCIe controllers
- RCA power domain for PCIe/CCIX controllers
- DDR4 power domain for memory IOs and DIMMs

And there are several power rails, 1.5/1.8/2.5/3.3 volts, for IO domains

Infineon voltage regulators, XDPE12284 and XDPE12254, are used for these high-power domains along with TDA21472 and TDA21535 power stages. Both VRD's are PMBus™ system interface rev 1.2 compliant for telemetry of voltage, current, power, temperature, and fault conditions. Also, they support dynamic output voltage transitions with programmable slew rates via PMBus interface with 100kHz ~ 400kHz frequency.

For other power rails of the Altra / AltraMax processors, TI TPS53915 voltage converter is used except for VTT power rail where TI TPS53317 voltage converter is used.

BMC sub-system needs 1.05/1.15/1.2/2.5V and 3.3V power rails. TI TPS56C215 voltage converter is used to covert 12V AUX power to 5V stand-by power which is converted into 1.05/1.15/1.2V power by TI TPS62140 and 2.5/3.3V power by TI TPS53915 voltage converters. Also, TI TPS74801 is used to convert 3.3V SB power rail to 2.5V power rail for BMC DDR4 device and Monolithic Power System's MPQ8623 voltage converter is used to step-down 3.3V SB power to 1.8V power for CPLD device.

PCIE peripherals need 3.3V and 12V power. The 3.3V power is converted from 12V main power by TI TPS548D22 to support up to 21A. The PCIE 12V power is directly connected from power supply.

The configuration of the voltage regulators and converters are listed below.

13.2.1. XDPE12284C - VRD for VDDC_PCP Power Rail

One channel (8-Phase) multiphase controller per processor, 8-phases along with 9x TDA21472 power stages support up to 420A as max current.

XDPE12284C + 8xTDA21472	
SMBus Address (7-Bit)	0x60
Loop configuration	8+0
Loop A Fsw	600Khz
Loop A Vboot – VDDC_PCP	0.75V
DC+AC Ripple	+/- 5%
Loop A Loadline	0
Loop A Iccmax	420A
Load Step	130A
Loop A IOCP	464A

Table 14 XDPE12284C Configuration for VDD_PCP Power Rail

13.2.2. XDPE12254 – VRD for VDDC_SOC and VDDC_RCA Power Rails

One dual-channel multiphase controller per processor, one phase is used for VDDC_SOC along with 1x TDA21472 power stage supporting up to 24A and the other phase for VDDC_RCA paired with 1x TDA21535 power stage supporting up to 16A.

XDPE12254A + 1xTDA21472/TDA21535	
SMBus Address (7-Bit)	0x58
Loop configuration	1+1
Loop A/B Fsw	600Khz
Loop A Vboot – VDDC_SOC	0.8V
DC+AC Ripple	+/- 5%
Loop A Iccmax	25A
Load Step	12A
Loop A IOCP	38A
Loop B Vboot – VDDC_RCAx	0.85V
DC+AC Ripple	+/- 5%
Loop B Iccmax	16A
Load Step	7A
Loop B IOCP	25A

Table 15 XDPE12254A Configuration for VDD_SOC and VDD_RCA Power Rail

13.2.3. XDPE12284B – VRD for VDDQ_DDR* and VPP_DDR*

One dual-channel (4-Phase + 1-Phase) multiphase controller for 4 DDR4 channels, 4-phases along with 4x TDA21472 power stages support up to 200A as max current and the other phase with TDA21535 power stage supports 15A as max current for DIMMs' VPP power. This design requires total 2 sets of 1x XDPE12284B controller, 4x TDA21472 and 1x TDA21535 power stages to support for 8 DDR4 channels with 32 DIMMs.

XDPE12284B + 5xTDA21472/TDA21535	
SMBus Address (7-Bit)	0x68
Loop configuration	5+1
Loop A/B Fsw	600Khz
Loop A Vboot – VDDQ	1.2V
DC+AC Ripple	+/- 5%
Loop A Iccmax	200A
Load Step	100A
Loop A IOCP	250A
Loop B Vboot – VPP	2.5V
DC+AC Ripple	+/- 5%
Loop B Iccmax	15A
Load Step	8A
Loop B IOCP	25A

Table 16 XDEP12284B Configuration for VDDR Power Rail

13.2.4. TPS53915 – Voltage Converter for VDD18_SOC, VDDH_RCA, VDDH_RCB, VDD33_SOC Power Rails

Small-sized synchronous buck converter supporting 12A continuous output current. It supports voltage margin and adjustment through PMBus command. TPS553915 is used for VDD18_SOC, VDDH_RCB, VDDH_RCA, and VDD33_SOC power rails of Altra / AltraMax processor. It is also used to convert 5V stand-by power to 3.3V stand-by power for BMC and peripherals.

Power Rails	VDD18_SOC	VDDH_RCB	VDDH_RCA	VDD33_SOC	3V3_SB
SMBus Address (7-Bit)	0x1E	0x1C	0x1D	0x1B	N/A
Fsw	400Khz				
Vout	1.8V	1.5V	1.8V	3.3V	3.3V
Imax	4A	4A	6A	2A	7A
IOCP	7A	7A	8A	3.5A	9A
DC+AC Ripple	+/- 5%				

Table 17 TPS53915 Configuration for VDD18_SOC, VDDH_RCA, VDDH_RCB, VDD33_SOC Power Rails

13.2.5. TPS548D22 – Voltage Converter for 3.3V SB Power Rail

Compact single buck converter supporting 40A continuous output current, used to convert 5V stand-by power to 3.3V stand-by power for BMC peripherals and PCIE risers.

Vout	3.3V
Ripple	+/- 0.5%
AC+DC TOB	+/- 5%
Itdc	22A
Imax	26.7A
OCP	34A
Iout step	1A
Iout slew rate	1A/uS
Fsw	650Khz

Table 18 TPS548D22 Configuration for PCIE 3.3V Power Rail

13.2.6. TPS56C215 – Voltage Converter for 5V Stand-By Power Rail

Monolithic 12A synchronous buck converter supporting 12A continuous output current, used to convert 12V_AUX power from PSU to 5V stand-by power for BMC and PCIE devices in stand-by power domain.

Vout	5V
Ripple	+/- 1%
AC+DC TOB	+/- 5%
Itdc	7A
Imax	8.18A

OCP	13A
Iout step	1A
Iout slew rate	1A/uS
Fsw	800Khz

Table 19 TPS56C215 Configuration for 5V Stand-By Power Rails

13.2.7. TPS62140 – Voltage Converter for 1.05/1.15/1.2V Power Rails

Easy-to-use synchronous step-down DC-DC converter with maximum 2A output current with adjustable output voltage from 0.9V to 6V. TPS62140 is used to convert 5V SB power to 1.05/1.15/1.2V SB powers for USB-Hub/BMC-Core/BMC-DDR.

Power Rails	**1V05_SB**	**1V15_SB**	**1V2_SB**
Freq	2.5MHz		
Vout	1.05V	1.15V	1.2V
Itdc	0.8A	0.68A	1.1A
Imax	2A		
IOCP	3.15A		
Tss	5ms		

Table 20 TPS62140 Configuration for 1.05/1.15/1.2V Stand-By Power Rails

14. Environmental and Regulations

15. Environmental Requirements

CE Mark International Compliance
FCC Part 15 Emissions Verification (USA & Canada)
UL / NRTL Certification (USA & Canada)

16. Prescribed Materials

[Note to author of this specification: This section should document the incremental features in the product implementation. The product must be 100% compliant with any and all features or requirements described in this baseline specification.]

17. Software Support (recommended)

17.1. Software tools to validate the Hardware design

Please list any software tools used to validate the hardware design. The tools could be related to:

- Keysight ADS
- Cadence Allegro to verify layout
- Motherboard has been manufactured in HVM environment.

18. System Firmware

All products seeking OCP Accepted™ Product Recognition must complete the Open System Firmware (OSF) Tab in the 2021 Supplier Requirements Checklist.

If based on an open bios (like AMI's Aptio-OpenEdition), a completed checklist shall be uploaded and made available on the OCP Github.
https://github.com/opencomputeproject/Hardware-Management/amperecomputing/mtjade

19. Hardware Management

19.1 Compliance

All products seeking OCP Inspired™ or OCP Accepted ™ Product Recognition shall comply with the OCP Hardware Management Baseline Profile V1.0 and provide such evidence by completing the Hardware Management Tab in the 2021 Supplier Requirements Checklist.

19.2 BMC Source Availability (if applicable)

All Products seeking OCP Accepted™ Product Recognition shall have source code and binary blobs submitted for BMC, if applicable.

The BMC management source code shall be uploaded at:
https://github.com/opencomputeproject/Hardware-Management/amperecomputing/mtjade

If the BMC is based on an open source BMC (like AMI's MegaRAC-OpenEdition), the BMC source code shall be uploaded and made available on the OCP Github.

20. Security

All products seeking OCP Inspired™ or OCP Accepted™ Product Recognition shall have a completed Security Profile in the 2021 Supplier Requirements Checklist. Whether the answer is a yes or no, the profile must be completed. For Additional Security Badges (Bronze/Silver/Gold), please fill out the Security Profile in accordance with the requirements for that level. Security Badges will be reassessed on an annual basis as requirements are subject to change.

21. References (recommended)

[1] "Title", publication year, publication journal/conference/standard, volume, pages, link to publication if available
[2] OCP Profiles - https://github.com/opencomputeproject/OCP-Profiles
[3] Redfish Interop Validator - https://github.com/DMTF/Redfish-Interop-Validator
[4] Redfish Service Validator - https://github.com/DMTF/Redfish-Service-Validator
[5] Redfish Service Conformance Check - https://github.com/DMTF/Redfish-Service-Conformance-Check

Appendix A - Requirements for IC Approval (to be completed Contributor(s) of this Spec)

List all the requirements in one summary table with links from the sections.

Requirements	Details	Link to which Section in Spec
Contribution License Agreement	Which one?	Link to Sec 1
Are All Contributors listed in Sec 1: License?	Yes	
Did All the Contributors sign the appropriate license for this spec? Final Spec Agreement/HW License?	Yes	
Which 3 of the 4 OCP Tenets are supported by this Spec?	Openness Efficiency Impact Scale	List reasons here. Openness – Mt. Jade layout is generic and will scale to many other processor providers Efficiency – the power delivery and use of platinum PSUs drives efficient power consumption in conjunction with the Ampere processors Impact – First dual socket ARM motherboard Scale – Design enables scaling to Cloud deployment in standard 19” rack
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	Wiwynn Corporation
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	Please have each Supplier fill out Appendix B.

Appendix B – OCP Supplier Information (to be provided by each Supplier of Product)

Company: Wiwynn Corporation
Contact Info: Bing Wu (bing_wu@wiwynn.com)

Product Name: Mt. Jade
Product SKU#: SV328R
Link to Product Landing Page:

Please complete the following 2021 Supplier Requirements. This link will allow you to create a copy for your product-specific requirements.

For OCP Inspired™,

- All Suppliers must be a OCP Solution Provider.
- All Suppliers must run the Hardware Management Conformance Checks and all products must meet the OCP Hardware Baseline Profile v1.0.0.
- All Suppliers must fill out a Security Profile (No Badge Level) for their product.

For OCP Accepted™, Supplier details are required.

- All Suppliers must be a OCP Solution Provider.
- All Suppliers must run the Hardware Management Conformance Checks and all products must meet the OCP Hardware Baseline Profile v1.0.0.
- All Suppliers must fill out a Security Profile (No Badge Level) for their product.
- All Products must meet the Open System Firmware requirements.
- All Products must have source code for BMC, if applicable. This must be in the OCP Github repository.

List all the requirements in one summary table with links from the sections.

Requirements	**Details**	**Links**
Which Product recognition?	OCP Accepted™ or OCP Inspired™	Provide Marketplace Link
If OCP Accepted™, who provided the Design Package?	Wiwynn Corporation	Link

2021 Supplier Requirements for your product(s)	Yes	Link