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Mission Peak Hardware System Specification

V1.0

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Table of Contents

List of Figures

List of Tables

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2. Overview

2.1 Executive Summary

The 1U Mission Peak server platform was developed with the latest technologies with up to 576TB of high-speed NF1 (NGSFF) form factor NVMe SSDs. It offers more than 5X higher capacity and 3X more IOPS than traditional flash storage solutions within the same footprint and ease of implementing this total solution in data centers.

2.2 Introduction

This document serves as the specification for the Mission Peak – NF1 reference system design. Mission Peak is a rack-mounted, all-flash-based storage server in a 1U EIA-310D (19”) form factor with Samsung NF1 devices. It is comprised of 36 X NF1 SSD drives (up to 16TB of each NF1) connected to a compute motherboard via a PLX PCIe switch fabric, dual Intel® Xeon® processors and 2X100Gbe and 2X50Gbe NIC cards. Each processor has a PCIe root complex to connect to the NICs and the PLX PCIe switches. The processors function in a fully balanced and symmetrical topology to deliver the desired bandwidth from the NF1 SSDs, as well as from NICs out the box. Mission Peak can deliver a half petabyte and 10M random read IOPs in a 1U system.

The Mission Peak platform uses the latest Intel DP Skylake baseboard architecture, but extends the PCIE port to connect with a Broadcom PCIE switch, in order to support 36 Samsung NF1 NVMe SSDs. Mission Peak also uses the latest generation of Broadcom PCIE switch PEX9797. Each PEX9797 connects X24 PCIe links from the CPU to 36 NF1 NVMe SSDs (a 64X NF1 configuration would need to be confirmed through a thermal evaluation). The two PEX9797 switches are able to support a total of 36 NF1 NVMe SSDs within a single system.

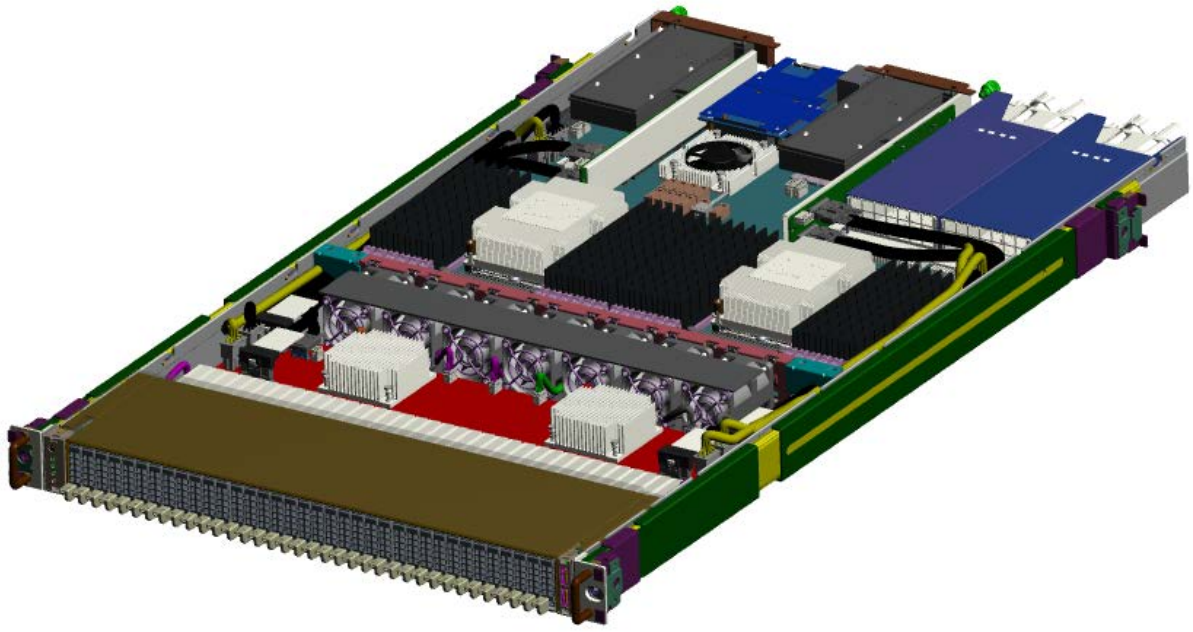


Figure 1 - Mission Peak NF1 (NGSFF) Reference Platform

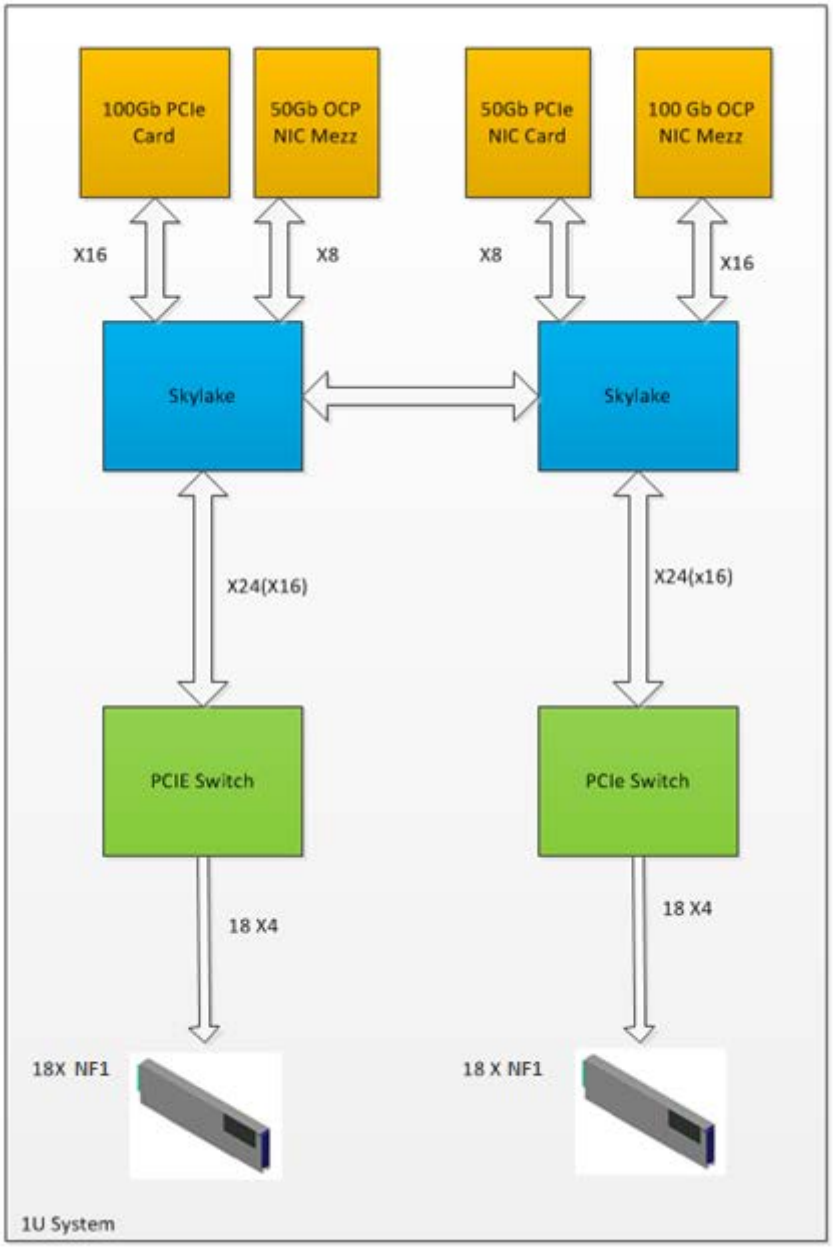


Figure 2 - NF1 (NGSFF) POC High-level System Block Diagram

Table 1 - Key Features

Feature	Description / Comments
Form Factor	• Standard EIA-310 1U Rack-mount chassis, <= 800mm deep
SSDs Drive Bays	• 36 X NF1 NVMe front-loaded, hot swappable SSD bays (more if thermal evaluation allows).

	(A 64X NF1 will be verified instead, if the thermal is allowed.)
Boot Drive	• On motherboard M.2
System Firmware	• **BIOS and BMC Features:** ACPI, PXE boot, Wake-on-LAN, AC loss recovery, IPMI 2.0 KCS interface, SMBIOS, Serial console redirection, BIOS boot specification, BIOS recovery mode, SRIOV, iSCSI, TPM support, PCIe NTB.
Front Panel	• **Controls:** o Power On/Off • **Indicator LEDs:** o Power Status o Global SSD activity o Global network activity o Global fault • **Interfaces:** o [TBD] x USB 2.0 ports
Motherboard Features	• **Processors:** 2x Intel® Xeon® Processors E5-2600 v5 (Skylake) • **QPI Speeds:** 9.6 GT/s, 8 GT/s, 7.2 GT/s • **Chipset:** Intel® C620 Chipset • **System Memory:** 24 DIMM slots (2 CPU sockets × 6 channels/CPU socket × two slots/channel)

2.3 Block Diagram of Mission Peak System

Mission Peak has an EIA standard 1U chassis. It should be used at the product level, as a popular form-factor chassis for datacenter storage servers. The chassis holds an Intel Skylake Xeon-based baseboard in its rear section, cooling fans in the middle, and a modular backplane, plus up to 36 NVME SSD drives in the front drive bay area. The front panel includes a power button, reset button, LEDs to indicate power and status, and one USB port. The rear of the chassis has two redundant hot plug power supplies whose power capacity is 1500Watt to support maximum system power.

To optimize performance, the Mission Peak system utilizes all PCIe resources in a balanced and symmetric topology. We extracted all the PCIe IOs available through Skylake to maximize system storage IO performance.

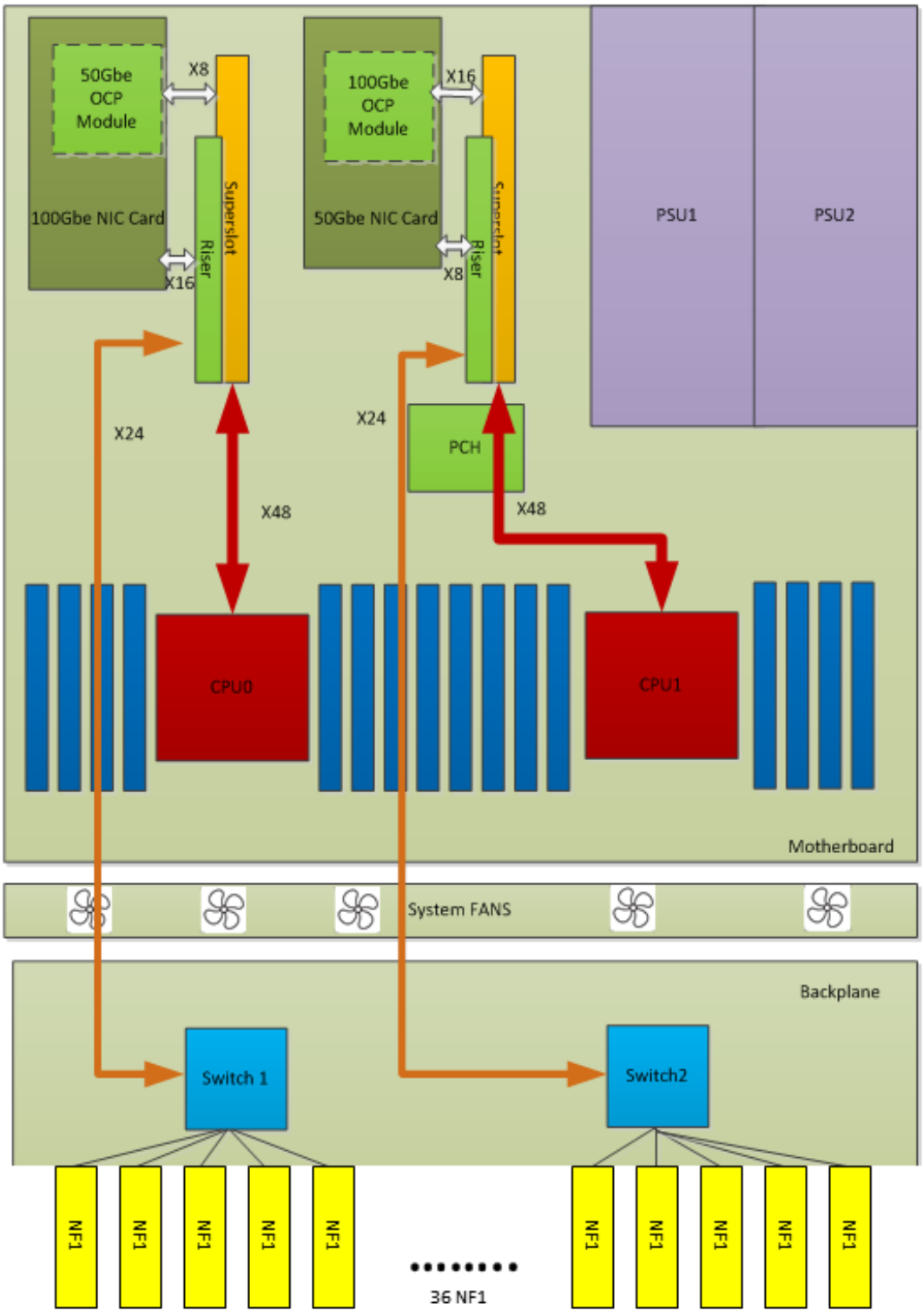


Figure 3 - Mission Peak System Placement Block Diagram

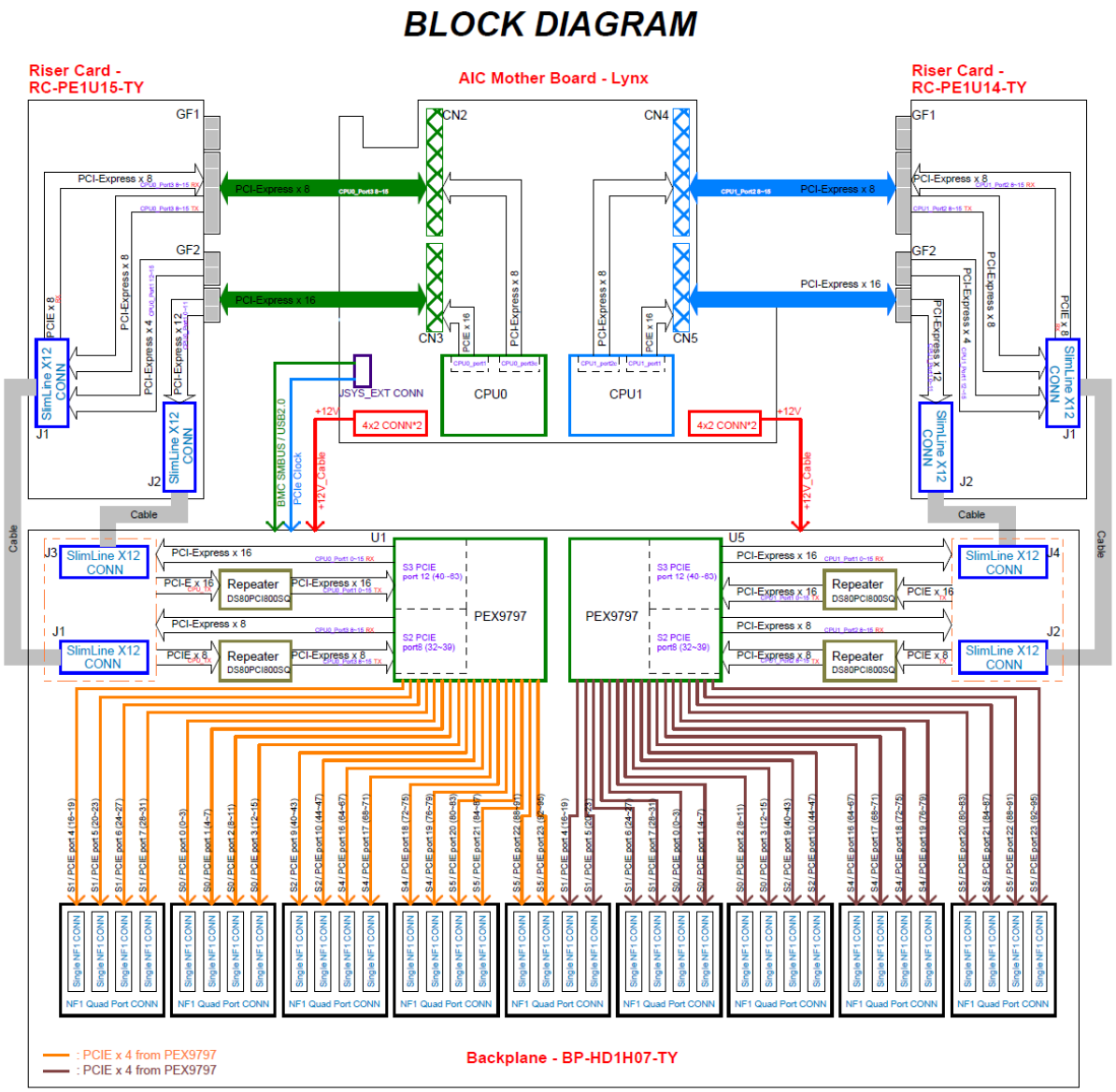


Figure 4 - Mission Peak System Architecture

2.4 Mission Peak Motherboard

The Mission Peak motherboard provides all PCIe lanes from the CPUs to allow users to select the optimal usage model. It also delivers advanced performance and enables a high degree of power efficiency, making it well-suited for highly efficient performance platforms.

The motherboard supports the latest dual Intel Xeon processor, which is a part of the Intel Xeon E5 Skylake product family. Given the above, the motherboard offer six channels of DDR4-2400 per socket, which gives users a 24-DIMM slot for large memory capacity.

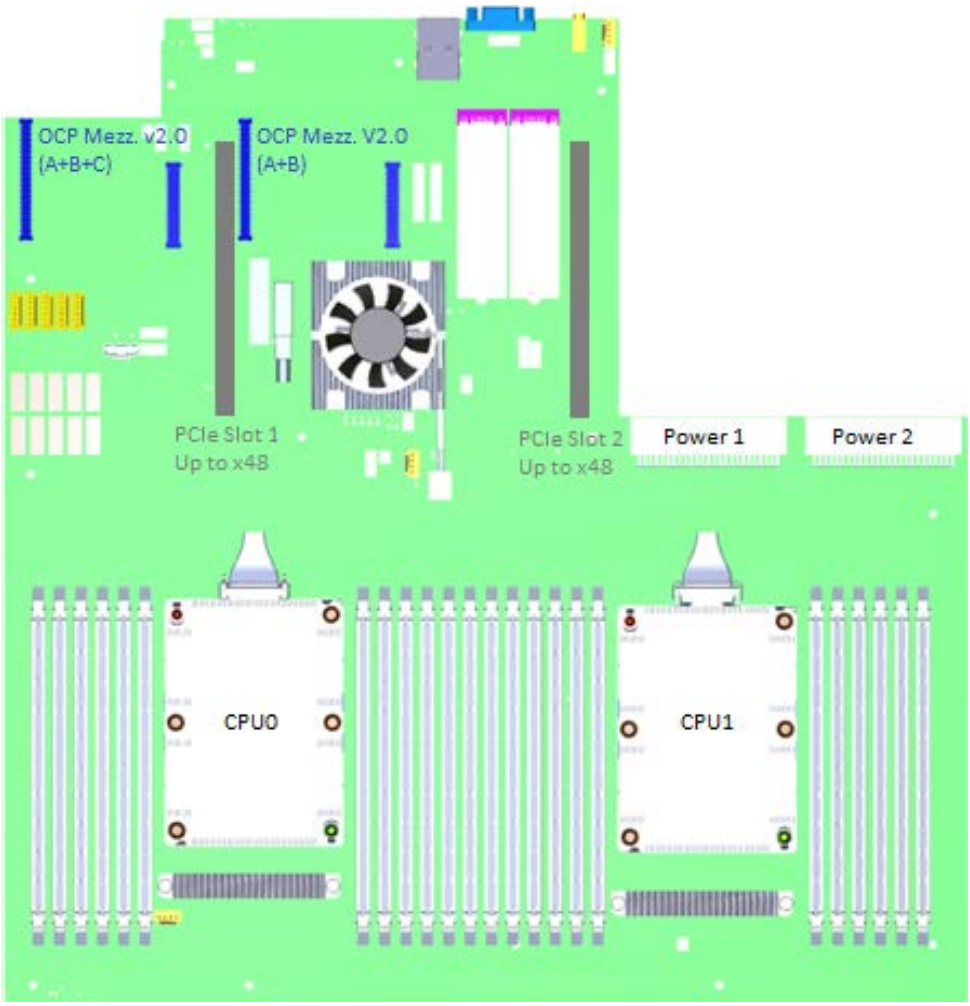


Figure 5 - Mission Peak Motherboard Function Diagram

In regards to I/O, the motherboard supports the following major I/O interfaces:

PCIE:

- Supper slot #1: X48 PCIe Gen3 lanes from CPU0
- Supper slot #2: X48 PCIe Gen3 lanes from CPU1
- 2XM.2 support for PCI-E Gen3 X2

Ethernet LAN:

- 2X 100Gbe
- 2X 50Gbe
- 1X Gbe RJ45 – dedicated to BMC management

I/O:

- 1X external VGA port
- 1X COM port

- 2X USB type A connectors + 1XRJ45 port for BMC management

Motherboard configuration:

PCIE Signal Distribution:

There are 2 PCIE superslots on the motherboard. Each CPU provides all its PCIe lanes (48 PCIe Gen3 lanes) to form a single superslot. Configuring a superslot depends upon how the lanes would be distributed (by function) within the system. To maximize the performance of NF1 POC in a 1U system, all the Skylake PCIe lanes are fully used; avoiding any bandwidth bottleneck, while the PCIe topology is balanced and symmetric. Out of the 48 lanes in each CPU, X24 lanes go to NIC and X24 lanes connect to the PCIe switch in order to link up with the NF1 SSDs, so the bandwidth between CPU <-> SSDs and CPU <-> NIC is matched and balanced. And, because the connection between two CPUs is symmetric, data traffic across the QPI is avoided, eliminating a possible performance bottleneck, to deliver the best performance from SSDs out of the box. The following is a table that shows PCIe signal distribution.

Table 2 - NF1 (NGSFF) POC PCIe Slot Configuration

Superslot #	PCIE width	From which CPU	Usage
Slot1	X16	CPU0	100Gbe PCIe adding card
Slot1	X8	CPU0	50Gbe OCP Mezz Card
Slot1	X24	CPU0	Riser card and cable connect to midplane
Slot2	X16	CPU1	100Gbe OCP Mezz Module
Slot2	X8	CPU1	50Gbe PCIe adding card
Slot2	X24	CPU1	Riser card and cable connect to midplane

2.5 PCIe Switch Midplane/Backplane

The Mission Peak midplane is the board located between the motherboard and the NF1 SSDs. It contains two Broadcom PLX9797 switches. Each switch is configured with X24 PCIe upstream ports and X72 PCIe downstream ports. PCIe Switch 1 connects to CPU1 via one X24 PCIe riser on superslot #1 of the motherboard, and PCIe switch 2 connects to CPU2 via one X24 PCIe riser on superslot #2 of the motherboard. The PCIe reference clock is delivered from the riser to the PCIe switches on the midplane via separate cable connections.

In addition, other miscellaneous signals are connected with the motherboard, such as JSGPIO, IPMI signals, and front panel signals.

The midplane contains a temperature sensor to report thermal conditions in the PCIe switch area to the BMC for system level thermal control. It also can provide enclosure management logic in a CPLD to offer enclosure management features at the system level.

Furthermore, the midplane can be treated as a backplane, because the NF1 SSDs will directly dock to the board by using a right angle NF1 connector.

This has three major benefits:

1) The architecture saves a board, reducing cost and risk.

2) It improves signal integrity because the PCIe routing trace is much shorter and there are no extra interconnectors.

3) It improves thermal conditions and airflow for NF1 SSDs. Because there are no vertical backplanes, the airflow is much more open for NF1 device cooling.

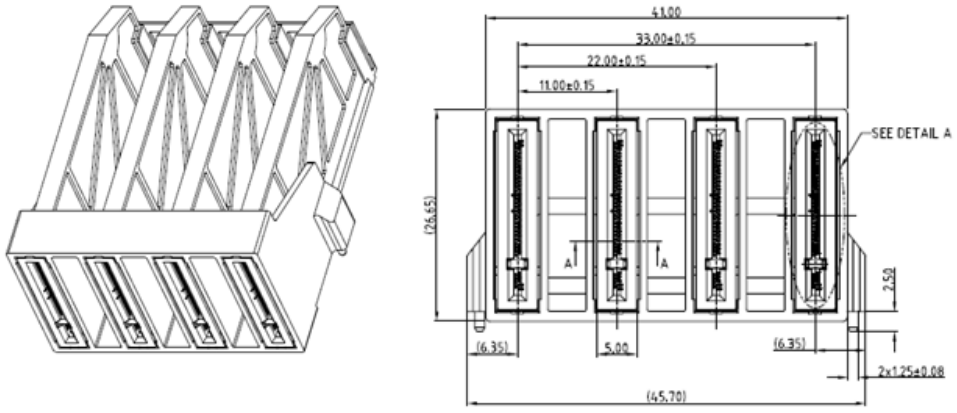


Figure 6- NF1 (NGSFF) Orthogonal Connector Specification

2.6 IOPs Performance Evaluation

Based on FIO testing, the local 4K random read IOPS can reach up to 10MIOP, and remote 4K random read IOPS with NVMeoF via RDMA can reach up to 8.5M IOPS.

As shown in Figure 7, when we compare this to a 2U 24XU.2 NVMe storage server reference design that we published at 2015, performance increased about X3 times. In a 4U space, the Mission Peak design can provide as much as 40MIOPs.

The following figure shows NF1 POC system performance and density improvement compared to our 2015 Sierra reference design.

Figure 7 - NF1 (NGSFF) POC System Performance Improvement

3. Physical Specifications

3.1 Placement and Form Factor

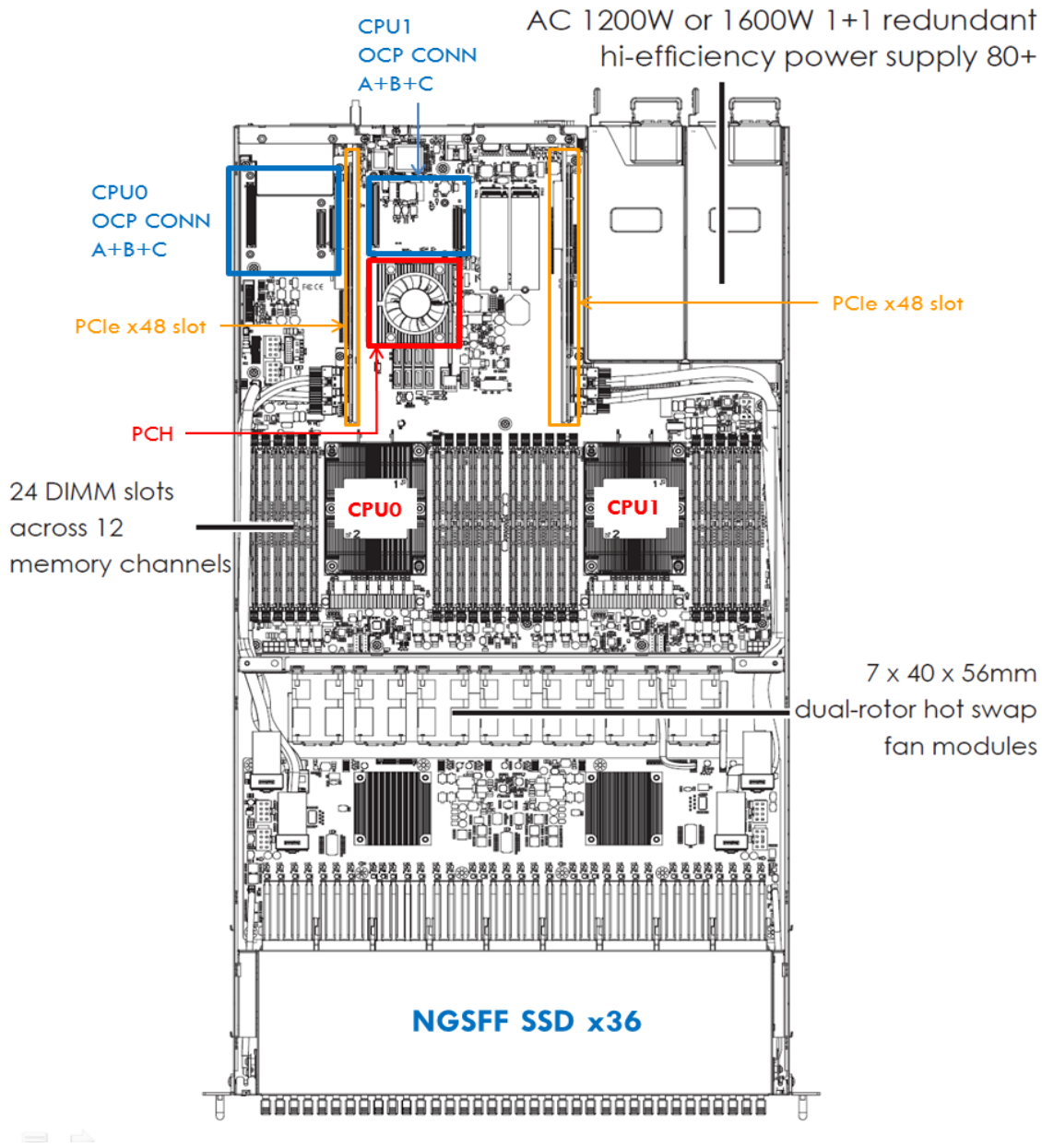


Figure 8 - Mechanical Placement

3.2 CPU and Memory/Platform Controller Hub (PCH)/PCIe

<table>
<tr><th>Feature</th><th>Description / Comments</th></tr>
<tr><td>Motherboard

CPU/Memory</td><td>
● Dual Intel® Xeon® Processor Scalable Family, Skylake /Cascade Lake process.
● 12x 288-pin DDR4 DIMM slots per CPU socket
● Support DDR4-2933/2666/2400/2133/1866 RDIMM/LRDIMM
● On-board graphic controller to provide VGA connectivity to external monitor

Intel® Xeon® processor E5 v4 Family
<table>
<tr><th>E5 v4</th><th>TDP</th><th>CC</th><th>GHz</th><th>SIR*</th><th>SFR*</th><th>LINPACK*</th></tr>
<tr><td>E5-2699A v4</td><td>145</td><td>22</td><td>2.4</td><td>67.6%</td><td>65.9%</td><td>55.3%</td></tr>
<tr><td>E5-2699 v4</td><td>145</td><td>22</td><td>2.2</td><td>63.2%</td><td>64.6%</td><td>52.7%</td></tr>
</table>
Intel® Xeon® processor Scalable Family
<table>
<tr><th>Skylake-SP</th><th>TDP</th><th>CC</th><th>GHz</th><th>SIR*</th><th>SFR*</th><th>LINPACK*</th></tr>
<tr><td>8180</td><td>205</td><td>28</td><td>2.5</td><td>100.0%</td><td>100.0%</td><td>100.0%</td></tr>
<tr><td>8176</td><td>165</td><td>28</td><td>2.1</td><td>89.7%</td><td>92.3%</td><td>76.5%</td></tr>
<tr><td>8170</td><td>165</td><td>26</td><td>2.1</td><td>84.5%</td><td>89.0%</td><td>71.0%</td></tr>
<tr><td>8168</td><td>205</td><td>24</td><td>2.7</td><td>92.4%</td><td>95.7%</td><td>95.8%</td></tr>
<tr><td>8164</td><td>150</td><td>26</td><td>2.0</td><td>82.2%</td><td>88.6%</td><td>65.5%</td></tr>
<tr><td>8160</td><td>150</td><td>24</td><td>2.1</td><td>79.8%</td><td>87.5%</td><td>70.6%</td></tr>
<tr><td>6154</td><td>200</td><td>18</td><td>3.0</td><td>77.2%</td><td>85.5%</td><td>79.4%</td></tr>
</table>
</td></tr>
<tr><td>Motherboard

PCH</td><td>
● Intel® C620 Series Chipset (Lewisburg)

<table>
<tr><th>Product Name</th><th>SKU</th><th>10Gb/1 Gb Ethernet Ports</th><th>Compression</th><th>Encryption</th><th>RSA</th><th>Max PCIe* Uplink</th><th>Recommended Min uplink Config</th><th>PCIe* Uplink x8 Optional Muxed Link</th><th>Est TDP (W)</th></tr>
<tr><td></td><td></td><td></td><td colspan="3">Intel® QuickAssist Technology</td><td></td><td></td><td></td><td></td></tr>
<tr><td>Intel® C621 Chipset</td><td>LBG-1G</td><td>0/4</td><td>N/A</td><td>N/A</td><td>N/A</td><td>x1</td><td>x1</td><td>disabled</td><td>~15</td></tr>
<tr><td>Intel® C622 Chipset</td><td>LBG-2</td><td>2/4†</td><td>N/A</td><td>N/A</td><td>N/A</td><td>x8</td><td>x4</td><td>disabled</td><td>~17</td></tr>
<tr><td>Intel® C624 Chipset</td><td>LBG-4</td><td>4/4</td><td>N/A</td><td>N/A</td><td>N/A</td><td>x16</td><td>x8</td><td>disabled</td><td>~19</td></tr>
<tr><td>Intel® C625 Chipset</td><td>LBG-E</td><td>4/4</td><td>20 Gb/s</td><td>20 Gb/s</td><td>20K Ops/s</td><td>x16</td><td>x16</td><td>disabled</td><td>~22</td></tr>
<tr><td>Intel® C626 Chipset</td><td>LBG-M</td><td>4/4</td><td>40 Gb/s</td><td>40 Gb/s</td><td>40K Ops/s</td><td>x16</td><td>x16</td><td>enabled</td><td>~26</td></tr>
<tr><td>Intel® C627 Chipset</td><td>LBG-T</td><td>4/4</td><td>100 Gb/s</td><td>100 Gb/s</td><td>100K Ops/s</td><td>x16</td><td>x16</td><td>enabled</td><td>~29</td></tr>
<tr><td>Intel® C628 Chipset</td><td>LBG-L</td><td>4/4</td><td>100 Gb/s</td><td>100 Gb/s</td><td>100K Ops/s</td><td>x16</td><td>x16</td><td>enabled</td><td>~21</td></tr>
</table>
†Four ports total: ports 0 & 1 can run up to 10 GbE, while ports 2 & 3 are limited to 1 GbE
Package Size (all SKUs): 34x28mm, Package Pin Count: 1310
Intel recommends two lanes of PCIe3 for each active 10GbE port for networking and x16 if Intel® QuickAssist Technology is active
LBG supports x16, x8, x4 and x1 options, up to the maximum uplink width.
*These Ethernet ports are in addition to the 1Gb port used by ME11.6
All LBG skus support 7 year production and 10 year use in line with the Unique Extended Supply Life CPU SKUs (10-year use + NEBS-Friendly Thermal Specification)
All SKUs, frequencies and features are PRELIMINARY and can change without notice.
</td></tr>
<tr><td>Motherboard

Input / Output</td><td>
● PCIe:

o 2 x NIC Cards
o 2 x OCP Mezzanine Card

● LAN:

o CPU0 : 1 x 100GbE (PCIE add on card) + 1 x 50GbE single port (OCP)
o CPU1 : 1 x 100GbE (OCP) + 1 x 50GbE dual port (PCIE add-on card)
o 2 × USB 3.0 + 2 x USB 2.0

● SATA:

o 8 x SATA3 ports on the motherboard

● VGA:

o 1 x external VGA port
</td></tr>
</table>

	● **Serial port** o Via micro USB to serial controller o 1 x internal DB-9 serial pin-header ● **Other:** Debug display pin-header, GPIO port, IPMB pin-header, chassis intrusion

3.3 PCB Stack-Up

The following PCB stack-up includes a motherboard, riser card and backplane design. This is required to check with PCB fab vendors to fine-tune impedance based on the impedance control table below, before starting the PCB design.

The PCB material is referenced as IT-180I.

Table 3 - Motherboard PCB Stack-up

Bus							MISO,DDR4(DQ/DQS), Breakout	DDR4	HSD breakout	Clocks,PCIe,SATA,QPI,DMI,USB2/3	SFI 10G-KR	LAN(I210),LSI
Z Type							Single	Single	Differential	Differential	Differential	Differential
Freq.(MHz)												
Target Z (ohms)							50(Outer)/50(Inner)	40(Outer)/40(Inner)	83(Outer)/85(Inner)	85(Outer)/85(Inner)	93(Outer)/93(Inner)	100(Outer)/100(Inner)
Z tolerance							+/- 10%	+/- 10%	+/- 10%	+/- 10%	+/- 10%	+/- 10%
Layer	Lyr Type	Finished Cu Wt	Material		Tolerance	Er	Trace	Trace	Trace / Space / Trace	Trace / Space / Trace	Trace / Space / Trace	Trace / Space / Trace
		Soldermask		0.70								
1	TOP	1/3oz Copper Foil+plating		1.60			4 (49.78)	6.5 (39.29)	4 / 4 / 4 (82.33)	4.5 / 6 / 4.5 (84.73)	4.5 / 15 / 4.5 (92.27)	3.5 / 10 / 3.5 (100.25)
		Prepreg	1080.00	2.66	+/- 1 mil	3.8						
2	GND	1 oz		1.20			GND	GND	GND	GND	GND	GND
		Core	0.11mm	4.00	+/- 1 mil	3.9						
3	IN1	1 oz		1.20			5 (49.37)	7.5 (40.75)	4 / 4 / 4 (83.81)	5 / 6.5 / 5 (85.82)	4.5 / 8 / 4.5 (92.73)	4 / 10 / 4 (100.25)
		Prepreg	2116HR*3+2113	13.40	+/- 1 mil	4.2						
4	IN2	1 oz		1.20			5 (49.37)	7.5 (40.75)	4 / 4 / 4 (83.81)	5 / 6.5 / 5 (85.82)	4.5 / 8 / 4.5 (92.73)	4 / 10 / 4 (100.25)
		Core	0.11mm	4.00	+/- 1 mil	3.9						
5	VCC	1 oz		1.20			VCC	VCC	VCC	VCC	VCC	VCC
		Prepreg	2113	3.34	+/- 1 mil	3.9						
6	IN3	1 oz		1.20			5 (50.17)		4.5 / 7 / 4.5 (85.33)	5 / 12 / 5 (85.18)		
		Prepreg	0.25mm	10.00	+/- 1 mil	4.2						
7	IN4	1 oz		1.20			5 (50.17)		4.5 / 7 / 4.5 (85.33)	5 / 12 / 5 (85.18)		
		Core	2113	3.34	+/- 1 mil	3.9						
8	VCC1	1 oz		1.20			VCC	VCC	VCC	VCC	VCC	VCC
		Core	0.11mm	4.00	+/- 1 mil	3.9						
9	IN5	1 oz		1.20			5 (49.37)	7.5 (40.75)	4 / 4 / 4 (83.81)	5 / 6.5 / 5 (85.82)	4.5 / 8 / 4.5 (92.73)	4 / 10 / 4 (100.25)
		Prepreg	2116HR*2+2113	13.40	+/- 1 mil	4.2						
10	IN6	1 oz		1.20			5 (49.37)	7.5 (40.75)	4 / 4 / 4 (83.81)	5 / 6.5 / 5 (85.82)	4.5 / 8 / 4.5 (92.73)	4 / 10 / 4 (100.25)
		Core	0.11mm	4.00	+/- 1 mil	3.9						
11	GND1	1 oz		1.20			GND	GND	GND	GND	GND	GND
		Prepreg	1080.00	2.66	+/- 1 mil	3.8						
12	BOT	1/3oz Copper Foil+plating		1.60			4 (49.78)	6.5 (39.29)	4 / 4 / 4 (82.33)	4.5 / 6 / 4.5 (84.73)	4.5 / 15 / 4.5 (92.27)	3.5 / 10 / 3.5 (100.25)
		Soldermask		0.70								
Total Thickness				81.40	± 10%							

Table 4 - Riser Card PCB Stack-up

10-Layer 1.6mm Stackup(IT-180)

Microstrip : 9H / 11H
Stripline : 3H / 5H

Bus					Normal	SAS GEN3	PCIE GEN3
Z Type					Single	Differential	Differential
Freq.(MHz)						12G	8G
Target Z (ohms)					50	100	85
Z tolerance					Outer Layer ± 15% / Inner Layer ± 10%	Outer Layer ± 15% / Inner Layer ± 10%	Outer Layer ± 15% / Inner Layer ± 10%
Layer	Lyr Type	Material	Thickness(mil)	Er	Trace/Space	Trace/Space/Trace/ To others	Trace/Space/Trace/ To others
		Soldermask	0.8	3.80			
1	TOP	Cu+plating	1.4		5	4 / 7 / 4	5 / 5 / 5
		Prepreg	3.08	3.9			
2	GND1	Cu	1.3		GND	GND	GND
		Core	4	3.8			
3	IN1	Cu	1.3		4	4 / 8 / 4	5 / 6 / 5
		Prepreg	8.73	4			
4	VCC1	Cu	1.3		VCC	VCC	VCC
		Core	4	3.8			
5	VCC2	Cu	1.3		VCC	VCC	VCC
		Prepreg	8.23	4			
6	IN2	Cu	1.3		4	4 / 8 / 4	5 / 6 / 5
		Core	4	3.8			
7	GND2	Cu	1.3		GND	GND	GND
		Prepreg	8.73	4			
8	IN3	Cu	1.3		4	4 / 8 / 4	5 / 6 / 5
		Core	4	3.8			
9	GND3	Cu	1.3		GND	GND	GND
		Prepreg	3.08	3.9			
10	BOT	Cu+plating	1.4		5	4 / 7 / 4	5 / 5 / 5
		Soldermask	0.8	3.80			
		Tatal thickness	1.6mm+/-10%				

Table 5 - Backplane PCB Stack-up

16-Layer 2.4mm Stackup

							Microstrip : 9H / 11H Stripline : 3H / 5H	Microstrip : 9H / 11H Stripline : 3H / 5H	
Bus						**Normal**	**PCIe GEN3**	**SAS**	
Z Type						Single	Differential	Differential	
Freq.(MHz)							8G	12G	
Target Z (ohms)						50	85 (single : 50 ohms)	100 (single : 50 ohms)	
Z tolerance						Outer Layer ± 15% / Inner Layer ± 10%	Outer Layer ± 15% / Inner Layer ± 10%	Outer Layer ± 15% / Inner Layer ± 10%	
Layer	Lyr Type	Finished Cu Wt	Thickness	Tolerance	Er	Trace/Space	Trace/Space/Trace/ To others	Trace/Space/Trace/ To others	Trace/Space
		Soldermask	1.00		3.80				
1	TOP	0.5 oz+Platting	1.60			7	6/5 / 40 / 48	5/7.5 / 40 / 48	
		Prepreg	4.44	+E9/- 1mil	4.00				
2	GND	1 oz	0.65			GND	GND	GND	GND
		Core	5.00	+/- 1mil	3.80				
3	IN1	1 oz	0.65			5	5.5/5.5 / 20 / 30	4/7 / 20 / 30	
		Prepreg	6.01	+/- 1mil	4.20				
4	VCC/GND	1 oz	0.65			VCC/GND	VCC/GND	VCC/GND	VCC/GND
		Core	5.00	+/- 1mil	3.80				
5	IN2	1 oz	0.65			5	5.5/5.5 / 20 / 30	4/7 / 20 / 30	
		Prepreg	6.01	+/- 1mil	4.20				
6	GND	1 oz	0.65			GND	GND	GND	GND
		Core	5.00	+/- 1mil	3.80				
7	IN3	1 oz	0.65			5	5.5/5.5 / 20 / 30	4/7 / 20 / 30	
		Prepreg	6.01	+/- 1mil	4.20				
8	VCC	1 oz	0.65			VCC	VCC	VCC	VCC
		Core	5.00	+/- 1mil	3.80				
9	VCC	1 oz	0.65			VCC	VCC	VCC	VCC
		Prepreg	6.01	+/- 1mil	4.20				
10	IN4	1 oz	0.65			5	5.5/5.5 / 20 / 30	4/7 / 20 / 30	
		Core	5.00	+/- 1mil	3.80				
11	GND	1 oz	0.65			GND	GND	GND	GND
		Prepreg	6.01	+/- 1mil	4.20				
12	IN5	1 oz	0.65			5	5.5/5.5 / 20 / 30	4/7 / 20 / 30	
		Core	5.00	+/- 1mil	3.80				
13	VCC/GND	1 oz	0.65			VCC/GND	VCC/GND	VCC/GND	VCC/GND
		Prepreg	6.01	+/- 1mil	4.20				
14	IN6	1 oz	0.65			5	5.5/5.5 / 20 / 30	4/7 / 20 / 30	
		Core	5.00	+/- 1mil	3.80				
15	GND	1 oz	0.65			GND	GND	GND	GND
		Prepreg	4.44	+/- 1mil	4.00				
16	BOT	0.5 oz+Platting	1.60			7	6/5 / 40 / 48	5/7.5 / 40 / 48	
		Soldermask	1.00		3.80				
		Total Thickness	94.24	(+7 / -5)					

3.4 NF1 (NGSFF) NVMe SSD

The Samsung SSD PM983 delivers wide bandwidth of up to 3,100MB/s sequential read speed and up to 2,000MB/s sequential write speed under up to 10.0W power. With the help of a toggle 3.0 NAND Flash interface, the Samsung SSD PM983 delivers random performance of up to 540KIOPS for random 4KB read and up to 50KIOPS for random 4KB write in a sustained state.

In addition, the Samsung SSD PM983 supports Power Loss Protection (PLP). PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure.

The system will use Samsung NF1 SSDs in front of the drive bay. NF1 supports the following main features:

1) Dimensions: 110X30.5X4.38 mm

2) Hot-plug

3) Activity and fault LED on drive (controlled by the SSD drive itself)

4) Power loss protection

5) A holder or carrier to allow a user to easily plug in and out of the system.

6) Power target at 10W per unit for datacenter drive (NF1 spec leave 16W for enterprise SSD version)

7) Capacity is up to 16TB

8) Supports SSD Enhanced S.M.A.R.T. feature set

9) Hardware based AES-XTS 256-bit encryption engine

10) Static and Dynamic Wear Leveling

11) Compliant with PCI Express CEM Specification Rev. 3.0

12) Compliant with PCI Express Base Specification Rev. 3.1

13) Compliant with NVM Express Specification Rev. 1.2b

14) RoHS / Halogen-Free Compliance

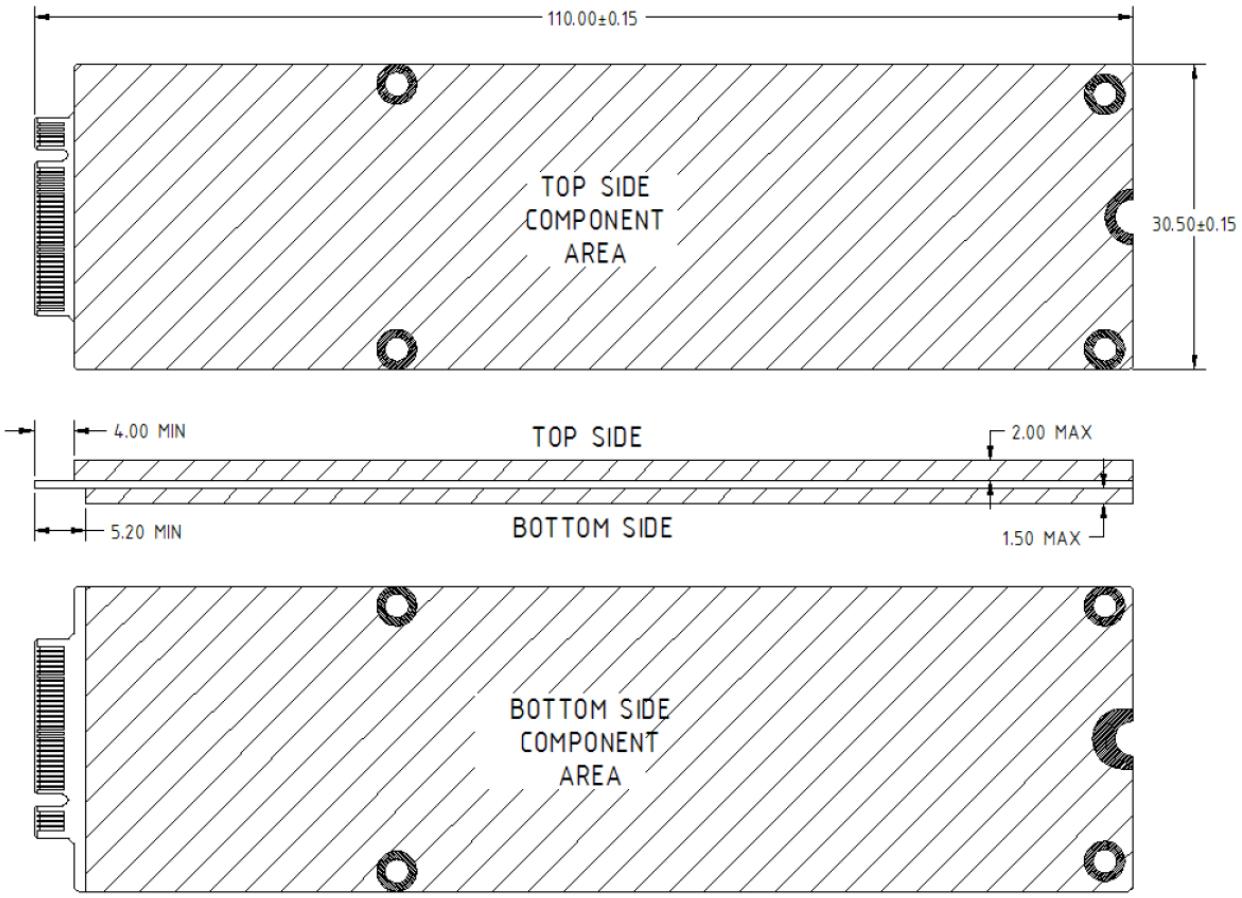


Figure 9 - NF1 (NGSFF) Form Factor (Mechanical Outline)

The Samsung PM983 supports an LED to indicate the online and activity status of SSD. “Activity” or “good” states are displayed as a Green LED. Degraded or fault states are displayed as an Amber LED. The table below describes all possible activity states of the LED's according to the condition of the drive.

Color	Condition	Activity
LED1 (Amber)	Drive Healthy, or slot power off	OFF
	Drive Fault	Steady ON
LED2 (Green)	Drive Not Operational, or Powered-off	OFF
	Drive Operational, no Activity, no Fault	Steady ON
	Drive Operational, Read/Write Activity	Activity Blink (Blinks at the rate of 375ms on, 125ms off)

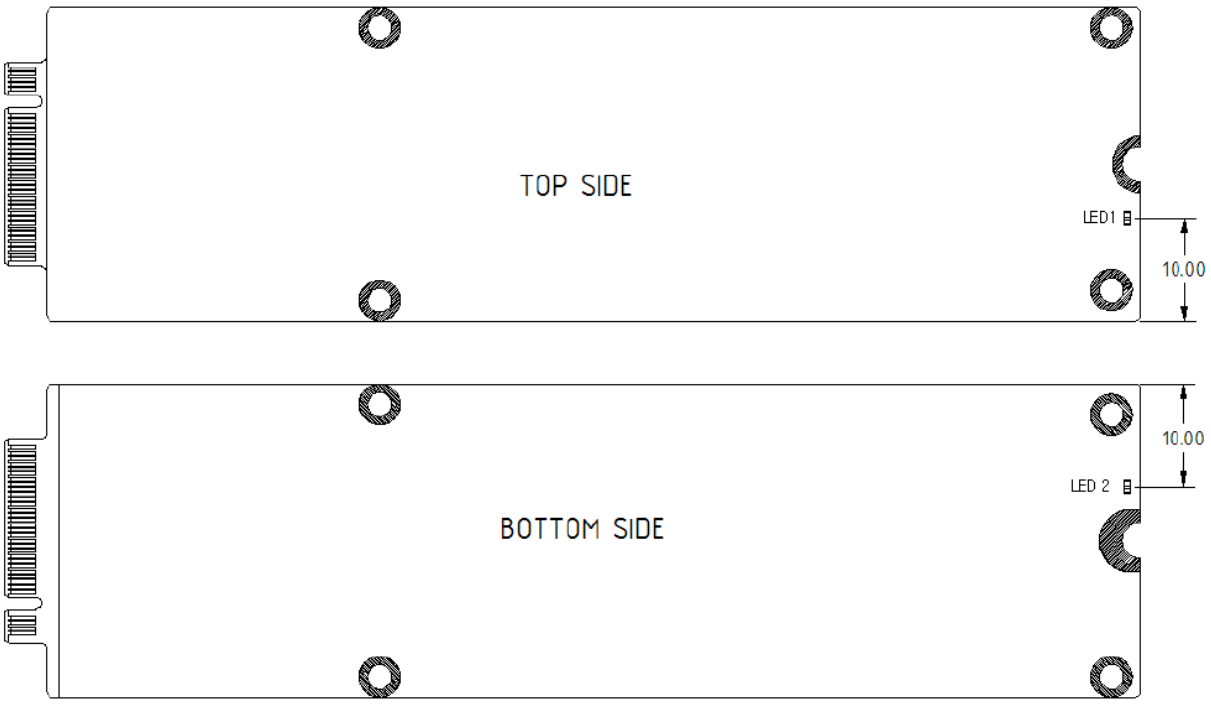
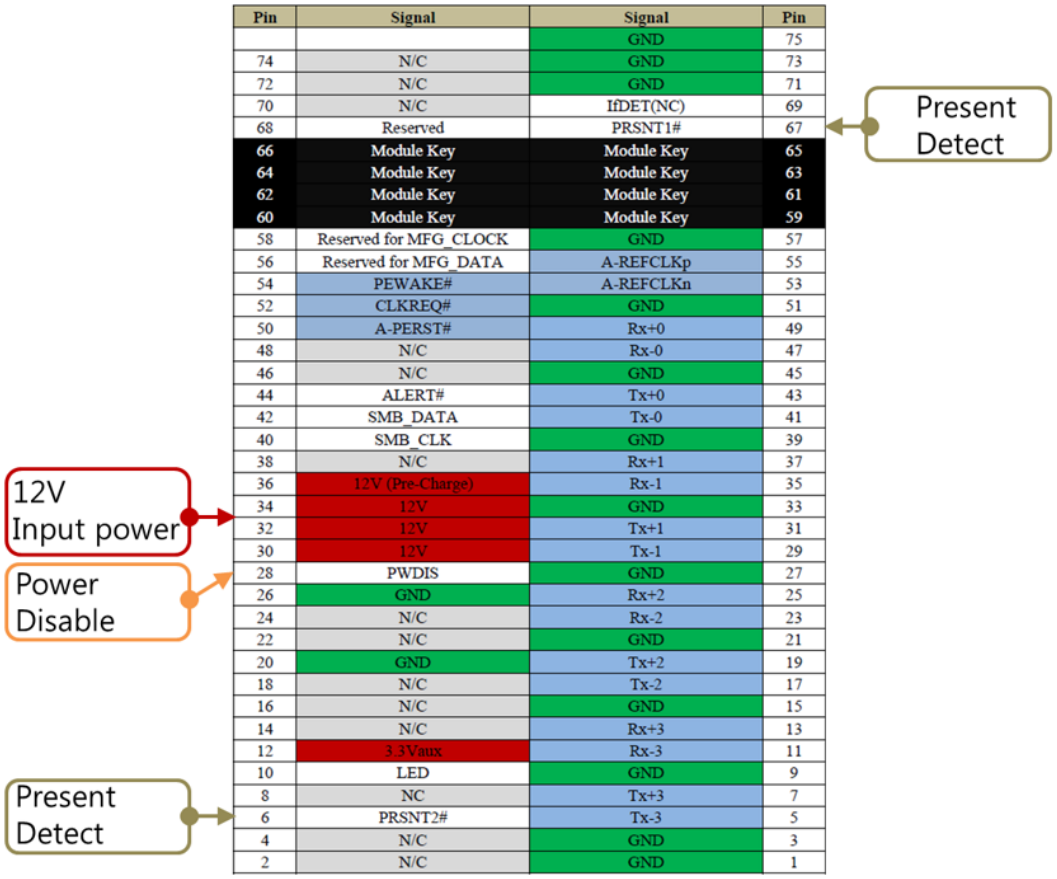


Figure 10 - NF1 (NGSFF) LED Position

3.4.1 NF1 (NGSFF) SSD Pinout

NF1 leverages the M.2 pinout by adding signals to the NC pins. So it is backward compatible with M.2 devices. A total of 13 new nets have been added. And, all M.2 3.3V pins on the M.2 connector are changed to N/C pins for NF1 connections.



Pin	Signal	Signal	Pin
		GND	75
74	N/C	GND	73
72	N/C	GND	71
70	N/C	IfDET(NC)	69
68	Reserved	PRSNT1#	67
66	Module Key	Module Key	65
64	Module Key	Module Key	63
62	Module Key	Module Key	61
60	Module Key	Module Key	59
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	A-REFCLKp	55
54	PEWAKE#	A-REFCLKn	53
52	CLKREQ#	GND	51
50	A-PERST#	Rx+0	49
48	N/C	Rx-0	47
46	N/C	GND	45
44	ALERT#	Tx+0	43
42	SMB_DATA	Tx-0	41
40	SMB_CLK	GND	39
38	N/C	Rx+1	37
36	12V (Pre-Charge)	Rx-1	35
34	12V	GND	33
32	12V	Tx+1	31
30	12V	Tx-1	29
28	PWDIS	GND	27
26	GND	Rx+2	25
24	N/C	Rx-2	23
22	N/C	GND	21
20	GND	Tx+2	19
18	N/C	Tx-2	17
16	N/C	GND	15
14	N/C	Rx+3	13
12	3.3Vaux	Rx-3	11
10	LED	GND	9
8	NC	Tx+3	7
6	PRSNT2#	Tx-3	5
4	N/C	GND	3
2	N/C	GND	1

Figure 11 - NF1 (NGSFF) Pinout

4. BIOS

The BIOS is tuned to minimize system power consumption. It supports the following features:

• “Unused device” disablement, including PCIe lanes, PCI lanes, USB ports and SATA/SAS ports

• Tuning CPU/chipset settings to attain minimal power consumption and best performance

• Use of SPEC_power as the guidance for ODM to validate BIOS tuning results

The ODM provides a BIOS specification, which includes the complete BIOS, setup menu, and default settings. The setup menu allows its options to be configured before the operating system loads.

Configuration options available through the boot menu include the following:

• Settings to adjust memory speed, QPI speed, Speed-step/Turbo mode, and CPU Cx power state

• Setting for power feature after AC failure; default is set to power on

• Setting for fan speed control (for SIO FSC-enabled board only)

• Setting for altitude of server deployment location

• Hardware health monitoring display

• Setting for watchdog timer (default is enabled, and timeout value is 15 minutes)

• Event log viewing and clearing

• Setting for ECC error threshold, available settings are 1, 4, 10, and 1000.

• If a CMOS checksum error occurs (for example, one caused by a BIOS update), the BIOS loads the system default automatically after displaying a message in the console for five seconds and rebooting the system to apply the update without waiting for user input.

• Setting to disable all "wait for keyboard input to continue" types of features.

4.1 BIOS Chip

The Mission Peak system uses WINBOND W25Q256FVFIQ as the BIOS chip.

The BIOS chip is designed to use the PCH’s SPI interface through a BMC-controlled MUX to allow the BMC to perform offline BIOS updates or recovery. A 32 megabyte (32MB) capacity is recommended, considering the space required for both BIOS and Intel® ME firmware.

4.2 BIOS Source Code

Source code vendor is Insyde, A United Extensible Firmware Interface (UEFI) BIOS firmware is used. Insyde and AIC will maintain BIOS source code to ensure that it uses the latest code release from Intel and codebase vendors.

4.3 BIOS Feature Requirements

4.3.1 Optimization

The BIOS is tuned to minimize system power consumption and maximize performance. This includes:

- Enabling PCIe ASPM, C state, and disable unused devices.
- Enabling Turbo Mode.
- Following the Intel Xeon Scalable Family Purley platform performance and power optimization guide. (Document number:569458)

4.3.2 Setup Menu

Provide setup menu and default settings.

- Settings for adjusting memory speed, QPI speed, speed-step/turbo mode, and the following CPU C-state power states. The default follows the CPU and chipset vendor's POR, unless otherwise mentioned.
- Settings to enable a variety of turbo mode tuning settings based on CPU SKU and memory configurations. The default follows the CPU and chipset vendor's POR, unless otherwise mentioned.
- Setting for the power feature after AC failure. Default is set to "power off".
- Setting for the local physical COM port (COMA) and Serial-Over-LAN (SOL) (COMB). The default enables console redirection on COMB with baud rate 115200, hardware flow control, terminal type VT100, 8 data bits, no parity, and 1 Stop bit.
- Setting for ECC error event log
- A default setting to disable all "wait for keyboard input to continue" features
- Setting of UEFI and Legacy boot options. The default is UEFI.
- Display RC version
- Display CPU information
- Display memory information

4.3.3 Boot Options

The BIOS supports the Preboot eXecution Environment (PXE) boot capability in IPv4 and IPv6 environments simultaneously and boots from the SATA/SAS and USB interfaces. The BIOS also has the capability for boot option selection.

4.3.4 SMBIOS sync with BMC FRU

The BIOS compares SMBIOS and FRU during POST, and updates SMBIOS automatically if different in Types 1, 2 and 3.

BMC FRU DATA	SMBIOS TABLE
Product Manufacturer	-> (Type 1) Manufacturer
Product Name	-> (Type 1) Product Name
Product Part/Model Number	-> (Type 1) SKU Number

Product Version	-> (Type 1) Version
Product Serial Number	-> (Type 1) Serial Number
Board Manufacturer	-> (Type 2) Manufacturer
Board Product Name	-> (Type 2) Product Name
Board Serial Number	-> (Type 2) Serial Number
Chassis Serial Number	-> (Type 3) Serial Number

4.3.5 POST Messages

- BIOS version, build date
- Some hardware information (CPU, Memory, etc.)
- Hot key messages during POST
- Boot device names

4.3.6 Event log

The BIOS performs event logging through BMC SEL with Generator ID 0x0001, and meets SEL log requirements.

4.4 Firmware Feature Plan of Record

Regarding the Intel SPS firmware plan of record, Intel's Management Engine (ME) runs Intel server platform services firmware (SPS). Intel SPS is required for system operation. The FW can be updated by the Insyde BIOS update utility.

5. BMC

5.1 Management Network Interface GbE(PHY)

Dedicated NIC RMII (GbE PHY) x 1

Hare NIC RMII/NCSI x 1

The following outlines requirements for the BMC's management network interface:

The BMC should have both a RMII and an NC-SI port for OOB access.

There are two options for OOB access that should be supported:

Option 1: The shared NIC uses the RMII interface to pass management traffic onto the RTL8201EL-VC-GR data network. The RTL8201EL-VC-GR has a 10/100/1000 MDI interface to the RJ45.

Option 2: The shared NIC uses the RMII/NCSI interface to pass management traffic on the Intel® I210-AT data network. The Intel I210-AT has a 10/100/1000 MDI interface to the RJ45.

The BMC firmware needs to be flexible as to which interface and device to activate, either by hardware strapping or a preset priority policy. The BMC needs to ensure that unused interfaces and devices are disabled and do not interfere with the activated management interface and device.

The OOB MAC address should use the NIC's data network MAC with an offset defined by NIC vendors.

The BMC management network firmware and utility must support all features defined in this specification for IPv4 and IPv6 network environments.

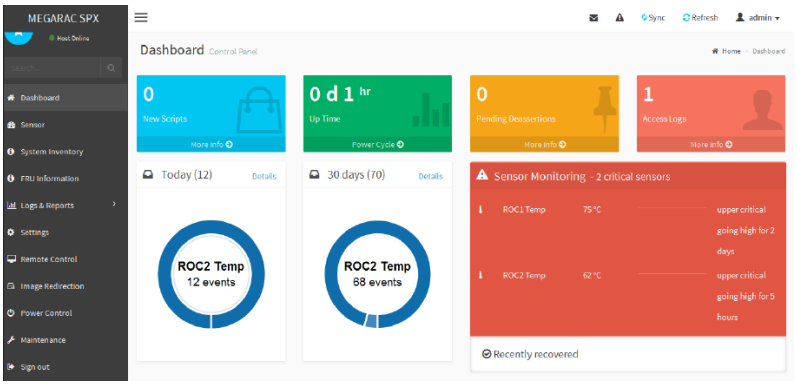
5.2 Local Serial Console and SOL BMC

Local serial console: Hardware not supported

SOL: Hardware is supported

5.3 Graphic and GUI

Supports BMC WEB GUI and iKVM (KVM over IP)



5.4 Remote Power Control and Power policy

Remote Power Control: Support power on/off/reset/cycle

Power policy: Need system reboot to take effect as “always on or “always off,” with a last-state option

5.5 Port 80 POST

Supports IMPI command to get port 80 POST code

5.6 Power and System Identification LED

Supports power LED x 1 and ID LED x 1

Solid on ID LED: BMC detect fail

Blinking ID LED: OEM function for customer to turn on ID LED

5.7 Platform Environment Control Interface (PECI)

Supports PECI through PCH SMLink 0

5.8 Power and Thermal Monitoring and power limiting

Supports Intel SPS NM power limiting, via IMPI bridge command to ME

5.9 SMBUS Diagram:

Appears as an I2C tree diagram, immediately below.

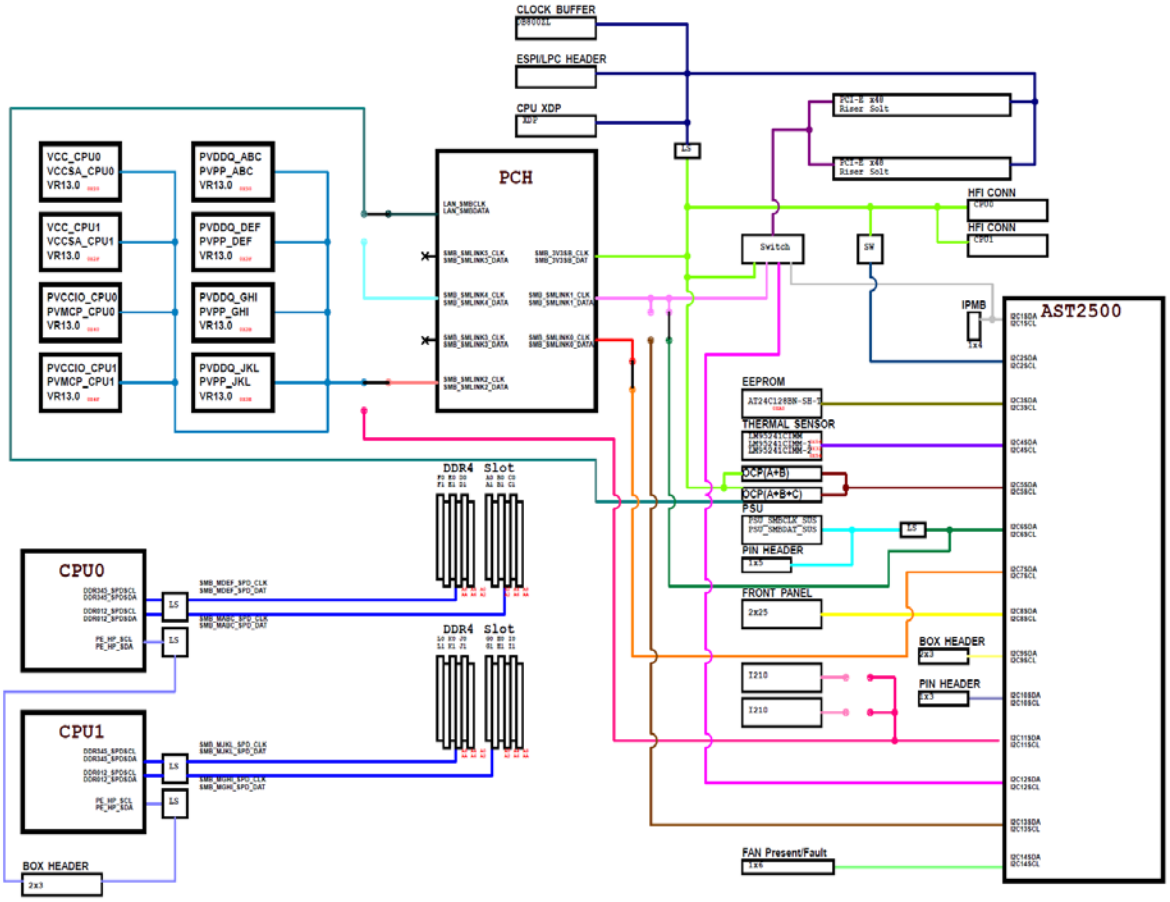


Figure 12 - I2C tree diagram

5.10 Sensors

The motherboard has the following thermal sensors:

- Two for monitoring the temperature of CPU1 and CPU2, retrieved via ME
- Temperature of CPU1 DIMM group and that of the CPU2 DIMM group, retrieved via ME
- PCH temperature, retrieved through Intel® C620 chipset internal DTS, through PCH SMLink1
- Inlet temperature, retrieved through the thermistor, and located on the front of the motherboard
- Outlet temperature, retrieved through the thermistor, and located at the rear of the motherboard
- One or two thermal sensors on the backplane to get SSD area thermal information

The fan control algorithm in the BMC makes sure that no CPU throttling is triggered due to thermal issues, under the following environmental conditions:

• Inlet temperature lower than or including 30°C, and 0 inch H2O pressure

• Inlet temperature higher than 30°C but no higher than 35°C, with 0.01 inch H2O pressure.

The sensors ensure that the total airflow rate for the chassis is lower than 220CFM, including PSU. In the event that one fan (one rotor as the dual rotor fan case) fails, an inlet temperature of 30°C with 0 inch H2O pressure environment is used to verify the thermal sensor.

Table 6 – List of System Sensors

Senser Number	Default Senser Name	Threshold	Show Name **X** is Hide	Power off system V : power off - : do not power off	Type 80	Remark	Modifiable
01	FAN2	LNR assert	Fan1A_BP	-	1000	Connector on backplane. J1,HW_FAN_TACH1,PWM_1	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
02	FAN2	LNR assert	Fan1B_BP	-	1000	Connector on backplane. J1,HW_FAN_TACH2,PWM_1	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
03	FAN2	LNR assert	Fan2A_BP	-	1000	Connector on backplane. J2,HW_FAN_TACH3,PWM_2	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
04	FAN2	LNR assert	Fan2B_BP	-	1000	Connector on backplane. J2,HW_FAN_TACH4,PWM_2	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
05	FAN2	LNR assert	Fan3A_BP	-	1000	Connector on backplane. J3,HW_FAN_TACH5,PWM_3	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
06	FAN2	LNR assert	Fan3B_BP	-	1000	Connector on backplane. J3,HW_FAN_TACH6,PWM_3	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
07	FAN2	LNR assert	Fan4A_BP	-	1000	Connector on backplane. J4,HW_FAN_TACH7,PWM_4	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		
08	FAN2	LNR assert	Fan4B_BP	-	1000	Connector on backplane. J4,HW_FAN_TACH8,PWM_4	
		LC assert		-	2000		
		LNR deassert		-	1500		
		LC deassert		-	2500		

SDR_List_2018_0319_OB127.xls

5.11 SEL

The SEL list appears below.

Table 7 – List of SEL

No.	Field	Record ID	Record Type	Time-stamp	Generator		EvM Rev	Sensor Type	Sensor #	Event Dir| EventType	Event Data1	Event Data2	Event Data3
-	Byte	1~2	3	4~7	8	9	10	11	12	13	14	15	16
1	Thermtrip	update	2h	update	20h	0h	4h	0x07	A3h ~ AAh	6Fh:Asserted Event	01h	FFh	FFh
2	DIMM Correctable ECC Error	update	2h	update	01h	0h	4h	0x0C	C4h	6Fh	A0h	cpu#(bit[3:0]), dimm#(bit[7:4])	Channel number [7:0]
3	DIMM Uncorrectable ECC Error	update	2h	update	01h	0h	4h	0x0C	C5h	6Fh	A1h	cpu#(bit[3:0]), dimm#(bit[7:4])	Channel number [7:0]
4	Add-in Card (PCI-E error)	update	2h	update	01h	0h	4h	0x17	CBh	6Fh	bit [7:4]=A ,bit[3:0]=fun#	bus#	dev# (bit[7:3]); bit[0:2](0=Correctable Error,1=Non-Fatal Error,2=Fatal Error)
5	Critical Interrupt (NMI included)	update	2h	update	20h	0h	4h	0x13	A2h	6Fh	0x00: front panel switch 0x03: Software NMI	0xFF	0xFF
6	System Firmware Progress (POST error)	update	2h	update	01h	0h	4h	0x0F	CCh	6Fh	C0h C0h E0h 80h 80h	07h: Keyboard error 0Ah: No video device detected 0Dh: CPU speed matching failure FEh: CMOS checksum bad (OEM event) FFh: RTC error (OEM event)	FFh FFh cpu#(bit[3:0]) FFh FFh
7	Temperature	update	2h	update	20h	0h	4h	0x01	20h ~ 3Fh	01h:Asserted Event 81h:Deasserted Event	59h: Upper Critical - going high 5Bh: Upper Non-recoverable - going high	Reading that triggered event	Threshold Value
8	voltage	update	2h	update	20h	0h	4h	0x02	40h ~ 6Fh	01h:Asserted Event 81h:Deasserted Event	50h: Lower Non-critical - going low 52h: Lower Critical - going low 54h: Lower Non-recoverable - going low 59h: Upper Critical - going high	Reading that triggered event	Threshold Value
9	Fan	update	2h	update	20h	0h	4h	0x04	00h ~ 1Fh	01h:Asserted Event 81h:Deasserted Event	54h: Lower Non-recoverable - going low	Reading that triggered event	Threshold Value
10	Watchdog	update	2h	update	20h	0h	4h	0x23	CAh	6Fh:Asserted Event	C0h:Timer expired, status only (no action, no interrupt) C1h:Hard Reset C2:Power Down C3:Power Cycle C8h:Timer Interrupt	[7:4] interrupt type 0h = none 1h = SMI 2h = NMI 3h = Messaging Interrupt [3:0] timer use at expiration: 1h = BIOS FRB2 2h = BIOS/POST 3h = OS Load 4h = SMS/OS 5h = OEM	FFh
11	Power On	update	2h	-	20h	0h	4h	C0h	A0h	0Ah:Asserted Event	00h:Thansition to Running	FFh	FFh
12	Power Off	update	2h	update	20h	0h	4h	C0h	A0h	0Ah:Asserted Event	02h:Thansition to Off	FFh	FFh
13	Power Reset	update	2h	update	20h	0h	4h	C0h	A1h	6Fh	00h: Power Reset	FFh	FFh
14	BMC Shutdown System	update	2h	update	20h	0h	4h	C0h	A9h	6Fh	01h: BMC shutdown system	FFh	FFh
15	PSU failure	update	2h	update	20h	0h	4h	09h	79h~7Bh	6Fh	06h:Fail signal(FAIL) 86h	FFh 01h: Over Voltage Protection(OVA) 02h: Over Current Protection(CPA) 03h: Under Voltage Protection(UVA) 04h: FAN Alarm(stop)(FANA) 05h: Thermal Alarm(THA) 06h: FAN Alarm(slow rotation)(PRFL) 07h:Over Voltage waring 08h:Over Temp waring	FFh FFh
16	PSUX Present	update	2h	update	20h	0h	4h	09h	81h~83h	08h	00h: Device Absent 01h: Device Present	FFh	FFh
17	PSU I2C Present	update	2h	update	20h	0h	4h	09h	7Fh	08h	00h: Device Absent 01h: Device Present	FFh	FFh
18	System Event	update	2h	update	01h	0h	4h	12h	83h	6Fh	05h:Timestamp Clock Synch	00h	FFh
19	PSUX Status	update	2h	update	20h	0h	4h	08h	84h~86h	6Fh	00h: Presence detected 01h: Power Supply Failure detected 03h: Power Supply input lost (AC/DC)	FFh	FFh
20	OS boot	update	2h	update	01h	0h	4h	1Fh	0h	6Fh	05h: ROM boot completed	00h	00h
21	I2C Hw Recovery	update	2h	update	20h	0h	4h	28h	AEh	71h	FFh	FFh	FFh
22	Monitor ASIC/IC	update	2h	update	20h	0h	4h	26h	ACh	71h	00h: RMC active -> non-active (default disable) 01h: RMC non-active -> active (default disable) FFh: IPMI stack or BMC Reboot (default disable)	FFh	FFh

SEL_List_20180409-Release.xls

5.12 FSC in BMC

The BMC samples the thermal sensors in real time and drives PWM output to an optimized speed.

5.13 BMC FW chip and Firmware Update

Supports remote OOB update F/W and local tool updates.

5.14 BMC Update Dual PCH flash

The MB/system does not have a dual PCH flash.

5.15 BMC Update and Access to CPLD

Supports remote OOB update F/W. The MB/system does not have CPLD.

5.16 BMC Time Sync

BMC time will sync with BIOS when BIOS POST or BMC reboots.

6. Thermal Design Requirements

To meet thermal reliability requirements, the thermal and cooling solutions should dissipate heat from the various components when the system is operating at maximum thermal power. The thermal solution can be found by setting a high power target for the initial design in order to avoid redesign of the cooling solution. However, the final system thermal solution should be optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. The thermal solution should not allow any overheating issues for any components in the system. The CPU and memory should not throttle due to any thermal issue under the following environment:

Inlet temperature lower than or equal to 35°C, and 0 inch H2O datacenter pressure with all FANs in each thermal zone running properly.

6.1 Data Center Environmental Conditions

The thermal design for the Intel Motherboard V4.0 needs to satisfy data center operational conditions as described below.

Data centers will generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with a 3°C standard deviation. The cold aisle temperature in a data center may fluctuate minutely depending to the outside air temperature of the data center. Every component in the system must be cooled and maintained below its maximum specified temperature for any cold aisle within the data center.

6.1.1 Cold-Aisle Temperature

Data centers will generally maintain cold-aisle temperatures between 18°C and 30°C (65°F to 85°F). This means that the temperature in the cold aisle is 24°C with a 3°C standard deviation. The cold-aisle temperature in a data center may fluctuate minutely depending to the outside air temperature of the data center. Every component in the system must be cooled and maintained below its maximum specified temperature in any cold aisle environment within the data center.

6.1.2 Cold-Aisle Pressurization

Data centers will maintain the cold aisle pressure between 0” H2O and 0.005” H2O.

The thermal solution of the system accommodates worst-case operational pressurization in the data center.

6.1.3 R.H

Most data centers will maintain a relative humidity of between 20% and 90%. The thermal solution must sustain uninterrupted operation of the system across the RH range.

6.2 Server operational condition

6.2.1 System Loading

The power consumption of individual components on the system motherboard will vary by application or by motherboard SKU. The total system power consumption may vary with use, or with the number of PCIe cards in the system.

Other system loading specifications:

- System loading: idle to 100%
- Number of PCIe full height or half height cards that can be installed: 0 to 2
- Number of PCIe Mezz cards that can be installed: 0 to 2
- Number of NF1 SSD: 0 to 36

A unified thermal solution that can cover 100% of system loading is preferred. However, an ODM can propose a non-unified thermal solution if there is an alternative way to improve costs, while the air-duct design should be unified for all SKUs.

6.2.2 DDR DIMM DRAM Operation

Thermal design should accommodate a DIMM maximum operating temperature of 85°C with a single refresh rate. Thermal test should be done based on a DIMM module‘s AVL (Approved Vendor List). The vendor should implement a BIOS and memory subsystem that optimizes the refresh rate and utilizes an optional DIMM Auto-Self-Refresh (ASR) based on the DIMM temperature. Implementation should follow an updated DDR4 memory controller and DIMM vendor’s specifications.

6.2.3 Inlet Temperature

The inlet air temperature will vary. The cooling system should cover inlet temperatures at 20°C, 25°C, 30°C, and 35°C. Cooling above 30°C is beyond the operating specification, but used during validation to demonstrate design margin. CPU throttling is not allowed to activate over the validation range of 20°C – 35°C.

6.2.4 Thermal Margin

The thermal margin is the difference between the maximum theoretically-safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component in the system. Otherwise, the thermal margin for every component is at least 7% for temperatures up to 30°C.

6.3 Thermal Kit Requirements

Thermal testing must be performed at an inlet temperature of up to_35°C (95°F) to guarantee reliability at high temperatures.

6.3.1 Heat Sink

The heat sink design should be the most optimized design with the lowest cost. The heat sink should be reliable and the most energy efficient design element, satisfying all the conditions described above. The number of heat pipes in the heat sink should not exceed three. The ODM can propose alternatives for different heat sink types if there is an alternative way to provide cost benefits. The heat sink should be accompanied by complex installation guidance, such as for air-flow direction.

6.3.2 System Fan

The system fan must be highly power-efficient with dual bearings. Any propagation of vibration caused by fan rotation should be minimized. The minimum frame size of the fan

is 40x40mm and the maximum frame size is 40x40mm. The ODM can propose a frame for a fan larger than 40x40mm if and only if there is alternative way to provide cost benefits. The maximum thickness of the fan should not be greater than 56mm. Each rotor in the fan should have a maximum of five wires. Except for the condition when one fan (or one rotor) fails, the fan power consumption in the system should not exceed 5% of total system power excluding fan power.

The system fan need not have back rush current in all conditions. System fan should have an inrush current of less than 1A on 12V per fan. When there is a step change in the fan PWM signal from low PWM to high PWM, there should be less than 10% of overshoot or no overshoot for fan input current. System should stay within its power envelope (300W for an Open Rack V1 configuration) under all conditions of fan operation.

6.3.3 Air-Duct

The air duct needs to be part of the motherboard tray cover. A highly energy efficient air-duct design should be simple and easily serviceable. In addition, the air-duct design should be unified for all SKUs. Using highly “green” or reusable material for the duct is preferred.

6.3.4 Thermal sensor

The maximum allowable tolerance of the thermal sensors for the motherboard is ±3°C.

7. I/O System

7.1 PCIe x32 Slot/Riser Card

PCIe risers are used to convert the PCIe slot connection to a cable connection, so that PCIe signals from the CPU can be connected to PCIe switches. To consider signal integrity and leave sufficient margins, as seen on the eye diagram, the riser card is comprised of a PCIE redrive and clock buffer to redrive PCIe signals before sending them to the cable connectors. Each riser also contains a DC-DC to support 12V to 3.3V of power for the on-board redrivers. The riser provides X8 PCIe lanes to the PCIe slot, and X24 PCIe lanes to the PCIe switch via cables.

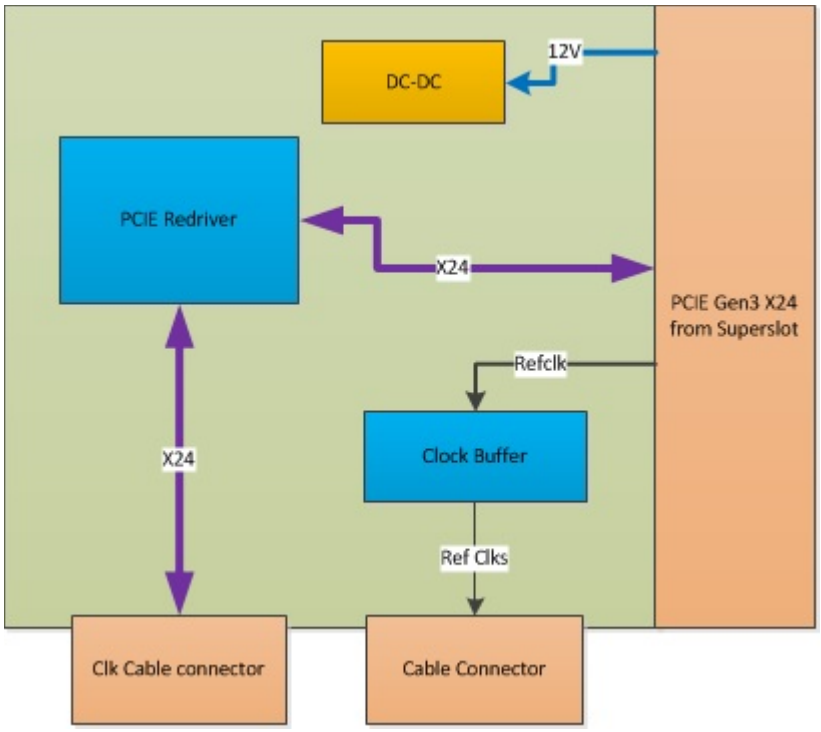


Figure 13 - NF1 (NGSFF) POC PCIe Riser

To provide flexibility for different user applications, we suggest use of a second riser that would provide X16 PCIe lanes to the PCIe slot, and X16 PCIe lanes to the PCIe switch. Such a configuration will allow users to include an X16 PCIe adding card with the system, such as an acceleration card, if more compute is needed. This will provide much more flexibility for selecting the ideal configuration based on user application needs.

The motherboard has two 2x sockets to be used by the PCIe riser cards. Each 2x socket contains:

- x32 slot Samtec/HSEC81-100-01-L-DV-A-K (200-pin) – used for x32 PCIe and power delivery.
- x16 slot Samtec/HSEC8-160-01-S-DV-A-K (120-pin) – used for x16 PCIe, side-band signal and power delivery.

The PCIe lane-to-riser card slot consists of two parts: CPU0 & CPU1. For individual connector definitions, please refer to the tables below:

Figure 14 - CN3

Table 8 - SAMTEC Connector definition for CPU0 (CN3)

+12V	1	2	+12V
GND	3	4	GND
CPU0_EXP2_TX_DP_0	5	6	CPU0_EXP2_RX_DP_0
CPU0_EXP2_TX_DN_0	7	8	CPU0_EXP2_RX_DN_0
GND	9	10	GND
CPU0_EXP2_TX_DP_1	11	12	CPU0_EXP2_RX_DP_1
CPU0_EXP2_TX_DN_1	13	14	CPU0_EXP2_RX_DN_1
GND	15	16	GND
CPU0_EXP2_TX_DP_2	17	18	CPU0_EXP2_RX_DP_2
CPU0_EXP2_TX_DN_2	19	20	CPU0_EXP2_RX_DN_2
GND	21	22	GND
CPU0_EXP2_TX_DP_3	23	24	CPU0_EXP2_RX_DP_3
CPU0_EXP2_TX_DN_3	25	26	CPU0_EXP2_RX_DN_3
GND	27	28	GND
CPU0_EXP2_TX_DP_4	29	30	CPU0_EXP2_RX_DP_4
CPU0_EXP2_TX_DN_4	31	32	CPU0_EXP2_RX_DN_4
GND	33	34	GND
CPU0_EXP2_TX_DP_5	35	36	CPU0_EXP2_RX_DP_5
CPU0_EXP2_TX_DN_5	37	38	CPU0_EXP2_RX_DN_5
GND	39	40	GND
CPU0_EXP2_TX_DP_6	41	42	CPU0_EXP2_RX_DP_6
CPU0_EXP2_TX_DN_6	43	44	CPU0_EXP2_RX_DN_6
GND	45	46	GND
CPU0_EXP2_TX_DP_7	47	48	CPU0_EXP2_RX_DP_7
CPU0_EXP2_TX_DN_7	49	50	CPU0_EXP2_RX_DN_7
GND	51	52	GND
CPU0_EXP2_TX_DP_8	53	54	CPU0_EXP2_RX_DP_8
CPU0_EXP2_TX_DN_8	55	56	CPU0_EXP2_RX_DN_8
GND	57	58	GND
CPU0_EXP2_TX_DP_9	59	60	CPU0_EXP2_RX_DP_9
CPU0_EXP2_TX_DN_9	61	62	CPU0_EXP2_RX_DN_9
GND	63	64	GND
GND	65	66	GND
CPU0_EXP2_TX_DP_10	67	68	CPU0_EXP2_RX_DP_10

CPU0_EXP2_TX_DN_10	69	70	CPU0_EXP2_RX_DN_10
GND	71	72	GND
CPU0_EXP2_TX_DP_11	73	74	CPU0_EXP2_RX_DP_11
CPU0_EXP2_TX_DN_11	75	76	CPU0_EXP2_RX_DN_11
GND	77	78	GND
CPU0_EXP2_TX_DP_12	79	80	CPU0_EXP2_RX_DP_12
CPU0_EXP2_TX_DN_12	81	82	CPU0_EXP2_RX_DN_12
GND	83	84	GND
CPU0_EXP2_TX_DP_13	85	86	CPU0_EXP2_RX_DP_13
CPU0_EXP2_TX_DN_13	87	88	CPU0_EXP2_RX_DN_13
GND	89	90	GND
CPU0_EXP2_TX_DP_14	91	92	CPU0_EXP2_RX_DP_14
CPU0_EXP2_TX_DN_14	93	94	CPU0_EXP2_RX_DN_14
GND	95	96	GND
CPU0_EXP2_TX_DP_15	97	98	CPU0_EXP2_RX_DP_15
CPU0_EXP2_TX_DN_15	99	100	CPU0_EXP2_RX_DN_15
GND	101	102	GND
CPU0_EXP3_TX_DP_0	103	104	CPU0_EXP3_RX_DP_0
CPU0_EXP3_TX_DN_0	105	106	CPU0_EXP3_RX_DN_0
GND	107	108	GND
CPU0_EXP3_TX_DP_1	109	110	CPU0_EXP3_RX_DP_1
CPU0_EXP3_TX_DN_1	111	112	CPU0_EXP3_RX_DN_1
GND	113	114	GND
CPU0_EXP3_TX_DP_2	115	116	CPU0_EXP3_RX_DP_2
CPU0_EXP3_TX_DN_2	117	118	CPU0_EXP3_RX_DN_2
GND	119	120	GND
CPU0_EXP3_TX_DP_3	121	122	CPU0_EXP3_RX_DP_3
CPU0_EXP3_TX_DN_3	123	124	CPU0_EXP3_RX_DN_3
GND	125	126	GND
CPU0_EXP3_TX_DP_4	127	128	CPU0_EXP3_RX_DP_4
CPU0_EXP3_TX_DN_4	129	130	CPU0_EXP3_RX_DN_4
GND	131	132	GND
CPU0_EXP3_TX_DP_5	133	134	CPU0_EXP3_RX_DP_5
CPU0_EXP3_TX_DN_5	135	136	CPU0_EXP3_RX_DN_5
GND	137	138	GND
CPU0_EXP3_TX_DP_6	139	140	CPU0_EXP3_RX_DP_6
CPU0_EXP3_TX_DN_6	141	142	CPU0_EXP3_RX_DN_6
GND	143	144	GND
CPU0_EXP3_TX_DP_7	145	146	CPU0_EXP3_RX_DP_7
CPU0_EXP3_TX_DN_7	147	148	CPU0_EXP3_RX_DN_7
GND	149	150	GND
CPU0_EXP3_TX_DP_8	151	152	CPU0_EXP3_RX_DP_8
CPU0_EXP3_TX_DN_8	153	154	CPU0_EXP3_RX_DN_8
GND	155	156	GND
CPU0_EXP3_TX_DP_9	157	158	CPU0_EXP3_RX_DP_9
CPU0_EXP3_TX_DN_9	159	160	CPU0_EXP3_RX_DN_9
GND	161	162	GND
CPU0_EXP3_TX_DP_10	163	164	CPU0_EXP3_RX_DP_10
CPU0_EXP3_TX_DN_10	165	166	CPU0_EXP3_RX_DN_10
GND	167	168	GND

CPU0_EXP3_TX_DP_11	169	170	CPU0_EXP3_RX_DP_11
CPU0_EXP3_TX_DN_11	171	172	CPU0_EXP3_RX_DN_11
GND	173	174	GND
CPU0_EXP3_TX_DP_12	175	176	CPU0_EXP3_RX_DP_12
CPU0_EXP3_TX_DN_12	177	178	CPU0_EXP3_RX_DN_12
GND	179	180	GND
CPU0_EXP3_TX_DP_13	181	182	CPU0_EXP3_RX_DP_13
CPU0_EXP3_TX_DN_13	183	184	CPU0_EXP3_RX_DN_13
GND	185	186	GND
CPU0_EXP3_TX_DP_14	187	188	CPU0_EXP3_RX_DP_14
CPU0_EXP3_TX_DN_14	189	190	CPU0_EXP3_RX_DN_14
GND	191	192	GND
CPU0_EXP3_TX_DP_15	193	194	CPU0_EXP3_RX_DP_15
CPU0_EXP3_TX_DN_15	195	196	CPU0_EXP3_RX_DN_15
GND	197	198	GND
PCH_WAKE_N	199	200	RST_PCIE_SLOT_0

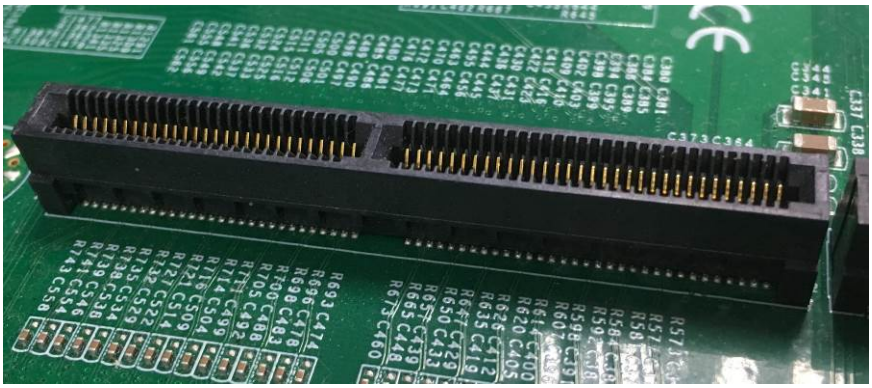


Figure 15 - CN8

Table 9 - SAMTEC Connector definition for CPU0 (CN8)

+12V	1	2	+12V
+12V	3	4	+12V
++3.3V	5	6	+12V
+3.3V	7	8	+3.3V
+3.3V_DUAL	9	10	GND
CPU0_HP_I2C_CLK	11	12	CLK_100M_PCIE1_P
CPU0_HP_I2C_DAT	13	14	CLK_100M_PCIE1_N
GND	15	16	GND
CPU0_EXP1_TX_DP_15	17	18	CPU0_EXP1_RX_DP_15
CPU0_EXP1_TX_DN_15	19	20	CPU0_EXP1_RX_DN_15
GND	21	22	GND
CPU0_EXP1_TX_DP_14	23	24	CPU0_EXP1_RX_DP_14
CPU0_EXP1_TX_DN_14	25	26	CPU0_EXP1_RX_DN_14
GND	27	28	GND
CPU0_EXP1_TX_DP_13	29	30	CPU0_EXP1_RX_DP_13
CPU0_EXP1_TX_DN_13	31	32	CPU0_EXP1_RX_DN_13
GND	33	34	GND
CPU0_EXP1_TX_DP_12	35	36	CPU0_EXP1_RX_DP_12
CPU0_EXP1_TX_DN_12	37	38	CPU0_EXP1_RX_DN_12
GND	39	40	GND
CPU0_EXP1_TX_DP_11	41	42	CPU0_EXP1_RX_DP_11
CPU0_EXP1_TX_DN_11	43	44	CPU0_EXP1_RX_DN_11
GND	45	46	GND
CPU0_EXP1_TX_DP_10	47	48	CPU0_EXP1_RX_DP_10
CPU0_EXP1_TX_DN_10	49	50	CPU0_EXP1_RX_DN_10
GND	51	52	GND
CPU0_EXP1_TX_DP_9	53	54	CPU0_EXP1_RX_DP_9
CPU0_EXP1_TX_DN_9	55	56	CPU0_EXP1_RX_DN_9
GND	57	58	GND
CPU0_EXP1_TX_DP_8	59	60	CPU0_EXP1_RX_DP_8
CPU0_EXP1_TX_DN_8	61	62	CPU0_EXP1_RX_DN_8
GND	63	64	GND
GND	65	66	GND

CPU0_EXP1_TX_DP_7	67	68	CPU0_EXP1_RX_DP_7
CPU0_EXP1_TX_DN_7	69	70	CPU0_EXP1_RX_DN_7
GND	71	72	GND
CPU0_EXP1_TX_DP_6	73	74	CPU0_EXP1_RX_DP_6
CPU0_EXP1_TX_DN_6	75	76	CPU0_EXP1_RX_DN_6
GND	77	78	GND
CPU0_EXP1_TX_DP_5	79	80	CPU0_EXP1_RX_DP_5
CPU0_EXP1_TX_DN_5	81	82	CPU0_EXP1_RX_DN_5
GND	83	84	GND
CPU0_EXP1_TX_DP_4	85	86	CPU0_EXP1_RX_DP_4
CPU0_EXP1_TX_DN_4	87	88	CPU0_EXP1_RX_DN_4
GND	89	90	GND
CPU0_EXP1_TX_DP_3	91	92	CPU0_EXP1_RX_DP_3
CPU0_EXP1_TX_DN_3	93	94	CPU0_EXP1_RX_DN_3
GND	95	96	GND
CPU0_EXP1_TX_DP_2	97	98	CPU0_EXP1_RX_DP_2
CPU0_EXP1_TX_DN_2	99	100	CPU0_EXP1_RX_DN_2
GND	101	102	GND
CPU0_EXP1_TX_DP_1	103	104	CPU0_EXP1_RX_DP_1
CPU0_EXP1_TX_DN_1	105	106	CPU0_EXP1_RX_DN_1
GND	107	108	GND
CPU0_EXP1_TX_DP_0	109	110	CPU0_EXP1_RX_DP_0
CPU0_EXP1_TX_DN_0	111	112	CPU0_EXP1_RX_DN_0
GND	113	114	GND
PCIE_SMCLK_0	115	116	CLK_100M_PCIE2_P
PCIE_SMDAT_0	117	118	CLK_100M_PCIE2_N
BMC_GPIOG5	119	120	PCH_GPP_C8

Figure 16 - CN4

Table 10 - SAMTEC Connector definition for CPU1 (CN4)

+12V	1	2	+12V
GND	3	4	GND
CPU1_EXP2_TX_DP_0	5	6	CPU1_EXP2_RX_DP_0
CPU1_EXP2_TX_DN_0	7	8	CPU1_EXP2_RX_DN_0
GND	9	10	GND
CPU1_EXP2_TX_DP_1	11	12	CPU1_EXP2_RX_DP_1
CPU1_EXP2_TX_DN_1	13	14	CPU1_EXP2_RX_DN_1
GND	15	16	GND
CPU1_EXP2_TX_DP_2	17	18	CPU1_EXP2_RX_DP_2
CPU1_EXP2_TX_DN_2	19	20	CPU1_EXP2_RX_DN_2
GND	21	22	GND
CPU1_EXP2_TX_DP_3	23	24	CPU1_EXP2_RX_DP_3
CPU1_EXP2_TX_DN_3	25	26	CPU1_EXP2_RX_DN_3
GND	27	28	GND
CPU1_EXP2_TX_DP_4	29	30	CPU1_EXP2_RX_DP_4
CPU1_EXP2_TX_DN_4	31	32	CPU1_EXP2_RX_DN_4
GND	33	34	GND
CPU1_EXP2_TX_DP_5	35	36	CPU1_EXP2_RX_DP_5
CPU1_EXP2_TX_DN_5	37	38	CPU1_EXP2_RX_DN_5
GND	39	40	GND
CPU1_EXP2_TX_DP_6	41	42	CPU1_EXP2_RX_DP_6
CPU1_EXP2_TX_DN_6	43	44	CPU1_EXP2_RX_DN_6
GND	45	46	GND
CPU1_EXP2_TX_DP_7	47	48	CPU1_EXP2_RX_DP_7
CPU1_EXP2_TX_DN_7	49	50	CPU1_EXP2_RX_DN_7
GND	51	52	GND
CPU1_EXP2_TX_DP_8	53	54	CPU1_EXP2_RX_DP_8
CPU1_EXP2_TX_DN_8	55	56	CPU1_EXP2_RX_DN_8
GND	57	58	GND
CPU1_EXP2_TX_DP_9	59	60	CPU1_EXP2_RX_DP_9
CPU1_EXP2_TX_DN_9	61	62	CPU1_EXP2_RX_DN_9
GND	63	64	GND
GND	65	66	GND
CPU1_EXP2_TX_DP_10	67	68	CPU1_EXP2_RX_DP_10
CPU1_EXP2_TX_DN_10	69	70	CPU1_EXP2_RX_DN_10
GND	71	72	GND
CPU1_EXP2_TX_DP_11	73	74	CPU1_EXP2_RX_DP_11
CPU1_EXP2_TX_DN_11	75	76	CPU1_EXP2_RX_DN_11
GND	77	78	GND
CPU1_EXP2_TX_DP_12	79	80	CPU1_EXP2_RX_DP_12
CPU1_EXP2_TX_DN_12	81	82	CPU1_EXP2_RX_DN_12
GND	83	84	GND
CPU1_EXP2_TX_DP_13	85	86	CPU1_EXP2_RX_DP_13
CPU1_EXP2_TX_DN_13	87	88	CPU1_EXP2_RX_DN_13
GND	89	90	GND
CPU1_EXP2_TX_DP_14	91	92	CPU1_EXP2_RX_DP_14
CPU1_EXP2_TX_DN_14	93	94	CPU1_EXP2_RX_DN_14
GND	95	96	GND
CPU1_EXP2_TX_DP_15	97	98	CPU1_EXP2_RX_DP_15
CPU1_EXP2_TX_DN_15	99	100	CPU1_EXP2_RX_DN_15

GND	101	102	GND
CPU1_EXP3_TX_DP_0	103	104	CPU1_EXP3_RX_DP_0
CPU1_EXP3_TX_DN_0	105	106	CPU1_EXP3_RX_DN_0
GND	107	108	GND
CPU1_EXP3_TX_DP_1	109	110	CPU1_EXP3_RX_DP_1
CPU1_EXP3_TX_DN_1	111	112	CPU1_EXP3_RX_DN_1
GND	113	114	GND
CPU1_EXP3_TX_DP_2	115	116	CPU1_EXP3_RX_DP_2
CPU1_EXP3_TX_DN_2	117	118	CPU1_EXP3_RX_DN_2
GND	119	120	GND
CPU1_EXP3_TX_DP_3	121	122	CPU1_EXP3_RX_DP_3
CPU1_EXP3_TX_DN_3	123	124	CPU1_EXP3_RX_DN_3
GND	125	126	GND
CPU1_EXP3_TX_DP_4	127	128	CPU1_EXP3_RX_DP_4
CPU1_EXP3_TX_DN_4	129	130	CPU1_EXP3_RX_DN_4
GND	131	132	GND
CPU1_EXP3_TX_DP_5	133	134	CPU1_EXP3_RX_DP_5
CPU1_EXP3_TX_DN_5	135	136	CPU1_EXP3_RX_DN_5
GND	137	138	GND
CPU1_EXP3_TX_DP_6	139	140	CPU1_EXP3_RX_DP_6
CPU1_EXP3_TX_DN_6	141	142	CPU1_EXP3_RX_DN_6
GND	143	144	GND
CPU1_EXP3_TX_DP_7	145	146	CPU1_EXP3_RX_DP_7
CPU1_EXP3_TX_DN_7	147	148	CPU1_EXP3_RX_DN_7
GND	149	150	GND
CPU1_EXP3_TX_DP_8	151	152	CPU1_EXP3_RX_DP_8
CPU1_EXP3_TX_DN_8	153	154	CPU1_EXP3_RX_DN_8
GND	155	156	GND
CPU1_EXP3_TX_DP_9	157	158	CPU1_EXP3_RX_DP_9
CPU1_EXP3_TX_DN_9	159	160	CPU1_EXP3_RX_DN_9
GND	161	162	GND
CPU1_EXP3_TX_DP_10	163	164	CPU1_EXP3_RX_DP_10
CPU1_EXP3_TX_DN_10	165	166	CPU1_EXP3_RX_DN_10
GND	167	168	GND
CPU1_EXP3_TX_DP_11	169	170	CPU1_EXP3_RX_DP_11
CPU1_EXP3_TX_DN_11	171	172	CPU1_EXP3_RX_DN_11
GND	173	174	GND
CPU1_EXP3_TX_DP_12	175	176	CPU1_EXP3_RX_DP_12
CPU1_EXP3_TX_DN_12	177	178	CPU1_EXP3_RX_DN_12
GND	179	180	GND
CPU1_EXP3_TX_DP_13	181	182	CPU1_EXP3_RX_DP_13
CPU1_EXP3_TX_DN_13	183	184	CPU1_EXP3_RX_DN_13
GND	185	186	GND
CPU1_EXP3_TX_DP_14	187	188	CPU1_EXP3_RX_DP_14
CPU1_EXP3_TX_DN_14	189	190	CPU1_EXP3_RX_DN_14
GND	191	192	GND
CPU1_EXP3_TX_DP_15	193	194	CPU1_EXP3_RX_DP_15
CPU1_EXP3_TX_DN_15	195	196	CPU1_EXP3_RX_DN_15
GND	197	198	GND
PCH_WAKE_N	199	200	RST_PCIE_SLOT_1

Figure 17 - CN9

Table 11 - SAMTEC Connector definition for CPU1 (CN9)

+12V	1	2	+12V
+12V	3	4	+12V
++3.3V	5	6	+12V
+3.3V	7	8	+3.3V
+3.3V_DUAL	9	10	GND
CPU1_HP_I2C_CLK	11	12	CLK_100M_PCIE3_P
CPU1_HP_I2C_DAT	13	14	CLK_100M_PCIE3_N
GND	15	16	GND
CPU1_EXP1_TX_DP_15	17	18	CPU1_EXP1_RX_DP_15
CPU1_EXP1_TX_DN_15	19	20	CPU1_EXP1_RX_DN_15
GND	21	22	GND
CPU1_EXP1_TX_DP_14	23	24	CPU1_EXP1_RX_DP_14
CPU1_EXP1_TX_DN_14	25	26	CPU1_EXP1_RX_DN_14
GND	27	28	GND
CPU1_EXP1_TX_DP_13	29	30	CPU1_EXP1_RX_DP_13
CPU1_EXP1_TX_DN_13	31	32	CPU1_EXP1_RX_DN_13
GND	33	34	GND
CPU1_EXP1_TX_DP_12	35	36	CPU1_EXP1_RX_DP_12
CPU1_EXP1_TX_DN_12	37	38	CPU1_EXP1_RX_DN_12
GND	39	40	GND
CPU1_EXP1_TX_DP_11	41	42	CPU1_EXP1_RX_DP_11
CPU1_EXP1_TX_DN_11	43	44	CPU1_EXP1_RX_DN_11
GND	45	46	GND
CPU1_EXP1_TX_DP_10	47	48	CPU1_EXP1_RX_DP_10
CPU1_EXP1_TX_DN_10	49	50	CPU1_EXP1_RX_DN_10
GND	51	52	GND
CPU1_EXP1_TX_DP_9	53	54	CPU1_EXP1_RX_DP_9
CPU1_EXP1_TX_DN_9	55	56	CPU1_EXP1_RX_DN_9
GND	57	58	GND
CPU1_EXP1_TX_DP_8	59	60	CPU1_EXP1_RX_DP_8
CPU1_EXP1_TX_DN_8	61	62	CPU1_EXP1_RX_DN_8
GND	63	64	GND
GND	65	66	GND
CPU1_EXP1_TX_DP_7	67	68	CPU1_EXP1_RX_DP_7
CPU1_EXP1_TX_DN_7	69	70	CPU1_EXP1_RX_DN_7
GND	71	72	GND

CPU1_EXP1_TX_DP_6	73	74	CPU1_EXP1_RX_DP_6
CPU1_EXP1_TX_DN_6	75	76	CPU1_EXP1_RX_DN_6
GND	77	78	GND
CPU1_EXP1_TX_DP_5	79	80	CPU1_EXP1_RX_DP_5
CPU1_EXP1_TX_DN_5	81	82	CPU1_EXP1_RX_DN_5
GND	83	84	GND
CPU1_EXP1_TX_DP_4	85	86	CPU1_EXP1_RX_DP_4
CPU1_EXP1_TX_DN_4	87	88	CPU1_EXP1_RX_DN_4
GND	89	90	GND
CPU1_EXP1_TX_DP_3	91	92	CPU1_EXP1_RX_DP_3
CPU1_EXP1_TX_DN_3	93	94	CPU1_EXP1_RX_DN_3
GND	95	96	GND
CPU1_EXP1_TX_DP_2	97	98	CPU1_EXP1_RX_DP_2
CPU1_EXP1_TX_DN_2	99	100	CPU1_EXP1_RX_DN_2
GND	101	102	GND
CPU1_EXP1_TX_DP_1	103	104	CPU1_EXP1_RX_DP_1
CPU1_EXP1_TX_DN_1	105	106	CPU1_EXP1_RX_DN_1
GND	107	108	GND
CPU1_EXP1_TX_DP_0	109	110	CPU1_EXP1_RX_DP_0
CPU1_EXP1_TX_DN_0	111	112	CPU1_EXP1_RX_DN_0
GND	113	114	GND
PCIE_SMCLK_1	115	116	CLK_100M_PCIE4_P
PCIE_SMDAT_1	117	118	CLK_100M_PCIE4_N
BMC_GPIOG6	119	120	PCH_GPP_B11

In the Mission Peak system, the block diagram for the riser card is shown below:

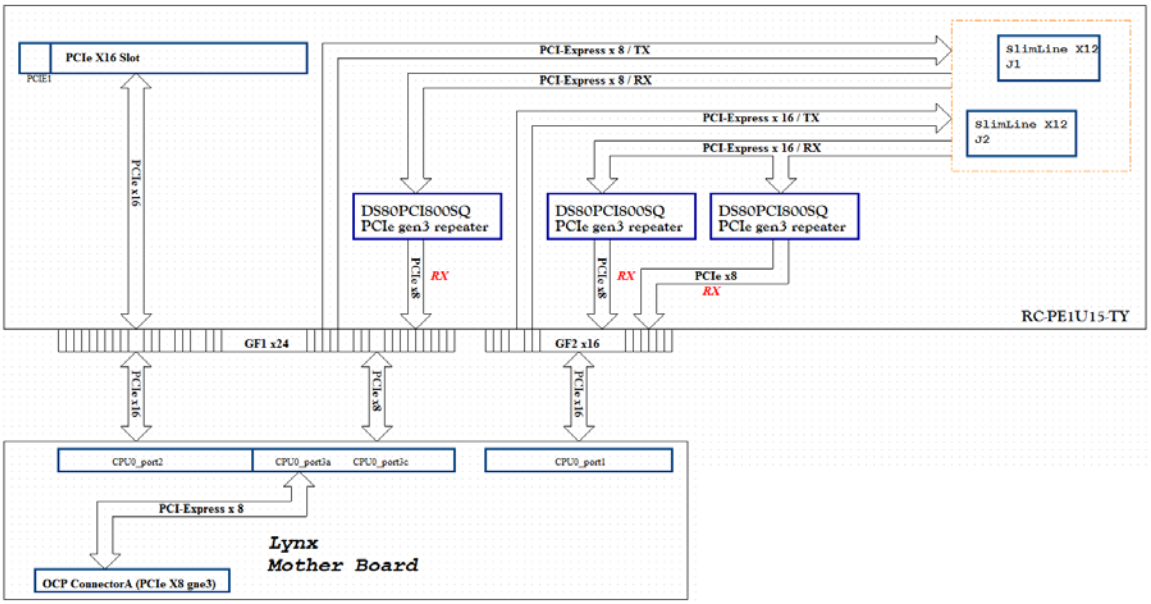


Figure 18 - RC-PE1U15-TY Block Diagram

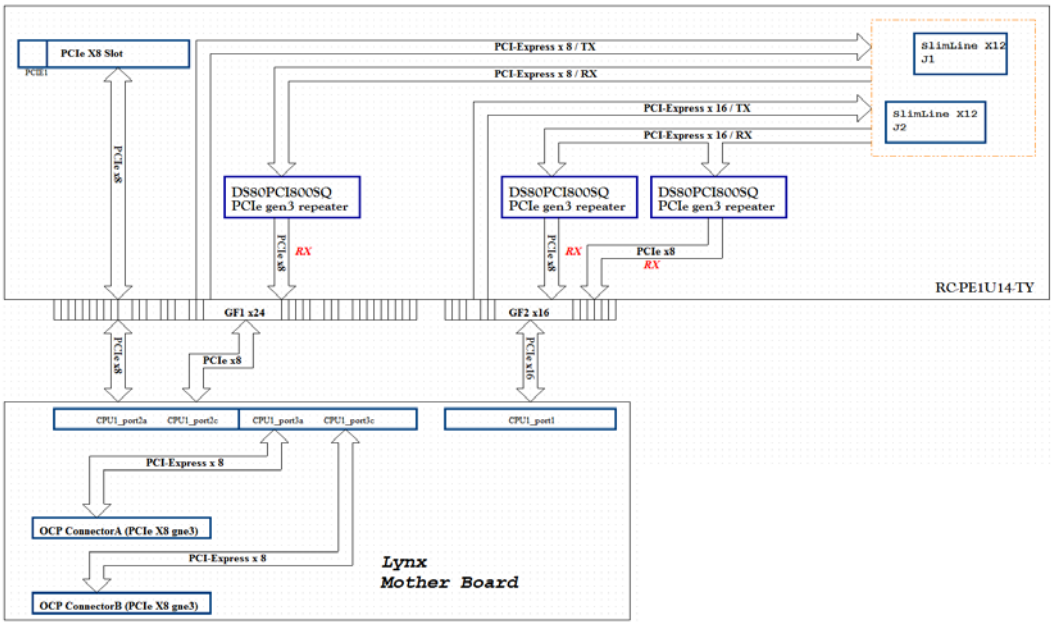


Figure 19 - RC-PE1U14-TY Block Diagram

7.1.1 Riser Card: RC-PE1U15-TY

The RC-PE1U15-TY is assembled on the motherboard with CN3 and CN8, which consist of one PCIe x16 slot and two slimline x12 of 74P connectors. The PCB placement and connector pin definition is as follows:

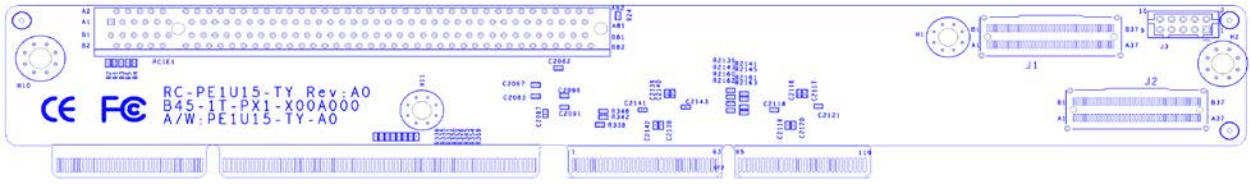


Figure 20 - PCBA Placement of RC-PE1U15-TY

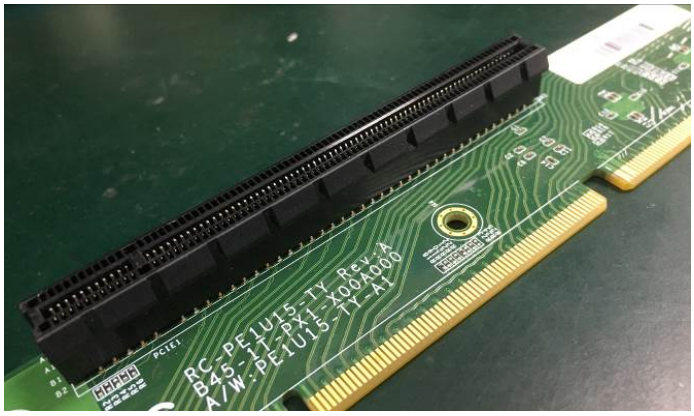


Figure 21 - PCIE x16 slot PCIE1

Table 12 - PCIE x16 slot Connector Pin-Out (PCIE1)

Pin	Description	Pin	Description
A1	GND	B1	+12V
A2	+12V	B2	+12V
A3	+12V	B3	+12V
A4	GND	B4	GND
A5	GND	B5	PCIE_SMCLK
A6	+3.3V	B6	PCIE_SMDAT
A7	NC	B7	GND
A8	+3.3V	B8	+3.3V
A9	+3.3V	B9	GND
A10	+3.3V	B10	+3.3V_DUAL
A11	RST_PCIE_SLOT	B11	PCH_WAKE_N
A12	GND	B12	NC
A13	CLK_100M_PCIE1_P	B13	GND
A14	CLK_100M_PCIE1_N	B14	CPU0_EXP2_TX_DP_0
A15	GND	B15	CPU0_EXP2_TX_DN_0
A16	CPU0_EXP2_RX_DP_0	B16	GND
A17	CPU0_EXP2_RX_DN_0	B17	GND
A18	GND	B18	GND
A19	NC	B19	CPU0_EXP2_TX_DP_1
A20	GND	B20	CPU0_EXP2_TX_DN_1
A21	CPU0_EXP2_RX_DP_1	B21	GND
A22	CPU0_EXP2_RX_DN_1	B22	GND
A23	GND	B23	CPU0_EXP2_TX_DP_2
A24	GND	B24	CPU0_EXP2_TX_DN_2
A25	CPU0_EXP2_RX_DP_2	B25	GND
A26	CPU0_EXP2_RX_DN_2	B26	GND
A27	GND	B27	CPU0_EXP2_TX_DP_3
A28	GND	B28	CPU0_EXP2_TX_DN_3
A29	CPU0_EXP2_RX_DP_3	B29	GND
A30	CPU0_EXP2_RX_DN_3	B30	NC
A31	GND	B31	GND
A32	NC	B32	GND
A33	NC	B33	CPU0_EXP2_TX_DP_4
A34	GND	B34	CPU0_EXP2_TX_DN_4
A35	CPU0_EXP2_RX_DP_4	B35	GND
A36	CPU0_EXP2_RX_DN_4	B36	GND
A37	GND	B37	CPU0_EXP2_TX_DP_5
A38	GND	B38	CPU0_EXP2_TX_DN_5
A39	CPU0_EXP2_RX_DP_5	B39	GND
A40	CPU0_EXP2_RX_DN_5	B40	GND
A41	GND	B41	CPU0_EXP2_TX_DP_6
A42	GND	B42	CPU0_EXP2_TX_DN_6
A43	CPU0_EXP2_RX_DP_6	B43	GND
A44	CPU0_EXP2_RX_DN_6	B44	GND
A45	GND	B45	CPU0_EXP2_TX_DP_7
A46	GND	B46	CPU0_EXP2_TX_DN_7

A47	CPU0_EXP2_RX_DP_7	B47	GND
A48	CPU0_EXP2_RX_DN_7	B48	GND
A49	GND	B49	GND
A50	NC	B50	CPU0_EXP2_TX_DP_8
A51	GND	B51	CPU0_EXP2_TX_DN_8
A52	CPU0_EXP2_RX_DP_8	B52	GND
A53	CPU0_EXP2_RX_DN_8	B53	GND
A54	GND	B54	CPU0_EXP2_TX_DP_9
A55	GND	B55	CPU0_EXP2_TX_DN_9
A56	CPU0_EXP2_RX_DP_9	B56	GND
A57	CPU0_EXP2_RX_DN_9	B57	GND
A58	GND	B58	CPU0_EXP2_TX_DP_10
A59	GND	B59	CPU0_EXP2_TX_DN_10
A60	CPU0_EXP2_RX_DP_10	B60	GND
A61	CPU0_EXP2_RX_DN_10	B61	GND
A62	GND	B62	CPU0_EXP2_TX_DP_11
A63	GND	B63	CPU0_EXP2_TX_DN_11
A64	CPU0_EXP2_RX_DP_11	B64	GND
A65	CPU0_EXP2_RX_DN_11	B65	GND
A66	GND	B66	CPU0_EXP2_TX_DP_12
A67	GND	B67	CPU0_EXP2_TX_DN_12
A68	CPU0_EXP2_RX_DP_12	B68	GND
A69	CPU0_EXP2_RX_DN_12	B69	GND
A70	GND	B70	CPU0_EXP2_TX_DP_13
A71	GND	B71	CPU0_EXP2_TX_DN_13
A72	CPU0_EXP2_RX_DP_13	B72	GND
A73	CPU0_EXP2_RX_DN_13	B73	GND
A74	GND	B74	CPU0_EXP2_TX_DP_14
A75	GND	B75	CPU0_EXP2_TX_DN_14
A76	CPU0_EXP2_RX_DP_14	B76	GND
A77	CPU0_EXP2_RX_DN_14	B77	GND
A78	GND	B78	CPU0_EXP2_TX_DP_15
A79	GND	B79	CPU0_EXP2_TX_DN_15
A80	CPU0_EXP2_RX_DP_15	B80	GND
A81	CPU0_EXP2_RX_DN_15	B81	GND
A82	GND	B82	NC

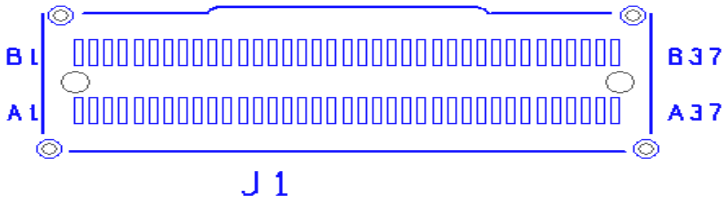


Figure 22 - Slimline Connector J1

Table 13 - Slimline 74P Connector Pin-Out (J1)

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU0_EXP3_TX_DP_8	B2	CPU0_EXP3_RX_DP_R_8
A3	CPU0_EXP3_TX_DN_8	B3	CPU0_EXP3_RX_DN_R_8
A4	GND	B4	GND
A5	CPU0_EXP3_TX_DP_9	B5	CPU0_EXP3_RX_DP_R_9
A6	CPU0_EXP3_TX_DN_9	B6	CPU0_EXP3_RX_DN_R_9
A7	GND	B7	GND
A8	CPU0_EXP3_TX_DP_10	B8	CPU0_EXP3_RX_DP_R_10
A9	CPU0_EXP3_TX_DN_10	B9	CPU0_EXP3_RX_DN_R_10
A10	GND	B10	GND
A11	CPU0_EXP3_TX_DP_11	B11	CPU0_EXP3_RX_DP_R_11
A12	CPU0_EXP3_TX_DN_11	B12	CPU0_EXP3_RX_DN_R_11
A13	GND	B13	GND
A14	CPU0_EXP3_TX_DP_12	B14	CPU0_EXP3_RX_DP_R_12
A15	CPU0_EXP3_TX_DN_12	B15	CPU0_EXP3_RX_DN_R_12
A16	GND	B16	GND
A17	CPU0_EXP3_TX_DP_13	B17	CPU0_EXP3_RX_DP_R_13
A18	CPU0_EXP3_TX_DN_13	B18	CPU0_EXP3_RX_DN_R_13
A19	GND	B19	GND
A20	CPU0_EXP3_TX_DP_14	B20	CPU0_EXP3_RX_DP_R_14
A21	CPU0_EXP3_TX_DN_14	B21	CPU0_EXP3_RX_DN_R_14
A22	GND	B22	GND
A23	CPU0_EXP3_TX_DP_15	B23	CPU0_EXP3_RX_DP_R_15
A24	CPU0_EXP3_TX_DN_15	B24	CPU0_EXP3_RX_DN_R_15
A25	GND	B25	GND
A26	CPU0_EXP1_TX_DP_15	B26	CPU0_EXP1_RX_DP_R_15
A27	CPU0_EXP1_TX_DN_15	B27	CPU0_EXP1_RX_DN_R_15
A28	GND	B28	GND
A29	CPU0_EXP1_TX_DP_14	B29	CPU0_EXP1_RX_DP_R_14
A30	CPU0_EXP1_TX_DN_14	B30	CPU0_EXP1_RX_DN_R_14
A31	GND	B31	GND
A32	CPU0_EXP1_TX_DP_13	B32	CPU0_EXP1_RX_DP_R_13
A33	CPU0_EXP1_TX_DN_13	B33	CPU0_EXP1_RX_DN_R_13
A34	GND	B34	GND
A35	CPU0_EXP1_TX_DP_12	B35	CPU0_EXP1_RX_DP_R_12
A36	CPU0_EXP1_TX_DN_12	B36	CPU0_EXP1_RX_DN_R_12
A37	GND	B37	GND

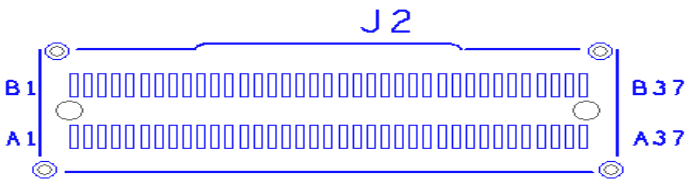


Figure 23 - Slimline Connector J2

Table 14 - Slimline 74P Connector Pin-Out (J2)

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU0_EXP1_TX_DN_0	B2	CPU0_EXP1_RX_DN_R_0
A3	CPU0_EXP1_TX_DP_0	B3	CPU0_EXP1_RX_DP_R_0
A4	GND	B4	GND
A5	CPU0_EXP1_TX_DN_1	B5	CPU0_EXP1_RX_DN_R_1
A6	CPU0_EXP1_TX_DP_1	B6	CPU0_EXP1_RX_DP_R_1
A7	GND	B7	GND
A8	CPU0_EXP1_TX_DN_2	B8	CPU0_EXP1_RX_DN_R_2
A9	CPU0_EXP1_TX_DP_2	B9	CPU0_EXP1_RX_DP_R_2
A10	GND	B10	GND
A11	CPU0_EXP1_TX_DN_3	B11	CPU0_EXP1_RX_DN_R_3
A12	CPU0_EXP1_TX_DP_3	B12	CPU0_EXP1_RX_DP_R_3
A13	GND	B13	GND
A14	CPU0_EXP1_TX_DN_4	B14	CPU0_EXP1_RX_DN_R_4
A15	CPU0_EXP1_TX_DP_4	B15	CPU0_EXP1_RX_DP_R_4
A16	GND	B16	GND
A17	CPU0_EXP1_TX_DN_5	B17	CPU0_EXP1_RX_DN_R_5
A18	CPU0_EXP1_TX_DP_5	B18	CPU0_EXP1_RX_DP_R_5
A19	GND	B19	GND
A20	CPU0_EXP1_TX_DN_6	B20	CPU0_EXP1_RX_DN_R_6
A21	CPU0_EXP1_TX_DP_6	B21	CPU0_EXP1_RX_DP_R_6
A22	GND	B22	GND
A23	CPU0_EXP1_TX_DN_7	B23	CPU0_EXP1_RX_DN_R_7
A24	CPU0_EXP1_TX_DP_7	B24	CPU0_EXP1_RX_DP_R_7
A25	GND	B25	GND
A26	CPU0_EXP1_TX_DN_8	B26	CPU0_EXP1_RX_DN_R_8
A27	CPU0_EXP1_TX_DP_8	B27	CPU0_EXP1_RX_DP_R_8
A28	GND	B28	GND
A29	CPU0_EXP1_TX_DN_9	B29	CPU0_EXP1_RX_DN_R_9
A30	CPU0_EXP1_TX_DP_9	B30	CPU0_EXP1_RX_DP_R_9
A31	GND	B31	GND
A32	CPU0_EXP1_TX_DN_10	B32	CPU0_EXP1_RX_DN_R_10
A33	CPU0_EXP1_TX_DP_10	B33	CPU0_EXP1_RX_DP_R_10
A34	GND	B34	GND
A35	CPU0_EXP1_TX_DN_11	B35	CPU0_EXP1_RX_DN_R_11
A36	CPU0_EXP1_TX_DP_11	B36	CPU0_EXP1_RX_DP_R_11
A37	GND	B37	GND

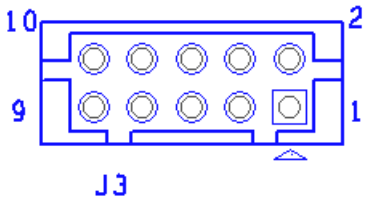


Figure 24 - 2x5P Box-Header J3

Table 15 - 2x5P Box-Header Pin-Out (J3)

Pin	Description	Pin	Description
1	BMC_GPIOG6	2	+3.3V
3	GND	4	PCH_WAKE_N
5	CLK_100M_PCIE4_P	6	RST_PCIE_SLOT
7	CLK_100M_PCIE4_N	8	CPU1_HP_I2C_CLK
9	PCH_GPP_B11	10	CPU1_HP_I2C_DAT

7.1.2 Riser Card: RC-PE1U14-TY

The RC-PE1U14-TY is being assembled on motherboard housings CN4 and CN9, which consist of one PCIe x8 slot and two slimline x12 of 74P connectors. The PCB placement and connector pin definition is as follows:

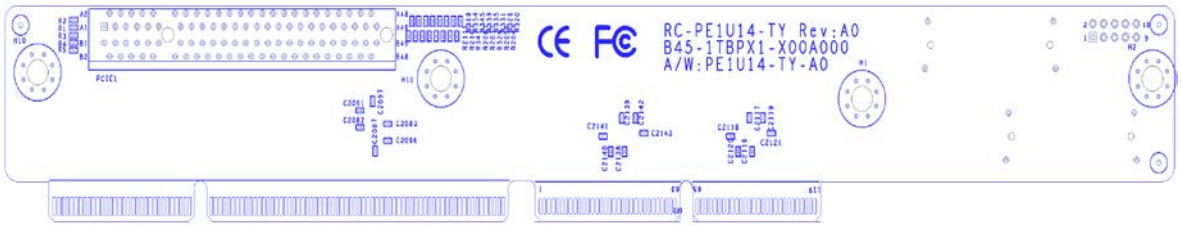


Figure 25 - Top Side PCBA Placement of RC-PE1U14-TY

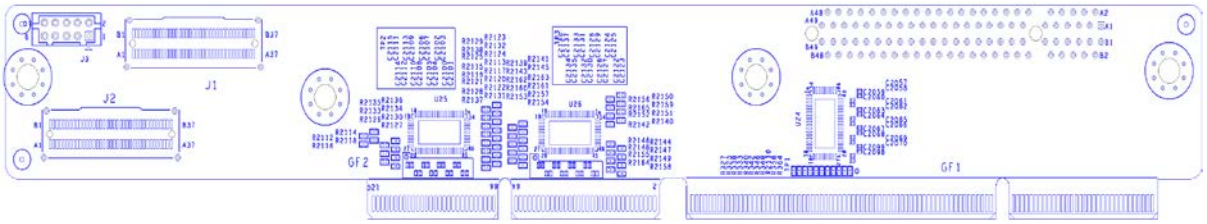


Figure 26 - Bottom Side PCBA Placement of RC-PE1U14-TY

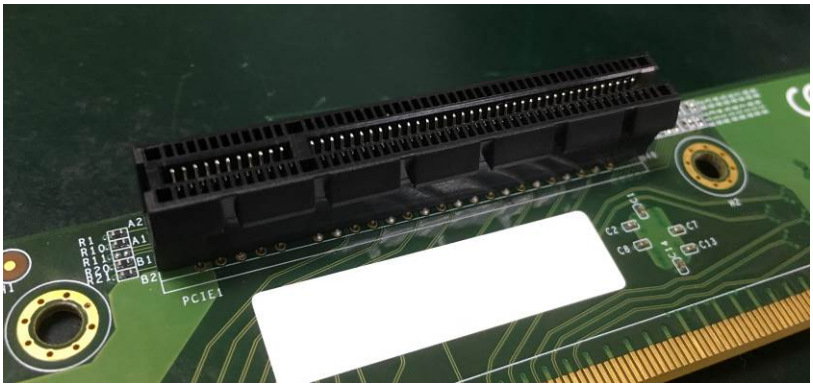


Figure 27 - PCIE x8 slot PCIE1

Table 16 - PCIE x8 slot Connector Pin-Out (PCIE1)

Pin	Description	Pin	Description
A1	GND	B1	+12V
A2	+12V	B2	+12V
A3	+12V	B3	+12V
A4	GND	B4	GND
A5	GND	B5	PCIE_SMCLK
A6	+3.3V	B6	PCIE_SMDAT
A7	NC	B7	GND
A8	+3.3V	B8	+3.3V
A9	+3.3V	B9	GND
A10	+3.3V	B10	+3.3V_DUAL
A11	RST_PCIE_SLOT	B11	PCH_WAKE_N
A12	GND	B12	NC
A13	CLK_100M_PCIE1_P	B13	GND
A14	CLK_100M_PCIE1_N	B14	CPU0_EXP2_TX_DP_0
A15	GND	B15	CPU0_EXP2_TX_DN_0
A16	CPU0_EXP2_RX_DP_0	B16	GND
A17	CPU0_EXP2_RX_DN_0	B17	GND
A18	GND	B18	GND
A19	NC	B19	CPU0_EXP2_TX_DP_1
A20	GND	B20	CPU0_EXP2_TX_DN_1
A21	CPU0_EXP2_RX_DP_1	B21	GND
A22	CPU0_EXP2_RX_DN_1	B22	GND
A23	GND	B23	CPU0_EXP2_TX_DP_2
A24	GND	B24	CPU0_EXP2_TX_DN_2
A25	CPU0_EXP2_RX_DP_2	B25	GND
A26	CPU0_EXP2_RX_DN_2	B26	GND
A27	GND	B27	CPU0_EXP2_TX_DP_3
A28	GND	B28	CPU0_EXP2_TX_DN_3
A29	CPU0_EXP2_RX_DP_3	B29	GND
A30	CPU0_EXP2_RX_DN_3	B30	NC
A31	GND	B31	GND
A32	NC	B32	GND
A33	NC	B33	CPU0_EXP2_TX_DP_4
A34	GND	B34	CPU0_EXP2_TX_DN_4
A35	CPU0_EXP2_RX_DP_4	B35	GND
A36	CPU0_EXP2_RX_DN_4	B36	GND
A37	GND	B37	CPU0_EXP2_TX_DP_5
A38	GND	B38	CPU0_EXP2_TX_DN_5
A39	CPU0_EXP2_RX_DP_5	B39	GND
A40	CPU0_EXP2_RX_DN_5	B40	GND
A41	GND	B41	CPU0_EXP2_TX_DP_6
A42	GND	B42	CPU0_EXP2_TX_DN_6
A43	CPU0_EXP2_RX_DP_6	B43	GND
A44	CPU0_EXP2_RX_DN_6	B44	GND
A45	GND	B45	CPU0_EXP2_TX_DP_7
A46	GND	B46	CPU0_EXP2_TX_DN_7

A47	CPU0_EXP2_RX_DP_7	B47	GND
A48	CPU0_EXP2_RX_DN_7	B48	GND
A49	GND	B49	GND

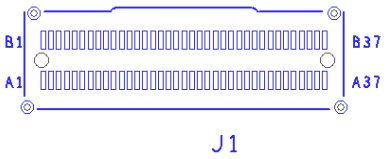


Figure 28 - Slimline Connector J1

Table 17 - Slimline 74P Connector Pin-Out (J1)

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU0_EXP1_RX_DN_R_12	B2	CPU0_EXP1_TX_DN_12
A3	CPU0_EXP1_RX_DP_R_12	B3	CPU0_EXP1_TX_DP_12
A4	GND	B4	GND
A5	CPU0_EXP1_RX_DN_R_13	B5	CPU0_EXP1_TX_DN_13
A6	CPU0_EXP1_RX_DP_R_13	B6	CPU0_EXP1_TX_DP_13
A7	GND	B7	GND
A8	CPU0_EXP1_RX_DN_R_14	B8	CPU0_EXP1_TX_DN_14
A9	CPU0_EXP1_RX_DP_R_14	B9	CPU0_EXP1_TX_DP_14
A10	GND	B10	GND
A11	CPU0_EXP1_RX_DN_R_15	B11	CPU0_EXP1_TX_DN_15
A12	CPU0_EXP1_RX_DP_R_15	B12	CPU0_EXP1_TX_DP_15
A13	GND	B13	GND
A14	CPU0_EXP2_RX_DN_R_15	B14	CPU0_EXP2_TX_DN_15
A15	CPU0_EXP2_RX_DP_R_15	B15	CPU0_EXP2_TX_DP_15
A16	GND	B16	GND
A17	CPU0_EXP2_RX_DN_R_14	B17	CPU0_EXP2_TX_DN_14
A18	CPU0_EXP2_RX_DP_R_14	B18	CPU0_EXP2_TX_DP_14
A19	GND	B19	GND
A20	CPU0_EXP2_RX_DN_R_13	B20	CPU0_EXP2_TX_DN_13
A21	CPU0_EXP2_RX_DP_R_13	B21	CPU0_EXP2_TX_DP_13
A22	GND	B22	GND
A23	CPU0_EXP2_RX_DN_R_12	B23	CPU0_EXP2_TX_DN_12
A24	CPU0_EXP2_RX_DP_R_12	B24	CPU0_EXP2_TX_DP_12
A25	GND	B25	GND
A26	CPU0_EXP2_RX_DN_R_11	B26	CPU0_EXP2_TX_DN_11
A27	CPU0_EXP2_RX_DP_R_11	B27	CPU0_EXP2_TX_DP_11
A28	GND	B28	GND
A29	CPU0_EXP2_RX_DN_R_10	B29	CPU0_EXP2_TX_DN_10
A30	CPU0_EXP2_RX_DP_R_10	B30	CPU0_EXP2_TX_DP_10
A31	GND	B31	GND
A32	CPU0_EXP2_RX_DN_R_9	B32	CPU0_EXP2_TX_DN_9
A33	CPU0_EXP2_RX_DP_R_9	B33	CPU0_EXP2_TX_DP_9
A34	GND	B34	GND
A35	CPU0_EXP2_RX_DN_R_8	B35	CPU0_EXP2_TX_DN_8

A36	CPU0_EXP2_RX_DP_R_8	B36	CPU0_EXP2_TX_DP_8
A37	GND	B37	GND

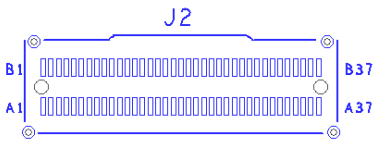


Figure 29 - Slimline Connector J2

Table 18 - Slimline 74P Connector Pin-Out (J2)

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU0_EXP1_RX_DP_R_11	B2	CPU0_EXP1_TX_DP_11
A3	CPU0_EXP1_RX_DN_R_11	B3	CPU0_EXP1_TX_DN_11
A4	GND	B4	GND
A5	CPU0_EXP1_RX_DP_R_10	B5	CPU0_EXP1_TX_DP_10
A6	CPU0_EXP1_RX_DN_R_10	B6	CPU0_EXP1_TX_DN_10
A7	GND	B7	GND
A8	CPU0_EXP1_RX_DP_R_9	B8	CPU0_EXP1_TX_DP_9
A9	CPU0_EXP1_RX_DN_R_9	B9	CPU0_EXP1_TX_DN_9
A10	GND	B10	GND
A11	CPU0_EXP1_RX_DP_R_8	B11	CPU0_EXP1_TX_DP_8
A12	CPU0_EXP1_RX_DN_R_8	B12	CPU0_EXP1_TX_DN_8
A13	GND	B13	GND
A14	CPU0_EXP1_RX_DP_R_7	B14	CPU0_EXP1_TX_DP_7
A15	CPU0_EXP1_RX_DN_R_7	B15	CPU0_EXP1_TX_DN_7
A16	GND	B16	GND
A17	CPU0_EXP1_RX_DP_R_6	B17	CPU0_EXP1_TX_DP_6
A18	CPU0_EXP1_RX_DN_R_6	B18	CPU0_EXP1_TX_DN_6
A19	GND	B19	GND
A20	CPU0_EXP1_RX_DP_R_5	B20	CPU0_EXP1_TX_DP_5
A21	CPU0_EXP1_RX_DN_R_5	B21	CPU0_EXP1_TX_DN_5
A22	GND	B22	GND
A23	CPU0_EXP1_RX_DP_R_4	B23	CPU0_EXP1_TX_DP_4
A24	CPU0_EXP1_RX_DN_R_4	B24	CPU0_EXP1_TX_DN_4
A25	GND	B25	GND
A26	CPU0_EXP1_RX_DP_R_3	B26	CPU0_EXP1_TX_DP_3
A27	CPU0_EXP1_RX_DN_R_3	B27	CPU0_EXP1_TX_DN_3
A28	GND	B28	GND
A29	CPU0_EXP1_RX_DP_R_2	B29	CPU0_EXP1_TX_DP_2
A30	CPU0_EXP1_RX_DN_R_2	B30	CPU0_EXP1_TX_DN_2
A31	GND	B31	GND
A32	CPU0_EXP1_RX_DP_R_1	B32	CPU0_EXP1_TX_DP_1
A33	CPU0_EXP1_RX_DN_R_1	B33	CPU0_EXP1_TX_DN_1
A34	GND	B34	GND
A35	CPU0_EXP1_RX_DP_R_0	B35	CPU0_EXP1_TX_DP_0
A36	CPU0_EXP1_RX_DN_R_0	B36	CPU0_EXP1_TX_DN_0

A37	GND	B37	GND

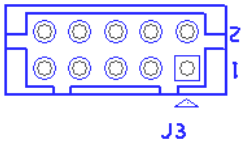


Figure 30 - 2x5P Box-Header J3

Table 19 - 2x5P Box-Header Pin-Out (J3)

Pin	Description	Pin	Description
1	BMC_GPIOG5	2	+3.3V
3	GND	4	PCH_WAKE_N
5	CLK_100M_PCIE2_P	6	RST_PCIE_SLOT
7	CLK_100M_PCIE2_N	8	CPU0_HP_I2C_CLK
9	PCH_GPP_C8	10	CPU0_HP_I2C_DAT

7.2 DIMM Sockets

The motherboard supports up to 24 DDR4 2400/2600/2933 RDIMMs/LRDIMMs. The location of the DIMM socket is shown below.

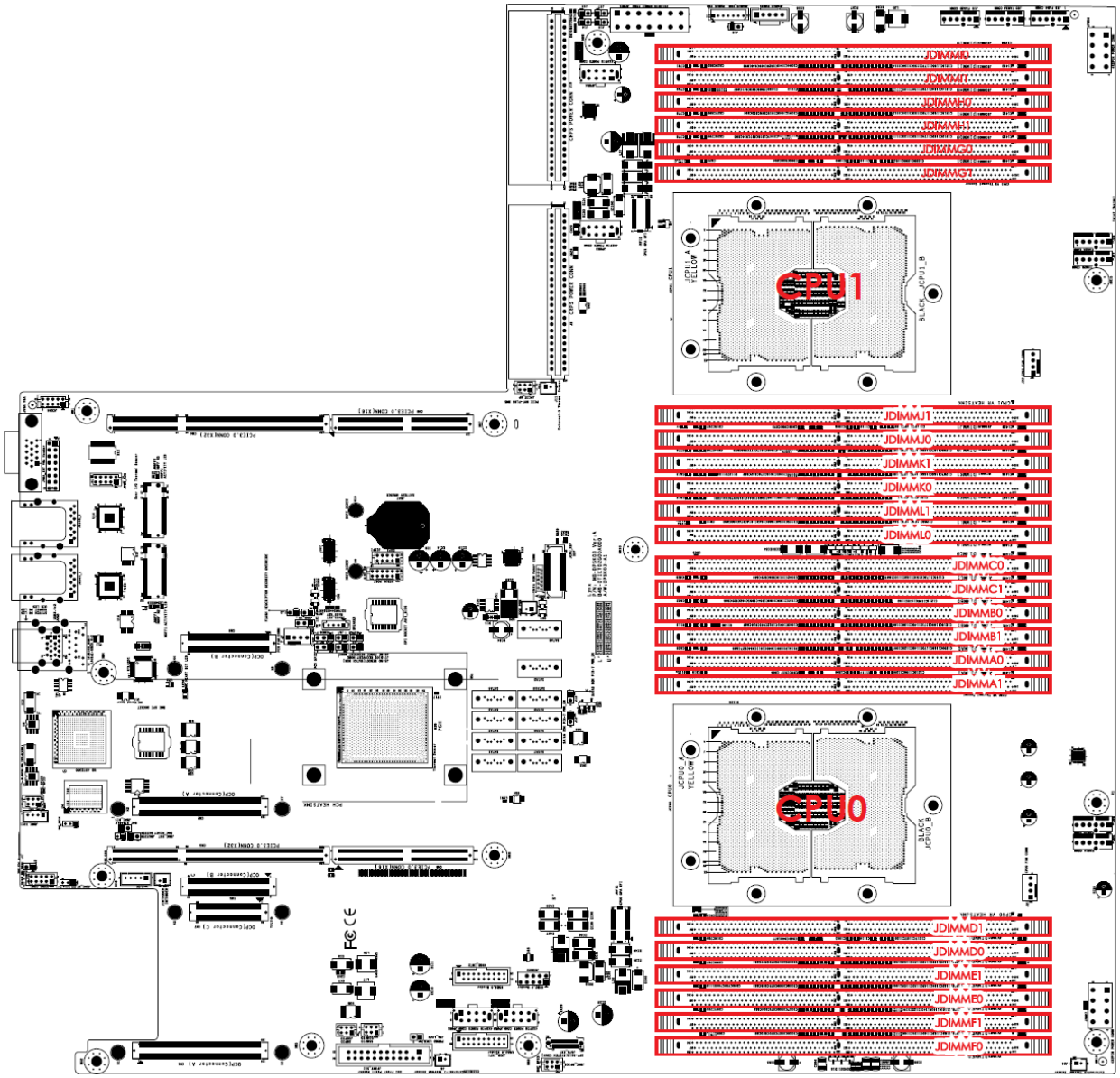


Figure 31 - DIMM Socket Location

7.3 Mezzanine Card

The motherboard has OCP Mezz 2.0 connectors A and B to provide up to a x16 PCIe Gen3 connection to the Mezzanine card. The motherboard also has an OCP Mezz 2.0 Connector C to provide up to x4 KR. Connector C can be used independently on the Mezzanine card side. For the OCP connector type and label, please refer to the following table.

Table 20 - OCP Connector type

OCP Connector type	Location
A	CN1, CN2
B	CN5, CN6
C	CN7

Table 21 - PCIe Slot Configuration

SuperSlot#	PCIE width	From which CPU	Usage
Slot1	X16	CPU0	100Gbe PCIe adding card
Slot1	X8	CPU0	50Gbe OCP Mezz Card
Slot1	X24	CPU0	Riser card and cable connect to backplane
Slot2	X16	CPU1	100Gbe OCP Mezz Module
Slot2	X8	CPU1	50Gbe PCIe adding card
Slot2	X24	CPU1	Riser card and cable connect to backplane

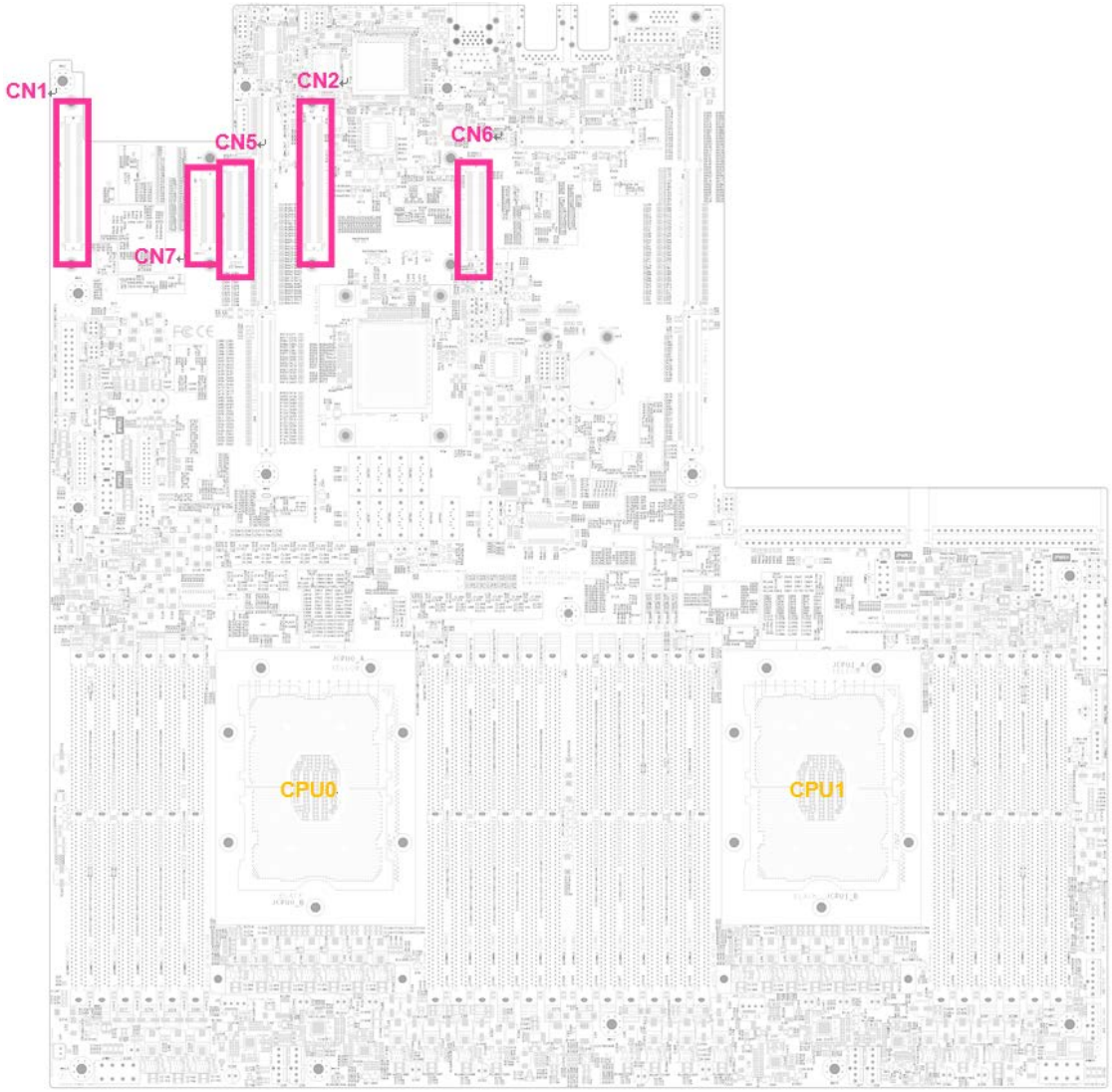


Figure 32 - OCP Connector Location

Table 22 - OCP MEZZ Connector A definition (CN1)

GND	1	2	+12V
+5V_AUX	3	4	+12V
+5V_AUX	5	6	+12V
+5V_AUX	7	8	GND
GND	9	10	GND
GND	11	12	+3.3V_DUAL
+3.3V_DUAL	13	14	GND
GND	15	16	GND
GND	17	18	+3.3V
+3.3V	19	20	+3.3V
+3.3V	21	22	+3.3V
+3.3V	23	24	+3.3V

+3.3V	25	26	GND
N.C.	27	28	SMB_OCP1_ALERT_N
N.C.	29	30	SMB_3V3SB_CLK_OCP_0
N.C.	31	32	SMB_3V3SB_DAT_OCP_0
OCP_RST_N_0	33	34	PCH_WAKE_N
I2C5SCL_OCP_0	35	36	N.C.
I2C5SDA_OCP_0	37	38	GND
GND	39	40	N.C.
GND	41	42	N.C.
N.C.	43	44	GND
N.C.	45	46	GND
GND	47	48	CLK_100M_OCP1_P
GND	49	50	CLK_100M_OCP1_N
CLK_100M_OCP2_P	51	52	GND
CLK_100M_OCP2_N	53	54	GND
GND	55	56	CPU0_OCP_TX_DP_0
GND	57	58	CPU0_OCP_TX_DN_0
CPU0_OCP_RX_DP_0	59	60	GND
CPU0_OCP_RX_DN_0	61	62	GND
GND	63	64	CPU0_OCP_TX_DP_1
GND	65	66	CPU0_OCP_TX_DN_1
CPU0_OCP_RX_DP_1	67	68	GND
CPU0_OCP_RX_DN_1	69	70	GND
GND	71	72	CPU0_OCP_TX_DP_2
GND	73	74	CPU0_OCP_TX_DN_2
CPU0_OCP_RX_DP_2	75	76	GND
CPU0_OCP_RX_DN_2	77	78	GND
GND	79	80	CPU0_OCP_TX_DP_3
GND	81	82	CPU0_OCP_TX_DN_3
CPU0_OCP_RX_DP_3	83	84	GND
CPU0_OCP_RX_DN_3	85	86	GND
GND	87	88	CPU0_OCP_TX_DP_4
GND	89	90	CPU0_OCP_TX_DN_4
CPU0_OCP_RX_DP_4	91	92	GND
CPU0_OCP_RX_DN_4	93	94	GND
GND	95	96	CPU0_OCP_TX_DP_5
GND	97	98	CPU0_OCP_TX_DN_5
CPU0_OCP_RX_DP_5	99	100	GND
CPU0_OCP_RX_DN_5	101	102	GND
GND	103	104	CPU0_OCP_TX_DP_6
GND	105	106	CPU0_OCP_TX_DN_6
CPU0_OCP_RX_DP_6	107	108	GND
CPU0_OCP_RX_DN_6	109	110	GND
GND	111	112	CPU0_OCP_TX_DP_7
GND	113	114	CPU0_OCP_TX_DN_7
CPU0_OCP_RX_DP_7	115	116	GND
CPU0_OCP_RX_DN_7	117	118	GND
GND	119	120	+3.3V_DUAL

Table 23 - OCP MEZZ Connector B definition (CN5)

GND	1	2	+12V
GND	3	4	+12V
CPU0_OCP_RX_DP_8	5	6	N.C.
CPU0_OCP_RX_DN_8	7	8	GND
GND	9	10	CPU0_OCP_TX_DP_8
GND	11	12	CPU0_OCP_TX_DN_8
CPU0_OCP_RX_DP_9	13	14	GND
CPU0_OCP_RX_DN_9	15	16	GND
GND	17	18	CPU0_OCP_TX_DP_9
GND	19	20	CPU0_OCP_TX_DN_9
CPU0_OCP_RX_DP_10	21	22	GND
CPU0_OCP_RX_DN_10	23	24	GND
GND	25	26	CPU0_OCP_TX_DP_10
GND	27	28	CPU0_OCP_TX_DN_10
CPU0_OCP_RX_DP_11	29	30	GND
CPU0_OCP_RX_DN_11	31	32	GND
GND	33	34	CPU0_OCP_TX_DP_11
GND	35	36	CPU0_OCP_TX_DN_11
CPU0_OCP_RX_DP_12	37	38	GND
CPU0_OCP_RX_DN_12	39	40	GND
GND	41	42	CPU0_OCP_TX_DP_12
GND	43	44	CPU0_OCP_TX_DN_12
CPU0_OCP_RX_DP_13	45	46	GND
CPU0_OCP_RX_DN_13	47	48	GND
GND	49	50	CPU0_OCP_TX_DP_13
GND	51	52	CPU0_OCP_TX_DN_13
CPU0_OCP_RX_DP_14	53	54	GND
CPU0_OCP_RX_DN_14	55	56	GND
GND	57	58	CPU0_OCP_TX_DP_14
GND	59	60	CPU0_OCP_TX_DN_14
CPU0_OCP_RX_DP_15	61	62	GND
CPU0_OCP_RX_DN_15	63	64	GND
GND	65	66	CPU0_OCP_TX_DP_15
GND	67	68	CPU0_OCP_TX_DN_15
CLK_100M_OCP3_P	69	70	GND
CLK_100M_OCP3_N	71	72	GND
GND	73	74	CLK_100M_OCP4_P
OCP_RST_N_0	75	76	CLK_100M_OCP4_N
OCP_RST_N_0	77	78	GND
OCP_RST_N_0	79	80	+3.3V_DUAL

Table 24 - OCP MEZZ Connector C definition (CN7)

LAN_SMBCLK	1	33	+12V
LAN_SMBDAT	2	34	+12V
TP_EXT_MDIO_I2C_SEL	3	35	+12V

GND	4	36	N.C.
KR_L2_TX_DP	5	37	LAN_MOD_ABS0
KR_L2_TX_DN	6	38	LAN_MOD_ABS1
GND	7	39	GND
LAN_LED_P1_0	8	40	KR_L0_TX_DP
LAN_LED_P1_1	9	41	KR_L0_TX_DN
GND	10	42	GND
KR_L3_TX_DP	11	43	LAN_LED_P0_0
KR_L3_TX_DN	12	44	LAN_LED_P0_1
GND	13	45	GND
LAN_LED_P2_0	14	46	KR_L1_TX_DP
LAN_LED_P2_1	15	47	KR_L1_TX_DN
GND	16	48	GND
KR_L2_RX_C_DP	17	49	TP_SHARED_KR_MDC_0
KR_L2_RX_C_DN	18	50	TP_SHARED_KR_MDIO_0
GND	19	51	GND
LAN_SCL0	20	52	KR_L0_RX_C_DP
LAN_SDA0	21	53	KR_L0_RX_C_DN
GND	22	54	GND
KR_L3_RX_C_DP	23	55	LAN_LED_P3_0
KR_L3_RX_C_DN	24	56	LAN_LED_P3_1
GND	25	57	GND
LAN_SCL1	26	58	KR_L1_RX_C_DP
LAN_SDA1	27	59	KR_L1_RX_C_DN
GND	28	60	GND
LAN_SCL3	29	61	LAN_SCL2
LAN_SDA3	30	62	LAN_SDA2
LAN_MOD_ABS2	31	63	GND
LAN_MOD_ABS3	32	64	+3.3V_DUAL

Table 25 - OCP MEZZ Connector A definition (CN2)

GND	1	2	+12V
+5V_AUX	3	4	+12V
+5V_AUX	5	6	+12V
+5V_AUX	7	8	GND
GND	9	10	GND
GND	11	12	+3.3V_DUAL
+3.3V_DUAL	13	14	GND
GND	15	16	GND
GND	17	18	+3.3V
+3.3V	19	20	+3.3V
+3.3V	21	22	+3.3V
+3.3V	23	24	+3.3V
+3.3V	25	26	GND
N.C.	27	28	SMB_OCP2_ALERT_N
N.C.	29	30	SMB_3V3SB_CLK_OCP_1
N.C.	31	32	SMB_3V3SB_DAT_OCP_1
OCP_RST_N_1	33	34	PCH_WAKE_N

I2C5SCL_OCP_1	35	36	N.C.
I2C5SDA_OCP_1	37	38	GND
GND	39	40	N.C.
GND	41	42	N.C.
N.C.	43	44	GND
N.C.	45	46	GND
GND	47	48	CLK_100M_OCP5_P
GND	49	50	CLK_100M_OCP5_N
CLK_100M_OCP6_P	51	52	GND
CLK_100M_OCP6_N	53	54	GND
GND	55	56	CPU1_OCP_TX_DP_0
GND	57	58	CPU1_OCP_TX_DN_0
CPU1_OCP_RX_DP_0	59	60	GND
CPU1_OCP_RX_DN_0	61	62	GND
GND	63	64	CPU1_OCP_TX_DP_1
GND	65	66	CPU1_OCP_TX_DN_1
CPU1_OCP_RX_DP_1	67	68	GND
CPU1_OCP_RX_DN_1	69	70	GND
GND	71	72	CPU1_OCP_TX_DP_2
GND	73	74	CPU1_OCP_TX_DN_2
CPU1_OCP_RX_DP_2	75	76	GND
CPU1_OCP_RX_DN_2	77	78	GND
GND	79	80	CPU1_OCP_TX_DP_3
GND	81	82	CPU1_OCP_TX_DN_3
CPU1_OCP_RX_DP_3	83	84	GND
CPU1_OCP_RX_DN_3	85	86	GND
GND	87	88	CPU1_OCP_TX_DP_4
GND	89	90	CPU1_OCP_TX_DN_4
CPU1_OCP_RX_DP_4	91	92	GND
CPU1_OCP_RX_DN_4	93	94	GND
GND	95	96	CPU1_OCP_TX_DP_5
GND	97	98	CPU1_OCP_TX_DN_5
CPU1_OCP_RX_DP_5	99	100	GND
CPU1_OCP_RX_DN_5	101	102	GND
GND	103	104	CPU1_OCP_TX_DP_6
GND	105	106	CPU1_OCP_TX_DN_6
CPU1_OCP_RX_DP_6	107	108	GND
CPU1_OCP_RX_DN_6	109	110	GND
GND	111	112	CPU1_OCP_TX_DP_7
GND	113	114	CPU1_OCP_TX_DN_7
CPU1_OCP_RX_DP_7	115	116	GND
CPU1_OCP_RX_DN_7	117	118	GND
GND	119	120	+3.3V_DUAL

Table 26 - OCP MEZZ Connector B definition (CN6)

GND	1	2	+12V
GND	3	4	+12V

CPU1_OCP_RX_DP_8	5	6	N.C.
CPU1_OCP_RX_DN_8	7	8	GND
GND	9	10	CPU1_OCP_TX_DP_8
GND	11	12	CPU1_OCP_TX_DN_8
CPU1_OCP_RX_DP_9	13	14	GND
CPU1_OCP_RX_DN_9	15	16	GND
GND	17	18	CPU1_OCP_TX_DP_9
GND	19	20	CPU1_OCP_TX_DN_9
CPU1_OCP_RX_DP_10	21	22	GND
CPU1_OCP_RX_DN_10	23	24	GND
GND	25	26	CPU1_OCP_TX_DP_10
GND	27	28	CPU1_OCP_TX_DN_10
CPU1_OCP_RX_DP_11	29	30	GND
CPU1_OCP_RX_DN_11	31	32	GND
GND	33	34	CPU1_OCP_TX_DP_11
GND	35	36	CPU1_OCP_TX_DN_11
CPU1_OCP_RX_DP_12	37	38	GND
CPU1_OCP_RX_DN_12	39	40	GND
GND	41	42	CPU1_OCP_TX_DP_12
GND	43	44	CPU1_OCP_TX_DN_12
CPU1_OCP_RX_DP_13	45	46	GND
CPU1_OCP_RX_DN_13	47	48	GND
GND	49	50	CPU1_OCP_TX_DP_13
GND	51	52	CPU1_OCP_TX_DN_13
CPU1_OCP_RX_DP_14	53	54	GND
CPU1_OCP_RX_DN_14	55	56	GND
GND	57	58	CPU1_OCP_TX_DP_14
GND	59	60	CPU1_OCP_TX_DN_14
CPU1_OCP_RX_DP_15	61	62	GND
CPU1_OCP_RX_DN_15	63	64	GND
GND	65	66	CPU1_OCP_TX_DP_15
GND	67	68	CPU1_OCP_TX_DN_15
CLK_100M_OCP7_P	69	70	GND
CLK_100M_OCP7_N	71	72	GND
GND	73	74	CLK_100M_OCP8_P
OCP_RST_N_0	75	76	CLK_100M_OCP8_N
OCP_RST_N_0	77	78	GND
OCP_RST_N_0	79	80	+3.3V_DUAL

7.4 Network

- CPU0 → 1 x 100GbE (PCIE add on card) + 1 x 50GbE single port (OCP)
- CPU1 → 1 x 100GbE (OCP) + 1 x 50GbE dual port (PCIE add on card)
- 1 × GbE RJ45 dedicated to BMC management

7.5 USB

The motherboard has one external Type-A connector and provides two USB 3.0 ports in the rear, as well as two internal box-header supports for USB 2.0/3.0. The connection to either a UHCI or

the EHCI is dynamic and dependent on the USB device capability. Therefore, all ports support SS/HS/FS/LS USB devices.

Table 27 - Front I/O USB Header definition (JUSB_INT1、JUSB_INT2)

KEY (no pin)	20	1	+5V_USB23
+5V_USB23	19	2	PCH_FP_USB3_RX_N2
PCH_FP_USB3_RX_N3	18	3	PCH_FP_USB3_RX_P2
PCH_FP_USB3_RX_P3	17	4	GND
GND	16	5	PCH_FP_USB3_TX_N2
PCH_FP_USB3_TX_N3	15	6	PCH_FP_USB3_TX_P2
PCH_FP_USB3_TX_P3	14	7	GND
GND	13	8	PCH_FP_USB2_N2
PCH_FP_USB2_N3	12	9	PCH_FP_USB2_P2
PCH_FP_USB2_P3	11	10	PCH_USB_OC#23

Table 28 - Front I/O USB 2.0 Header definition (JUSB20)

+5V_USB67	2	1	+5V_USB67
PCH_FP_USB2_N8	4	3	PCH_FP_USB2_N9
PCH_FP_USB2_P8	6	5	PCH_FP_USB2_P9
GND	8	7	GND
N.C.	10	9	GND

7.6 SATA

The motherboard has 10 standard SATA connectors, whose locations are shown below. Each port can support data transfer rates up to 6.0 Gb/s (600 MB/s).

All SATA ports can support Raid 0, 1, 5, 10.

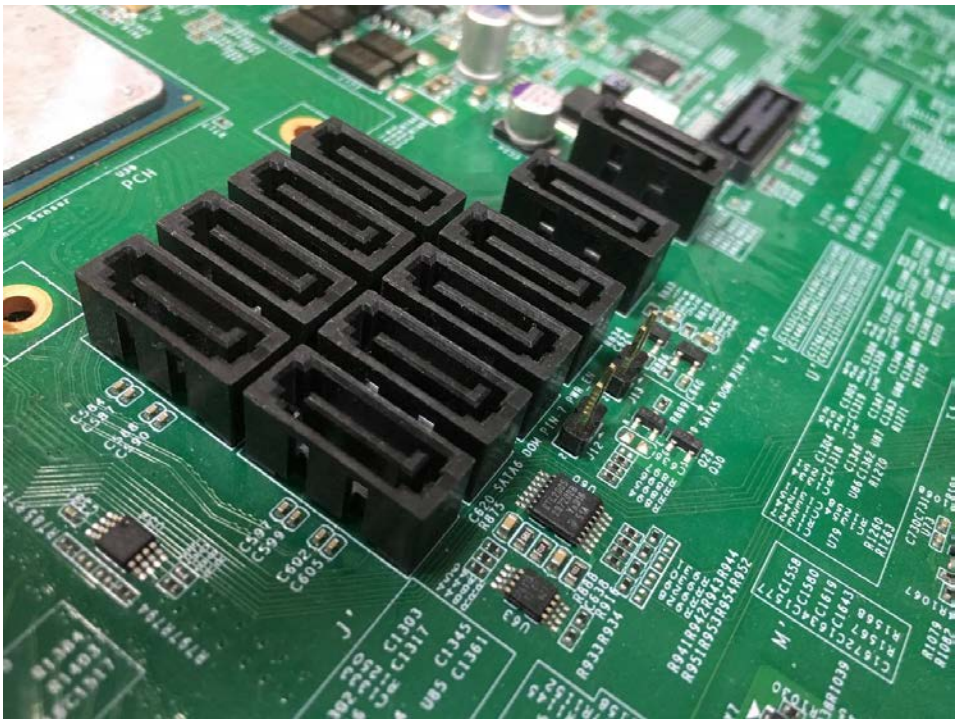


Figure 33 - Standard SATA Connector on motherboard

7.7 M.2

The motherboard has 2x M.2 connectors to provide an optional connection to the PCIe x4 or SATA port from the PCH. Both onboard M.2 connectors only support the 2280 card form factor.

The sideband should be connected when sideband signals such as WAKE# and SATA_ACTIVITY apply. The PERST# signal shall be activated before the power behind the M.2 connector is removed, per the PCI CEM specification.

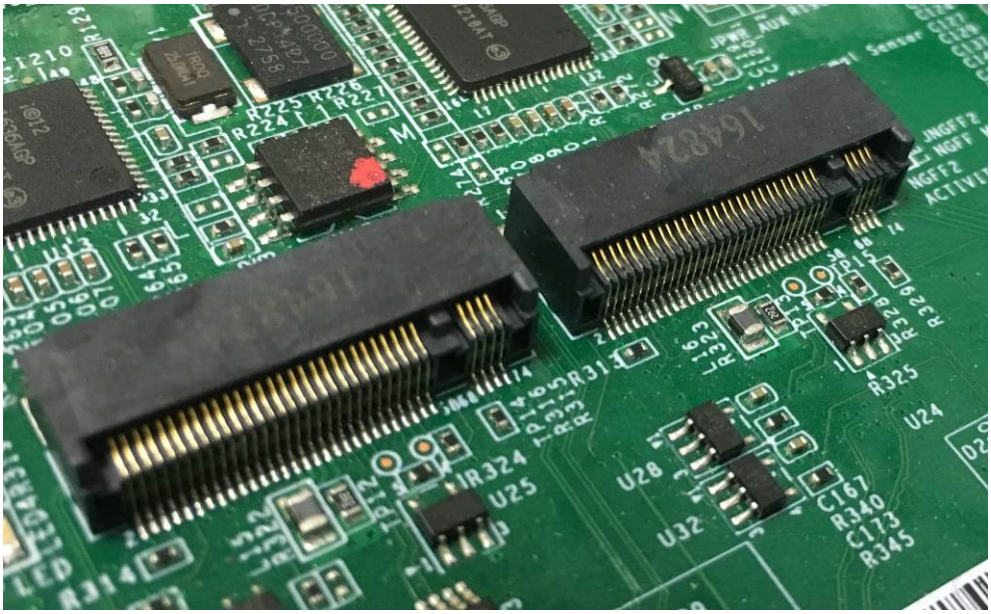


Figure 34 - M.2 Connector

Table 29 - NGFF Connector definition (JNGFF1, JNGFF2)

GND	1	2	+3.3V
GND	3	4	+3.3V
N.C.	5	6	+3.3V
N.C.	7	8	N.C.
GND	9	10	NGFF_ACT_LED
N.C.	11	12	+3.3V
N.C.	13	14	+3.3V
GND	15	16	+3.3V
N.C.	17	18	+3.3V
N.C.	19	20	N.C.
GND	21	22	N.C.
N.C.	23	24	N.C.
N.C.	25	26	N.C.
GND	27	28	NGFF_PWDIS
PCH_M2_EXP_RX_DN	29	30	+12V
PCH_M2_EXP_RX_DP	31	32	+12V
GND	33	34	+12V
PCH_M2_EXP_TX_DN	35	36	+12V
PCH_M2_EXP_TX_DP	37	38	NGFF_DEVSLP
GND	39	40	NGFF_SCL
NGFF_SATA_B+_TX_DN	41	42	NGFF_SDA
NGFF_SATA_B-_TX_DP	43	44	NGFF_ALERT#

GND	45	46	N.C.
NGFF_SATA_A-_TX_DN	47	48	N.C.
NGFF_SATA_A+_TX_DP	49	50	RST_PCIE_M2
GND	51	52	NGFF_CLKREQ#
CLK_100M_NGFF_DN	53	54	PCH_WAKE_N
CLK_100M_NGFF_DP	55	56	N.C.
GND	57	58	N.C.
KEY M			
GND	67	68	PCH_SUSCLK_N
NGFF_PEDET	69	70	+3.3V
GND	71	72	+3.3V
GND	73	74	+3.3V
GND	75		

7.8 Debug Header

The motherboard has two debug headers: JBMC_DP and JLPC_DP.

The JBMC_DP is a 1x3 pin header placed in front of the motherboard, and is used to provide BMC functionality test information.

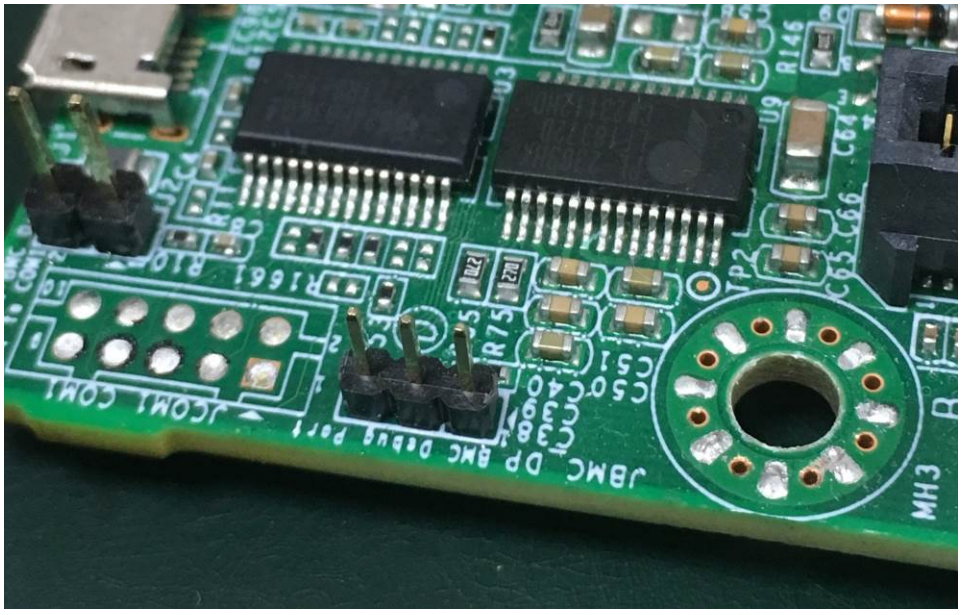


Figure 35 - JBMC Debug Header

Table 30 - BMC Debug port header definition (JBMC_DP)

1	BMC_UART_TXD5
2	BMC_UART_RXD5
3	GND

The JLPC_DP is a 2x6 pin box-header, which uses a debug card to get the BIOS status code. Through this header, the debug card should provide one UART serial port connector and two 7-segment LED displays. The debug card can be connected to this header directly or through a cable.

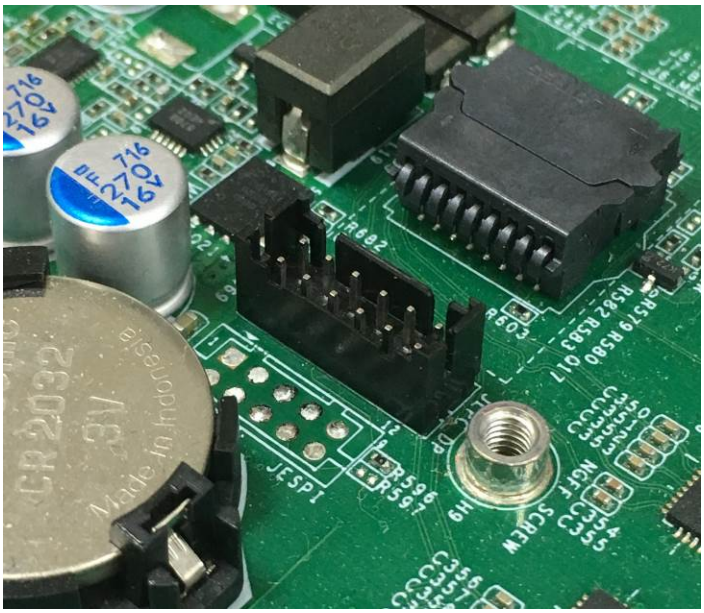


Figure 36 - JLPC Debug Header

Table 31 - Debug port header definition (JLPC_DP)

CLK_24M_DP80	2	1	GND
PCH_LFRAME_N	4	3	PCH_LDRQ0_N
RST_PLTRST_N	6	5	AST_SERIRQ
PCH_LPC_LAD3	8	7	PCH_LPC_LAD2
+3.3V	10	9	PCH_LPC_LAD1
PCH_LPC_LAD0	12	11	GND

7.9 Switches and LEDs

The system shall include a power switch, power LED, HDD activity LED, Network LED and Error LED.

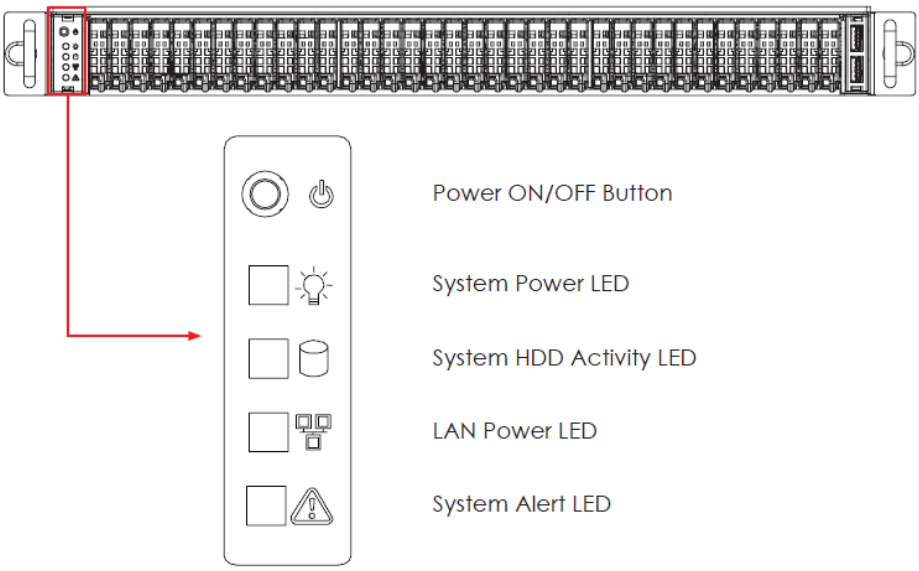


Figure 37 - System Front Panel

The table below indicates the color and function of each LED. The system's silkscreen shall indicate the functionality of each of these LEDs. Looking from the front panel towards the LEDs, from up to down, the sequence is Green, Green, Green, Red.

Table 32 - Front Panel LED Definition

LED Color	Function	Silk Screen Label
Green	Power LED. This LED shall illuminate if the motherboard is in the "power on" state.	PWR
Green	Hard drive activity. This LED shall illuminate when there is activity on the motherboard's 36 x NF1 NVMe SSD drive and 2 x M.2 NGFF connector interface.	HDD
Green	Network active LED. This LED shall illuminate when network port is either connected or receiving a signal.	Network
Red	Error LED. This LED shall illuminate when the BMC has a predefined error identified by the LED.	Fault

7.10 Fan connector

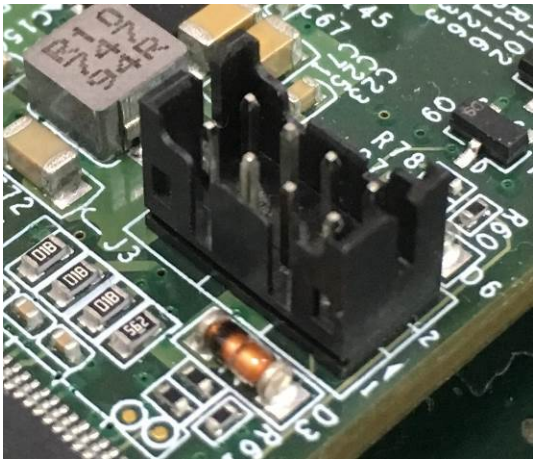


Figure 38 - Fan Connector

The system has seven fan connectors on the backplane (J1~J7). Each fan has eight pins, which is compatible with a standard 8-Wire FAN connector to support a dual rotor fan that has separate tachometer (TACH) and Pulse Width Modulation (PWM) signals. The connector pin-out is shown in section 6.1.1.

The power switch is black, on the top side in the front panel.

If the power switch is depressed for under four seconds, a power management event will be issued, indicating that the power switch has been triggered. If the power switch is depressed for longer than four seconds, the motherboard will initiate a hard “power off.”

Power switch functionality can be triggered by the BMC.

7.11 TPM Connector and Module

This system can support TPM 2.0. NUVOTON NPCT650 is used on board the module.

7.12 Sideband Connector

The system uses a SFF-8612 42P connector to deliver USB, PCIE 100MHz Clock and an I2C signal to the backplane.

Figure 39 - SFF-8612 Connector on motherboard

7.13 VGA header

The motherboard includes a DSUB 15-Pin Blue Female connector. The VGA connector is located in the EATX I/O aperture area. This connector must be compatible with the VESA DDC/CI Version 1 standard and the plastic color should be blue to signify such compliance. The VGA connector must have both mounting posts installed even if the VGA connector is included in a combo connector, such as serial over VGA.

Figure 40 - VGA Header

Table 33 - VGA Header Definition (JVGA)

DACROA	1	9	DVO_5V
DACGOA	2	10	GND
DACBOA	3	11	NC
NC	4	12	DDC_DATAO
GND	5	13	AHSYNCO
GND	6	14	AVSYNCO
GND	7	15	DDC_CLKO
GND	8		

8. Rear Side Power, I/O and Midplane

8.1 Overview of Footprint and Population Options

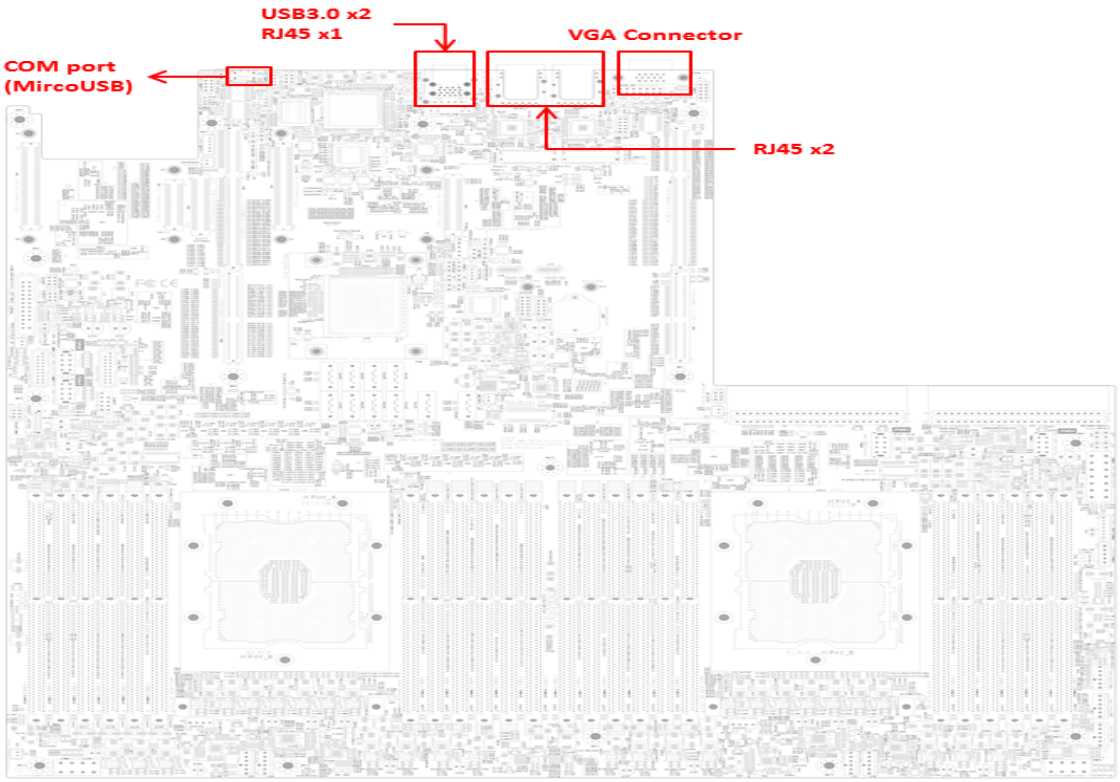


Figure 41 - Rear Side I/O Location

8.2 Rear Side Connectors

Refer to the table below for the function and definition of rear side connectors.

Table 34 - Rear I/O

Connector Function	Physical Description	Comments
COM Port	Micro-USB type B	J1
USB3.0 x2/Ethernet x1	USB3.0 double-stack+ RJ45	JRJ45_USB：Type A USB3.0 double-stack+10/100MBPS PHYCEIVER JUSB：Type A USB3.0 double-stack
Ethernet x1	RJ45	JRJ45_1：integrated LEDs
Ethernet x1	RJ45	JRJ45_2：integrated LEDs
VGA	DSUB 15 Pin Blue Female	JVGA

8.3 Midplane

In this section, the definition and location of the various connectors on the backplane will be described.

8.3.1 Placement & Connectors Location

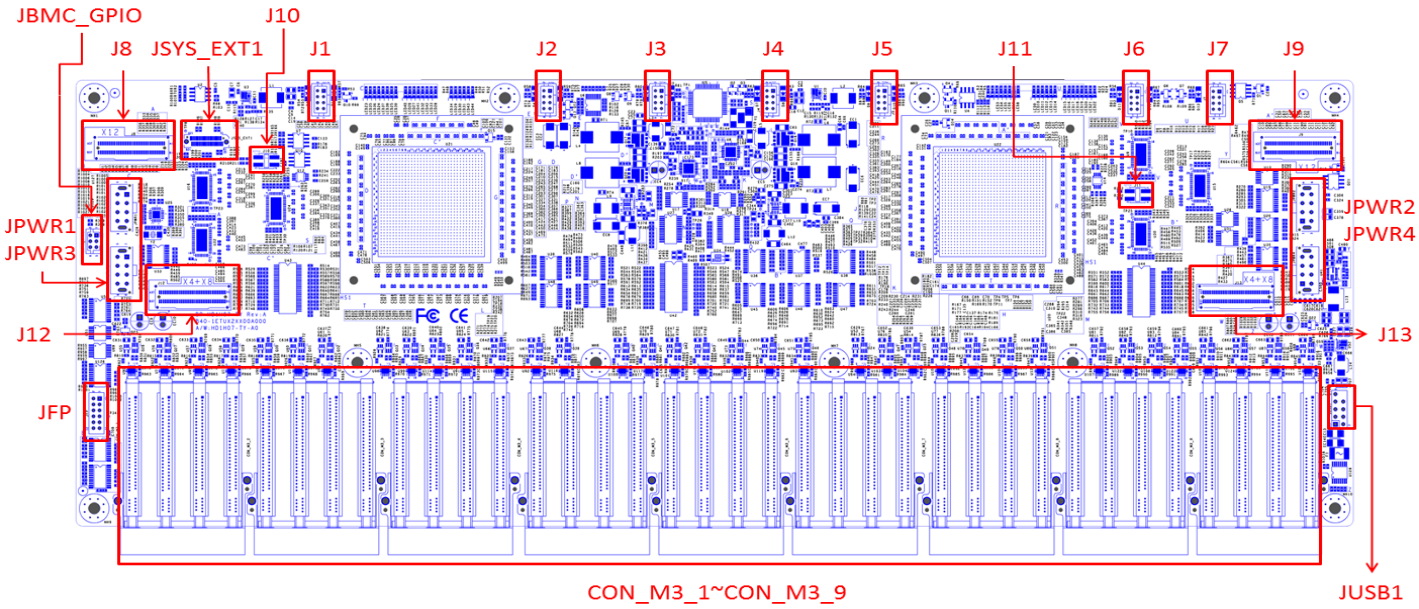


Figure 42 - Backplane Connector Location

8.3.2 Connector Definition Overview

Table 35 - Connector Definition

Connector Function	Physical Description	Comments
Fan CONN (J1~J7)	Pin Header 2x4p	Fan power & PWM signal
PCIE x12 (J8,J9)	Slimline x12 74p	PCIe x12 from motherboard
PEX_CLK&DAT (J10,J11)	Pin Header 2x2p	PEX9797 I2C pin header
PCIE x4 + x8 (J12,J13)	Slimline x4 + x8 74p	PCIe x12 from motherboard
PWR CONN (JPWR1~JPWR4)	Box Header 2x4p	+12V power supply from motherboard
OCulink x4 (JSYS_EXT1)	OCulink 42p	PCIe 100MHz CLK & sideband signal
GPIO CONN(JBMC_GPIO)	Box Header 2x3p	GPIO for BMC
Front Panel CONN(JFP)	Box Header 2x6p	Sideband signal for front panel
USB CONN(JUSB1)	Pin Header 2x5p	USB
PCIE x4 (CON_M.3_1~ CON_M.3_9)	NGSFF Connecter	PCIE x4 Slot X4

8.3.3 Connector Pin-Out

J1~J7:

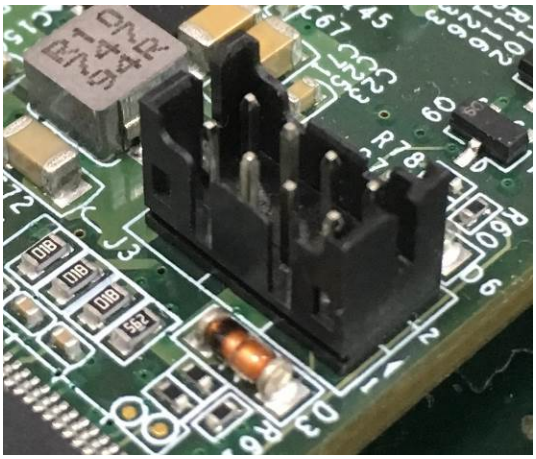


Figure 43 - J3

Table 36 - J1 Connector Pin-Out

Pin	Description	Pin	Description
1	HW_FAN_TACH_2	5	PWM_1
2	HW_FAN_TACH_1	6	PWM_1
3	+12V	7	GND
4	+12V	8	GND

J8:

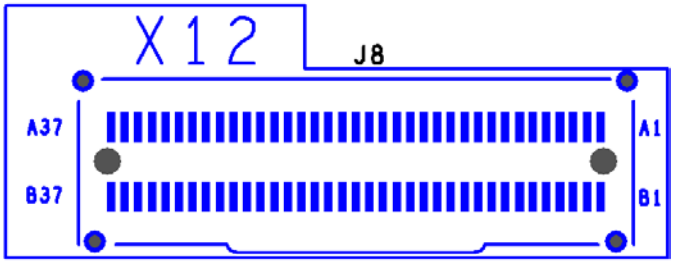


Figure 44 - J8

Table 37 - J8 Connector Pin-Out

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU0_EXP1_RX_DN_0	B2	CPU0_EXP1_TX_DN_R_0
A3	CPU0_EXP1_RX_DP_0	B3	CPU0_EXP1_TX_DP_R_0
A4	GND	B4	GND
A5	CPU0_EXP1_RX_DN_1	B5	CPU0_EXP1_TX_DN_R_1
A6	CPU0_EXP1_RX_DP_1	B6	CPU0_EXP1_TX_DP_R_1
A7	GND	B7	GND
A8	CPU0_EXP1_RX_DN_2	B8	CPU0_EXP1_TX_DN_R_2
A9	CPU0_EXP1_RX_DP_2	B9	CPU0_EXP1_TX_DP_R_2
A10	GND	B10	GND

A11	CPU0_EXP1_RX_DN_3	B11	CPU0_EXP1_TX_DN_R_3
A12	CPU0_EXP1_RX_DP_3	B12	CPU0_EXP1_TX_DP_R_3
A13	GND	B13	GND
A14	CPU0_EXP1_RX_DN_4	B14	CPU0_EXP1_TX_DN_R_4
A15	CPU0_EXP1_RX_DP_4	B15	CPU0_EXP1_TX_DP_R_4
A16	GND	B16	GND
A17	CPU0_EXP1_RX_DN_5	B17	CPU0_EXP1_TX_DN_R_5
A18	CPU0_EXP1_RX_DP_5	B18	CPU0_EXP1_TX_DP_R_5
A19	GND	B19	GND
A20	CPU0_EXP1_RX_DN_6	B20	CPU0_EXP1_TX_DN_R_6
A21	CPU0_EXP1_RX_DP_6	B21	CPU0_EXP1_TX_DP_R_6
A22	GND	B22	GND
A23	CPU0_EXP1_RX_DN_7	B23	CPU0_EXP1_TX_DN_R_7
A24	CPU0_EXP1_RX_DP_7	B24	CPU0_EXP1_TX_DP_R_7
A25	GND	B25	GND
A26	CPU0_EXP1_RX_DN_8	B26	CPU0_EXP1_TX_DN_R_8
A27	CPU0_EXP1_RX_DP_8	B27	CPU0_EXP1_TX_DP_R_8
A28	GND	B28	GND
A29	CPU0_EXP1_RX_DN_9	B29	CPU0_EXP1_TX_DN_R_9
A30	CPU0_EXP1_RX_DP_9	B30	CPU0_EXP1_TX_DP_R_9
A31	GND	B31	GND
A32	CPU0_EXP1_RX_DN_10	B32	CPU0_EXP1_TX_DN_R_10
A33	CPU0_EXP1_RX_DP_10	B33	CPU0_EXP1_TX_DP_R_10
A34	GND	B34	GND
A35	CPU0_EXP1_RX_DN_11	B35	CPU0_EXP1_TX_DN_R_11
A36	CPU0_EXP1_RX_DP_11	B36	CPU0_EXP1_TX_DP_R_11
A37	GND	B37	GND

J9:

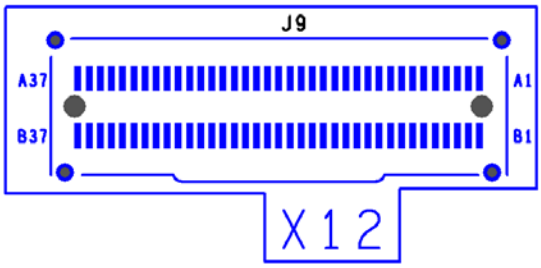


Figure 45 - J9

Table 38 - J9 Connector Pin-Out

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU1_EXP1_TX_DP_R_11	B2	CPU1_EXP1_RX_DP_11
A3	CPU1_EXP1_TX_DN_R_11	B3	CPU1_EXP1_RX_DN_11
A4	GND	B4	GND
A5	CPU1_EXP1_TX_DP_R_10	B5	CPU1_EXP1_RX_DP_10
A6	CPU1_EXP1_TX_DN_R_10	B6	CPU1_EXP1_RX_DN_10

A7	GND	B7	GND
A8	CPU1_EXP1_TX_DP_R_9	B8	CPU1_EXP1_RX_DP_9
A9	CPU1_EXP1_TX_DN_R_9	B9	CPU1_EXP1_RX_DN_9
A10	GND	B10	GND
A11	CPU0_EXP1_RX_DN_3	B11	CPU1_EXP1_RX_DP_8
A12	CPU0_EXP1_RX_DP_3	B12	CPU1_EXP1_RX_DN_8
A13	GND	B13	GND
A14	CPU0_EXP1_RX_DN_4	B14	CPU1_EXP1_RX_DP_7
A15	CPU0_EXP1_RX_DP_4	B15	CPU1_EXP1_RX_DN_7
A16	GND	B16	GND
A17	CPU0_EXP1_RX_DN_5	B17	CPU1_EXP1_RX_DP_6
A18	CPU0_EXP1_RX_DP_5	B18	CPU1_EXP1_RX_DN_6
A19	GND	B19	GND
A20	CPU0_EXP1_RX_DN_6	B20	CPU1_EXP1_RX_DP_5
A21	CPU0_EXP1_RX_DP_6	B21	CPU1_EXP1_RX_DN_5
A22	GND	B22	GND
A23	CPU0_EXP1_RX_DN_7	B23	CPU1_EXP1_RX_DP_4
A24	CPU0_EXP1_RX_DP_7	B24	CPU1_EXP1_RX_DN_4
A25	GND	B25	GND
A26	CPU0_EXP1_RX_DN_8	B26	CPU1_EXP1_RX_DP_3
A27	CPU0_EXP1_RX_DP_8	B27	CPU1_EXP1_RX_DN_3
A28	GND	B28	GND
A29	CPU0_EXP1_RX_DN_9	B29	CPU1_EXP1_RX_DP_2
A30	CPU0_EXP1_RX_DP_9	B30	CPU1_EXP1_RX_DN_2
A31	GND	B31	GND
A32	CPU0_EXP1_RX_DN_10	B32	CPU1_EXP1_RX_DP_1
A33	CPU0_EXP1_RX_DP_10	B33	CPU1_EXP1_RX_DN_1
A34	GND	B34	GND
A35	CPU0_EXP1_RX_DN_11	B35	CPU1_EXP1_RX_DP_0
A36	CPU0_EXP1_RX_DP_11	B36	CPU1_EXP1_RX_DN_0
A37	GND	B37	GND

J10:

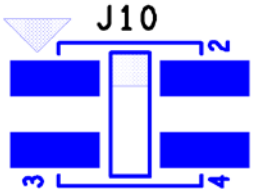


Figure 46 - J10

Table 39 - J10 Connector Pin-Out

Pin	Description	Pin	Description
1	PEX_SCL0_R_X0	2	GND
3	PEX_SDA0_R_X0	4	NC

J11:

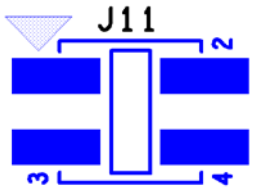


Figure 47 - J11

Table 40 - J11 Connector Pin-Out

Pin	Description	Pin	Description
1	PEX_SCL0_R_X1	2	GND
3	PEX_SDA0_R_X1	4	NC

J12:

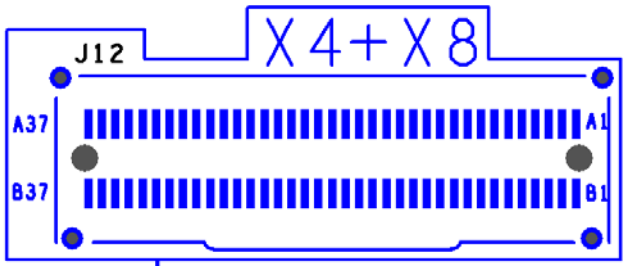


Figure 48 - J12

Table 41 - J12 Connector Pin-Out

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU0_EXP2_RX_DP_8	B2	CPU0_EXP2_TX_DP_R_8
A3	CPU0_EXP2_RX_DN_8	B3	CPU0_EXP2_TX_DN_R_8
A4	GND	B4	GND
A5	CPU0_EXP2_RX_DP_9	B5	CPU0_EXP2_TX_DP_R_9
A6	CPU0_EXP2_RX_DN_9	B6	CPU0_EXP2_TX_DN_R_9
A7	GND	B7	GND
A8	CPU0_EXP2_RX_DP_10	B8	CPU0_EXP2_TX_DP_R_10
A9	CPU0_EXP2_RX_DN_10	B9	CPU0_EXP2_TX_DN_R_10
A10	GND	B10	GND
A11	CPU0_EXP2_RX_DP_11	B11	CPU0_EXP2_TX_DP_R_11
A12	CPU0_EXP2_RX_DN_11	B12	CPU0_EXP2_TX_DN_R_11
A13	GND	B13	GND
A14	CPU0_EXP2_RX_DP_12	B14	CPU0_EXP2_TX_DP_R_12
A15	CPU0_EXP2_RX_DN_12	B15	CPU0_EXP2_TX_DN_R_12
A16	GND	B16	GND
A17	CPU0_EXP2_RX_DP_13	B17	CPU0_EXP2_TX_DP_R_13

A18	CPU0_EXP2_RX_DN_13	B18	CPU0_EXP2_TX_DN_R_13
A19	GND	B19	GND
A20	CPU0_EXP2_RX_DP_14	B20	CPU0_EXP2_TX_DP_R_14
A21	CPU0_EXP2_RX_DN_14	B21	CPU0_EXP2_TX_DN_R_14
A22	GND	B22	GND
A23	CPU0_EXP2_RX_DP_15	B23	CPU0_EXP2_TX_DP_R_15
A24	CPU0_EXP2_RX_DN_15	B24	CPU0_EXP2_TX_DN_R_15
A25	GND	B25	GND
A26	CPU0_EXP1_RX_DP_15	B26	CPU0_EXP1_TX_DP_R_15
A27	CPU0_EXP1_RX_DN_15	B27	CPU0_EXP1_TX_DN_R_15
A28	GND	B28	GND
A29	CPU0_EXP1_RX_DP_14	B29	CPU0_EXP1_TX_DP_R_14
A30	CPU0_EXP1_RX_DN_14	B30	CPU0_EXP1_TX_DN_R_14
A31	GND	B31	GND
A32	CPU0_EXP1_RX_DP_13	B32	CPU0_EXP1_TX_DP_R_13
A33	CPU0_EXP1_RX_DN_13	B33	CPU0_EXP1_TX_DN_R_13
A34	GND	B34	GND
A35	CPU0_EXP1_RX_DP_12	B35	CPU0_EXP1_TX_DP_R_12
A36	CPU0_EXP1_RX_DN_12	B36	CPU0_EXP1_TX_DN_R_12
A37	GND	B37	GND

J13:

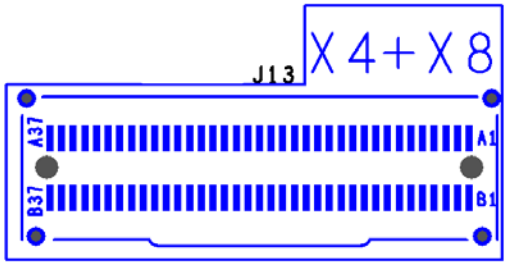


Figure 49 - J13

Table 42 - J13 Connector Pin-Out

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	CPU1_EXP1_TX_DN_R_12	B2	CPU1_EXP1_RX_DN_12
A3	CPU1_EXP1_TX_DP_R_12	B3	CPU1_EXP1_RX_DP_12
A4	GND	B4	GND
A5	CPU1_EXP1_TX_DN_R_13	B5	CPU1_EXP1_RX_DN_13
A6	CPU1_EXP1_TX_DP_R_13	B6	CPU1_EXP1_RX_DP_13
A7	GND	B7	GND
A8	CPU1_EXP1_TX_DN_R_14	B8	CPU1_EXP1_RX_DN_14
A9	CPU1_EXP1_TX_DP_R_14	B9	CPU1_EXP1_RX_DP_14
A10	GND	B10	GND
A11	CPU1_EXP1_TX_DN_R_15	B11	CPU1_EXP1_RX_DN_15
A12	CPU1_EXP1_TX_DP_R_15	B12	CPU1_EXP1_RX_DP_15
A13	GND	B13	GND

A14	CPU1_EXP2_TX_DN_R_15	B14	CPU1_EXP2_RX_DN_15
A15	CPU1_EXP2_TX_DP_R_15	B15	CPU1_EXP2_RX_DP_15
A16	GND	B16	GND
A17	CPU1_EXP2_TX_DN_R_14	B17	CPU1_EXP2_RX_DN_14
A18	CPU1_EXP2_TX_DP_R_14	B18	CPU1_EXP2_RX_DP_14
A19	GND	B19	GND
A20	CPU1_EXP2_TX_DN_R_13	B20	CPU1_EXP2_RX_DN_13
A21	CPU1_EXP2_TX_DP_R_13	B21	CPU1_EXP2_RX_DP_13
A22	GND	B22	GND
A23	CPU1_EXP2_TX_DN_R_12	B23	CPU1_EXP2_RX_DN_12
A24	CPU1_EXP2_TX_DP_R_12	B24	CPU1_EXP2_RX_DP_12
A25	GND	B25	GND
A26	CPU1_EXP2_TX_DN_R_11	B26	CPU1_EXP2_RX_DN_11
A27	CPU1_EXP2_TX_DP_R_11	B27	CPU1_EXP2_RX_DP_11
A28	GND	B28	GND
A29	CPU1_EXP2_TX_DN_R_10	B29	CPU1_EXP2_RX_DN_10
A30	CPU1_EXP2_TX_DP_R_10	B30	CPU1_EXP2_RX_DP_10
A31	GND	B31	GND
A32	CPU1_EXP2_TX_DN_R_9	B32	CPU1_EXP2_RX_DN_9
A33	CPU1_EXP2_TX_DP_R_9	B33	CPU1_EXP2_RX_DP_9
A34	GND	B34	GND
A35	CPU1_EXP2_TX_DN_R_8	B35	CPU1_EXP2_RX_DN_8
A36	CPU1_EXP2_TX_DP_R_8	B36	CPU1_EXP2_RX_DP_8
A37	GND	B37	GND

JPWR 1~4:

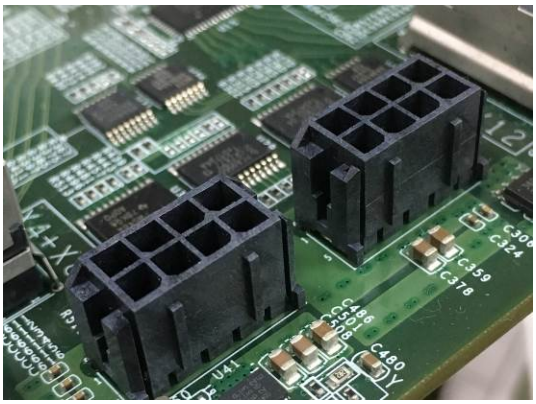


Figure 50 - JPWR2 & JPWR4

Table 43 - JPWR1~4 Connector Pin-Out

Pin	Description	Pin	Description
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V

JBMC_GPIO:

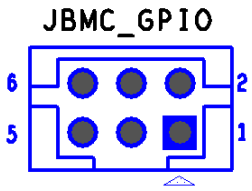


Figure 51 - JBMC_GPIO

Table 44 - JBMC_GPIO Connector Pin-Out

Pin	Description	Pin	Description
1	GND	2	HP_INT#_8
3	HP_INT#_14	4	GPIOP2
5	+3.3V_DUAL	6	GPION7

JSYS_EXT1:

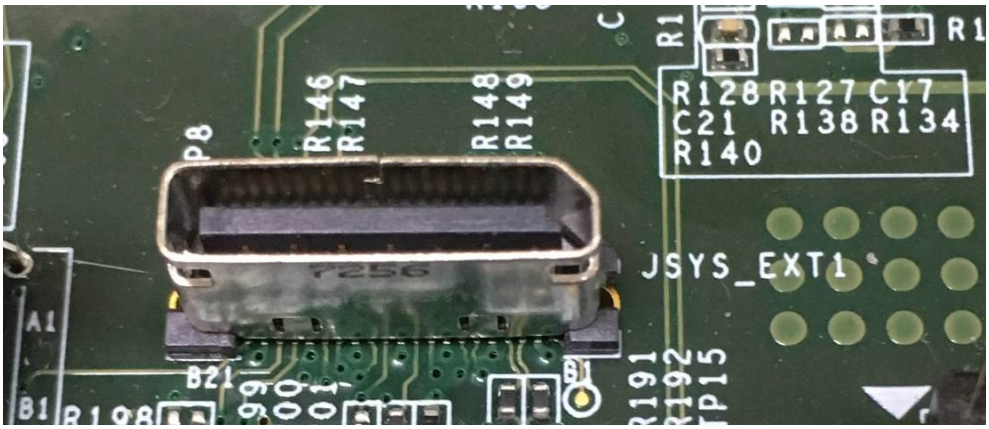


Figure 52 - JSYS_EXT1

Table 45 - JSYS_EXT1 Connector Pin-Out

Pin	Description	Pin	Description
A1	PCH_USB_OC#89	B1	TP15
A2	GND	B2	GND
A3	CLK_100M_PCIE6_R_P	B3	CLK_100M_PCIE5_R_P
A4	CLK_100M_PCIE6_R_N	B4	CLK_100M_PCIE5_R_N
A5	GND	B5	GND
A6	PCH_USB2_P11	B6	PCH_USB2_P10
A7	PCH_USB2_N11	B7	PCH_USB2_N10
A8	GND	B8	GND
A9	PCIE_SMCLK	B9	SW_PWR_BTN#
A10	PCIE_SMDAT	B10	PCH_WAKE#
A11	GND	B11	GND
A12	RST_PCIE_SLOT	B12	Global_SSD_ACT#

A13	SYS_FAULT#	B13	Global_LAN_ACT#
A14	GND	B14	GND
A15	I2C13SDA_R	B15	I2C9SDA
A16	I2C13SCL_R	B16	I2C9SCL
A17	GND	B17	GND
A18	I2C8SDA	B18	I2C10SDA
A19	I2C8SCL	B19	I2C10SCL
A20	GND	B20	GND
A21	TP8	B21	UIDLED_OUT#

JUSB1:

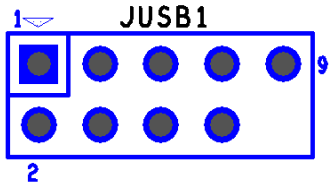


Figure 53 - JUSB1

Table 46 - JUSB1 Connector Pin-Out

Pin	Description	Pin	Description
1	+5V_USB89	2	+5V_USB89
3	PCH_USB2_N11	4	PCH_USB2_N10
5	PCH_USB2_P11	6	PCH_USB2_P10
7	GND	8	GND
9	GND		

JFP:

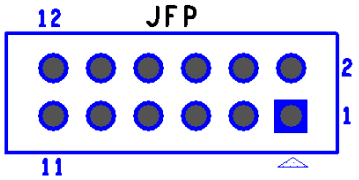


Figure 54 - JFP

Table 47 - JFP Connector Pin-Out

Pin	Description	Pin	Description
1	+3.3V_DUAL	2	+3V3
3	PWR_LED	4	Global_SSD_R_ACT#
5	SW_PWR_BTN#	6	Global_LAN_ACT#
7	SW_RST_BTN#	8	GPIOP3
9	SYS_FAULT#	10	GPIOI3
11	UIDLED_OUT#	12	GND

9. Mechanical

9.1 PCB Thickness

To ensure proper alignment of the motherboard and backplane interface within their mechanical enclosure, the motherboard should match the thickness of the PCB stack up to 81.4mil (2.06mm). The backplane's PCB thickness should be 94.24mil (2.4mm). The riser card's PCB thickness should be 62.6mil (≈1.6mm).

9.2 Heat Sinks and ILM

The motherboard shall support heat sinks that are mounted according to the Intel thermal mechanical specification and design guide. The vendor shall comply with all "keep out" zones defined by Intel in the referenced specification.

9.3 Silk Screen

The silk screen shall be white in color and include labels for the component numbers.

9.4 DIMM Connector Color

Colored DIMM connectors shall be used to indicate the first DIMM of each memory channel. This first DIMM in each channel is defined as the DIMM that is the furthest away from its associated CPU. The first DIMM connector is blue in the Mission Peak motherboard, and shall be populated first when the memory is only partially populated.

9.5 PCB Color

The PCB color is green to denote EVT、DVT and PVT, and is controlled by the PCB P/N.

10. Motherboard Power System

10.1 Input Voltage

The input voltage delivered by the power supply is 12 VDC nominal for light loading, with a range of 11V to 13V. The motherboard shall accept and operate normally with an input voltage tolerance range between 10.8V and 13V. The motherboard's VR Digital Controller shall provide an under-voltage protection level to 9.5V, as well as an over-voltage protection level to over 14V.

10.2 CPU VR Optimizations

CPU VR optimizations shall be implemented to minimize cost and increase the efficiency of the power conversion system. Vendors shall only use the minimum number of total phases to support the maximum CPU power. CPU VR should have an auto phase dropping feature, and run at the optimized phase count and maximum phase count. CPU VR should support all Power States to allow the VRM to operate at peak efficiency during light loading. The CPU VR should comply with the latest VR specification and validation method, and pass test with margin.

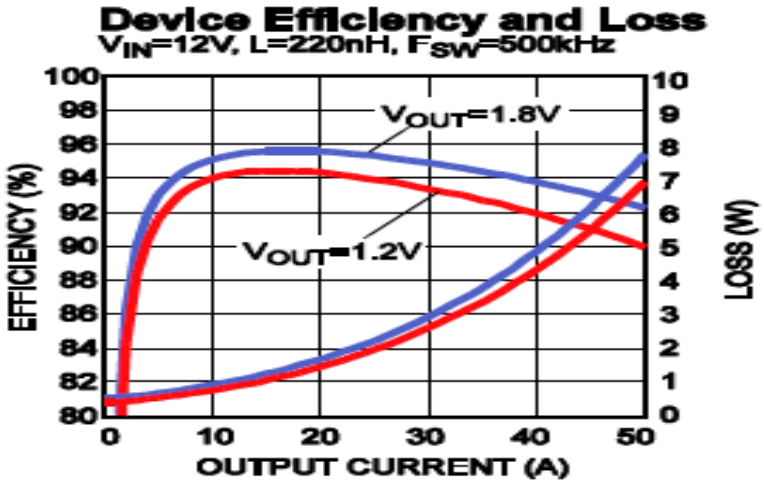


Figure 55 - CPU VR Optimizations

CPU VR Efficiency

For CPU efficiency measurement:

1. VID is set to 1.82V and 1.6V.

2. Vin is set to 12V.

3. Efficiency is measured from input inductor to socket.

4. Driver and controller loss should be included.

5. Output voltage is gathered from the Vsense of each socket.

6. No additional air flow shall be supplied to the VR area other than that from the VRTT tool FAN.

7. Test is done at room temperature(20°C~25°C).

8. Voltage measurement shall be done by tool and method with 0.05% accuracy or better.

9. Current measurement shall be done by tool and method with 0.25% accuracy or Better.

10.3 DIMM VR Optimizations

DIMM VR should support auto phase dropping for high efficiency across all loading. It also should comply with the latest VR specification, and the updated validation guideline from the memory controller vendor, and pass test with margin.

DIMM VR Efficiency

For DIMM VR efficiency measurement:

1. VID is set to 1.2V.

2. Vin is set to 12V.

3. Efficiency is measured from input inductor to socket.

4. Driver and controller loss should be included.

5. Output voltage is gathered from the Vsense of each socket.

6. No additional air flow shall be supplied to the VR area.

7. Test is done at room temperature (20°C~25°C).

8. Voltage measurement shall be done by tool and method with 0.05% accuracy or better.

9. Current measurement shall be done by tool and method with 0.25% accuracy or better.

10.4 VRM design guideline

For VRMs, the vendor should list the current budget for each power rail, based on “worst case loading” in all possible operation conditions. General requirements for VR component selection and VR design should meet 150% of this budget, and OCP should be set to 200% of the same budget. Vendors should conduct a design check, inform purchasers about the actual OCP setting chosen for VRM, and explain if it cannot meet this general requirement above.

For VRMs that require firmware, power code or configuration files, vendors should maintain version control to track all releases and changes between each version, and provide a method (using application software) to retrieve each version during system run time.

VR13 defines the PWM control chip features for VR13 CPU DC-DC converters used in Intel platforms. VR13 includes a Serial VID (SVID) interface. VR13 PWM includes the following:

- Dual-rail output configuration
- Support for a selectable VID table (10mV steps or 5mV) on each rail
- Input-power sensor and PWR_IN alert function
- Auto phase-shedding function
- PMBus Compliant (1MHz Bus Speed)

10.5 System VRM efficiency

Vendors shall supply high efficiency VRMs for all voltage regulators under 20W that are not defined in this specification. All other voltage regulation modules shall provide 86 ~ 92% efficiency over the 30% to 90% load range, If higher efficiencies are available at additional cost, vendors shall make those options known.

10.6 Power On

Motherboard should be set to restore last power state during AC on/off. This means when AC goes through an on/off cycle, the motherboard should power on automatically without requiring interaction with the power button. Only when the motherboard is powered off on purpose, should it keep power off through an AC on/off.

10.7 High power use case

A high power use case is defined as whenever system power is between 1200W and 1600W.Typically, this is caused by fully populating the DIMM, high TDP CPU or a combination of the above. The motherboard design and power delivery shall allow such use cases with a change in the Bill of Materials (BOM). The vendor shall perform simulation during design, and testing during validation, for a high power kit.

10.8 Power Budget

The power budget is evaluated based on the configuration of the system. The maximum power level of the system is evaluated in the table below.

Table 48 - Power Budget Configuration

Power Budget	Unit Power	Quantity	Total
CPU Xeon E5 (Skylake)	145	2	290
Chipset	15	1	15
BMC	3	1	3
FANs	10	5	50
Clock Logic	2	1	2
on board M.2 booting SSDs	8	2	16
NGSFF NVMe Drives	10	36	360
100Gbe Ethernet Module	20	2	40
50G Ethernet card	10	2	20
DDR4 DIMMs	12	24	288
PCIe switch	35	2	70
Misc	50	1	50
Total System Max Power (watts)			1204

10.9 Power Supply Requirement

Two redundant power supply units (PSUs) are supported in the NF1 POC system to supply 12V to the motherboard. The capacity of the PSUs is 1500Watts, in order to support the system, and the NF1 SSDs. The PSU contains internal fans and has an LED on back to indicate the power status, and support interfacing of the PMBus with the BMC. The PSU is rated higher than 80+ Platinum. The PSU provides 12V and 5V power rails to the motherboard.

As part of the system PSU requirement, 1+1 redundant design is necessary. Also, based on a system power budget with a different SKU, PSU watt selection should be AC 1200W or 1600W 1+1 redundant hi-efficiency power supply 80+.

PSU requirements are listed as below:

- 80+ Platinum class
- Hot-pluggable
- 1 +1 redundant and current sharing design
- Dimensions (LxWxH): 195x73.5x40mm or 7.67x2.89x1.57 inches

11. Environmental and Regulations

11.1 Environmental

The full system shall meet RoHS Directive 2011/65/EU environmental requirements.

The full system with board installed must meet the following environmental requirements:

• Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985

• Storage relative humidity: 10% to 90% (non-condensing)

• Storage temperature range: -40°C to +70°C (long-term storage)

• Transportation temperature range: -55°C to +85°C (short-term storage)

• Operating altitude (with no de-rating) to 1,000 meters (3,300 feet)

11.2 EMC

The full system shall meet the following EMC environmental requirements:

- FCC 47 CFR part 15 subpart B, Class A
- ICES-003: issue 6, Class A
- EN55032: 2012+AC:2013, Class A
- EN61000-3-2: 2014
- EN61000-3-3: 2013
- EN55024: 2010
- AS/NZS CISPR32: 2015

11.3 Safety

Safety measures shall comply with the following regulations:

IEC 60950-1: 2005(2nd Edition)+A1:2009+A2:2013

EN 60950-1: 2006+A11:2009+A1:2010+A12:2011+A2:2013

12. Environmental Requirements

12.1 Vibration & Shock

The system shall meet shock and vibration requirements according to IEC specifications: IEC 68-2-(*) Standard & Levels. The testing requirements are listed in Table 49. The motherboard shall fully comply with this specification, without any electrical discontinuities during the operating vibration and shock tests. No physical damage or limitation of functional capabilities (as defined in this specification) shall occur to the motherboard during the non-operational vibration and shock tests.

Table 49 - Vibration and Shock Requirements

	Operating	Non-Operating
Vibration	0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave / minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave / minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks for each of the three axes	12g, half-sine 11mS, 10 shocks for each of the three axes

12.2 Regulations

The system shall meet the following regulations:

- UL, CE, FCC, and CB
- BSMI, VCCI, and CCC (optional)

The sled should comply with RoHS and WEEE.

12.3 Labels and Markings

The system shall include the following labels on the chassis and motherboard. The labels shall be placed in a way that does not cause them to disrupt the functionality or the airflow path of the motherboard.

Table 50 - Label Configuration

Description	Type	Barcode Required?
MAC Address (On motherboard; one per network interface)	Adhesive label	Yes
Mother Board Date Code (WEEK / YEAR)	Adhesive label	Yes
CE Marking	Silk screen	No
FCC Marking	Silk screen	No
System P/N	Adhesive label	Yes
Purchaser P/N	Adhesive label	Yes
Country of Origin	Silk screen	No

13. Prescribed Materials

13.1 Disallowed Components

The following components shall not be used in the design of the motherboard:

Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS)

13.2 Capacitors & Inductors

The following limitations shall be applied to the use of capacitors:

- Only aluminum organic polymer capacitors shall all be used. They must be rated 105°C.
- All capacitors will each have a predicted life of at least 50,000 hours at a 45C inlet air temperature, under projected worst conditions.
- Tantalum capacitors using manganese dioxide cathode are not allowed.
- SMT Ceramic Capacitors with case size > 1206 are not preferred. The vendor shall discuss with Facebook before using MLCC > 1206 case by case. Size 1206 is still allowed when a capacitor is installed far from the edge of the PCB, and with an orientation that minimizes the risk of cracks.
- X7R Ceramics material shall be used for SMT capacitors by default. COG or NP0 type should be used in critical portions of the design. X6S can be used in the CPU Cage area. Vendor shall discuss with Facebook before using X5R, with full consideration of worst case temperature at the location.
- Only SMT inductors may be used. The use of through-hole inductors is disallowed.

13.3 Component De-rating

For inductors, capacitors and FETs, de-rating analysis should be based on at least a 20% de-rating.

14. Reliability and Quality

14.1 Specification Compliance

Vendors must ensure that the motherboard meets these specifications as a stand-alone unit and while functioning in a complete server system. The vendor is ultimately responsible for assuring that production motherboards conform to this specification with no deviations. The vendor shall exceed the quality standards demonstrated during the pilot build (PVT) while the motherboard is in mass production. The customer must be notified if any changes are made that may impact product quality.

14.2 Change Orders

Vendors must notify the customer any time a change is made to the motherboard. A "Specification Compliance Matrix" will be submitted to the customer for each revision of the motherboard, including prototype samples.

14.3 Failure Analysis

Vendors shall perform failure analysis on defective units, which are returned to the vendor. Feedback shall be provided to the customer with a Corrective Action plan within two weeks of the date that the units were received at the vendor's facility.

14.4 Warranty

The vendor shall warrant the motherboard against defects and workmanship for a period of two years from the date of initial deployment at the customer's facility. The warranty will be fully transferable to any end user.

14.5 MTBF Requirements

The motherboard shall have a minimum calculated MTBF of 300K hours for a 90% confidence level, at a 45°C ambient temperature. The motherboard shall demonstrate the MTBF requirement above by running at full load and with a 50% load, while performing an AC cycling test 50% of the time at 45C. Typical alternation period is one week for a stress test and one week for the AC cycling test. This MTBF demonstration shall finish prior to First Customer Shipment (pilot samples, mass production units). The motherboard shall have a minimum service life of five years (24 hours/day, Full Load at 45°C ambient temperature).

Vendors shall provide a calculated MTBF number based on the expected component life.

14.6 Control Change Authorization and Revision Control

After the motherboard is released to mass production, no design changes, AVL changes, manufacturing process adjustments or material changes are allowed without prior written authorization from the customer. The AVL (Approved Vendor List) is defined by the list of components specified in the BOM.

Any request for changes must be submitted to the customer with proper documentation showing details of the changes, and the reason for them. This includes changes affecting form, fit, function, safety or serviceability of the product. Major changes in the product (or in the manufacturing process) will require re-qualification and/or product recertification. A new set of First Article Samples may be required to complete the ECO process. Any modifications after

approval shall phase-in during production without causing any delay or shift in the current production schedule.

Vendors shall provide sufficient advance notice to the customer to prevent any of production. All changes beginning with the pilot run must go through a formal ECO process. The revision number (on the motherboard label) will be adjusted accordingly. Revision Control: copies of all ECOs affecting the product will be provided to the customer for approval.

14.7 PCB Tests

The PCB test report includes motherboard, riser card and backplane, as noted below.

Motherboard:

ALLIED CIRCUIT CO., LTD

QUALITY INSPECTION REPORT

Date: 2017/6/2

Customer(客戶)	華泰	Instrument type 機型規格	47G0121-122N	REV.	
Date Code(週期)	1722P	(P/ N)博智料號	366S837A68N	Q'TY(數量)	25 PCS

	Description	Requirement	Q'ty	Measurement					ACC/REJ
1	**Material Thickness**								
	a)Raw Material	FR-4 IT180I		FR-4 IT180I					
	b)Finished PCB (mil)	81±8	5	80.6	80.1	81.3	81.2	80.4	ACC
2	**Copper Thickness**								
	a)PTH Wall (mil.)	min 0.8,avg.1.0	1	1.55	NA	NA	NA	NA	ACC
	b)Surface (mil.)	1.60±0.2	1	1.77	1.77	NA	NA	NA	ACC
3	**Solder Thickness**								
	a)HAL (u")								
	b)Cladding								
4	**Immersion Gold Thickness (u")**								
	Nickel Thickness (u")								
5	**Plating Gold Thickness (u")**								
	Nickel Thickness (u")								
6	**ENTEK Thickness**	0.203~0.508 μm	5	0.31	0.33	0.33	0.31	0.32	ACC
7	**Immersion silver Thickness (u")**								
8	**Solder Mask Thickness**	0.7±0.2mil	1	0.62	0.64	NA	NA	NA	ACC
9	**Copper Pattern**								
	a)Line Width (mil.)	3.5±20%	5	3.0	3.1	3.0	2.9	3.0	ACC
	b)Line Spacing (mil.)	4.0±20%	5	4.6	4.6	4.5	4.4	4.6	ACC
	c)Annular Ring (mil.)	≧2	5	4.3	4.2	4.3	4.3	4.1	ACC
10	**Tape Test**	3M Tape							
	a)Solder Resist	No Peeling	5	OK	OK	OK	OK	OK	ACC
	b)Legend	No Peeling	5	OK	OK	OK	OK	OK	ACC
	c)GOLD								
11	**Warpage**	≦0.7%	5	OK	OK	OK	OK	OK	ACC
12	**Dimension**	Per Drawing							
13	**Solderability**	≧95%Wetting	1	OK					ACC
14	**Ionic**	<1.56ug.Nacl/Sq.cm	1	0.30					ACC
15	**V-CUT(mm)**								
16	**Electrical Testing**	50Ω/10MΩ/250V							ACC
17	**Visual Defect**	依AQL-MIL-STD 105E抽樣							
	a)Solder Resist			OK					ACC
	b)Legend			OK					ACC
	c)Vender Code			OK					ACC
	d)Solder			OK					ACC
	f)Gold								
	g)Board Edge			OK					ACC
18	G/F Bevel Depth								

FM800303-01 A/2 (4year)

Approved By： _____. **Inspector By：** Judy .

Figure 56 - Motherboard PCB Test Report

Riser Card, Right Side:

邑昇實業股份有限公司 出貨檢驗報告
EISO INSPECTION REPORT

客戶名稱: CUSTOMER:	思創科技股份有限公司	出貨數量: Q'TY:	108 PCS
客戶料號: CUSTOMER P/N:	47G0121N009L BRC-PE10014A_A02	週期: DATE CODE:	1815
供應商料號: VENDER P/N:	EG1001110R0A	日期: DATE:	2018/5/11

檢驗內容
INSPECTION DESCRIPTION

NO:	檢驗項目 INSPECTION ITEM	規格 SPEC	單位 UNIT	實際 ACTUAL	結果 RESULT	備註 REMARK
	材料 MATERIAL					
1	基材供應商 MATERIAL SUPPLIER	IT180		IT180	ACC	
2	基板材質 BASE OF MATERIAL	FR-4		FR-4	ACC	
3	耐熱等級 FLAMMABILITY CLASS	94V-0		94V-0	ACC	
4	銅箔 COPPER FOIL	1/1	mil	0	ACC	
5	層面結構 LAYER TACK	4	LAYERS	4	ACC	
6	公司商標 LOGO				ACC	
7	UL	ES6		ES6	ACC	
	防焊 SOLDER MASK					
1	型號 BRAND TYPE	PSR2000 LF07		PSR2000 LF07	ACC	
2	防焊顏色 S/M COLOR	綠-GREEN		綠-GREEN	ACC	
3	防焊厚度 S/M THICKNESS	0.4(min)	mil	0	ACC	
	外觀 APPEARANCE					
1	表面處理 SURFACE FINISHED	化金		化金	ACC	
2	GOLD SRFACE THICKNESS 金厚度 Au THICKNESS 鎳厚度 Ni THICKNESS	>3u" >120 u"	μ in	(x)3.341 (x)136.58	ACC	
3	線寬 NESTED LINE WIDTH	4.60 mil ±20%	mil	4.79	ACC	
4	線距 NESTED LINE SPACING	5.40 mil ±20%	mil	5.22	ACC	
5	板厚 BOARD THICKNESS	1.6±0.16	mm	1.62	ACC	
6	文字廠商 LEGEND SUPPLIER	永勝泰		永勝泰	ACC	
7	文字顏色 LEGEND COLOR	白-WHITE		白-WHITE	ACC	
8	V-cut 刀數	2	刀	2		
9	V-cut 殘厚	0.6	mm	0.53		
10	斜邊角度	30	°	30		
11	斜邊深度	0.78	mm	0.78		
12	板彎/板翹 BOWING/TWIST	<0.75%	mm	0.01	ACC	<0.75%
13	阻抗測試 IMPDEMANCE TEST	附件四			ACC	
14	疊板結構 STACK-UP STUCTURE	附件一			ACC	
15	外觀 CHECK	依IPC-A-600規範			ACC	
	尺寸確認 DIMENSIONAL INSPECTION					
1	單片尺寸 BOARD SIZE	214.5*32.5	mm	214.52*32.51	ACC	(±0.1)
2	連板尺寸 PNL SIZE	230.5*207	mm	230.52*207.02	ACC	(±0.1)
3	外型尺寸 DIMENSION	附件三			ACC	
4	孔徑尺寸 HOLE SIZE	附件二			ACC	
	剝離測試 PEELING TEST					
1	防焊 PEELING TEST	3M#610 膠帶			ACC	
2	文字 PEELING TEST	3M#610 膠帶			ACC	
3	線路 PEELING TEST	3M#610 膠帶			ACC	
4	化(鍍)金 PEELING TEST	3M#610 膠帶			ACC	
	信賴性測試RELIABILITY TEST					
1	焊錫性 SOLDER ABILITY	260+/-5度C/5sec			ACC	
2	熱應力試驗 THERMAL STRESS ABILIT	288+/-5度C/10sec 循環3次			ACC	

Figure 57 - RC-PE1U14-TY PCB Test Report

Riser Card, Left Side:

邑昇實業股份有限公司 出貨檢驗報告
EISO INSPECTION REPORT

客戶名稱: CUSTOMER:	思創科技股份有限公司	出貨數量: QTY:	54 PCS
客戶料號: CUSTOMER P/N:	47G0121N010K BRC-PE10015A_A02	週期: DATE CODE:	1815
供應商料號: VENDER P/N:	EG1001210R0A	日期: DATE:	2018/5/11

檢驗內容
INSPECTION DESCRIPTION

NO:	檢驗項目 INSPECTION ITEM	規格 SPEC	單位 UNIT	實際 ACTUAL	結果 RESULT	備註 REMARK
	材料 MATERIAL					
1	基材供應商 MATERIAL SUPPLIER	IT180		IT180	ACC	
2	基板材質 BASE OF MATERIAL	FR-4		FR-4	ACC	
3	耐熱等級 FLAMMABILITY CLASS	94V-0		94V-0	ACC	
4	銅箔 COPPER FOIL	1/1	mil	0	ACC	
5	層面結構 LAYER TACK	4	LAYERS	4	ACC	
6	公司商標 LOGO	E		E	ACC	
7	UL	ES6		ES6	ACC	
	防焊 SOLDER MASK					
1	型號 BRAND TYPE	PSR2000 LF07		PSR2000 LF07	ACC	
2	防焊顏色 S/M COLOR	綠-GREEN		綠-GREEN	ACC	
3	防焊厚度 S/M THICKNESS	0.4(min)	mil	0	ACC	
	外觀 APPEARANCE					
1	表面處理 SURFACE FINISHED	化金		化金	ACC	
2	GOLD SRFACE THICKNESS 金厚度 Au THICKNESS 鎳厚度 Ni THICKNESS	 >3u" >120 u"	μin	 (x)3.341 (x)136.58	ACC	
3	線寬 NESTED LINE WIDTH	4.60 mil ±20%	mil	4.79	ACC	
4	線距 NESTED LINE SPACING	5.40 mil ±20%	mil	5.22	ACC	
5	板厚 BOARD THICKNESS	1.6±0.16	mm	1.62	ACC	
6	文字廠商 LEGEND SUPPLIER	永勝泰		永勝泰	ACC	
7	文字顏色 LEGEND COLOR	白-WHITE		白-WHITE	ACC	
8	V-cut 刀數	2	刀	2		
9	V-cut 殘厚	0.6	mm	0.54		
10	斜邊角度	30	°	30		
11	斜邊深度	0.78	mm	0.78		
12	板彎/板翹 BOWING/TWIST	<0.75%	mm	0.01	ACC	<0.75%
13	阻抗測試 IMPDEMANCE TEST	附件四			ACC	
14	疊板結構 STACK-UP STUCTURE	附件一			ACC	
15	外觀 CHECK	依IPC-A-600規範			ACC	
	尺寸確認 DIMENSIONAL INSPECTION					
1	單片尺寸 BOARD SIZE	214.5*32.5	mm	214.52*32.51	ACC	(±0.1)
2	連板尺寸 PNL SIZE	230.5*207	mm	230.52*207.02	ACC	(±0.1)
3	外型尺寸 DIMENSION	附件三			ACC	
4	孔徑尺寸 HOLE SIZE	附件二			ACC	
	剝離測試 PEELING TEST					
1	防焊 PEELING TEST	3M#610 膠帶			ACC	
2	文字 PEELING TEST	3M#610 膠帶			ACC	
3	線路 PEELING TEST	3M#610 膠帶			ACC	
4	化(鍍)金 PEELING TEST	3M#610 膠帶			ACC	
	信賴性測試RELIABILITY TEST					
1	焊錫性 SOLDER ABILITY	260+/-5度C/5sec			ACC	
2	熱應力試驗 THERMAL STRESS ABILI	288+/-5度C/10sec 循環3次			ACC	

Figure 58 - RC-PE1U15-TY PCB Test Report

Backplane:

邑昇實業股份有限公司 出貨檢驗報告
EISO INSPECTION REPORT

客戶名稱: CUSTOMER:	思創科技股份有限公司	出貨數量: Q'TY:	60 PCS
客戶料號: CUSTOMER P/N:	TBBP-HD10021A_B01	週期: DATE CODE:	1817
供應商料號: VENDER P/N:	EG1001016G0A	日期: DATE:	2018/5/11

檢驗內容
INSPECTION DESCRIPTION

NO:	檢驗項目 INSPECTION ITEM	規格 SPEC	單位 UNIT	實際 ACTUAL	結果 RESULT	備註 REMARK
	材料 MATERIAL					
1	基材供應商 MATERIAL SUPPLIER	IT180		IT180	ACC	
2	基板材質 BASE OF MATERIAL	FR-4		FR-4	ACC	
3	耐熱等級 FLAMMABILITY CLASS	94V-0		94V-0	ACC	
4	銅箔 COPPER FOIL	1/1	mil	1.852	ACC	
5	層面結構 LAYER TACK	16	LAYERS	16	ACC	
6	公司商標 LOGO	㊣		㊣	ACC	
7	UL	ES6		ES6	ACC	
	防焊 SOLDER MASK					
1	型號 BRAND TYPE	PSR2000 LF07		PSR2000 LF07	ACC	
2	防焊顏色 S/M COLOR	綠-GREEN		綠-GREEN	ACC	
3	防焊厚度 S/M THICKNESS	0.4(min)	mil	0.794	ACC	
	外觀 APPEARANCE					
1	表面處理 SURFACE FINISHED	化金		化金	ACC	
2	GOLD SRFACE THICKNESS 金厚度 Au THICKNESS 鎳厚度 Ni THICKNESS	>3u" >120 u"	μ in	(x)3.325 (x)135.45	ACC	
3	線寬 NESTED LINE WIDTH	4.0 mil ±20%	mil	4.22	ACC	
4	線距 NESTED LINE SPACING	4. mil ±20%	mil	3.87	ACC	
5	板厚 BOARD THICKNESS	2.4±0.24	mm	2.41	ACC	
6	文字廠商 LEGEND SUPPLIER	永勝泰		永勝泰	ACC	
7	文字顏色 LEGEND COLOR	白-WHITE		白-WHITE	ACC	
8	V-cut 刀數	1	刀	1	ACC	
9	V-cut 殘厚	0.8	mm	0.8	ACC	(±0.1)
10	斜邊角度	N/A	°	N/A		
11	斜邊深度	N/A	mm	N/A		
12	板彎/板翹 BOWING/TWIST	<0.75%	mm	0.01	ACC	<0.75%
13	阻抗測試 IMPDEMANCE TEST	附件四			ACC	
14	疊板結構 STACK-UP STUCTURE	附件一			ACC	
15	外觀 CHECK	依IPC-A-600規範			ACC	
	尺寸確認 DIMENSIONAL INSPECTION					
1	單片尺寸 BOARD SIZE	420*150	mm	420.02*150.01	ACC	(±0.1)
2	連板尺寸 PNL SIZE	158*420	mm	158.02*420.03	ACC	(±0.1)
3	外型尺寸 DIMENSION	附件三			ACC	
4	孔徑尺寸 HOLE SIZE	附件二			ACC	
	剝離測試 PEELING TEST					
1	防焊 PEELING TEST	3M#610 膠帶			ACC	
2	文字 PEELING TEST	3M#610 膠帶			ACC	
3	線路 PEELING TEST	3M#610 膠帶			ACC	
4	化(鍍)金 PEELING TEST	3M#610 膠帶			ACC	
	信賴性測試RELIABILITY TEST					
1	焊錫性 SOLDER ABILITY	260+/-5度C/5sec			ACC	
2	熱應力試驗 THERMAL STRESS ABILI	288+/-5度C/10sec 循環3次			ACC	

Figure 59 - Backplane PCB Test Report

14.8 Secondary Component

All secondary components are listed in the BOM, respectively. Please refer to the lists immediately below.

Motherboard:

	YRMFS016			Orient Semiconductor Electronics, Limited			Page:1
	Plant ID : FP			AVL & Customer Relation Report By BOM (Model)			Date:06/08/2018
	OSE Model:DEG053P0089		Cust Model:BMB-DPS0003B_A03	Description:LYNX OCP 8 + 16 REV.A3			
EOL	OSE P/N	Customer P/N	Description	Vendor	Vendor P/N	QTY	Location
	11G0019-006N	MP-00004637-000	STICKER FOR SOCKET 771 CAP	ABLECOM	04-LBL00XXXX001T001	2	CPU0_STICKER.CPU1_STICKER
	98GDE00-010	H87U000000-00013-0	LABEL AMI MEGARAC 10*10MM COLD	DIGIPRO	AST2500A2-GP	1	LABLE-BMC
		MP-00004493-000		DIGIPRO	AST2500A1-GP		
		CM1-00004493		DIGIPRO	AST2400A1-GP		
				DIGIPRO	AST2150A2-GP		
				DIGIPRO	AST2050A3-GP		
				AMI	5013		
	98GDE00-252	H87U000000-00000-1	INSYDE BIOS LABEL	INSYDE	H87U000000-00000-1	1	LABLE-BIOS
		MP-00005156-000					
		CM1-00005156					
	98GDE03-003	H54U000000-SA00100	SOCKET LGA3647-P0 NRW-NF CLIP	FOXCONN	WNMEL00-82N00-EH	2	JCPU1_CLIP.JCPU0_CLIP
		MP-00005658-000					
		CM1-00005658					
	DEG053-101M		433.87*424.18mm Packing			1	
	12G0002-499G		510(L)X440(W)X500(H) M/M	CHIN HWA	12G0002-499G	0.143	
	12G0004-004D		1500(L)*1300(W)*0.1(THK) M/M	HONG MING		0.018	
				TAO TI			
				TAO TI	12G0004-004D		
	12G0004-097D		860(L)X(620+600)X0.08(THK) (METAL)	TAO TI	12G0004-097D	1	
	12G0004-398K		85*120* M/M (NO.4)	YANG CHIN	12G0004-398K	0.143	
				YANG CHIN			
				TAO TI			
				TAO TI	12G0004-398K		
	12G0005-015F		160(L)*(140+70)(W)*φ10 M/M (TRI. ANTI.)	TAO TI	12G0005-015F	1	
				TAO TI			
				HONG MING			
	12G0009-007H		1000(L)*55(W)*55(H)* M/M (RIGHT)	CHIN HWA	12G0009-007H	0.143	
				CHIN HWA			
	12G0009-965Z		505(L)X435(W)X7.5(THK) M/M	CHIN HWA	12G0009-965Z	0.286	

BMB-DPS0003B_A03_20181227.xls

Riser Card: RC-PE1U14-TY:

Content & Block Diagram Revised: Tuesday, May 16, 2017										
RC-PE1U14-TY Revision: A										
B45-1TBPX1-X00A100										
BRC-PE10014A_A02										
Item	Insert	Quantity	Reference	Description	Manuf1_name	Manuf1_PN	AIC PN1_12	AIC PN1_18	Manuf2_name	Manuf2_PN
Consign part										
1	I	2	J1,J2	CONN,SAS,SLIMLINE 12I,VT,85ohm,SMD,P0.6,74P,SIL	Amphenol	P-U10-K274-350T	CM1-00006257_A01			
2	I	3	U2000,U2001,U2002	IC,REPEATER,DS80PCI800SQ,SQA54A,54P,	NS	DS80PCI800SQ	CM1-00004630	C01ZDS80PCI8990TI0		
SMD										
1	I	18	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18	CAP,X5R,0.1uF,0402,25V,0.1	TDK	C1005X5R1E104KT000E				
2	I	48	C2000,C2001,C2002,C2003,C2004,C2005,C2006,C2007,C2008,C2009,C2010,C2011,C2012,C2013,C2014,C2015,C2016,C2017,C2018,C2019,C2020,C2021,C2022,C2023,C2024,C2025,C2026,C2027,C2028,C2029,C2030,C2031,C2032,C2033,C2034,C2035,C2036,C2037,C2038,C2039,C2040,C2041,C2042,C2043,C2044,C2045,C2046,C2047	CAP,X5R,0.22UF,0201,6.3V,10%	WALSIN TECHNOLOGY	0201X224K6R3CT				
3	I	4	R1,R10,R20,R21	RES,CHIP,0402,4K7 OHM,5%,1/16W	WALSIN TECHNOLOGY	WR04X472 JTL				
4	I	18	R5,R8,R12,R13,R2002,R2007,R2012,R2017,R2018,R2022,R2023,R2033,R2044,R2046,R2052,R2053,R2054,R2058	RES,CHIP,0402,1K OHM,5%,1/16W	WALSIN TECHNOLOGY	WR04X102 JTL			YAGEO	RC0402JR-071KL
5	I	9	R14,R17,R2008,R2014,R2035,R2037,R2040,R2042,R2063	RES,CHIP,0402,1K OHM,1%,1/16W	WALSIN TECHNOLOGY	WR04X1001FTL				
DIP										
1	I	1	J3	CONN,BOX-HDR,PHD105-6T,DIP,P2.0,2x5P,BLK	Anytronic	182002151000#0-BLF			HAOGUO/JS-CONN	PHD105-BK-6T
2	I	1	PCIE1	CONN-F,PCI-E,DICONN,PCIE,2E004917-DPDB-DF ,DIP,P1.0,98P,BI	WINWIN	WPES-098AN41B22UWC				

BRC-PE10014A_A02_RC-PE1U14-TY_A1

Riser Card: RC-PE1U15-TY:

Content & Block Diagram Revised: Tuesday, May 16, 2017
RC-PE1U15-TY Revision: A
B45-1T-PX1-X00A100
BRC-PE10015A_A02

Item	Insert	Quantity	Reference	Description	Manuf1_name	Manuf1_PN	AIC PN1_12	AIC PN1_18	Manuf2_name	Manuf2_PN
Consign part										
1	I	2	J1,J2	CONN,SAS,SLIMLINE 12i,VT,85ohm,SMD,P0.6,74P,SIL	Amphenol	P-U10-K274-350T	CM1-00006257_A01			
2	I	3	U2000,U2001,U2002	IC,REPEATER,DS80PCI8005Q,SQA54A,54P,	NS	DS80PCI8005Q	CM1-00004650	C01ZDS80PCI8990TI0		
SMD										
1	I	18	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18	CAP,X5R,0.1uF,0402,25V,0.1	TDK	C1005X5R1E104KT000E				
2	I	48	C2000,C2001,C2002,C2003,C2004,C2005,C2006,C2007,C2008,C2009,C2010,C2011,C2012,C2013,C2014,C2015,C2016,C2017,C2018,C2019,C2020,C2021,C2022,C2023,C2024,C2025,C2026,C2027,C2028,C2029,C2030,C2031,C2032,C2033,C2034,C2035,C2036,C2037,C2038,C2039,C2040,C2041,C2042,C2043,C2044,C2045,C2046,C2047	CAP,X5R,0.22UF,0201,6.3V,10%	WALSIN TECHNOLOGY	0201X224K6R3CT				
3	I	1	R1	RES,CHIP,0402,0R OHM,5%,1/16W	WALSIN TECHNOLOGY	WR04X000 PTL				
4	I	4	R2,R3,R5,R6	RES,CHIP,0402,4K7 OHM,5%,1/16W	WALSIN TECHNOLOGY	WR04X472 JTL				
5	I	18	R8,R10,R18,R22,R2002,R2011,R2012,R2017,R2029,R2031,R2033,R2038,R2043,R2044,R2050,R2053,R2054,R2055	RES,CHIP,0402,1K OHM,5%,1/16W	WALSIN TECHNOLOGY	WR04X102 JTL			YAGEO	RC0402JR-071KL
6	I	9	R2007,R2013,R2021,R2022,R2024,R2036,R2047,R2056,R2059	RES,CHIP,0402,1K OHM,1%,1/16W	WALSIN TECHNOLOGY	WR04X1001FTL				
DIP										
1	I	1	J3	CONN,BOX-HDR,PHD10S-6T,DIP,P2.0,2x5P,BLK	Anytronic	1820021S1000H0-BLF			HAOGUO/JS-CONN	PHD10S-BK-6T
2	I	1	PCIE1	CONN-F,PCI-E,DIP,P1.0,164P,BLK	WINWIN	WPES-164AN41B22UW5				

BRC-PE10015A_A02
_RC-PE1U15-TY_A1

Backplane:

M3 NVMe SSDs x36 system Revised: Friday, March 21, 2018
BP-HD1H07-TY Revision: B01
TBBP-HD10021A_B01

Item	Insert	Quantity	Reference	Description	Manuf1_name	Manuf1_PN	AIC PN1_12	AIC PN1_18
Consign part								
1	I	9	CON_M3_1,CON_M3_2,CON_M3_3,CON_M3_4,CON_M3_5,CON_M3_6	CONN,NGFF,NGFF_M3_RA_M_KEY_1x4 ,DIP,P1.1,300P,STD	Amphenol	CE1006700424041	CM1-00006126	E07-T10TV8RFH00AH0
2	I	4	J8,J9,J12,J13	CONN,SAS,SLIMLINE 12i,VT,85ohm,SMD,P0.6,74P,SIL	Amphenol	P-U10-K274-350T	CM1-00006257	
3	I	1	JSYS_EXT1	CONN,PCIE,SFF-8612(Vertical),SMD,P0.5,42P,SIL	Amphenol	G14A42221612HR	CM1-00005637	E01-020H2LRFH00AH0
4	I	2	U21,U22	IC,CHIPEST,PEX9797,HFC-BGA,1156P	AVAGO	PEX9797-B080BC G	CM1-00006118	C013PEX9797B240L50
5	I	2	U19,U126	IC,I2C,PCA9552,TSSOP,24P,	NXP	PCA9552PW	CM1-00005164	C01ZPCA9552P070RW0
6	I	36	U90,U91,U92,U93,U94,U95,U96,U97,U98,U99,U100,U101,U102,U103,U	IC,PWR CTRL,TPS259261,VSON(10),10P,	TEXAS INSTRUMENTS	TPS259261	CM1-00005574	C01ZPS259261990TI0
7	I	3	U42,U43,U44	IC,CLOCK,9DB1233AGLFT,TSSOP,64P,	IDT	9DB1233AGLFT	CM1-00005615	C0179DB1233A070IDO
9	I	2	U27,U28	IC,CLOCK,9DB433AGILFT,TSSOP,28P,	IDT	9DB433AGILFT	CM1-00004643	C0179DB433AG070IDO
10	I	2	U8,U11	IC,PWM,ISL6353CRTZ,TQFN,40P,	INTERSIL	ISL6353CRTZ	CM1-00004024	C332-ISL63532102T0
11	I	2	U20,U23	IC,PWM,TPS56C215RNNT,QFN,17P,	TEXAS INSTRUMENTS	TPS56C215RNNT	CM1-00006067	C01STPS56C21290TI0
12	I	1	U41	IC,PWM,MPQ8633BGLE,QFN,21P,	MPS	MPQ8633BGLE	CM1-00005821	C01SMPQ8633B290MP0
13	I	6	U9,U15,U16,U24,U30,U32	IC,REPEATER,DS80PCI800SQ,SQA54A,54P,	NS	DS80PCI800SQ	CM1-00004650	C01ZDS80PCI8990TI0
14	I	1	U5	IC,HW_MONITOR,W83795G,LQFP,64P,	NUVOTON	W83795G	CM1-00005045	C01ZW83795G-120NT0
SMD								
1	I	198	C1,C3,C5,C6,C10,C11,C14,C16,C17,C19,C133,C143,C150,C161,C197,C238	CAP,X5R,0.1uF,0402,25V,0.1	TDK	C1005X5R1E104KT000E		
2	I	4	C4,C9,C2012,C2021	CAP,X5R,0805,22UF,6V3,20%	SAMSUNG	CL21A226MQQNNNE		
3	I	6	C7,C8,C12,C627,C628,C2002	CAP,X5R,10UF,0805,25V,10%	TDK	C2012X5R1E106KT		
4	I	14	C13,C165,C190,C562,C626,C2011,C2019,C2020,C2071,C2095,C2099,C21(	CAP,X5R,1uF,0402,16V,10%	TAIYO	EMK105BJ105KV-F		
5	I	2	C15,C665	CAP,X7R,0402,220PF,50V,10%	WALSIN TECHNOLOGY	0402B221J500CT		
6	I	6	C18,C23,C139,C174,C2484,C2526	CAP,Y5V,1UF,0603,25V,20%	TAIYO	CETMK107F105MOOT		
7	I	8	C20,C22,C24,C68,C69,C70,C2027,C2033	CAP,X7R,0402,0.1UF,16V,10%	WALSIN TECHNOLOGY	0402B104K160CT		
8	I	1	C21	CAP,X7R,330PF,0402,50V,10%	YAGEO	CC0402KRX7R9BB331		
9	I	8	C25,C65,C71,C156,C179,C196,C201,C275	CAP,X5R,22uF,1206,16V,20%	MURATA	GRM31CR61C226ME15L		
10	I	4	C27,C131,C622,C623	CAP,X7R,2200PF,0402,50V,10%	WALSIN	0402B222J500CT		
11	I	480	C28,C29,C30,C31,C32,C33,C34,C35,C36,C37,C38,C39,C40,C41,C42,C43,C(	CAP,X5R,0.22UF,0201,6.3V,10%	WALSIN TECHNOLOGY	0201X224K6R3CT		
12	I	20	C64,C384,C404,C2039,C2041,C2048,C2069,C2078,C2079,C2092,C2121,C(	CAP,X5R,22uF,0603,6V3,20%	SAMSUNG	CL10A226MQ8NRNE		
13	I	64	C66,C399,C405,C409,C2042,C2043,C2044,C2045,C2046,C2049,C2050,C2(	CAP,X5R,1UF,0402,6.3V,10%	YAGEO	CC0402KRX5R5BB105		
14	I	4	C67,C155,C198,C274	CAP,X7R,0402,1000PF,50V,10%	WALSIN TECHNOLOGY	0402B102K500CT		
15	I	6	C72,C129,C160,C175,C448,C464	CAP,X5R,1206,10UF,25V,20%	MATSUSHITA	ECJ3YB1E106M		
16	I	8	C135,C208,C260,C261,C2058,C2067,C2081,C2145	CAP,X7R,0603,0.22UF,25V,10%	WALSIN TECHNOLOGY	0603B224K250CT		
17	I	2	C137,C246	CAP,X5R,0402,0.22UF,6.3V,10%	WALSIN TECHNOLOGY	0402X224K6R3CT		
18	I	2	C144,C231	CAP,X5R,0402,0.22UF,6.3V,10%	WALSIN TECHNOLOGY	0402X224K6R3CT		
19	I	29	C145.C230.C498.C2566.C2567.C2568.C2569.C2571.C2573.C2574.C2575.(	CAP,X7R,0402,0.1UF,16V,10%	WALSIN TECHNOLOGY	0402B104K160CT		

TBBP-HD10021A_B
01_BP-HD1H07-TY_