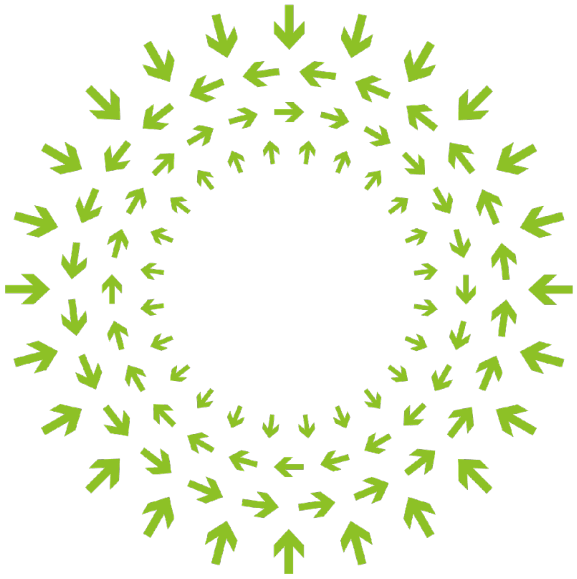

OPEN

Compute Project

HGX Form Factor Specification

Revision 1.0
Version 0.1

Author: Nvidia (John Norton, Rob Ober)

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1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

Whitney Zhao (Meta)
Song Kok Hang (Intel)

2. Compliance with OCP Tenets

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2.1. Openness

The measure of openness is the ability of a third party to build, modify, or personalize the device or platform from the contribution. OCP strives to achieve completely open platforms, inclusive of all programmable devices, firmware, software, and all mechanical and electrical design elements. Any software utilities necessary to modify or use design contributions should also be open-sourced. Barriers to achieving this goal should be constantly addressed and actions taken to remove anything that prevents an open platform. Openness can also be demonstrated through collaboration and willingness to share, seek feedback, and accept changes to design and specification contributions under consideration.

HGX based systems are the most common AI Training platform globally. The optimized AI Training frameworks, Cuda libraries, communication libraries, tuned neural networks as well as most AI research are open and available via GitHub and container repositories. Open MLPerf results enable anyone to replicate state of the art performance and productivity, and often HGX partners do replicate perf results and publish in MLPerf releases.

2.2. Efficiency

Continuous improvement has been a fundamental value of the industry. New contributions (and updates to existing contributions) shall be more efficient than existing or prior generation contributions. Efficiency can be measured in many ways - OpEx and CapEx reduction, performance, modularity, capacity, power or water consumption, raw materials, utilization, size, or floorspace are some examples. The goal is to express efficiency with clear metrics, valued by end-users, when the contribution is proposed.

This is the 3rd generation HGX board form factor. Each generation has provided ~3x-5x higher AI Training throughput, while consuming similar active power. As a result, the HGX board is now the defacto-standard, with most global hyperscalers designing around this form factor for AI training and inference.

2.3. Impact

OCP contributions should have a transformative impact on the industry. This impact can come from introducing new technology, time-to-market (TTM) advantage of technology, and/or enabling technology through supply chains that deliver to many customers in many regions of the world. New technologies are impactful when such technology is enabled through a global supply channel. One example is the NIC 3.0 specification that achieved global impact by having over 12 companies author, adopt, and supply products that conformed to the specification. Another example is emerging and open security features that establish and verify trust of a product.

The NVIDIA HGX platforms have become the defacto global standard for AI training platforms. Systems are deployed at most global hyperscalers and built by most global ODMs and OEMs. Opening this HGX form factor allows other AI accelerator vendors to leverage the HGX ecosystem of systems and enclosures. This should accelerate other AI vendors.

2.4. Scale

OCP contributions must have sufficient enabling, distribution, and sales support (pre and post) to scale to Fortune 100 as well as large hyperscale customers. Demonstration of this tenet can be accomplished by providing sales data or by providing go-to-market plans that involve either platform/component providers or systems integrator/VAR (direct and/or channel). Platform/component providers or systems integrators/VARs that can use this contribution to obtain product recognition (OCP Accepted™ or OCP Inspired™) and create Integrated Solutions, which would also demonstrate scale. Software projects can also demonstrate this tenet when software is adopted across business segments or geographies, when software is a key factor in accelerating new technology, or when software provides scale of new hardware, which meets OCP tenets.

Globally, hundreds of thousands of HGX systems are in production. The current form factor will also deploy at scale. The systems and enclosures for this form factor will be stable, and built at scale.

3. Version Table

Date	Version #	Author	Description
4/26/22	0.1	John Norton	Initial Draft

4. Scope

This document defines the technical details for one of the following types of specifications:

- base specification for a de-facto standard (new standard with no hardware product)
- base specification for an intended physical <hardware product type>
- modification of an existing specification (state that existing specification is being modified)
    - either a complete revision update or
    - a minor version update
- a detailed specification for a GPU Baseboard Assembly with a product being available in 120 days of approval of this specification.

Any supplier seeking OCP recognition for a hardware product based on this specification must be 100% compliant with any and all features or requirements described in this specification.

5. Overview

This document describes an HGX GPU baseboard assembly form factor that may be incorporated into an adopter's tray and chassis design. The HGX assembly includes 8-GPU modules with heat sinks attached to a host PCBA with mounting features and connector interfaces for PCIe and power. This specification documents mechanical dimensions required for mounting, connector pinouts, and electrical specifications required for an adopter to design a chassis and midplane assembly. Figure 1 illustrates the 3D volumetric of the assembly being specified.

Figure 1. HGX Baseboard Assembly Form Factor

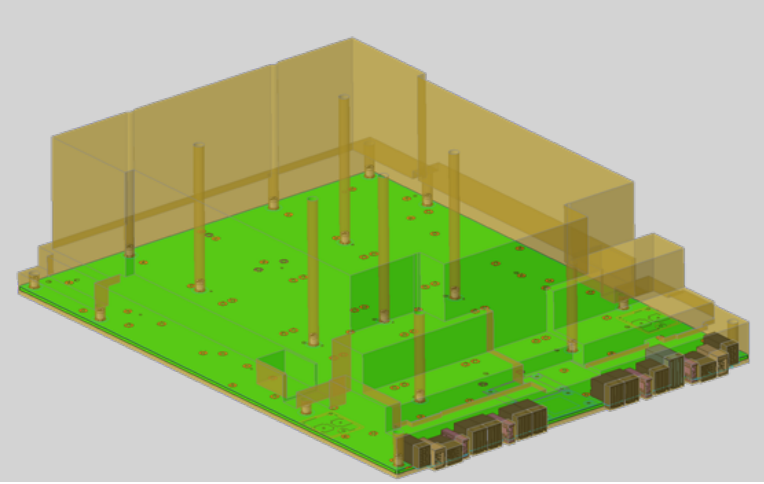


Table 1. HGX GPU Baseboard Specifications

Specification	Description
Baseboard power	Up to 6860 W[1]
Power connectors and headers	4 × AirMax connectors 2 × PwrMAX connectors 4 × RadSok pins
GPU	Hopper based SXM, eight per baseboard
NVLink	NVSwitch, four per baseboard
PCI Express interface (to CPU node)	8 × PCI Express 5.0 x16 (for SXM5) 1 × PCI Express 4.0 x2 (for NVLink Fabric) Lane and polarity reversal supported
System management interface	2 × I2C (400 KHz maximum speed, 100 KHz supported) 1 x PCI Express 2.0 x1 (for FPGA) 1 x USB 2.0 (for HMC)

Specification	Description
Baseboard dimensions (without connectors)	553.0 mm × 416.0 mm × 153.2 mm
Baseboard dimensions (with connectors)	565.4 mm × 416.0 mm × 153.2 mm
Baseboard weight (estimated	31.8 kg (~70 lbs) for fully populated baseboard Includes all heat sinks and handles
Baseboard LED indicators	Six LED indicators

Note:
[1]Based on maximum upper limit of 700 W GPU power.

6. Rack Compatibility

The baseboard assembly described in this specification may be mounted in either a standard EIA 19 inch rack or an OCP specified rack using a chassis assembly designed by the adopter.

7. Physical Specifications

The following section specifies the mechanical dimensions of the form factor, mounting locations, and connector locations. For dimensions not shown in the following figures refer to the 3D CAD model contributed with this specification. Figure 2 illustrates maximum XY dimensions of the PCB. Figure 3 illustrates the maximum height, PCB top surface for reference to connector alignment and PCB thickness variation.

Figure 2. Form Factor Volumetric Dimensions

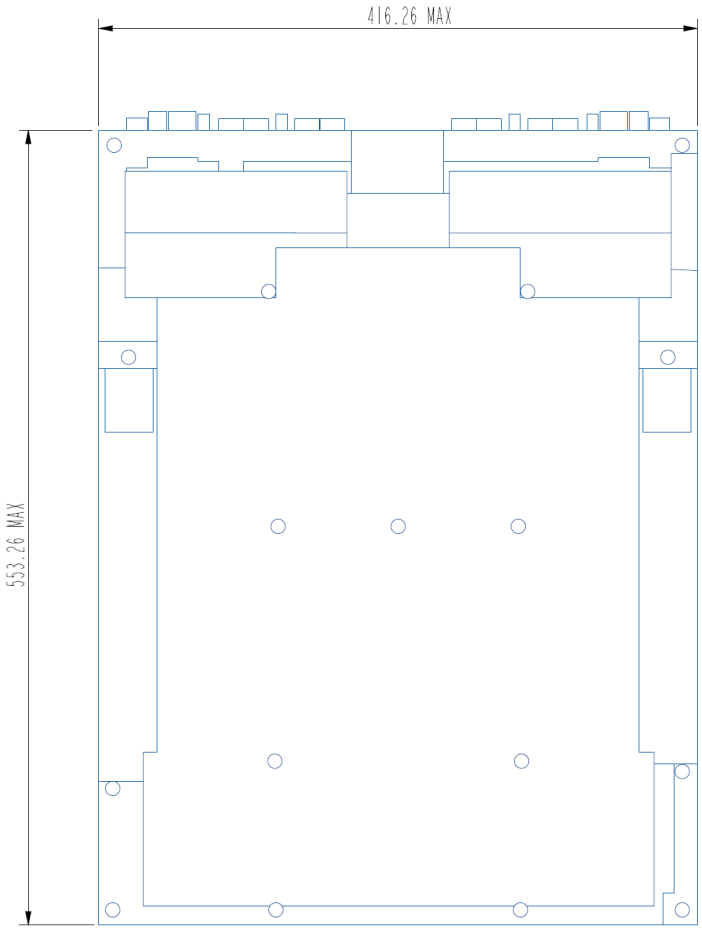
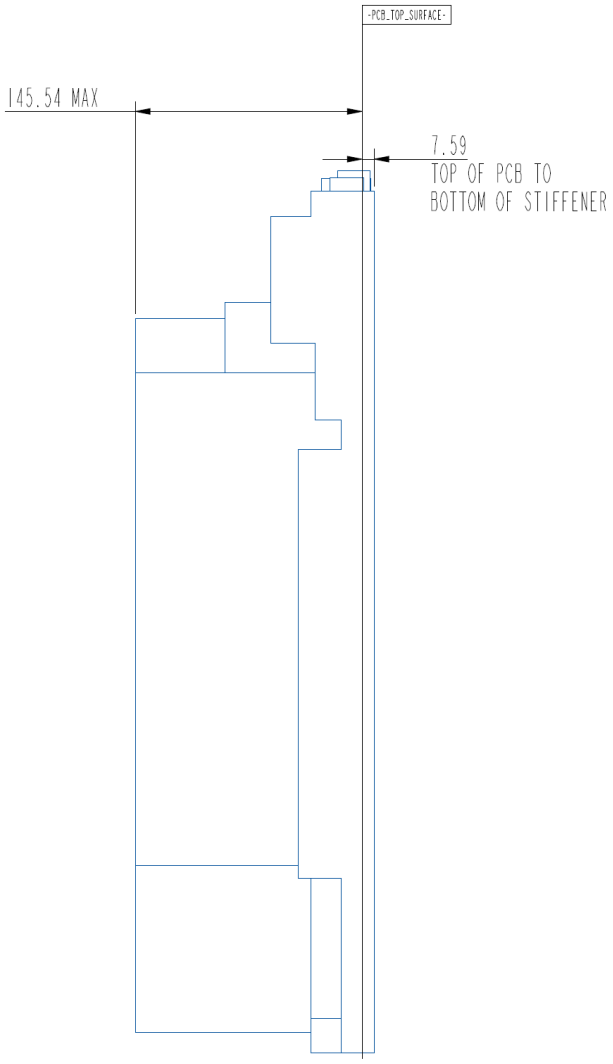


Figure 3. Form Factor Volumetric Dimensions Side View



8. Thermal Design Requirements

Thermal design requirements will be dependent upon the adopter's chassis design, fan configuration, air flow direction, acoustical limits, ambient temperatures, fan power limits and many other factors.

9. I/O System

All connectors on the HGX baseboard are on the PCIe side of the board as illustrated in the following table. These connectors provide eight x16 PCIe Gen5, one x2 PCIe Gen4 and one x1 PCIe Gen2 signals. The connectors also provide 54.0V DC power inputs. The following table provides a summary of the connectors on the baseboard.

Table 2. HGX Baseboard Connector Summary

HGX Baseboard Connectors	Quantity	Purpose	Complementary Mating Connectors
10131762-301LF (6x8)	1	PCIe	10124752-101LF 10124558-101LF[1]
10137002-101LF (4x8)	7	PCIe	10121067-101LF 10128419-101LF[1]
10061289-001LF (2x3)	2	54V Power/GND	10061290-555444PLF 10146092-555444PLF[1]
10028917-001LF (2x2)	2	54V Power/GND	10028916-5544P00LF 10052620-5544P00LF[1]
10136689-003LF	2	54V Power/GND	10136691-001LF 10141042-200A003LF[1]
10037909-101LF (Single Pin)	4	Guide Pin for Mech Assy	10037908-101LF 10044314-101LF[1]
C10-779583-000 (Single Pin, 5.7 mm)	4	54V Power/GND	C10-779657

Note:
[1]For coplanar applications.

All mating and un-mating forces in Table 3 are specified per EIA 364-13 for ExaMAX and AirMax connectors.

Table 3. HGX Baseboard Connector Mating Force

Connector Configuration	HGX Baseboard Connectivity	Number of Connectors	Total Quantity of Mating Contacts per Connector	Maximum Mating Force per Connector (N)	Maximum Compressive Load per Connector (N)	Minimum Unmating Force per Connector (N)
4x8 10137002-101LF	PCIe	7	112	50.4	151.2	11.2
6x8 10131762-301LF	PCIe	1	160	72.0	216.0	16.0
2x3 10061289-001LF	Power	2	6	50.0	150.0	13.5
2x2 10028917-001LF	Power	2	4	33.4	100.2	9.0
10136689-003LF	Power	2	2	40	120	13

Figure 4. HGX Baseboard Connectors

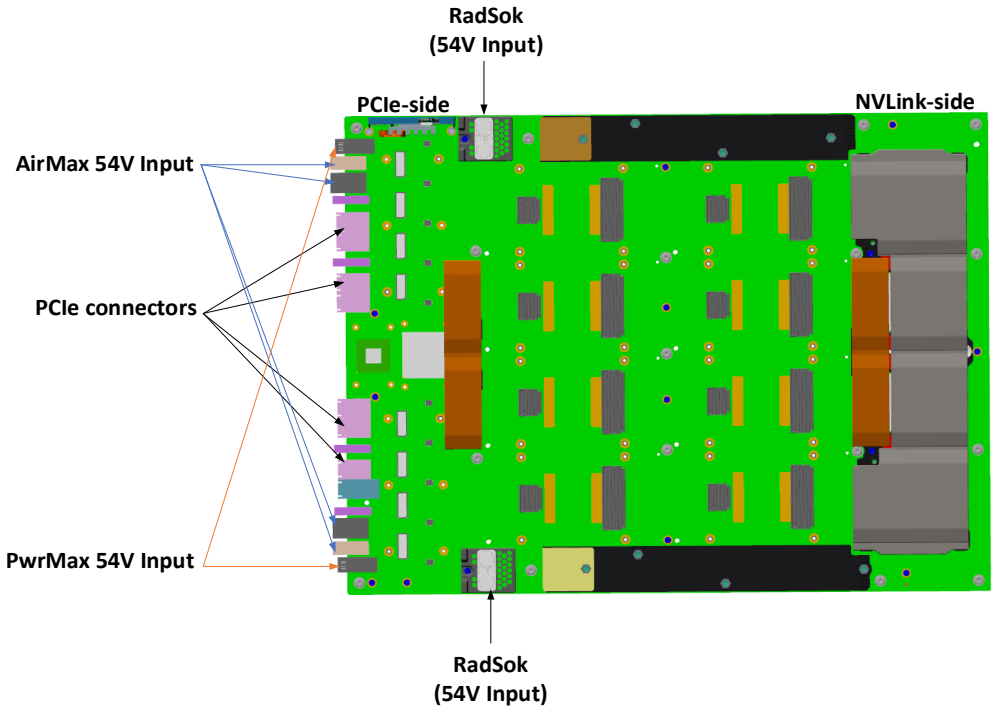


Figure 5. ExaMAX Connector – 10131762-301LF

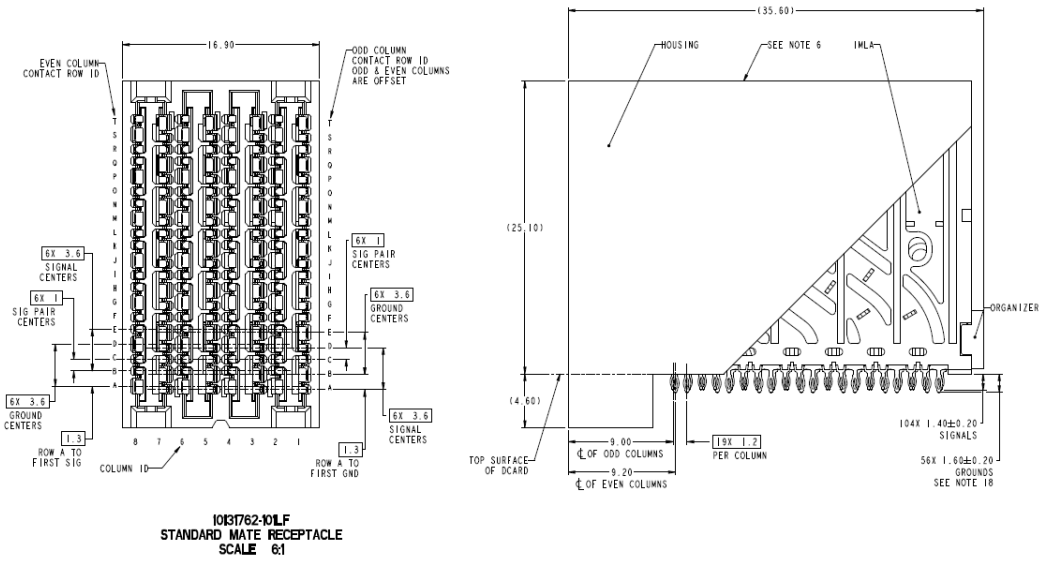


Figure 6 ExaMAX Connector – 10137002-101LF

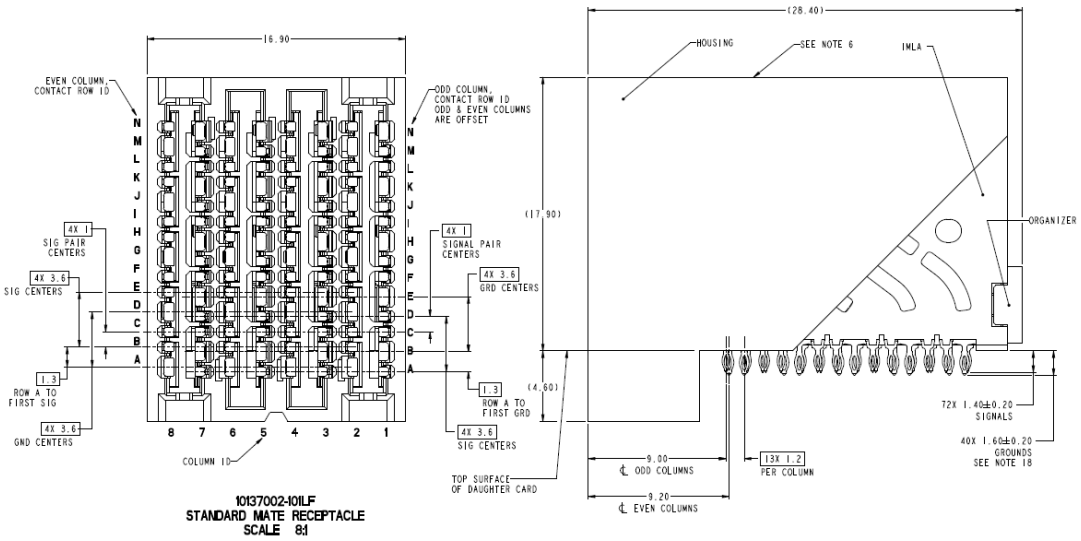


Figure 7. AirMax Connector – 10061289-001LF

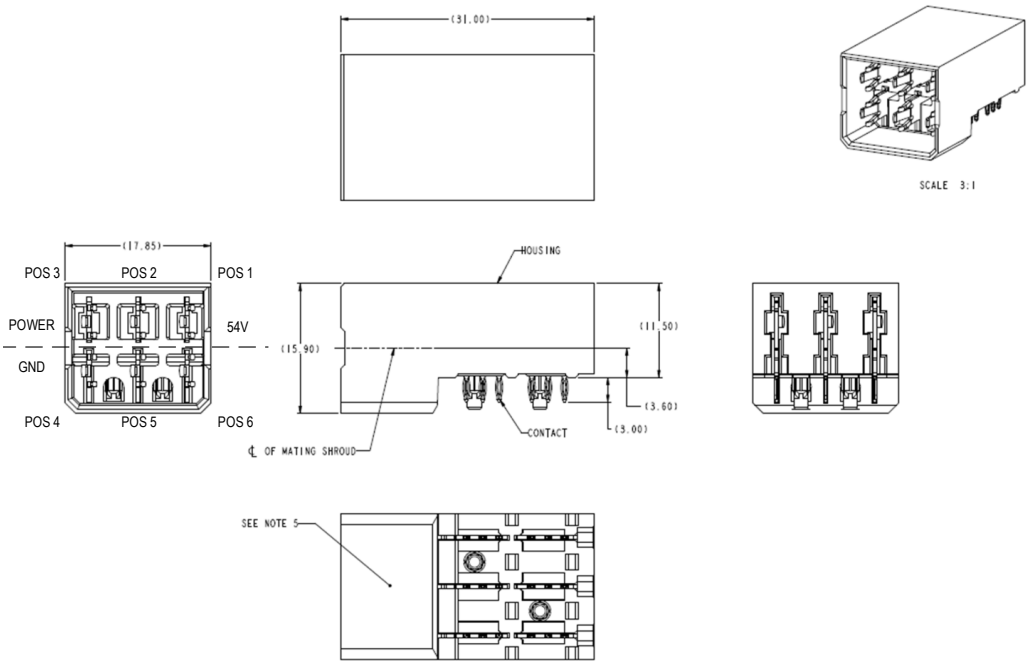


Figure 8. AirMax Connector – 10028917-001LF

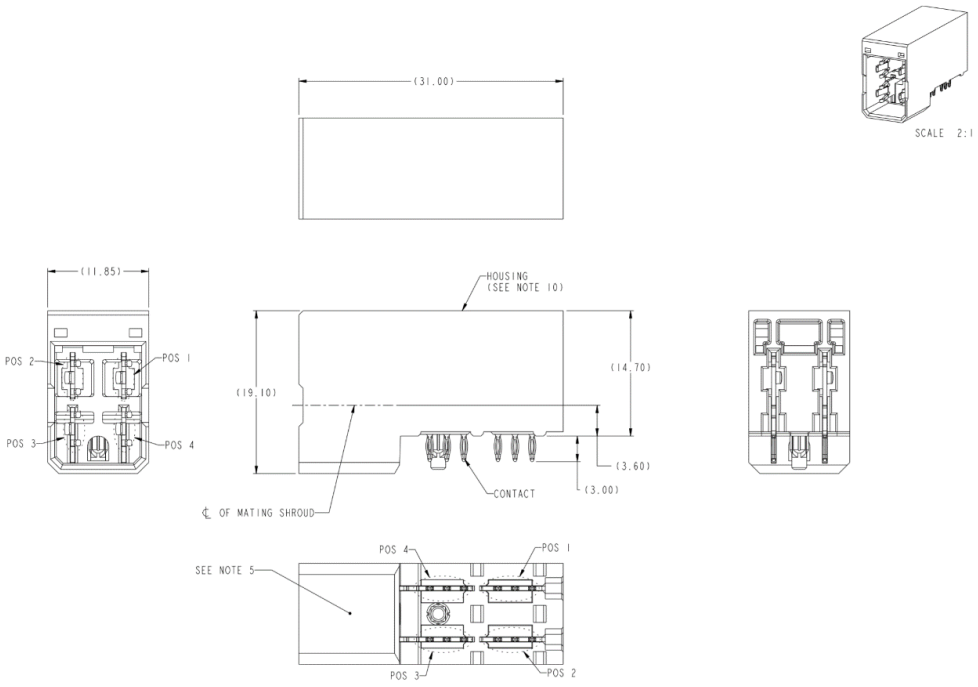


Figure 9. PwrMax Connector – 10136689-003LF

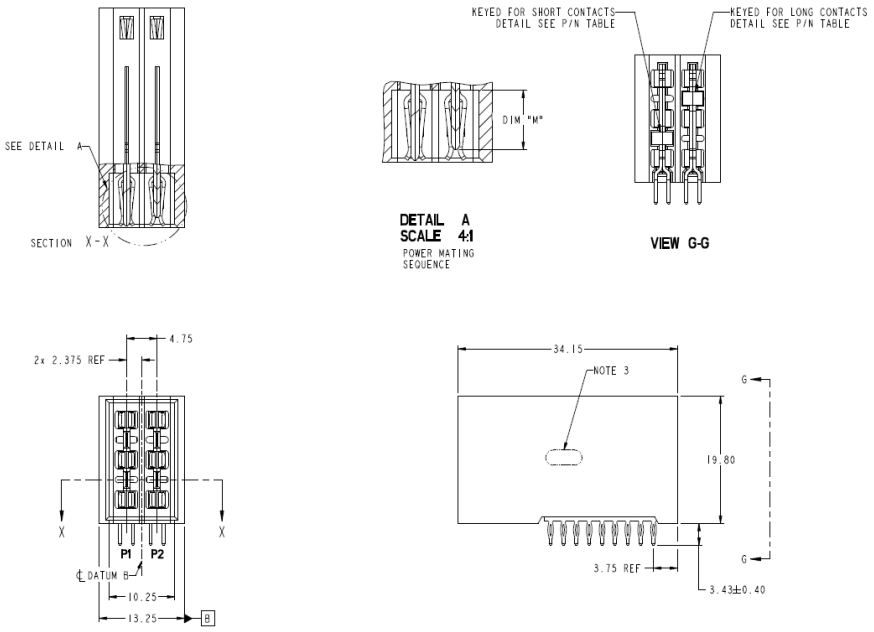
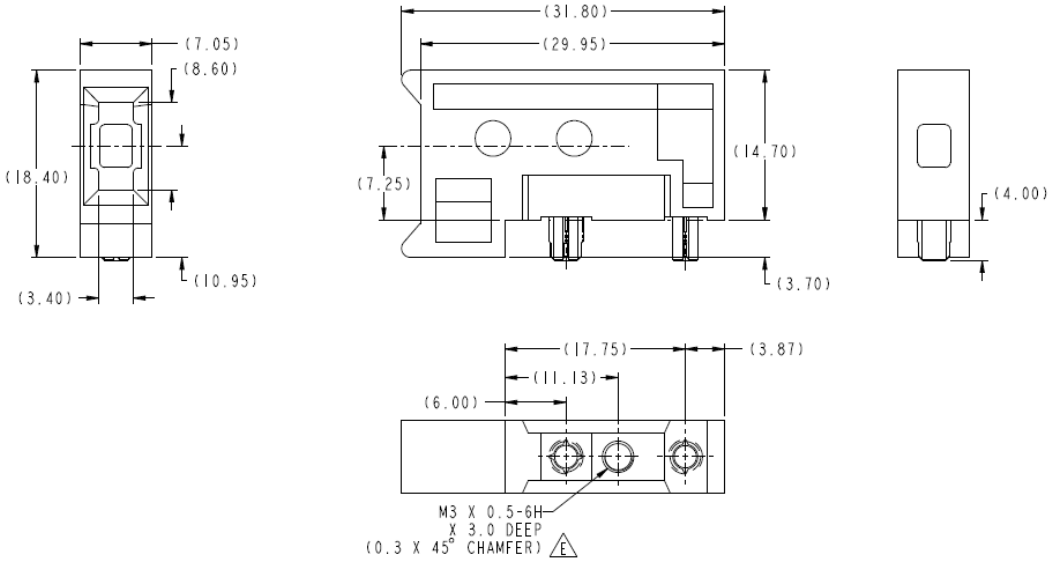


Figure 10. Guide Pin Receptable – 10037909-101LF



Power may be alternatively delivered to the HGX baseboard through cables to the RadSok pin connectors on the baseboard. For RadSok pin connections on the host side, the implementer is recommended to use C10-779583-000. These cables may come from any power source, including directly from a 54.0 V power supply, or from a bus bar. Cables should be properly secured to ensure the system passes shock and vibration tests. If the RadSok connectors are not used, safety covers can be placed over the connectors to minimize exposure to high-voltage potential sources. Amphenol C10-779657 SurLok clamshell assemblies are compatible for power supply connectivity. This SurLok clamshell assembly is used in a cable assembly that consists of five twisted pairs of 10 AWG wires (reference part number: CR-302018-319 for 1 m, CR302024-319 for 330 mm cable).

Input power cable inductance is an important system design consideration and cable length should be kept as short as possible. Maximum suggested cable length is 1 m.

Figure 11. SurLok Assembly

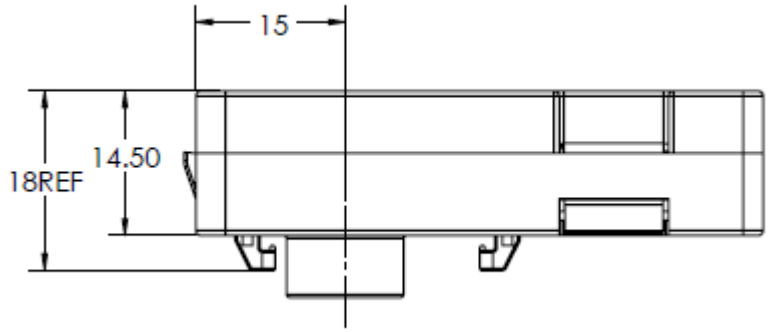
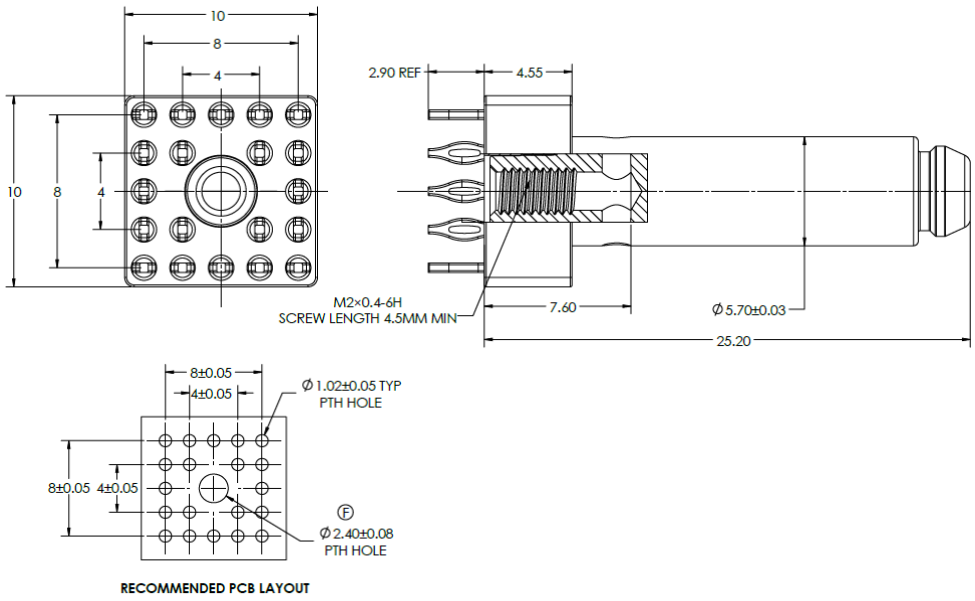
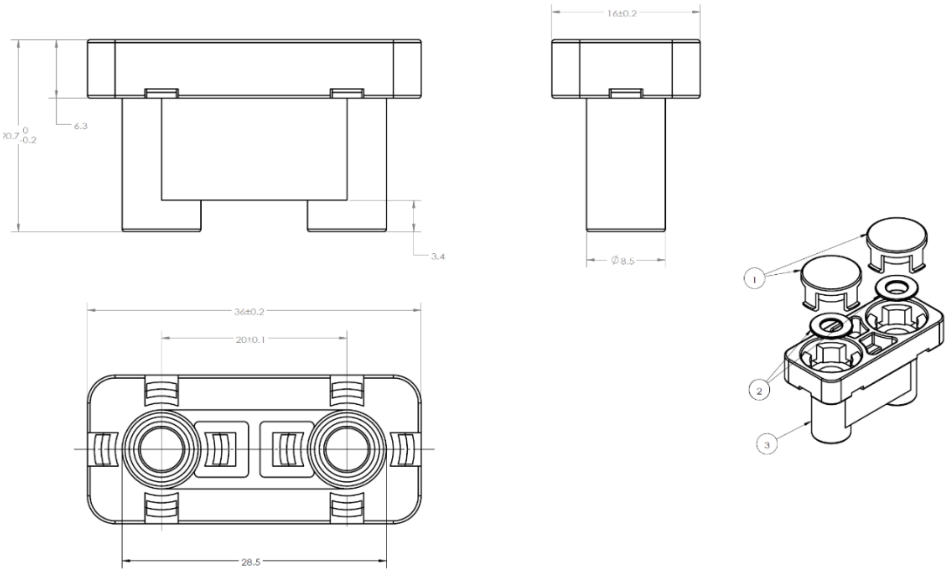


Figure 12. RadSok Pin – C10-779583-000



The RadSok pin section is made of copper alloy and plated with 3.81 µm silver. See the *HGX Platform Design Guide* (DG-10333-001) for the recommended SurLok mating assembly. If the RadSok connector is not used for input power, recommends leaving the provided RadSok pin safety cap on.

Figure 13. RadSok Pin Safety Cap – C10-753825-000



10. Rear Side Power, I/O, Expansion Board and Midplane Subsystems

10.1 PCI Express Interface

The PCIe interface between the CPU and SXM5 modules is a required interface on the HGX baseboard. The information provided in this specification refers to what is on the baseboard. For guidance on how to design a PCIe topology compatible with the HGX baseboard, see Chapter 4 in the *HGX Platform Design Guide* (DG-10333-001).

10.1.1 PCI Express Signals

The PCIe signals are connected out from the HGX baseboard through the ExaMAX connectors on the PCIe side. The signals are routed with the impedance stated in Table 4 and should be matched with external routing.

Table 4. Required PCIe Signals

Signal Name	I/O	Impedance	Description
GPU[x]_PEX_RX[y]*	I	85 Diff	PCIe input to the GPUs on baseboard. 'x' indicates the GPU number from [8:1] and 'y' indicates PCIe lane [15:0].
GPU[x]_PEX_TX[y]*	O	85 Diff	PCIe output from GPUs to the Root Complex. 'x' indicates the GPU number from [8:1] and 'y' indicates PCIe lane [15:0]
NVS_PEX_RX[x]*	I	85 Diff	PCIe input to PM41028 for NVLink Fabric. 'x' indicates the PCIe lane from [1:0].
NVS_PEX_TX[x]*	O	85 Diff	PCIe input to PM41028 for NVLink Fabric. 'x' indicates the PCIe lane from [1:0].
PEX_REFCLK[x]_IN*	I	85 Diff	PCIe reference clock inputs to the HGX baseboard. 'x' indicates the PCIe reference clock input [2:0]. Refer to the following section for more details.
PEX_RST[x]_N	I	-	PCIe reset signal inputs to the HGX baseboard. 'x' indicates the PCIe reset input [2:0]. Refer to the following section for more details.
PEX_STRAP[x]	Strap		PCIe strapping for reference clock and reset configuration on the HGX baseboard. 'x' indicates the PCIe strapping bit [1:0]. Refer to the following section for more details.

10.1.2 PCI Express Reference Clocks and Resets

The HGX baseboard supports up to three unique PCIe reference clock and reset pairs for the data plane. The quantity of PCIe reference clock and reset pairs on HGX is configurable by the PEX_STRAP[1:0] pins connected to the FPGA. The default PCIe reference clock and PCIe reset configuration on HGX is identical to the HGX A100 8-GPU baseboard. It has one reset for all devices and two duplicate copies of one reference clock per baseboard.

The HGX baseboard has three onboard PCIe clock buffers that take two or three external clock inputs depending on PEX_STRAP[1:0] configuration and provide clocks for SXM5 modules, PCIe Gen5 retimer, PCIe switch, and NVLink fabric.

Table 5. PEX_STRAP[1:0] Pinout

Signal	Connector	Pin
PEX_STRAP1	J4	A1
PEX_STRAP0	J4	A5

Table 6. PCIe Reset Inputs for HGX

PEX_STRAP[1:0]	PEX_RST			
	# of Resets	Reset Pin	Description	HGX Device Mapping
11*	1	J3.T8	PEX_RST0	One reset for all HGX devices. This is the same mapping used in HGX A100 8-GPU.
00	3	J3.T8	PEX_RST0	SXM5[3:0] + PCIe retimer[3:0]
		J3.A5	PEX_RST1	SXM5[7:4] + PCIe retimer[7:4]
		J3.A1	PEX_RST2	NVSwitch + PM41028

Note: FPGA has internal pull up resistors to set PEX_STRAP[1:0] = 11 when pins are left floating on ExaMAX connector.

Table 7. HGX PCIe RefCLK Inputs

PEX_STRAP[1:0]	PEX_REFCLK			
	# of RefCLKs	RefCLK Pins	Description	HGX Device Mapping
11*	1 (2 identical copies)	J3.O3/P3	PEX_REFCLK0_IN*	SXM5[3:0] + PCIe retimer[3:0]
		J3.N4/O4	PEX_REFCLK1_IN*	SXM5[7:4] + PCIe retimer [7:4]+ NVSwitch + PM41028
00	3	J3.O3/P3	PEX_REFCLK0_IN*	SXM5[3:0] + PCIe retimer[3:0]
		J3.N4/O4	PEX_REFCLK1_IN*	SXM5[7:4] + PCIe retimer[7:4]
		J3.O1/P1	PEX_REFCLK2_IN*	NVSwitch + PM41028

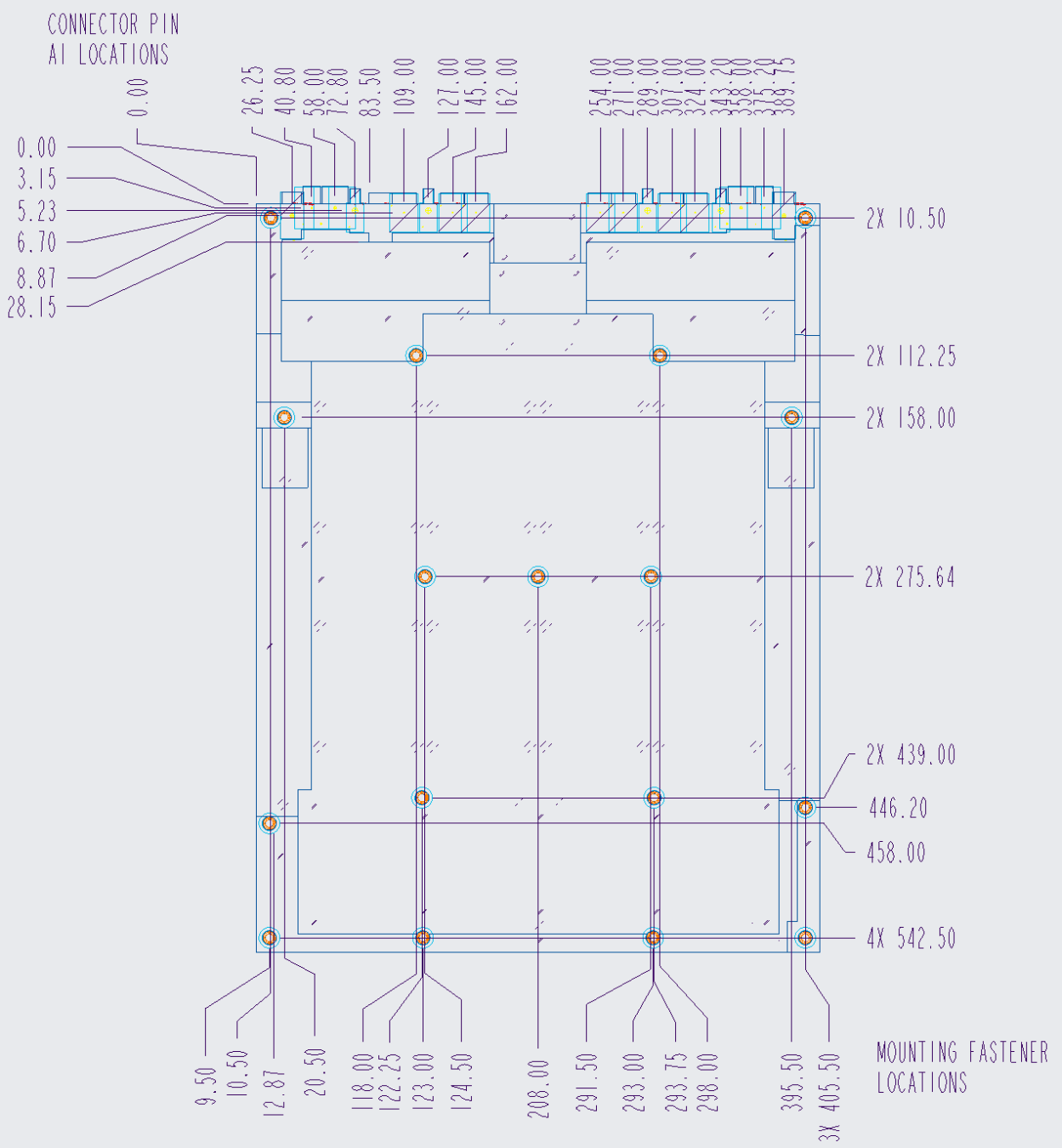
Note: FPGA has internal pull-up resistors to set PEX_STRAP[1:0] = 11 when pins are left floating on ExaMAX connector.

The HGX baseboard has separate reference clock and reset input to support the PCIe Gen2 x1 management interface.

11. Mechanical

The following figure illustrates connector and mounting hole locations.

Figure 14. Mounting Fastener and Connector A1 Locations



The HGX baseboard consists of 17 captive screws for mounting the baseboard, as shown in Figure 15. One tight hole and one slot are also labeled in Figure 15 to help alignment when mounting the baseboard in a chassis tray. For additional detail, refer to the 3D model.

Figure 15. Captive Screw, Slot, and Tight Hole for Mounting

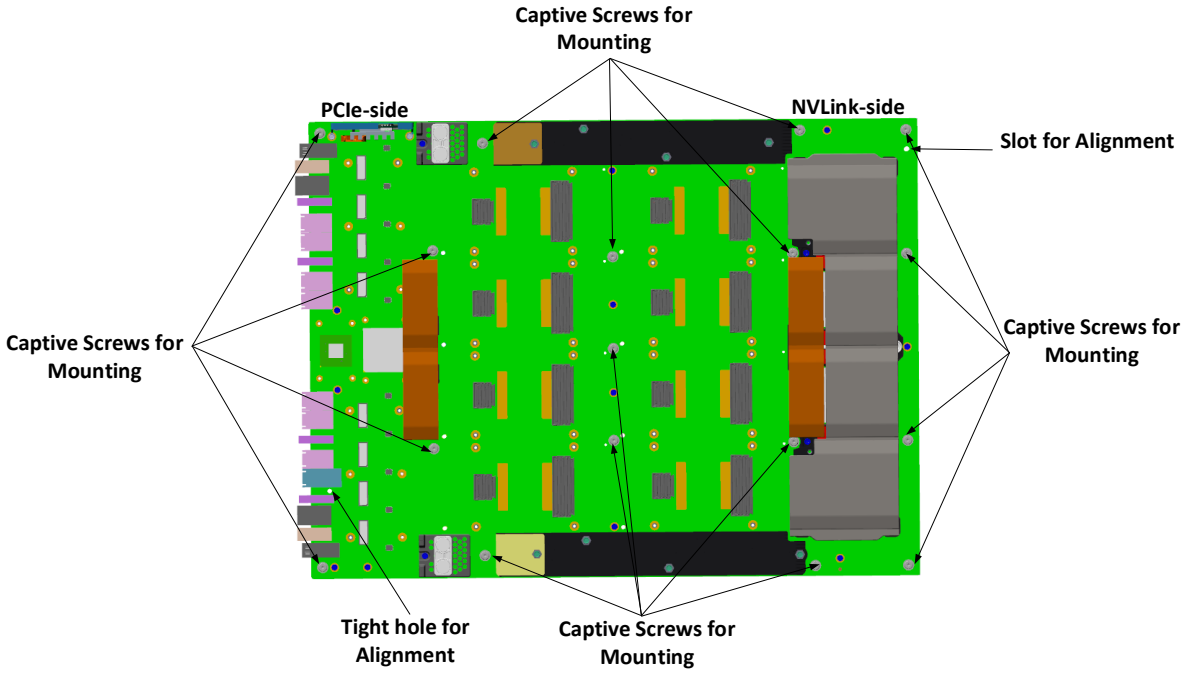


Table 8. HGX Baseboard Mechanical Specifications

Specification	Description
Baseboard dimensions (without connector)	553.0 mm × 416.0 mm × 153.2 mm
Baseboard dimensions (with connector)	565.4 mm × 416.0 mm × 153.2 mm
Partner label area	TBD mm × TBD mm
ExaMAX connector (10131762-301LF, 10137002-101LF)	200 insertion/removal cycles per EIA 364-09
AirMax connector (10028917-001LF, 10061289-001LF)	200 insertion/removal cycles per EIA 364-09
PwrMAX connector (10136689-003LF)	200 insertion/removal cycles per EIA 364-09
RadSok connector (C10-779583-000)	200 insertion/removal cycles per EIA 364-09

The following table lists all the screws present on the baseboard.

Table 9. Screw Specifications

Item	Count	Screw Head	Screw Thread	Torque (Nominal)	Torque Tolerance	Notes
Mounting Screws	17	Torx T15	M3	0.6 Nm (5.3 in-lbf)	+/-4%	Captive screws with baseboard (PN: 52-SM-99-125)
GPU Screws	32	Torx T15	M3	0.6 Nm (5.3 in-lbf)	+/-4%	Required for RMA. Across and diagonal pattern for insertion and removal. For insertion, full torque at first pass is acceptable. Recommend a second pass to verify all screws at correct torque specifications.

12. Onboard Power System

12.1 Power Specifications

The following tables summarize the electrical specifications for the HGX baseboard. The input voltage measured at the module connector should never exceed the voltage range defined in Table 10. Input power (54V_BUS_IN) can be provided either through PCIe side AirMax and PwrMAX connectors or RadSok pins. The recommended nominal voltage is 54.0 V. The composition of AC noise is shown in Figure 16.

Table 10. HGX Baseboard Input Voltage Specifications

Specifications	Signal	Value
Recommended Nominal Input Voltage (DC)[1]	54V_BUS_IN_1C, 54V_BUS_IN_2C	48.0 V to 54.0 V
Absolute Input Voltage Range (DC + AC)[1]		40.0 V to 59.5 V
Maximum AC Noise (pk-pk)[1,2,3]		5.5 V

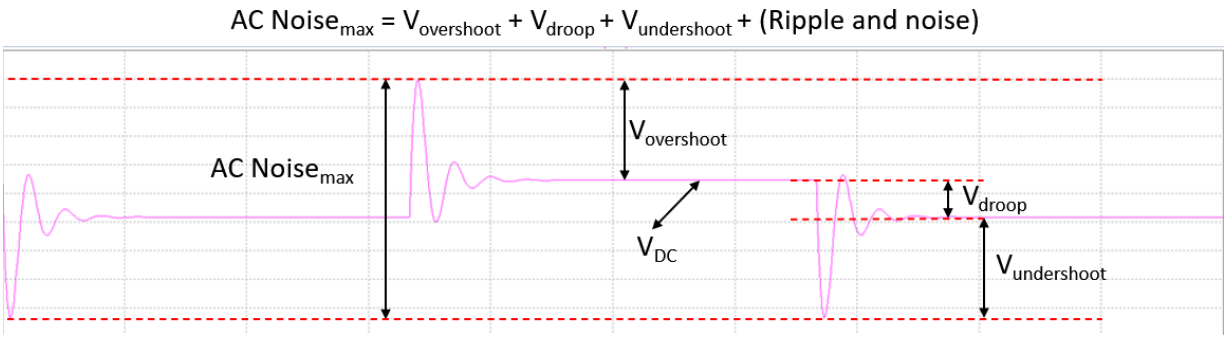
Notes:

[1]Specificatons are measured at the RadSok input power connector. Measurements shall be made differentially using an oscilloscope with 20 MHz bandwidth limit feature enabled.

[2]Maximum AC noise is measured under full system performance and should be simulated using the “HGX Baseboard Power SPICE Model” (NVOnline: 1073294).

[3]Maximum AC noise-absolute limits are inclusive of PSU ripple and noise, dynamic response, and voltage droop. Refer to the *54V Power Supply Specification Application Note* (NVOnline: 1029576) for reference PSU specifications.

Figure 16. Maximum AC Noise Composition



Note: Maximum AC noise composition waveform shown is meant for illustration purposes only and is not representative of an actual system waveform.

12.1.1 Input Voltage Rails

The DC voltage tolerances in Table 10 are specified by measurement at the input to the HGX baseboard power connector. The HGX baseboard can tolerate a larger AC+DC voltage swing on 54V_BUS_IN during transient loads. Peak currents are defined at the nominal voltages of 48.0 V and 54.0 V.

13. Environmental Regulations and Environmental Requirements

The following table details the environmental and reliability specifications.

Table 11. Board Environment and Reliability Specifications

Specification	Condition
Inlet temperature to baseboard (sea level)	5 °C to 40 °C
Operating ambient humidity	10% to 85%, non-condensing
Storage temperature	-40 °C to 65 °C
Storage humidity	10% to 90% relative humidity

14. Prescribed Materials

15. Hardware Management

System management is available through USB, I2C, and 3.3V tolerant GPIO signals. Refer to the pin map for locations.

16. References (recommended)

Appendix A - Checklist for IC Approval of This Specification (to Be Completed by Contributors of This Spec)

Complete all the checklist items in the table with links to the section where it is described in this specification or an external document.

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes or No	Yes
Was it approved in the OCP Contribution Portal?	Yes or No	Yes
Is there a Suppliers that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes or No	List Supplier Names TBD
Will Suppliers have the product available for GENERAL AVAILABILITY within 120 days?	Yes or No	UBB2.0 will be a superset of this spec and product will come from the next gen OAI specs

Appendix B-__ <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist

(to be provided by each supplier seeking OCP recognition for a hardware product based on this specification)

Company:
Contact Info:

Product Name:
Product SKU#:
Link to Product Landing Page:

The following is needed for OCP hardware product recognition:

For OCP Inspired™

- All Suppliers must be a Silver, Gold or Platinum Member.
- Declare product is 100% compliant with specification
- Complete the OCP Inspired™ Product Recognition Checklist, which includes hardware management conformance checks and security profile.

For OCP Accepted™

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Complete the OCP Accepted™ Product Recognition Checklist, which includes hardware management conformance checks, security profile and open system firmware conformance checks.
- Submit a design package meeting OCP Hardware Design Guideline Contribution Checklist (if not already submitted by the contributor). If already submitted, declare the product is 100% compliant with the design package.
- Submit a firmware package including a firmware image, build scripts, documentation, test results and a tool that verifies modifications
- Submit the BMC source code, if applicable to product type

Complete the OCP Inspired™ Product Recognition Submission Checklist or OCP Accepted™ Product Recognition Checklist and the following table.

Item	Details	Links
Which product recognition?	OCP Accepted™ or OCP Inspired™	Provide link for the appropriate Product Checklist
If OCP Accepted™, who provided the Design Package?		Link to OCP Contribution Database
Where can a potential adopter purchase the product?		Link to OCP Marketplace

Appendix C - Contribution Process FAQs

As a contributor to a hardware specification, here are some questions that often come up.

Q1. What type of hardware specification am I contributing to OCP? Is it any of the following?
   a. base specification for a de-facto standard (new standard with no hardware product on the horizon)
   b. base specification for an intended physical <hardware product type> (product may be coming but within the next 1-2 years)
   c. modification of an existing specification (state which existing spec is being modified)
      i. either a complete revision update or
      ii. a minor version update
   d. design spec (based on an existing base specification) with more refined design details (product coming in 12-15months)
   e. a detailed specification for a <hardware product type> for a very specific product being available in 3-6months of approval of this specification
   f. If none of the above, contact OCP Staff for better direction.

Q2. How do I know if what I am contributing will be accepted by OCP?
   a. Before contributing any specifications, please contact either OCP Staff (Archna Haylock or Michael Schill) or the Project Lead for the project that best represents your contribution. For example, if you are contributing a server specification, contact one of the server project leads. You can see all the projects here.
   b. They will help you with your contribution and help you navigate the process.

Q3. What is the contribution process for my hardware specification?
   a. Follow the flow for your specification type here.
   b. This flow is subject to change so check with the OCP Staff for more information or any questions.

Q4.What if my specification is not developed yet and I want to collaborate with other companies?
   a. Contact either OCP Staff (Archna Haylock or Michael Schill) or the project lead for the project that best represents your contribution.
   b. They will help you find other collaborators and help you with the contribution process for a multi-party contribution.

Q5.I have a question on the Contribution License Agreement.
   a. Contact OCP Staff and we can help you with questions.

Q6.Do I need to have a product to contribute a specification?
   a. See Q1. Some types of specifications do not require an immediate product. Some do. Work with the OCP Staff on better direction on your specification type.