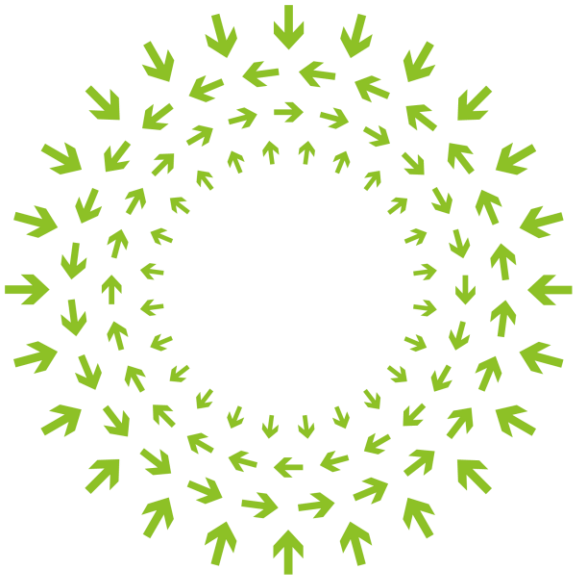


OPEN Compute Project

V2 Power Shelf Specification 6600W @ 12.6V DC (2+1) Redundant

Author: Pierluigi Sarti, Technical Lead, Open Rack and Power, Facebook

Author: Samir Kala, Power Engineer, Facebook

Author, Zoh Ebrahimzadeh, Power Engineer, Facebook (RS485 Communication Manual and Digital section)

Scope

This specification defines the requirement for a 6600W stand-alone V2 Power Shelf, single-voltage 12.6Vdc output, powered from three-phase AC line, hosting three 3300W hot-swappable single-phase power modules. This product is used for IT Systems, for both online and back-up power functions. At the system level, this device will work in conjunction with battery back-up unit (BBU) modules (installed in the same shelf) for power back-up functionality.

Table of Contents

1 Overview

This document lists the requirements for the 6600W V2 Power Shelf (2 + 1) redundant, and the 3300W V2 Power Module. The V2 Power Shelf is three open units (OU) high. It hosts three power modules with the outputs connected in parallel. Each module is an AC/DC power converter rated at 3300W @ 12.6Vdc of nominal output power. It is hot swappable, has accurate current sharing and is self-cooled.

NOTE: 1 OU = 48mm.

Each power module has its own BBU that powers the bulk voltage during an AC outage. In addition to the main 3300W DC/DC step-down converter, the power module also contains:

- A 3600W DC/DC step-up converter which is on during backup and supplies power to the bulk voltage via the BBU,
- A 270W DC/DC 52.5Vdc step-down converter for charging the BBU,
- A 300W DC/DC 54Vdc output auxiliary converter to supply power to the IT switches.

This V2 Power Shelf is fully compatible with OCP Open Rack V2. Throughout this specification, the V2 Power Shelf is referred to as Power Shelf, the power module as module, and the populated shelf (power station) as station (3 modules installed).

Please refer to the V2 BBU Spec document for detailed information on the BBU.

2 License

TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

3 Compliance Requirements

The power supply shall comply with the following standards as a stand-alone unit. It must be certified and labeled accordingly.

3.1 Safety Certifications, Applicable Documents

- UL60950-1 (Standard for Safety of IT Equipment)
- CAN/CSA-C22.2 No. 60950-1-03 (Standard for Safety of IT Equipment)
- EN60950-1:2006 / IEC60950-1 (Standard for Safety of IT Equipment)
- cCSAus Certification is allowed in place of the equivalent UL certification
- CE Mark, CB Report & Certificate
- EU Low Voltage Directive, EMC Directive
- UL94V-0 material flammability rating, with an Oxygen index of at least 28%

3.2 Immunity Standards, EMC

- EN61000 / IEC61000 applicable standards for Emissions & Immunity Requirements
    - EN61000-3-2 (AC Mains Harmonic Current Emissions)
    - EN61000-3-3 (Voltage Flicker)
    - EN61000-4-2, Level 4 (ESD)
    - EN61000-4-3 (Radiated Immunity, 3V/m)
    - EN61000-4-4, Level 4 (EFT/Burst)
    - EN61000-4-5 (AC Mains Surge Immunity, see levels at § 5.9)
    - EN61000-4-6 (Conducted Radio Frequency Immunity, 3V/m)
    - EN61000-4-8 (Power Frequency Magnetic Fields)
    - EN61000-4-9 (Pulse Magnetic Field)
    - EN61000-4-11 (AC Mains Voltage Dips and Sags, Fluctuations)
- The power supply shall always resume operations after any fatal power line disturbance (PLD).
- Output voltage must never dip if backup voltage is applied to the PSU.
- Backup functionality is not affected by substantial repetitive dips and sags
    - GR-1089-CORE, Issue 4 PLD
    - BS EN 55024:1998, CISPR 24:1997 - Information Technology Equipment

Note: When the power supply unit (PSU) is installed at the system level, the equipment under test powered by the PSU shall continue to operate without interruptions and/or resets during the above tests under EN61000-4-(*).

3.3 Industrial Immunity Standards

- EN61000 standards for Industrial Immunity

- EN61000-6-1 (Immunity / Light Industry)
- EN61000-6-2 (Immunity / Industry)

This section of BS EN61000 applies to electrical and electronic apparatus intended for use in industrial environments. This standard applies to an apparatus that people intend to connect to a power network supplied from a high or medium voltage transformer that is

- Dedicated to the supply of an installation feeding industrial plants,
- Intended to operate in (or in proximity to) industrial locations.

This standard also applies to any apparatus that is battery operated and that people intend to use in industrial locations. The environments encompassed by this standard are industrial (both indoor and outdoor) and include locations where heavy inductive or capacitive loads are frequently switched, and have/or are in the presence of high currents and associated magnetic fields.

3.4 EMI Compliance & Limits

The AC main tests are conducted as a stand-alone unit, at 200Vac and 277Vac, and at full load (3300W + 300W + 270W):

- FCC Part 15, EN55022, CISPR 22: Conducted Emission, Class B (peak-reading)
- FCC Part 15, EN55022, CISPR 22: Radiated Emission, Class B
- The DC back-up converter shall meet Class A limits (no dB margin) with at 35Vdc input and full load

System Level: the power supply shall comply with Class A limits for both conducted and radiated emissions, with at least a 3 dB margin for both AC & DC inputs / converters.

3.5 Environmental Engineering Standards

- ETS 300 019-2-3, Class 3.2 (Operation)
- ETS 300 019-2-2, Class 2.3 (Transportation)
- ETS 300 019-2-1, Class 1.2 (Storage)

3.6 AC Mains Leakage Current

The leakage current per module shall be in compliance with applicable EN/IEC standards, and shall not exceed 7mA RMS at 60 Hz and 277Vac.

3.7 Restriction of Hazardous Substances (RoHS) Compliance

The power supply is RoHS-6 compliant (BOM & Manufacturing Process)

4 AC Input Requirements (Main AC to DC converter)

4.1 AC Input Voltage, AC Loss Detection Time

- The AC input voltage range is 180Vac to 305Vac RMS (auto ranging).

- The nominal AC input voltage is 277Vac RMS (200-277Vac).
- The power module shall comply with the specification up to 290Vac RMS correspondent to 277Vac (+5%).
- All the components used in the AC input section shall have a voltage rating compatible with 300Vac operations, up to 305Vac (277Vac + 10%). The power module must withstand continuous exposure to 305Vac RMS input with no damage, while at this voltage level is not expected to meet the power factor and total harmonic distortion (THD) requirements.
- Input voltages higher than 310Vac RMS may damage the PSU.
- The front-end circuitry must be able to detect any AC loss within 5ms after the actual occurrence, at any AC input level and at any phase of the input AC sinusoidal waveform (from 1° to 360°, wherever the AC loss event occurs).

4.2 Input AC/DC PSU Connector, Fuse, EMI Filter

Each power module must have an AC input fuse. The fuse is used for safety and extreme protection in case of catastrophic failures. The AC input connector is polarized. The fuse is connected in series to the hot conductor (line). The fuse rating is a 25A. It is a slow-blow type fuse. It must never blow during inrush or during any AC input current transients. The fuse shall be a safety-approved component with rating of at least 400Vac RMS (it may be a larger size due to the high AC voltage involved). At the system level, the PSU is powered by a custom AC PDU connected directly to the tap box without any extra protection. a proper I2T coordination shall be verified when the PSU is powered by the PDU (e.g. in the event that the AC input stage of the power supply fails – a short circuit, for example – then the power supply input AC fuse should blow while the breaker in the tap box should not trip).

- The EMI filter should not make use of more than two cells with low series DC resistance. The design should preferably use bulky choke components in order to reduce the copper losses and maximize efficiency. Smart design of common mode (CM) windings that are able to include some differential (DM) impedance (DM leakage) is welcomed because it helps electromagnetic interference (EMI) suppression. As already mentioned, all the components used in the AC input power section must be rated at least 305Vac root mean square (RMS) (e.g. AC input connector, protection fuse, X2 EMI caps, surge protection devices, bleeder resistors, etc.).

4.3 Primary Metal-oxide Semiconductor (MOS) and BULK Caps

- The bulk capacitor shall be rated at 500Vac 105°C and shall have long-life components. For each bulk capacitor, a single component rated at 500Vac is required (compared to the potential alternative of having two capacitors rated at 250Vac each and connected in series). Voltage stress, especially when the positive peak of the low frequency ripple voltage at the worst conditions is included, is not negligible, while at the same time a reliable design, fully working up to 290Vac RMS input, must be guaranteed (305Vac RMS peak). See Section 5.5 for more information.
- The 500Vac rating gives enough margin for a nominal bulk voltage that shall likely be in the 430Vdc ~ 440Vdc range.

- All of the high voltage power metal–oxide–semiconductor field-effect transistor (MOSFET)s used in the primary side must be rated 600Vac (minimum), 650Vac is preferred.

NOTE: If a bridgeless type power factor correction (PFC) is chosen, it must have at least two high voltage silicon diodes (in series) from the AC grid. This is for safety. If the bulk voltage is energized by the Li-ion BBU during an AC outage, the bulk voltage (supplied by the BBU) must not be able to discharge to the AC input line after a single failure (e.g. in the event where one of the two diodes fail and create a short circuit).

4.4 AC Inrush Current, Preferred Topology

The inrush current shall never exceed 30A peak at cold start, V_{in} = 290Vac RMS, T_{amb} = +35°C. Perform the inrush test by synchronizing the positive (or negative) peak (90°) of the sinusoidal AC input voltage using a very low impedance AC source. Perform repetitive inrush sequences to validate the test. Make sure they are set at least one minute apart. The spikes of current due to the charging of the X2 EMI capacitors should not be considered. In realistic operations, the inrush sequence will have to repeat after any AC interruptions of sufficient duration to cause the PSU to enter back-up status, including dips and sags (i.e. multiple input dropouts). The PFC start-up current peak shall be lower compared to the AC inrush current peak. The AC inrush current during the main 12.6Vdc soft start up shall be less than 16A RMS at 230Vac. The inrush MOSFET or relay will be driven by the microprocessor. The inrush-limiting component (power resistor or NTC) will be placed in series to the input AC power train, before the input bridge rectifier (this topology will provide the best performance vs. the surge test). The relay must open and the sequence should be repeated every time the bulk voltage (BULK_OK) falls below the bulk-low threshold.

4.5 AC Hold-up Time

The hold-up time is defined for the power module standalone without the DC input applied from the BBU. The minimum hold-up time shall be 20ms at full load (3300W main load + 300W auxiliary). A longer hold-up time may be required to reduce the peak start-up current from the BBU during back-up mode, if too high. Hold-up time is measured at full load, with no extra capacitance added to the output at T = 25°C, sinusoidal 200Vac RMS, 50Hz, from when AC is lost at the 0° or the worst-case angle crossing, to when the output voltage falls below 12.0Vdc.

4.5.1 AC Drop Test

The power supply, including the auxiliary, shall remain in regulation when the AC input voltage drops to zero volts for half of a cycle at 50Hz, happening exactly at a 0° or the worst-case angle crossing, 200Vac, under a full load (3300W main converter + 300W auxiliary). Here are a few reasons why an extended hold-up time (and a reasonable size of the bulk capacitor) is needed:

- It can indirectly reduce the peak start-up current of the DC backup converter.
- It guarantees smooth back-up operations under all conditions (as mentioned above).
- It reduces the peak-peak low frequency ripple to limit the voltage stress on the bulk capacitors (they are used in PFC scheme working at up to 290Vac continuous).

- The target of this PSU is to obtain a very high efficiency during normal operation, so the nominal duty cycle of the DC-DC converter used after the AC-DC PFC state should be the highest possible – this implies the usage of bigger bulk capacitors for the same hold-up time.

4.6 AC Input Under Voltage Protection

The PSU shuts down during input AC under voltage and is able to automatically restart when a minimum voltage level is reached. The PSU shall turn on when the AC input voltage range is between 175 to 180Vac. The PSU shall turn off at 10 to 12.5V below the turn on voltage. No hiccups or on/off oscillations are allowed under any conditions.

The PSU shall withstand, without being damaged, multiple input dropouts under all conditions, and:

- It shall resume normal operations when no back-up voltage is connected to the PSU.
- It shall resume normal operations after multiple successful back-up sequences, when back-up voltage is connected to the PSU, without any output voltage dips.
- Input over voltage protection is not required.

4.7 Internal Bias Supply

The internal DC bias supply (auxiliary supply) is only intended for housekeeping functions (no externally available standby voltage is required). The implementation of an independent bias supply is the preferred solution and it should work from a minimum of 100Vac RMS (correspondent to 140Vdc on the bulk capacitors). The bias supply should be implemented with a high-efficiency scheme; the vendor shall propose the best solution.

A back bias connection that takes the 12.6Vdc from the common output busbar in the shelf, which is powered by the other PSUs, is needed. In the event of a PSU failure, the back bias will provide power to the failed PSU's secondary logic, communication circuits, and LEDs. The 12.6Vdc back bias shall not power any PSUs under normal condition (only when the PSU has a failure and cannot produce its own 12.6Vdc). Also, a thermal fuse – positive thermal coefficient (PTC) – and negative thermal coefficient (NTC) should be used as an internal short-circuit protection in conjunction with a resistor to limit the inrush current.

An analog circuitry shall be added to bring the REDUNDANCY_LOST_L signal low in parallel with the communication circuit in order to guarantee that we always know if a PSU has failed. We would like to compare the voltage before the Or-ing MOSFET transistor and compare it to around an 11V threshold. If the voltage reaches this threshold then it should be also used to drive the REDUNDANCY_LOST_L signal as well. Please use a comparator, half a volt of hysteresis to clear the signal, and around a one- second persistence delay. The voltage comparison threshold should set to 11V.

4.8 Power Factor & THD

The PSU shall comply with EN61000-3-2 (see Section 4.2) up to 290Vac RMS input. See further requirements in Section 6.9.3.

4.9 Input AC Surge

See Section 4.2 (EN61000-4-5) with the following limits:

- 2kV DM (Differential Mode is line to neutral)
- 4kV CM (Common Mode is line/neutral to ground)

The power supply must be protected against surge events. It must not be damaged if a surge occurs. The PSU shall continue to operate without functional failures or hiccups during surge tests, per the above limits. Surge pulses should not affect the output voltage under any conditions. Surge events shall not be able to reset the system when the PSU is used in the final application at system level. At the system level, the PSU is powered by a custom AC PDU, which is directly connected to the tap box without any other protection or surge circuitry. Under these conditions, the PSU is expected to pass 2kV DM and 4kV CM (to be tested and verified), stand alone and at shelf level with (one, two or three) power modules installed in the shelf.

4.9.1 Primary Protection

The primary section (PFC, DC-DC) shall include an over-power protection rating higher than the PSU power rating. A small not-replaceable fuse may (or may not) be added in series to the bulk voltage feeding the following DC-DC converter. The vendor is free to define the best topology for safe operations.

4.9.2 Isolation Requirements

- The PSU will support safety-reinforced isolation between the high voltage AC primary section and any secondary section (3000Vac RMS of isolation).
- Isolation between the high voltage AC primary section and the chassis GND is 1500Vac RMS.
- Both positive and negative 12.6Vdc output terminations are floating with respect to the chassis GND, with a galvanic isolation of 100Vdc.
- The step-down, step-up, and auxiliary converters should also have the same reinforced isolation between the primary and secondary side (3000Vac). As a reminder, the negative returns of the auxiliary output and the 270W charger are electrically connected to the 12.6Vdc negative return.

4.9.3 High Potential and Ground Continuity

- The PSU shall be tested 100% in production for both high potential (with the applicable limits for the AC leakage current) and ground continuity (per the applicable standard). Stamps shall be applied to the chassis proving that both tests passed in production.
- The vendor must verify the ground bond test at the design stage, and it must comply with applicable IEC standards.

Tech tips:

- A ground continuity test must be performed on the GND pin of a line cord-terminated product (normally the center pin of an IEC320 socket). This test verifies that the safety ground is present in the system. However, it does not test the ability of the safety ground to withstand a faulty current.

- Perform the ground bond test in a similar fashion to verify that a product's safety ground can adequately handle any fault currents due to insulation failure. The test duration may vary (it last up to 120 seconds).

5 DC Output Requirements (Main Converter)

5.1 Output Voltage and Power

The PSU is a single voltage power converter:

- The nominal output voltage is set to 12.6Vdc at 10% loading. See Section 12 for the output voltage set point under share functionality (calibration will happen on the production line, during the final test). The surface mount technology (SMT) dividing resistors for output voltage reading shall be rated 0.1%.
- The output voltage regulation is ± 1% under any conditions. (input voltage, load, temperature, aging, etc.)
- The PSU shall withstand a no-load condition for an indefinite time, without damage and with (or without) the max allowed capacitive load connected to the output terminals.
- The nominal continuous output power is 3300W on the 12.6Vdc output.
- An output ORing metal-oxide semiconductor (MOS) is installed inside the PSU for current share, parallel operations, and hot-swap conditions.

5.2 Output Over Current Protection

- The over current threshold is set to 280A (+5%, -2%) for the 12.6Vdc output. The protection mode during a short circuit or an overload is constant current mode. Output voltage must recover automatically when the over-current condition (or short circuit) is less than two seconds. The PSU is sized (thermally and electrically) to indefinitely stand a short circuit, without damage, under any conditions.
- An over-current condition lasting more than two seconds (± 0.2s) latches off the 12.6Vdc output only and an AC recycle (≥ 1 second) is needed to resume operations. The two-second timer resets every time the PSU exits the over current condition even for a very short time (>20ms typical).
- The PSU is able to start under overload or short circuit conditions.

5.3 Output Over Voltage Protection

- The over voltage threshold is set to 15Vdc.
- The protection mode is the latch off type, so an AC input recycle (≥ 1 seconds) is needed when attempting to resume operations after an over-voltage event.
- The over-voltage circuitry is independent, it includes a separate voltage reference device, and it does not make use of the microprocessor to implement the function. The microprocessor may be notified in case of an over-voltage event, if necessary.

5.4 Over Temperature Protection (OTP)

The PSU is protected against overheating to prevent damage or degradation. The PSU may overheat for many reasons, including (but not only) internal failing conditions, environmental factors, or because of improper use, such

as air obstruction. All the PSUs' outputs shut down for over temperature protection (OTP) and will not be able to automatically (needs an AC recycle) resume operations once the temperature falls below 10°C of the OTP limit (with some hysteresis). The OTP limit should be set as high as possible to maintain safe operation. No components shall be over stressed at the temperature shutdown threshold level. There should be enough temperature sensors within the PSU to guarantee safe operation. An OTP alarm for one PSU shall not force any of the other two PSUs in the shelf to also turn off. Each PSU shall act independently for OTP.

For example:

- Primary thermal switch (e.g., normally closed for primary heat sink OT protection).
- Secondary thermal switch (e.g., normally closed for secondary heat sink OT protection).
- The BBU step-up, step-down BBU charger, and the auxiliary 54Vdc DC-DC converters should stay within their temperature range
- All of the thermal sensors should be routed to the microprocessor (primary sensors are opto- isolated). The vendor is free to propose the best solution for OTP.

The air inlet temperature sensor is needed to implement the fan's automatic speed control. An extra outlet temperature sensor is also added. The microprocessor oversees all PSU functionalities.

5.5 Capacitive Load

The maximum capacitive load at system level is 200,000µF. A single PSU is able to start up properly and, more importantly, is unconditionally stable when such a capacitance (or a lesser capacitance) is connected to the output (in parallel to any resistive loads, or just the capacitance).

5.6 Transient Response

The amplitude of the positive and negative output voltage peaks during a transient-load test shall be within ±2.5% of the nominal output voltage (±300mV), with a response time of <5ms, under the following conditions:

- Electronic load set in constant current mode.
- Current step-cycles from 50% to 100% of the PSU max load, at 50Hz dynamic load frequency, 50% duty cycle, and 1A/µs slew rate (min).
- Transient requirements shall be met with (or without) the max-allowed capacitive load connected to the output terminations.

5.7 Output Voltage Ripple and Noise

The max ripple and noise shall never exceed 200mV peak to peak of the 12.6Vdc output at 20Mhz bandwidth.

No external capacitive load is connected to the output terminals during this test. Measurements are performed at the output connector at PCB level, with the board installed in the chassis, a safety ground connected through an AC power cord, 180Vac input and full load. A digital oscilloscope is used for this measurement, with acquisition set to

peak detect mode. The probe will be used without its cap to minimize the length of the return connection in order to achieve a reliable R&N reading (negative return is directly connected to the metal body of the probe). A small 1uF X7R 0805 SMT ceramic capacitor may be connected locally to the probe tip during this measurement. As a design note, the 12.6Vdc output stage may include a small CM choke added very near the output connector, for CM noise suppression.

5.8 Output Turn-on/Turn-off

Under any conditions of dissipative load, capacitive load, temperature, with backup voltage connected to the PSU, or without:

- The PSU shall turn on when a valid AC input is provided. Stand-by switch and/or on/off signal are not required. The design of the PFC & DC-DC circuitry, soft starts, etc., will be such that the total time, from when a valid AC input is applied to when the DC output voltage reaches regulation, is a maximum of two seconds under any conditions with Vin > 200Vac RMS.
- The 12.6Vdc rise time should be less than 20ms from 10% to 90% of the 12.6V output at any loading.
- The PSU is able to start properly during no-load conditions or overload conditions.
- For any loads (from no-load to max-load), the output voltage will rise monotonically from 0Vdc to 12.6Vdc, without overshoot or ringing, at any turn on following the application of AC input voltage, and anytime when the PSU resumes functionalities after an automatic protection condition (including parallel operations). The output voltage will fall monotonically from 12.6Vdc to 0Vdc, without undershoot or ringing, at any AC loss, and at any turn off caused by an automatic protection condition (including parallel operations). The backup voltage is not applied for this test, but the same performances are expected regardless of whether the input is supplied by AC or DC power (via the BBU).
- Output voltage shall never reverse polarity at the turn off (all conditions and converters).
- The PSU shall include a soft-start that promptly resets at any input AC loss of > 20ms, or after any automatic protection conditions.
- See Section 7.1 for PSU behavior on AC loss, when a valid backup voltage is connected to the PSU.

5.8.1 Power Supply Turn-On Sequence

5.8.1.1 Normal Conditions

After a valid AC input is applied, the internal bias supply turns on and the entire circuitry is powered. There is always a turn-on-sequence requirement when the AC input voltage is applied to the power supply, regardless of whether the DC backup BBU is installed. The three normal scenarios are described:

1. Every time AC is applied to the shelf including after the 90-second backup timeout: the shelf (3 PSU units) turns on synchronously.

- **Sequence**: After AC voltage is applied, the internal bias supply starts, the µP boots and keeps the PFC off as well as the step-up, step-down and auxiliary 54Vdc converter. Then the µP closes the inrush relay and turns on all of the converters. The step-down BBU charger is turned on two seconds after the main 12.6V is within regulation. (LED = solid green or solid yellow).

2. AC restore during a backup lasting less than eight seconds: the shelf turns on with a random delay between zero and two seconds.
    - **Sequence**: After AC voltage restores, the µP keeps the PFC converter OFF. Then the µP generates a random number *n* between 0 and 2,000 turning ON the PFC with a delay equal to *n* milliseconds (LED = solid green). The shelf then sends a SYNC signal, which is dictated by the random number generated by the PSU module in slot #1. If the power module in slot #1 has failed (or is not even installed) at the time of AC restore during backup, the remaining two units start up at the end of Interval D (with no random time) synchronously, when AC becomes available and is present for at least one second.
3. AC restore during a backup lasting greater than eight seconds: the shelf turns ON with a random delay between zero and eight seconds.
    - **Sequence**: After AC voltage restores, the µP keeps the PFC converter OFF. Then the µP generates a random number *n* between 0 and 2,000 and turns ON the PFC converter with a delay equal to *n*x4 milliseconds (LED = solid green). The shelf then sends a SYNC signal. The random number generated by the PSU module in SLOT #1 dictates the signal. If the power module in SLOT #1 has failed (or is not even installed) at the time of AC restore during backup, the remaining two units start up at the end of Interval D (with no random time) synchronously, when AC becomes available and is present for at least one second.

- The random numbers above shall be dynamically generated immediately after each AC recycle. They must not be generated one time and then stored in the EEPROM for future use.
- The PFC starts once the AC voltage is available, then the DC main 12.6Vdc converter and the 54V auxiliary converters powered by the bulk voltage are turned on together (The vendor may add a small delay if needed) followed by the step down charger to charge the BBU (if needed) after two seconds (maximum five-second delay window).
- If the BBU in slot #1 fails before or during an outage so that the PSU in the master slot is not delivering 12V during back up, when AC power returns, the PSU in slot #1 shall still dictate the random timing and shall bring the shelf back synchronously out of back up. The PSU with the failed BBU during back up shall not turn on immediately when AC returns.
    - If the PSU in slot #1 is running an SoH test, and an AC power outage happens, then when AC power returns, the PSU in the other slots shall turn on synchronously without the random timing. [Same scenario as if the PSU in slot#1 has failed]
- If a BBU in slot #2 or slot #3 fails before or during an AC power outage, then when AC power returns the PSU in the master slot #1 shall still dictate the random timing and shall bring the shelf back synchronously out of back up. The PSU with the failed BBU during back up shall not turn on immediately when AC power returns.

5.8.1.2 Dead-Bus Event

As described above, when AC power gets restored during a backup phase after an AC power outage, the PSU will randomly restart in the two- or eight-second window. If the DC input (battery voltage) fails during that two- or eight-second window, in which the AC mains is actually available, or within the one-second filter window that is always present before the PFC starts delivering power (see Backup Sequence, interval D), then the PFC would provide power to the main converter instantly with reasonable output voltage (it shall not dip below 11.3Vdc during the Dead-Bus test at worst conditions and at full load). The backup sequence chart shows the exact point where to test the Dead-Bus event (see the complete backup sequence in the figures below). The PSU's 12.6Vdc output must stay within regulation and meet the DEAD-BUS requirement when battery voltage Vin(DC) ≥ 35 Vdc. The battery pack sends a stop_discharge signal when the voltage level falls below 33.8Vdc (2.6V per cell), to protect the batteries from excessive discharge. If the back-up step-up converter in the power supply is still running when the battery voltage approaches the 33.8Vdc (2.6V per cell) cut off voltage, this means that an entire system shut down event is imminent (the standby emergency power generator did not turn ON, AC power is not available). Achievable Dead-Bus performance may be discussed during the design phase. Dead-Bus performances get worse at low temperature.

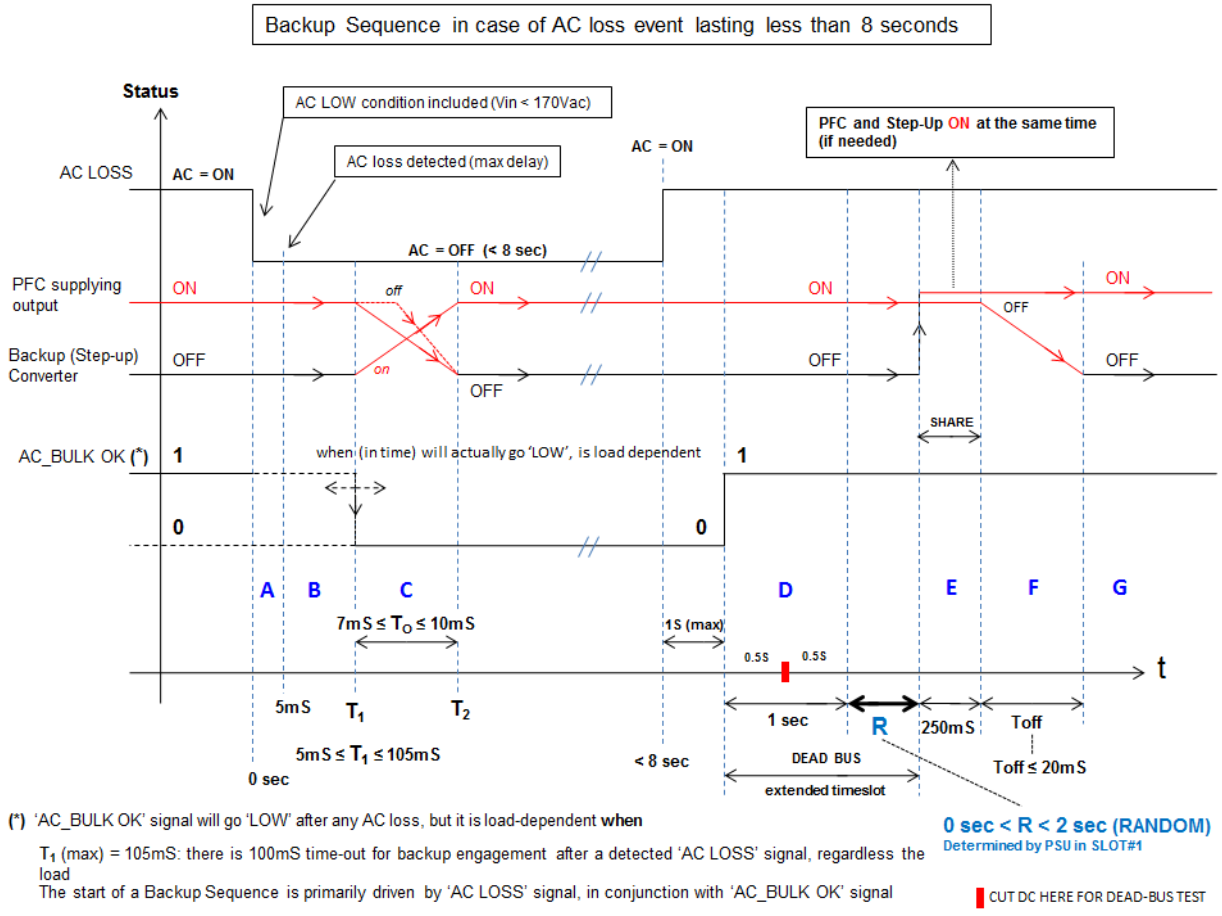


Figure 1: AC outage lasting less than 8 seconds transition sequence diagram

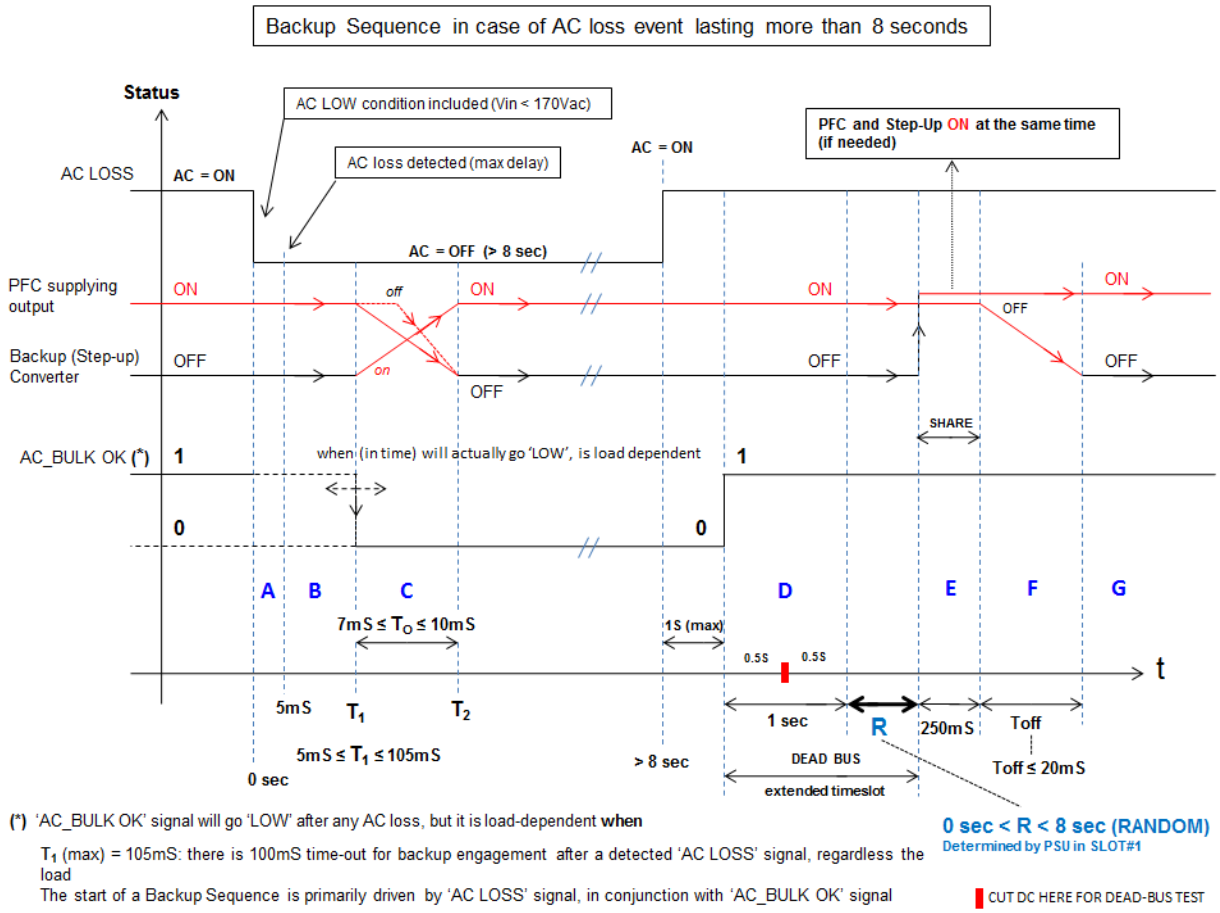


Figure 2: AC outage lasting more than 8 seconds transition sequence diagram

5.9 Microprocessor Control, Digital Bus, R&D Support

It is expected that all the logic and housekeeping function (over voltage excluded) are implemented and driven by a low-power-consumption microprocessor and low-power-consumption circuitry. This microprocessor oversees all PSU functionality. If a digital signal processor (DSP) is used to drive the pulse width modulations (PWMs), then it may (or may not) include the microprocessor functions.

The power module is entirely a digital power converter with the exception of an integrated circuit (IC) analog controller admitted only for the 300W auxiliary DC-DC (it provides 54Vdc output) and for the 270W DC-DC battery charger.

The three power modules are digitally interconnected with a separate internal digital bus (it does not go out from the shelf) for data exchange between the units, including: battery test priority, synchronized start-up and shut-down, randomization of the AC restart at shelf level, etc. If a PSUs internal (ex. CAN bus) communication fails and cannot receive message from any of the other PSUs then its fail LED should turn red, but it should still allow the main 12.6Vdc to provide power. The step-up, charger and auxiliary IT switch converter shall turn off.

NOTE: The shelf shall still be able to start up if all PSUs and BBUs are not installed.

The random restart command is assigned to the power module installed in SLOT #1: it enables the entire shelf to transition back to AC power for itself and to the two remaining modules, for a shelf synchronized random restart after the AC power restores (after outages). See Section 6.8.1 for more information.

A further independent RS-485 isolated digital bus is generated by each PSU, paralleled inside the shelf, and is connected to the RJ45 socket in the shelf's rear panel. This digital bus is used solely for data reporting. Such reports include power module failure, output/input power, and boot-loader function. It is possible to update the firmware of all the DSPs and/or microprocessors used inside the power module via the boot-loader through the shelf's RJ45 socket. Please refer to the V2 Communication specification for more information. The PSU shall blink green at 2Hz when the PSU is being updated via the boot-loader.

Input power reporting can be calculated accurately by measuring the output power and then dividing by the efficiency curve stored inside the EEPROM. There are two curves stored, at 5% load steps, from 10% load for the sole (PFC + main DC-DC) power converter:

- 230Vac
- 277Vac

The power module is able to determine when 230Vac range voltage or 277vac range voltage is applied to the PFC, and then select the proper efficiency curve to use for the back calculation of input AC power (in Watts).

The power module is able to shut-down the PFC by itself, to simulate an AC power outage for battery test purposes, every time the BBU that is connected to that power module requests a battery test. This periodic test is used as a status of health (SoH) check for the battery pack installed inside the BBU module. The BBU module also provides an end of life (EOL) signal when it needs to be replaced. When the battery test sequence is over (it can last minutes), the PFC resumes working using the AC voltage from the grid. It should not have any interruptions on the 12.6Vdc bus during the process. For the digital signals present during a battery test case, please refer to Section 7.2.4.

Several signals interconnect each power module with its own BBU, but not a digital bus. The PSUs can talk to each other via a digital bus, but the BBUs cannot. The BBU can only communicate via high/low signals to the PSU above it.

The firmware of the microprocessor and/or DSP must be upgradeable anytime during the life of the power supply. The design (and the vendor) must support the following:

- The PSU chassis cover shall have a small opening. The opening must provide access to a programming connector placed at the top of the logic board (it could be edge-pads on the PCB itself, or an equivalent location) that enables the user to upgrade the firmware easily without the need to uninstall the PSU cover. This opening is only required for EVT and DVT samples.

- A small indentation on the metal chassis or a mark will provide reference for ‘pin 1’ of the programming connector. The programming connector is only needed for EVT/DVT samples debugging (for PVT/MP the firmware can be upgraded by the shelf’s boot loader).
- The vendor will supply the programmer needed to upload firmware, interconnection cables, functional software, and the set of instructions needed to upgrade the firmware at remote sites.
- The vendor will provide, free of charge, a reasonable amount of connectors, wire harnesses, and other items needed to qualify and use in their testing set up.
- The vendor will be able to provide quick new releases of the firmware code during development in order to speed-up fixes of any PSU issues, phase in improvements, system level bug fixes; including late findings or fine tuning.
- The vendor’s R&D team is expected to be proactive and quick in resolving any hardware or firmware issues that may arise during the development, including potential technical malfunctions at the system level, or system integration issues.

All signals return should be decoupled from the power return using three 1Ω high pulse current resistors in parallel (SMT1206) and 1uF capacitors on either side or the resistors between the negative return plane of the logic board and the negative return of the main 3300W DC/DC converter.

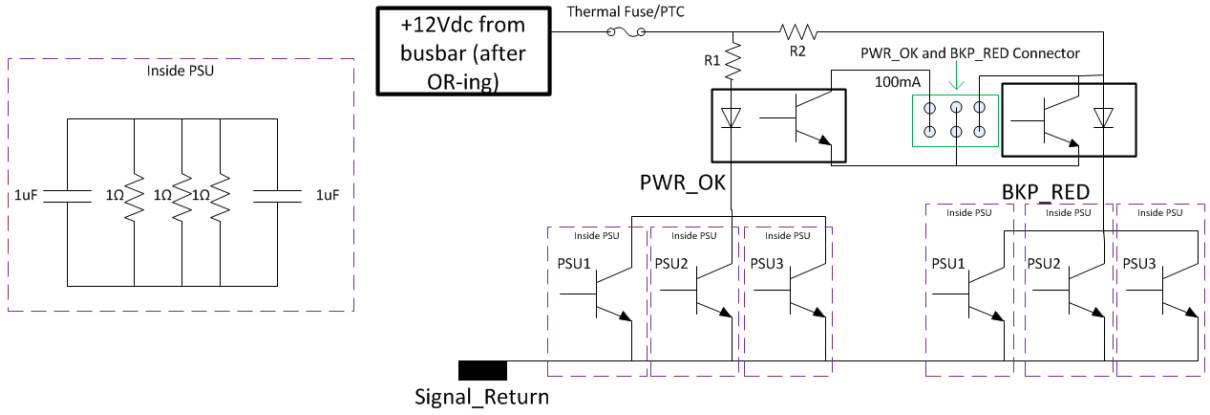


Figure 3: Signal ground decoupling schematic in the PSU

The figure below shows the signal ground decoupling in the BBU (left) connected to the DSP of the PSU (right)

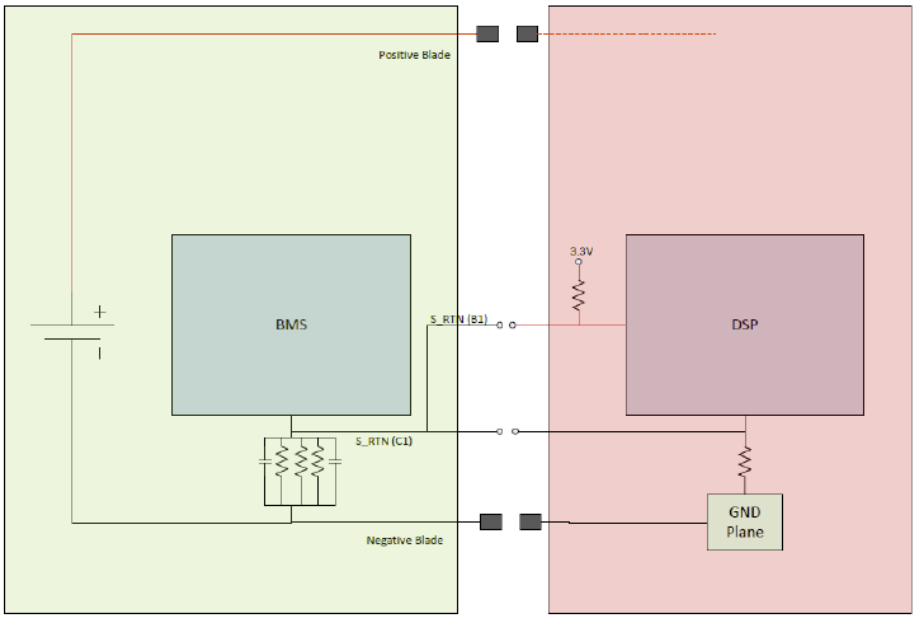


Figure 4: Signal ground decoupling between BBU and PSU

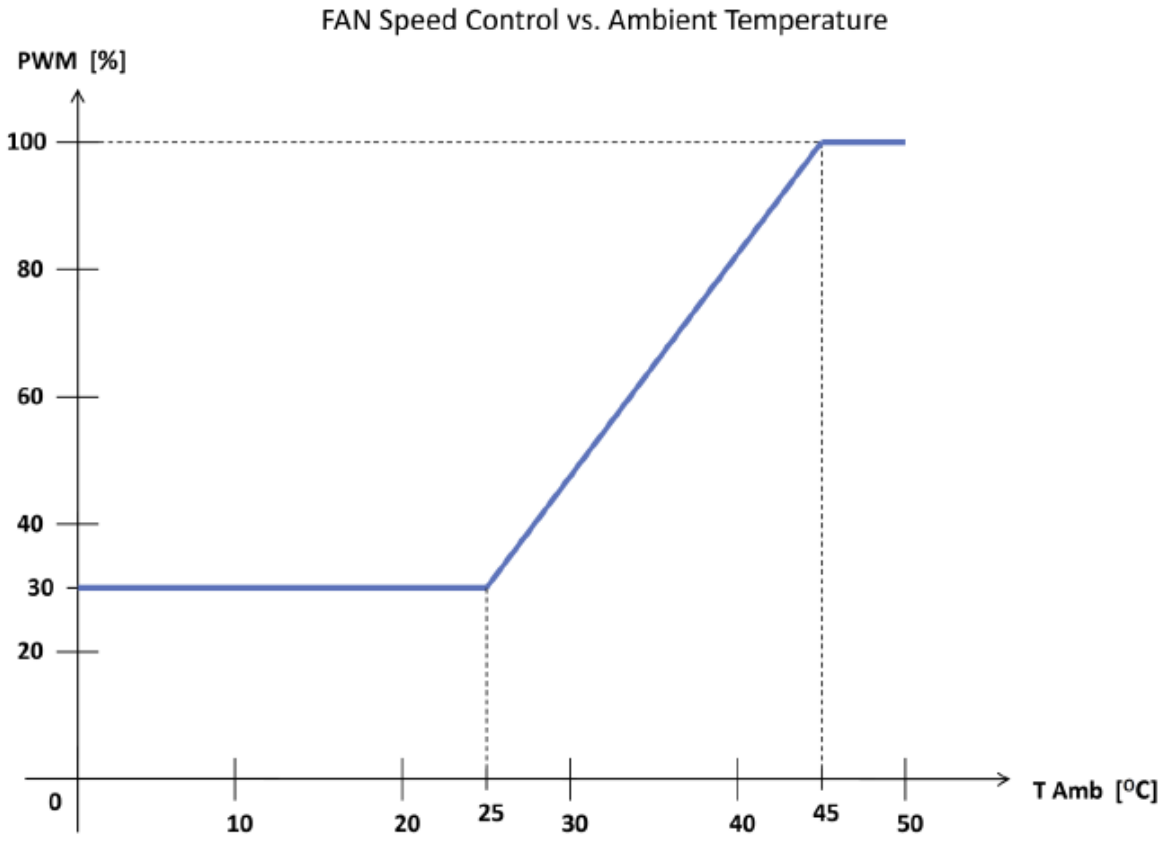
Please refer to the V2 BBU, Battery Backup Module 3600W specification for the BBU signal and operation information.

5.9.1 Internal Cooling Fan, External Fan Guard

- The PSU must be self-cooled using either one or two internal power efficient fans pulling cold air inside the PSU (airflow is from front to back). The fan guard can either be built into the chassis sheet metal or into an external chrome plated fan guard. The PSU front is the side facing the cold aisle where the LEDs are installed. The fan mechanical mounting method should limit the propagation of vibrations to the PSU caused by the rotating fan. A soft rubber sheet material between the fan housing and the sheet metal chassis may be used for this purpose. The fan shall be installed using four flat head screws, properly located in order to avoid any potential air short circuits.
  - The fan is a 12Vdc component. It's dimensions are 60mm × 60 × 25mm. the vendor can choose mm, min cubic feet per minute (CFM) (TBD), four-wire type, and double-ball-bearing type only. A reference fan is TBD.
  - The fan speed is driven by the microprocessor (the automatic speed control is based on the intake air temperature). The fan is used for PSU cooling purposes and for some extra airflow. The minimum duty cycle of the PWM signal applied to the fan shall be at least 30% (base value), no matter the PSU cooling conditions. Base speed is required because the PSU needs to provide some minimum degree of CFM air to the system. See the fan PWM [%] vs. Ambient Temperature graph below. The minimum fan speed (or PWM) should be not less than 30%. Higher than 30% PWM base value may be agreed upon, based on the actual thermal performances of the power supply.

- The air temperature sensor for the automatic speed control must be located near the air inlet panel. The fan shall not directly change speed with the output current level.
- The fan speed algorithm of the PSU should be computed while the PSUs are installed in the shelf and using the PSU that is inserted in the 'worst case' slot, which is the PSU with the highest back pressure (highest air flow impedance).
- At the PSU turns on, the fan should start up at full speed and then settle down to its self-regulated speed value.
- The fan is a 12Vdc component and so it can be powered directly by the output voltage. A C-L-C filter may be used to power the fan in order to reduce injection of spikes to the main 12.6Vdc supply output. In fact, the brushless fan generates significant amounts of ripple and noise to its DC supply. To endure the low frequency ripple current with extra margin (low ESR and long life component), the electrolytic capacitor connected directly in parallel to the fan must be selected.
    - **Layout Rule**: At board level, the fan's positive and negative terminals are connected directly to the main output capacitors before any further PSU output filters, using independent dedicated copper traces routed away from any noise-sensitive circuitry (e.g. the main feedback loop circuitry, etc.).
- The microprocessor monitors the fan speed using the TACH signal and will shut down the PSU in the following cases:
    - Fan failure
    - Fan blockage
    - Inconsistent fan speed readings.
- Under any fan failure conditions, the FAIL (red) LED will turn on and the PSU will shut down (see Section 18).
- If two fans are used and one fan fails, the event should be treated as a fan failure and the PSU should turn off.
- The fan will always run at full speed during a back-up phase or battery test.
- The fan must stay on at full speed for at least 1 minute after a backup lasting more than 30 seconds or a battery test before going back to its normal self-regulated speed.
- The fan L10 life shall be at least 50 000 hours at a 45°C inlet air temperature and full speed (to be verified with the fan vendor)

Note: The battery back up can last up to five minutes at 2,200W constant power or the backup converter can provide constant power for 3,300W for up to 90 seconds. During battery back up the fan should run at full speed.



5.9.2 Power Supply Efficiency (AC Main Converter)

The PSU cost and actual measured efficiency (pilot samples) can be used for internal TCO evaluation and analysis.

Efficiency shall meet Titanium efficiency limits at 277Vac (the 52.5V battery charger and the 54Vdc AUX output converters are completely disabled [inputs are not connected during efficiency measurements]. All fans are powered externally and all voltages measurements at PCB).

The Titanium efficiency limits are as follows:

- 90% at 10% of the load
- 94% at 20% of the load
- 96% at 50% of the load
- 91% at 100% of the load

Further efficiency target requirement:

- Efficiency > 95% between 30% load to 90% load at 277Vac input

Measurements are performed as follows:

- Input AC power voltage of 277Vac RMS (50Hz or 60Hz)
- A power analyzer with reading accuracy better than 0.1% will be used for the measurements
- A precise low distortion AC power source supplies the input voltage during the measurement
- The PSU board is correctly installed in the chassis, with the cover and with the safety chassis GND connected through the AC power connector.
- AC- and DC-power input voltages are measured directly at the respective PCB pads.
- Fans should be powered externally.
- The output 12.6Vdc measurement shall be made at the output of the busbar blades of the PSU at PCB level.
- The ambient temperature should be around 25°C.
- The measurement load step shall be an increment of 5%. Take measurements after 30 minutes under initial 75% load, over five samples (they all need to pass).

NOTE: The PFC may include interleaved topology with phase management in order to maximize the efficiency at light load (phase shedding).

5.9.3 Power Quality

THE power factor and iTHD (total harmonic distortion of the AC input current, with order of the harmonics up to and including 40) at 200-300Vac shall be:

- PF > 0.95 (>10% of max load)
- iTHD < 10% (>10% of max load)

The vendor is encouraged to propose solutions exceeding the above limits if they make cost sense for a 3,300W power supply. Efficiency is the first priority.

Measurements are performed from the same test set up as described in Section 6.9.2.

5.9.4 Stability

- The power supply shall be unconditionally stable, under any conditions or combinations of resistive and capacitive loading, constant power loading, temperature, aging, etc. Feedback loop control (analog or digital) shall never cause the E/A to enter a non-linear status during extreme transients.
- The Bode plot will show a phase margin better than 45 degrees at worst conditions (or 60 degrees at nominal conditions), and the dynamic step-load plots (see Section 6.6) will show no ringing. Rather, they will show a smooth recovery shape similar to a second order system with a damping factor $\sigma > 0.7$.
- The stability criteria is met with and without the maximum allowed capacitive load.
- The stability margin should not be excessive. Exaggerated reductions of the line frequency ripple or slow transient response time are not desired.

6 Battery Backup Section (Back-up Converter)

The power supply is able to provide short term backup power in case of an AC power outage. To enable this function, an independent isolated DC-DC power converter capable of 3,600W+300W, and an independent isolated 270W step down DC-DC power converter will be included within the PSU to provide power during backup and charging of the Li-ion batteries. The target is to provide seamless backup performance and enable smooth operations under any conditions, such as transients of AC power input, so as to be equivalent at system level to an online UPS.

6.1 Summary for the Whole Back-up Section Requirements.

For the backup power converter, all the input and output requirements, performance, compliance requirements, etc., are equivalent to what was specified for the DC main converter, powered by the high voltage bulk. The output of the back-up converter will also power the high voltage bulk. Additionally, there is an auxiliary isolated 300W DC-DC power standalone converter, which is powered by the bulk voltage. It outputs 54Vdc to the IT switches.

6.2 Signal Definitions:

Below are some definitions of some shelf-level signals:

AC_LOSS: This is an internal signal reporting the status of the AC power input voltage. This signal is required to change status within 5mS after an AC power loss event, which may occur at any phase angle of the input AC power sinusoidal waveform (50Hz or 60Hz, 180Vac to 290Vac RMS).

BULK_OK: When the energy in the bulk capacitors of the power modules drops below a minimum threshold. This is an internal to the PSU signal reporting the status of health of the bulk voltage:

- AC_BULK OK = good (logic status ‘1’) if bulk voltage > 90% of its nominal value.
- AC_BULK = no good (logic status ‘0’) if bulk voltage < 85% of its nominal value.
- Hysteresis = 5%

POWER_FAIL_L: This is an active low open collector signal. It is normally high. This signal is sent low out of the shelf via pin 2 on the RJ45 connector every time the following condition occurs:

- At 45 seconds into backup mode if AC_OK is still not present (three phase AC outage), then send out the POWER_FAIL_L signal and then at 90 seconds shut down the power shelf for a timeout.

NOTE: The POWER_FAIL_L signal is not for a sudden failure, a sudden over current condition, or a lack of energy in the BBUs, which may cause the shelf to shut down. An SoH should not cause the POWER_FAIL_L to be asserted.

REDUNDANCY_LOST_L: This is an active low open collector signal. It is normally high. This signal is sent low out of the shelf via pin 3 on the RJ45 connector every time the following condition occurs:

- When the Power Shelf loses redundancy. This means that at least one power module in the shelf has failed (red LED on the PSU), a BBU in the shelf has failed, or the sleep/insert signal is high.
- The REDUNDANCY_LOST_L signal should also be asserted when the PSU is performing a bootload or when the BBU voltage is below 31.85Vdc.

NOTE: An AC power outage/backup or one BBU performing a battery test should not make the REDUNDANCY_LOST_L signal go low. The REDUNDANCY_LOST_L signal may go low if any of the above requirements are met while in AC power outage mode. For example, if a PSU fails during an AC power outage the REDUNDANCY_LOST_L signal should go low. The signal should also not assert when any BBUs in the shelf have the Stop_Discharge/Protection signal low.

The POWER_FAIL_L and REDUNDANCY_LOST_L signals will also be used to drive a simple 9Vdc 1A regulator driven by the external 12Vdc common bus (via thermal fuse, etc., for protection) and activated by the logic present in the shelf. The 9Vdc shall turn on (be driven high) and be present on the Molex Minifit connector when the POWER_FAIL_L and REDUNDANCY_LOST_L signals are asserted low, (discussed in Section 22.2.3) at the back of the power shelf within 500μs.

SYNC: There should be a few SYNC signals reserved to be used for synchronized PSU turn-on and turn-off. The vendor can add other shelf-level signals.

6.2.1 Shelf AC Turn On Sequence

Initial AC power turns on, regardless how many PSU and BBU modules are inserted.

1. The PSU checks to make sure that all PSUs inserted in the shelf have AC_OK as well as BULK_OK signal asserted high. If any of the PSUs AC_OK or BULK_OK signals are low, the PSU will make the AC_OK and BULK_OK shelf level signal low.
2. Once both shelf-level signal of AC_OK and BULK_OK signal are good, a SYNC signal is given to turn on the PSUs synchronously.
    - The 12.6V and 54Vaux turn on together, first (the vendor may add a delay if necessary), followed by the battery charger which will turn on with an initial two-second delay if the Charge_Enable signal is low from the BBU.

6.2.2 Shelf AC Turn Off Sequence

1. If AC power input is removed from the shelf, the PSU will enter the backup sequence and wait for AC power to return within 90 seconds.
    a. If AC power does not return within 45 seconds the PSUs will assert the POWER_FAIL_L signal low and at 90 seconds should turn off the PSUs synchronously.
2. If there aren't any BBU units installed in the shelf, the shelf shall synchronously shutdown the 12.6Vdc output monotonically when the AC input is disconnected from the shelf.

Please see Section 7.2 for more information of when the shelf shall always shut down synchronously and assert the POWER_FAIL_L signal.

NOTE: If AC power returns anytime before the 88th second, the 90-second timer shall be ignored. This guarantees that the shelf does not turn off due to the eight-second random window.

6.2.3 Backup Sequence

1. As long as the BBU is inserted and has not failed/sleep (INSERT and BBU_FAIL signals) the PSU module may power the bulk voltage from the Li-ion batteries via the step- up converter.
2. The PSU should request power from the BBUs when both the AC_LOSS signal is low (the AC input fell below the minimum threshold Vin < 170Vac RMS) and the AC BULK_OK signal is low (bulk voltage fell below the minimum threshold). The power modules can independently go into backup.
    - As per Section 5.1, any sinusoidal AC power loss must be detected within 5ms after the actual loss.
    - Backup Engagement Timeout: There is a 100ms timeout for backup engagement after a continuous detected AC loss, regardless of the status of AC BULK_OK. At high load the AC BULK_OK signal changes status a few milliseconds after the AC_LOSS does (it triggers the backup engagement). But the AC BULK_OK status is load-dependent and so it may not trigger before 100ms, while the backup sequence would engage for the 100ms timeout. The transition from AC power mode to DC power mode will last a maximum of 10ms, in which the two converters, PFC and backup step-up, will gracefully exchange the load. During the transition from the bulk voltage being powered from the AC line or from the BBU, output voltage dips and spikes must stay within ±2% of the output voltage as it is set to as full load conditions. The vendor is required to control the transition between power coming from the PFC and DC power step-up converter during transitions in to and out of the backup sequence. For example, the step-up converter could be set at 400Vdc and then be slowly brought to nominal bulk voltage. This is particularly useful to limit the BBU startup current.
3. In normal conditions when a valid AC voltage is present, the PFC delivers power to the bulk voltage and the step-up converter is kept off to enhance the overall PSU efficiency. However, it is ready to kick in at any AC power loss.
4. If during a backup phase the AC power comes back, the PFC will start powering the bulk voltage only after a continuous valid AC input voltage is present for at least one second. It will transition the load between the PFC and the step-up converter for 0.25 seconds. If AC_LOSS or BULK_OK signals toggle during the timing intervals above, the counters (one second or 0.25 seconds) will reset and start over. At the end of the 0.25-second portion, the DC backup step-up converter will phase out in <20ms, releasing the full load back to the PFC. The target is to generate a backup sequence mode that guarantees the highest rejection against input AC power disturbances/random dips. It also guarantees UPS-grade performance during AC power

outages. The vendor is encouraged to propose the best refined timings vs. the actual topology adopted for best performance.

5. The backup phase will last for no more than 90 seconds at full load (3,300W + 300W) at 33.8Vdc at 45°C.
    - Backup Phase Time Out: the power supply will shut down after a continuous 90 seconds of backup operations. This functionality shall be built in the logic of the power supply.
6. The fan(s) will run at full speed during the backup phase.
7. If there is not enough energy in the BBUs installed in the Power Shelf to reach 90 seconds, then a POWER_FAIL_L asserts at 45 seconds.
8. Dead-Bus sequence: See Section 6.8.1.

Design: The target of the design is to provide a seamless output voltage level no matter what happens to the AC input voltage if a valid BBU voltage is applied to the power module. The discontinuity of the AC power can be a simple AC outage, or a sudden dip, glitch, disturbance, etc. The vendor is encouraged to propose the best solution that meets or exceeds the specified requirements without sacrificing cost and performance.

6.2.4 Battery Test Sequence

The BBU will determine internally (with random logic) when the BBU needs to be tested. Please refer to the V2 BBU Spec for more information. The logic of how a BBU test should be implemented once the SoH signal is low appears below.

The PSU will turn off the step-up converter and stop using the BBU as a source of power once the SoH signal is high. At any time during the battery test, when the SoH signal is low, if the BBU gives the ‘stop_discharge’ or ‘fail’ signal the PSU shall stop using the BBU as a power source.

1) CHECK: Make sure all three PSUs and BBUs are installed and communication is available.
2) CHECK: Are any BBUs currently running a self test? This is determined via internal communication.
    - YES: Queue the test
    - No: Continue
3) CHECK: Are the shelf level AC_OK and BULK_OK signal valid (AC power is present to all three PSUs)?
    - YES: Continue
    - No: Queue the test
4) CHECK: Are there
    - Any failed PSUs or BBUs
    - Any BBUs displaying the following low signals:
        - Stop_Discharge
        - EoL
        - Protection
    - Any BBUs with a high Sleep or Inert signal,
    - Any PSUs in the shelf performing a FW update (boot loader)

- YES: Queue the test
- No: Continue

5) CHECK: Are there any BBUs being charged at the moment via the Charge_Enable signal or are there any BBU packs with a voltage less than 50.7Vdc?
    - YES: Queue the test
    - No: Continue
6) CHECK: Is the load greater than 500W for at least one minute (consecutively)?
    - YES: Continue (if load decreases during the test, continue. Once you perform a test you must commit to it)
    - No: Queue the test
7) START self test
    - IF another BBU fails or another PSU in that shelf fails
        i. THEN continue the test as normal
    - IF the shelf goes into backup mode
        i. THEN continue the test as normal
    - IF the BBU is physically removed
        i. THEN end the test. The BBU will consider this as a failed test and wait for the next scheduled test.
    - IF the PSU whose battery is being tested FAILS
        i. THEN ABORT test (BBU goes into sleep mode)
8) IF SoH re-asserts high, or if Fail or Stop_Discharge appears, then the PSU will stop discharging the BBU.
    - Determine if the test is valid:
        i. The BBU will determine the validity of the test data> If valid, it will begin its open circuit voltage (OCV) period and will determine if the BBU has reached EoL at the end of this period. During this period the BBU will not be recharged. The charge_enable signal will remain high.
            1. IF for any reason during this OCV period the battery asks to be charged (‘Charge_enable’ is low) this means that the test data was not useful and the BBU has aborted the test.
            2. IF an AC power outage occurs during this OCV period, the outage is always given priority and the PSU can use the BBU as a power source, until the stop_discharge signal is given. The BBU will abort its battery test.
    - Once that BBU has been fully recharged, the PSU will consider the test complete and will allow another BBU to be tested if it was in queue.
9) During a battery test the internal digital BUS informs the other power modules installed in the shelf that they cannot perform any battery tests until:
    - The current test completes

- The module performing the battery test recharges

If multiple BBUs are in queue at the same time, base the priority of the battery tests on the slot number (first Slot #1, then Slot #2, and finally Slot #3). For example, if the BBU in Slot #3 entered the queue, followed by the BBU in Slot #1, then the BBU in Slot#1 will perform its battery test first. If an SoH signal was low for a BBU prior to an AC outage (a PSU was in queue for any reason) then the PSU should go into battery backup. Once the outage is over, the PSU shall return to AC power. The BBU SoH signal will change from low to high, assuming a battery test was performed (the BBU will try to use the discharge data to figure out if the data is valid of not) and will ask to be checked again, via the SOH signal in 90 days.

Use the following flow chart as a high-level reference. Please follow the detailed checks mentioned above.

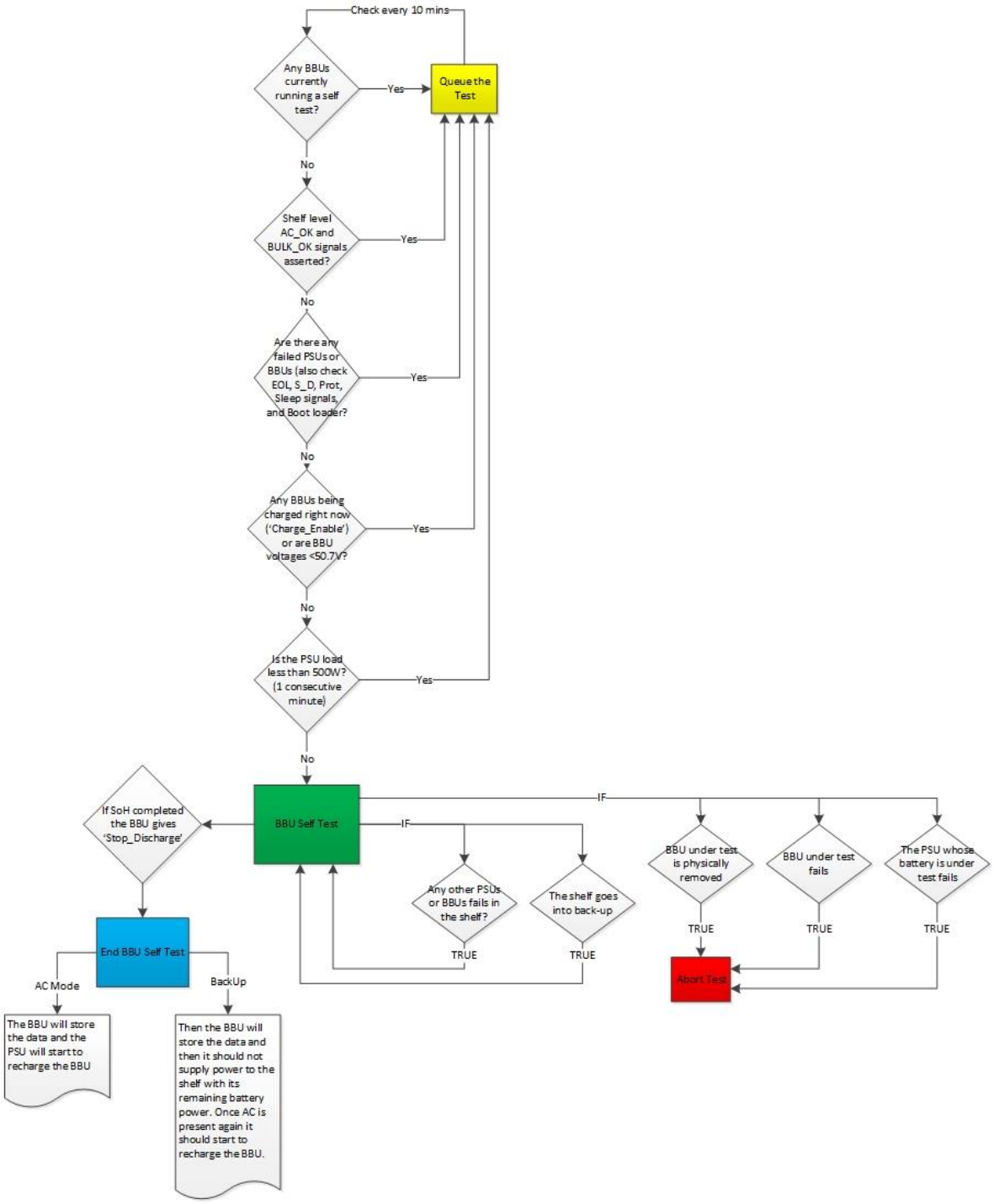


Figure 5:High level flow chart of battery test requirements

6.3 Charge Sequence

The step down charger will only turn on for two seconds after the charge_enable signal from the BBU becomes low. The BBU's internal charge MOSFETs will close as soon as the charge_enable signal becomes low. See Section 9.2 for more information regarding the output of the battery charger converter.

7 Battery Backup Unit

Please refer to the latest V2 BBU, Battery Backup Module 3,600W specification for this section. The V2 BBU specification will have details about the connector, signal and pins, logic, and operation of the BBU.

7.1 12Vdc from the PSU to the BBU

The PSU shall power the LEDs on the BBU via its 12Vdc output. Four pins will be reserved on the PSU FCI connector, two pins for +12Vdc and two pins for return. The 12Vdc should be taken before the output 12Vdc ORing MOSFET inside the PSU. This is to ensure that if the PSU fails the BBU will go into 'sleep mode' since the 12.6Vdc will not be present (Section 8.1 in the V2 BBU Spec). Note, that the layout for this connection needs to be done in such a way that the electrical noise generated from the BBU does not pollute the 12.6Vdc output of the main power module. A thermal fuse should be placed on the positive output of this connection.

7.2 BBU Latched Condition

For the BBU, a latched off signal indicates that one of the EoL or FAIL signals are asserted. Both signals are independently latched off. See Section 18. The method used to guarantee the latching-OFF condition of the EoL signal (and yellow LED) and of the FAIL signal (and red LED), may involve corresponding information being written by the BBU logic in the non-volatile memory EEPROM used in the BBU. Removing a BBU unit from the slot and re-installing it in the slot, with or without the presence of 12V at shelf level, cannot reset the latching-OFF condition.

7.3 BBU Signals

There are eight analog signals that the PSU will receive from the BBU:

- Fail
- Charge_Enable
- SoH
- EoL
- Stop_Discharge
- Sleep
- Protection
- Insert

All of these signals are normally high except the Sleep signal, which is normally low. When the Sleep signal is high, it indicates that the BBU has gone into a software sleep mode. The Insert pin is also normally low when inserted into

the shelf. The PSU shall implement a minimum of a one-second persistence delay before it takes the appropriate action. The PSU shall not try to use the BBU as an energy source if the Stop_Discharge signal goes low. If the Stop_Discharge signal is asserted low, the PSU shall ignore it for the first 15 seconds into the backup. If the signal is still low at 16 seconds, then the PSU shall stop discharging the BBU. After the initial 15 seconds of backup, the persistence delay of the Stop_Discharge signal shall change to one second. If the Fail signal is low, the PSU shall not discharge or charge the BBU. If the Sleep signal is high, the PSU shall not try to use the BBU (both these signal shall also have the one-second delay). If the SoH signal is low and all requirements are met in Section 7.2.4, then the PSU shall discharge the BBU until the SoH signal becomes high. The PSU shall only charge the BBU when the Charge_Enable signal goes low. In the odd case that the Charge_Enable signal goes low during a BBU discharge, the PSU shall ignore it and shall not charge the BBU while the step-up converter in the PSU is delivering power.

7.4 BBU Leakage Current

The leakage current at 52.5Vdc main output blades (including the sense lines) from the BBU input should be a maximum of 2mA regardless of the what state the power supply is in (ex. on, off, failed, etc.).

8 Backup Converter – Step Down

8.1 DC Input Requirements

The input of the 270W step-down DC-DC battery charger converter will be connected directly to the bulk voltage of the main converter. This converter will provide 52.5Vdc ± 0.2% for battery charging purposes. It is a stand-alone analog converter, powered by the bulk voltage, reinforced, isolated, and hot pluggable. This converter connects directly to the Li-Ion BBU battery module with an ORing diode/MOSFET, to avoid the spikes of current that occur when a charged BBU is installed in the shelf (it blocks the voltage from the BBU). It is activated/deactivated by the DSP/microprocessor. The leakage of the ORing diode/MOSFET shall be less than 0.5mA and two 100kΩ in parallel before the ORing shall be placed in parallel to the output capacitors so that the output capacitors do not become charged to 52.5Vdc and do not fake the converter into seeing a correct voltage if the step down converter does not work.

The feedback for the step down charger shall be taken at the three power blades of the negative connector of the battery and the five positive charge pins with a differential amplifier. The sense lines provided from the BBU will be also connected to a differential amplifier used for monitoring the battery voltage.

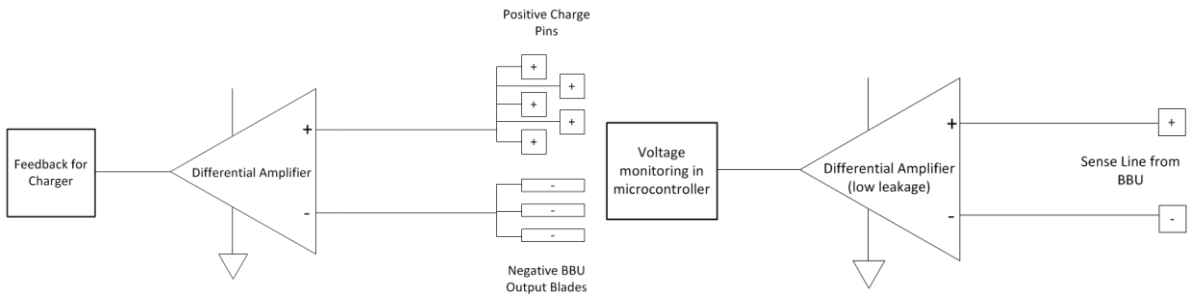


Figure 6: Block diagram of how differential amplifiers should be connected to the battery

8.2 DC Output Requirements

The 270W DC-DC power converter must be precise with a 0.1% voltage reference IC and 0.1% accurate resistors to guarantee that the output voltage is set to 52.5Vdc ± 0.2%. The output charging current, which is set by the DSP, may be set anywhere between 2A to 5A. The DSP should also be able to read the output voltage of the step-down converter to ensure it's providing a voltage within its range 52.5Vdc ± 0.2%. If the current given by the charger is less than 1A and if the voltage is not within the 52.5Vdc ± 2% range for two consecutive seconds (at the sense lines) then the Fail signal on the PSU shall be asserted. This signal will subsequently cause the BBU to go into sleep mode and the BBU will then open its charging MOSFETs. Also, if the BBU does not see any current for five consecutive minutes then the BBU will go into Sleep mode and assert a high Sleep signal. If the battery charger is on for more than five consecutive hours then it should be considered failed and assert the Fail LED. The failure of the battery charger should not latch off the main 12.6Vdc output. Additionally, there should be no overshoot. The output voltage must rise monotonically. The earliest the BBU charger turns on is two seconds (the maximum delay is five seconds) after the main 12.6V and 54V auxiliary outputs are turned on. During turn-off, the output voltage must fall monotonically. The converter should be cooled appropriately via the PSUs internal fan(s) so as to remain within its thermal limits. Over voltage protection (OVP) should be set at 54Vdc ± 0.5%. The converter should meet the same ripple and noise specification stated for the main converter in Section 6.7. The step-down converter shall always remain off during a battery test or during backup mode (the same signal used to tell the shelf to go into backup can be used to turn off the charger). The battery charger converter shall remain off if the BBU is not present and should only turn on once the BBU asks to be charged via the Charge_Enable signal. Please see Section 7.3 for the charging sequence diagram.

9 Backup Converter – Step Up

9.1 DC Input Requirements

The input to the step-up converter will range from 24-55Vdc, which will come directly from the Li-ion battery pack. The normal working range is 52.5-32Vdc. The converter should control input inrush (less than 20A), to avoid the spikes of current that occur when a charged BBU is installed in the shelf. The converter turns on during an AC outage or battery back-up test as defined in Section 6.8.1.

The BBU will provide an analog, active low signal to alert if an over-temperature condition has occurred (protection pin from BBU). This signal shall be one of two inputs to a logic OR circuit. The second signal will be generated if an under-voltage condition is seen on the BBU sense lines. A comparator should be placed after the amplification circuit of the BBU sense voltage lines and referred to a voltage which is equivalent to 2.154V × 13 per cell, 28Vdc. A small delay, 100ms, should be implemented (to ensure the signal is valid and not just noise) after the comparator before the signal is ORed with the active low signal (Protection) from the BBU. The step-up converter's MOSFET driver shall be enabled again, 15Vdc hysteresis, when the voltage at the sense lines increases back to 43Vdc (3.3V

per cell). The OR logic output of these two signals shall be used to immediately turn off the step up converters DSP's in case of any one of those two conditions are met. The under voltage protection of the step-up converter shall be set to 23Vdc seen at the converters input (not using the BBU sense wires).

9.2 DC Output Requirements

The converter should be larger than 3,300W to compensate for the efficiency loss through the main converter. The converter will be connected to the bulk voltage via a diode, to ensure that current cannot flow in the reverse direction. The total efficiency of the step-up + main converter with 300W on auxiliary and the PSU fans at full speed should be greater than 92.5% at 48Vdc when the load is greater than 30%. A further efficiency requirement of greater than 87% is required when the input voltage is 30Vdc.

This type of converter may be prone to large startup currents. This issue must be considered in the design. The maximum peak of the start-up output current during an AC outage, while the PSU is switching to backup mode, shall never exceed +20% of the related steady-state output current, tested at any input voltages ranging from 30Vdc to 55Vdc (with 2V step increments), and at all valid loads. The max peak of the startup current shall never last more than 5ms.

The turn on and turn off of the step-up converter shall always be monotonic without any over- or under-shoot. The converter should be cooled appropriately via the PSUs internal fan(s) so as to remain within its thermal limits during a battery test or back-up situation.

During a AC outage, if the voltage reading of the battery pack via the BBU sense line drops below 31.85Vdc ± 0.5% (2.45V per cell × 13 cells in series), then the power supply should stop the BBU discharge by turning off the step-up controller. There shall be a 15 second initial delay from the start of a backup if the PSU reads that the voltage is below 31.85Vdc ± 0.5%. After the initial 15 seconds of the backup, the persistence delay changes to one second. The step-up controller shall not turn back on until AC power returns. This is to prevent any further reduction in the BBU voltage during a backup. If the battery is conducting a battery test and 31.85Vdc ± 0.5% (2.45V per cell × 13 cells in series) is reached then this means that the BBU's Stop_Discharge signal did not work and that the step-up converter should shut down (with 15 seconds then one second persistence) and should not turn back on until there is an AC power outage, regardless of the SoH signal being low (active).

10 Auxiliary Converter

10.1 DC Input Requirements

The input of the 300W DC-DC power auxiliary converters will also be powered from the bulk voltage. It is a stand-alone analog converter (might be small resonant TV appliance style), powered by the bulk voltage, reinforced, isolated, hot pluggable and has ORing diode/MOSFET.

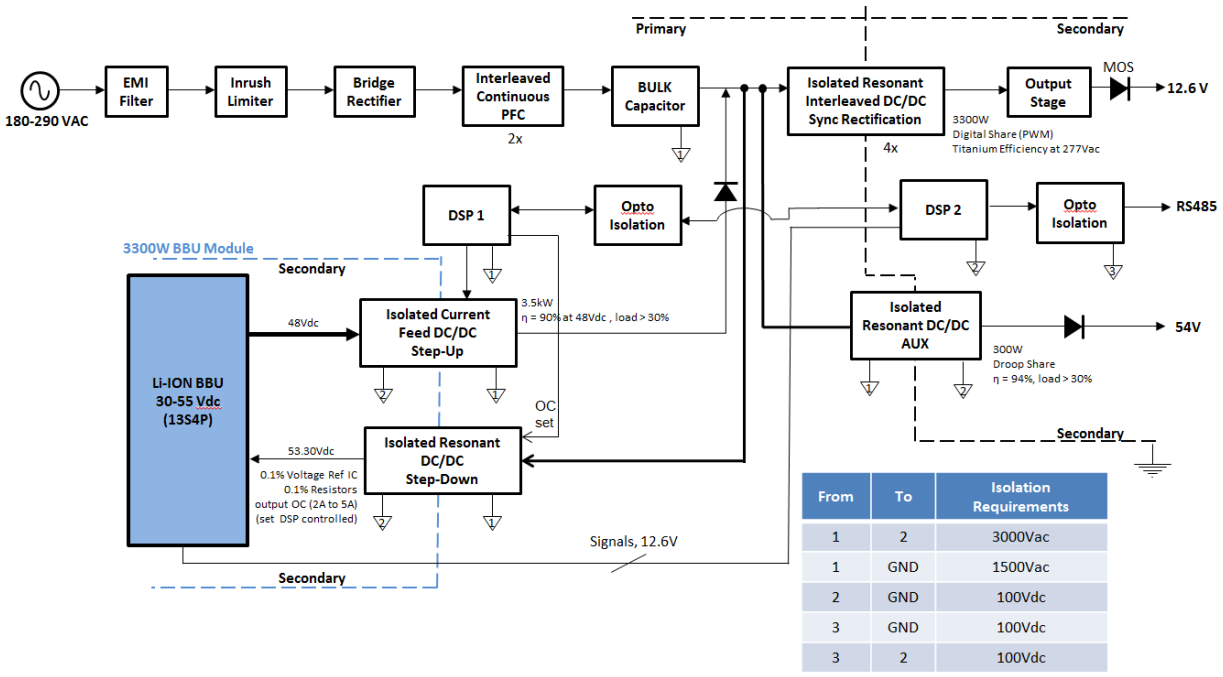
10.2 DC Output Requirements

The nominal output voltage is 54Vdc ±1% (at no load) and is used to power the top of rack switches and other IT equipment. A droop-share should be implemented, -1V droop from 0-100% of the load; the vendor may increase the droop if necessary. The over voltage protection should be set at 60Vdc. This output may power DC-DC power supplies with an input range of 40V to 72V. Turn on and turn off of the auxiliary converter shall always be monotonic without any over- or under-shoot. The converter should stay within its thermal limits at all times. The maximum capacitive load for the auxiliary output is 10,000µF. The PSU is able to start up properly and, more importantly, is unconditionally stable when such a capacitance (or lesser value) is connected to the output (in parallel to any resistive loads, or just the capacitance). The converter should meet the same transient, ripple, and noise specification stated for the main converter in Section 6.6. This output voltage should rise at the same time as the main 12.6Vdc output and continue to run during a back-up condition without any significant dips or spikes following an AC power outage. It should also have hot pluggable compatibility using an ORing MOSFET.

11 Current Share Functionalities

The power module shares the current with the remaining two modules in the shelf using a current share topology that shall allow excellent sharing at light load. The preferable implementation would be a through a PWM digital approach. A very precise analog approach is also allowed. The current share accuracy over the three modules should be within 5% of the modules theoretical output current, when the PSUs are at 20% of its rated load (each PSU at 660W loading). A further efficiency target is to have a 1% current sharing accuracy at 100% shelf loading when two power modules are installed in the shelf (each PSU is at full load, 3,300W). Different loading conditions on the battery charger or auxiliary charger should not affect the overall output sharing. A further droop-share is added on top of the regular current share, to help the current share functionality during transients: -0.15V from 10% load to 90% load.

12 Power Supply Block Diagram



From	To	Isolation Requirements
1	2	3000Vac
1	GND	1500Vac
2	GND	100Vdc
3	GND	100Vdc
3	2	100Vdc

Figure 7: High Level Power Supply Block Diagram

NOTE: This is a high-level block diagram and just a suggestion on the topology for the actual implementation. Isolation voltage levels are also listed.

13 Environmental Requirements

- Gaseous contamination: Severity level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: -5°C to +45°C
- PSU is able to start at -15°C of ambient temperature
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-ratings: 3,000m (10,000 feet)
- System level ambient temperature: target is < 27°C (for information only)
- The PSU main board shall be partially conformal coated (see Section 19.9.2)

13.1 Vibration & Shock

The PSU shall meet shock and vibration test per IEC78-2-(*) & IEC721-3-(*) standard & levels, with the specifications listed below. During operating vibration and shock tests, the PSU shall exhibit full compliance to the specification without any electrical discontinuities.

During the non-operating tests, no damages of any kind (included physical damages) should occur and they should not corrupt the functionalities of the PSU per the specification.

- VIBRATION
    - Operating: 0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave /minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
    - Non-Operating: 1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave /minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
- SHOCK
    - Operating: 6g, half-sine 11ms, 5 shocks per each of the three axes
    - Non-Operating: 12g, half-sine 11ms, 10 shocks per each of the three axes

14 Safety Label

The power supply will be shipped with the safety label applied to the cover. The vendor may propose a suitable location. The label should be 102mm × 51mm in size, UL-approved material, orange (Pantone 715 – or a similar agreed upon color), with a matte finish. The fonts shall be black, Arial bold with a ~ 2.5mm font. Barcodes shall follow the CODE 128-AUTO standard. The label location and orientation on the chassis cover is indicated in the mechanical drawing at the end of document. The sheet metal shall be recessed 1mm to avoid scratching the label when installing the power supply (see the mechanical drawing). The label material shall be scratch resistant. The label shall include the following information and identification marks:

- Safety Markings
- Vendor name, Country of origin
- Model: AC-DC 3,300W
- Type: Vendor part number (also included in the first barcode, with only the number)
- The output format should be as follows; Voltage (at No Load), Output (max), Current (max). The maximum accuracy of the values should be to one decimal place. In this case the voltage and current does not match the rated power capability. The vendor is free to suggest any other format.
    - Input 1: 200-277V ~ 50/60Hz - 19A
    - Input 2: 33.8-52.5Vdc - 107A
    - Output 1: 12.6V == 265A, 3,300W
    - Output 2: 52.5V == 5A, 270W
    - Output 3: 54.0V == 6A, 300W
- Date Code, Serial Number, REV

- WWYYYYSSSSSXX: Shall be included in the third barcode (WW = week of the year; YY+ year; SSSSS = serial number; XX = revision)
- RoHS-6 symbol of compliance shall be added to the label
- WEEE symbol: The PSU label will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.
- Label: A sample label must be submitted to the purchaser for review and approval
    - The applied label shall be -1 mm embossed to avoid the risk of scratching the label when the power supply is installed in the shelf.

15 Connectors

15.1 12V Output from the PSU

The power module output ± 12Vdc connectors will be directly soldered onto the PCB board (or via a similar approach) to lower the output resistance path of the output current. Output resistance can reach around 265A. The connectors will mate with the Tyco Crown Clip II connector. The Tyco Crown Clip II connector will connect directly onto the output busbars of the shelf. The busbar blades should be nickel-plated and 3mm × 25mm. The negative busbar should be premating. Therefore, the output blades should also be offset by 2.5mm or the female receptacle in the shelf (Tyco Crown Clip II) should be offset 2.5mm to ensure premating.

15.2 AC and DC Input for the PSU

The power input connector will be male. It will be soldered directly onto the power module PCB. This connector shall contain the AC input, BBU input, 52.5Vdc BBU charging output, and the 54Vdc auxiliary output, as well as all the signals pins. All the negative and ground blades are pre-mating. The negative, ground, PS_KILL signal pins should be short pins to ensure premating. The actual choice of this connector is left to the vendor but the gender and floating requirements must be followed. Please refer to Section 22.3.2.

16 Mechanical Requirements

16.1 Physical Dimensions

The sheet metal material shall be steel, pre-plated hot-dip zinc coated, 1mm thick. See Section 19.9.1 for details on the finish and its resistance against corrosion. The detailed PSU chassis mechanical drawing is included at the end of this document before the appendix.

The Power Supply dimensions are:

- Height: 65mm
- Width: 165mm
- Depth: ~500mm

The PSU mechanical chassis is composed of a base and a cover. It is assembled using flathead screws. No rivets are allowed (the PSU may be opened by using a screwdriver). The cover shall have a small opening for microprocessor / DSP firmware upgrade (see Section 6.9). The pilot and mass production units will be built with the hard-tooled chassis. In the final application, the PSU will be installed in a metal shelf, with a direct interface with several input and output connectors inside it.

A mechanical latch should be used to securely fasten the PSU within the shelf. All touch points, including the latch, should be colored green (Pantone 375C). The latches shall have a backstop to prevent damage to the latch during actuation and should only lock into place when a good electrical contact is made on the rear connectors. A sturdy handle should be implemented which makes removal and insertion of the PSU as smooth as possible. Both the latch and handle should be implemented in a way such that it does not obscure any LEDs or silkscreens. The PSU will be heavy. The handle should be sturdy enough to carry the entire weight of the PSU. This scheme will allow a technician to quickly install the PSU in the tray, without using a screwdriver. The front face where the handle is attached should have perforated holes to allow airflow for the fan(s). Furthermore a 'keying' feature should be used so that the PSU cannot be installed upside down. Refer to the mechanical drawings

17 LEDs, Silkscreen

Use two 3mm LEDs to indicate the power supply's status. Locate them on the front panel face on the top left corner. There should be a distance of 8mm between the stickers.

Silkscreen text must be located next to each LED. The font must be black Arial condensed bold, with a size of ~2.5mm. The text to the right of the green LED should be PWR OK / BKP. The text to the right of the red LED should be FAIL.

The drawing below shows a typical location and silkscreen for the LEDs. The final proposed location is subject to the purchaser's approval.

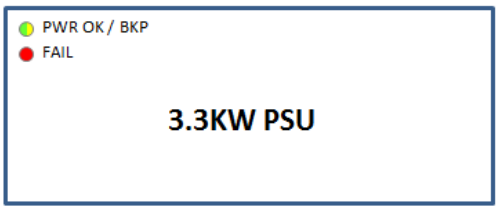


Figure 8: LED position/color and text diagram

PWR OK / BKP LED Values:

- Yellow (solid): When a valid AC input is applied, 12.6Vdc output is in regulation, and BBU is not installed, under 32Vdc, has the Fail/Protection/Stop_Discharge signals low or Sleep/Insert signal is high. Off, otherwise.
- Green (solid): When a valid AC input is applied, 12.6Vdc output is in regulation, and a BBU is installed (a valid BBU voltage should be 32Vdc or greater).
    - **NOTE**: This voltage should be measured at the DC input to the PSU via the discharge path of the BBU. It should not be measured from the sense line, in case of a blown fuse or a loose connection wire).
- Yellow (blinking): Blinks at 1Hz during the backup phase with a 90-second timeout. During the backup phase, the time counter of each power module must be synchronized (the yellow LEDs will blink in synchrony). Synchronization can be achieved by using a X-TAL crystal as a reference clock for the microprocessor installed in the power module, or by equivalent means.

FAIL LED:

- Red LED (Solid) for general power module failures, including fan failure. It follows the same rules for the red LED in the V1 Power Module. Off otherwise.
- If the main 12Vdc output fails, all other secondary converters shall be latched off. The 54Vdc auxiliary and battery charger converters should also shut down.
- If the 54Vdc auxiliary or the BBU step-up or the step-down battery charger converter fails or the CAN bus internal communication fails, the red Fail LED should turn on and the fail signal should be latched, but the main converter (LLC) should still provide 12.6Vdc to the busbars.
    - If the BBU step-up or step-down converter fails do not allow an AC power reset to clear the LED.

Alarm in AC mode	**PWR OK**	**FAIL Behavior**		**How to Clear the Alarm?**	
	LED	**LED**	**12V Output**	**Physical plug in / plug out**	
				Fail LED	**12V output**
AC Input without BBU (or BBU <32Vdc, BBU Fail/Protection/Stop_Discharge signals low, or Sleep signal is high)	Yellow	Off	On	-	-
AC + DC input (BBU > 32Vdc)	Green	Off	On	-	-
Backup mode	Blinking Yellow (1Hz)	Off	On	-	-

Boot-loading Mode	Green Blinking (2 Hz)	Off	-	-	-
Fan Failure, OCP, OVP, OTP, AC Input fail, Any general failures, 12V out of regulation	Off	Red	Off	Turn Off	Allow Restart
54Vdc Aux output fail	Off	Red	On	Remain On	Allow Restart
BBU Step-up converter fail	Off	Red	On	Remain On	Allow Restart (write to EEPROM)
BBU Step-down charger fail	Off	Red	On	Remain On	Allow Restart (write to EEPROM)
CAN bus internal communication failure	Off	Red	On	Remain On	Allow Restart

NOTE: The green/yellow PWR OK LED and FAIL LED cannot be on at the same time. Also, the Fail LED should not clear while the PSU enters a back-up condition. The Fail LED should be latched permanently when a failure occurs in the step-up condition.

Latching-OFF conditions (power module also latches-OFF):

- General power supply failure
- The output 12V before the ORing MOSFET goes out of regulation
- Fan failure or fan low speeds (5 sec delay on persistency)
- Over current protection (2 sec delay on persistency)
- Over temperature protection (2 sec delay on persistency)
- Over voltage protection

NOTE: The latching conditions also apply to the BBU step-up and step-down converter

18 Reliability, Quality, Miscellaneous

18.1 Spec Compliance, Quality FA, Warranty

- The vendor is responsible for the PSU meeting the specifications as stand-alone unit, as well as at the system level. They must also ensure that the power supplies shipped in production will conform to the specification with no deviations.
- The vendor is responsible to exceed the production quality standards achieved on the pilot run, without fluctuations.

- A complete failure and root cause analysis are required of all failures from EVT, DVT, and PVT. The vendor must report the actions taken to correct these failures prior to entering mass production.
- The vendor shall warrant the power supply for defects and workmanship for a period of three years from the date of shipment when the device is operated within specifications. The warranty is fully transferable to any end user. A standard VOID warranty sticker may be applied.

18.2 Mass Production: First Article Samples

Prior to final project release and mass production, the vendor will submit a good quantity (TBD) of PVT production pilot run verification samples, including the following:

- All the pertinent development documents, production documents, and reports necessary to release the product for mass production.
- The pilot samples shall be built in the allocated facility for mass production and use hard-tooled chassis and parts (where applicable).
- A full specification compliance matrix, full test report, and production line final test PASS tickets.
- Samples that passed the burn-in process planned for production (if any).
- Samples must be shipped using a shipping box that is approved for production.
- The units are certified and have a safety label applied[1].

18.3 Mean Time Between Failures Requirements

- The PSU shall meet the mean time between failures (MTBF) calculation, which is proposed by the vendor and agreed upon by the purchaser. The MTBF calculation should be at 90% confidence level, 45°C of ambient temperature, 277Vac of input voltage, and full load (per the latest version of Telcordia SR-332, alternatively per MIL-HDBK-217). The fan is not included in the calculation. The vendor will provide the MTBF of the fan separately.
- The PSU shall meet a demonstrated MTBF of minimum 500K hours at 90% confidence level prior to first customer shipment (including pilot samples and mass production units).
- MTBF goal: the vendor shall provide the best MTBF numbers that the PSU will be able to meet, no matter the minimum demonstrated MTBF requested.
- The PSU shall have a minimum service life of five years (24 hours/day, Full load, 277Vac, 45°C of ambient temperature).

18.4 Design-rating Guidelines, Design for Test, Design for Manufacture

- For all the boards used in the PSU design, the in-circuit test coverage and test point access shall be > 95% or higher.

[1] A “Pending Certification” sticker may be allowed until the certification process is complete.

- The vendor will provide the standard de-rating guidelines normally used for the design of the industrial custom power products for purchaser audit.
- The vendor shall provide design for test (DFT) and design for manufacture (DFM) reports at EVT phase.

18.5 Not Allowed Components

- Trimmers and/or potentiometers
- Tantalum capacitors
- Dip switches
- High side driver ICs
- Paralleled power MOS are allowed provided that the design prevents parasitic oscillations
- Phase shift topology
- SMT ceramic capacitors are allowed with the case size < 1206. The size 1206 can still be used when SMT capacitors are placed far from the PCBs edge, and with a correct orientation that minimizes the risk of cracking
- Allowed ceramics materials for SMT capacitors are:X7R or better material. The COG or NP0 types should be used in critical portions of the design, such as feedback loop, PWM clock settings, etc.
- The use of any electro-mechanical relays, and the relay type shall be discussed up front before any approval is given to include them in the design.

Capacitors:

- All the electrolytic capacitors shall be rated at 105°C and shall be selected from proven quality manufacturers only.
- All capacitors shall have a predicted life of at least 50,000 hours at 45°C inlet air temperature under the worst conditions.

18.6 Quality Control, Process, Burn-In

- Incoming Quality: <0.1% rejections
- Process capability (Cpk) values should equal or exceed 1.33 (pilot build and production) using a sample size equal to 32 for Cpk measurement.
- Perform Cpk measurements on every batch/lot for pilot and mass production builds
- The vendor will implement additional quality control procedures during production, by sampling power supplies randomly from the production line and running full tests to prove ongoing compliance to the requirements (it may include EMI production).
- PCB boards are UL recognized components rated 94 V-0 (or better) and rated 130Vac
- Multi-layered (> 2 layers) PCB boards are welcome for a better layout and simplification of the manufacturing process, if they make economic sense.

18.7 Packaging

The PSU shall be shipped using a custom package containing multiple units (max TBD each box). The packaging for the PSU must ensure that it will not get damaged during transportation. Units must arrive in optimum conditions and be ready for immediate use. A shipping box shock test shall be proposed by the vendor and submitted to the recipient for audit and approval. The vendor is required to provide a test report for shock and vibration and for the packaging drop test.

18.8 Documentation

The vendor shall provide the following documentation (prototypes may not include some of these documents):

- Theory of operation
- Block diagrams
- Schematics, component placements, board layouts (PDF)
- BOM ordered per reference designators
- BOM ordered per components (including AVL)
- Mechanical drawings (PDF format. Native files and/or DXFs will be provided to perform collaborative work on the design, for a seamless PS integration at the system chassis level)
- Functional test report (DVT report)
- De-ratings report (worst conditions)
- Temperature test report (indicating critical de-ratings, if any)
- MOSFET waveforms at all worst-case operating conditions
- Capacitor life calculation
- EMI plots for conducted and radiated emission
- MTBF data and report, including calculation
- Production line automatic final test procedure

NOTE: The vendor shall propose a qualification test plan and a reliability test plan. An EDVT test procedure in a thermal chamber, with thermal shocks on all corners should also be included. All documentation provided must be searchable. For example, searchable PDF schematics.

Sheet Metal material, Zink Whiskers implications, Conformal Coating

- Sheet Metal Chassis Material is hot-dip Zinc coated, JIS G3302 SGCC (Z20 to Z22), with 1mm of thickness. The ‘Z’ parameter defines the metal coating thickness: Z20 is for 40μm of thickness, and Z22 is for 43μm.
- The Japanese standard is ‘JIS G3302’, while the US standard is ‘ASTM A653’.
- Mechanical design shall prevent sharp edges and possible metal oxidation in the critical points of the sheet metal (e.g. in the cut & bends portions, etc.).

- Both chassis design and metal base material will not promote the growth and propagation of zinc and tin whiskers.
- Metal base materials with electro-zinc plating, or poor conductivity plating, are not allowed.
- Alloy materials are a possible option, while stainless steel is another possibility provided that it makes cost sense (both options are subject to customer approval)
- Aluminum material is not allowed for the enclosures.
- The chassis enclosure, as well as the whole electronics, shall meet certain contamination requirements (see ANSI spec at § 14)
- The Power Shelf and Modules are not classified as "Fire Enclosure"

18.8.1 Conformal Coating and Protection

The gate terminals of all high-voltage MOSFETs as well as the most sensitive areas of the electronic circuitry in the boards must be protected against potential resistive contacts with other voltage potentials (e.g. MOS Drain leads, etc.) due to whiskers, pollutant particles, dust, moisture (for example contaminant substances can become conductive in presence of moisture), and up to some local wet condensation occurrences.

Local Conformal Coating shall be applied to critical areas of the boards to protect sensitive circuitries, using an atomized spray process (no dipping process is considered here). The thickness of the coating shall be ~ 50µm to ~ 150µm. The vendor (mainly the ultimate Manufacturing Facility) shall demonstrate to possess good skills, experience, and long years of experience on automated Conformal Coating application and process. The power modules and shelves' main board shall be partially Conformal Coated (top & bottom); critical board areas shall be agreed upon, typically the ac high-voltage input section at shelf level, like the AC input, board-mount connector area.

V2 Shelf-Only Specification

19 V2 Shelf Overview

This specification defines the requirements for a 6,600W standalone V2 Power Shelf (hereinafter, shelf), single-voltage 12.6Vdc output, powered from a three-phase AC line, hosting three 3300W (N + 1) hot swap single-phase power modules. This product is used for IT Systems, both online and back-up power functions. This shelf will also host three BBU modules for the power backup functions.

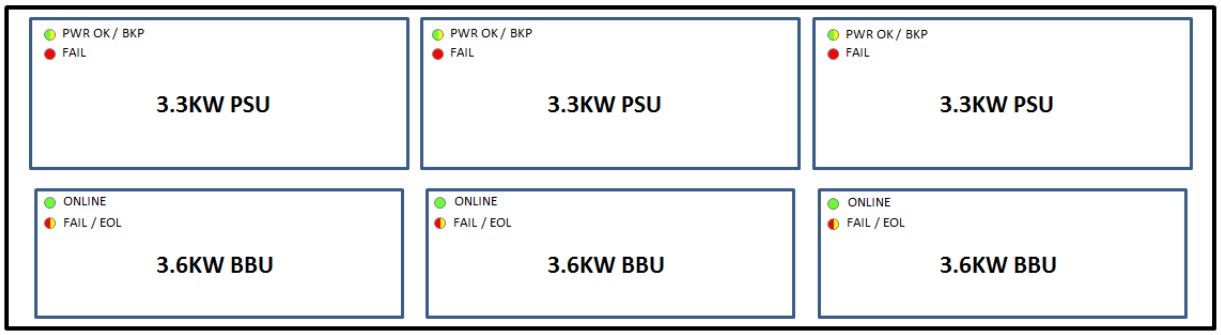


Figure 9: Shelf-only diagram with PSUs and BBUs

20 Mechanical Dimensions

The dimensions (width × height) are the same as for the OCP 'V1 Power Shelf' except the depth of the shelf is now changed to 650mm. The shelf should use a 1.2mm sheet metal thickness. The shelf should securely latch into the OpenRack and should follow all dimensions shown in the reference diagram below. The weight of the shelf plus three PSUs and three BBUs should not exceed 70kg.

20.1 Power Module Dimensions

Please refer to Section 17 for the power module mechanical specifications.

20.2 BBU Dimensions

The BBU module is provided on the side, and it is not part of this specification. Several BBU signals are connected to the power module: please refer to the V2 BBU specification. The size is (62mm (H) x 160mm (W) x 420 (D) mm). The BBU depth is fixed to 435mm; the power module depth will be longer. The output voltage is 32Vdc (discharged batteries) to 52.5Vdc (fully charged batteries) with a max output current of 120A. Output connector: A FCI connector (P/N: 51915-415) will be used on the rear of the BBU (3 blades + 24 signals + 3 blades). Please refer to the V2 BBU Specification for more information.

20.3 Bus bar plating

The copper bus bars used inside the shelf are nickel plated, including the output 12Vdc blade pair. Two plating process options are:

- Minimum 10 microns of nickel plating
- Minimum of 5 microns of nickel plating, and on top minimum 10 microns of tin plating

The above is electroplating. The final look (smooth or grain) depends on the finish of the copper blade base material. The plating finish itself can be matte (smooth finish) or brush (grain finish), whatever is best for the interface resistance of the terminal lug.

20.4 Shelf/Safety Labels

Silkscreen text of Slot #1, Slot #2, and Slot #3 should be added to designate the three columns (each PSU/BBU pair). Slot #1 should be the first slot to the left looking at the shelf from the front (where you insert the PSUs and BBUs).

There should be silkscreen text for every input and output connectors on the back of the shelf. The suggested silkscreen text is as follows, AUX, MGMT, PWR OK, and 3Φ AC INPUT. The text 12 V should be written above the green LED. Add silkscreen text to indicate which main output blade is positive (+) and negative (-). Please refer to the attached mechanical reference drawing for suggested placement.

A yellow rectangular safety label shall be placed near the AC input connector, which instructs the operator that caution high voltage, and to disconnect AC plug from the AC source before installing or removing the connector. Sample of the label will be submitted to the Vendor for review and approval.
A product label shall be placed on top of the power shelf as well, similar to Section 15.

21 Input and Output Connectors

All the connectors used on the rear of the shelf must have a locking latch mechanism. All the connectors must also be keyed. The input/output shelf PCB must be insulated at the bottom to prevent any of short circuits with the mechanical shelf chassis. The opening shall be large enough to accommodate the extra room needed for unlatching the latch mechanism.

21.1 AC Input

The AC input power inlet is a 5 pin Positronic connector p/n : SP5YYE48M0LN9A1/AA-PA1067, male socket high conductivity contacts, board mount right angle, RoHS compliant, solder type with metal fasters for mechanical strength. General requirements for the AC connector are as follows:

- Must be locked in
- Must have the possibility to install a pre-mating pin (bottom right pin) for GND.
- Must be at least 32A rated and 600V (Size 12 contacts)
- Its connector counterpart (carrying the AC voltage from the grid) must be able to have a custom molded strain relief built on the housing, for both safety and mechanical strength)
- There should also be two screws on the side of the connector that directly connect the screw into the standoff between the PCB and sheet metal, for extra strength.

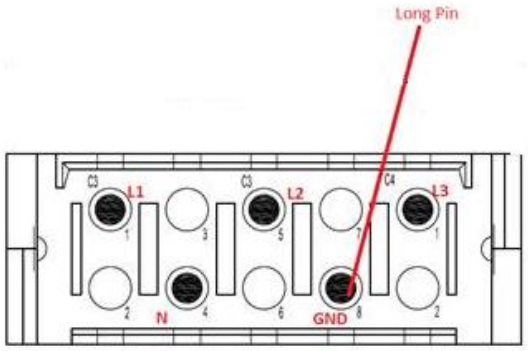


Figure 10: 5-pin Positronic connector

Pin Assignment: The top three pins should be used for Line 1, Line 2, Line 3, and the bottom left pin should be used for neutral and the bottom right pin should be ground where its male pin is longer than the other 5 pins (looking at the male connector from the back of the shelf).

21.1.1 AC Surge Protection Inductors

Three inductors shall be installed horizontally near the AC input Positronic connector, one for each of the input lines. The inductor shall be wound around a ferrite cylindrical core (at least 8mm in diameter with at least 2.8mm diameter copper winding). The minimum inductance shall be around 1µH. The vendor is free to choose the inductor. The main purpose is to help with AC power surge protection.

21.2 Outputs

21.2.1 54Vdc Auxiliary Output

The 54V output connector should be a 3 pin Molex Sabre (P/N: 43160-3103) type used as a 54Vdc output from the rear panel of the shelf. The connector will power the IT switches. The female mating connector in the DC V2 PDU will use a 14 AWG 3-wire cable. The connector should be arranged such that latch shall be on top and the connector polarity should match the figure below (looking at the shelf from the rear). The sheet metal cutout on the back of the shelf shall be large enough to accommodate a person unlatching the latching mechanism.

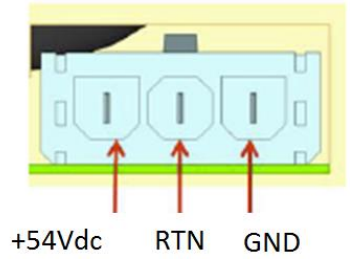


Figure 11: Molex Male Sabre connector for IT switch load

21.2.2 Mgmt – RJ45

An RJ45 output is needed on the rear panel of the shelf for the RS-485 digital bus. Ideally, the connector should be placed flush with the output of the shelf, Its cutout on the sheet metal shall accommodate the latch. More information for the technical use of this connector can be found in the V2 Power Shelf Communication specification.

Table 1:RJ-45 pin functions

Pin	Wire color	Function
1	White/Orange	GND
2	Orange	POWER_FAIL_L
3	White/Green	REDUNDANCY_LOST_L
4	Blue	+RS-485 A
5	White/Blue	- RS-485 B
6	Green	Shelf Position
7	White/Brown	Rack Position
8	Brown	Rack Position

21.2.3 POWER_FAIL_L/REDUNDANCY_LOST_L

A six-pin POWER_FAIL_L connector will be needed to send out the 9Vdc (1A) POWER_FAIL_L and REDUNDANCY_LOST_L signal. Please refer to Section 7.2 above for more information regarding the operation of these two optocoupler signals. An isolation of 100Vdc is needed. The 9Vdc output should be available within 500 μs from when the signals, POWER_FAIL_L and REDUNDANCY_LOST_L, are asserted low. Use a Molex Minifit Jr (P/N: 39-30-1062) connector in the shelf. In the figure below, we can see the pin outs as if we were looking at the rear of the shelf. The POWER_FAIL_L and REDUNDANCY_LOST_L signals will also be routed to pin 2 and pin 3 respectively, after the optocoupler to the RJ45 connector, as well as the RTN pin can be routed directly to the pin 1 on the RJ45 connector, which is also RTN.

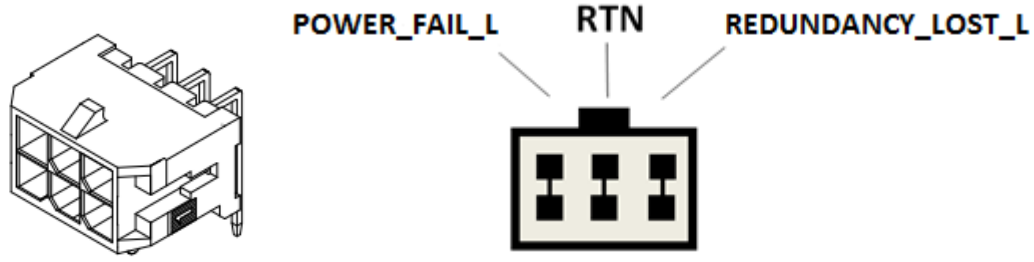
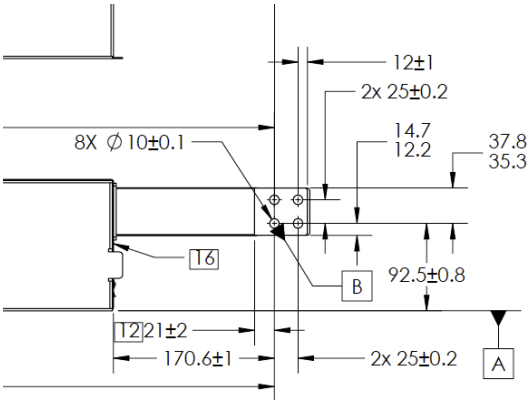


Figure 12: Molex MiniFit Jr Connector diagram

21.2.4 12Vdc Output

The 12.6Vdc outputs are a pair of busbar blades, which are 50mm tall, 3mm thick, with a 23mm distance between the positive and negative pair. The length of the busbar should be less than 190mm with the busbar offset by 2.5mm

(negative is shorter). Looking from the rear of the shelf, the +12Vdc busbar is the busbar to the right. It protrudes 2.5mm outwards. The location of the busbar shall be 15mm from the top of the shelf and the bottom of the busbar blade shall be 75mm from the bottom of the shelf. There should be four round shape holes in a square pattern with 25mm distance from the center of the round holes. Please refer to the figure below and the detailed mechanical drawing attached at the end of the specification. The busbar should be able to directly interconnect with the busbar installed in the V2 OpenRack. The busbar shall be protected with shrink tubing insulating material, preferably red for the +12Vdc and black for the return. Ferrites CM chokes should be installed on the 12Vdc output, similar to in the V1 Power Shelf. The center output busbar pair should be able to carry 6600W of full power when used alone. The worst-case thermal area on the shelf's busbars should not exceed a 30°C delta temperature rise. Design the busbar in such a way that there is only a maximum loss of 33W (0.50% efficiency loss) total in the worst-case condition when the shelf is running at a maximum of 6,600W. Design note: The output busbars should be placed inside the shelf in such a way that they do not impede the airflow out of the PSU modules.



Side view of the rear of the Power Shelf

21.2.5 12Vdc Green LED

A 5mm Green LED, installed on the rear panel should turn on when there is greater than 11Vdc on the common output busbar. This is a 12V Power Good indication from the rear of the shelf.

21.3 Internal Shelf Mating

21.3.1 Output from the PSU

Since the power module output +/- 12V connectors are directly soldered onto the PCB board, which will mate with the Tyco Crown Clip II Sockets, which will be screwed onto the output busbars of the shelf. The Tyco 1643903-1 allows six degrees of float for improved blind mating.

Figure 13: Power Module Output 12 V Blade Connector

21.3.2 AC and DC Input for the PSU

The shelf will contain a female FCI T60 type connector that will be wire terminated (wires coming from AC input and BBU) and shall be floating in the shelf.

The suggested connector should be similar to the one below with at least 11 blades and 48 signal pins (the order of the blades and pins do not matter). A spacer is advised between AC power line and the signals to ensure enough safety clearance. Ground pins should mate first. Some signal pins should be shorter than the other pins (ex. PS_KILL, etc.). The vendor is free to choose the exact number of signal pins, power blades, and layout based on their PSU layout/design. The BBU charging voltage can use a few signal pins or have one extra blade designated for charging. The diagram below is just a suggestion on how to implement the male connector on the PSU.

Table 2: Output connector values

Auxiliary 54V	Auxiliary 54V Return	3 Blades for BBU input (+)	3 Blades for BBU input (-)	1	2	3	4	5	6	7	8	9	10	11	12	AC Line	AC Neutral	GND
				13	14	15	16	17	18	19	20	21	22	23	24			
				25	26	27	28	29	30	31	32	33	34	35	36			
				37	38	39	40	41	42	43	44	45	46	47	48			

21.3.3 BBU Output

The output of the BBU will be a female FCI connector, soldered directly on the PCB board that is installed inside the BBU. The shelf shall house the male counterpart with the negative, ground, and a few pre-mated signal pins, that is wire terminated and floating in the shelf. The wires will terminate at the female connector of the PSU above.

The figure below shows the male BBU mating connector (P/N: 10097404-072LF) on the shelf as if you were looking at it head on from the front of the shelf.

Table 3: Output connector values

Batt (-)	Batt (-)	Batt (-)	1	2	3	4	5	6	Batt (+)	Batt (+)	Batt (+)
			7	8	9	10	11	12			
			13	14	15	16	17	18			
			19	20	21	22	23	24			

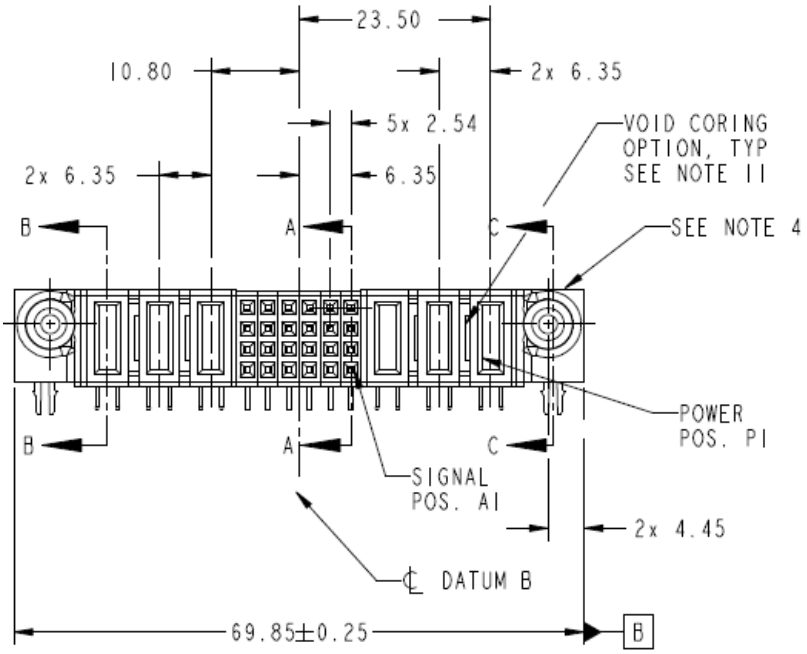


Figure 14: BBU output connector
For more information please refer to the V2 BBU specifications.

21.4 Latches/Other Connectors

All touch points, including the latch, should be colored green (Pantone 375C). The latches shall have a backstop to prevent damage to the latch during actuation.

In addition to the shelf latches there will also be an oval hole on either side of the shelf to securely fasten the shelf into the rack as shown in Detail A of the mechanical drawing below.

Any other connectors used internally in the shelf should use a latch and lock type connector.

22 Environmental Requirements

Refer to Section 14 above.

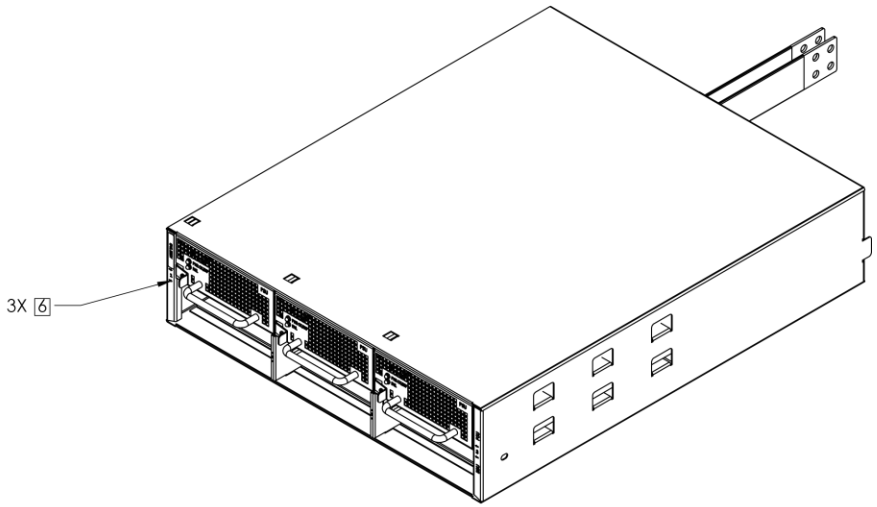
23 Mechanical Drawings

NOTES

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE MM.
3. ALL COMPONENTS SHALL BE UL 94V-0 RECOGNIZED AND ROHS COMPLIANT.
4. CASE MATERIAL SHALL RESIST THE CREATION OF ZINC WHISKERS, SUCH AS ASTM A653 AND JISG3302 SGCC.
5. ALL DIMENSIONS ARE CONSIDERED CRITICAL TO FUNCTION DIMENSIONS AND SHALL BE INCLUDED IN PART QUALIFICATION.
6. PSU, BAY NUMBERS, REAR IO CONNECTORS, BUSBAR POLARITY, AND LEDS TO BE LABELED IN A PERMANENT AND LEGIBLE MANNER LOCATED APPROXIMATELY WHERE SHOWN. TEXT 4MM TALL MINIMUM.
7. LATCH COLOR PANTONE 375C GREEN OR SIMILAR WITH WRITTEN APPROVAL FROM FACEBOOK ENGINEERING. LATCHES MUST HAVE A BACKSTOP TO PREVENT DAMAGE TO LATCH DURING ACTUATION. PSU AND BBU LATCHES MAY NOT LATCH UNTIL AFTER PSU HAS GOOD ELECTRICAL CONNECTION.
8. AIRFLOW PER INDICATED DIRECTION.
9. RESERVE LOCATION TO PLACE ASSET TAG APPROXIMATELY WHERE SHOWN.
10. ALL EDGES SHALL BE CONDITIONED FOR HANDLING WITH INDUSTRY STANDARD BURR NO LARGER THAN 10% OF MATERIAL THICKNESS AND SHALL CONFORM TO UL SAFETY SPECIFICATION 1349.
11. PSU HANDLE SHAPE AND LOCATION PER DESIGNER'S PREFERENCE.
12. EXTERNAL OUTPUT BUSBARS WILL BE INSULATED. POSITIVE TO BE RED. NEGATIVE TO BE BLACK. POLARITY AS DEFINED.
13. METHOD OF KEY CONSTRUCTION AT SUPPLIER'S DISCRETION. KEY LOCATION FOR SHELF SUPPLIER #1 ONLY.
14. METHOD OF KEY CONSTRUCTION AT SUPPLIER'S DISCRETION. KEY LOCATION FOR SHELF SUPPLIER #2 ONLY.
15. ALL COMPONENTS SHALL BE CLEAN AND FREE OF RUST AND FOREIGN MATERIAL SUCH AS DIRT,OIL, GREASE, OR OTHER CONTAMINANTS.
16. ADD RADIUS TO EDGE TO HELP WITH INSTALLATION INTO RACK.
17. ADD SAFETY LABEL AS DEFINED IN POWER SHELF ELECTRICAL SPECIFICATION APPROXIMATELY WHERE SHOWN.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	INITIAL RELEASE	06AUG13	SM
	2	BUSBAR HEIGHT; CHASSIS HEIGHT	08AUG13	SM
	3	DEL NOTE 10;ADD 13; ADD REF DES TO REAR WALL; ADD DETAIL D AND E	22AUG13	SM
	4	CHG PWR_OK CONNECTOR; CHANGE BBU KEY DETAIL	20 SEP 13	SM
	5	ADD BBU KEY DETAIL;UPDATE NOTE 6, 7, 9,12 AND13;ADD NOTE10,14 AND 15	22 OCT 13	SM
	6	ADD BUSBAR SIZE TO 2B1;REDUCE BBU BAY WIDTH; INCREASE BBU BAY HEIGHT	5FEB14	SM
	7	INCREASE HEIGHT OF PSU TO 65MM; INCREASE BUSBAR TOLERANCE @2B1;	18FEB14	SM
	8	UPDATE PSU ARTWORK; ADD SLOTS FOR BBU PROTECTION BRACKET IN DETAIL F; ADD NOTE 17 @3D2	5MAR14	SM
	9	ADJUST BBU KEY @ 2A8 AND LABEL LOCATION @3C3; ADD DIM FOR BBU LATCH @2D4	20JUN14	SM
	10	REDUCE WARNING LABEL SIZE AND ADD NOTE 17; ADD DIM FOR BBU TO CONNECTOR TOLERANCE @2D4	23JUL14	SM
	11	MOVED LOCATION OF DATUM B FROM THE CHASSIS FRONT 0.5MM @2A3	25 JUL 14	SM



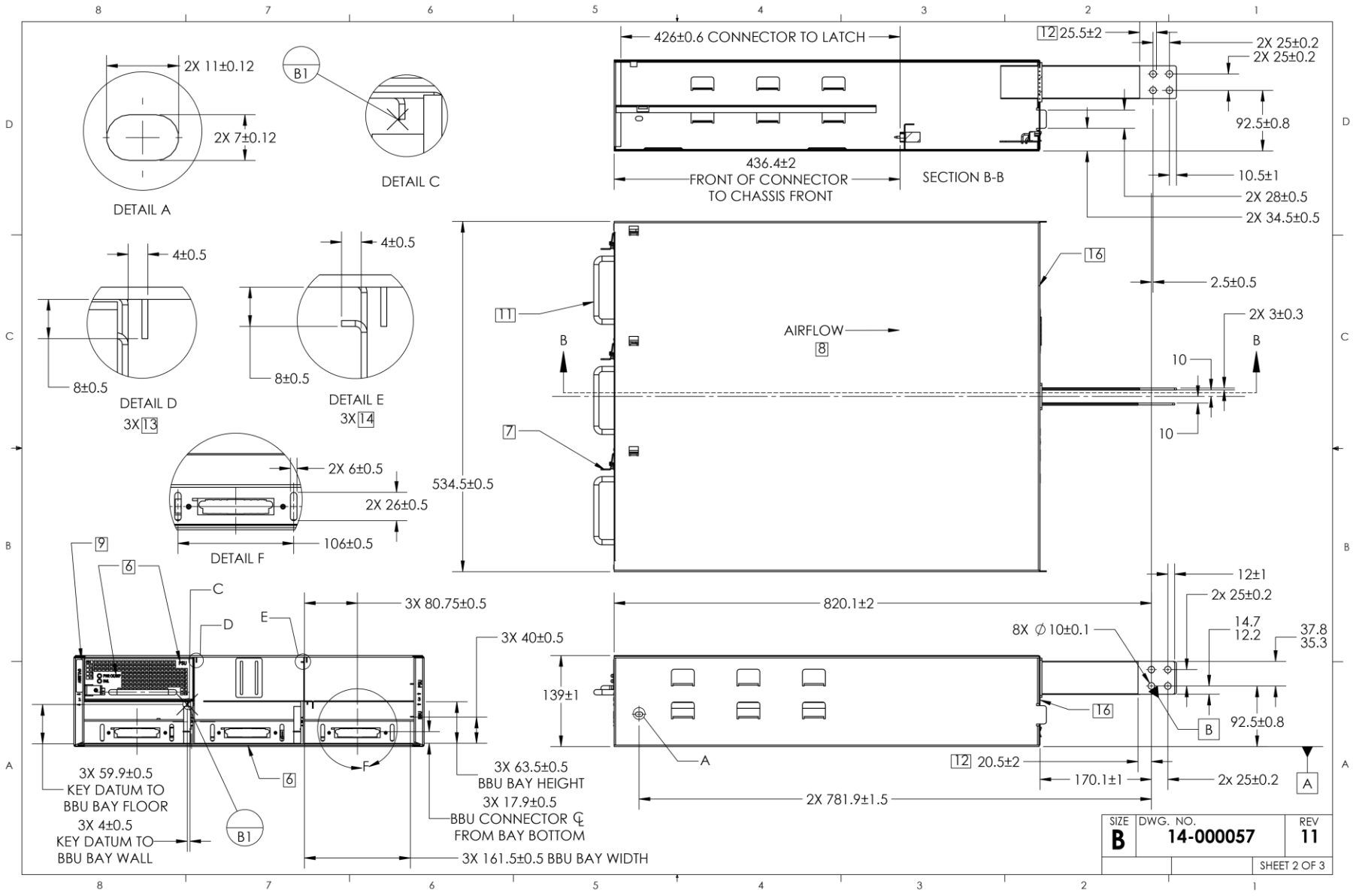
	NAME	DATE
DRAWN	MILLS	6AUG13
CHECKED		
ENG APPR.		
MFG APPR.		

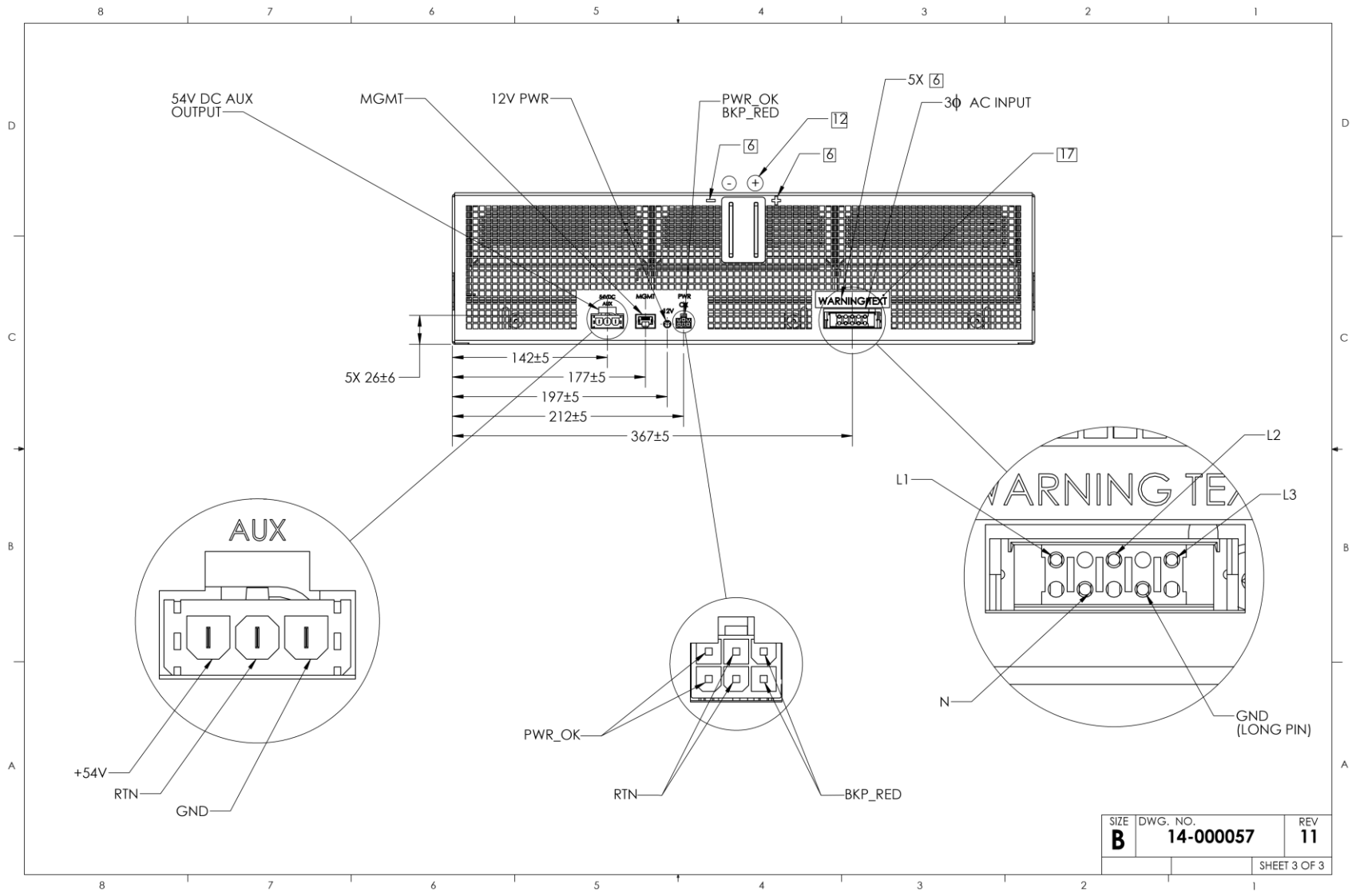
facebook

TITLE: POWER SHELF V2 12.5V 6.6KW

SIZE B | DWG. NO. 14-000057 | REV 11

SHEET 1 OF 3

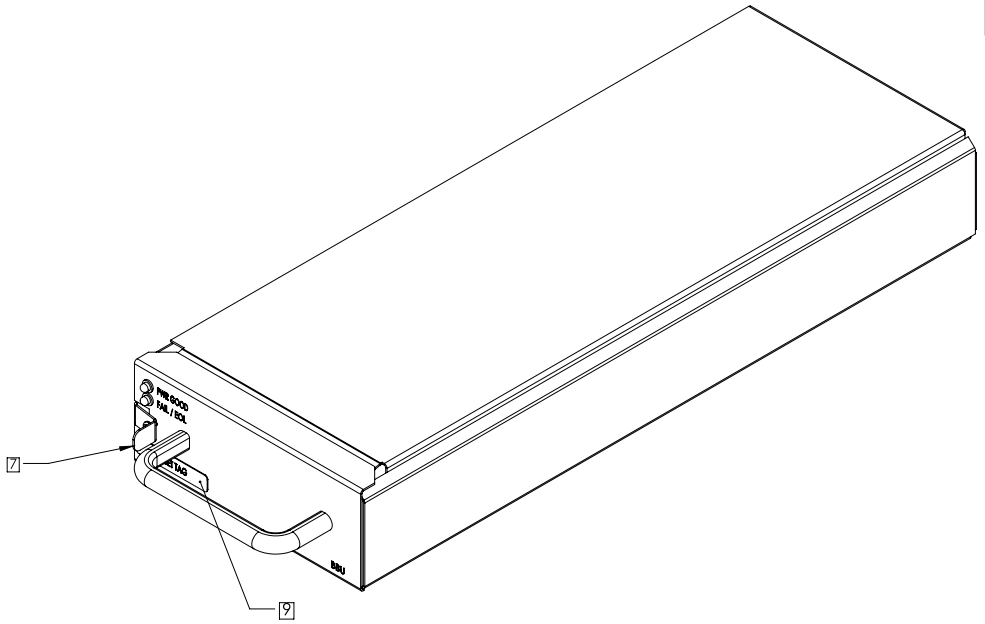

2X 11±0.12
2X 7±0.12
DETAIL A
B1
DETAIL C
426±0.6 CONNECTOR TO LATCH
12 25.5±2
2X 25±0.2
2X 25±0.2
92.5±0.8
436.4±2
FRONT OF CONNECTOR
TO CHASSIS FRONT
SECTION B-B
10.5±1
2X 28±0.5
2X 34.5±0.5
4±0.5
8±0.5
DETAIL D
3X 13
4±0.5
8±0.5
DETAIL E
3X 14
16
2.5±0.5
11
AIRFLOW
8
2X 3±0.3
B
B
10
10
7
2X 6±0.5
2X 26±0.5
106±0.5
DETAIL F
534.5±0.5
9
6
C
D
E
3X 80.75±0.5
3X 40±0.5
820.1±2
12±1
2x 25±0.2
8X ∅10±0.1
14.7
12.2
37.8
35.3
139±1
16
B
92.5±0.8
A
12 20.5±2
170.1±1
2x 25±0.2
A
2X 781.9±1.5
3X 59.9±0.5
KEY DATUM TO
BBU BAY FLOOR
3X 4±0.5
KEY DATUM TO
BBU BAY WALL
6
B1
F
3X 63.5±0.5
BBU BAY HEIGHT
3X 17.9±0.5
BBU CONNECTOR ℄
FROM BAY BOTTOM
3X 161.5±0.5 BBU BAY WIDTH
SIZE
B
DWG. NO.
14-000057
REV
11
SHEET 2 OF 3


54V DC AUX OUTPUT
MGMT
12V PWR
PWR_OK BKP_RED
5X 6
3ϕ AC INPUT
12
6
6
17
WARNING TEXT
5X 26±6
142±5
177±5
197±5
212±5
367±5
AUX
+54V
RTN
GND
PWR_OK
RTN
BKP_RED
L1
L2
L3
N
GND (LONG PIN)
SIZE B
DWG. NO. 14-000057
REV 11
SHEET 3 OF 3

NOTES

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE MM.
3. ALL COMPONENTS SHALL BE UL 94V-0 RECOGNIZED AND ROHS COMPLIANT.
4. CASE MATERIAL SHALL RESIST THE CREATION OF ZINC WHISKERS SUCH AS ASTM A653 AND JISG3302 SGOC.
5. ALL DIMENSIONS ARE CONSIDERED CRITICAL TO FUNCTION DIMENSIONS AND SHALL BE INCLUDED IN PART QUALIFICATION.
6. LEDS LABELED IN A PERMANENT AND LEGIBLE MANNER LOCATED APPROXIMATELY WHERE SHOWN. TEXT 4MM TALL MINIMUM.
7. LATCH COLOR PANTONE 375C GREEN. LATCHES MUST HAVE A BACKSTOP TO PREVENT DAMAGE TO LATCH DURING ACTUATION.
8. AIRFLOW PER INDICATED DIRECTION.
9. RESERVE SOLID AREA IN CHASSIS TO PLACE ASSET TAG APPROXIMATELY WHERE SHOWN.
10. ALL EDGES SHALL BE CONDIFTIONED FOR HANDLING WITH A BURR NO GREATER THAN 10% OF MATERIAL THICKNESS AND SHALL CONFORM TO UL SAFETY SPECIFICATION 1439.
11. COMPONENT SHALL BE CLEAN AND FREE FROM FOREIGN MATERIAL. DIRT,OIL,GREASE,OR OTHER CONTAMINANTS ARE NOT ALLOWED.
12. CLEARANCE FOR ALIGNMENT PIN. 12MM PROTRUSION INTO BBU MAX.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	INITIAL RELEASE		SM
	2	CONVERT DESIGN TO CAM	29AUG13	SM
	3	ADD KEY; MOVE CONNECTOR INSIDE	9 SEP 13	SM
	4	ADD PIN LOCATIONS;CHANGE KEY DETAIL	20 SEP 13	SM
	5	REDUCE KEY SIZE; MOVE CONNECTOR AND ALIGNMENT HOLES	15 OCT 13	SM
	6	INCREASE HEIGHT TO 62MM; CHANGE CAM O LATCH AND HANDLE; REMOVED AIRHOLES AT EXIT; KEY SIZE INCREASED	5 FEB 14	SM
	7	ADD BRACKETS TO PROTECT CONNECTOR	10 MAR 14	SM
	8	REMOVE FRONT AIR HOLES; ADJUST LED AND KEY	11 MAR 14	SM
	9	ADD TOLERANCE @2D8	13MAR14	SM
	10	DELETE SHELF SIDE CONNECTOR FROM VIEWS	29MAY14	SM



	NAME	DATE
DRAWN	MILLS	7MAR13
CHECKED		
ENG APPR.		
MFG APPR.		

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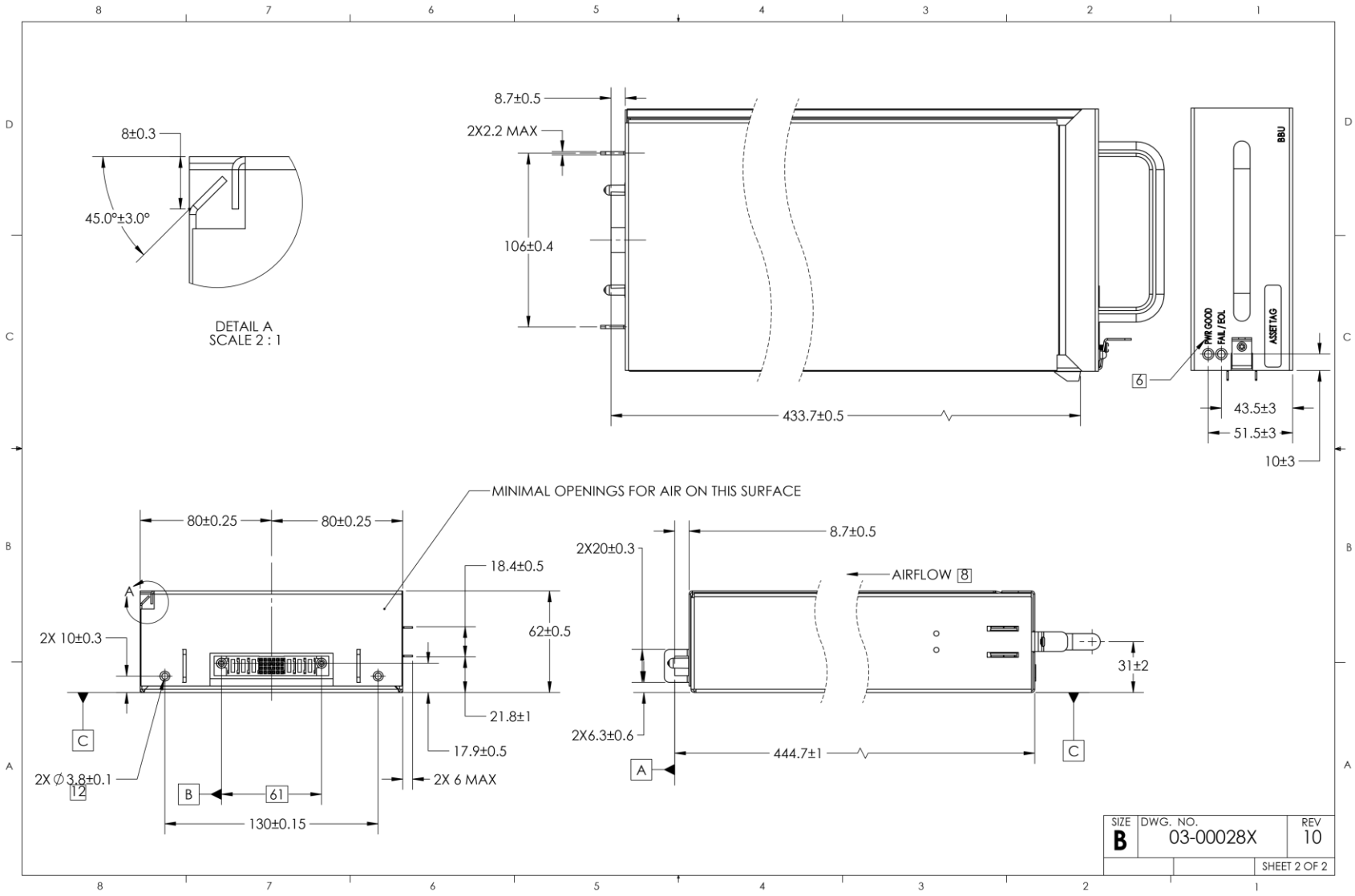
TITLE: BATTERY BACK UP UNIT, V2 53VDC BBU

SIZE	DWG. NO.	REV
B	03-00028X	10

SHEET 1 OF 2


8±0.3
45.0°±3.0°
DETAIL A
SCALE 2 : 1
8.7±0.5
2X2.2 MAX
106±0.4
433.7±0.5
BBU
PWR GOOD
FAIL / EOL
ASSET TAG
6
43.5±3
51.5±3
10±3
MINIMAL OPENINGS FOR AIR ON THIS SURFACE
80±0.25
80±0.25
18.4±0.5
62±0.5
2X 10±0.3
21.8±1
17.9±0.5
2X 6 MAX
2X ∅3.8±0.1
12
61
130±0.15
2X20±0.3
8.7±0.5
AIRFLOW 8
31±2
2X6.3±0.6
444.7±1
SIZE B
DWG. NO. 03-00028X
REV 10
SHEET 2 OF 2

Appendix

23.1 How the PSU shall interrupt signals from the BBU

All the information below has already been provided in the PSU/Power Shelf/BBU specifications. The following content is only meant as a summary and aggregate of all that information.

The signals that come from the BBU shall only be used by the PSU that is directly connected above it. For example, if one BBU asserts a low stop_discharge signal it should not affect the other two PSU/BBU pairs.

23.1.1 Charge_Enable

When the PSU sees this signal go low, it must wait two seconds then turn on the charger and start charging the PSU until the Charge_Enable signal goes high.

- If the Charge_Enable signal is low for some reason during a BBU discharge (outage/self test) the PSU shall not charge the BBU and shall keep the step-down convert off.
- If the current given by the charger is less then 500mA and if the voltage is not within 52.5Vdc ± 2% (at the sense lines) then the Fail signal on the PSU shall be asserted which will subsequently cause the BBU to go into sleep mode and the BBU will then open its charging MOSFETs.
- If the BBU does not see any current for 5 consecutive minutes then the BBU will go into sleep mode and assert a high Sleep signal.
- If the battery charger is on for more than five consecutive hours then the battery charger should be considered failed and the PSU should assert the Fail LED. At the fourth consecutive hour the BBU will consider itself failed. If for some reason this doesn't happen, there is a 5-hour timer on the PSU.
- If one of the Charge_Enable signals is low for any of the three BBUs then it should block itself, and the other BBUs, from performing a SoH check.

NOTE: the step-down (charger) and the step-up converter shall never be on at the same time.

23.1.2 State of Health

- If the SoH is low the PSU shall check that all the criteria are met in Section 7.2.4. If so, then the PSU shall use the BBU as the energy source until the SoH signal goes high. If any of the conditions in Section 7.2.4 are not met the PSU shall recheck the conditions every 10 minutes as long as the SoH signal is low.
- If at any time during the battery test, when the SoH signal is low, if the BBU gives the Stop_Discharge or Fail signal the PSU shall stop using the BBU as a source of power.
- If the PSU in Slot #1 is running a SoH test, and an AC power outage happens, then when AC power returns the PSU in the other slots shall turn on synchronously without the random timing. This is the same scenario as having the PSU in Slot#1 fail.
- If a SoH signal was low for a BBU prior to an AC power outage (the PSU was in queue for any reason) then the PSU should go into battery backup. Once the AC power outage is over, the PSU shall return back

to AC power, the BBU SoH signal will change from low to high – assuming a battery test was preformed (the BBU will try to use the discharge data to figure out if the data is valid of not) – and will ask to be checked again in 90 days.

23.1.3 Stop_Discharge

- If Stop_Discharge is asserted low, the PSU shall ignore it for the first 15 seconds of the backup, if the signal is still low at 16 seconds, then the PSU shall stop discharging the BBU. After the initial 15 seconds, the persistence delay of the Stop_Discharge signal shall change to one second.
- If one of the Stop_Discharge signals is low for any of the three BBUs then it should block itself, and the other BBUs, from performing a SoH check.

23.1.4 Sleep

- If the BBU has the sleep signal high that means the BBU is gone into sleep mode. The PSU shall not use that BBU during an AC power outage/self-test.
- If one of the sleep signals is high for any of the three BBUs then it should block itself, and the other BBUs, from performing a SoH check.
- If during a discharge/charging if the BBU asserts the sleep signal high the PSU shall stop discharging/charging the BBU after one second.

23.1.5 End of Life

- If one of the EoL signals is low for any of the three BBUs then it should block itself, and the other BBUs, from performing a SoH check.
- Otherwise the EoL signal being low shall not affect the definition or behavior of the PSU as defined earlier.

23.1.6 Fail

- If the BBU has the fail signal low, it means the BBU has failed. The PSU shall not use that BBU during an AC outage/self-test (one-second persistence delay)
- If one of the fail signals is low for any of the three BBUs then it should block itself, and the other BBUs, from performing a SoH check.

23.1.7 Protection

- This signal is ORed together with the analog 2.154V voltage reading and will turn off the driver to the step-up converter MOSFETS.
- If one of the protection signals is low for any of the three BBUs then it should block itself, and the other BBUs, from performing a SoH check.

23.1.8 Insert

- Signal is always low when the BBU is physically installed in the shelf.
- This signal can be used to figure out if the BBU is inserted or not.

- If one of the insert signals is high for any of the three BBUs then it should block the other BBUs from performing a SoH check.

23.2 Protection Levels for start up

Protection Cell Value	**Protection Pack Value**	**Value read location**	**BBU Action**	**PSU Response Delay**	**PSU Action**	**Alarm Cleared**
2.6V	33.8V	BBU Sense Lines	BBU will assert a low Stop_Discharge signal	The first 15 seconds of the backup, then one second thereafter	Turn off the step-up converter and do not discharge from the BBU	BBU will charge back up (temperature has to be in range for charging)
2.45V	31.85V	BBU Sense Lines	-	The first 15 seconds of the backup, then one second thereafter	Turn off the step-up converter and do not discharge from the BBU. The step-up controller shall not turn back on until AC returns (regardless if SoH is low). The GREEN LED CHANGES TO YELLOW AND REDUNDANCY_LOST_L signal is asserted	Step up will activate once the next AC outage happens. In the meantime the BBU should start charging.
2.154V	28V	BBU Sense Lines	-	100ms	Shutdown of step-up converter MOSFET drivers	Once the voltage reaches 43Vdc at the sense lines, the protection shall be cleared.
N/A	N/A		Protection Signal	Immediate	Immediate shutdown of step-up converter MOSFET drivers	
2.0	26V	Internal in BBU	Fail Signal asserted LOW	1 Second	Stop charging or discharging. Do not perform a battery test on another BBU in the meantime.	

1.77Vdc	25-23V	3+3 blade connectors		Immediate	Under voltage protection of step-up converter	

RS485 Communication Manual for V2 Power Shelf

24 Introduction

This manual describes the communication protocol implemented in the Open Rack V2 project; to be used with the Rack Monitor and Power Shelf V2.

25 Data Link Layer

25.1 Standard and protocol

Open Rack V2 utilizes the RS485 standard for communication between the power supplies residing in a Power Shelf and a Rack Monitor.

MODBUS is the serial communication protocol to be used with this standard.

All aspects of the MODBUS protocol are to follow the MODBUS Organization specifications and implementation guides, namely the reference documents below:

[1]: MODBUS Serial Line Protocol and Implementation Guide V1.02
[2]: MODBUS Protocol Specification (MODBUS APPLICATION PROTOCOL SPECIFICATION V1.1b)

There will be exceptions granted if the hardware does not allow for the use of required transmission (MSB vs LSB). However, the transmission across products and vendors must remain as stated in this document

The protocol is a half duplex Master/Slave. The rack monitor is always the Master and has complete, unidirectional control over the Slaves. Power supplies and other devices are considered slaves in this arrangement.

The unicast protocol mode is to be implemented. This means that the Master always addresses one node only at a given time. Broadcast mode is not allowed in this communication scheme. There is only one master in the system. Slaves do not initiate communication to the Master or other Slaves.

25.1.1 MODBUS Transaction state diagram

The figure below outlines the transaction state diagram between the Master (Rackmon) and Slaves along with exception to be thrown where appropriate.

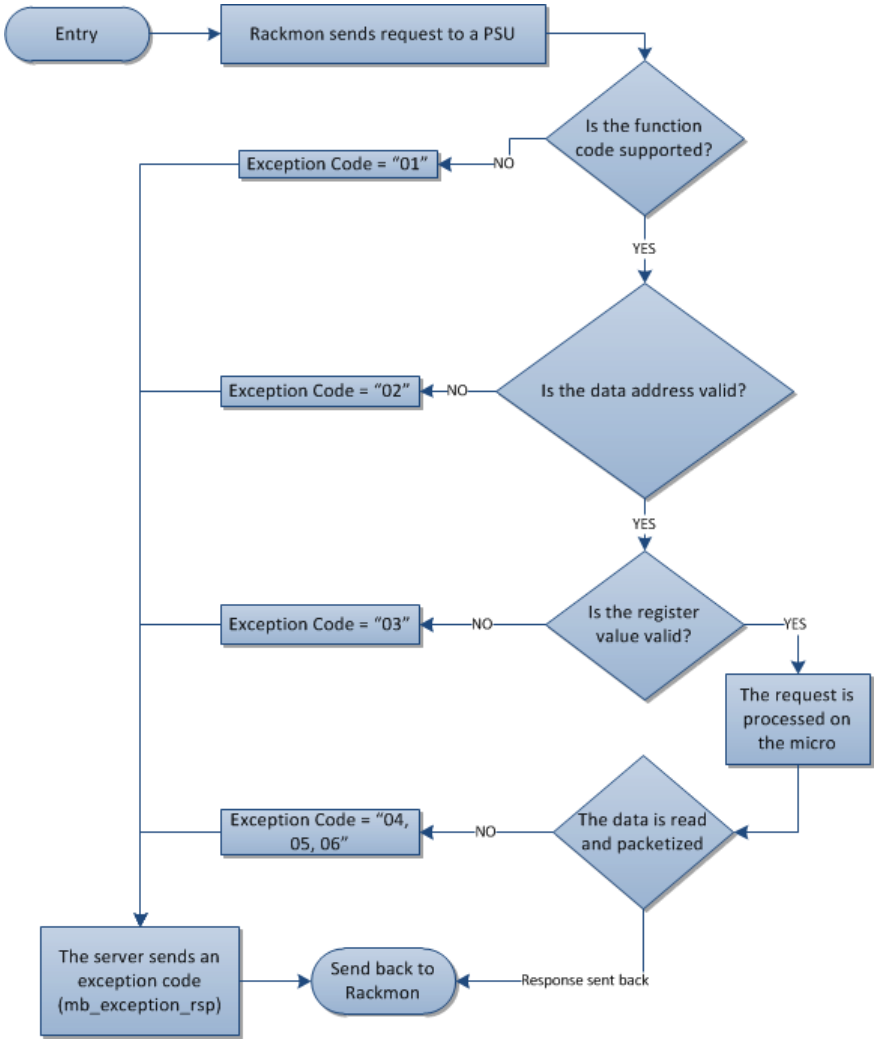


Figure 15: Transaction State diagram

26 Hardware Interface

Up to three racks can be connected to one system monitor. In each rack, there can be at most two power shelves; each power shelf houses three power supplies. All Slaves are to have their own unique address.

To accommodate for such addressing, without allowing broadcast mode, the following structure is to be used to give each power supply a unique address, for up to 18 power supplies.

26.1 Addressing

Slave addresses are reserved for 0x01 to 0xF7.

Each power supply will have an address in the following format:

Table 4: Power Supply address format

Format	Rack	Rack	Shelf	PSU	PSU
0b101	X1	X2	Y	Z1	Z2

Where X, Y and Z indicate the rack, shelf and PSU position respectively.

The five address lines above indicate the position of a power supply. The following tables demonstrate this addressing scheme:

Shelf 2			Shelf 2			Shelf 2		
PSU 1	PSU 2	PSU 3	PSU 1	PSU 2	PSU 3	PSU 1	PSU 2	PSU 3
Shelf 1			Shelf 1			Shelf 1		
PSU 1	PSU 2	PSU 3	PSU 1	PSU 2	PSU 3	PSU 1	PSU 2	PSU 3
Rack 1			Rack 2			Rack 3		

Figure 16: Slave arrangements

Table 5: PSU position address

Power Supply Position	Z1	Z2	Address
PSU 1	0	0	0b101xxy00
PSU 2	0	1	0b101xxy01
PSU 3	1	0	0b101xxy10

Table 6: Shelf position address

Shelf Position	Y	Address
Shelf 1	0	0b101xx0zz
Shelf 2	1	0b101xx1zz

Table 7: Rack position address

Rack Position	X1	X2	Address
Rack 1	0	0	0b10100yzz
Rack 2	0	1	0b10101yzz
Rack 3	1	0	0b10110yzz

Table 8: Example of full addressing

	Rack	Shelf	PSU	Address
Example 1	1	2	3	0b10100110
Example 2	2	1	1	0b10101000

All power supplies must have HIGH signals (or 1s) for Shelf Position and Rack Position addresses. These high signals are brought to ground inside the Open Rack DC PDU for Shelf position and inside the Rack monitor for Rack position. The ground is the system isolated GND inside the power supply, which is ultimately shorted with the Rack Monitor's ground (Figure 17).

NOTE: A three racks to one Rack Monitor configuration may not be used. The addressing is not affected in that case.

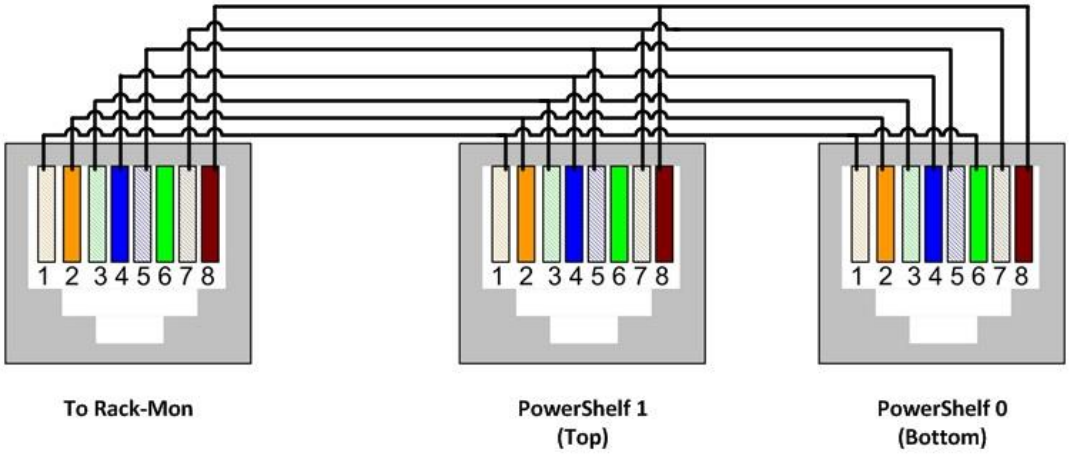


Figure 17: DC PDU addressing Shelf position in a Rack

26.1.1 Message Frame

The message frame follows a standard MODBUS RTU frame format:

Table 9: Message Frame

Start	Address	Function	Data	CRC	End
≥3.5 Bytes	1 Byte	1 Byte	0-32 Bytes	2 Bytes	≥3.5 Bytes

Parameter	Description
Bit Rate	19.2 kbps (The speed may be increased at PVT)
Bits per Byte	1 Start Bit
	8 Data Bits (LSB sent first)
	1 Parity Bit (Even)
	1 Stop Bit
Address	Slave Address (0x01 to 0xF7)
Function	Refer to Table 7

Data	Read request: 4 bytes Write request 1-32 bytes Read/Write request is determined by the number of Bytes received
CRC	Refer to reference 1, section 2.5.1.2
Start/End	At least 3.5 Bytes
Reply Timeout	1 sec

26.1.2 MODBUS Functions

A subset of the standard MODBUS functions will be used. All functions that are not defined will return an exception code.

Table 10: Function Table

Function Name	Type	Comments	Code	Notes
Read Holding register	R	Read register	0x03	Required
Read input register	R	Read register	0x04	Required
Write Single Register	W	Write register	0x06	Required but will fail on all read only registers
Write multiple register	W	Write multiple registers	0x10	Optional but will fail if not properly implemented
Read File Record	R	May be used by vendor for Firmware update, etc.	0x14	Optional but will fail if not properly implemented
Write File Record	W	May be used by vendor for Firmware update, etc.	0x15	Optional but will fail if not properly implemented
Bit masked Write register	W	Write only unmasked bits in a register	0x16	Optional but will fail if not properly implemented
R/W multiple	R/W	Read a register and write many registers at once	0x17	Optional but will fail if not properly implemented

Encapsulated Transport	NA	May be used by vendor for Firmware update, etc.	0x2B	Optional but will fail if not properly implemented
Vendor defined functions	N/A	May be used by vendor for Firmware update, etc.	0x41 to 0x48	Optional but will fail if not properly implemented

26.1.2.1 3.3.1Code example:

```
switch(function_code){
  case 0x03 :
    read_register(Frame_Data);
    break;
  case 0x04 /** same code can be used for both read functions **/
    read_register(Frame_Data);
    break;
   case etc : /** other implemented functions **/
  case 0x2B :
    Fail_response(unimplmented);
    break;

  /* you can have any number of case statements */
  default : /* Optional */
    Fail_response(unsupported_function_code);
}
```

26.1.3 Read Holding Register

The (0x03) function code is to be implemented per state diagram below; extracted from the [2]MODBUS protocol Specification V1.1b, Section 6.3.

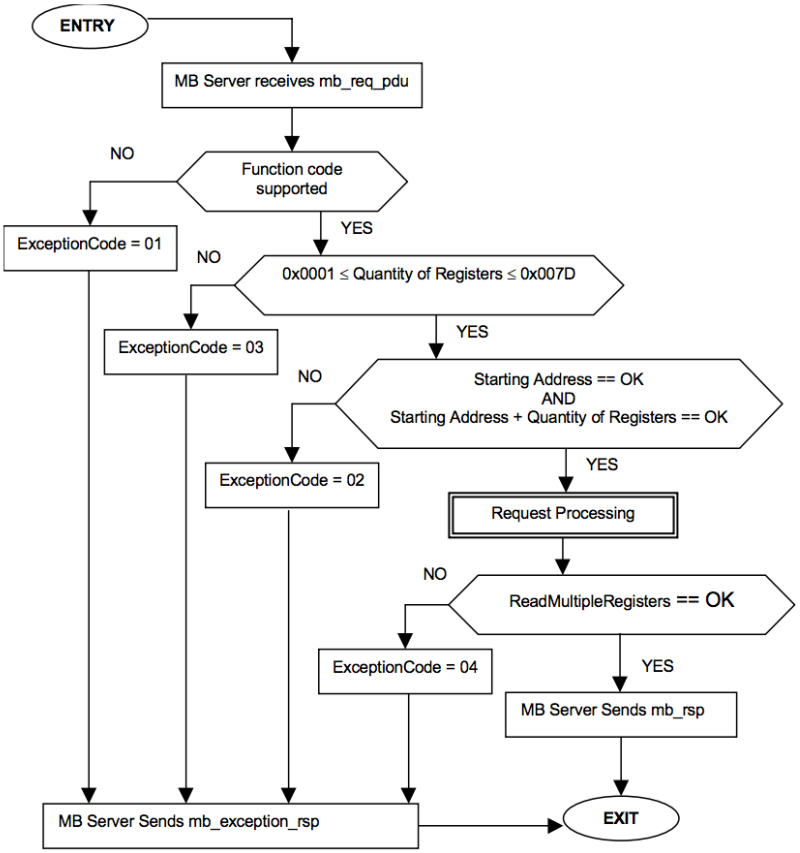


Figure 18: Read holding Register state diagram

26.1.4 Register Mapping

The two types of registers – Holding and Input – will be mapped to the same memory space. A read of a holding register at address X will return the same result as a read of an input register at address X. Writes will only be allowed to writable registers. All attempts to write to read only registers will result in a normal exception (Section 7, [2] MODBUS Protocol Specification V1.1b).

26.1.5 Two Wire MODBUS implementation

This serial communication is implemented on a two-wire interface in accordance with EIA/TIA-485. In this two-wire implementation only one Master-Slave (driver) pair can transmit.

In addition to the two transmit wires. A reference ground will be available on pin 1.

Since this system is used locally within a rack, the wire length is under 2.5meters. The number of slaves will be limited to the number of power supplies used: six per rack. Also, considering the baud rate of the system, no termination is required at this time.

NOTE: Termination may be introduced if necessary at DVT, PVT.

The unit load of each device will be ¼ units or less.

The Master and Slaves will utilize RJ45 connectors and twisted Cat-5 cable to accommodate for the two-wire system. Other extra pins on the cable and connector will be used for addressing purposes.

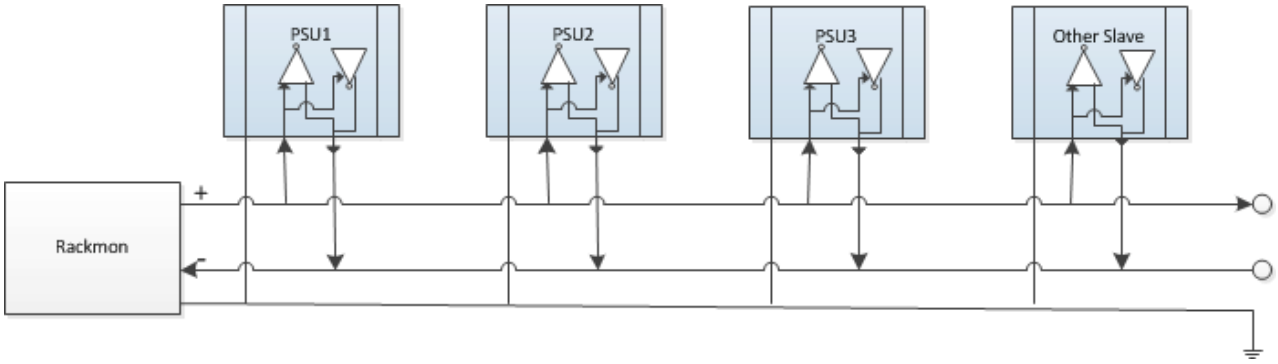


Figure 19: Two-wire implementation
The pin out is as follows (using the TIA-568-B wire coloring):

Table 11: RJ45 Connector pin-out

Pin	Wire color	Function
1	White/Orange	GND
2	Orange	PWR_OK
3	White/Green	BKP_RED
4	Blue	+RS-485 A
5	White/Blue	- RS-485 B
6	Green	Shelf Position
7	White/Brown	Rack Position
8	Brown	Rack Position

Table 12: Register Definitions

Hex Address	Size in byte	R/RW	Data	Description of data	Encoding	Format (Example)
0x00*	16	R	MFR_MODEL	16 bytes of ASCII	ASCII	
0x10*	16	R	MFR_DATE	16 bytes of ASCII	ASCII	WW/YYYY (48/2010)

0x20*	16	R	FB part#	16 bytes of ASCII	ASCII	######## (03000280)
0x30*	8	R	HW Revision	8 bytes of ASCII	ASCII	ZZZ (0AA)
0x38*	8	R	FW Revision	8 bytes of ASCII	ASCII	ZZZ (001)
0x40*	32	R	MFR_SERIAL	32 bytes of ASCII	ASCII	SSSSS (123456)
0x60*	8	R	Workorder #	8 bytes of ASCII	ASCII	XXXXXXX X
0x68	2	R	PSU Status register	2 byte register	Bit mapped per failure (Table 13)	
0x69	2	R	Battery Status register	2 byte register	Bit mapped per failure (Table 14)	
0x6A	20			Reserved		
0x80	2	R	Input Voltage AC	2bytes	2's comp+sign N=6	
0x81				Reserved		
0x82	2	R	Input Current AC	2bytes	2's comp+sign N=10	
0x83				Reserved		
0x84	2	R	Battery Voltage	2bytes	2's comp+sign N=9	
0x85				Reserved		
0x86	2	R	Battery Current output	2bytes	2's comp+sign N=8	
0x87				Reserved		
0x88	2	R	Battery Current Input	2bytes	2's comp+sign N=12	
0x89				Reserved		
0x8A	2	R	Output Voltage (main converter)	2bytes	2's comp+sign N=11	

0x8B				Reserved		
0x8C	2	R	Output Current (main converter)	2bytes	2's comp+sign N=6	
0x8B				Reserved		
0x8E	2	R	IT load Voltage Output	2bytes	2's comp+sign N=9	
0x8F				Reserved		
0x90	2	R	IT load Current Output	2bytes	2's comp+sign N=l2	
0x9l				Reserved		
0x92	2	R	Bulk Cap Voltage	2bytes	2's comp+sign N=6	
0x93				Reserved		
0x94	2	R	Input Power	2bytes	2's comp+sign N=3	
0x95				Reserved		
0x96	2	R	Output Power	2bytes	2's comp+sign N=3	
0x97				Reserved		
0x98	2	R	RPM fan0	2bytes	Decimal	
0x99				Reserved		
0x9A	2	R	RPM fanl	2bytes	Decimal	
0x9B				Reserved		
~~0x9C~~	~~2~~	~~RW~~	~~Set fan speed~~	~~2bytes~~	~~Decimal~~	
0x9D				Reserved		
0x9E	2	R	Temp0	2bytes	2's comp+sign N=7	
0x9F				Reserved		

0xA0	2	R	Temp1	2bytes	2's comp+sign N=7	
<…>				Reserved		
0xD0	2				Bit mapped per failure	
0xD1	2				Bit mapped per failure	
0xD2	2				Bit mapped per failure	
0xD3	2				Bit mapped per failure	
0xD4	2				Bit mapped per failure	
0xD5	2				Bit mapped per failure	
0xD6				Reserved		
0xD7	2				Bit mapped per failure	
0xD8	2				Bit mapped per failure	

26.1.6 Register memory map for Slaves

Note: ‘Format (Example)’ to be finalized based on accuracy and across products

* Registers to be used as required based on the ASCII length

26.1.6.1 Example of 2’s compliment encoding

$$Y = \frac{X}{2^N} \quad 277volts = \frac{17728}{2^6}$$

Where Y is the real world measurement expressed in an integer. 277 Volts displayed to the user by the application run on the Master device.

X is the decimal representation of the binary number held in the register. 17728 in binary is 0100010101000000. The leftmost bit is the most significant and is 0 therefore it is a positive number.

N is the sign magnitude. This is specified in the table above (N=6 for Input Voltage AC).

26.1.6.2 Status Register encoding

Subsystem failure occurs when a bit is set to 1

Table 13: PSU Register Encoding

0x68	Bit	Name	Description
	7		
	6		
	5		
	4		
	3		
	2		
	1		
High Byte	0	SoH Discharge	
	7	SoH Requested	
	6	Battery Alarm	Set for BBU Fail or BBU voltage =< 26 VDC
	5	Fan Alarm	
	4	Temp Alarm	Alarm set at shutdown temp
	3	Current Feed (Boost Converter) Fail	
	2	Battery Charger Fail**	
	1	Aux 54V Converter Fail	
Low Byte	0	Main Converter Fail	

** If the Battery Charger failure cannot be determined by the power supply, charger output voltage out of regulation, as allowed by the power supply spec should be used.

Table 14: BBU Register Encoding

0x69	Bit	Name	Description
High Byte	7		

	6		
	5		
	4		
	3		
	2		
	1		
	0		
	7		
	6		
	5		
	4		
	3		
	2	End of Life	
	1	Low Voltage	BBU Voltage =< 33.8
Low Byte	0	BBU Fail	

Table 15: General Alarm Register Encoding

0xD0	Bit	Name	Description
	7		
	6		
	5		
	4		
High Byte	3		

	2		
	1		
	0		
	7	Com	
	6	Fan	
	5	Temp	
	4	BC	
	3	Auxiliary	
	2	CF	
	1	LLC	
Low Byte	0	PFC	

Table 16: PFC Alarm Register Encoding

0xD1	Bit	Name	Description
	7		
	6		
	5		
	4		
	3	LLC Enabled	
	2	Input Relay on	
	1	!(Bulk_OK)	
High Byte	0	AC_OK	AC_OK
Low Byte	7		

	6		
	5		
	4		
	3		
	2		
	1	OVP	AC input over voltage protection asserted
	0	UVP	AC input under voltage protection asserted

Table 17: LLC Alarm Register Encoding

0xD2	Bit	Name	Description
	7		
	6		
	5		
	4		
	3		
	2	Oring Fail	
	1	2ndary DSP Failure	
High Byte	0	DC/DC failure	
	7		
	6		
	5		
Low Byte	4		

	3		
	2	OCP	Output Over Current protection asserted
	1	OVP	Output Over Voltage protection asserted
	0	UVP	Output Under Voltage protection asserted

Table 18: Current Feed Alarm Register Encoding

0xD3	Bit	Name	Description
	7		
	6		
	5		
	4		
	3		
	2		
	1		
High Byte	0	CF Failure	Failure with CF
	7		
	6		
	5		
	4	OPP	Over Power Protection (more than 4200W input to CF)
	3	Battery_UVP	
Low Byte	2	Battery_OVP	

	1	Bulk_UVP	
	0	Bulk_OVP	

Table 19: Auxiliary Alarm Register Encoding

0xD4	Bit	Name	Description
High Byte	7		
	6		
	5		
	4		
	3		
	2		
	1		
	0	Aux alarm	Failure with auxiliary converter
Low Byte	7		
	6		
	5		
	4		
	3		
	2	OCP	Over Current Protection asserted
	1	OVP	Output Over Voltage protection asserted
	0	UVP	Output Under Voltage Protection asserted

Table 20: Battery Charger Alarm Register Encoding

0xD5	Bit	Name	Description
	7		
	6		
	5		
	4		
	3		
	2		
	1		
High Byte	0	Charger alarm	Charger failure
	7		
	6		
	5		
	4		
	3		
	2	Timeout alarm	Charger ON for more than 5hrs
	1	UVP	Output Under Voltage Protection asserted
Low Byte	0	OVP	Output Overvoltage Protection asserted

Table 21: Temperature Alarm Register Encoding

0xD7	Bit	Name	Description
	7		
High Byte	6		

	5		
	4		
	3		
	2		
	1		
	0		
	7	PFC temp alarm	
	6	LLC temp alarm	
	5	CF temp alarm	
	4	Aux temp alarm	
	3	Sync Rectifier temp alarm	
	2	Oring temp alarm	
	1	Inlet temp alarm	
Low Byte	0	Outlet temp alarm	

Table 22: Fan Alarm Register Encoding

0xD8	Bit	Name	Description
	7		
	6		
	5		
	4		
	3		
High Byte	2		

	1		
	0		
	7		
	6		
	5		
	4		
	3		
	2		
	1		
Low Byte	0	Fan alarm	Fan failure

Table 23: Communication Alarm Register Encoding

0xD9	Bit	Name	Description
	7		
	6		
	5		
	4		
	3		
	2		
	1		
High Byte	0		
	7		
Low Byte	6		

	5		
	4		
	3		
	2		
	1		
	0	Internal Communication alarm	Internal Communication fail