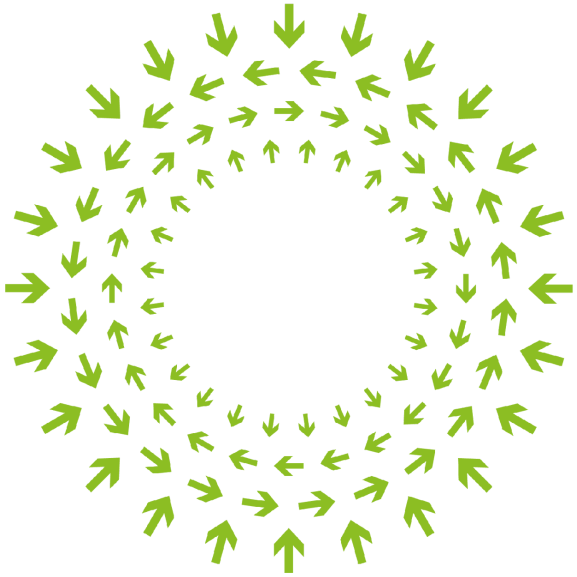

OPEN

Compute Project

APEC

Advanced PCIe Enclosure Compatible Card Specification

Revision 0.8

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2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

3. Compliance with OCP Tenets

3.1. Openness

By providing a next generation standardized connector and card format for APEC, it enables seamless interoperability between different hardware architectures, software stacks.

3.2. Efficiency

Contributes to the reduction of infrastructure costs by providing a standardized next generation PCIe connector and card format

3.3. Impact

APEC is already being adopted in infrastructure, and our proposed standardization approach aims to preserve this investment while advancing the state of PCIe capability in the future. By defining a common APEC standard, we aim to enable APEC through a global supply chain, achieving the transformative impact that the Open Compute Project seeks.

3.4. Scale

With the exponential growth in AI systems and servers globally in the next five years, it's crucial to have PCIe connector and card format that support the increasing bandwidth, lane count, power and management diversity of high volume production. Our contribution meets this scale tenet by defining a common next generation connector and card format that enables adoption of new technology through a global supply channel, accelerates time-to-market advantage of technology, and supports ongoing innovation as well as legacy infrastructure.

3.5. Sustainability

The specification minimizes the compute intensity by enabling more efficient communication and computation between the increasing array of NIC, accelerators, etc. that are common in data centers. By ensuring that there is a clear common connector and card formats, the APEC

specification can help reduce the need for additional hardware and tooling and thereby limit the environmental impact of data centers.

4. Change Log

Date	Version #	Author	Description
30Sept2024	0.8	Rick Roy	initial OCP submission
2024-10-01	0.9	joeh@	Edit for release

5. Scope

APEC - (Advanced PCIe Enclosure Compatible)

This specification covers the requirements of the APEC electrical, mechanical interconnect, and associated interfaces.

The intent of this specification is to specify the electrical and mechanical aspects required to address the signal interconnect and power delivery of add-in cards, utilizing the APEC interface assembly.

- APEC is capable of meeting/exceeding PCIe Gen6 data transfer rate in a reliable, repeatable, robust, and scalable manner.
- APEC connector comes in two specified versions:
    - DLF (Direct Lead Frame)
    - SMT (Surface Mount Technology)
- APEC assemblies may be configured as a PCIe Endpoint, a Root Port, or a hybrid Endpoint and Root Port.

The larger system aspects of power delivery, signal fidelity, and thermal management are out of scope for this document.

The following are included in the scope of this specification:

- General
    - PCIe Gen 6 capability

    - x32 PCIe lane
    - Management
    - Power delivery
- APEC connector
    - Mechanical
    - Electrical (signal and power)
    - Functional
- APEC connector PCBA mounting
    - Mechanical
    - Electrical
- APEC card
    - Mechanical
    - Electrical

6. Terms

The table below defines terms used in this specification.

Term	Definition
x1, x2, x4, x8, x16, x32	Refers to PCI Express Lane of basic bandwidth. For example: x4 refers to a collection of four PCI Express Lanes and is typically read as “by four.”
Add-in Card, AIC	A card that is plugged into a connector and mounted in a chassis slot.
APEC	Advanced PCIe Enclosure Compatible
Auxiliary signals	Signals, some of which are defined in the PCI Express Base Specification, that are used along with PCI Express signaling. Some are necessary for basic PCI Express operation (e.g., reference clock and reset), while others provide ancillary capabilities (e.g., the SMBus signals). See also **Sideband signaling.**
Card	An Add-in Card that is plugged into a connector and mounted in a chassis slot.
DLF	Direct Lead Frame
DownStream	Generally refers to external links and connections that are commanded and controlled.
DUT	Device Under Test

Endpoint	A device that resides as the target and implements a single Upstream Port toward the Root Port.
Host	Typically, the motherboard or baseboard mounting the CEM Slot Connector. A riser card and connector are considered part of the host, by extension.
Hot Plug	Hot insertion and/or hot removal of a card into an active backplane or system board as defined in PCI Express Base Specification
Lane	A differential TX and RX pair carrying PCI Express high-speed data. TX and RX are from the perspective of the root port.
Link	A collection of one or more PCI Express Lanes.
REFCLK	The reference clock differential pair consists of auxiliary signals REFCLKp and REFCLKn
Root Port	A PCIe controller that serves as the entry and exit point for all PCIe traffic within a PCIe topology.
Sideband signaling	A method for signaling events and conditions using physical signals separate from signals forming the Link between two components. See also Auxiliary signals.
SMT	Surface Mount Technology
Sustained Power	Average power in a 1 second or greater timeframe.
TDP	Thermal Design Power: maximum sustained power.
TIM	Thermal Interface Materials.
UpStream	Generally refers to the links and connections that accept commands and control from an external device.
UUT	Unit Under Test
WAKE	A mechanism used by a component to request the reapplication of main power when in the L2 Link state. Two such mechanisms are defined in the PCI Express Base Specification: **Beacon** and **WAKE#**. This specification requires the use of WAKE# on any Add-in Card or system board that supports wakeup functionality.

7. Reference Documents

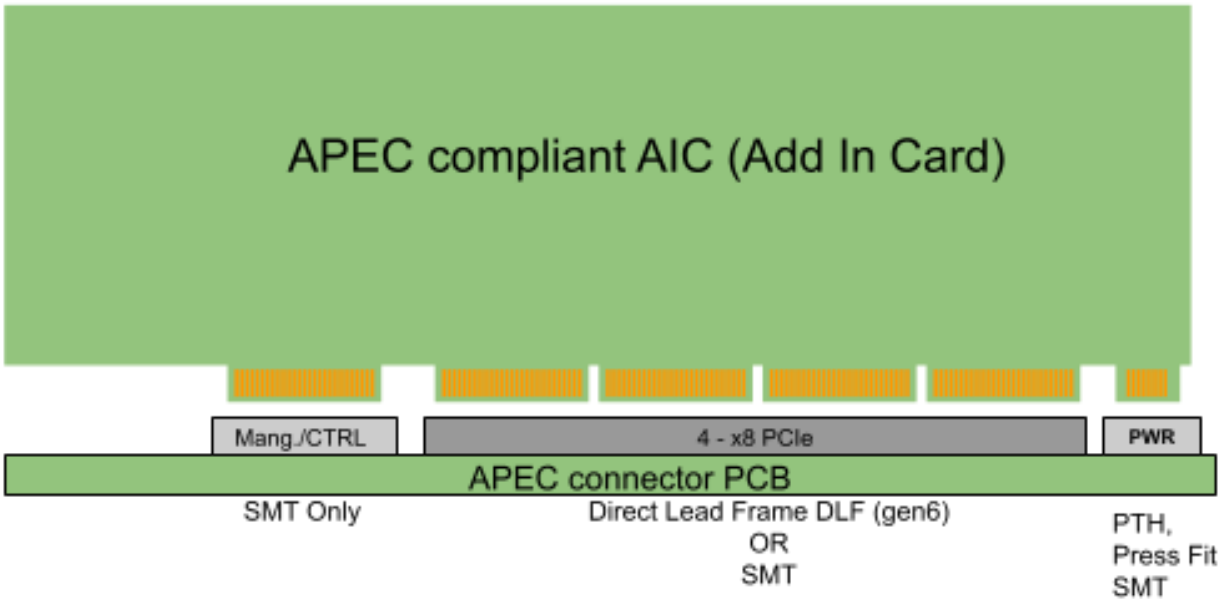
- PCI Express Base Specification Revision 6.0
- PCI Express Jitter modeling - very lightweight
- SMBus Specification
- IEEE 1149.1 JTAG
- APEC Pinout

8. Overview

APEC is a card and connector system with a PCIe interface supporting up to PCIe Gen 6 (64GT/s per lane or 128GB/s for a x16 link width).

9. Electrical

PCIe TX and RX electrical requirements are specified in the PCIe Base Specification. Functional layout is provided in the following illustration.



APEC 3 piece connector solution

The table below lists supported configurations.

Support Configurations	Management/CTRL	32 PCIe lanes 4 - x8 PCIe	Power
PCIe gen[6..1]	SMT	DLF	SMT,PTH,PF
PCIe gen[5..1]	SMT	SMT	SMT,PTH,PF

10. APEC Assembly

APEC assembly with Add-in Card (AIC) and paddleboard is shown. AIC is shown with a retention bracket and installed into APEC paddleboard adapter through an SMT connector.

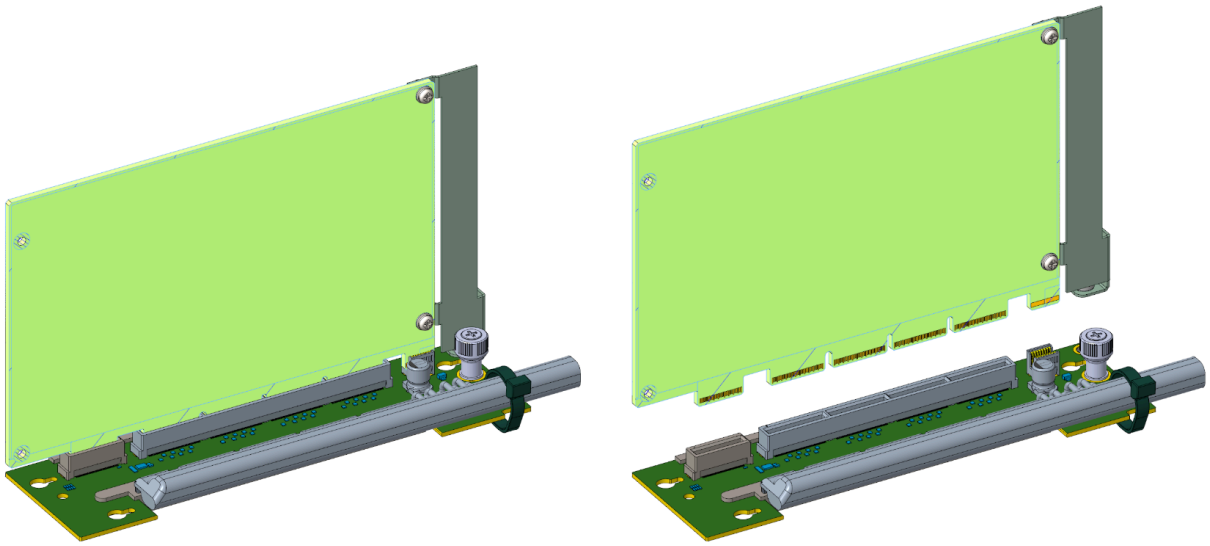


Figure: APEC Assembly

11. APEC Signal Grouping

APEC signals are grouped into three functional sections:

- 32 Lane PCIe Connector section
- Management and Control section
- Power section

See reference drawing.

11.1. 32-Lane PCIe Connector Section

The following signals are included as part of the APEC specification and may be required for a configuration use case.

- APEC PCIe SerDes signals
    - Primary PCIe signaling
        - PETn/p,PERn/p up to 32 lanes
        - Full sideband support at a x8 lane basis
        - PCIe link width and number of controllers available are dependent on the Root Port controller(s).
    - TX and RX are from the perspective of the Root port.
        - Each instance will need to review connector schematic and PCB CAD symbols to ensure intended connectivity.
- Reference Clock, REFCLKp/REFCLKn
    - Requirements for REFCLK in a system are defined in the PCI Express Base Specification. A system board must provide a reference clock that meets all requirements for the common clock architecture as defined for the reference clock in the PCI Express Base Specification.
    - Two APEC modes: Endpoint and Root Port
        - Endpoint: One REFCLK pair input per x8 PCIe connectivity defined
        - Root Port: One REFCLK pair output defined
- Presence detect, PRSNT#
        - Add-in Card or cable presence detect pin.
        - If implemented, the PCI Express Hot Plug controller on the system board detects the presence of an Add-in Card or cable using the PRSNT# signal. It is the responsibility of the port connected to the APEC interface to determine the presence of the Add-in Card or cable and set the presence detected bits in the appropriate register as described in Chapter 7 of the PCI Express Base Specification.
- PCIe Reset, PERST#

    - Indicates when the power is active and stable. PERST# is in the inactive state after a delay of Tpvperl time from the power rails achieving specified tolerance on power up. See PCI Express Base specification.
    - The PERST# signal also initializes a component's state machines and other logic once power supplies stabilize. On power-up, the de-assertion of PERST# is delayed 100 ms (Tpvperl) after power is indicated stable. Reference clocks (REFCLKp, REFCLKn) are to become stable before PERST# is de-asserted. PERST# is asserted in advance of the power being switched off in a power-managed state like S3. PERST# is asserted when the power supply is powered down, but without the advanced warning of the transition.
- I2C, I3C, USB
    - Dedicated per x8 PCIe primary section.
    - I2C follows historical PCIe CEM use.
    - I3C and USB dedicated pins allow for APEC optionality.

11.2. Management and Control Connector Section

- Auxiliary PCIe option
    - PET_AUXn/p, PER_AUXn/p - 1 lane link width
    - Dedicated APEC x1 Root Port
- JTAG (TDI, TDO, TCK, TMS, TRST#)
    - IEEE Standard 1149.1
    - All TAP JTAG signals are intended to be from the perspective of the add-in card.
        - One must check connectivity intent with respect to APEC connector naming convention.
- OOB management ()
    - NCSI connectivity via SGMII TX/RX
        - APEC dedicates a pair of TX pins and RX pins to SGMII interconnect intended for NCSI NIC-to-BMC communication.
    - Alternate NCSI connection via USB
        - If SGMII is not utilized for NIC to BMC communication, USB is made available.
            - SGMII TX → USB2 DATAp, and DATAn
            - SGMII RX → unused
        - There are no plans to support USB3.x
    - 3.3V_STBY
        - 3.3V is to be supplied for any/all standby, PROM, FRU identification, etc.
            - 3.3V current is limited to 2A maximum.

11.3. Power Connector Section

- Dedicated power section

    - 12V OR 54V
        - Mechanically keyed to prevent inadvertent use.
    - APEC cards are expected to perform all necessary DC/DC conversion from 12V or 54V (with the exception of the dedicated 3.3V standby supplied on the Management/Control connector section)

12. Clocking

- Reference Clock requirements and guidance
    - Requirements for REFCLKp/n are defined in the PCI Express Base Specification.
    - The reference clock pair is routed point-to-point. All appropriate SI constraints must be met to satisfy the PCI Express Base Specification requirements.
- Spread Spectrum Clocking, SSC
    - May be required to meet EMC compliance.
    - The requirements for spread spectrum modulation rate and magnitude are given in the PCI Express Base Specification.
    - EMI emissions will be reduced if unused clocks are disabled at the clock source.

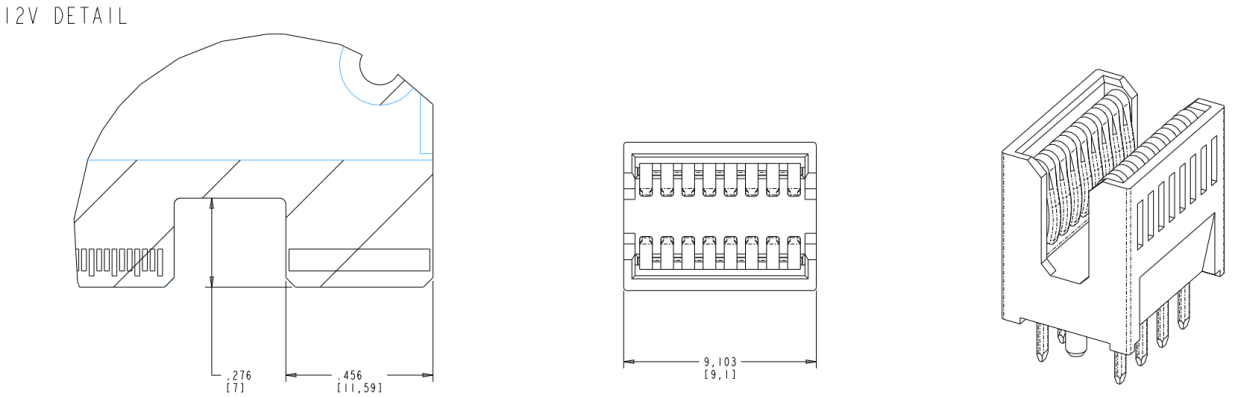
The table below presents the Reference Clock's Supported Architecture

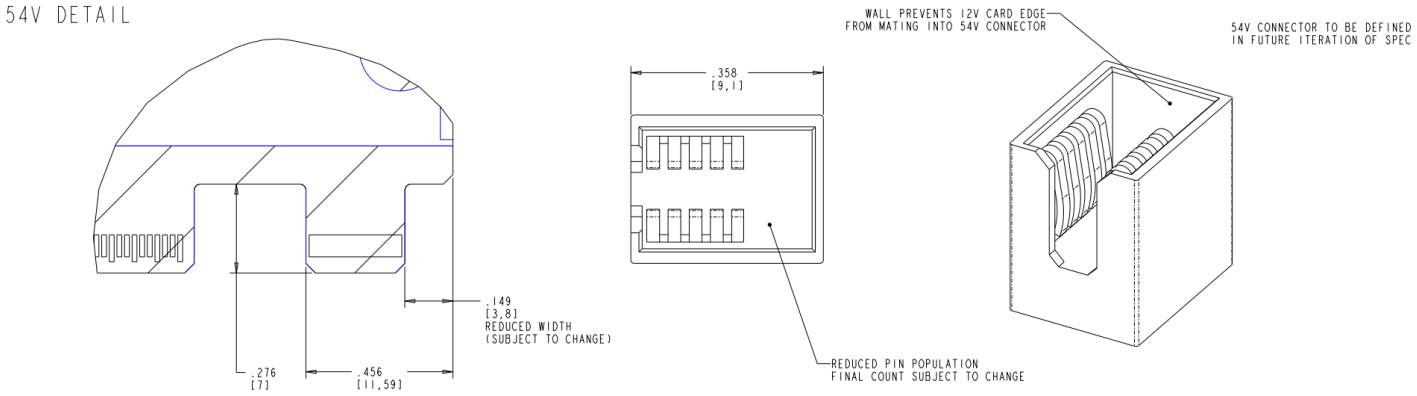
System Arch.	Server PCBA	Card/cable w/o retimer	Card/cable w/ retimer
Common Clock	Required	Required (internal)	Required (internal)
SRIS	Not part of APEC	Not part of APEC	Optional
SRNS	Not part of APEC	Not part of APEC	Optional

13. APEC Power Supply Rail Requirements

APEC interface supports either 12V OR 54V input voltage.

- The APEC power connector physical location defines 12V OR 54V operation.
    - 12V and 54V power options shall require the support of two different power connectors
    - To prevent improper assembly of 12V APEC cards into 54V APEC connectors, 54V PWR connectors shall be keyed to prevent mating of 12V APEC cards and 54V APEC cards shall have power card edges reduced in width (final width subject to change) to enable this. 54V connector design will be updated in a future revision. See drawing:





- Simultaneous 12V and 54V connectivity is NOT allowed
- APEC devices are responsible for converting and regulating voltage as needed for the 12V or 54V input.

APEC connector input current rating.

- APEC power connector consists of power/return pairs rated at maximum 34A per connector. *54V current artificially reduced to 21A viaprotective keying.
- APEC power consumption as an endpoint is conservatively defined as shown below.

+12V	+54V
+12V +/- 8%, 34A max, [375/400/440W]	+54V +10%, -25%, 21A max, [>800W]

APEC power delivery as a Root Port.

- All APEC connected endpoints must supply and regulate their own power

14. Supported Configurations

Term	Definition	Note
End Point	1 - x32	*Uncommon today, but can be supported*
	2 - x16	
	4 - x8	
	8 - x4	*Must use Independent Clock*
	8 - x1, x2	*Must use at a x4 increment*
Root Port	1 - x1	*Dedicated “AUX” x1 root port*
	8 - x4	
Endpoint + Root Port	1 - x16 EP + 4 - x4 RP	
Any EP + Any RP		*Any combination of EP + RP can accommodate up to a total of 32 lanes plus one single lane.*

14.1. APEC Pin Definition

The table below defines APEC gold finger pins.

Signal Category	Signal/ Netnames	Pin number	Baseboard direction	Example
Power	GND	APWR[1:8]	Input	Reference and return
Power	+12V, +54V	BPWR[1:8]	Input	Source
Power	3.3V_STBY	ACTRL_27, BCTRL_27	Input	Source
Control	WAKE#, PWRBRK#,	BCTRL_14, BCTRL_4	Input	Optional
PCIe	PERp0/PERn0 PERp1/PERn1 PERp2/PERn2 PERp3/PERn3 PERp4/PERn4 PERp5/PERn5 PERp6/PERn6 PERp7/PERn7 PERp8/PERn8 PERp9/PERn9 PERp10/PERn10 PERp11/PERn11 PER12/PERn12 PERp13/PERn13 PERp14/PERn14 PERp15/PERn15 PERp16/PERn16 PERp17/PERn17 PERp18/PERn18 PERp19/PERn19 PERp20/PERn20 PERp21/PERn21 PERp22/PERn22 PERp23/PERn23 PERp24/PERn24 PERp25/PERn25 PERp26/PERn26 PERp27/PERn27 PERp28/PERn28 PERp29/PERn29 PERp30/PERn30 PERp31/PERn31	A5/A6 A8/A9 A11/A12 A14/A15 A17/A18 A20/A21 A23/A24 A26/A27 A39/A40 A42/A43 A45/A46 A48/A49 A51/A52 A54/A55 A57/A58 A60/A61 A73/A74 A76/A77 A79/A80 A82/A83 A85/A86 A88/A89 A91/A92 A94/A95 A107/A108 A110/A111 A113/A114 A116/A117 A119/A120 A122/A123 A125/A126 A128/A129		

PCIe	PETp0/PETn0 PETp1/PETn1 PETp2/PETn2 PETp3/PETn3 PETp4/PETn4 PETp5/PETn5 PETp6/PETn6 PETp7/PETn7 PETp8/PETn8 PETp9/PETn9 PETp10/PETn10 PETp11/PETn11 PET12/PETn12 PETp13/PETn13 PETp14/PETn14 PETp15/PETn15 PETp16/PETn16 PETp17/PETn17 PETp18/PETn18 PETp19/PETn19 PETp20/PETn20 PETp21/PETn21 PETp22/PETn22 PETp23/PETn23 PETp24/PETn24 PETp25/PETn25 PETp26/PETn26 PETp27/PETn27 PETp28/PETn28 PETp29/PETn29 PETp30/PETn30 PETp31/PETn31	B5/B6 B8/B9 B11/B12 B14/B15 B17/B18 B20/B21 B23/B24 B26/B27 B39/B40 B42/B43 B45/B46 B48/B49 B51/B52 B54/B55 B57/B58 B60/B61 B73/B74 B76/B77 B79/B80 B82/B83 B85/B86 B88/B89 B91/B92 B94/B95 B107/B108 B110/B111 B113/B114 B116/B117 B119/B120 B122/B123 B125/B126 B128/B129		
PCIe	REFCLKn_A[] REFCLKp_A[]			
PCIe	PRST_A0#			
PCIe	PERST_A0#			
PCIe	PET_AUXp0, PET_AUXn0 PER_AUXp0, PER_AUXn0			
PCIe	REFCLKAUXp0, REFCLKAUXn0			
PCIe	PRSNTAAUX#			
PCIe	PERST1AUX#			

PCIe	Ref CLK			REFCLKn_xy REFCLpn_xy
I2C or SMB	SDA, SCL			/I2C_DATA_xy I2C_CLK_xy
I3C or SMB	SDA, SCL			I3C0DATA_xy I30CLK_xy
USB	USB_DAT0n_xy USB_DATpn_xy			USB_DAT0n_xy USB_DATpn_xy
Reserved/ JTAG	TDI, TDO, TCK, TRST, TMS			Optional
Status	PWR_Good			PWR_Good,
Status	PWR_Enable			PWR_Enable
Status	APEC_PWR_Good			APEC_PWR_Good
Status	AUX_PWR_Eable			AUX_PWR_Eable
NCSI	SGMII_RXn, SGMII_RXp SGMIITXn, SGMII_TXp			SGMII_RXn, SGMII_RXp SGMIITXn, SGMII_TXp
RESET	SYS_RESET			SYS_RESET
Control	WAKE#			
Control	PWRBRK#			
Status	Boot_drive_prsnt			Boot_drive_prsnt
Status	Card_present#			Card_present#
Mode Select	BIF[0..3]			BIF0,BIF1,BIF2,BIF3

15. APEC Pinout

The card side implementation supports up to 32 PCIe lanes. Cards may implement less than the full set of PCIe lanes (e.g. 1x16 lanes or 2x16 bifurcated lanes). The APEC pinout is shown below.

A			B		
Pin#	**Name**	**Mating**	**Mating**	**Name**	**Pin#**
APWR_8	GND	First	Second	+12V OR +54V	BPWR_8
APWR_7	GND	First	Second	+12V OR +54V	BPWR_7
APWR_6	GND	First	Second	+12V OR +54V	BPWR_6
APWR_5	GND	First	Second	+12V OR +54V	BPWR_5
APWR_4	GND	First	Second	+12V OR +54V	BPWR_4
APWR_3	GND	First	Second	+12V OR +54V	BPWR_3
APWR_2	GND	First	Second	+12V OR +54V	BPWR_2
APWR_1	GND	First	Second	+12V OR +54V	BPWR_1
A136	GND	First	First	GND	B136
A135	SMBDATA/I2C_DATA_B1	Second	Second	Reserved	B135
A134	SMBCLK/I2C_CLK_B1	Second	Second	Reserved	B134
A133	GND	First	First	GND	B133
A132	SMBDATA/I3C_DATA_B1	Second	Second	USB_DAT0n_B1	B132
A131	SMBCLK/I3C_CLK_B1	Second	Second	USB_DAT0p_B1	B131
A130	GND	First	First	GND	B130
A129	PERn31	Second	Second	PETn31	B129
A128	PERp31	Second	Second	PETp31	B128
A127	GND	First	First	GND	B127
A126	PERn30	Second	Second	PETn30	B126
A125	PERp30	Second	Second	PETp30	B125
A124	GND	First	First	GND	B124

A123	PERn29	Second	Second	PETn29	B123
A122	PERp29	Second	Second	PETp29	B122
A121	GND	First	First	GND	B121
A120	PERn28	Second	Second	PETn28	B120
A119	PERp28	Second	Second	PETp28	B119
A118	GND	First	First	GND	B118
A117	PERn27	Second	Second	PETn27	B117
A116	PERp27	Second	Second	PETp27	B116
A115	GND	First	First	GND	B115
A114	PERn26	Second	Second	PETn26	B114
A113	PERp26	Second	Second	PETp26	B113
A112	GND	First	First	GND	B112
A111	PERn25	Second	Second	PETn25	B111
A110	PERp25	Second	Second	PETp25	B110
A109	GND	First	First	GND	B109
A108	PERn24	Second	Second	PETn24	B108
A107	PERp24	Second	Second	PETp24	B107
A106	GND	First	First	GND	B106
A105	REFCLKn_B1	Second	Second	PRESENT_B1#	B105
A104	REFCLKp_B1	Second	Second	PERST_B1#	B104
A103	GND	First	First	GND	B103
Key					
A102	GND	First	First	GND	B102
A101	SMBDATA/I2C_DATA_B0	Second	Second	Reserved	B101
A100	SMBCLK/I2C_CLK_B0	Second	Second	Reserved	B100
A99	GND	First	First	GND	B99
A98	SMBDATA/I3C_DATA_B0	Second	Second	USB_DAT0n_B0	B98
A97	SMBCLK/I3C_CLK_B0	Second	Second	USB_DAT0p_B0	B97
A96	GND	First	First	GND	B96
A95	PERn23	Second	Second	PETn23	B95
A94	PERp23	Second	Second	PETp23	B94

A93	GND	First	First	GND	B93
A92	PERn22	Second	Second	PETn22	B92
A91	PERp22	Second	Second	PETp22	B91
A90	GND	First	First	GND	B90
A89	PERn21	Second	Second	PETn21	B89
A88	PERp21	Second	Second	PETp21	B88
A87	GND	First	First	GND	B87
A86	PERn20	Second	Second	PETn20	B86
A85	PERp20	Second	Second	PETp20	B85
A84	GND	First	First	GND	B84
A83	PERn19	Second	Second	PETn19	B83
A82	PERp19	Second	Second	PETp19	B82
A81	GND	First	First	GND	B81
A80	PERn18	Second	Second	PETn18	B80
A79	PERp18	Second	Second	PETp18	B79
A78	GND	First	First	GND	B78
A77	PERn17	Second	Second	PETn17	B77
A76	PERp17	Second	Second	PETp17	B76
A75	GND	First	First	GND	B75
A74	PERn16	Second	Second	PETn16	B74
A73	PERp16	Second	Second	PETp16	B73
A72	GND	First	First	GND	B72
A71	REFCLKn_B0	Second	Second	PRESENT_B0#	B71
A70	REFCLKp_B0	Second	Second	PERST_B0#	B70
A69	GND	First	First	GND	B69
Key					
A68	GND	First	First	GND	B68
A67	SMBDATA/I2C_DATA_A1	Second	Second	Reserved	B67
A66	SMBCLK/I2C_CLK_A1	Second	Second	Reserved	B66
A65	GND	First	First	GND	B65
A64	SMBDATA/I3C_DATA_A1	Second	Second	USB_DAT0n_A1	B64

A63	SMBCLK/I3C_CLK_A1	Second	Second	USB_DAT0p_A1	B63
A62	GND	First	First	GND	B62
A61	PERn15	Second	Second	PETn15	B61
A60	PERp15	Second	Second	PETp15	B60
A59	GND	First	First	GND	B59
A58	PERn14	Second	Second	PETn14	B58
A57	PERp14	Second	Second	PETp14	B57
A56	GND	First	First	GND	B56
A55	PERn13	Second	Second	PETn13	B55
A54	PERp13	Second	Second	PETp13	B54
A53	GND	First	First	GND	B53
A52	PERn12	Second	Second	PETn12	B52
A51	PERp12	Second	Second	PETp12	B51
A50	GND	First	First	GND	B50
A49	PERn11	Second	Second	PETn11	B49
A48	PERp11	Second	Second	PETp11	B48
A47	GND	First	First	GND	B47
A46	PERn10	Second	Second	PETn10	B46
A45	PERp10	Second	Second	PETp10	B45
A44	GND	First	First	GND	B44
A43	PERn9	Second	Second	PETn9	B43
A42	PERp9	Second	Second	PETp9	B42
A41	GND	First	First	GND	B41
A40	PERn8	Second	Second	PETn8	B40
A39	PERp8	Second	Second	PETp8	B39
A38	GND	First	First	GND	B38
A37	REFCLKn_A1	Second	Second	PRESENT_A1#	B37
A36	REFCLKp_A1	Second	Second	PERST_A1#	B36
A35	GND	First	First	GND	B35
Key					
A34	GND	First	First	GND	B34

A33	SMBDATA/I2C_DATA_A0	Second	Second	Reserved	B33
A32	SMBCLK/I2C_CLK_A0	Second	Second	Reserved	B32
A31	GND	First	First	GND	B31
A30	SMBDATA/I3C_DATA_A0	Second	Second	USB_DAT0n_A0	B30
A29	SMBCLK/I3C_CLK_A0	Second	Second	USB_DAT0p_A0	B29
A28	GND	First	First	GND	B28
A27	PERn7	Second	Second	PETn7	B27
A26	PERp7	Second	Second	PETp7	B26
A25	GND	First	First	GND	B25
A24	PERn6	Second	Second	PETn6	B24
A23	PERp6	Second	Second	PETp6	B23
A22	GND	First	First	GND	B22
A21	PERn5	Second	Second	PETn5	B21
A20	PERp5	Second	Second	PETp5	B20
A19	GND	First	First	GND	B19
A18	PERn4	Second	Second	PETn4	B18
A17	PERp4	Second	Second	PETp4	B17
A16	GND	First	First	GND	B16
A15	PERn3	Second	Second	PETn3	B15
A14	PERp3	Second	Second	PETp3	B14
A13	GND	First	First	GND	B13
A12	PERn2	Second	Second	PETn2	B12
A11	PERp2	Second	Second	PETp2	B11
A10	GND	First	First	GND	B10
A9	PERn1	Second	Second	PETn1	B9
A8	PERp1	Second	Second	PETp1	B8
A7	GND	First	First	GND	B7
A6	PERn0	Second	Second	PETn0	B6
A5	PERp0	Second	Second	PETp0	B5
A4	GND	First	First	GND	B4
A3	REFCLKn_A0	Second	Second	PRESENT_A0#	B3

A2	REFCLKp_A0	Second	Second	PERST_A0#	B2
A1	GND	First	First	GND	B1
ACTRL_28	GND	First	First	GND	BCTRL_28
ACTRL_27	3.3V_STBY	Second	Second	3.3V_STBY	BCTRL_27
ACTRL_26	GND	First	First	GND	BCTRL_26
ACTRL_25	PWR_Good	Second	Second	APEC_PWR_Good	BCTRL_25
ACTRL_24	PWR_Enable	Second	Second	AUX_PWR_Enable	BCTRL_24
ACTRL_23	GND	First	First	GND	BCTRL_23
ACTRL_22	SGMII_RXn	Second	Second	SGMII_TXn/USB_DAT0n_C0	BCTRL_22
ACTRL_21	SGMII_RXp	Second	Second	SGMII_TXp/USB_DAT0p_C0	BCTRL_21
ACTRL_20	GND	First	First	GND	BCTRL_20
ACTRL_19	SMBDATA/I2CDATA_OUT_C0	Second	Second	SMBDATA/I2CDATA_OUT_C1	BCTRL_19
ACTRL_18	SMBCLK/I2CCLK_OUT_C0	Second	Second	SMBCLK/I2CCLK_OUT_C1	BCTRL_18
ACTRL_17	GND	First	First	GND	BCTRL_17
ACTRL_16	Reserved (TDI)	Second	Second	Reserved (TDO)	BCTRL_16
ACTRL_15	Reserved (TCK)	Second	Second	Reserved (TRST)	BCTRL_15
ACTRL_14	Reserved (TMS)	Second	Second	Reserved (WAKE#)	BCTRL_14
ACTRL_13	GND	First	First	GND	BCTRL_13
ACTRL_12	PET_AUXn0	Second	Second	PER_AUXn0	BCTRL_12
ACTRL_11	PET_AUXp0	Second	Second	PER_AUXp0	BCTRL_11
ACTRL_10	GND	First	First	GND	BCTRL_10
ACTRL_9	REFCLKAUXn0	Second	Second	PRSNTAAUX#	BCTRL_9
ACTRL_8	REFCLKAUXp0	Second	Second	PERST1AUX#	BCTRL_8
ACTRL_7	GND	First	First	GND	BCTRL_7
ACTRL_6	SMBD_OUT/I3CDATA_OUT_C0	Second	Second	REFCLK_OUTn_C0	BCTRL_6
ACTRL_5	SMBCLK_OUT/I3CCLK_OUT_C0	Second	Second	REFCLK_OUTp_C0	BCTRL_5
ACTRL_4	BIF2	Second	Second	Reserved (PWRBRK#)	BCTRL_4

ACTRL_3	BIF0	Second	Second	BIF3	BCTRL_3
ACTRL_2	SYS_RESET	Second	Second	BIF1	BCTRL_2
ACTRL_1	Boot_drive_prsnt	Second	Second	Card_present#	BCTRL_1

16. APEC Endpoints and Root Port Guide

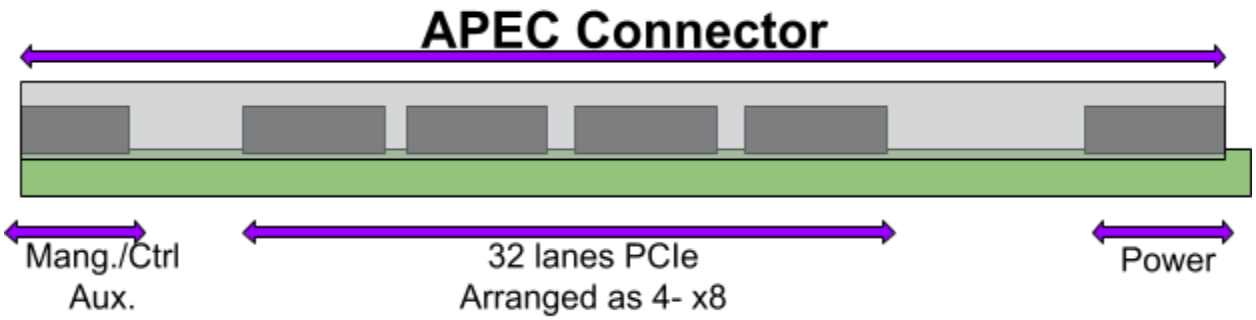


Figure: APEC Reference Drawing

Connector Section	Power	32 lanes PCIe	Aux.
End Point	n/a	Up to four sets of x8 lanes	0
Root Port	n/a	Up to 32 lanes*	1

* Side band signals must be generated for each Root port configuration.

16.1. APEC Endpoint Configuration Guidelines

- Sideband signals (PERST, PRST, I2C, I3C, USB) and CLK are available on a x8 lane link increment.
- x1, x2, x4 Lane links can be supported but use all of the x8 sideband signals; i.e, a x4 link uses full x8 sideband signal capability.
- APEC cards should provide a FRU device for each used lane configuration. Examples are presented below.

Configuration	FRU device req.	FRU attach
2 - x16	2	1x16, 1x16

4-x8	4	1x8, 1x8, 1x8, 1x8

16.2. APEC Root Port Configuration Guidelines

- There is a dedicated auxiliary x1 PCIe Root Port available within the management and control section of the APEC connector that can be used independently of the other 32 APEC PCIe lanes.
- All Root Port sideband signals (with the exception of the dedicated AUX port) must be generated through I2C expansion, and USB hub expansion devices mounted to the APEC slot card.
- All Root Port link CLK signals (with the exception of the dedicated AUX signal) must be generated through clock buffer component devices mounted to the APEC slot card.

16.3. APEC Root Port Example

It is the responsibility of the designer to ensure correct PET and PER connectivity perspectives end to end, and case by case.

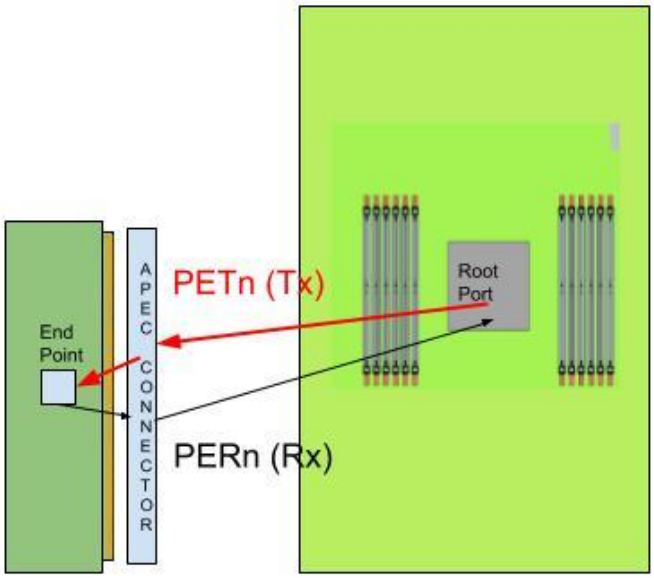
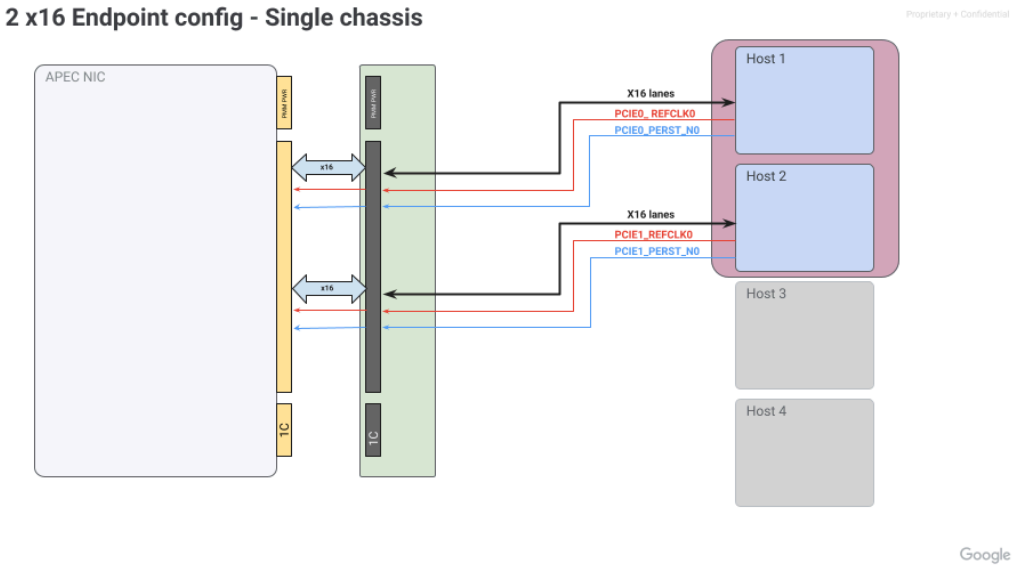
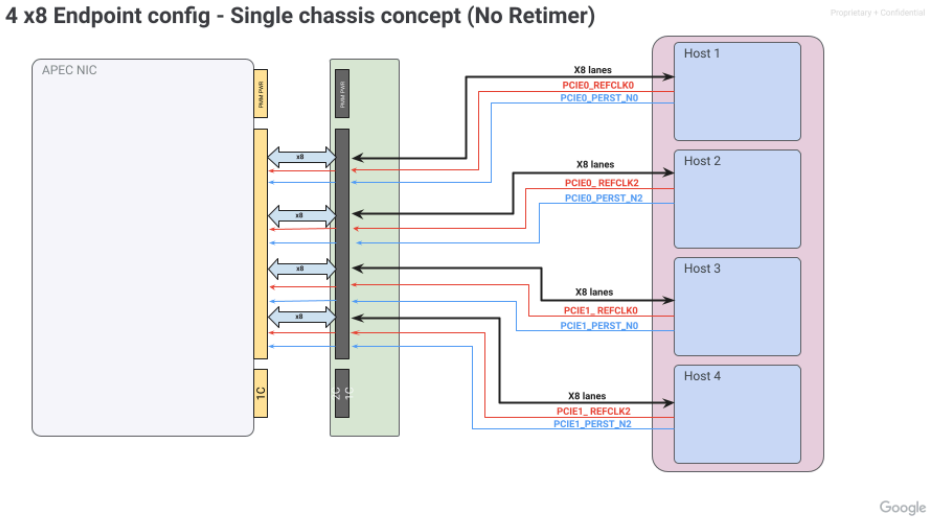


Figure: Root Port PET and PER Connectivity

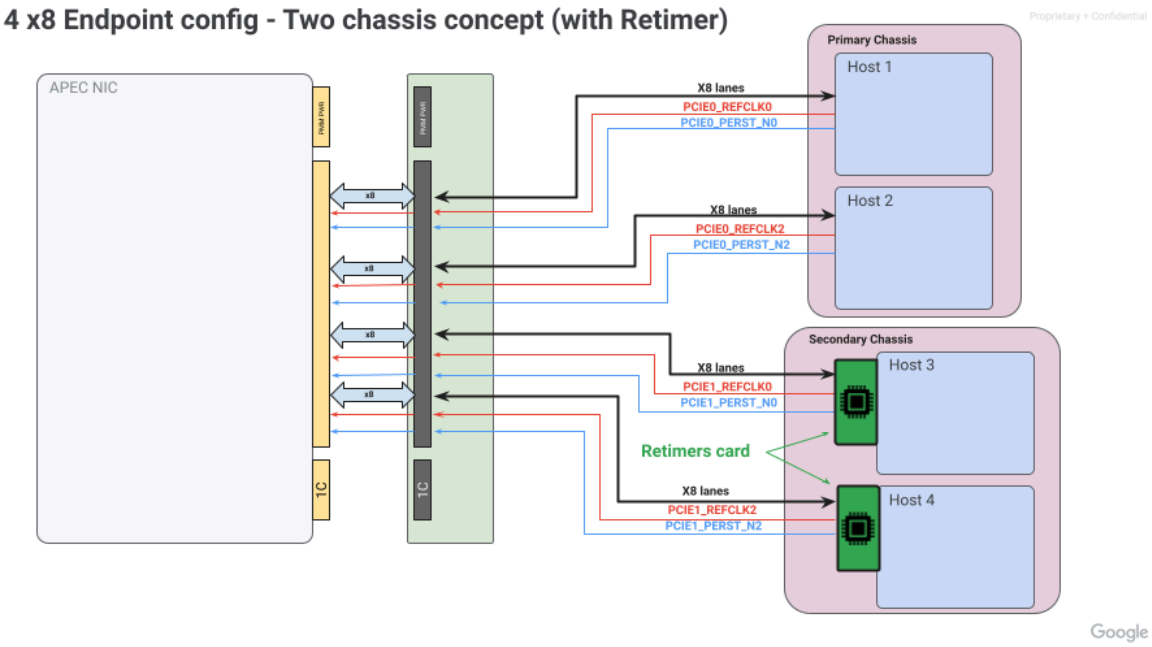
16.4. APEC-Supported Configurations[1]

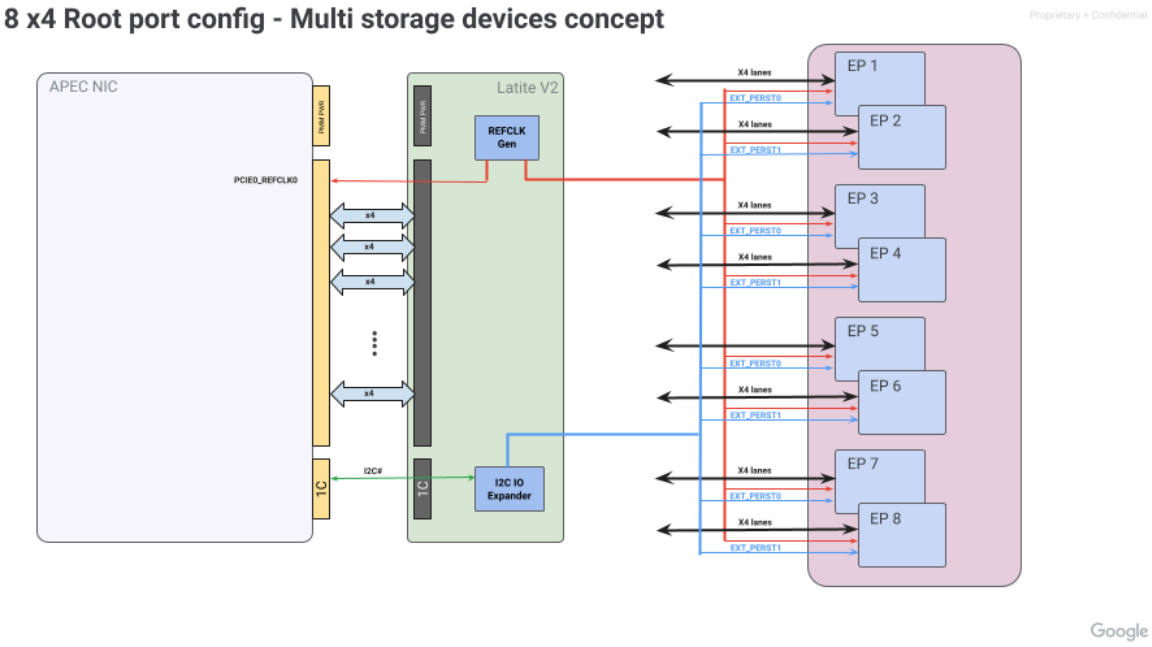
Examples of supported APEC configurations are shown below.

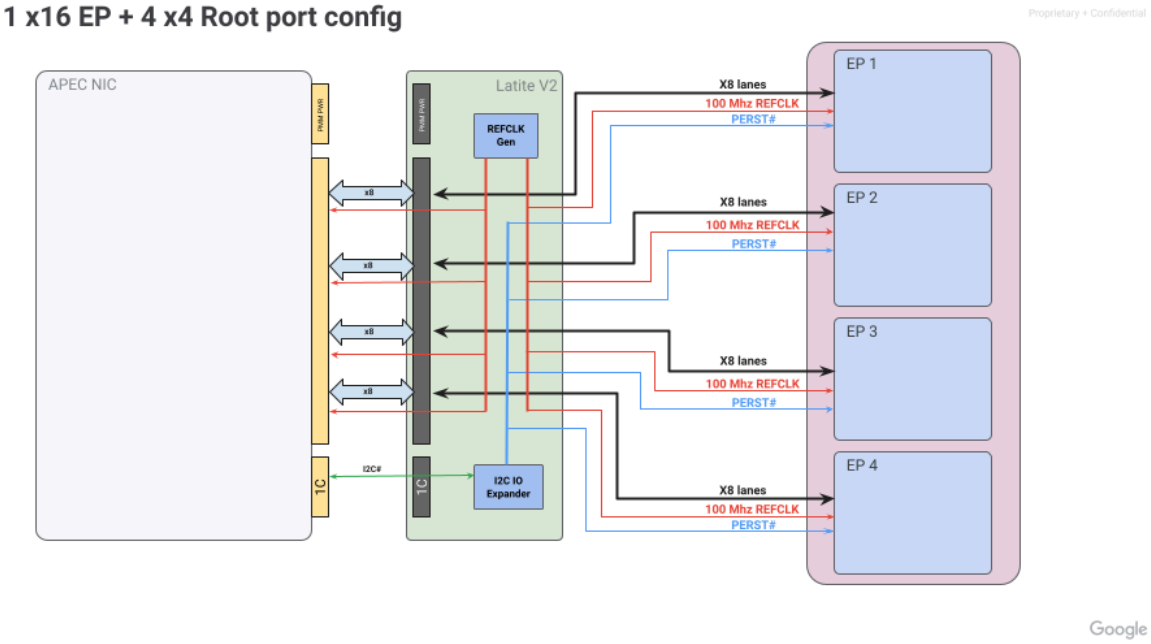




[1] Drawings mtrehan@


4 x8 Endpoint config - Two chassis concept (with Retimer)
Proprietary + Confidential
APEC NIC
PWM PWR
x8
1C
Primary Chassis
Host 1
Host 2
X8 lanes
PCIE0_REFCLK0
PCIE0_PERST_N0
X8 lanes
PCIE0_REFCLK2
PCIE0_PERST_N2
Secondary Chassis
Host 3
Host 4
X8 lanes
PCIE1_REFCLK0
PCIE1_PERST_N0
Retimers card
X8 lanes
PCIE1_REFCLK2
PCIE1_PERST_N2
Google


8 x4 Root port config - Multi storage devices concept
Proprietary + Confidential
APEC NIC
PWM PWR
PCIE0_REFCLK0
x4
1C
I2C#
Latite V2
REFCLK Gen
I2C IO Expander
X4 lanes
EXT_PERST0
EXT_PERST1
EP 1
EP 2
EP 3
EP 4
EP 5
EP 6
EP 7
EP 8
Google



The table below presents the example configuration signals.

		Lanes [0,1]	Lanes [2,3]	Lanes [4,5]	Lanes [6,7]	Lanes [8,9]	Lanes [10,11]	Lanes [12,13]	Lanes [14,15]	Lanes [16,17]	Lanes [18,19]	Lanes [20,21]	Lanes [22,23]	Lanes [24,25]	Lanes [26,27]	Lanes [28,29]	Lanes [30,31]
1	4 x 8EP	**End Point 1**				**End Point 2**				**End Point 3**				**End Point 4**			
		PCIE0_REFCLK0 PCIE0_PERST_N0				PCIE0_REFCLK2 PCIE0_PERST_N2				PCIE1_REFCLK0 PCIE1_PERST_N0				PCIE1_REFCLK2 PCIE1_PERST_N2			
2	2 x 16EP	**End Point 1**								**End Point 2**							
		PCIE0_REFCLK0 PCIE0_PERST_N0								PCIE1_REFCLK0 PCIE1_PERST_N0							
3	8 x 4RP	**Root Port 1**		**Root Port 2**		**Root Port 3**		**Root Port 4**		**Root Port 5**		**Root Port 6**		**Root Port 7**		**Root Port 8**	
		PCIE0_REFCLK0 EXT_PERST0		PCIE0_REFCLK0 EXT_PERST1		PCIE0_REFCLK0 EXT_PERST2		PCIE0_REFCLK0 EXT_PERST3		PCIE1_REFCLK0 EXT_PERST4		PCIE1_REFCLK0 EXT_PERST5		PCIE1_REFCLK0 EXT_PERST6		PCIE1_REFCLK0 EXT_PERST7	
4	1x16 EP + 4x4 RP	**End Point 1**								**Root Port 1**							
		PCIE0_REFCLK0 PCIE0_PERST_N0								PCIE1_REFCLK0 EXT_PERST0							

17. APCE Card Present Detect

The APEC connector supports a dedicated “Card_present#” pin on one end.

The APEC connector has dedicated power pins at the opposite end of “Card_present#”

It is suggested that APEC cards use a combination of the “Card_present#” pin and the +12V (or +54V) applied power. See example below.

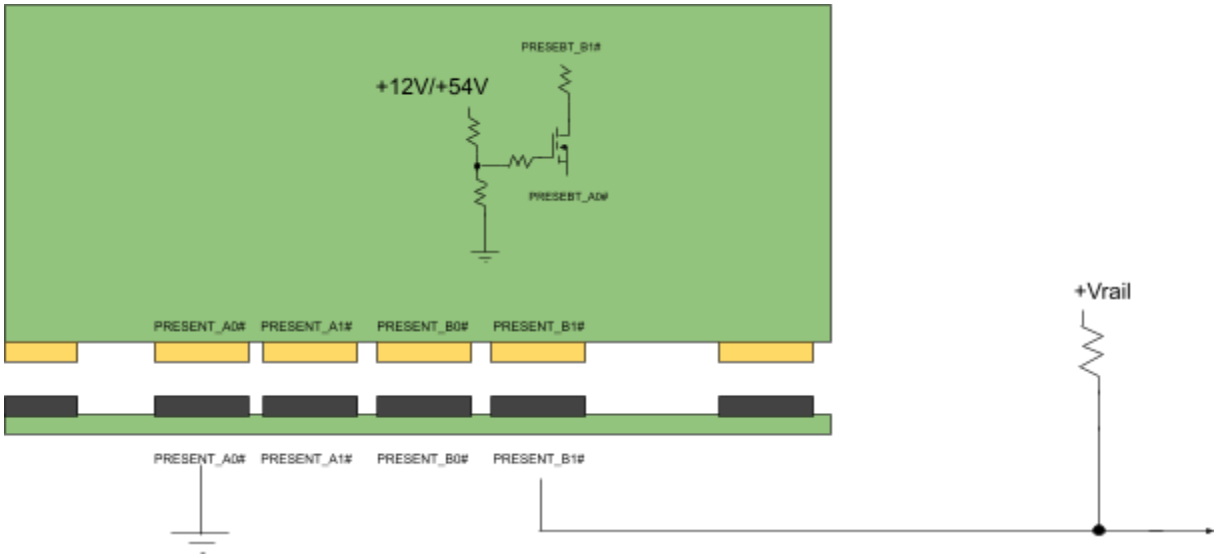


Figure: Card Present Detect

18. Mechanical Card Interface

APEC connector array can be supported on all currently defined CEM form factors, including Full Height Full Length. The primary APEC card form factor covered here is **Full-Height, Half-Length**. Key features are:

- 1x 56 pin section - management and control
- 4x 68 pin (4x 34 pair) sections - signal IO and isolation
- 1x 16 pin power connector section - supporting 12V OR 54V.

18.1. APEC Card Features

In general, APEC will similarly follow PCIe CEM rules regarding board area size, keepouts, and volumes.

- Envelope Dimensions : 111mm x 167.65mm
- Four corner holes are required for the APEC card
    - North West Hole: program/product dependent, used for front faceplate mounting, can be moved as needed.
    - South West Hole: fixed, used for front faceplate mounting, and CSYS 0,0 for placement.
    - North East Hole: fixed, used for retention bracket mounting or ejector module. If hole needs to be moved to accommodate the layout, custom mechanical parts can be made for the program/product.
    - South East Hole: fixed, used for retention bracket mounting or ejector module. If hole needs to be moved to accommodate the layout, custom mechanical parts can be made for the program/product.

18.2. APEC PCB Thickness

APEC will target a 93mil (+/- 8%) board (increased from 62mil PCIe CEM). The difference in board thickness will be subtracted from the top volume keepout in order to maintain the same bottom side keepout of 105mil.

APEC will only feature a dual-wide top volume. The intent of APEC dual wide is to maintain a 1.6” pitch (similar to CEM DW) between APEC cards, thus top side keep out is 1.336” compared to 1.37” in PCIe CEM.

This spec does not prohibit the creation of a single wide or ‘less-than-dual-wide’ spec. Use cases requiring these slimmer versions must also consider that the associated adapter must also fit within the single wide envelope. This may impact the feasibility of PCIe x32 in a single wide configuration.

The figure below provides board dimensions.

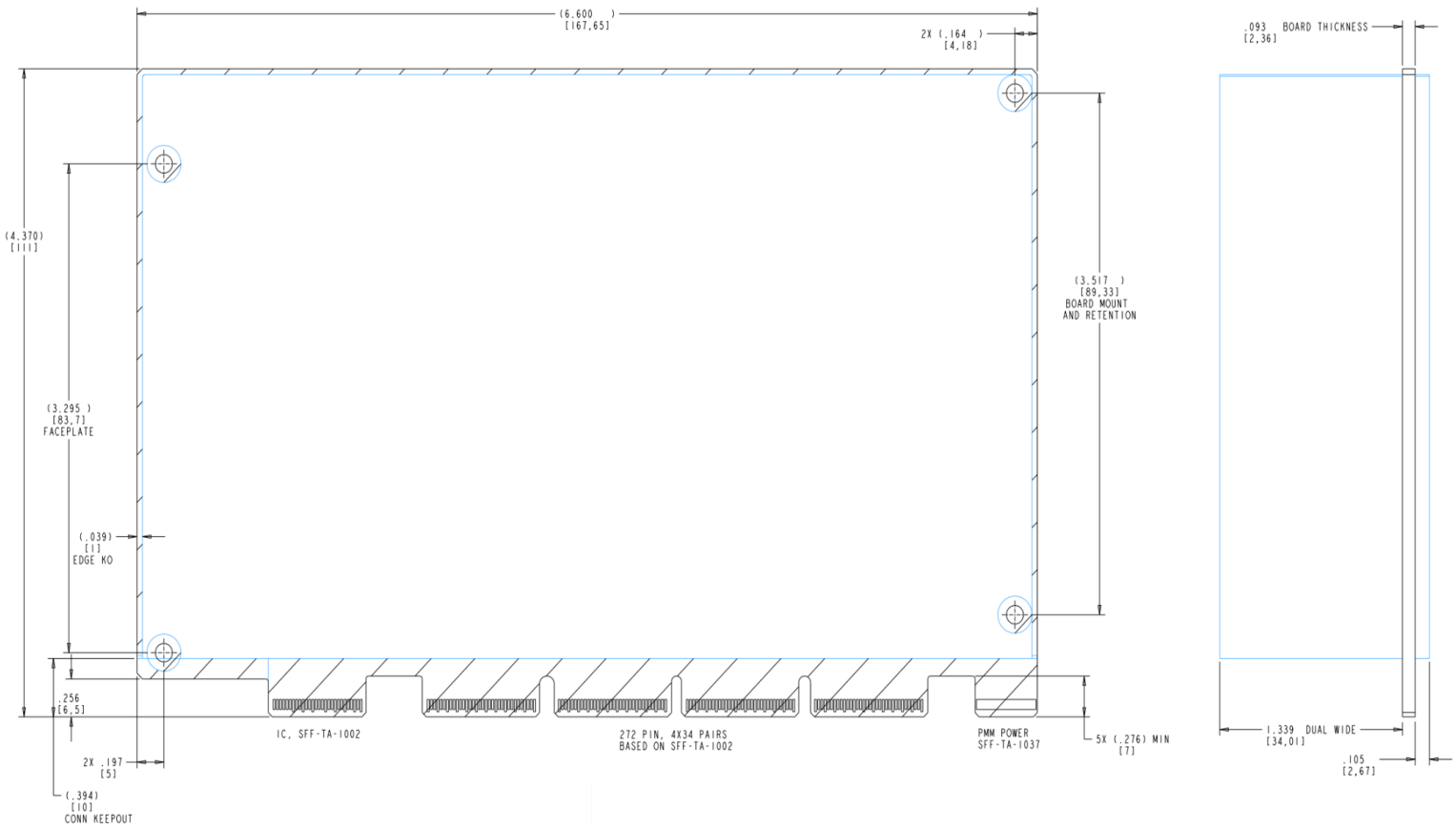


Figure: Board Dimensions

18.3. APEC Card Edge

As previously described in this section, the card edge has three discrete edge finger sections with dedicated features:

- 1x 56 pin section - management and control
- 4x 68 pin (4x 34 pair) sections - signal IO and isolation
- 1x 16 pin power connector section supporting 12V OR 54V.

Note that not all APEC add-in-cards applications will require the use of all three discrete edge finger sections. For example, an APEC AIC that only requires PCIe x16, would only need two out of the four 68 pin sections and the card edge design would omit the edge finger in the locations it is not needed to reduce insertion/extraction forces.

Locations of each discrete edge connector section shall be measured and datumed with respect to the south west mounting hole on the board. This ensures a consistent faceplate location when the card is installed. This card edge shall plug into three connector housings. The figure below illustrates the APEC Card Edge.

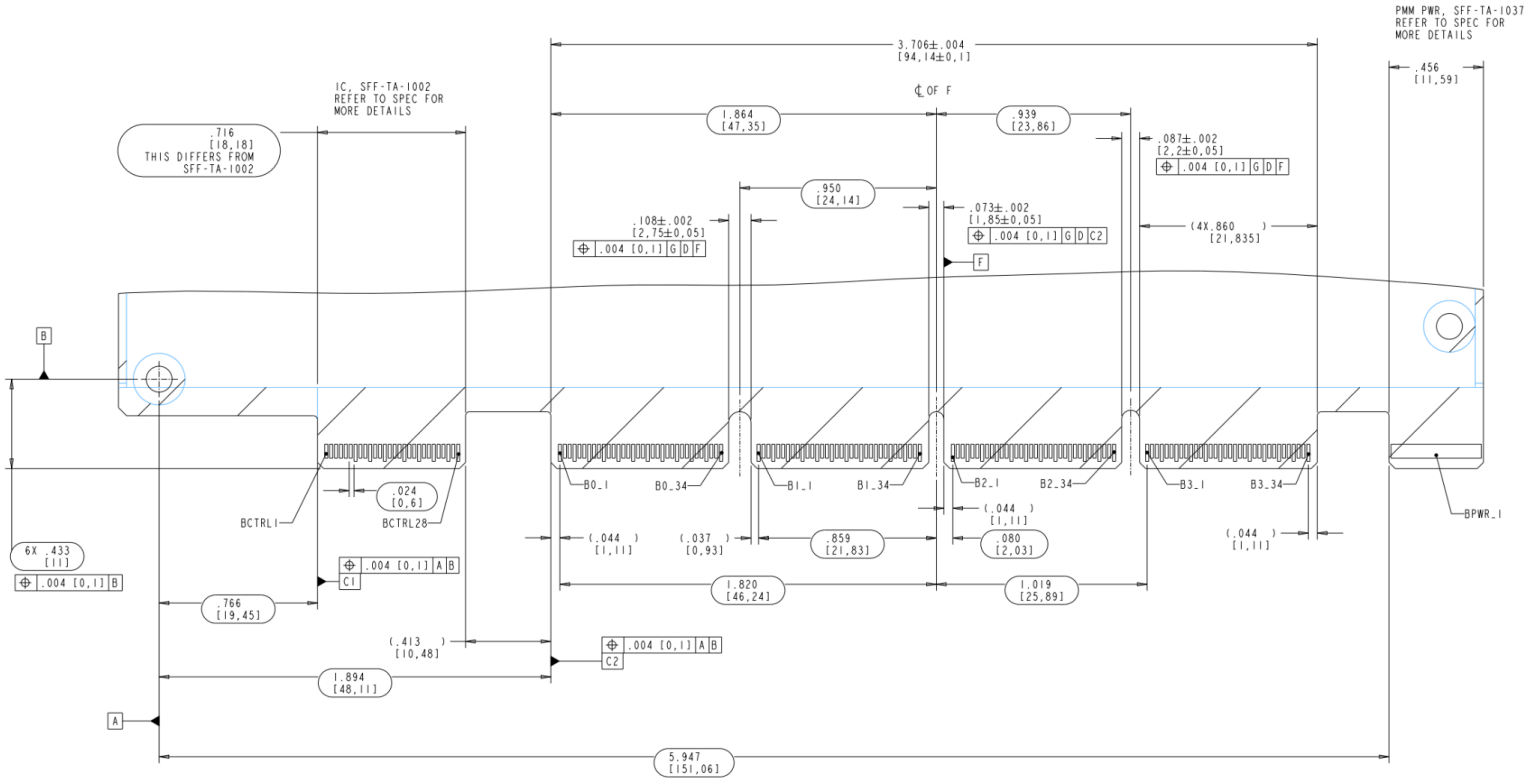


Figure APEC Card Edge

18.3.1. Management and Control: 1C Card Edge Section

Design of the 1C edge on APEC shall follow exactly SFF-TA-1002 except for the following change:

- The card edge width has been reduced from 18.48mm to 18.18mm to mitigate binding between the APEC card edge and the connectors.

Pad locations are measured from connector edge centerline, as specified in SFF-TA-1002; the card edge width reduction does not affect this. Refer to this spec for PCB thickness

18.3.2. 32 Lane PCIe Section: 272 Pin, 4x34 Pair Edge

This card edge consists of four identical-sized card edges.

- Pads shall follow spacing defined in SFF-TA-1002.
- The first pad centerline to alignment web dimensions are shown in the figure above, and shall be used to position all pad patterns.
- Refer to the SFF-TA-1002 spec for PCB thickness

Note that not all pad patterns are centered within their card edges. This is done to keep nominal alignment between the connector pins and card edge pads

18.3.3. Power Section: PMM Power

Follow SFF-TA-1037, using PCB width as defined in this spec.

19. Pinout Requirements

See APEC pinout

The contact sequence for each pin is shown, indicating the order in which the pins make contact. Edge gold fingers shall be plated with hard gold to maximize the number of insertion cycles.

20. SI Requirements

The SI requirements are listed below.

20.1. Mated Connectors

- SFF mated connector IL, RL and crosstalk are covered by snia.org specification.
- CEM mated connector IL, RL and crosstalk are covered by PCI SIG

20.2. Cable Assembly

The table below lists the cable specifications.

Parameter	Requirements
Differential Impedance	85 Ω differential 85 Ω +/- 10% and 42.5 Ω single-ended
Differential Insertion Loss (SDD21)	APEC connector cable mated end connector; 7.5dB PCIe gen6

21. Mechanical Requirements

21.1. Insertion/Extraction/Retention

Plug insertion, latch retention, and removal forces must adhere to the table below (from SFF). Plug side force refers to force applied perpendicular to the latching face of the plug and is the minimum requirement before connector cage damage.

The following table presents plug Insertion, latch retention, and removal specifications.

Measurement	Min	Max	Comments
Insertion	N/A	39.3lbs (175N)	Module to be inserted into connector and cage with latch mechanism included. ● SFF-TA-1002: “1.1N per pair”, (28+272/2*1.1) = 165N = 37.1lbs ● SFF-TA-1020: “SFF-TA-1002, Requirements + 10N MAX”, 175N = 39.3lbs
Extraction	3.37lbs (15N)	9lbs (44N)	Module to be removed from connector and cage with latching mechanism disengaged. ● 0.10 N/pin pair Minimum = 15N = 3.37lbs
Plug Retention in cage, straight pull (axial)	11.24lbs (50N)	N/A	No functional damage to module, cage, or connector.
Plug side force	20.2lbs (90N)	N/A	Perpendicular applied force to flat face of mated plug. Min force connector cage must withstand before connector damage and latch unsnap

22. Connector PCB Plating Requirements

Edge fingers, signal contacts, and power connectors shall be plated with hard gold to maximize the number of insertion cycles.

Plating for PCB contact pad is:

- Hard gold plating 0.76 µm min. over 2.54 µm minimum nickel.

23. Product Safety and RoHS

23.1. Flammability

- Bulk cable/conductors: UL certified, UL 1581, rated VW-1
- Connector: material rated V-0, 80°C minimum
- Label: material rated VTM-0
- Pull tab: material rated VTM-2 minimum
- Braided Expando: UL certified, UL 1441, rated VW-1 (UZIQ2 or UZKX2)
- Acetate Tape: UL certified, UL 510A (OARC2/OARC8)
- Acceptable Halogen-Free rating: Not Applicable

23.2. RoHS Compliance

- 2011/65/EU (RoHS 2)
- 2015/863 (RoHS 2 amendment)

24. Manufacturing Requirements

There should be no sharp edges on any surface that will normally be handled in operation/installation.

24.1. Electrical and Functional Test

All cables are to be electrically and functionally tested after assembly to ensure that the assemblies have no “shorts” or “opens,” but do have proper continuity, isolation, and functionality.

- Electrical tests shall include open, short, miswired, and hi-pot [high potential voltage to be determined by vendor].
- Manufacturing SI, through measurement (crosstalk excluded), shall ensure compliance with required SI requirements.
- Functional test at final integrated cable shall include list of items below:
    - All modules
        - EEPROM Write/Read/Erase
        - Verify 12V/3.3V/3.3V Aux power rail meets PCI Express CEM requirements.
    - Slot adapters
        - Exercise Function of I2C IO Expander, PCIe Clock MUX, and I2C-Bus Switch.
- A 5-digit unique serial number shall link to SI/Electrical/Functional test result and have dot marking on label, connector, or PCBA indicating tests have been passed.

24.2. PCBA Cleanliness

Target: IPC-A-610 Class 3. The following shall be in effect:

- Unit shall have no contamination on surface contact areas.
- Unit shall be clean, with no discernible flux residues.
- Unit shall be clean, with no foreign object debris (FOD).
- Unit shall be clean, with no discernible chlorides, carbonates, or white residues.

Acceptable: IPC-A-610 Class 3

- Flux residues from no-clean processes are allowed.

- FOD (no foreign object debris) is allowed as long as it meets the following criteria:
    - FOD is attached/entrapped/encapsulated on the PCBA surface or solder mask.
    - FOD does not violate minimum electrical clearance.
- No-clean flux residues on, around, or bridging between non-common lands, components leads and conductors, are allowed.
- No-clean flux residues shall not inhibit visual inspection and access to test points of the assembly.
- No dulling of metallic surfaces.

25. Packaging

Cables shall be individually wrapped at each end with clear anti-static LDPE bags, and placed onto a PET tray.

26. Interoperability

The cables shall be designed to meet the specification requirements of other vendors' connectors. Electrical performance, form-fit-function, and mechanical robustness shall be equivalent and meet all specifications within this document. These tests must be completed and performed within the specification limits to be considered as qualified.

The following table presents Interoperability Specifications.

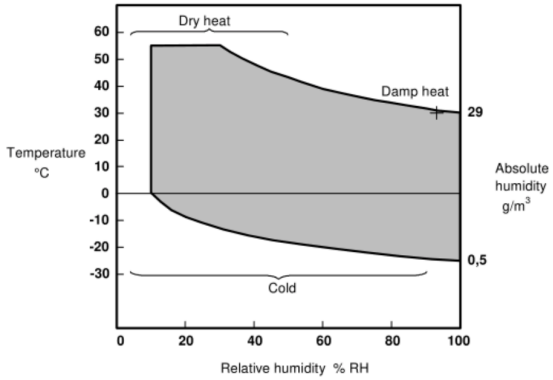
	Plug, Vendor A	**Plug, Vendor B**	**Plug, Vendor ...**	**...**
Connector, Vendor A				
Connector, Vendor B				
Connector, Vendor ...				
...				

27. Environmental and Reliability Requirements

27.1. Environmental Requirements

The connector interface environmental tests shall follow EIA-364-1000 and TS-1000B *Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications*. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA-364-1000. TS-1000B is based on the field temperature per the following:

- Field Life: 10 years, 87600 hours
- Operating Conditions: 0℃ to 80℃, 85% RH, no condensing
- Storage Climatic Condition:
    - IEC 60721-3-1 1K22
    - Enclosed storage location without temperature or humidity control
    - -25℃ to 55℃, 10% to 100% RH (classification of climatic conditions excerpted from IEC 60721-3-1, not the test conditions and no reliability or lifetime assessment is possible based on this classification)



- Shipping Climatic Conditions:
    - IEC 60721-3-2 2K12
    - Weather-protected transportation without temperature or humidity control
    - Public transportation
    - -45℃ to 70℃, 4% to 100% RH (classification of climatic conditions excerpted from IEC 60721-3-2, not the test conditions and no reliability or lifetime assessment is possible based on this classification)

Also reference “5.4 Cable Mechanical Performance & Reliability” in SFF-TA-1020 (linked above)

27.2. Atmospheric Conditions During Test (IEC 60068-1/IEC 61000-4-2)

- Standard Ambient
  - Temperature: 25℃ ± 10℃
  - Humidity: 25% to 75% RH
  - Air Pressure: 86 kPa to 106 kPa
- Controlled Ambient
  - Temperature: 25℃ ± 2℃
  - Humidity: 50% ± 5% RH
  - Air Pressure: 86 kPa to 106 kPa
- Climatic Conditions For ESD
  - Temperature: 25℃ ± 10℃
  - Humidity: 30% to 60% RH
  - Air Pressure: 86 kPa to 106 kPa

27.3. Reliability Requirements

This section lists the cable assembly reliability test conditions.

Following reliability testing, the connector(s) subjected to testing with the cable assembly must meet electrical, mechanical, and environmental criteria.

Test items and groups defined in this section are chosen to understand the possible failure modes and mechanisms of the unit under test (UUT), and to explore potential opportunities to improve the design and/or manufacturing processes. Therefore, *failing a test item or group defined in this section does not constitute a condition for halting shipment of cable assemblies described in this specification*. However, all failures need to be carefully examined, inspected, and analyzed to understand the cause of failure. Test items that incur failures may be added to Ongoing Reliability Testing (ORT) when the causes of failure can be attributed to deficiencies in the manufacturing process.

Samples submitted for testing shall be manufactured using mature design and manufacturing processes. Test and failure analysis reports must be submitted for review. Manufacturer site relocation may prompt repeating the test with UUTs manufactured at the new site.

27.3.1. Test Items

The table below lists the test items.

Item	Test Description	Test Procedure / Condition	Criteria
A	Low Level Contact Resistance	EIA-364-23, Option 1 20 mV max, 100 mA max	Termination of connector to test board shall be included in the measurement.
B	Durability	EIA-364-09, 200 Cycles	After test, cable must meet visual inspection criteria and electrical requirements.
C	Durability - Preconditioning	EIA-364-09, 20 Cycles	After test, cable must meet visual inspection criteria and electrical requirements.
D	Thermal Shock (Temperature Cycling)	EIA-364-32, Method A, -40℃ to 85℃, 100 Cycles,	Inspect function of cable every 25 cycles. After test, cable must meet electrical requirements.
E	Thermal Shock (Temperature Cycling) - Preconditioning	EIA-364-32, Method A, -40℃ to 85℃, 25 Cycles	After test, cable must meet electrical requirements.
F	Temperature Life	EIA-364-17, Method A. 85℃, 250 Hrs	After test, cable must meet electrical requirements.
G	Temperature Humidity	JESD22-101D, 85℃, 85% RH, 250 Hrs, no coil.	After test, cable must meet electrical requirements.
H	Operational Shock	EIA-364-27, Test condition E, 50g, Sawtooth, 11 ms Mounted In A Rigid Fixture That Duplicates The Support Points In The Actual Application Of The Cable On The Board.	After test, cable must meet visual inspection criteria and electrical requirements.
J	Operational Vibration	EIA-364-28, Test Condition VII, Letter D, Random Vibration 0.02 g/Hz, 20 Hz To 500 Hz, 3.10g RMS, 15 mins per axis Event Of Discontinuity: Unless otherwise specified, an electrical load of 100 mA maximum with a detector capable of detecting a discontinuity of 1.0 µs or longer. Monitoring must be performed pursuant to EIA-364-46. Mounted In A Rigid Fixture That Duplicates The Support Points In The Actual Application Of The Cable On The Board.	No more than one event. After test, cable must meet visual inspection criteria and electrical requirements.
K	Cable Static Pull Out	EIA-364-38, Method B. Grip the cable overmold and pull on the cable to test cable attachment to the	After test, cable must meet visual inspection criteria and electrical

		back shell ≧ 50N	requirements.
L	Bend Radius (Static Bend Under Temp/Humidity)	JESD22-101D, 85℃, 85% RH, 250 Hrs Fixture defined in 9.1	After test, cable must meet visual inspection criteria and electrical requirements.
M	Strain Relief (Dynamic Bend)	EIA-364-41, Test condition 1 Fixture defined in 9.1, Cycling rate shall be 12 ~14 cycles per minute, 25 cycles	After test, cable must meet visual inspection criteria and electrical requirements.
N	Gtest (Orbital Motion)	Gtest (Orbital Motion), Fixture defined in 9.2	After test, cable must meet visual inspection criteria and electrical requirements.
P	Porosity	IPC - TM-650 2.3.24 (TM-650 2.3.24.2A) for paddle board.	After test, meet visual inspection criteria.
Q	SI Measurement	Standard Ambient	Must meet SI performance requirements.
R	Transportation - Cold	IEC 60068-2-1, Ab: Cold, -40℃, 72 Hrs, tested without package	After test, cable must meet visual inspection criteria and electrical requirements.
S	Transportation - Dry Heat	IEC 60068-2-2, Bb: Dry Heat, 70℃, 72 Hrs, tested without package	After test, cable must meet visual inspection criteria and electrical requirements.
T	Transportation - Change of Temperature	IEC 60068-2-14, Nb: Change of Temperature, -40℃ to 30℃, 5 cycles (mass < 5 kg), t_1(exposure time)= 3 hours, 1℃/minute	After test, cable must meet visual inspection criteria and electrical requirements.
U	Plug Insertion	EIA-364-13, with latch mechanism included	Must meet 7.7. requirements.
V	Plug Extraction	EIA-364-13, with latching mechanism disengaged	Must meet 7.7. requirements.
W	Plug Retention	EIA-364-13, secured the test board with connector mounted and pulled on the plug and held for 1 minute minimum to test integrity of the latching mechanism.	Must meet 7.7. requirements.

* (Character I, O are avoided)

27.3.2. Test Groups

The following table lists the test groupings.

	Test Groups									
Orders	1	2	3	4	5	6	7	8	9	10
I	Q	Q	Q	Q	Q	Q	Q	Q	P	U
II	E	E	C	E	E	E	E	R		B
III	Q	Q	Q	Q	Q	Q	Q	Q		W
IV	B	C	D	C	C	C	C	S		
V	Q	Q	Q	Q	Q	Q	Q	Q		
VI	K	F		L	J	N	M	T		
VII	Q	Q		Q	Q	Q	Q	Q		
VIII				G	H			V		
IX				Q	Q					
X										
Qty	6	6	6	6	6	6	6	6	6	6

27.3.3. Ongoing Reliability Test

27.3.3.1. Sampling Plan

- Frequency: perform tests and submit test results on a quarterly basis.
- Sample size: same as qualification test plan, 6 pcs.

27.3.3.2. Test Group

The following table lists the test groupings.

Test Order	Test Description	Test Condition	Criteria
1	Initial SI Measurement	Standard Ambient, No Coil	Meet electrical requirements
2	Thermal Shock (Temperature Cycling) - Preconditioning	EIA-364-32, Method A, -40℃ to 85℃, 25 Cycles	No evidence of physical damage
3	SI Measurement	Standard Ambient, No Coil	Meet electrical requirements
4	Durability - Preconditioning	EIA-364-09, 20 Cycles	No evidence of physical damage
5	Strain Relief (Dynamic Bend)	EIA-364-41, Test condition 1 Fixture defined in 9.1, Cycling rate shall be 12 ~14 cycles per minute, 25 cycles	No evidence of physical damage No intermittent disconnection
6	SI Measurement	Standard Ambient, No Coil	Meet electrical requirements