

OCP3 GEN5 Compliance Baseboard (CBB)

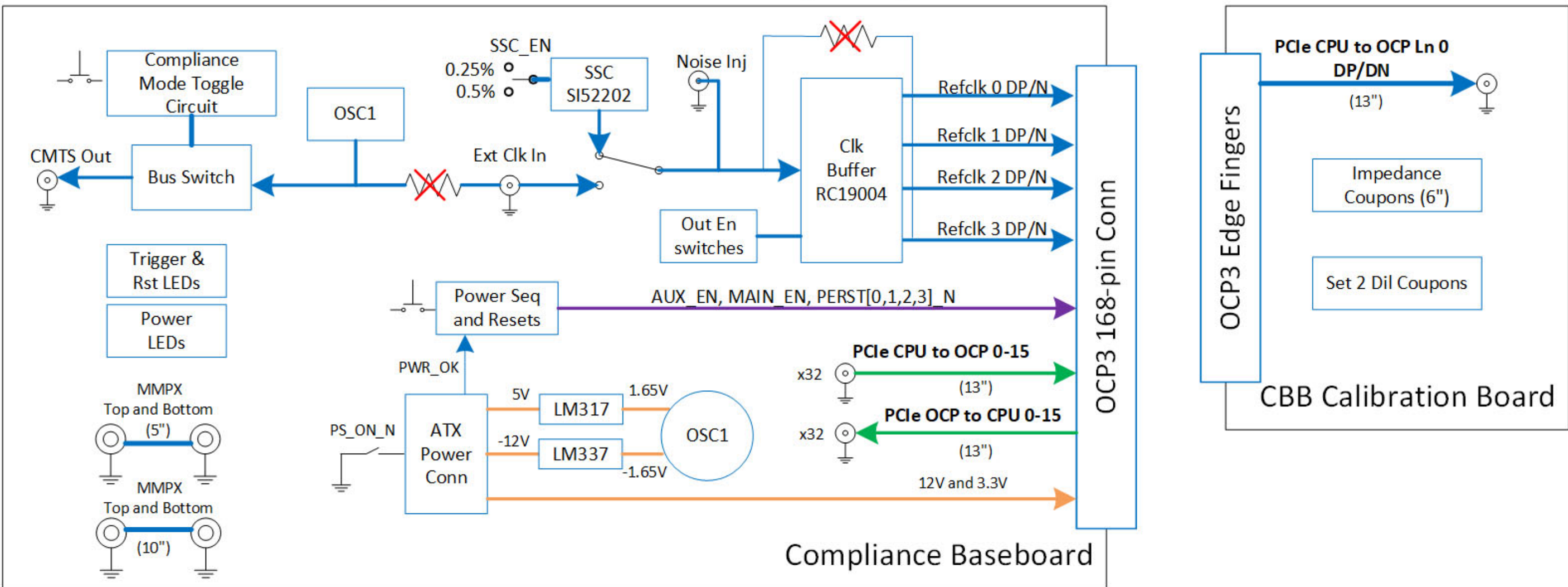


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PWA: JGWMJ
PWB: 7YKPM
Sch: X07NT

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TITLE		OCP3 SI TX CBB GEN 5	
DWG NO.		X07NT	REV. X00
DATE		Tuesday, September 06, 2022	SHEET 1 of 14

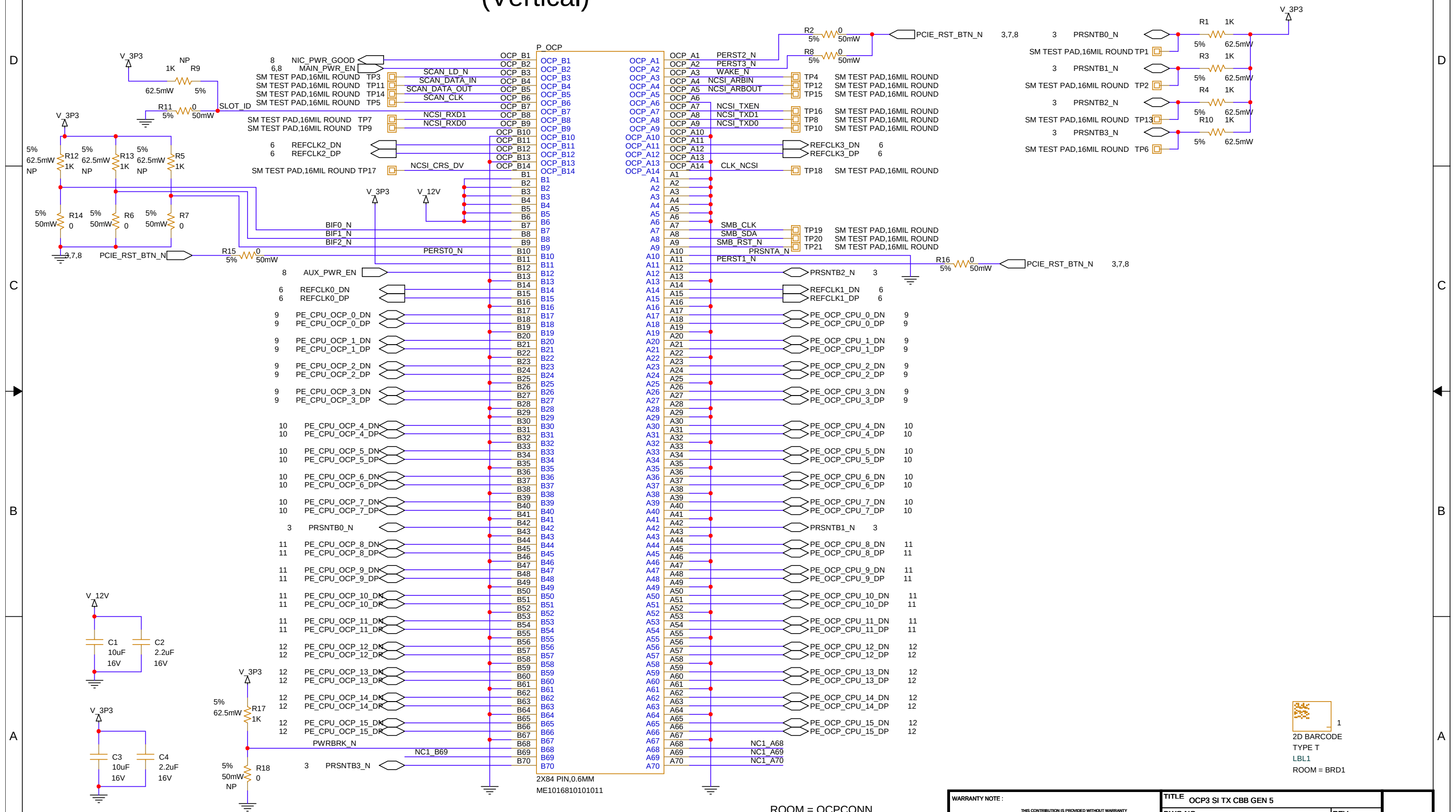
Layer	Info	Thickness
TOP	=====	0.5+Plating
	PP R-5670G 1080	2.821(mil)
L2	=====	1 Oz
	Core R-5775G 0.5	19.685(mil)
L3	=====	1 Oz
	PP R-5670G 2116*2	9.391(mil)
L4	=====	1 Oz
	Core R-5775G 0.5	19.685(mil)
L5	=====	1 Oz
	PP R-5670G 1080	2.821(mil)
BOT	=====	0.5+Plating

Finished:	62.992(6.299/-6.299) mil	1.6(+0.16/-0.16) MM
Designed:	60.787 mil	1.544 MM
Material:	R-5775G	R-5775G

Impedance Information:

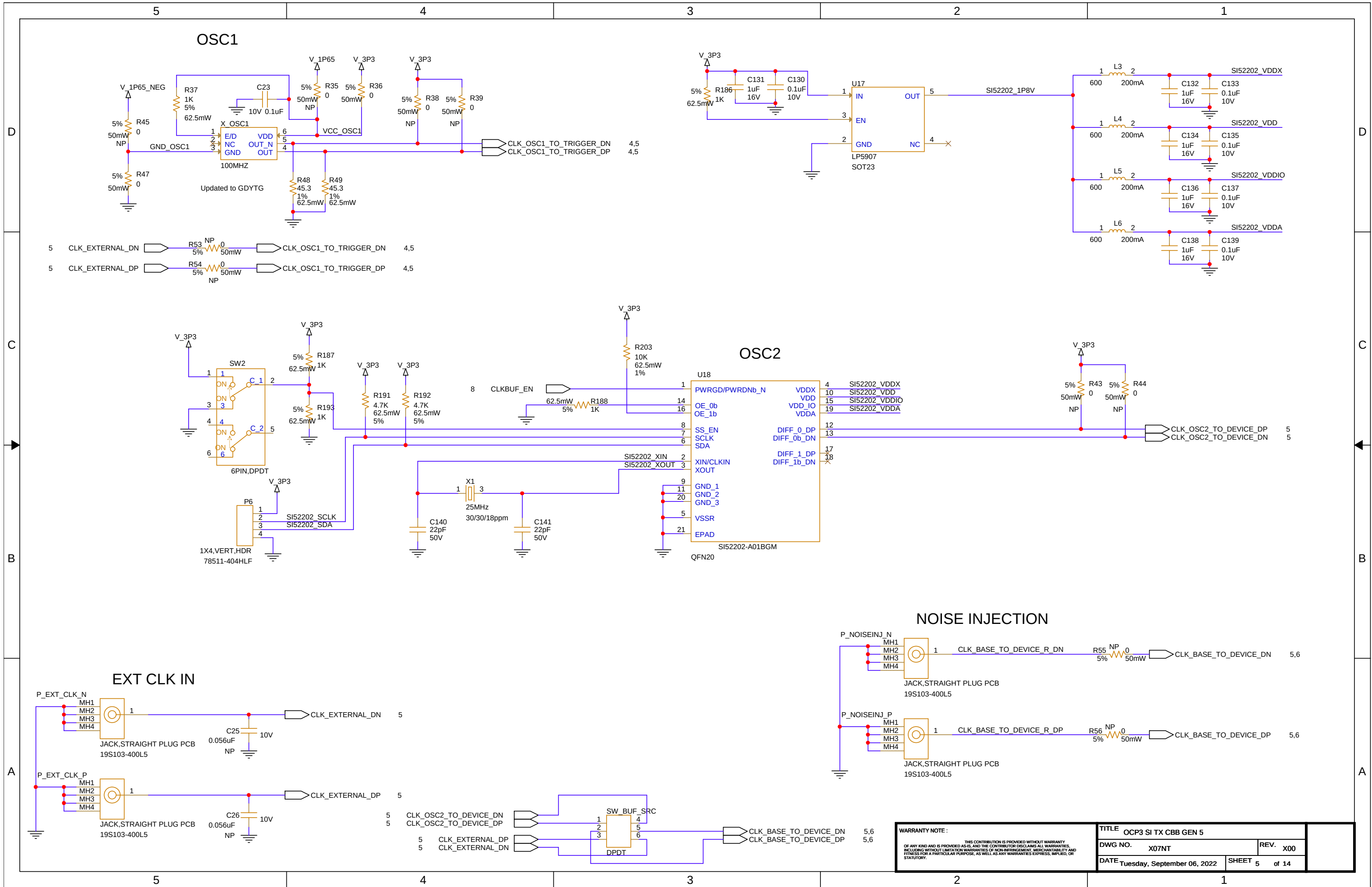
Ctrl	Ref	Imp_type	Cust_req	Imp_req	FP_des	Imp_des	mask	H1	Er1	H2	Er2
L1	L2	Single-Ended	6	42.5+/-10%	6.6	43.388	Yes	2.821	3.19		
L1	L2	Differential	5/7	85+/-10%	5.5/6.5	85.354	Yes	2.821	3.19		
L1	L2	Differential	3.9/10.1	100+/-10%	4.3/9.7	100.185	Yes	2.821	3.19		
L6	L5	Differential	3.9/10.1	100+/-10%	4.3/9.7	100.185	Yes	2.821	3.19		
L6	L5	Differential	5/7	85+/-10%	5.5/6.5	85.354	Yes	2.821	3.19		
L6	L5	Single-Ended	6	42.5+/-10%	6.6	43.388	Yes	2.821	3.19		

OCP3 Small Form Factor Connector (Vertical)



ROOM = OCPCONN

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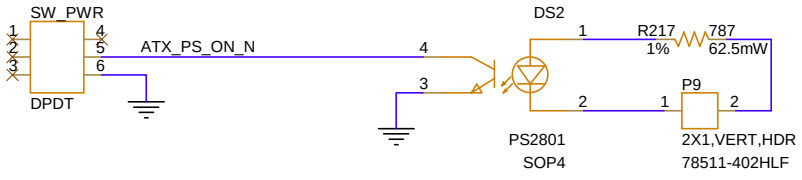
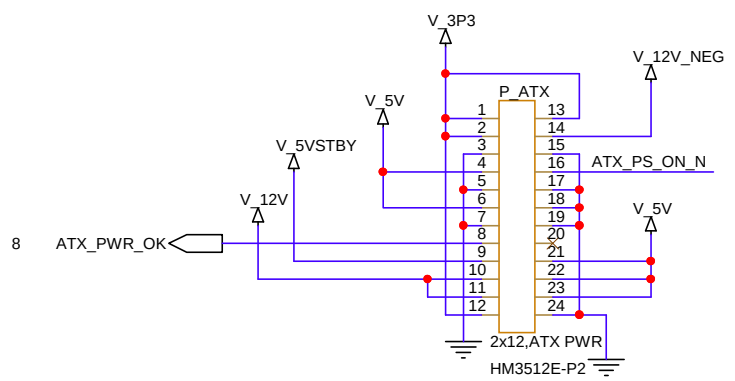
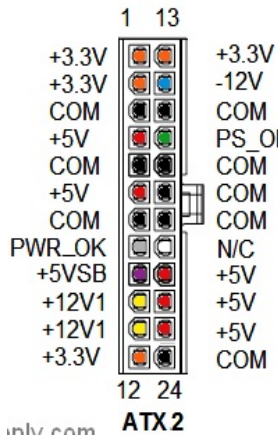
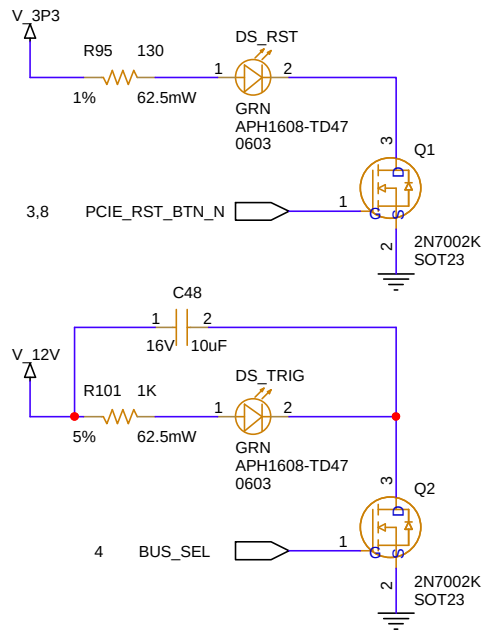
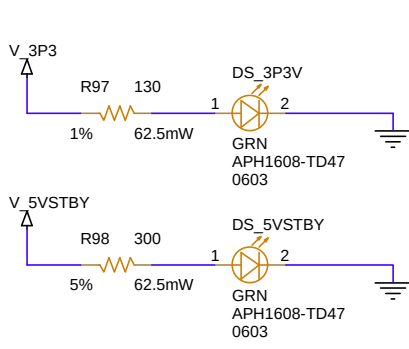
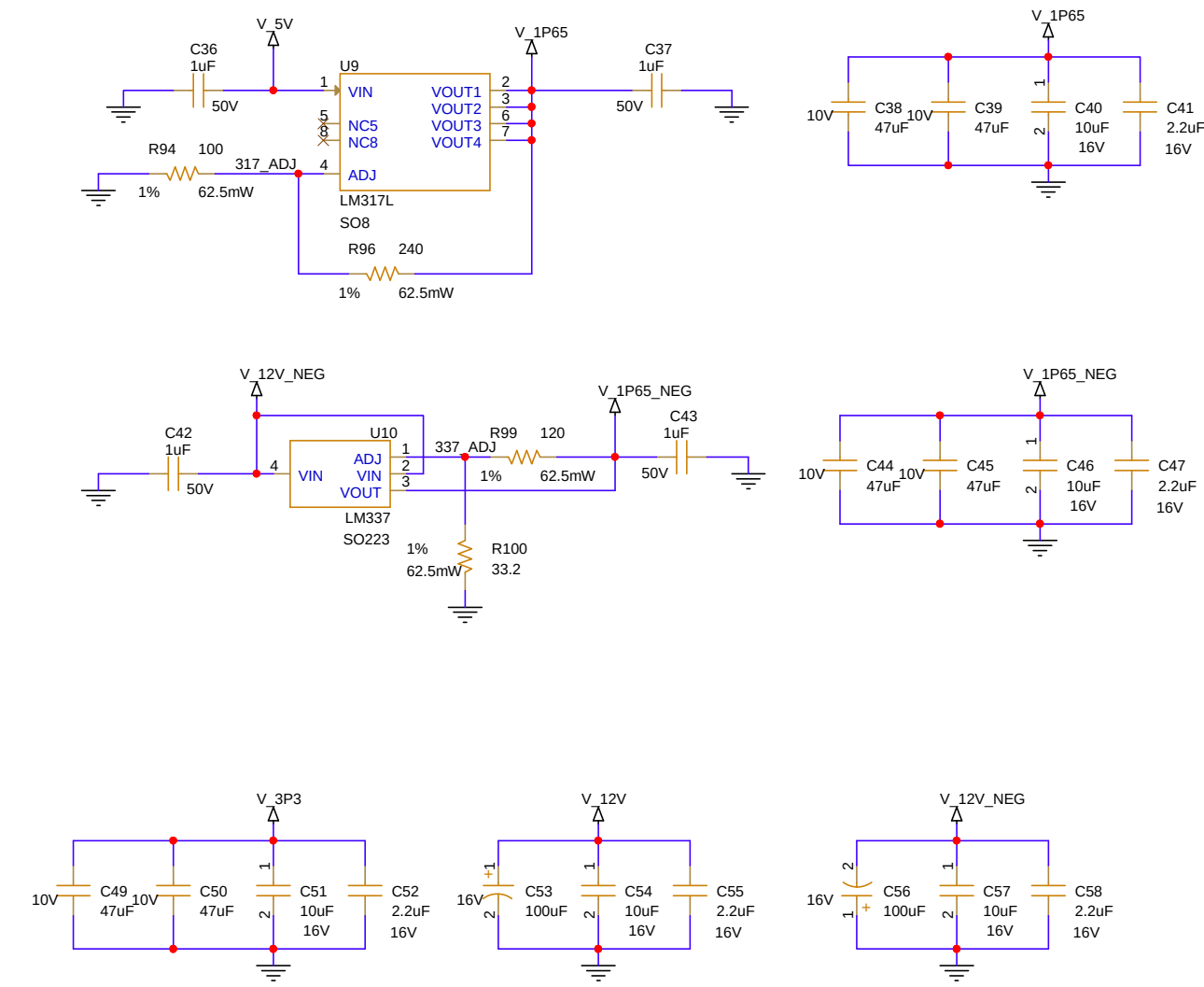


POWER

LEDs

Power Switch

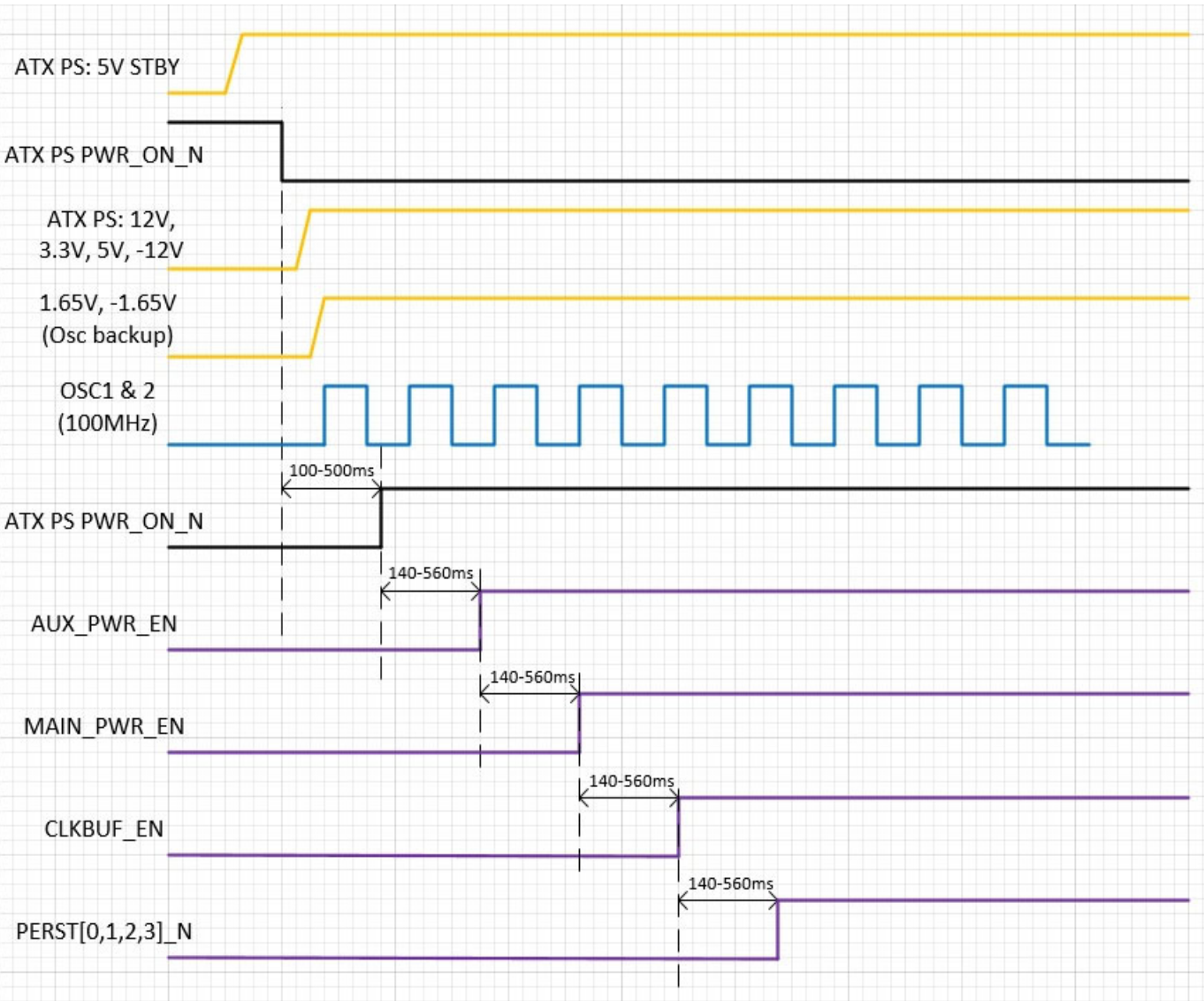
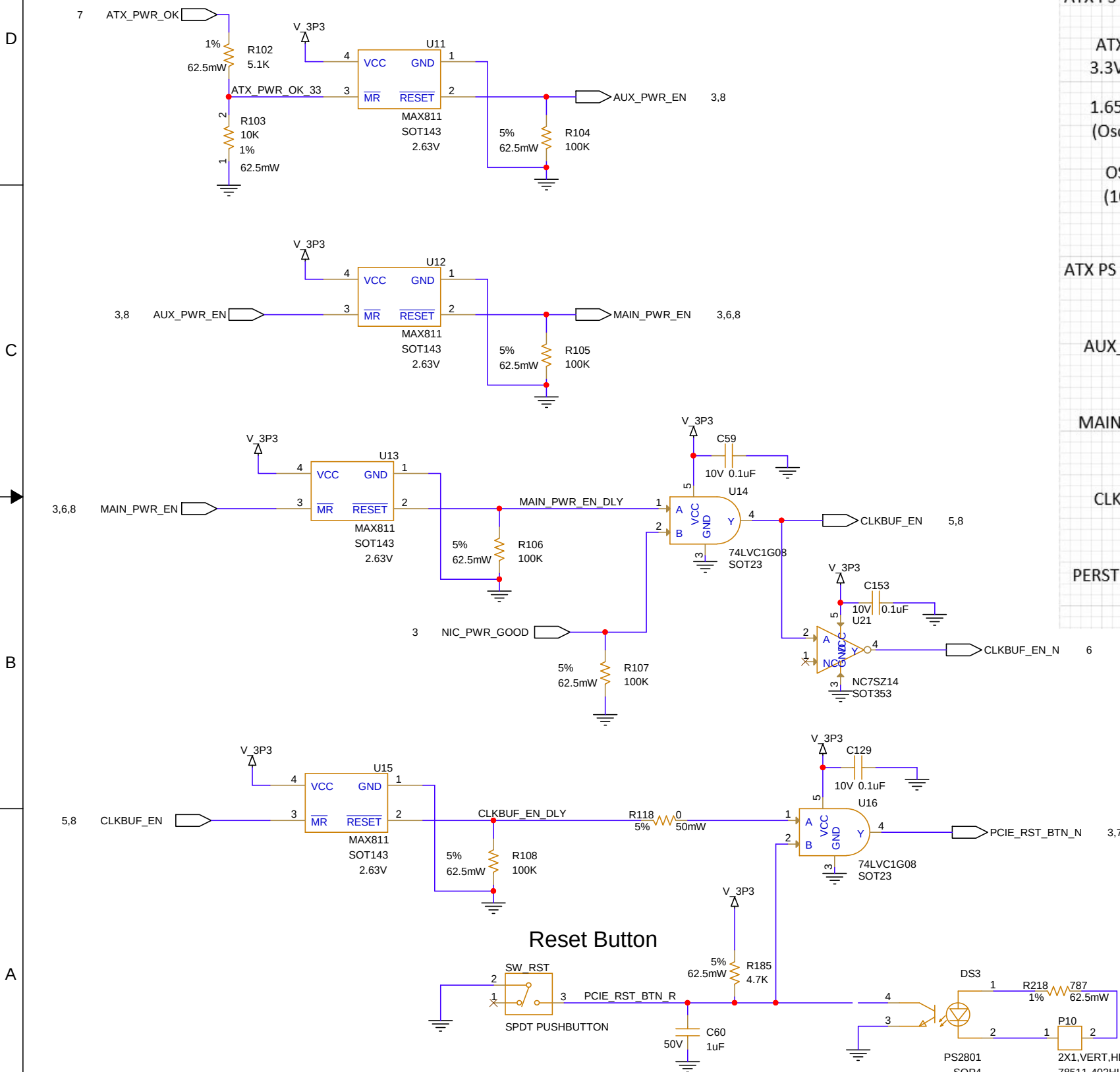
RESET AUTOMATION CONNECTOR



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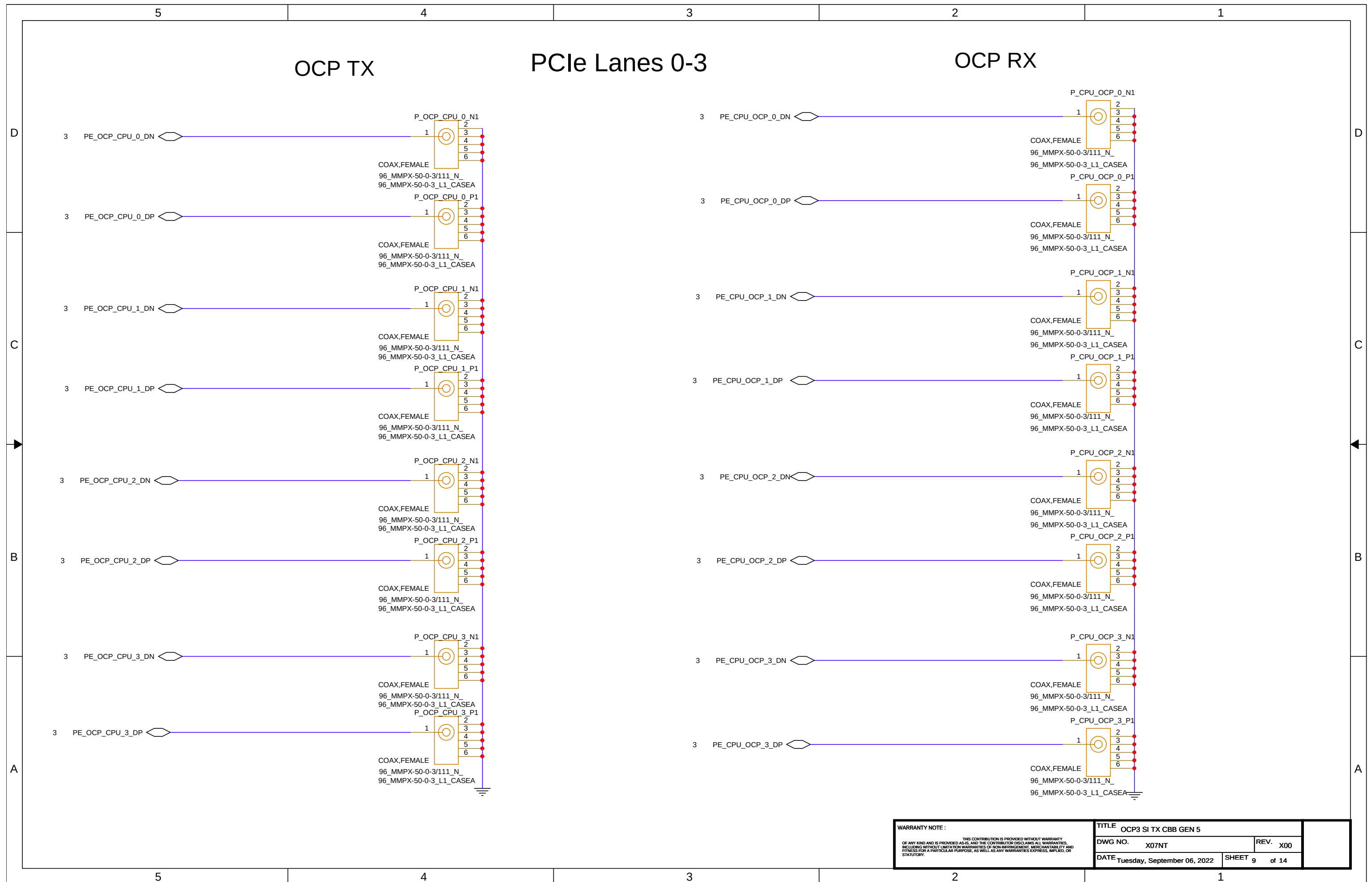
POWER SEQUENCE

MAX811 Reset Active Timeout Period Trp: 140 - 560ms



RESET AUTOMATION CONNECTOR

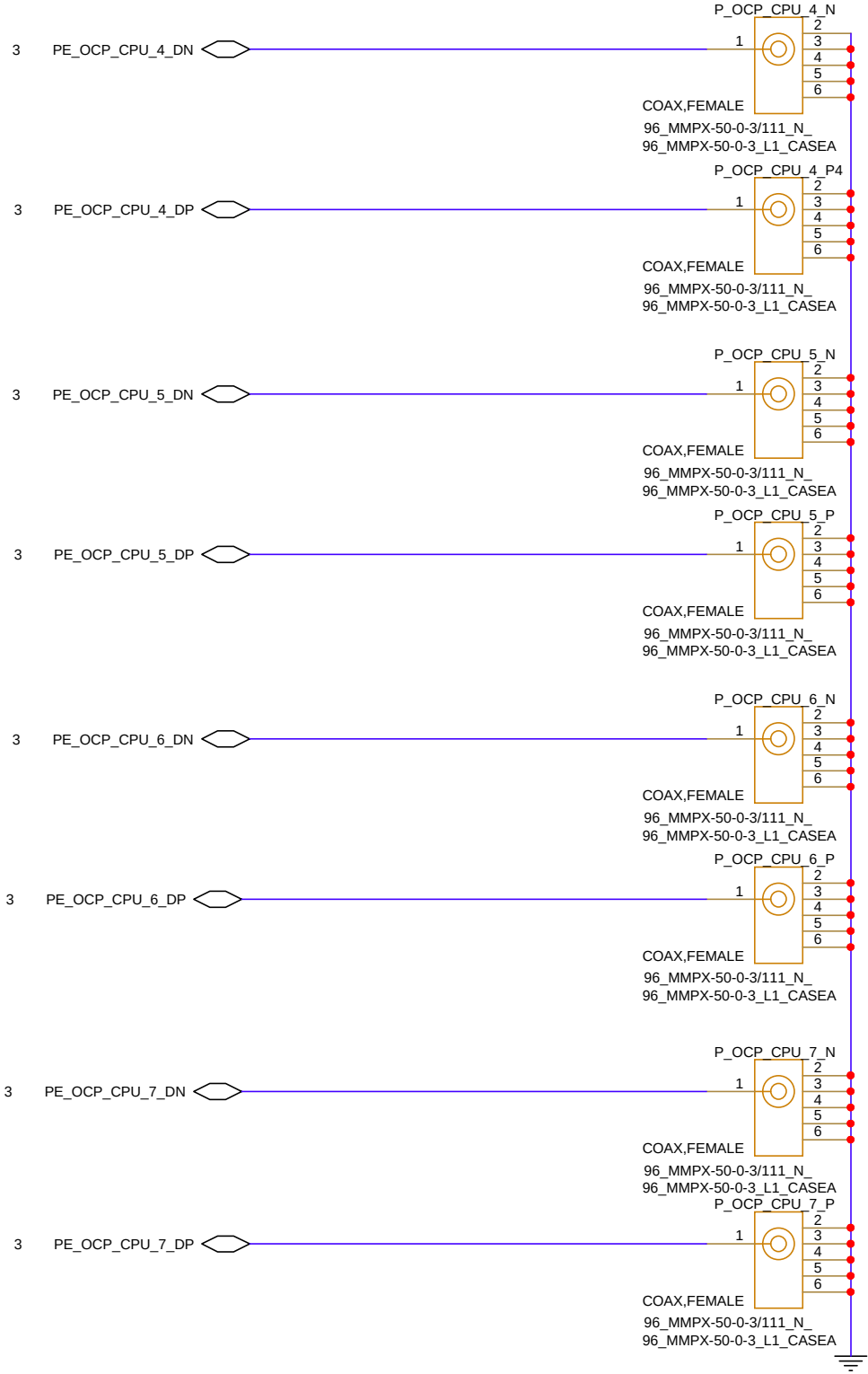
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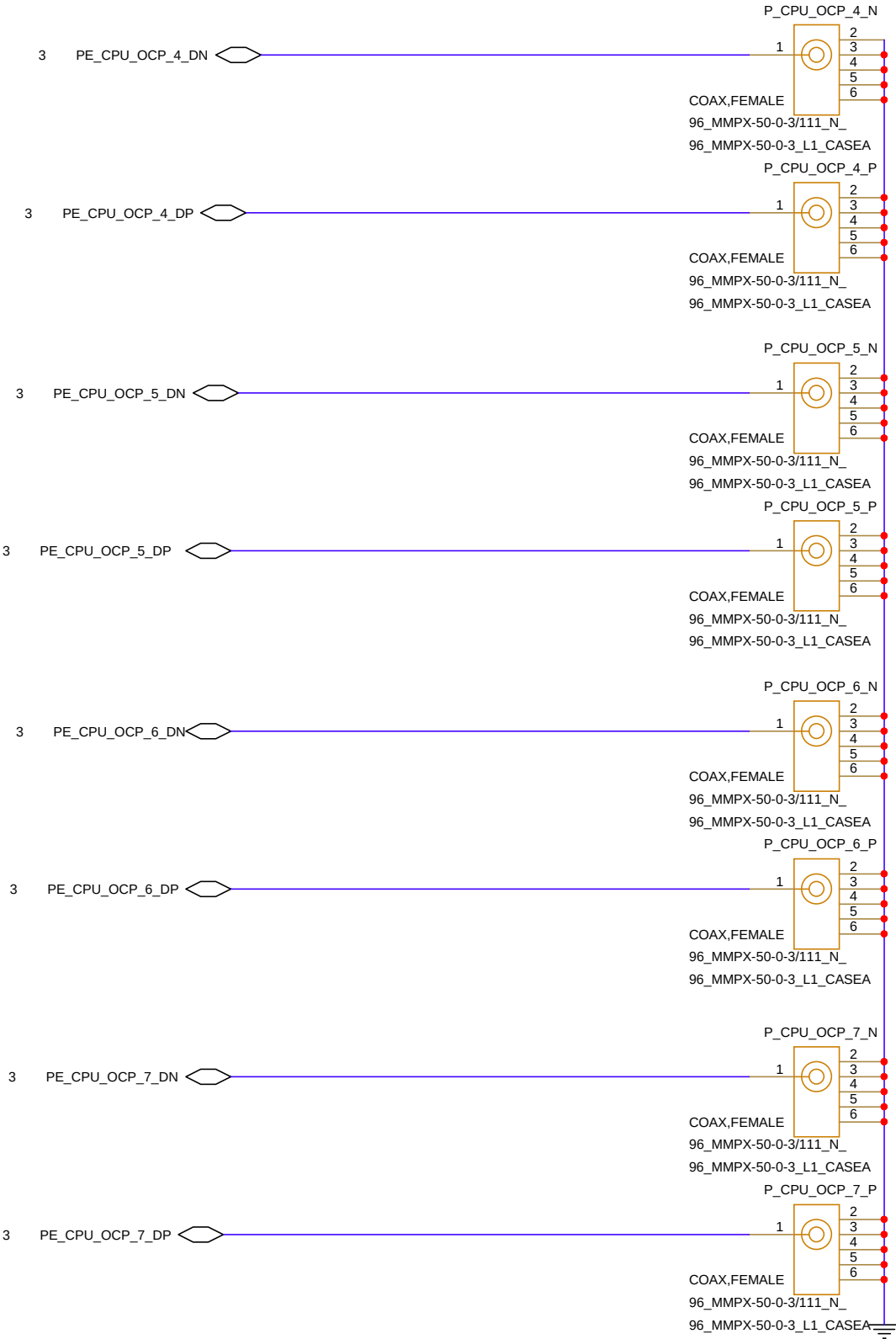
PCIe Lanes 4-7

OCP RX

OCP TX



3 PE_CPU_OCP_4_DN



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TITLE OCP3 SI TX CBB GEN 5

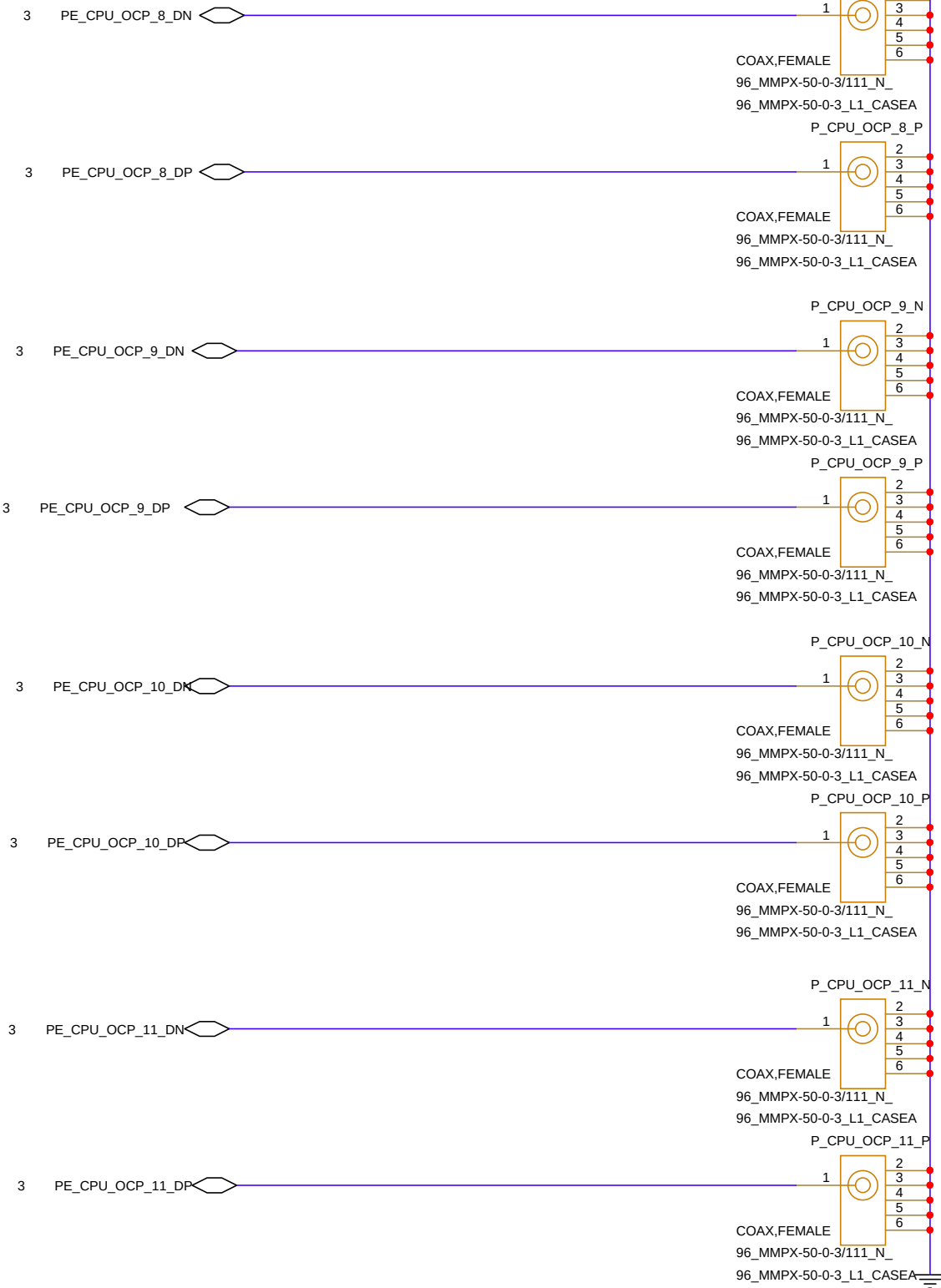
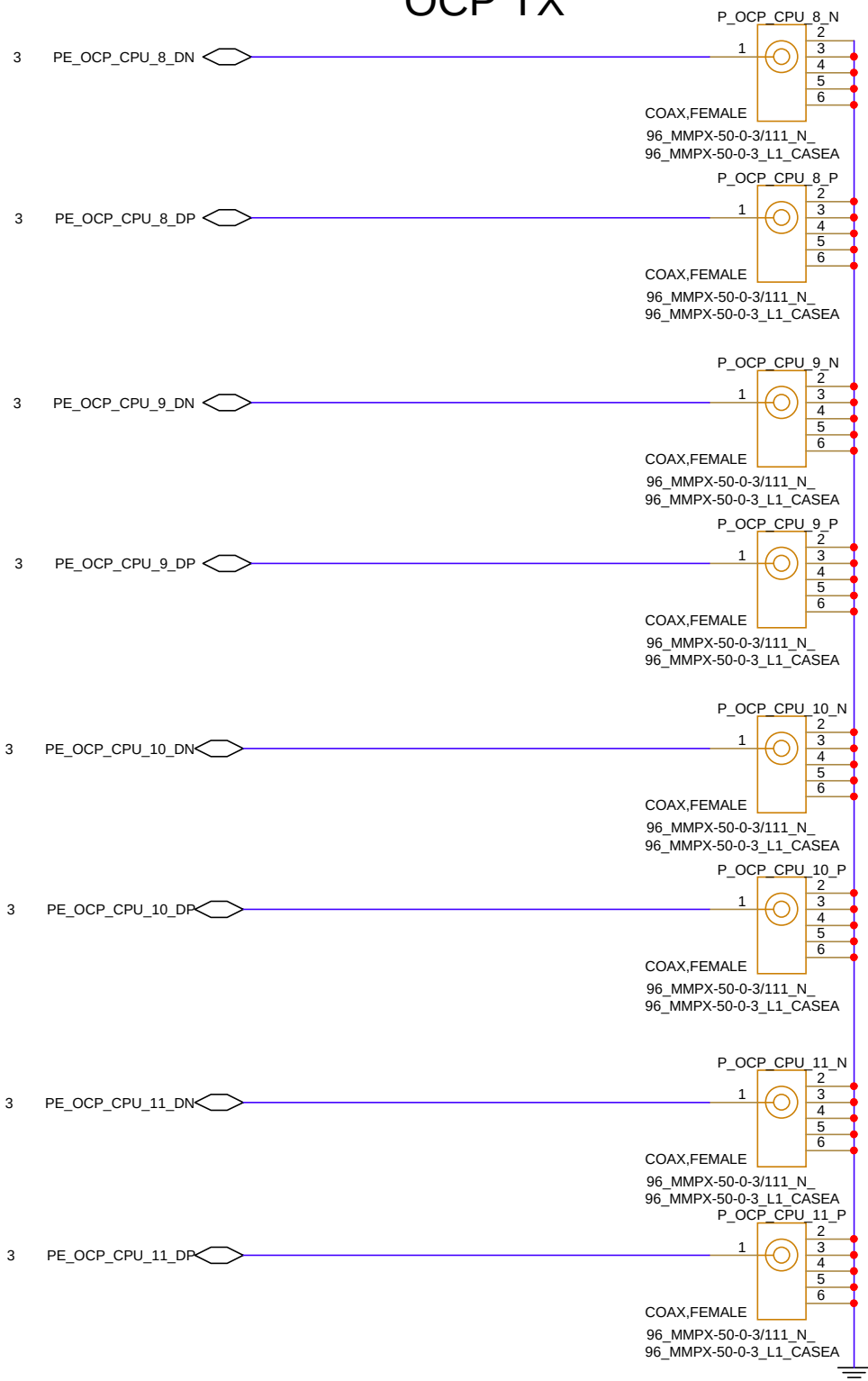
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PCIe Lanes 8-11

OCP RX

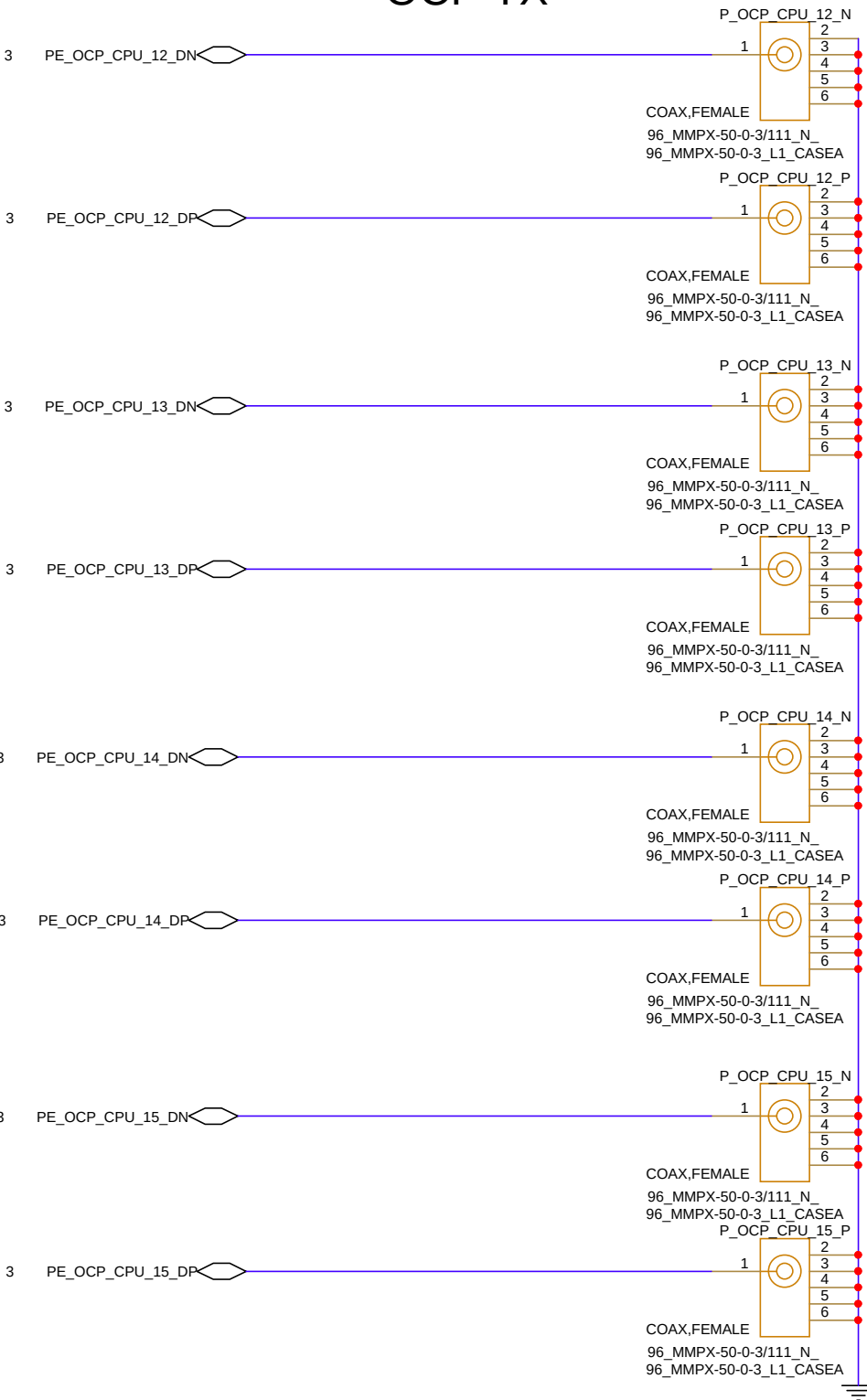
OCP TX



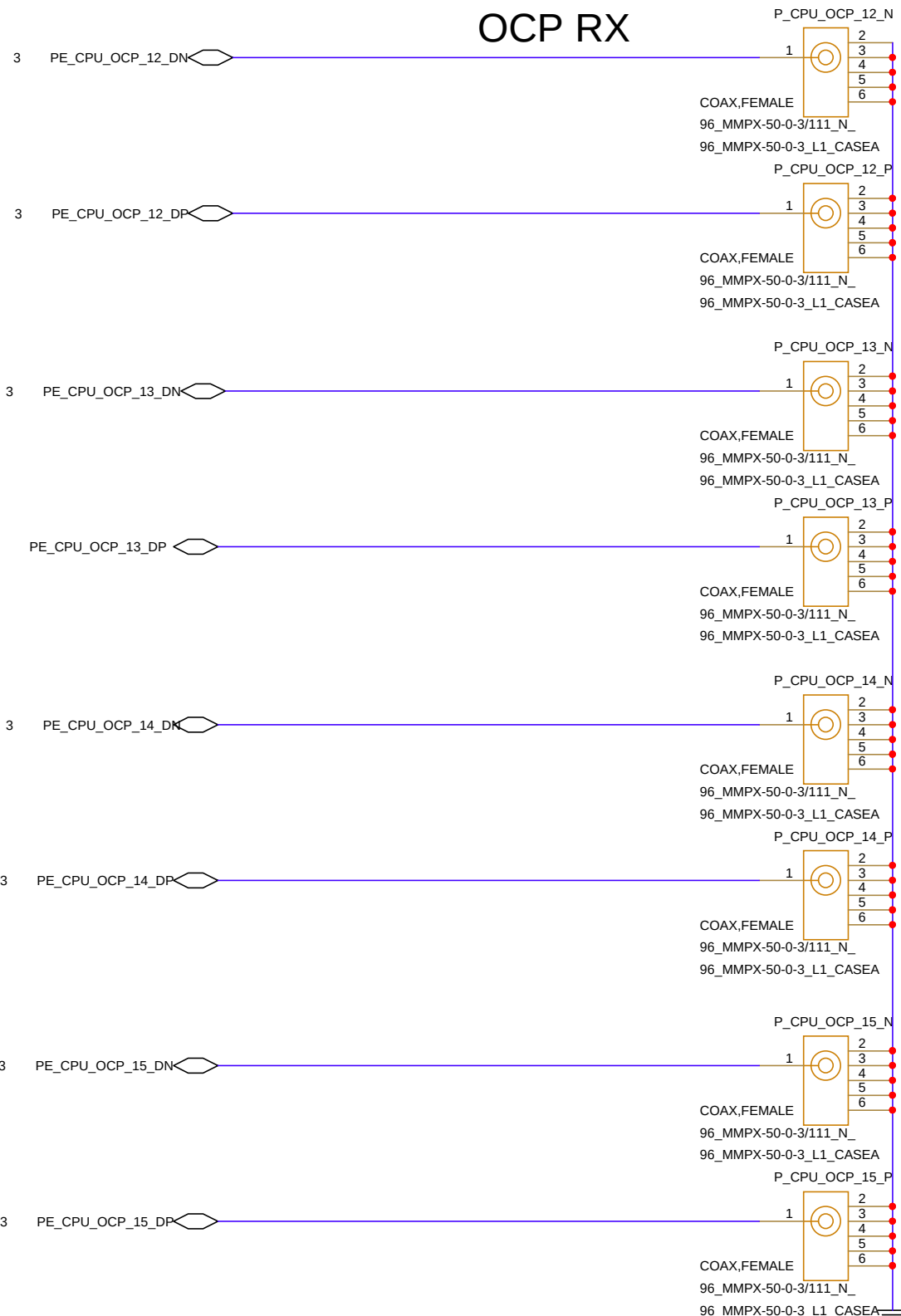
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PCIe Lanes 12-15

OCP TX

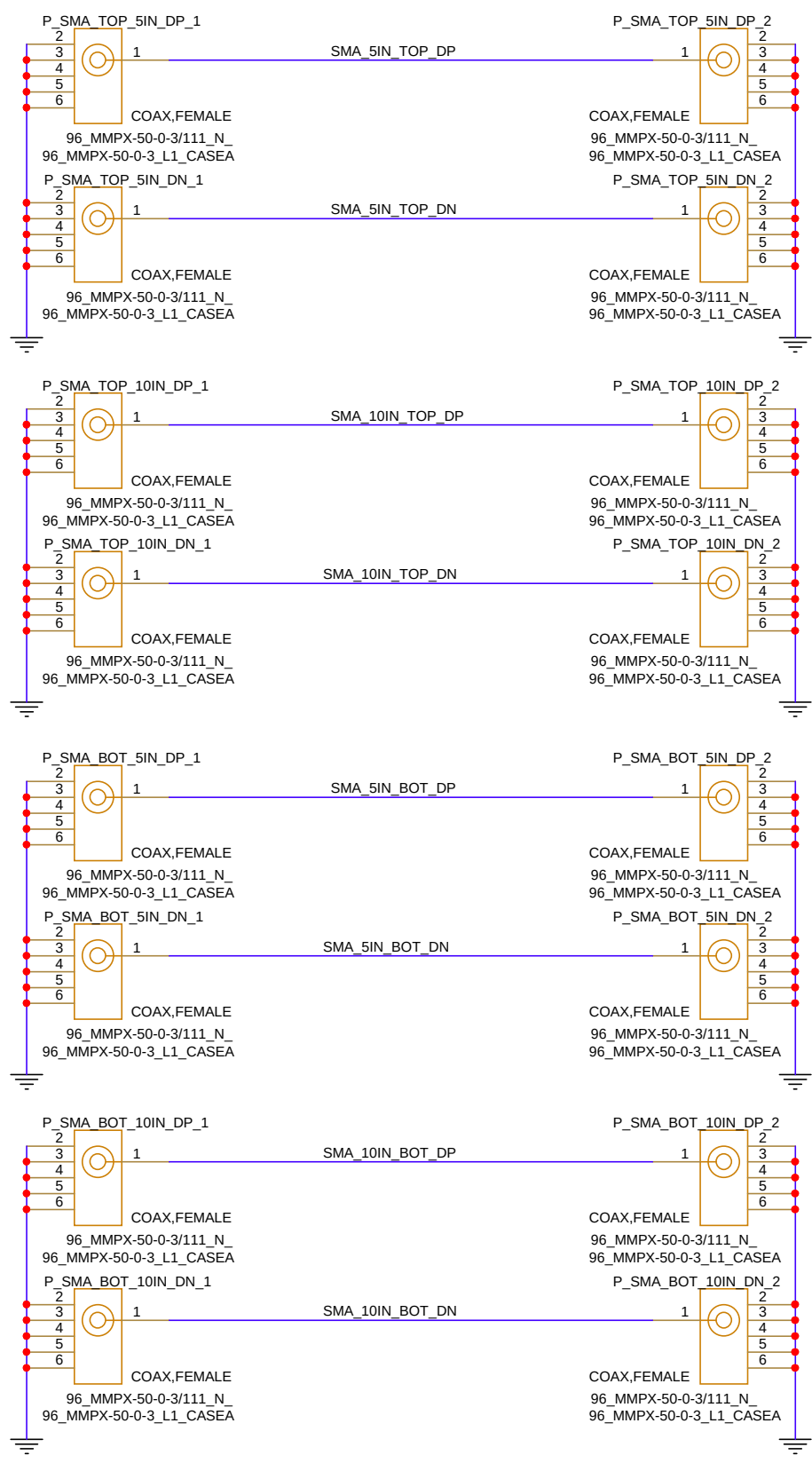


OCP RX



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MMPXs (5 in and 10 in) - Breakaway Tab 2



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CBB CALIBRATION BOARD - Breakaway Tab 1

D

C

B

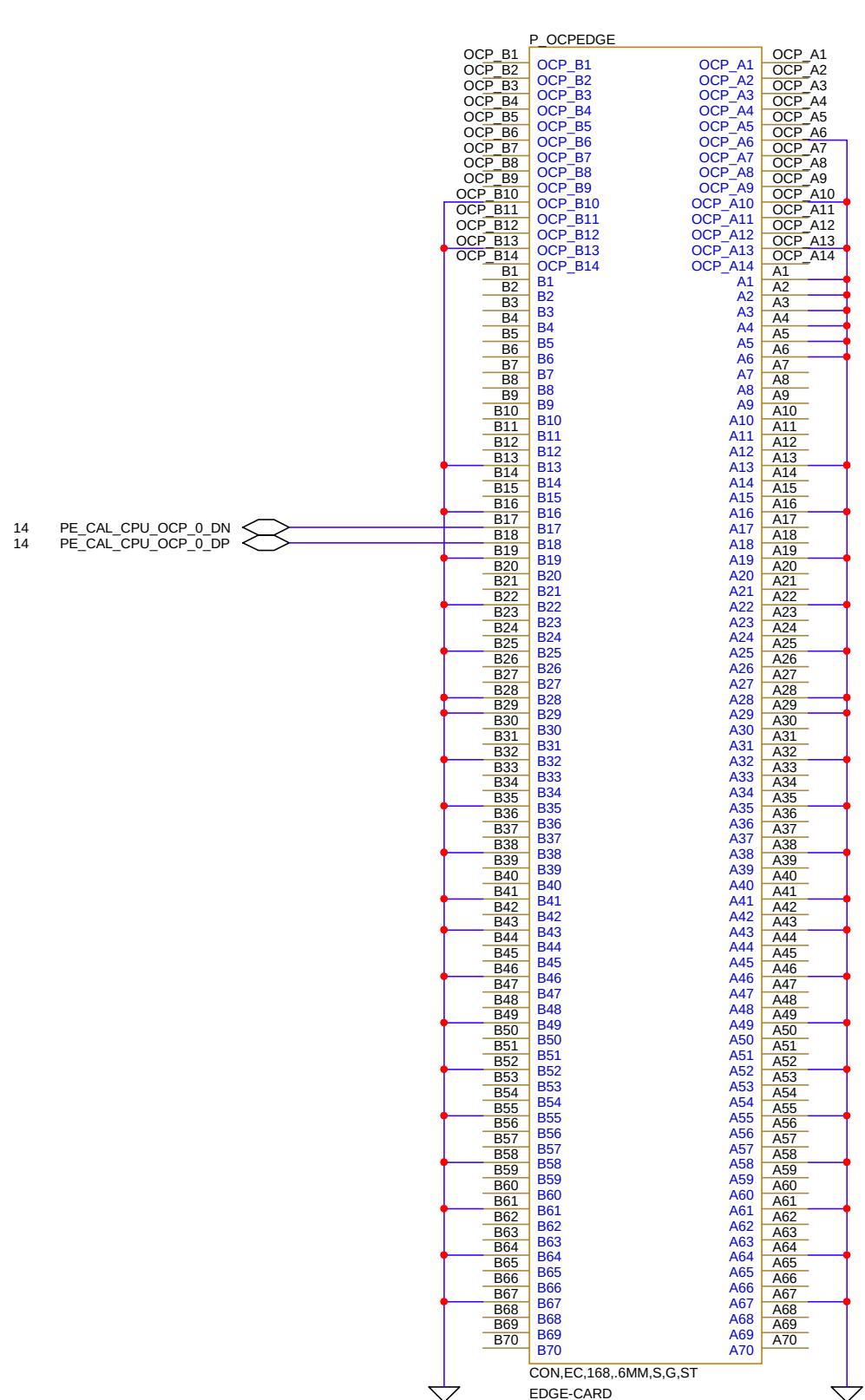
A

D

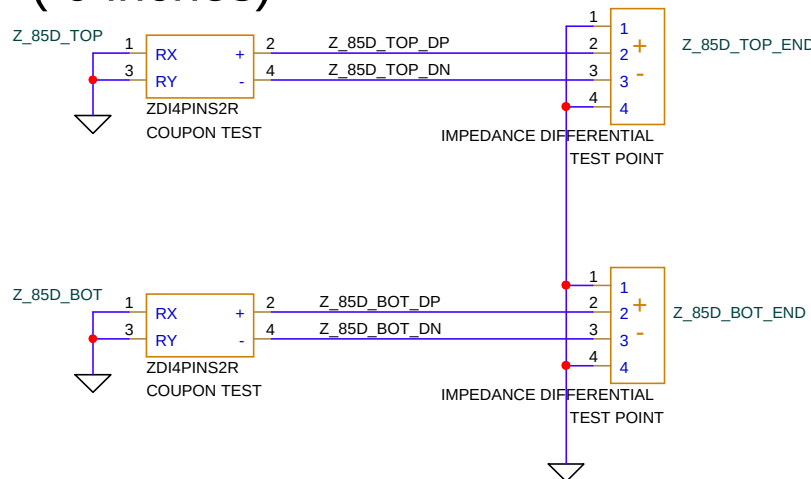
C

B

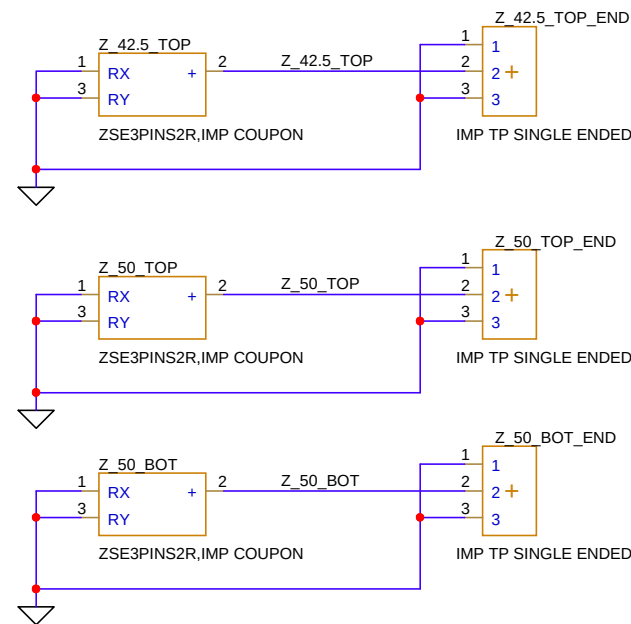
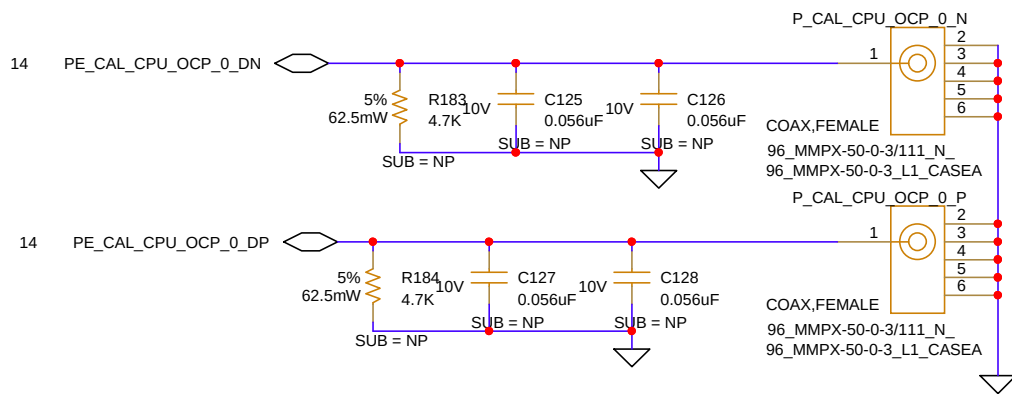
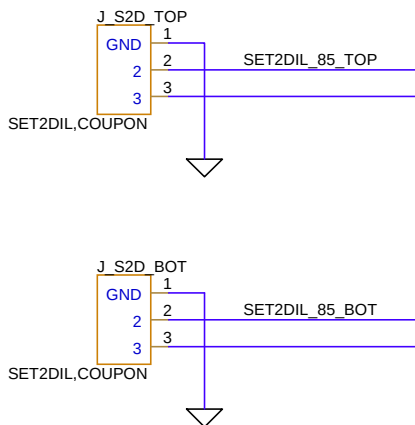
A



Impedance Coupons - Breakaway Tab 1 (6 inches)



SET 2 DIL Coupons - Breakaway Tab 1



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