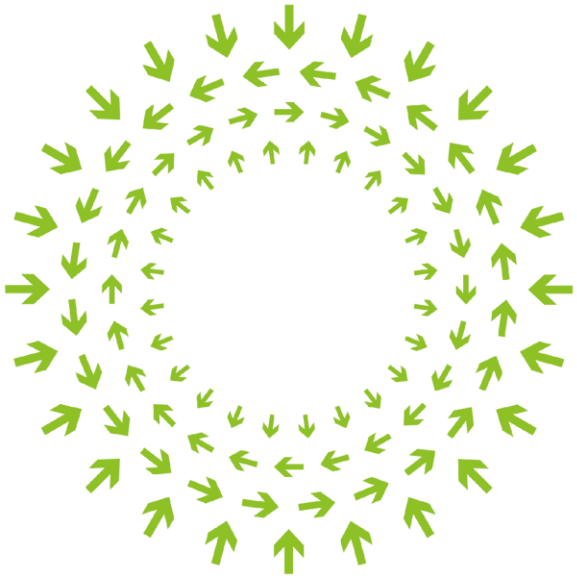


OPEN
Compute Project

OCP NIC 3.0 Design Specification

Version 1.6.0 - Release

March 31st, 2025

Author: OCP Server Workgroup, OCP NIC subgroup

Table of Contents

1 Overview 14
1.1 License 14
1.2 Acknowledgements 15
1.3 Open Compute Tenets 15
1.4 Overview 16
1.5 Non-NIC Use Cases 20
1.6 Conventions 20
1.7 References 21
1.7.1 Trademarks 22
1.8 Acronyms 23
2 Mechanical Requirements – Card Side 25
2.1 Mechanical Overview 25
2.1.1 Small Form Factor (SFF) 26
2.1.2 Tall Small Form Factor (TSFF) 26
2.1.3 Dual Small Form Factor (DSFF) 27
2.1.4 Tall Dual Small Form Factor (TDSFF) 28
2.2 Card Dimensions and Keep Out Zones 29
2.2.1 SFF Dimensions and Keep Out Zones 29
2.2.2 TSFF Dimensions and Keep Out Zones 33
2.2.3 DSFF Dimensions and Keep Out Zones 34
2.2.4 TDSFF Dimensions and Keep Out Zones 39
2.3 Card Edge Gold Finger Requirements 40
2.3.1 SFF Gold Finger Requirements 40
2.3.2 DSFF Gold Finger Requirements 40
2.3.3 Gold Finger Downshifting 40
2.3.4 Gold Finger Mating Sequence 43
2.4 Faceplate Options 45
2.4.1 SFF Faceplate Configurations 45
2.4.2 TSFF Faceplate Configurations 49
2.4.3 DSFF Faceplate Configurations 49
2.4.4 TDSFF Faceplate Configurations 51
2.5 Card Top Level Assemblies 51
2.5.1 SFF / TSFF Top Level Assemblies 52
2.5.2 DSFF / TDSFF Top Level Assemblies 53
2.6 Faceplate Subassembly 54
2.6.1 Faceplate Exploded View – SFF/TSFF 54
2.6.2 Faceplate Exploded View – DSFF/TDSFF 55
2.6.3 Generic I/O Faceplates 56
2.6.3.1 SFF Generic I/O Faceplates 56
2.6.3.2 TSFF Generic I/O Faceplates 57
2.6.3.3 DSFF Generic I/O Faceplate 59
2.6.3.4 TDSFF Generic I/O Faceplate 60
2.6.4 Ejector Levers 61
2.6.4.1 Ejector Lever (SFF) 61
2.6.4.2 Ejector Lock 62
2.6.4.3 Clinch Nut (For Ejector Levers) 63
2.6.5 SMT Nut 64
2.6.6 Faceplate Subassemblies – Bill of Materials (BOM) 65
2.7 Card Insulator / Backing Plate Requirements 67
2.7.1 SFF, TSFF Insulator 67
2.7.2 DSFF, TDSFF Insulator 69
2.7.3 DSFF, TDSFF Backing Plate 71
2.8 Card Critical-to-Function (CTF) Dimensions 73
2.8.1 CTF Tolerances 73
2.8.2 SFF CTF Dimensions 73
2.8.2.1 SFF Pull Tab CTF Dimensions 73
2.8.2.2 SFF Ejector Latch CTF Dimensions 75

2.8.2.3 SFF Internal Lock CTF Dimensions 76
2.8.3 TSFF CTF Dimensions 78
2.8.3.1 TSFF Pull Tab CTF Dimensions 78
2.8.3.2 TSFF Ejector Latch CTF Dimensions 78
2.8.3.3 TSFF Internal Lock CTF Dimensions 78
2.8.4 DSFF CTF Dimensions 79
2.8.4.1 DSFF Internal Lock CTF Dimensions 79
2.8.5 TDSFF CTF Dimensions 81
2.8.5.1 TDSFF Internal Lock CTF Dimensions 81
2.9 Labeling Requirements 82
2.9.1 General Guidelines for Label Contents 83
2.9.2 MAC Address Labeling Examples 83
2.9.2.1 MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller 84
2.9.2.2 MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controllers 84
2.9.2.3 MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers 85
2.9.2.4 MAC Address Label Example 4 – Singe Port with Quad Host, Single Managed Controller 85
2.10 Mechanical CAD Package Examples 87
3 Mechanical Requirements – Baseboard Side 88
3.1 Baseboard Connector Requirements 88
3.1.1 Connector Options 88
3.1.1.1 Right-angle Connector 88
3.1.1.2 Straddle Mount Connector 89
3.1.2 Connector Locations 91
3.1.2.1 SFF Connector Pitch 91
3.1.2.2 DSFF Connector Pitch 91
3.2 Baseboard Keep Out Zones 92
3.3 Baseboard Critical-to-Function (CTF) Requirements 92
3.3.1 CTF Tolerances 92
3.3.2 SFF Baseboard CTF Dimensions 93
3.3.3 TSFF Baseboard CTF Dimensions 95
3.3.4 DSFF Baseboard CTF Dimensions 95
3.3.5 TDSFF Baseboard CTF Dimensions 97
3.4 Card Guides 97
4 Electrical Interface Definition 98
4.1 Electrical Overview 98
4.1.1 Primary Connector 98
4.1.2 Secondary Connector 98
4.1.3 Connector Features 98
4.2 Pinout Definition 99
4.2.1 SFF Pinout 100
4.2.2 DSFF Pinout 102
4.3 DSFF Architectures 103
4.4 Line Side I/O Implementations 106
4.5 Signal Descriptions 107
4.5.1 PCIe Interface Pins 108
4.5.1.1 REFCLK[n/p][0:7] 110
4.5.1.2 PET[n/p][0:31] 110
4.5.1.3 PER[n/p][0:31] 111
4.5.1.4 PERST[0:7]# 111
4.5.1.5 WAKE[0:1]# 112
4.5.1.6 PWRBRK[0:1]# 113
4.5.1.7 PCIe Interface Topology Example 113
4.5.2 PCIe Present and Bifurcation Control Pins 114
4.5.2.1 PRSNTA[1:0]# 114
4.5.2.2 PRSNTB[7:0]# 114
4.5.2.3 BIF[5:0]# 115
4.5.2.4 PCIe Present and Bifurcation Example Topologies 115
4.5.3 SMBus Interface Pins 118

128 4.5.3.1 SMCLK[0:1] 118
129 4.5.3.2 SMDAT[0:1] 118
130 4.5.3.3 SMRST[0:1]# 119
131 4.5.3.4 SMBus Example Topology 119
132 4.5.4 NC-SI over RBT Interface / Flex I/O Pins 120
133 4.5.4.1 Interface Isolation Requirements 120
134 4.5.4.2 Flex I/O Pin Architecture 121
135 4.5.4.3 RBT Mode 121
136 4.5.4.3.1 RBT[0:1]_CLK_IN 123
137 4.5.4.3.2 RBT[0:1]_CRS_DV 123
138 4.5.4.3.3 RBT[0:1]_RXD[0:1] 123
139 4.5.4.3.4 RBT[0:1]_TX_EN 124
140 4.5.4.3.5 RBT[0:1]_TXD[0:1] 124
141 4.5.4.3.6 RBT[0:1]_ARB_OUT 124
142 4.5.4.3.7 RBT[0:1]_ARB_IN 124
143 4.5.4.3.8 RBT Example Topologies 126
144 4.5.4.4 Timing Synchronization Mode (Flex I/O) 129
145 4.5.4.4.1 TS[0:1]_TX_FREQ 130
146 4.5.4.4.2 TS[0:1]_TX_SYNC 130
147 4.5.4.4.3 TS[0:1]_RX_FREQ 131
148 4.5.4.4.4 TS[0:1]_RX_SYNC 131
149 4.5.4.4.5 TS[0:1]_GPI 131
150 4.5.4.4.6 TS[0:1]_GPO 132
151 4.5.4.4.7 TS[0:1]_RESERVED_NC 132
152 4.5.4.4.8 RBT[0:1]_ARB_OUT, RBT[0:1]_ARB_IN for SFF Timing NICs 132
153 4.5.4.4.9 Timing Synchronization Example Topology 134
154 4.5.5 Slot ID Pins 135
155 4.5.5.1 SLOT_ID[3:0] 136
156 4.5.5.2 SLOT_ID[3:0] Implementation Example 137
157 4.5.6 Scan Chain Pins 137
158 4.5.6.1 SCAN_CLK 138
159 4.5.6.2 SCAN_DATA_OUT 138
160 4.5.6.3 SCAN_DATA_IN 138
161 4.5.6.4 SCAN_LD# 138
162 4.5.6.5 Scan Chain Data Stream 139
163 4.5.6.6 Scan Chain Example Topology 145
164 4.5.7 Power Supply Pins 146
165 4.5.7.1 GND 147
166 4.5.7.2 +12V_EDGE 147
167 4.5.7.3 +3.3V_EDGE 147
168 4.5.7.4 AUX_PWR_EN[0:1] 147
169 4.5.7.5 MAIN_PWR_EN[0:1] 148
170 4.5.7.6 NIC_PWR_GOOD[0:1] 148
171 4.5.7.7 Power Supply Pins Example Topology 150
172 4.5.8 USB 2.0 (A68/A69) 151
173 4.5.8.1 USB_DAT[0:1]_p/n 151
174 4.5.8.2 USB Example Topology 152
175 4.5.9 RFU[1:4] Pins 152
176 4.5.9.1 RFU[1:4] Detailed Description 153
177 4.6 PCIe Bifurcation Mechanism 154
178 4.6.1 PCIe Present Configuration (PRSNTA[1:0]#, PRSNTB[7:0]#) 154
179 4.6.1.1 SFF PRSNTA0#, PRSNTB[3:0]# 154
180 4.6.1.2 DSFF PRSNTA, PRSNTB 154
181 4.6.2 PCIe Card Bifurcation Configuration (BIF[5:0]#) 155
182 4.6.2.1 SFF BIF[2:0]# 155
183 4.6.2.2 DSFF BIF[5:0] 155
184 4.6.3 PCIe Bifurcation Decoder 156
185 4.6.4 Bifurcation Detection Flow 158

4.6.5 PCIe Bifurcation Examples 159
4.6.5.1 Single Host (1 x16) Baseboard with a 1 x16 OCP NIC 3.0 Card (Single Controller) 159
4.6.5.2 Single Host (2 x8) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controllers) 160
4.6.5.3 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Single Controller) 161
4.6.5.4 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Quad Controllers) 162
4.6.5.5 Single Host (1 x16, no Bifurcation) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controller) 163
4.6.6 DSFF Bifurcation Discovery 164
4.7 PCIe REFCLK and PERST# Mapping 164
4.7.1 SFF REFCLK and PERST# Requirements 165
4.7.2 DSFF REFCLK and PERST# Requirements 165
4.7.3 SFF PCIe REFCLK and PERST# Mapping Examples 167
4.7.4 REFCLK and PERST# Mapping Expansion 170
4.8 Port Numbering and LED Implementations 171
4.8.1 OCP NIC 3.0 Port Naming and Port Numbering 171
4.8.2 OCP NIC 3.0 Card LED Configuration 171
4.8.3 OCP NIC 3.0 Card LED Ordering 173
4.8.4 Baseboard LEDs Configuration over the Scan Chain 174
4.9 Power State Machine 176
4.9.1 NIC Power Off 177
4.9.2 ID Mode 177
4.9.3 Aux Power Mode 178
4.9.4 Main Power Mode 178
4.9.5 Programming Mode 178
4.10 Power Supply Rail Requirements and Slot Power Envelopes 179
4.10.1 DSFF Current Sharing 181
4.11 Hot Swap Considerations for +12V_EDGE and +3.3V_EDGE Rails 181
4.12 Power Sequence Timing Requirements 183
4.12.1 Power Up Sequence Timing 183
4.12.2 Power Down Sequence Timing 184
4.12.3 Programming Mode Sequencing 185
4.12.4 Power Sequencing Timing Parameters 186
4.13 Digital I/O Specifications 187
5 Management and Pre-OS Requirements 188
5.1 Sideband Management Interface and Transport 188
5.2 NC-SI Traffic 189
5.3 Management Controller (MC) MAC Address Provisioning 189
5.3.1 MAC Address Allocation Scheme 190
5.3.2 MAC Address Allocation Scheme for Multi-Host Capable NICs 190
5.4 ASIC Die Temperature Reporting 191
5.4.1 Self-Shutdown 193
5.5 Power Consumption Reporting 193
5.6 Pluggable Transceiver Module Status and Temperature Reporting 194
5.7 Management and Pre-OS Firmware Inventory and Update 194
5.7.1 Secure Firmware 195
5.7.2 Firmware Inventory 195
5.7.3 Firmware Inventory and Update in Multi-Host Environments 195
5.8 NC-SI Package Addressing and Hardware Arbitration Requirements 196
5.8.1 NC-SI over RBT Package Addressing 196
5.8.2 Arbitration Ring Connections 196
5.9 SMBus 2.0 Addressing Requirements 196
5.9.1 SMBus Address Map 197
5.10 FRU EEPROM 197
5.10.1 FRU EEPROM Addressing and Size 197
5.10.2 FRU EEPROM Write Protection 199
5.10.3 FRU EEPROM Content Requirements 200
5.10.3.1 Base OEM Record (0xC0) 201
5.10.3.2 DSFF PCIe Link Subdivision Record 0 (0xD0) 208
5.10.3.3 DSFF PCIe Link Subdivision Record 1 (0xD1) 211

5.10.3.4 Extended OEM Record (0xD2) 212
5.10.3.5 Flex I/O OEM Record (0xD3) 214
5.10.4 FRU Template 217
6 Routing Guidelines and Signal Integrity Considerations 218
6.1 NC-SI over RBT 218
6.1.1 SFF/DSFF Baseboard Requirements 220
6.1.2 SFF/DSFF OCP NIC 3.0 Card Requirements 220
6.2 SMBus 2.0 222
6.3 PCIe 222
6.3.1 Channel Requirements 222
6.3.1.1 REFCLK requirements 222
6.3.1.2 Add-in Card Electrical Budgets 222
6.3.1.3 PCIe Gen 6 Informative Limits 223
6.3.1.4 Baseboard Channel Budget 223
6.3.1.5 SFF-TA-1002 Connector Channel Budget 224
6.3.1.6 Differential Impedance (Informative) 224
6.3.2 Test Fixtures 224
6.3.2.1 Compliance Load Board (CLB) 225
6.3.2.2 Compliance Baseboard (CBB) 226
6.3.3 Test Methodology 226
6.3.3.1 Test Setup 226
7 Thermal and Environmental 228
7.1 Airflow Direction 228
7.1.1 Hot Aisle Cooling 228
7.1.2 Cold Aisle Cooling 229
7.2 Thermal Design Guidelines 230
7.2.1 SFF Card ASIC Cooling – Hot Aisle 230
7.2.2 TSFF Card ASIC Cooling – Hot Aisle (TBD) 234
7.2.3 DSFF Card ASIC Cooling – Hot Aisle (TBD) 234
7.2.4 TDSFF Card ASIC Cooling – Hot Aisle (TBD) 234
7.2.5 SFF Card ASIC Cooling – Cold Aisle 234
7.2.6 TSFF Card ASIC Cooling – Cold Aisle (TBD) 237
7.2.7 DSFF Card ASIC Cooling – Cold Aisle (TBD) 237
7.2.8 TDSFF Card ASIC Cooling – Cold Aisle (TBD) 237
7.3 Thermal Simulation (CFD) Modeling 237
7.4 Thermal Test Fixture 237
7.4.1 Test Fixture for SFF Card 238
7.4.2 Test Fixture for TSFF Card (TBD) 240
7.4.3 Test Fixture for DSFF Card (TBD) 240
7.4.4 Test Fixture for TDSFF Card (TBD) 240
7.4.5 Test Fixture Airflow Direction 241
7.4.6 Thermal Test Fixture Candlestick Sensors 241
7.4.7 Software 244
7.5 Card Sensor Requirements 244
7.6 Card Cooling Tiers 244
7.7 Non-Operational Shock & Vibration Testing 246
7.7.1 Shock & Vibe Test Fixture 246
7.7.2 Test Procedure 247
7.8 Dye and Pull Test Method 249
7.9 Gold Finger Plating Requirements 251
7.9.1 Host Side Gold Finger Plating Requirements 251
7.9.2 Line Side Gold Finger Durability Requirements 251
8 Regulatory 252
8.1 Required Compliance 252
8.1.1 Required Environmental Compliance 252
8.1.2 Required EMC Compliance 252
8.1.3 Required Product Safety Compliance 253
8.1.4 Required Immunity (ESD) Compliance 253

8.2 Recommended Compliance 253
8.2.1 Recommended Environmental Compliance 253
8.2.2 Recommended EMC Compliance 254
9 Appendix – LFF 255
9.1 Mechanical Requirements – Card Side – LFF 255
9.1.1 Large Form Factor (LFF) 255
9.1.2 LFF Dimensions and Keep Out Zones 258
9.1.3 LFF Gold Finger Requirements 260
9.1.4 LFF Faceplate Configurations 261
9.1.5 LFF Top Level Assembly 265
9.1.6 Faceplate Subassembly – LFF 265
9.1.6.1 LFF Generic I/O Faceplate 266
9.1.6.2 Ejector Levers (LFF) 266
9.1.7 Faceplate Subassemblies – Bill of Materials (BOM) – LFF 267
9.1.8 LFF Insulator 267
9.1.9 LFF Ejector Latch CTF Dimensions 270
9.2 Mechanical Requirements – Baseboard Side – LFF 272
9.2.1 LFF Connector Pitch 272
9.2.2 LFF Baseboard CTF Dimensions 272
9.3 Electrical – LFF 274
9.3.1 LFF Pinout 274
9.3.2 Signal Descriptions 276
9.3.3 UART (A68/A69) – LFF Secondary Connector Only 276
9.3.3.1 UART_RX 276
9.3.3.2 UART_TX 276
9.3.3.3 UART Example Topology 277
9.3.4 PCIe Pins for LFF 277
9.3.4.1 LFF PRSNTA[1:0]#, PRSNTB[7:0]# 277
9.3.4.2 LFF BIF[5:0]# 277
9.3.4.3 PCIe REFCLK and PERST# Mapping – LFF 278
9.3.4.4 LFF PCIe REFCLK and PERST# Mapping 279
9.3.5 Power Supply Rail Requirements and Slot Power Envelopes for LFF 282
9.4 Signal Integrity Considerations – NC-SI over RBT – LFF 282
9.4.1 LFF Baseboard Requirements 282
9.4.2 LFF OCP NIC 3.0 Card Requirements 282
9.5 Thermal and Environmental – LFF 283
9.5.1 Thermal Design Guidelines – LFF 283
9.5.1.1 LFF Card ASIC Cooling – Hot Aisle 283
9.5.1.2 LFF Card ASIC Cooling – Cold Aisle 286
9.5.2 Test Fixture for LFF Card 288
9.5.3 Thermal Test Fixture Candlestick Sensors – LFF 289
9.5.4 Shock and Vibe Fixture – LFF 290
10 Revision History 291
10.1 Document Revision History 291
10.2 FRU Content Revision History 302

List of Figures

Figure 1: Representative SFF OCP NIC 3.0 Card with Dual QSFP Ports 17
Figure 2: Representative TSFF OCP NIC 3.0 Card with Dual QSFP Ports 18
Figure 3: Representative DSFF OCP NIC 3.0 Card in a DC-MHS M-FLW board 18
Figure 4: Representative 2x SFF OCP NIC 3.0 Cards in a DC-MHS M-FLW board 19
Figure 5: SFF Block Diagram (not to scale) 26
Figure 6: DSFF / 2xSFF Conversion (not to scale) 27
Figure 7: DSFF Block Diagram (not to scale) 28
Figure 8: SFF Keep Out Zone – Top View 29
Figure 9: SFF Keep Out Zone – Top View – Detail A 30
Figure 10: SFF Keep Out Zone – Bottom View 30
Figure 11: SFF with Backing Plate Keep Out Zone – Bottom View 31
Figure 12: SFF Keep Out Zone – Side View 31
Figure 13: SFF with Backing Plate Keep Out Zone – Side View 32
Figure 14: SFF Keep Out Zone – Side View – Detail D 32
Figure 15: SFF with Backing Plate Keep Out Zone – Side View – Detail D 32
Figure 16: TSFF Keep Out Zone – Side View 33
Figure 17: DSFF Keep Out Zone – Top View 34
Figure 18: DSFF Keep Out Zone – Top View – Detail A 35
Figure 19: DSFF with Insulator Keep Out Zone – Bottom View 36
Figure 20: DSFF with Insulator Keep Out Zone – Side View 36
Figure 21: DSFF with Backing Plate Keep Out Zone – Bottom View 37
Figure 22: DSFF with Backing Plate Keep Out Zone – Side View 37
Figure 23: DSFF with Insulator Keep Out Zone – Side View – Detail D 38
Figure 24: DSFF with Backing Plate Keep Out Zone – Side View – Detail D 38
Figure 25: TDSFF Keep Out Zone – Side View 39
Figure 26: DSFF Gold Finger Pitch – x32 – Top Side (“B” Pins) 40
Figure 27: Primary Connector (4C+) with 4C and 2C OCP NIC 3.0 SFF Cards 41
Figure 28: Primary Connector (4C+) Only Card Edge on DSFF 41
Figure 29: SFF NIC Configuration Views 46
Figure 30: SFF NIC Line Side 3D Views 47
Figure 31: SFF NIC Chassis Mounted 3D Views 48
Figure 32: TSFF NIC Configuration Views 49
Figure 33: DSFF NIC Configuration Views 50
Figure 34: TDSFF NIC Configuration Views 51
Figure 35: PBA Exploded Views (SFF, and TSFF) 52
Figure 36: PBA Exploded Views (DSFF with Insulator and Backing Plate Options) 53
Figure 37: Faceplate Assembly Exploded Views (SFF, TSFF) 54
Figure 38: Faceplate Assembly Exploded Views (DSFF, TDSFF) 55
Figure 39: SFF Generic I/O Faceplate – Pull Tab Version (2D View) 56
Figure 40: SFF Generic I/O Faceplate – Ejector Version (2D View) 56
Figure 41: SFF Generic I/O Faceplate – Internal Lock Version (2D View) 57
Figure 42: TSFF Generic I/O Faceplate – Pull Tab Version (2D View) 57
Figure 43: TSFF Generic I/O Faceplate – Ejector Version (2D View) 58
Figure 44: TSFF Generic I/O Faceplate – Internal Lock Version (2D View) 58
Figure 45: DSFF Generic I/O Faceplate – Pull Tab Version (2D View) 59
Figure 46: DSFF Generic I/O Faceplate – Internal Lock Version (2D View) 59
Figure 47: TDSFF Generic I/O Faceplate – Pull Tab Version (2D View) 60
Figure 48: TDSFF Generic I/O Faceplate – Internal Lock Version (2D View) 60
Figure 49: SFF I/O Faceplate – Ejector Lever (2D View) 61
Figure 50: Ejector Lock 62
Figure 51: Clinch Nut Option A 63
Figure 52: Clinch Nut Option B 63
Figure 53: SMT Nut CTF Dimensions 64
Figure 54: SFF, TSFF Bottom Side Insulator (3D View) 67
Figure 55: SFF, TSFF Bottom Side Insulator (Top and Side View) 68
Figure 56: SFF, TSFF Bottom Side Insulator (alternate) (Top and Side View) 69
Figure 57: DSFF, TDSFF Bottom Side Insulator (3D View) 69

Figure 58: DSFF, TDSFF Bottom Side Insulator (Top and Side View) 70
Figure 59: DSFF, TDSFF Bottom Side Backing Plate (3D View) 71
Figure 60: DSFF, TDSFF Bottom Side Backing Plate (Top and Side View) 72
Figure 61: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View) 73
Figure 62: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Front View) 74
Figure 63: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Side View) 74
Figure 64: SFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View) 75
Figure 65: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View) 75
Figure 66: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View) 76
Figure 67: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View) 76
Figure 68: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Front View) 77
Figure 69: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View) 77
Figure 70: TSFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View) 78
Figure 71: TSFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View) 78
Figure 72: TSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View) 78
Figure 73: DSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View) 79
Figure 74: DSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Front View) 80
Figure 75: DSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View) 80
Figure 76: TDSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View) 81
Figure 77: SFF Label Area Example 82
Figure 78: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller 84
Figure 79: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller 85
Figure 80: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers 85
Figure 81: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller 86
Figure 82: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller 86
Figure 83: Baseboard 4C+ and 4C Connectors – Right Angle 89
Figure 84: OCP NIC 3.0 Card and Host Offset for Right Angle Connectors 89
Figure 85: Baseboard 4C+ and 4C Connectors – Straddle Mount 90
Figure 86: Straddle Mount Connector with 0 mm Offset (Coplanar) for 1.57 mm and 2.36 mm (0.062” and 0.093”) Thick Baseboards 90
Figure 87: Straddle Mount Connector with -0.3 mm Offset for 1.93 mm (0.076”) Thick Baseboards 90
Figure 88: SFF Connector Pitch for multiple SFF slots 91
Figure 89: DSFF Connector Pitch 92
Figure 90: SFF Baseboard Chassis CTF Dimensions (Rear View) 93
Figure 91: SFF Baseboard Chassis to Card Thumb Screw CTF Dimensions (Side View) 93
Figure 92: SFF Baseboard Chassis to Ejector lever Card CTF Dimensions (Side View) 94
Figure 93: SFF Baseboard Chassis CTF Dimensions (Rear Guide Rail View) 94
Figure 94: SFF Baseboard Chassis CTF Dimensions (Guide Rail Detail) – Detail C 94
Figure 95: TSFF Baseboard Chassis CTF Dimensions (Rear View) 95
Figure 96: DSFF Baseboard Chassis CTF Dimensions (Rear View) 95
Figure 97: DSFF Baseboard Chassis CTF Dimensions (Rear Rail Guide View) 96
Figure 98: 2xSFF in DSFF Baseboard Chassis CTF Dimensions (Rear Rail Guide View) 96
Figure 99: TDSFF Baseboard Chassis CTF Dimensions (Rear View) 97
Figure 100: DSFF Architecture With a Single Silicon Device 104
Figure 101: DSFF Architecture With Dual Silicon Devices 105
Figure 102: PCIe Interface Topology Example 113
Figure 103: SFF PCIe Present and Bifurcation Pins (Baseboard Controlled BIF[2:0]#) 116
Figure 104: SFF PCIe Present and Bifurcation Pins (Static BIF[2:0]#) 116
Figure 105: DSFF PCIe Present and Bifurcation Pins (Controlled BIF[5:0]#) 117
Figure 106: Example SMBus Connections (SFF, DSFF) 119
Figure 107: NC-SI over RBT Connection Example – Single Primary Connector 126
Figure 108: NC-SI over RBT Connection Example – Dual Primary Connectors 127
Figure 109: Example Hardware Arbitration Mux Logic – Dual Primary Connectors 128
Figure 110: RBT Hardware Arbitration Logic Example for OCP Timing NIC Implementations 133
Figure 111: Flex I/O Baseboard with Timing NIC - Connection Example 134
Figure 112: Flex I/O Baseboard with RBT NIC - Connection Example 134
Figure 113: Timing Synchronization (Flex I/O) Connection Example (No RBT) 135
Figure 114: Slot ID Numbering for reconfigurable DSFF Baseboards 136

Figure 115: Scan Chain Timing Diagram Implementation 1 139
Figure 116: Scan Chain Timing Diagram Implementation 2 139
Figure 117: Scan Chain Connection Example 145
Figure 118: Example SFF Power Supply Topology 150
Figure 119: Example DSFF Power Supply Topology, Single Power Domain 150
Figure 120: USB 2.0 Connection Example – Basic Connectivity 152
Figure 121: USB 2.0 Connection Example – USB-Serial / USB-JTAG Connectivity 152
Figure 122: Single Host (1 x16) and 1 x16 OCP NIC 3.0 Card (Single Controller) 159
Figure 123: Single Host (2 x8) and 2 x8 OCP NIC 3.0 Card (Dual Controllers) 160
Figure 124: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Single Controller) 161
Figure 125: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Quad Controllers) 162
Figure 126: Single Host with no Bifurcation (1 x16) and 2 x8 OCP NIC 3.0 Card (Dual Controllers) 163
Figure 127: SFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links 167
Figure 128: SFF/ PCIe REFCLK Mapping – Dual Host – 2 and 4 links 168
Figure 129: SFF PCIe REFCLK Mapping – Quad Host – 4 Links 169
Figure 130: Port and LED Ordering – Example SFF Link/Activity and Speed LED Placement 174
Figure 131: Baseboard Power States 176
Figure 132: Power-Up Sequencing – Normal Operation 183
Figure 133: Power-Down Sequencing – Normal Operation 184
Figure 134: Programming Mode Sequencing 185
Figure 135: FRU EEPROM Writes with Double Byte Addressing 198
Figure 136: FRU EEPROM Reads with Double Byte Addressing 198
Figure 137: FRU Update Flow 199
Figure 138: OCP NIC 3.0 MultiRecord Structure 200
Figure 139: NC-SI over RBT Timing Budget Topology 219
Figure 140: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – No Clock Buffer 221
Figure 141: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – Clock Buffer 221
Figure 142: PCIe Load Board Test Fixture for OCP NIC 3.0 SFF and DSFF 225
Figure 143: PCIe Base Board Test Fixture for OCP NIC 3.0 SFF 226
Figure 144: Airflow Direction for Hot Aisle Cooling (Shown for SFF and LFF) 228
Figure 145: Airflow Direction for Cold Aisle Cooling (Shown for SFF and LFF) 229
Figure 146: ASIC Supportable Power for Hot Aisle Cooling – SFF 230
Figure 147: OCP NIC 3.0 SFF Reference Design and CFD Geometry 231
Figure 148: Server System Airflow Capability – SFF Card Hot Aisle Cooling 232
Figure 149: Server System Airflow Capability – SFF Card Hot Aisle Cooling in Aux Power Mode 233
Figure 150: ASIC Supportable Power for Cold Aisle Cooling – SFF Card 235
Figure 151: Server System Airflow Capability – SFF Cold Aisle Cooling 236
Figure 152: ASIC Supportable Power Comparison – SFF Card 236
Figure 153: SFF Thermal Test Fixture Preliminary Design 238
Figure 154: SFF Thermal Test Fixture Preliminary Design – Cover Removed 239
Figure 155: SFF Card Thermal Test Fixture PCB 239
Figure 156: Thermal Test Fixture Airflow Direction 241
Figure 157: External Thermocouple Placement for Cold Aisle Inlet Temperature Measurement 242
Figure 158: SFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow 243
Figure 159: TSFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow (TBD) 243
Figure 160: Graphical View of Card Cooling Tiers 245
Figure 161: Typical Operating Range for Hot Aisle Configurations 245
Figure 162: Typical Operating Range for Cold Aisle Configurations 246
Figure 163: SFF Shock and Vibe Fixture 247
Figure 164: DSFF Shock and Vibe Fixture 247
Figure 165: Dye and Pull Type Locations 250
Figure 166: Dye Coverage Percentage 250
Figure 167: Representative LFF OCP NIC 3.0 Card with Dual QSFP Ports 255
Figure 168: LFF Block Diagram (not to scale) 256
Figure 169: Primary Connector (4C+) and Secondary Connector (4C) LFF OCP NIC 3.0 Cards 257
Figure 170: Primary Connector (4C+) Only LFF OCP NIC 3.0 Cards 257
Figure 171: LFF Keep Out Zone – Top View 258
Figure 172: LFF Keep Out Zone – Top View – Detail A 259

Figure 173: LFF Keep Out Zone – Bottom View 259
Figure 174: LFF Keep Out Zone – Side View 260
Figure 175: LFF Keep Out Zone – Side View – Detail D 260
Figure 176: LFF (4C+ & 4C) Gold Finger Pitch – x32 – Top Side (“B” Pins) 260
Figure 177: LFF NIC Configuration Views 262
Figure 178: LFF NIC Line Side 3D Views 263
Figure 179: LFF NIC Chassis Mounted 3D Views 264
Figure 180: PBA Exploded Views (LFF) 265
Figure 181: Faceplate Assembly Exploded Views (LFF) 265
Figure 182: LFF Generic I/O Faceplate – Ejector Version (2D View) 266
Figure 183: LFF I/O Faceplate – Ejector Lever (2D View) 266
Figure 184: LFF Bottom Side Insulator (3D View) 268
Figure 185: LFF Bottom Side Insulator (Top and Side View) 269
Figure 186: LFF Bottom Side Insulator (alternate) (Top and Side View) 270
Figure 187: LFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View) 271
Figure 188: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View) 271
Figure 189: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View) 272
Figure 190: LFF Connector Pitch with Right Angle Connectors 272
Figure 191: LFF Connector Pitch with Straddle Mount Connectors 272
Figure 192: LFF Baseboard Chassis CTF Dimensions (Rear View) 273
Figure 193: LFF Baseboard Chassis CTF Dimensions (Side View) 273
Figure 194: LFF Baseboard Chassis CTF Dimensions (Guide Rail View) 273
Figure 195: LFF Baseboard Chassis CTF Dimensions (Guide Rail – Detail C) 274
Figure 196: UART Connection Example (LFF Secondary Connector only) 277
Figure 197: LFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links 279
Figure 198: LFF PCIe REFCLK Mapping – Dual Host – 2 and 4 links 280
Figure 199: LFF PCIe REFCLK Mapping – Quad Host – 4 Links 281
Figure 200: ASIC Supportable Power for Hot Aisle Cooling – LFF Card 283
Figure 201: OCP NIC 3.0 LFF Reference Design and CFD Geometry 284
Figure 202: Server System Airflow Capability – LFF Card Hot Aisle Cooling 285
Figure 203: ASIC Supportable Power for Cold Aisle Cooling – LFF Card 286
Figure 204: Server System Airflow Capability – LFF Cold Aisle Cooling 287
Figure 205: ASIC Supportable Power Comparison – LFF Card 287
Figure 206: LFF Card Thermal Test Fixture Design 288
Figure 207: LFF Card Thermal Test Fixture Design – Cover Removed 288
Figure 208: LFF Card Thermal Test Fixture PCB 289
Figure 209: LFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow 289
Figure 210: LFF Shock and Vibe Fixture 290

List of Tables

Table 1: Acknowledgements – Contributors – By Company 15
Table 2: Open Compute Tenets 15
Table 3: Example Non-NIC Use Cases 20
Table 4: Acronyms 23
Table 5: OCP NIC 3.0 Form Factor Dimensions 25
Table 6: Supported OCP NIC 3.0 Card Downshift Combinations 42
Table 7: Baseboard to OCP NIC Form Factor Compatibility Chart 43
Table 8: Contact Mating Sequence for the Card Gold Fingers / Connector 43
Table 9: Bill of Materials for the SFF and TSFF Faceplate Assemblies 65
Table 10: Bill of Materials for the DSFF and TDSFF Faceplate Assemblies 66
Table 11: CTF Default Tolerances 73
Table 12: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller 84
Table 13: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller 84
Table 14: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controller 85
Table 15: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller 86
Table 16: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller 86
Table 17: Baseboard Right Angle Connector Options 88
Table 18: Baseboard Straddle Mount Connector Options 89
Table 19: CTF Default Tolerances 92
Table 20: SFF Pin Definition (x16) 100
Table 21: DSFF Pin Definition (x32) 102
Table 22: OCP NIC 3.0 Line Side I/O Implementations 106
Table 23: Line Side I/O Cross Reference to Industry Standards 106
Table 24: Pin Descriptions – PCIe 108
Table 25: Pin Descriptions – PCIe Present and Bifurcation Control Pins 114
Table 26: Pin Descriptions – SMBus 118
Table 27: Flex I/O Mode Selection Truth Table 120
Table 28: Pin Descriptions – Flex I/O Pin Architecture 121
Table 29: RBT_ISOLATE# Truth Table 122
Table 30: Pin Descriptions – NC-SI over RBT 122
Table 31: Hardware Arbitration Mux Logic Truth Table 128
Table 32: FLEXIO_SEL[1:0] Truth Table 129
Table 33: Pin Descriptions – Time Synchronization Mode 129
Table 34: Pin Descriptions – SLOT_ID[1:0] 135
Table 35: Slot ID Numbering 136
Table 36: Pin Descriptions – Scan Chain 138
Table 37: Scan Chain Timing Requirements – Baseboard Side 140
Table 38: Scan Chain Timing Requirements – OCP NIC 3.0 Card Side 140
Table 39: Pin Descriptions – Scan Chain SCAN_DATA_OUT Bit Definition 140
Table 40: Pin Descriptions – Scan Chain SCAN_DATA_IN Bit Definition 141
Table 41: Pin Descriptions – Power (Per Connector) 146
Table 42: NIC_PWR_GOOD Pin States 149
Table 43: Pin Descriptions – USB 2.0 – 4C+ Connector only 151
Table 44: Pin Descriptions – RFU[1:4] 152
Table 45: PCIe Bifurcation Decoder for x32, x16, x8, x4, x2 and x1 Card Widths 157
Table 46: PCIe REFCLK and PERST Associations 164
Table 47: SFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2 and 4 Links 165
Table 48: DSFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2, 4 and 8 Links 166
Table 49: OCP NIC 3.0 Card LED Configuration with Two Physical LEDs per Port 172
Table 50: Available Card Functions per Power State 177
Table 51: Baseboard Power Supply Rail Requirements – Slot and Card Power Envelopes 180
Table 52: Power Sequencing Parameters 186
Table 53: Digital I/O DC specifications 187
Table 54: OCP NIC 3.0 Management Implementation Definitions 188
Table 55: Sideband Management Interface and Transport Requirements 188
Table 56: NC-SI Traffic Requirements 189
Table 57: MC MAC Address Provisioning Requirements 189

Table 58: Threshold Severity Level vs Example Threshold Values 192
Table 59: Temperature Reporting Requirements 192
Table 60: Power Consumption Reporting Requirements 193
Table 61: Pluggable Module Status Reporting Requirements 194
Table 62: Management and Pre-OS Firmware Inventory and Update Requirements 194
Table 63: Slot_ID[1:0] to Package ID[2:0] Mapping 196
Table 64: FRU EEPROM Address Map 197
Table 65: OCP NIC 3.0 MultiRecord Requirements 200
Table 66: Base OEM Record – 0xC0 201
Table 67: DSFF PCIe Link Subdivision Record 0 – 0xD0 208
Table 68: PCIe Mode Descriptor 209
Table 69: DSFF PCIe Link Subdivision Record 1 – 0xD1 211
Table 70: Extended OEM Record – 0xD2 212
Table 71: Flex I/O OEM Record – 0xD3 214
Table 72: NC-SI over RBT Timing Parameters 218
Table 73: PCIe Electrical Budgets 222
Table 74: PCIe Gen 6 Informative Limits 223
Table 75: PCIe Test Fixtures for OCP NIC 3.0 224
Table 76: Hot Aisle Air Temperature Boundary Conditions 229
Table 77: Hot Aisle Airflow Boundary Conditions 229
Table 78: Cold Aisle Air Temperature Boundary Conditions 229
Table 79: Cold Aisle Airflow Boundary Conditions 230
Table 80: Reference OCP NIC 3.0 SFF Card Geometry 231
Table 81: Card Cooling Tier Definitions (LFM) 244
Table 82: Random Vibration Testing 1.88 G_{RMS} Profile 248
Table 83: FCC Class A Radiated and Conducted Emissions Requirements Based on Geographical Location 252
Table 84: Safety Requirements 253
Table 85: Immunity (ESD) Requirements 253
Table 86: Bill of Materials for LFF Faceplate Assemblies 267
Table 87: LFF Pin Definition (x32) 274
Table 88: Pin Descriptions – UART – LFF Secondary Connector Only 276
Table 89: LFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2, 4 and 8 Links 278
Table 90: Baseboard Power Supply Rail Requirements – LFF Slot Power Envelopes 282
Table 91: Reference OCP NIC 3.0 LFF Card Geometry 284

1 Overview

Specification Opens

This document is an OCP NIC 3.0 specification **release**. The mechanical outline and electrical sections are complete and are ready for implementation.

The overall specification still contains several opens that need to be resolved prior to the next release – by end of Q2 2025:

- Thermal / Environmental
  - Thermal fixtures
  - Thermal curves
  - Thermal analysis

1.1 License

As of January 23rd, 2018, the following persons or entities have made this Specification available under the Open Compute Project Hardware License (Permissive) Version 1.0 (OCPHL-P)

- OCP NIC Subgroup

An electronic copy of the OCPHL-P is available at:

https://www.opencompute.org/documents/ocphl-permissive-v10

Your use of this Specification may be subject to other third-party rights. THIS SPECIFICATION IS PROVIDED "AS IS." The contributors expressly disclaim any warranties (express, implied, or otherwise), including implied warranties of merchantability, non-infringement, fitness for a particular purpose, or title, related to the Specification. The Specification implementer and user assume the entire risk as to implementing or otherwise using the Specification. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

1.2 Acknowledgements

The OCP NIC 3.0 specification was created under a collaboration from many OCP member companies and facilitated by the OCP NIC Subgroup under the OCP Server Workgroup.

The OCP NIC Subgroup would like to acknowledge the following member companies for their current and past contributions to the OCP NIC 3.0 specification:

Table 1: Acknowledgements – Contributors – By Company

Amphenol Corporation	Meta Platforms, Inc.
Broadcom Inc.	Molex LLC
Dell Technologies	Netronome Systems, Inc.
Hewlett Packard Enterprise Company	NVIDIA Corporation
Intel Corporation	Quanta Computer Inc.
Keysight Technologies	Spirent Communications
Lenovo Group Ltd	TE Connectivity Corporation
Marvell Semiconductor, Inc.	University of New Hampshire InterOperability Lab

1.3 Open Compute Tenets

The OCP NIC 3.0 specification meets the following Open Compute Tenets:

Table 2: Open Compute Tenets

Tenet	How this specification meets the Tenet
Openness	This is an open specification free of IP with a common goal of promoting unified board form factors for enterprise, data center, and high-performance computing applications.
Efficiency	Size-optimized card form factors are designed with thermally efficient, power-optimization feature sets to deliver the best networking performance in computational solutions.
Impact	Enables an ecosystem of removable network mezzanine cards built by multiple NIC vendors so that system developers can leverage a robust supply chain of NICs with enhanced capabilities within their portfolio of infrastructure solutions.
Scalability	Allows adopters to leverage a wide array of common remote management capabilities within the NICs to easily maintain their physical infrastructure, with a compatible pathway to utilize next-generation NICs and transceivers.
Sustainability	Utilizes a community of contributing companies to author a form factor specification that is both cost-focused and resource-efficient using common materials found in computational platforms.

1.4 Overview

The OCP NIC 3.0 specification is a follow-on to the OCP Mezz 2.0 rev 1.00 design specification. The OCP NIC 3.0 specification supports three basic card sizes, and a "tall" height variant (as designated by the "T" prefix) for two of the form-factors:

- Small Form Factor (SFF), Tall Small Form Factor (TSFF)
- Double Small Form Factor (DSFF), Tall Double Small Form Factor (TDSFF)
- Large Form Factor (LFF)

The SFF and TSFF allows for up to 16 PCIe® lanes on the card edge. The SFF and TSFF share the same board footprint and uses the same electrical parameters. The TSFF has a taller faceplate to accommodate taller optical cages, heatsinks and board level components.

The DSFF and TDSFF supports up to 32 PCIe lanes and allows compatible adjacent SFF slots to be combined into a single slot by removing the middle card guide rail. The adjacent SFF slot positions are as defined in the DC-MHS M-FLW specification and is also shown in Section 3 of this specification. DSFF capable slots are not backwards compatible with the LFF because the connectors and connector pitch are different. The DSFF and TDSFF share the same board footprint and uses the same electrical parameters. The TDSFF has a taller faceplate to accommodate taller optical cages, heatsinks and board level components.

The LFF supports up to 32 PCIe lanes in a dedicated slot and is downward compatible with an SFF when only using the primary connector. There is no Tall LFF (TLFF) for this outline.

> **Note:** LFF implementations have been deprecated in this version of the specification. System implementors are urged to use the SFF or DSFF. The majority of the LFF content has been moved to the Appendix in Section 9 for reference only. Where applicable for comparison reasons, references to the LFF are still made throughout this specification.

Unless required to distinguish mechanical and thermal differences, this specification will collectively refer to the SFF and TSFF form-factors as an SFF. Similarly, this specification will also collectively refer to the DSFF and TDSFF form-factors as an DSFF.

Compared to the OCP Mezz Card 2.0 Design Specification, the updated OCP NIC 3.0 specification provides a broader solution space for the NIC and system vendors to support the following use case scenarios:

- NICs with a higher Thermal Design Power (TDP)
- Power delivery supports up to 80 W to a single connector (SFF) card, up to 150 W to a dual connector (LFF) card, and 160 W for a dual connector (DSFF) card.

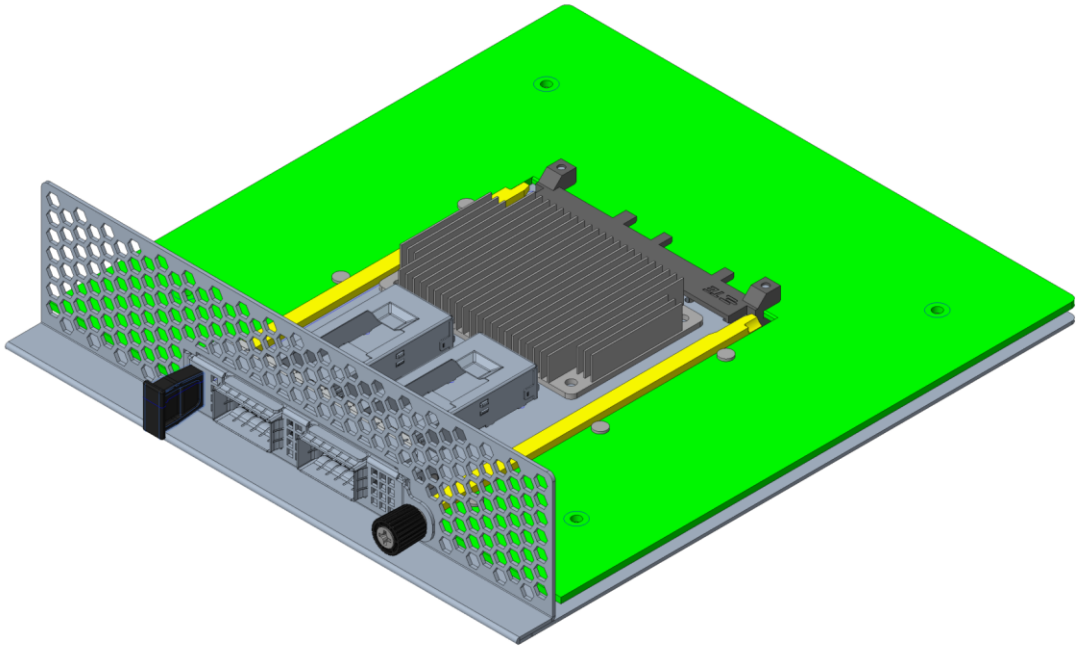
> **Note:** Baseboard vendors need to evaluate if there is sufficient airflow to thermally cool the OCP NIC 3.0 card. Refer to Section 7 for additional details.

- Support for up to PCIe Gen 5 (32 GT/s)
- Support for up to 32 lanes of PCIe per OCP NIC 3.0 card (on DSFF)
- Support for single host, multi-root complex, and multi-host environments
- Supports a greater board area for more complex OCP NIC 3.0 card designs
- Support for Smart NIC implementations with on-board DRAM and accelerators
- Simplification of FRU installation and removal while reducing overall down time

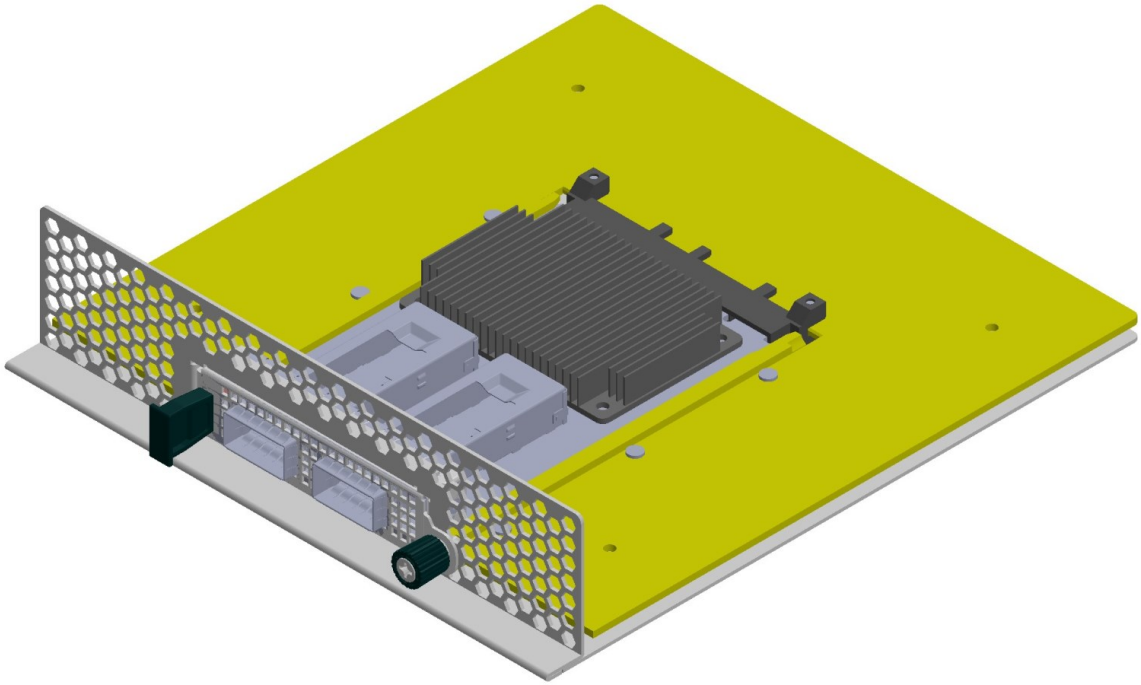
Representative OCP NIC 3.0 cards are shown in the following figures. The I/O cages are for examples only.

- Figure 1 shows a representative SFF
- Figure 2 shows a representative TSFF with a taller topside Z-height
- Figure 3 shows a representative DSFF
- Figure 4 shows a representative TDSFF also with a taller topside Z-height

Figure 1: Representative SFF OCP NIC 3.0 Card with Dual QSFP Ports

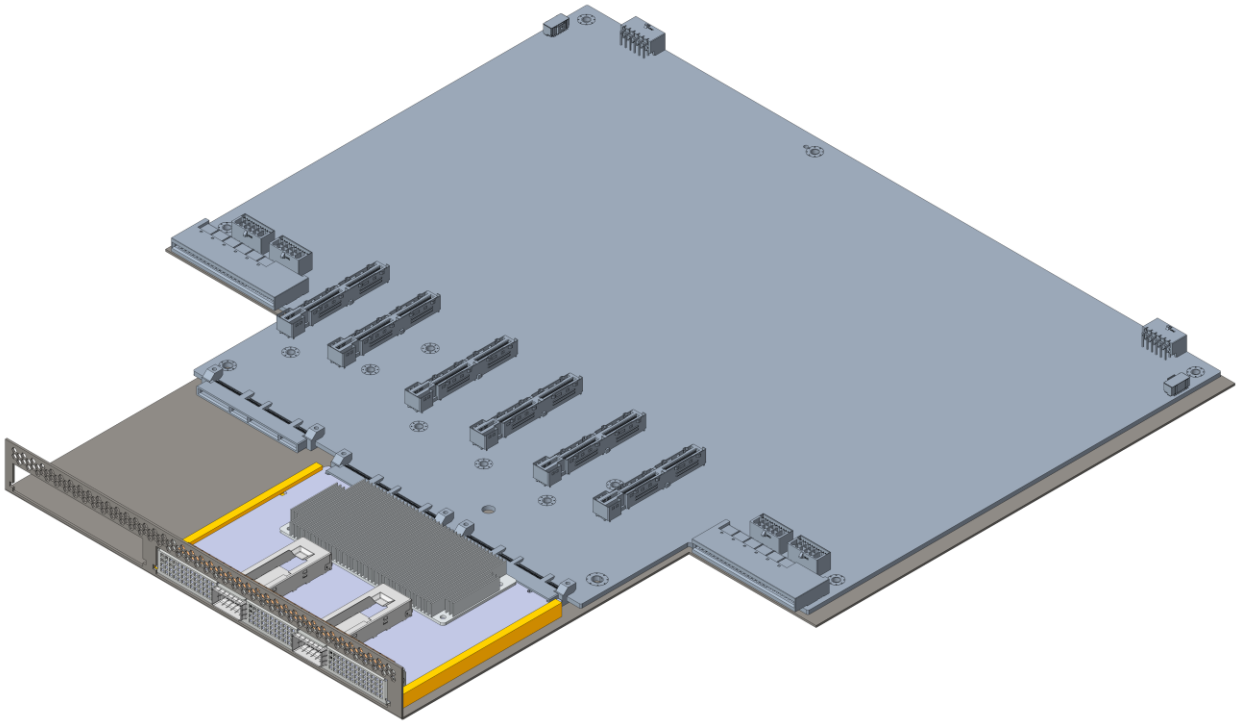


741
742 Figure 2: Representative TSFF OCP NIC 3.0 Card with Dual QSFP Ports



743
744

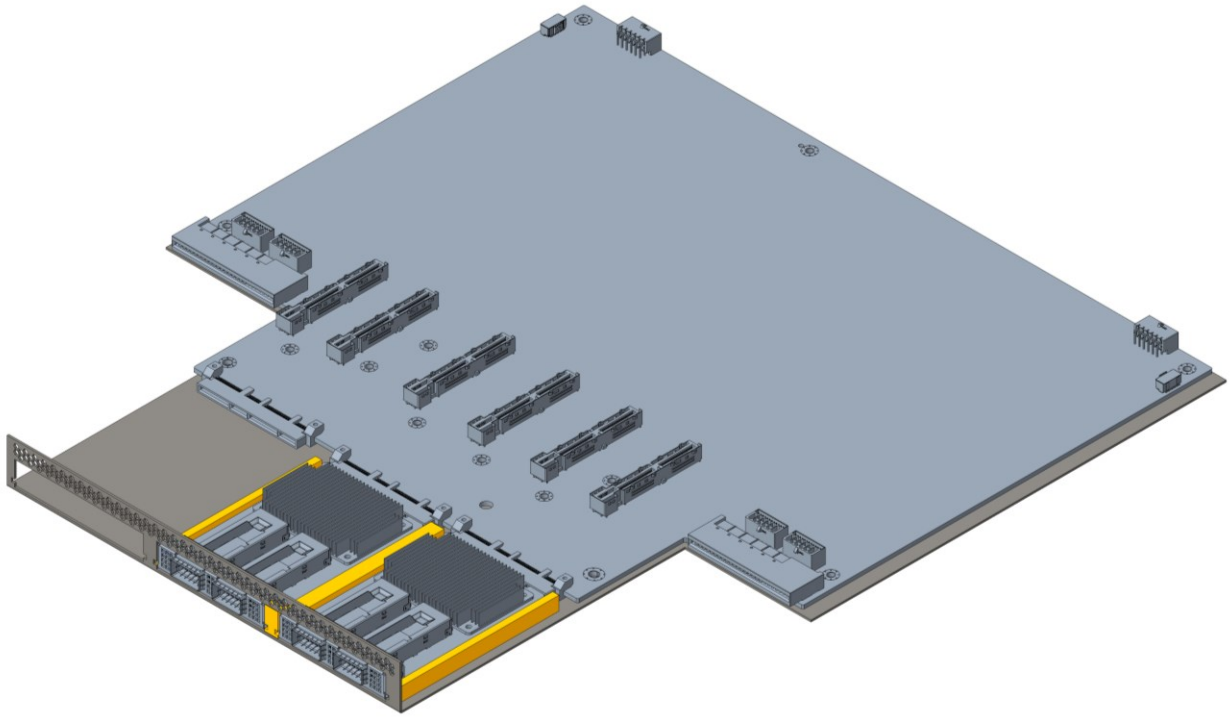
745 Figure 3: Representative DSFF OCP NIC 3.0 Card in a DC-MHS M-FLW board



746

747

748 Figure 4: Representative 2x SFF OCP NIC 3.0 Cards in a DC-MHS M-FLW board



749

750 To achieve the features outlined in this specification, OCP NIC 3.0 compliant cards are not backwards
751 compatible with OCP Mezz 2.0 cards. Further, baseboard implementations with a LFF and DSFF slot are
752 not compatible either due to the connector differences.

753 This specification is created under the OCP Server workgroup – OCP NIC subgroup. An electronic copy of
754 this specification can be found on the Open Compute Project and the OCP Marketplace websites:

755 • https://www.opencompute.org/wiki/Server/NIC#Released_Specification_Docs
756 • https://www.opencompute.org/contributions?query=OCP%20NIC%203.0
757
758

1.5 Non-NIC Use Cases

The OCP NIC 3.0 specification is mainly targeted for Network Interface Card applications. It is possible to use the same electrical and mechanical design to enable non-NIC use cases. The non-NIC use cases are not covered in the current revision of the OCP NIC 3.0 specification. Example non-NIC use cases implement various external I/O interfaces and are shown in Table 3.

Table 3: Example Non-NIC Use Cases

Example Use Case	Card External I/O Interface(s)
PCIe Retimer Card	PCIe
Accelerator Card	N/A
NVMe Card	N/A
Storage HBA / RAID Card	I/O Interface to be determined in future specification release.
Timing synchronization card	SMA / SMB (or similar) connectors

1.6 Conventions

The OCP NIC 3.0 specification adopts the following convention for numerical representations:

- Hexadecimal numbers are written with a 0x prefix with the most significant byte first – such as 0xFFFF
- Binary numbers are written with a 0b prefix with the most significant bit first – such as 0b0101
- Decimal numbers are indicated without any prefix (such as 25)

The unit representations are implemented per the International Bureau of Weights and measures (Bureau International des Poids et Mesures) (BIPM). The value and unit are separated by a space. The SI symbol and appropriate SI prefix are used (such as 50 °C, 15 A and 200 kΩ).

1.7 References

- DMTF Standard. DSP0222, Network Controller Sideband Interface (NC-SI) Specification. Distributed Management Task Force (DMTF), Rev 1.2.0, August 28th, 2023.
- DMTF Standard. DSP0236, Management Component Transport Protocol (MCTP) Base Specification. Distributed Management Task Force (DMTF), Rev 1.3.0, November 24th, 2016.
- DMTF Standard. DSP0237, Management Component Transport Protocol (MCTP) over SMBus/I^2C Transport Binding Specification. Distributed Management Task Force (DMTF), Rev 1.1.0, May 21st, 2017.
- DMTF Standard. DSP0238, Management Component Transport Protocol (MCTP) over PCIe VDM Transport Binding Specification. Distributed Management Task Force (DMTF), Rev 1.0.2, December 7th, 2014.
- DMTF Standard. DSP0239, MCTP IDs and Codes Specification. Distributed Management Task Force (DMTF), Rev 1.5.0, December 17th, 2017.
- DMTF Standard. DSP0240, Platform Level Data Model (PLDM) Base Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, April 23rd, 2009.
- DMTF Standard. DSP0240, Platform Level Data Model (PLDM) over MCTP Binding Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, April 23rd, 2009.
- DMTF Standard. DSP0245, Platform Level Data Model (PLDM) IDs and Codes Specification. Distributed Management Task Force (DMTF), Rev 1.2.0, November 24th, 2016.
- DMTF Standard. DSP0248, Platform Level Data Model (PLDM) for Platform Monitoring and Control Specification. Distributed Management Task Force (DMTF), Rev 1.1.1, January 10th, 2017.
- DMTF Standard. DSP0249, Platform Level Data Model (PLDM) State Sets Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, March 16th, 2009.
- DMTF Standard. DSP0283, Management Component Transport Protocol (MCTP) over USB Binding Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, November 7th, 2023.
- DMTF Standard. DSP0261, NC-SI over MCTP Binding Specification. Distributed Management Task Force (DMTF), Rev 1.2.0, August 26th, 2017.
- DMTF Standard. DSP0267, Platform Level Data Model (PLDM) for Firmware Update Specification. Distributed Management Task Force (DMTF), Rev 1.0.1, March 28th, 2018.
- DMTF Standard. DSP2054, PLDM NIC Modeling. Distributed Management Task Force (DMTF), Rev 1.0.0, December 18th, 2019.
- EDSFF. Enterprise and Datacenter SSD Form Factor Connector Specification. Enterprise and Datacenter SSD Form Factor Working Group, Rev 0.9 (draft), August 2nd, 2017.
- IPC. IPC-TM-650 Test Methods Manual number 2.4.53. Dye and Pull Test Method (Formerly Known as Dye and Pry), Association Connecting Electronics Industries, August 2017.
- IPMI Platform Management FRU Information Storage Definition, v1.0 Document Revision 1.3, March 24th, 2015.
- National Institute of Standards and Technology (NIST). Special Publication 800-193, Platform Firmware Resiliency Guidelines, May 2018.
- NXP Semiconductors. I^2C-bus specification and user manual. NXP Semiconductors, Rev 6, April 4th, 2014.
- OSFP MSA. Online. OSFP Octal Small Form Factor Pluggable Module, Revision 5.1, September 12th, 2024.
- Open Compute Project. OCP Data Center – Modular Hardware System (DC-MHS) Subgroup. Online. M-FLW Base Specification, Revision 1. 1 RC2, April 5th, 2024.
  https://www.opencompute.org/wiki/Server/DC-MHS

- Open Compute Project. OCP Data Center – Modular Hardware System (DC-MHS) Subgroup. Online. M-SDNO Base Specification, Revision 0.9 RC2, April 18th, 2024. https://www.opencompute.org/wiki/Server/DC-MHS
- Open Compute Project. OCP NIC Subgroup. Online. https://www.opencompute.org/wiki/Server/NIC
- PCI-SIG®. PCI Express® Base Specification, Revision 3.0 December 7th, 2015.
- PCI-SIG®. PCI Express® Base Specification, Revision 4.0 Version 1.0, October 5th, 2017.
- PCI-SIG®. PCI Express® Base Specification, Revision 5.0 Version 1.0, May 28th, 2019.
- PCI-SIG®. PCI Express® Base Specification, Revision 6.2 Version 1.0, January 25th, 2024.
- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 3.0, July 21st, 2013.
- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 4.0, September 2nd, 2019.
- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 5.1, August 17th, 2023.
- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 6.0 Draft 0.9, September 5th, 2024.
- SMBus Management Interface Forum. System Management Bus (SMBus) Specification. System Management Interface Forum, Inc, Version 2.0, August 3rd, 2000.
- SNIA. SFF-8472, Management Interface for SFP+. SNIA SFF TWG Technology Affiliate, Rev 12.4, March 21st, 2021.
- SNIA. SFF-8636, Management Interface for 4-lane Modules and Cables. SNIA SFF TWG Technology Affiliate, Rev 2.10a, September 24th, 2019.
- SNIA. SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector. SNIA SFF TWG Technology Affiliate, Rev 1.5, April 29th, 2024.
- UEFI Specification Version 2.5, http://www.uefi.org/sites/default/files/resources/UEFI%202_5.pdf, April 2015.
- USB Implementers Forum. Universal Serial Bus Communications Class Subclass Specification for Ethernet Emulation Model Devices, Revision 1.0, February 2nd, 2005.
- USB Implementers Forum. Universal Serial Bus Specification, Revision 2.0, April 27th, 2000.

1.7.1 Trademarks

Names and brands may be claimed as trademarks by their respective companies.

- I^2C® is a trademark of NXP Semiconductor.
- NVMe® is a trademark of NVM Express, Inc.
- PCIe® and PCI Express® are the registered trademarks of PCI-SIG.

1.8 Acronyms

For the purposes of the OCP NIC 3.0 specification, the following acronyms apply:

Table 4: Acronyms

Acronym	Definition
AIC	Add-in Card
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
BMC	Baseboard Management Controller
BOM	Bill of Materials
CAD	Computer Aided Design
CBB	Compliance Base Board
CEM	Card Electromechanical
CFD	Computational Fluid Dynamics
CFM	Cubic Feet per Minute
CLB	Compliance Load Board
CTD	Chain of Trust for Detection
CTF	Critical to Function
CTU	Chain of Trust for Update
DC-MHS	Data Center Modular Hardware System
DMTF	Distributed Management Task Force
DRAM	Dynamic Random Access Memory
DSFF	Dual Small Form Factor
EDSFF	Enterprise and Datacenter SSD Form Factor
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
EU	European Union
FCC	Federal Communications Commission
FRU	Field Replaceable Unit
HPM	Host Processor Module (from DC-MHS)
I/O	Input / Output
I2C	Inter-Integrated Circuit - two wire serial protocol
IEC	International Electrotechnical Commission
IPC	Institute for Printed Circuits
IPMI	Intelligent Platform Management Interface
ISO	International Organization for Standardization
LED	Light Emitting Diode
LFF	Large Form Factor
LFM	Linear Feet per Minute
MAC	Media Access Control
MC	Management Controller
MCTP	Management Component Transport Protocol
ME	Management Entity
M-FLW	Modular Full Width HPM (From DC-MHS)
MSA	Multi-source Agreement
M-SDNO	Modular Scalable Density Optimized (From DC-MHS)

Acronym	Definition
NC	No Connect
NC-SI	Network Controller Sideband Interface
NEBS	Network Equipment Building-System
NIC	Network Interface Card
OCP	Open Compute Project
ODM	Original Design Manufacturer
OEM	Original Equipment Manufacturer
OSFP-RHS	Octal Small Form Factor Pluggable Riding Heat Sink
PBA	Printed Board Assembly
PCB	Printed Circuit Board
PCI™	Peripheral Component Interconnect
PCIe®	PCI Express®
PDR	Platform Descriptor Record
PLDM	Platform Level Data Model
QSFP	Quad Small Form Factor Pluggable
QSFP-DD	Quad Small Form Factor Pluggable Double Density
QZ	Quiet Zone
RA	Right Angle
RBT	RMII Based Transport
REACH	Registration, Evaluation, Authorization and Restriction of Chemicals
RFU	Reserved Future Use
RJ45	Registered Jack 45 (IEC 60603-7 8P8C connector)
RoHS	Restriction of Hazardous Substances Directive
RSVD	Reserved
RTU	Root of Trust for Update
SFF	Small Form Factor
SFP	Small Form Factor Pluggable
SMBus	System Management Bus
SMT	Surface Mount Technology
TBD	To be Determined
TDP	Thermal Design Power
TDSFF	Tall Dual Small Form Factor
TSFF	Tall Small Form Factor
UART	Universal Asynchronous Receiver-Transmitter
UDID	Unique Device Identifier for each SMBus device. Refer to the SMBus 2.0 specification for the field definition.
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
VDM	Vendor Defined Messages
VR	Voltage Regulator
WEEE	Waste Electrical and Electronic Equipment

859

2 Mechanical Requirements – Card Side

2.1 Mechanical Overview

The OCP NIC 3.0 specification defines a third-generation mechanical form factor that allows for interoperability between compliant baseboards and OCP NIC 3.0 cards. There are three form-factors and two heights. Each card uses one or two mating connectors on the baseboard. The overall form factor dimensions, required connector types, and connector pitch are summarized in Table 5.

Table 5: OCP NIC 3.0 Form Factor Dimensions

Form Factor	Width (mm)	Depth (mm)	Z-height (mm)	Primary Connector	Secondary Connector	Primary / Secondary Connector Pitch (mm)	Typical Use Case
SFF	76.00 (W1)	115.00	11.50	4C+	N/A	89.00 See Note 1	Low profile NIC with a similar profile as an OCP NIC 2.0 card; up to 16 PCIe lanes.
TSFF			14.20				Higher thermal dissipation compared to SFF cards with the additional Z-height.
DSFF	157.55 (W3)	115.00	11.50	4C+	4C+	81.55	Larger PCB width to support additional components; up to 32 PCIe lanes. Compatible with DC-MHS M-FLW boards.
TDSFF			14.20				Higher thermal dissipation compared to DSFF cards with the additional Z-height.
LFF[2]	139.00 (W2)	115.00	11.50	4C+	4C	63.00	Larger PCB width to support additional components; up to 32 PCIe lanes. This form factor is deprecated.

Note 1: This is the minimum connector pitch to support adjacent SFF/TSFF cards for all faceplate variants (thumbscrew, ejector latch and internal lock). This dimension is not applicable for single SFF/TSFF slot baseboards.

Note 2: The LFF is a deprecated form-factor. The OCP NIC 3.0 workgroup strongly encourages the use of the SFF and the DSFF moving forward. The bulk of the LFF content has been moved to Section 9 for reference only.

These form factors support a Primary Connector and an optional Secondary Connector. The Primary Connector shall always be an SFF-TA-1002 compliant 4C+ connector and is used in all the form-factor offerings. The 4C+ connector is a 4C compliant implementation plus a 28-pin “OCP bay” for OCP NIC 3.0 specific pins. The Secondary Connector is defined to be one of two options: a 4C connector for the LFF, or a 4C+ for a DSFF.

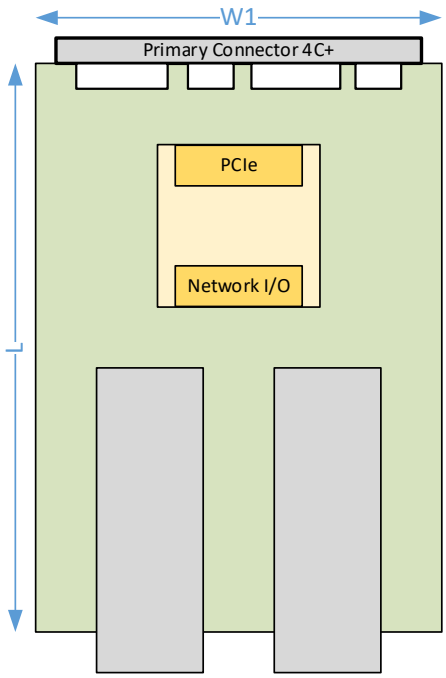
All mechanical board assemblies shall meet the safety requirements described in Section 8.1.3.

2.1.1 Small Form Factor (SFF)

The Small Form Factor (SFF) uses a single 4C+ Primary Connector, with corresponding 4C+ gold fingers. The SFF provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ45 for BASE-T operation. These were the minimum design targets for the SFF. Card vendors may use any I/O that fit within the faceplate connector region.

The SFF supports up to 80 W of delivered power to the card edge. Actual cooling capacity for a SFF card is dependent on the ambient conditions over the NIC. An example SFF block diagram is shown in Figure 5. The components shown in the figure are for illustrative purposes only.

Figure 5: SFF Block Diagram (not to scale)



2.1.2 Tall Small Form Factor (TSFF)

The Tall Small Form Factor (TSFF) is like the SFF. It shares the same PCB outline, connector and gold finger requirements and electrical parameters as the SFF.

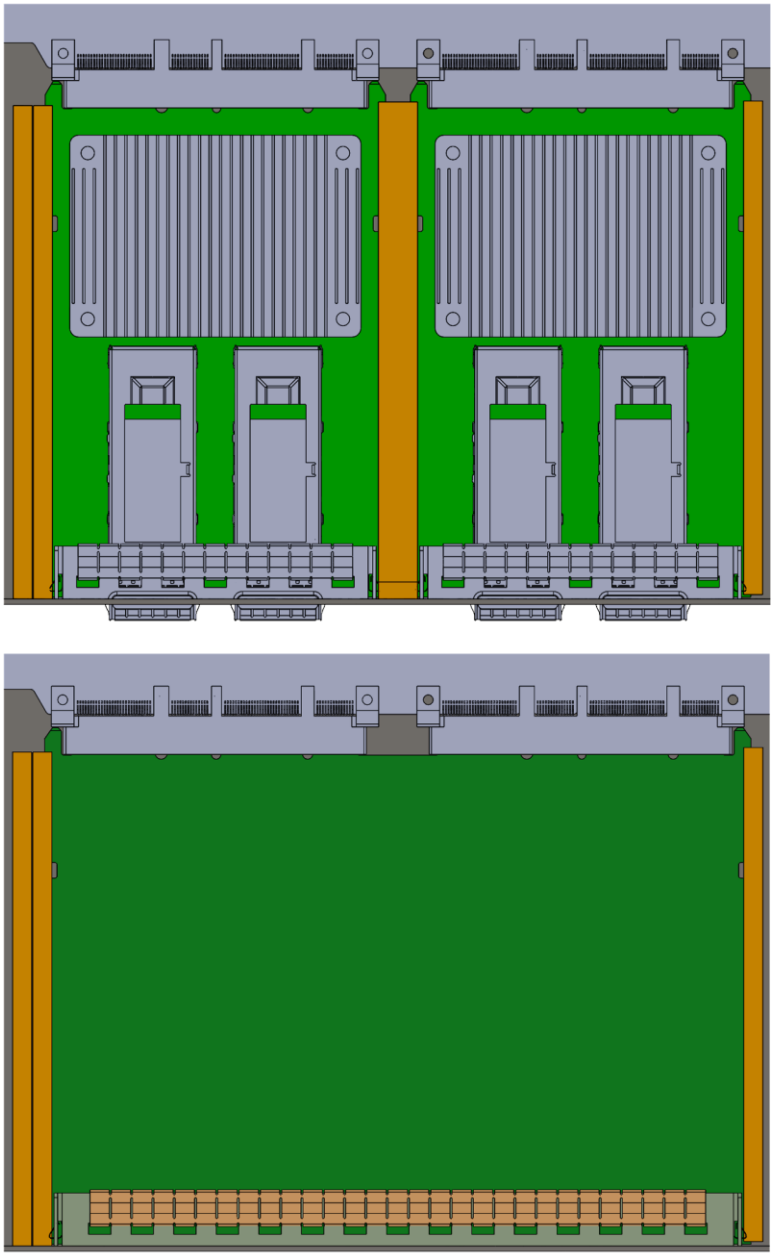
The TSFF allows for taller Z-height applications. The additional height allows for taller I/O cages and additional cooling capability.

A TSFF slot may mechanically accept a SFF NIC, however, while electrically permissible, addressing the electromagnetic interference implications due to the faceplate gap is outside the scope of this specification.

2.1.3 Dual Small Form Factor (DSFF)

The Dual Small Form Factor (DSFF) uses two 4C+ connectors with two corresponding 4C+ gold fingers. A DSFF compliant slot is comprised of two SFF slots with a removable mechanical guide rail. When the guide rail is removed, a DSFF may be inserted. This is illustrated in Figure 6.

Figure 6: DSFF / 2xSFF Conversion (not to scale)

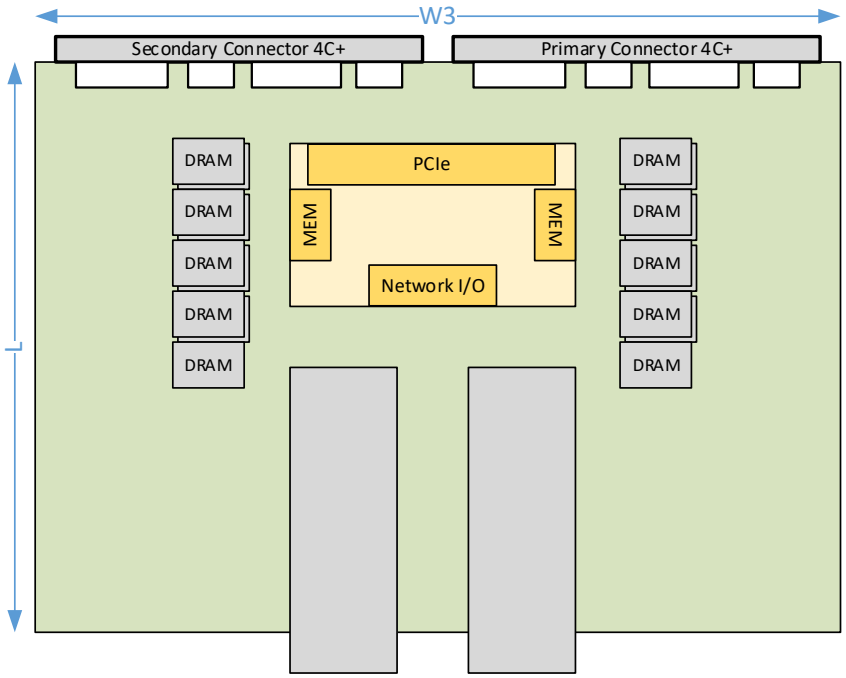


The DSFF supports up to 160 W of delivered power to the card edge across both connectors. Actual cooling capacity for the DSFF is dependent on the ambient conditions over the NIC. The DSFF requires the use of an insulator on the bottom side of the PCB to protect components from shorting out to the chassis. The insulator implementation may be the same insulator material found on the SFF with an option of using a backing plate with insulative properties instead. The backing plate allows component

placement closer to the gold finger edge while also adding the option of increasing mechanical rigidity. See Section 2.7 for more details. An example DSFF is shown in Figure 7. The components shown in the figure are for illustrative purposes only.

> **Note:** The DSFF connector pitch is 81.55 mm. This is smaller than two "normal" adjacent SFF slots. As a result, when this is configured as two SFF slots, faceplates with thumb screw implementations are not supported. Refer to the DC-MHS M-FLW specification for details.

Figure 7: DSFF Block Diagram (not to scale)



2.1.4 Tall Dual Small Form Factor (TDSFF)

The Tall Dual Small Form Factor (TDSFF) is like the DSFF. It shares the same PCB outline, connector and gold finger requirements and electrical parameters as the DSFF.

The TDSFF allows for taller Z-height applications. The additional height allows for taller I/O cages and additional cooling capability.

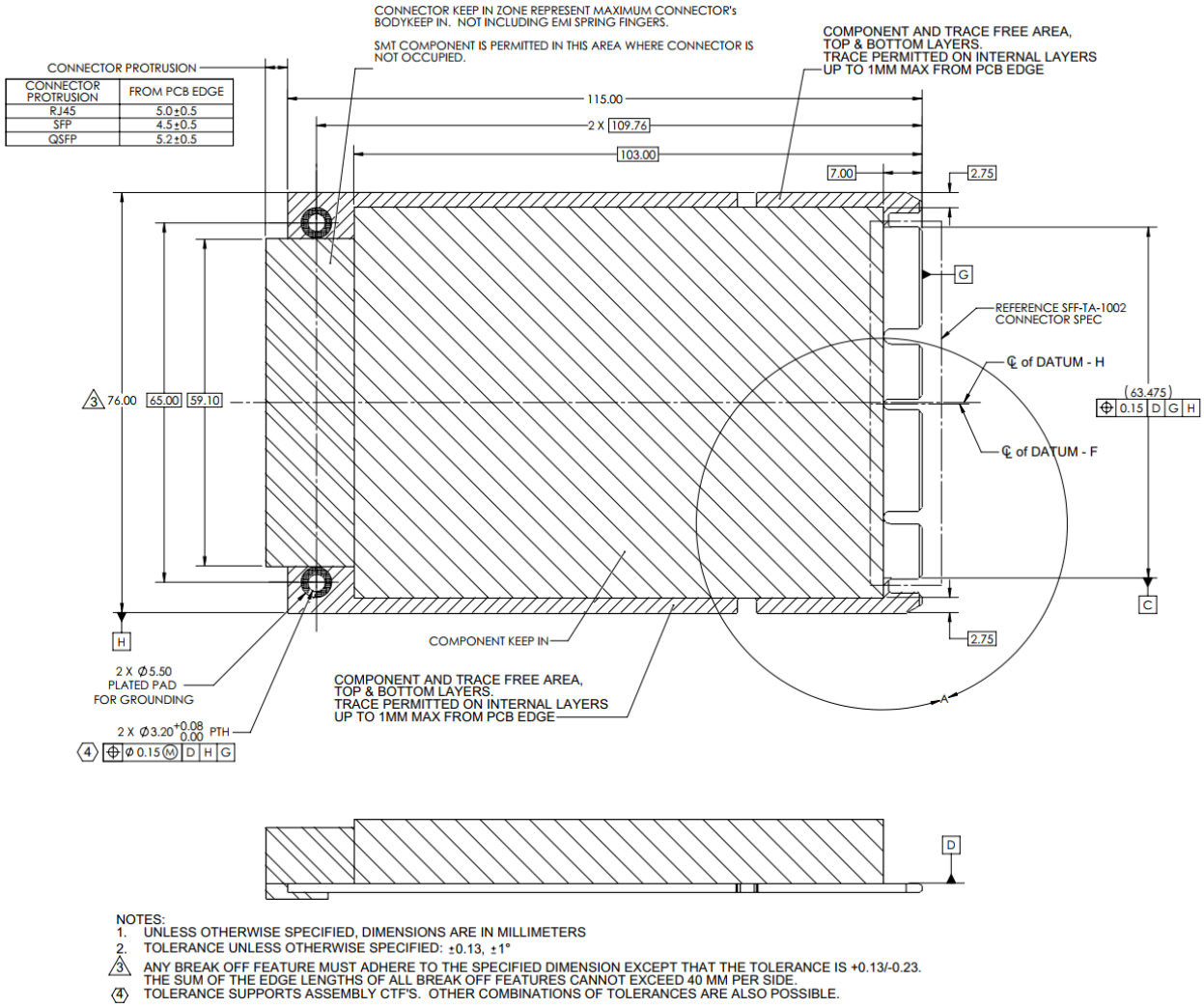
TDSFF baseboard slot may accept a DSFF sized NIC, however, while electrically permissible, addressing the electromagnetic interference implications due to the faceplate gap is outside the scope of this specification.

2.2 Card Dimensions and Keep Out Zones

2.2.1 SFF Dimensions and Keep Out Zones

Note: The SFF top, detail A and bottom view keep out zones are also applicable to the TSFF.

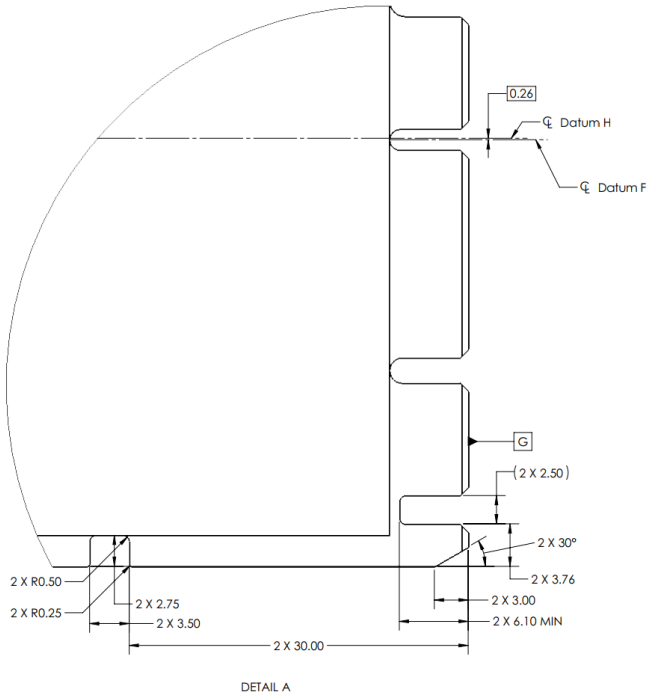
Figure 8: SFF Keep Out Zone – Top View



NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1°
3. ANY BREAK OFF FEATURE MUST ADHERE TO THE SPECIFIED DIMENSION EXCEPT THAT THE TOLERANCE IS +0.13/-0.23. THE SUM OF THE EDGE LENGTHS OF ALL BREAK OFF FEATURES CANNOT EXCEED 40 MM PER SIDE.
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE.

941
942

Figure 9: SFF Keep Out Zone – Top View – Detail A

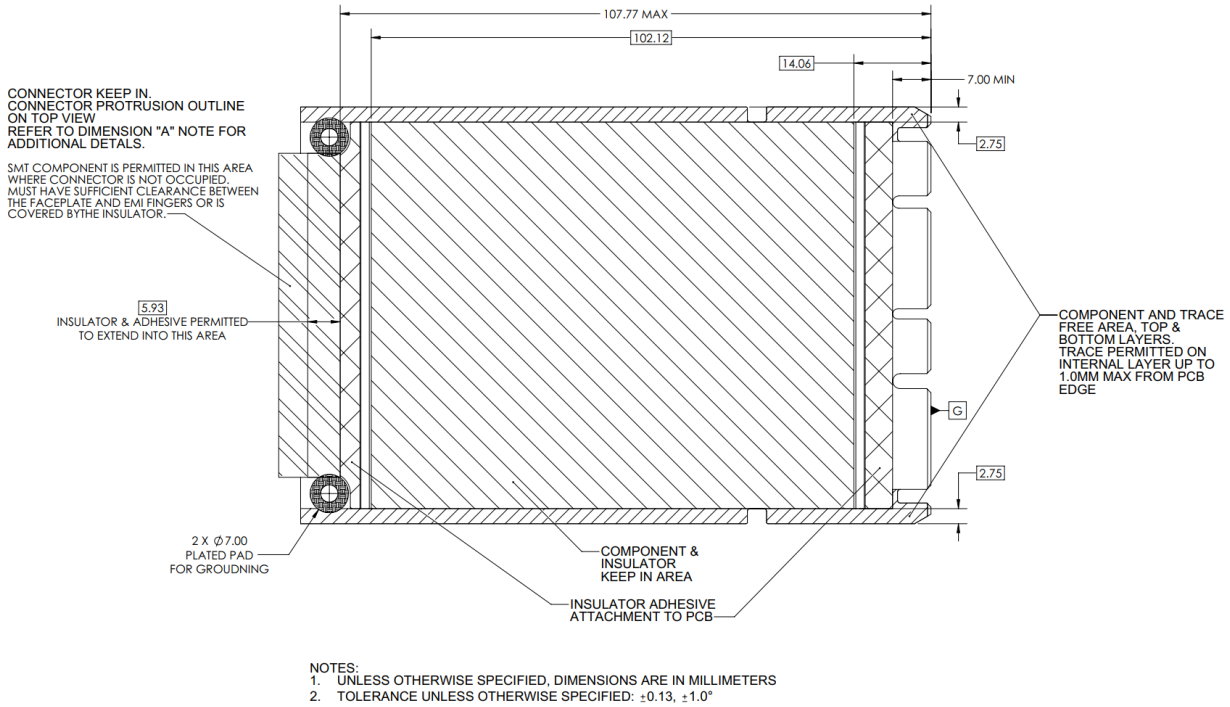


943

944

945

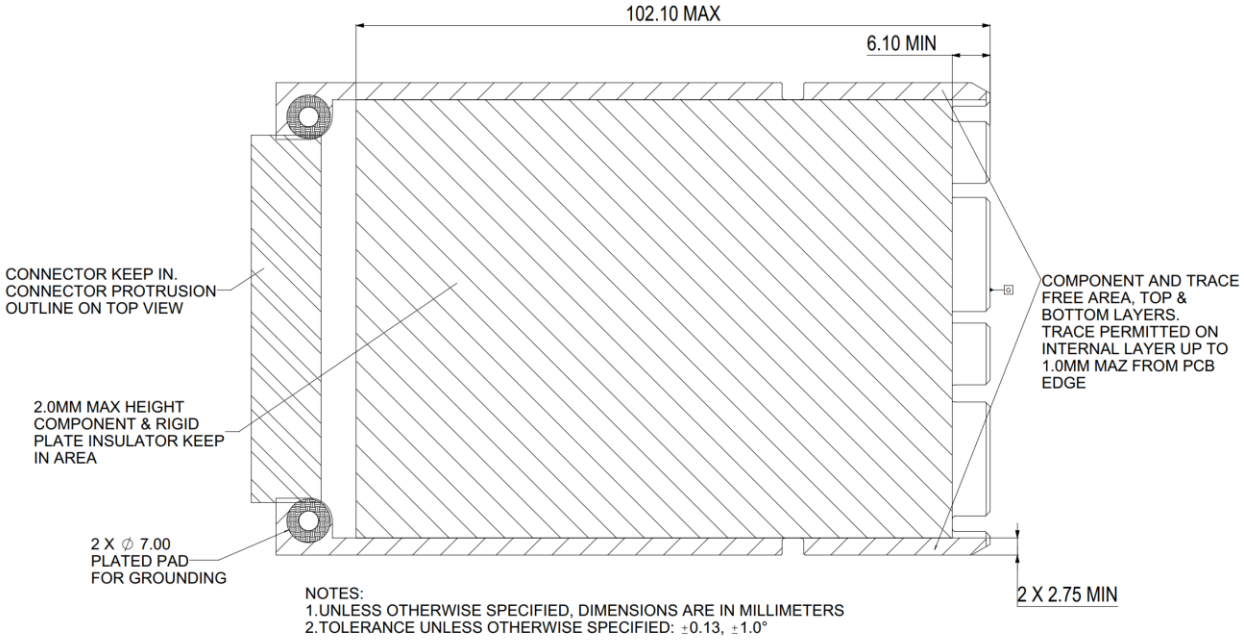
Figure 10: SFF Keep Out Zone – Bottom View



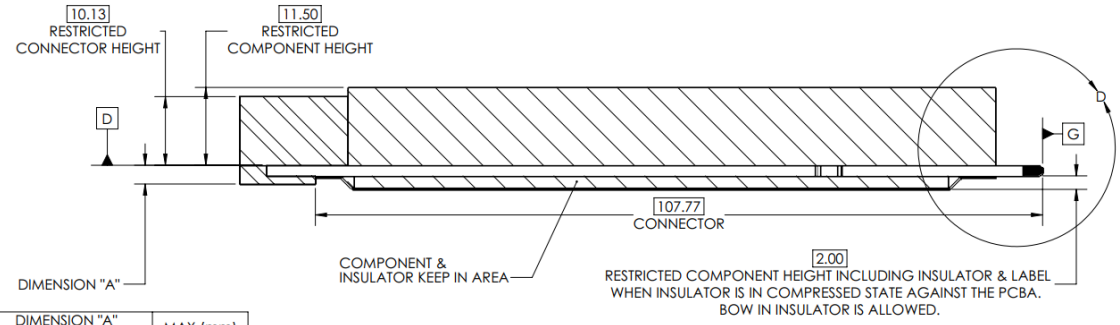
NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1.0°

946
947

948 Figure 11: SFF with Backing Plate Keep Out Zone – Bottom View



949
950
951
952 Figure 12: SFF Keep Out Zone – Side View

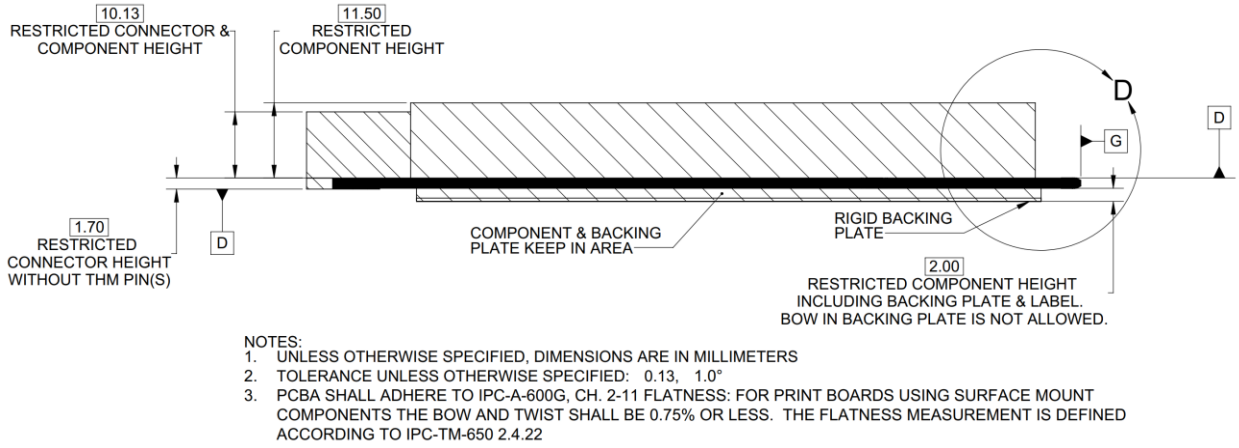


DIMENSION "A" CONNECTOR HEIGHT	MAX (mm)
WITH LATCH	1.70
W/O LATCH	2.77

NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1.0°
3. PCBA SHALL ADHERE TO IPC-A-600G, CH. 2-11 FLATNESS: FOR PRINT BOARDS USING SURFACE MOUNT COMPONENTS THE BOW AND TWIST SHALL BE 0.75% OR LESS. THE FLATNESS MEASUREMENT IS DEFINED ACCORDING TO IPC-TM-650 2.4.22

953
954

Figure 13: SFF with Backing Plate Keep Out Zone – Side View



Note: The area defined by DIMENSION "A" is between the faceplate and the primary side of the board. Grounded through-hole mounting pins are permitted but shall avoid interfering with the latching mechanism and EMI fingers. Signal pins are not permitted in this area.

Figure 14: SFF Keep Out Zone – Side View – Detail D

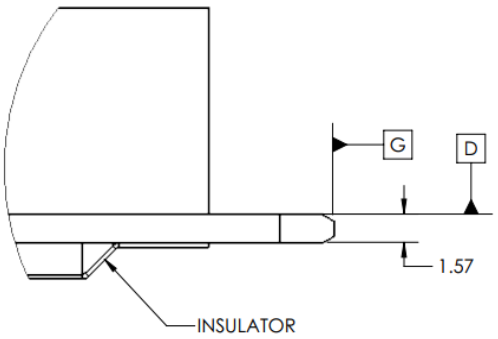
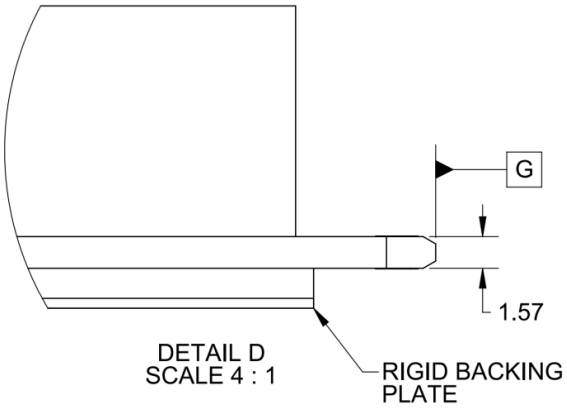


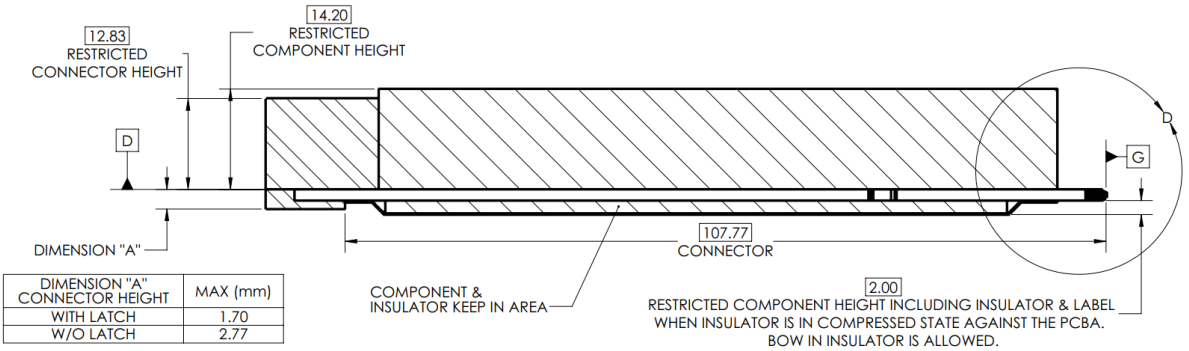
Figure 15: SFF with Backing Plate Keep Out Zone – Side View – Detail D



2.2.2 TSFF Dimensions and Keep Out Zones

The TSFF keep out zones are identical to the SFF except for the side view. This is shown in Figure 16. Refer to the SFF dimension and keep out zone in Section 2.2.1 for the remaining details.

Figure 16: TSFF Keep Out Zone – Side View



DIMENSION "A" CONNECTOR HEIGHT	MAX (mm)
WITH LATCH	1.70
W/O LATCH	2.77

NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1.0°
3. PCBA SHALL ADHERE TO IPC-A-600G, CH. 2-11 FLATNESS: FOR PRINT BOARDS USING SURFACE MOUNT COMPONENTS THE BOW AND TWIST SHALL BE 0.75% OR LESS. THE FLATNESS MEASUREMENT IS DEFINED ACCORDING TO IPC-TM-650 2.4.22

2.2.3 DSFF Dimensions and Keep Out Zones

Note: The DSFF top, detail A and bottom view keep out zones are also applicable to the TDSFF.

Figure 17: DSFF Keep Out Zone – Top View

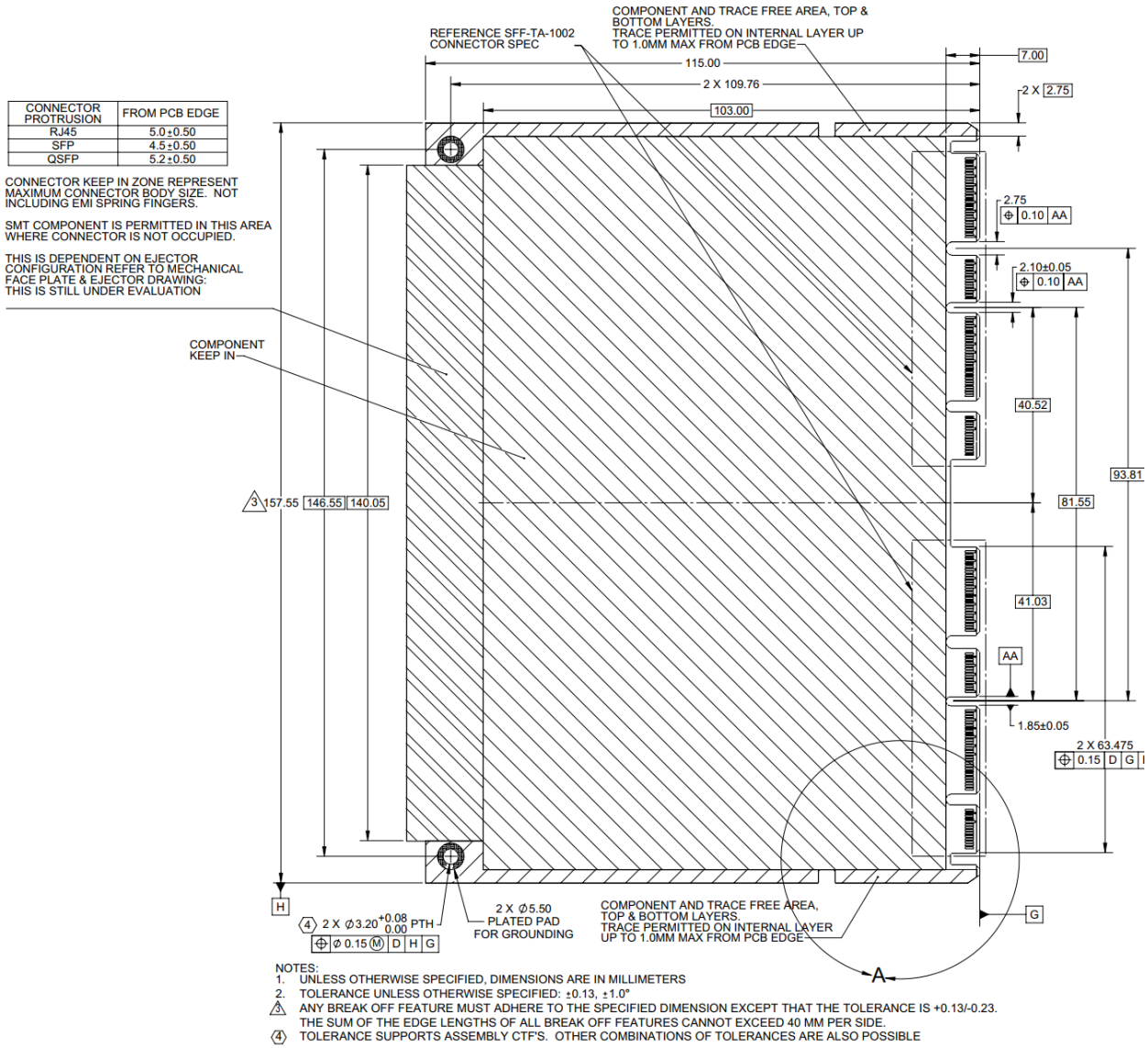


Figure 18: DSFF Keep Out Zone – Top View – Detail A

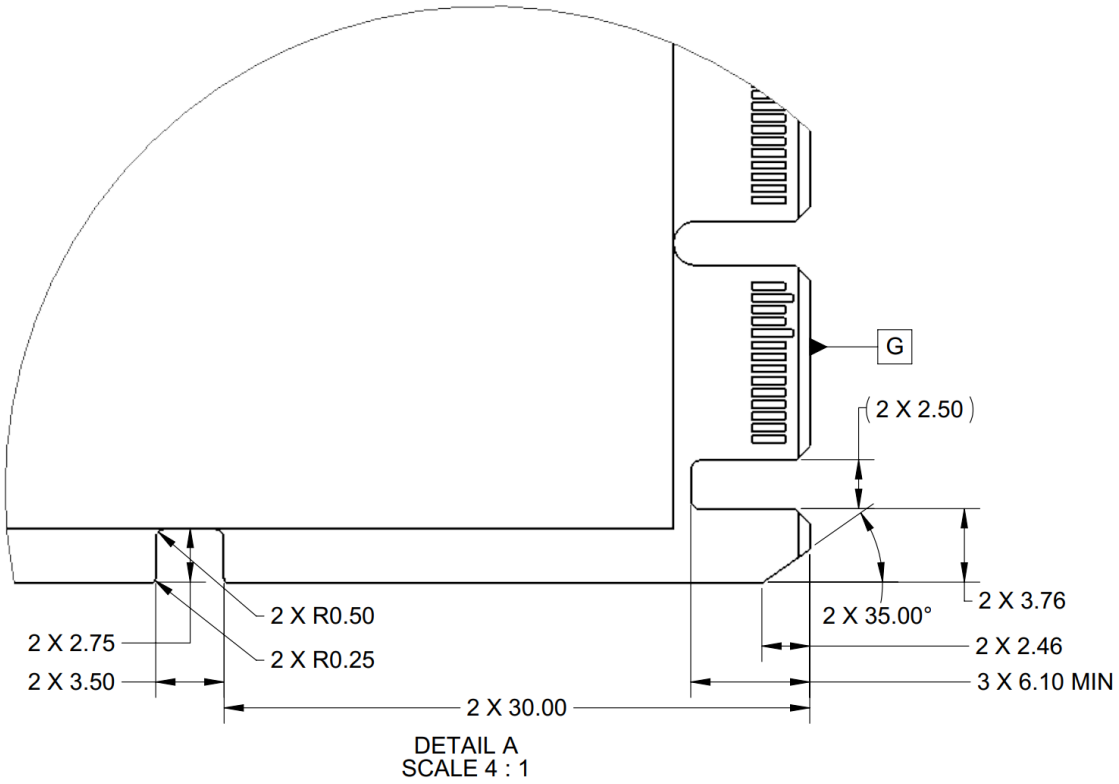


Figure 19: DSFF with Insulator Keep Out Zone – Bottom View

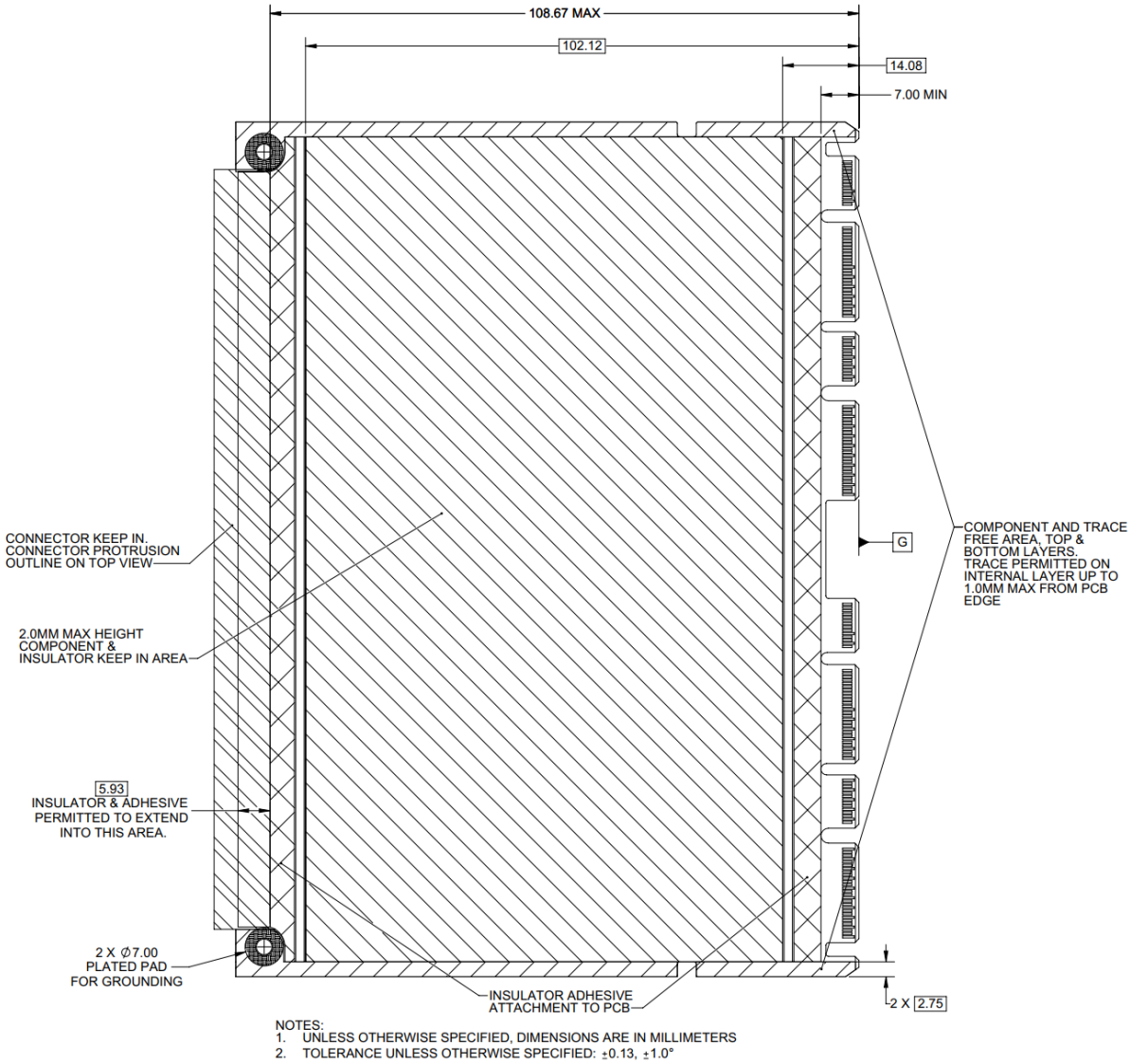


Figure 20: DSFF with Insulator Keep Out Zone – Side View

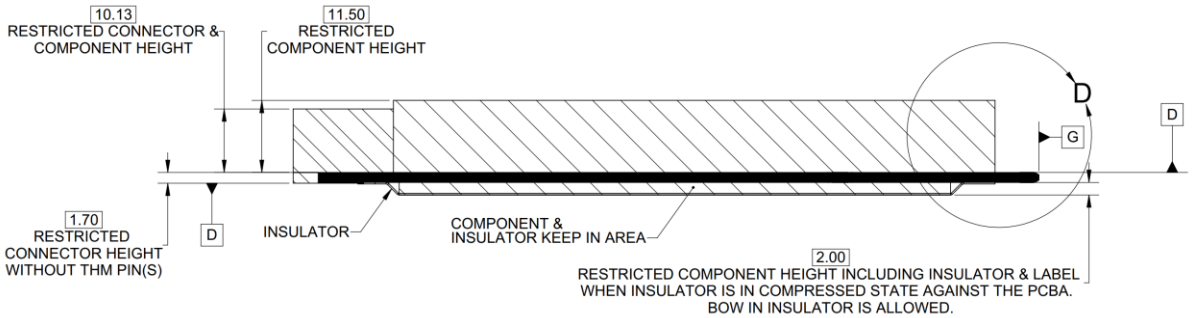


Figure 21: DSFF with Backing Plate Keep Out Zone – Bottom View

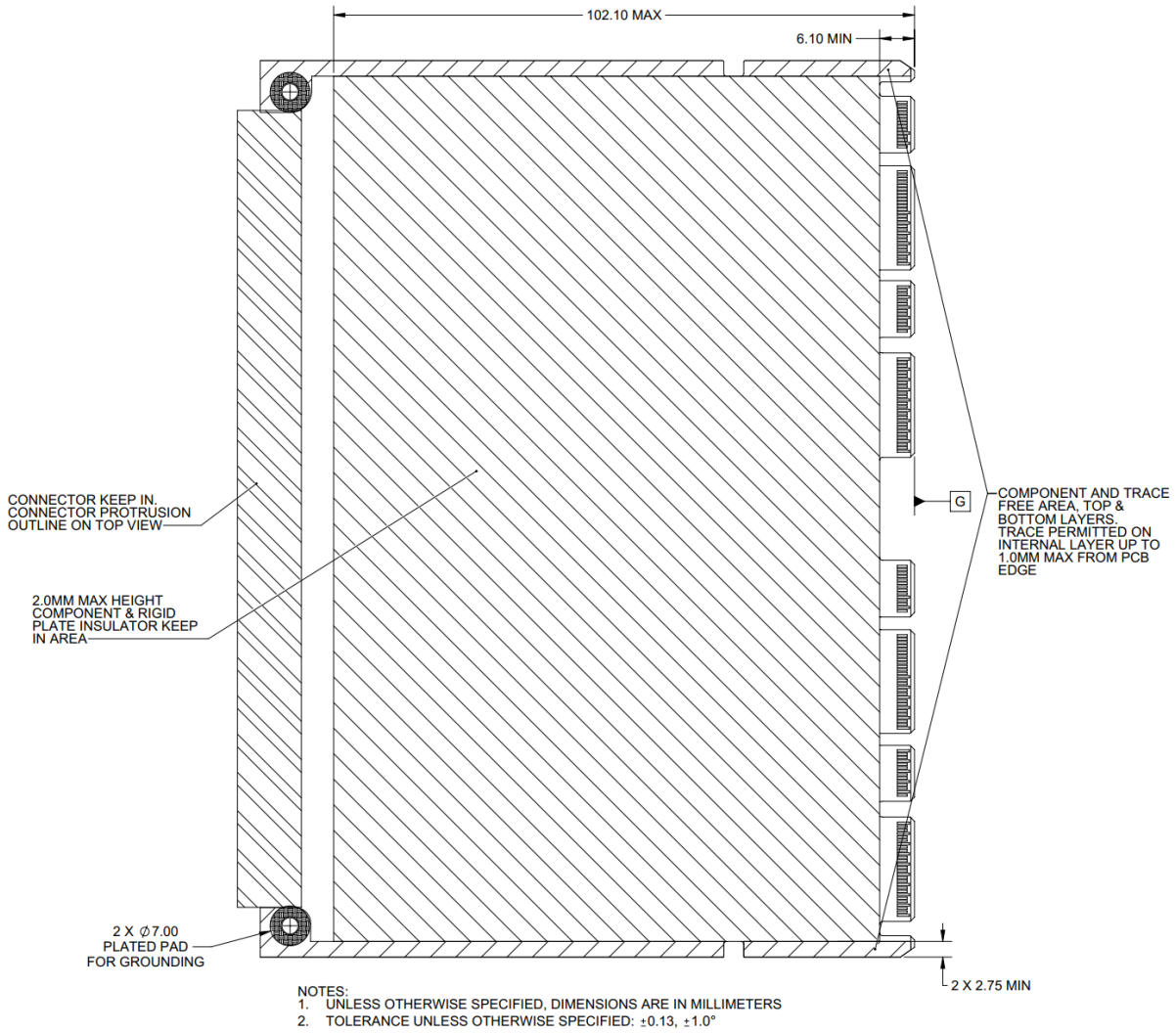


Figure 22: DSFF with Backing Plate Keep Out Zone – Side View

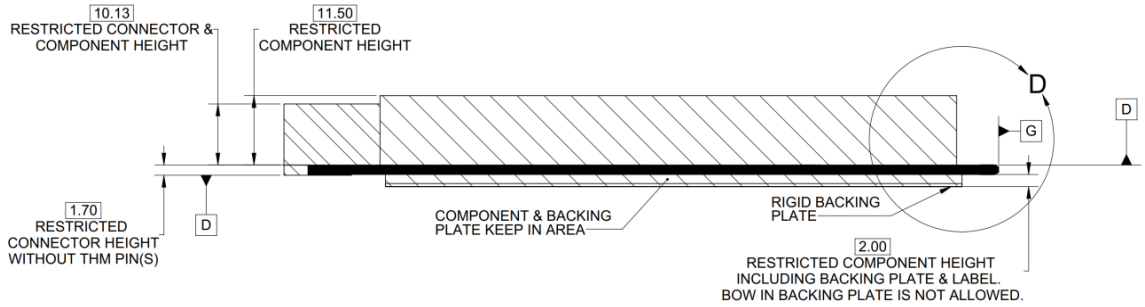


Figure 23: DSFF with Insulator Keep Out Zone – Side View – Detail D

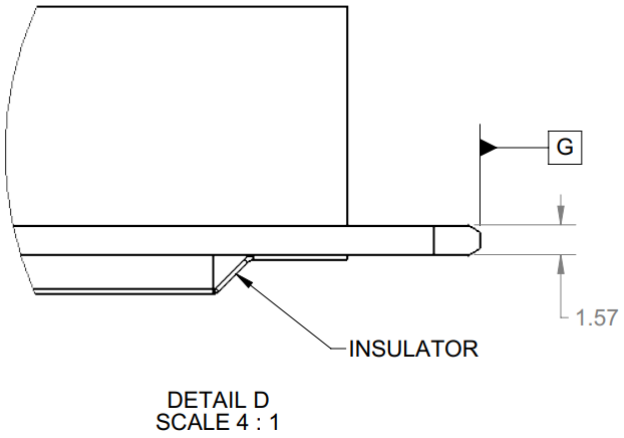
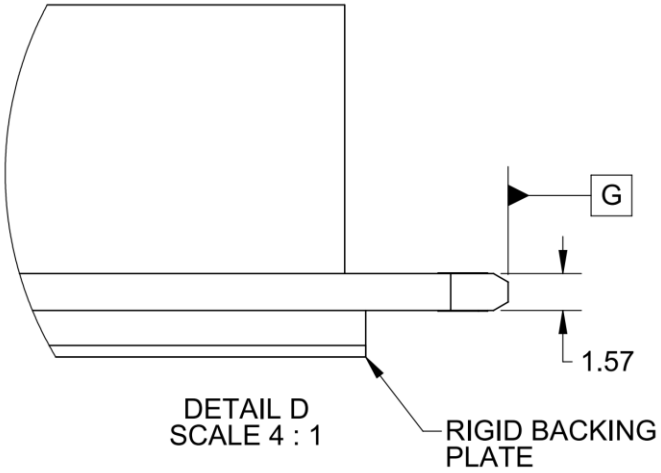


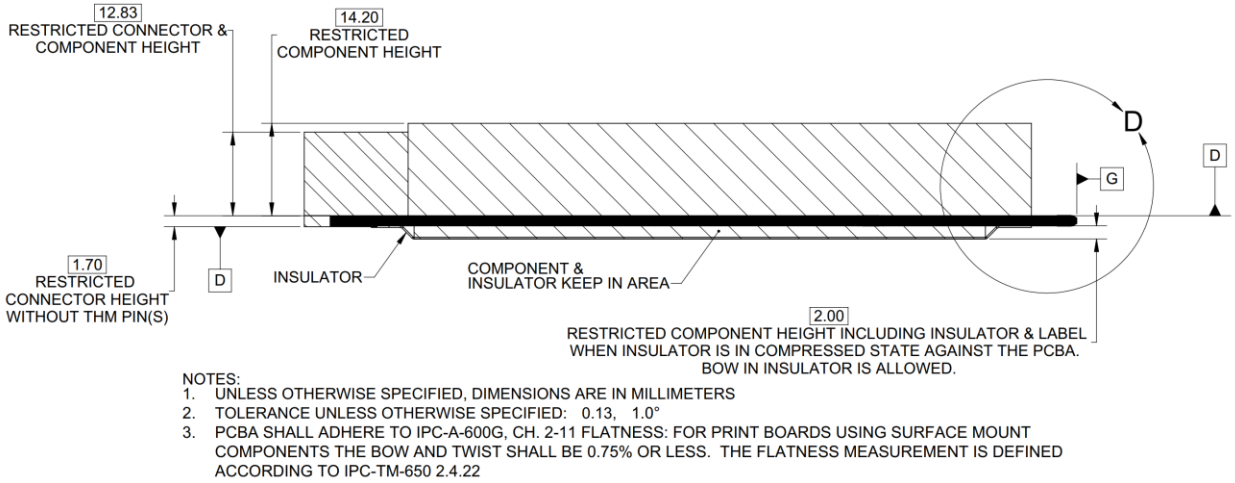
Figure 24: DSFF with Backing Plate Keep Out Zone – Side View – Detail D



2.2.4 TDSFF Dimensions and Keep Out Zones

The TDSFF keep out zones are identical to the DSFF except for the top side restricted connector and component heights. This is shown in Figure 25. Refer to the DSFF dimension and keep out zone in Section 2.2.3 for the remaining details.

Figure 25: TDSFF Keep Out Zone – Side View



2.3 Card Edge Gold Finger Requirements

The OCP NIC 3.0 cards are compliant to the SFF-TA-1002 specification for the gold fingers and connectors. Refer to the latest SFF-TA-1002 specification for details.

Note: The "B" pins on the connector are associated with the top side of the OCP NIC 3.0 card. The "A" pins on the connector are associated with the bottom side of the OCP NIC 3.0 card. The A and B side pins are physically on top of each other with zero x-axis offset.

2.3.1 SFF Gold Finger Requirements

Refer to SFF-TA-1002 and Section 2.3.3 for details on the 4C+ (Primary Connector) gold finger requirements.

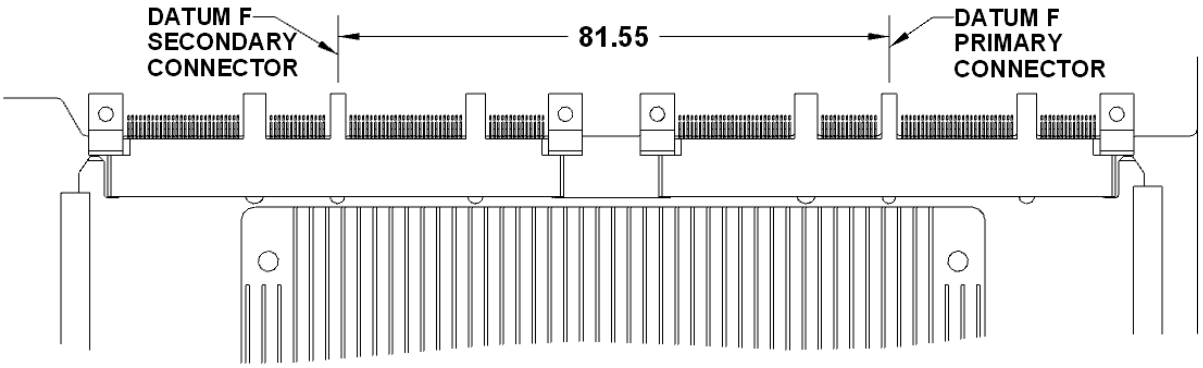
The SFF card requires a single connector. There are no connector pitch requirements. However, for baseboard designers that wish to design a multi-SFF capable baseboard, the minimum connector pitch is 89.00 mm to allow use of all the faceplate options.

2.3.2 DSFF Gold Finger Requirements

Refer to SFF-TA-1002 and Section 2.3.3 for the 4C+ (Primary Connector) and 4C+ (Secondary Connector) gold finger requirements.

The full complement of the DSFF pins span across two connectors and its respective card gold fingers. The connector pitch is defined in Figure 26. The pitch is measured from Datum F of each connector.

Figure 26: DSFF Gold Finger Pitch – x32 – Top Side ("B" Pins)

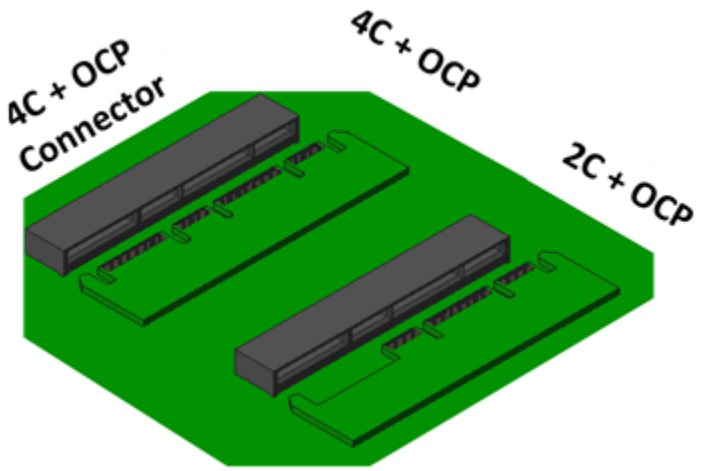


2.3.3 Gold Finger Downshifting

An OCP NIC 3.0 card may optionally implement a subset of pins to support less than the full complement of PCIe lanes. This card edge "downshifting" is supported by the SFF-TA-1002 connector. Downshifting is only permitted to sequentially reduce the card gold finger width. Card edge downshifting may save associated costs with gold plating non-functional pads.

For example, an SFF card may implement a 2C+ card edge per SFF-TA-1002. As an example, Figure 27 illustrates the supported SFF 4C+ and 2C+ card edge configurations on a 4C+ Primary Connector.

Figure 27: Primary Connector (4C+) with 4C and 2C OCP NIC 3.0 SFF Cards

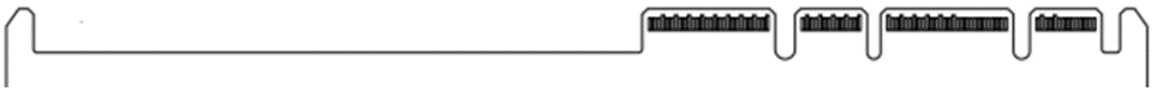


For the DSFF, the card may utilize the Primary and Secondary Connector edge, or downshift to the Primary Connector edge only. The following rules apply:

- The full complement of pins / card edge features is required when the card:
  - Implements more than 16 lanes of PCIe, or
  - Requires more than 80 W of power, or
  - Is a high mass card requiring both connections to minimize board deflection.
- A downshifted complement of pins / card edge features may be implemented when the card:
  - Implements less than or equal to 16 lanes of PCIe, and
  - Requires less than or equal to 80 W of power
- Downshifting the Primary Connector edge while using a full complement of the Secondary Connector edge is not permitted.
- When downshifting, the Secondary Connector edge features shall be entirely removed.

The PCB outline for the secondary connector edge is not permitted to remain when there is no gold plating. This requirement prevents scraping of PCB material on the baseboard connectors and leaving debris that may impact signal integrity performance. As an example, Figure 28 illustrates a properly implemented DSFF downshifted configuration with only a 4C+ Primary Connector edge.

Figure 28: Primary Connector (4C+) Only Card Edge on DSFF



1067

Note: For DC-MHS platforms, the NIC Primary Connector and Secondary Connector edge connections may be associated with different CPU instances. DC-MHS platforms may also be implemented as single or dual socket HPMs. Population of a "downshifted" DSFF card may not work in all HPM combinations.

For example, the M-FLW specification recommends associating the DSFF Primary Connector with CPU0. The DSFF Secondary Connector is recommended to be associated with CPU1. On M-SDNO platforms, this association is flipped. The M-SDNO specification recommends associating the DSFF Primary Connector with CPU1 while the DSFF Secondary Connector with CPU0. This association difference is from prioritizing the NIC as hot aisle or cold aisle implementations.

While these CPU assignments are not a mandatory, the respective DC-MHS specifications enable HPM designers to make common decisions across the ecosystem solutions.

The DSFF NIC with a downshifted connector edge may not operate at all if the DSFF Primary Connector is associated with a non-populated CPU socket.

1068

1069 In all cases, the baseboard side shall implement the full-sized 4C+ connector(s) and shall not use a
1070 reduced width version.

1071

1072 Table 6 summarizes the supported connector and card edge "downshift" combinations. SFF cards
1073 support the Primary Connector and up to 16 PCIe lanes. LFF cards support implementations with both
1074 the Primary and Secondary Connectors and up to 32 PCIe lanes, or a Primary Connector only up to 16
1075 PCIe lanes. DSFF cards support both the Primary and Secondary Connectors.

1076

1077 Table 6: Supported OCP NIC 3.0 Card Downshift Combinations

OCP NIC 3.0 Card Size and PCIe width	Baseboard Secondary Connector Up to x16 PCIe Lanes [31:16]	Baseboard Primary Connector Up to x16 PCIe Lanes [15:0]
SFF (x8)	Not used with SFF 2C+ Card Edge	x8 PCIe (Lanes 7:0)
SFF (x16)	Not used with SFF 4C+ Card Edge	x16 PCIe (Lanes 15:0)
LFF (x8)	Not used with LFF 2C+ Card Edge	x8 PCIe (Lanes 7:0)
LFF (x16)	Not used with LFF 4C+ Card Edge	x16 PCIe (Lanes 15:0)
LFF (x32)	x16 PCIe (Lanes 31:16)	x16 PCIe (Lanes 15:0)
DSFF (x16)	Not used with a x16 DSFF implementation	x16 PCIe (Lanes 15:0)
DSFF (x32)	x16 PCIe (Lanes 31:16)	x16 PCIe (Lanes 15:0)

1078

1079 The OCP NIC 3.0 design allows a few downward compatibility options between the card sizes. Table 7
1080 shows these compatibility options between the baseboard and NIC.

1081

Table 7: Baseboard to OCP NIC Form Factor Compatibility Chart

Baseboard Slot Size	NIC Size				
	SFF	TSFF	LFF	DSFF	TDSFF
SFF	Supported	Not supported	Not supported	Not supported	Not supported
TSFF	Fits mechanically	Supported	Not supported	Not supported	Not supported
LFF	Fits mechanically	Not supported	Supported	Not supported	Not supported
DSFF	Supported	Not supported	Not supported	Supported	Not supported
TDSFF	Fits mechanically	Supported	Not supported	Fits mechanically	Supported

Baseboard connector options are discussed in Section 3.

2.3.4 Gold Finger Mating Sequence

Per the SFF-TA-1002 specification, the Primary and Secondary Connectors are protocol agnostic and are optimized for high-speed differential pairs. In the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the required OCP NIC 3.0 card gold finger staging is shown in Table 8 for a two stage, first-mate, last-break functionality. The two-stage finger length is a normative requirement for the OCP NIC 3.0 card. The host connectors have a single stage mating and do not implement different connection depths.

This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings in SFF-TA-1002 for the pin first-mate and second-mate lengths.

Note: Refer to Section 4.1 for the pinouts of each form-factor.

Table 8: Contact Mating Sequence for the Card Gold Fingers / Connector

Side B			Side A			
Gold Finger Side			Gold Finger Side			Applicable Connector Size
	2nd Mate	1st Mate		2nd Mate	1st Mate	
OCP B1			OCP A1			4C+ only
OCP B2			OCP A2			
OCP B3			OCP A3			
OCP B4			OCP A4			
OCP B5			OCP A5			
OCP B6			OCP A6			
OCP B7			OCP A7			
OCP B8			OCP A8			
OCP B9			OCP A9			
OCP B10			OCP A10			
OCP B11			OCP A11			
OCP B12			OCP A12			
OCP B13			OCP A13			
OCP B14			OCP A14			
Mechanical Key						
B1			A1			4C+ and 4C
B2			A2			
B3			A3			
B4			A4			
B5			A5			
B6			A6			
B7			A7			
B8			A8			
B9			A9			
B10			A10			
B11			A11			
B12			A12			

Side B			Side A			
Gold Finger Side			Gold Finger Side			Applicable Connector Size
	2nd Mate	1st Mate		2nd Mate	1st Mate	
B13			A13			
B14			A14			
B15			A15			
B16			A16			
B17			A17			
B18			A18			
B19			A19			
B20			A20			
B21			A21			
B22			A22			
B23			A23			
B24			A24			
B25			A25			
B26			A26			
B27			A27			
B28			A28			
Mechanical Key						
B29			A29			4C+ and 4C
B30			A30			
B31			A31			
B32			A32			
B33			A33			
B34			A34			
B35			A35			
B36			A36			
B37			A37			
B38			A38			
B39			A39			
B40			A40			
B41			A41			
B42			A42			
Mechanical Key						
B43			A43			4C+ and 4C
B44			A44			
B45			A45			
B46			A46			
B47			A47			
B48			A48			
B49			A49			
B50			A50			
B51			A51			
B52			A52			
B53			A53			
B54			A54			
B55			A55			
B56			A56			
B57			A57			
B58			A58			
B59			A59			
B60			A60			
B61			A61			
B62			A62			
B63			A63			
B64			A64			
B65			A65			
B66			A66			
B67			A67			
B68			A68			
B69			A69			
B70			A70			

1100
1101

2.4 Faceplate Options

2.4.1 SFF Faceplate Configurations

The SFF configuration views are shown below. Three different faceplates for the same OCP NIC 3.0 PBA are each available for the SFF – pull tab, ejector latch and internal lock. Faceplates are attached to the PCBA at the time of manufacture. The drawings shown in Figure 29 below illustrate representative three-quarter, front, side and top views of the SFF implementations.

Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 mm x 3.0 mm may be added to help optimize airflow while maintaining the integrity of the faceplate structure. EMI mitigation should also be considered during the design process. Refer to the images shown in Figure 30 for example square vent configurations depending on the line side I/O connectors.

Depending on the OCP NIC 3.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep in regions as defined by the SFF PBA mechanical and faceplate drawings of Section 2.2.1.

The OCP NIC 3.0 outline provides an optional feature to lock the card into the chassis. This is accomplished with two notches – one on each side of the card. A baseboard may choose to use one or both notches for the internal locking mechanism as part of the card guide. The OCP NIC 3.0 outline provides a notch location on both guide rails to provide flexible configurations to baseboard vendors. If a locking feature is implemented on the baseboard, the OCP NIC 3.0 card may only be inserted or removed after actuating the internal locking mechanism. The PCB retention notches are compatible with all chassis implementations. Please refer to the SFF dimensions in Section 2.2.1 for details.

Note: The OCP NIC 3.0 card supplier may add port identification on the faceplate assembly that meet their manufacturing and customer requirements.

All the OCP NIC 3.0 CAD files are available for download and use on the OCP NIC 3.0 Wiki site: https://www.opencompute.org/wiki/Server/NIC.

Figure 29: SFF NIC Configuration Views

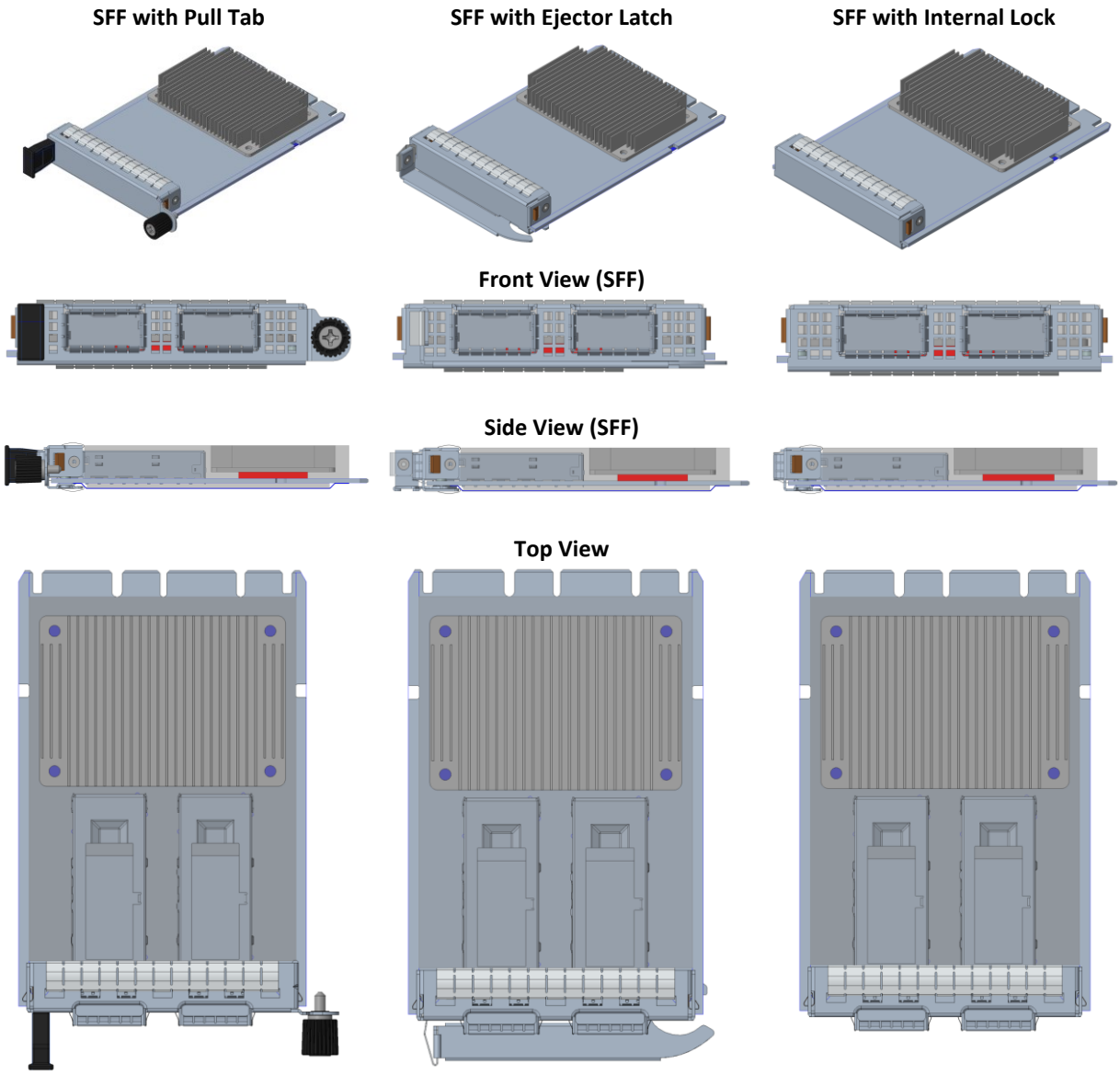


Figure 30 illustrates example SFF 3D views for the supported line side I/O implementations. The line side I/O implementations are discussed in Section 4.4.

Figure 30: SFF NIC Line Side 3D Views

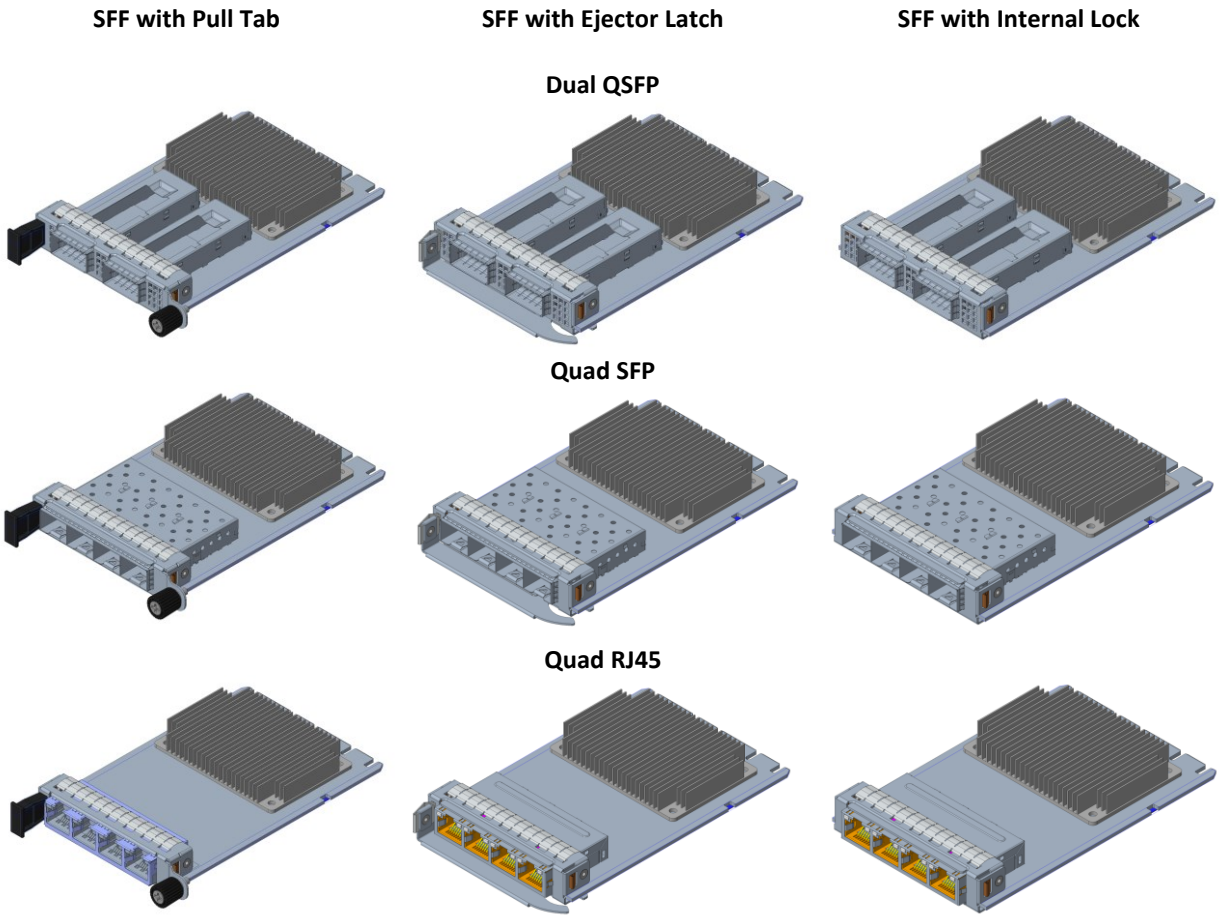


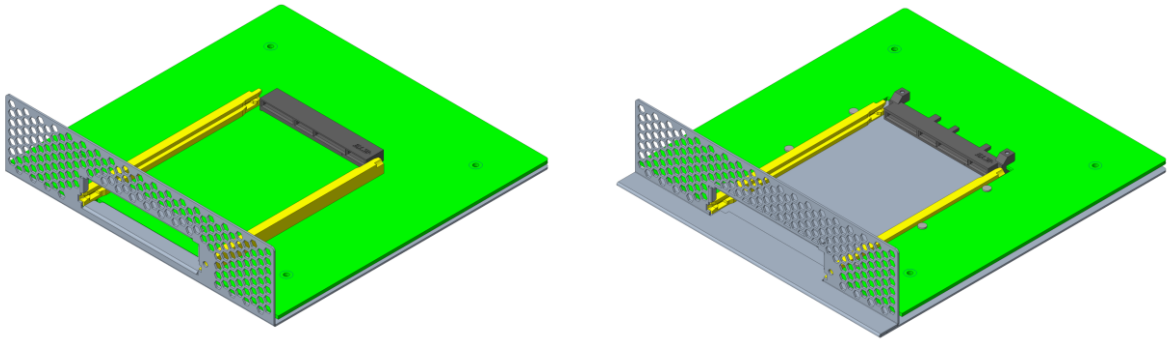
Figure 31 illustrates example SFF 3D views of the pull tab and ejector latch assemblies mounted in a chassis utilizing a straddle mount connector and a right-angle connector. The baseboard connector options are discussed in Section 3 The SFF OCP NIC 3.0 card is identical for both chassis connector options.

The OCP NIC 3.0 card provides a notch on each side of the card rail edge. This feature is used in conjunction with a baseboard's internal locking mechanism to prevent card insertion and removal. The internal locking mechanism is a baseboard vendor's optional feature and is not shown in the views below.

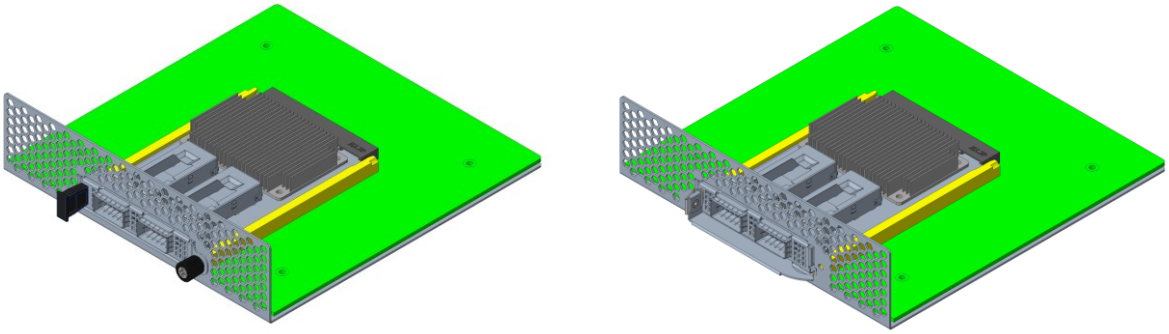
On the SFF internal lock variation only, a 5.4 kg force with a 1 second ramp may be applied to the heatsink during NIC ejection. The mechanical and thermal solution shall be implemented such that the thermal performance is maintained for 10 force cycles (i.e., the NIC still passes all functional tests). If there exists a minimum of (10 mm x 10 mm x 10 mm) of space behind the line side connectors, then each connector shall be able to sustain the same 5.4 kg force with a 1 second ramp.

1155 Figure 31: SFF NIC Chassis Mounted 3D Views

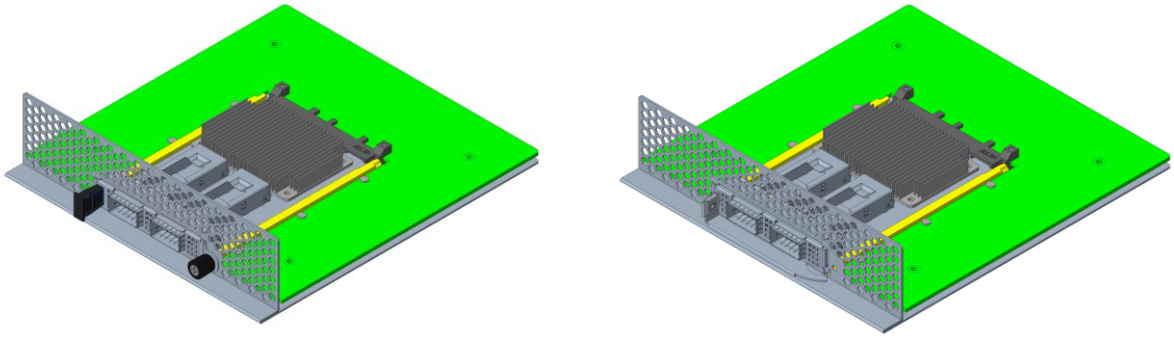
SFF with Pull Tab **SFF with Ejector Latch**



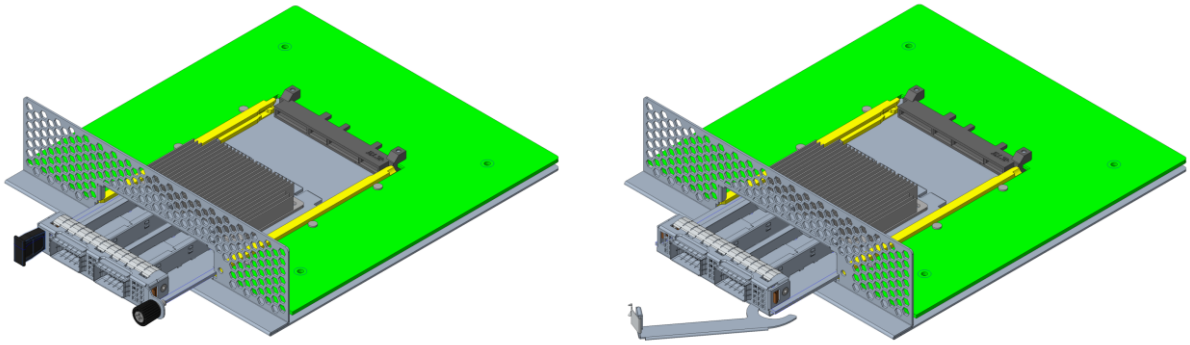
Right Angle vs Straddle Mount Chassis Configuration



Right Angle Baseboard Connector



Straddle Mount Baseboard Connector



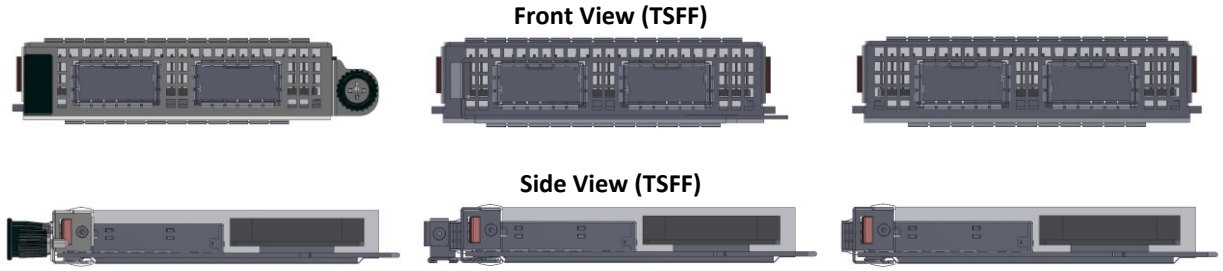
NIC Insertion / Removal (Shown with a Straddle Mount Connector)

1156

2.4.2 TSFF Faceplate Configurations

The TSFF implementation uses the same PCB outline as SFF. The faceplate and top-side Z-height envelope grows to 14.20 mm to support taller heatsink and line side I/O cage implementations. A TSFF faceplate may be used on a SFF PBA. The TSFF NIC front, and side views are shown in Figure 32 for a pull tab, ejector latch and internal lock implementation. All the SFF requirements, except for those relating to the Z-height, are applicable to the TSFF. Refer to the SFF discussion in Section 2.4.1 for additional details.

Figure 32: TSFF NIC Configuration Views



2.4.3 DSFF Faceplate Configurations

The DSFF currently supports two faceplate configurations, the internal lock and the pull tab. The ejector latch version is TBD. Faceplates are attached to the PCBA at the time of manufacture. The drawings shown in Figure 33 below illustrate representative three-quarter, front, side and top views of the DSFF implementations.

Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 mm x 3.0 mm may be added to help optimize airflow while maintaining the integrity of the faceplate structure. EMI mitigation should also be considered during the design process.

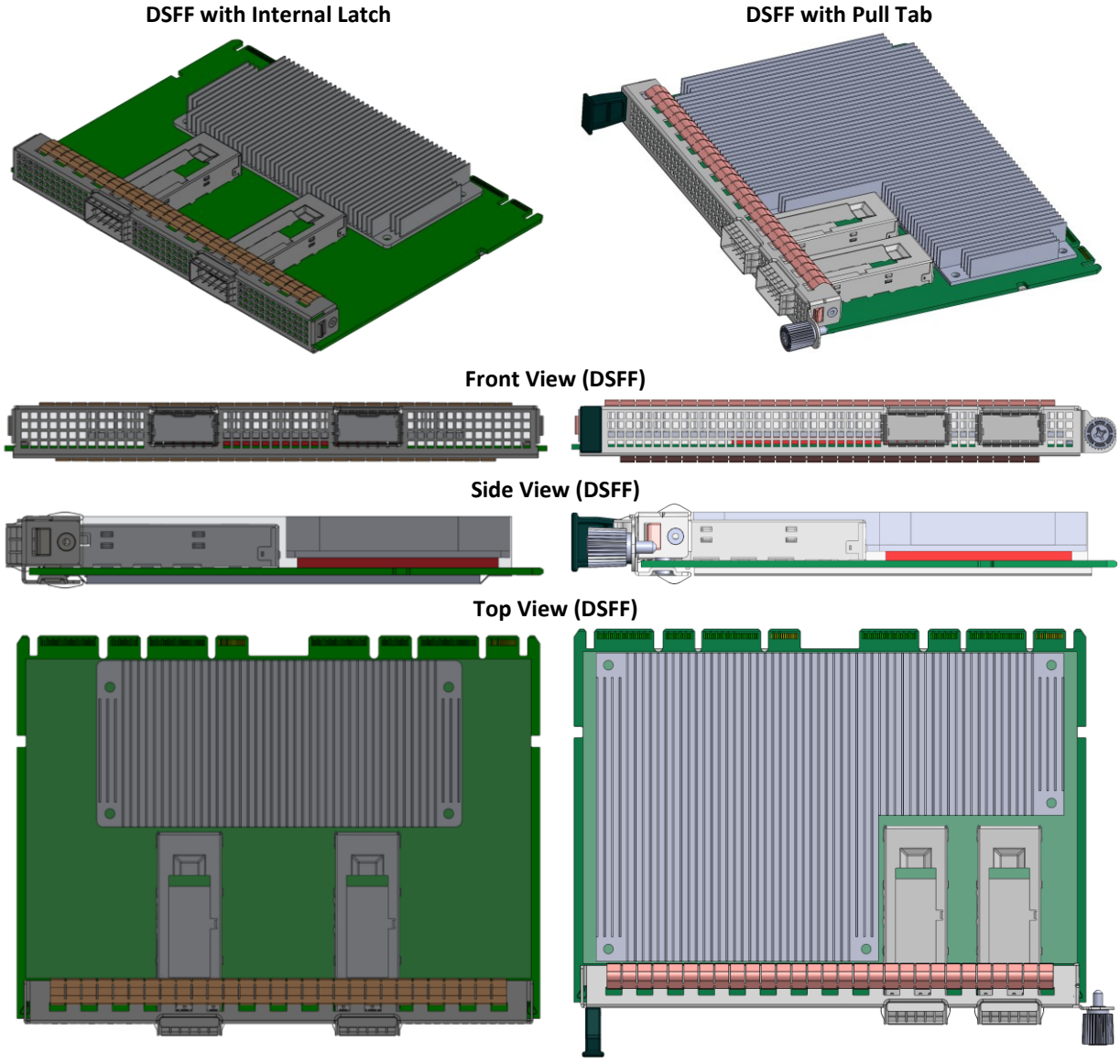
Depending on the OCP NIC 3.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep in regions as defined by the DSFF PBA mechanical and faceplate drawings of Section 2.2.3.

The OCP NIC 3.0 outline provides an optional feature to lock the card into the chassis. This is accomplished with two notches – one on each side of the card. A baseboard may choose to use one or both notches for the internal locking mechanism as part of the card guide. The OCP NIC 3.0 outline provides a notch location on both guide rails to provide flexible configurations to baseboard vendors. If a locking feature is implemented on the baseboard, the OCP NIC 3.0 card may only be inserted or removed after actuating the internal locking mechanism. The PCB retention notches are compatible with all chassis implementations. Please refer to the SFF dimensions in Section 2.2.3 for details.

Note: The OCP NIC 3.0 card supplier may add port identification on the faceplate assembly that meet their manufacturing and customer requirements.

All the OCP NIC 3.0 CAD files are available for download and use on the OCP NIC 3.0 Wiki site: https://www.opencompute.org/wiki/Server/NIC.

Figure 33: DSFF NIC Configuration Views



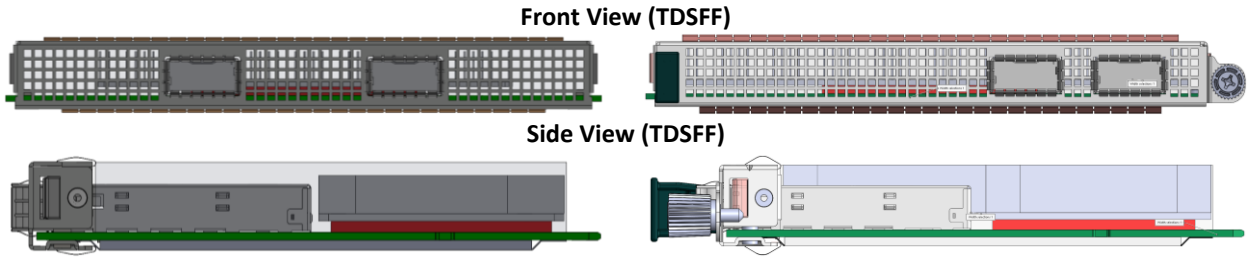
The OCP NIC 3.0 card provides a notch on each side of the card rail edge. This feature is used in conjunction with a baseboard's internal locking mechanism to prevent card insertion and removal. The internal locking mechanism is a baseboard vendor's optional feature and is not shown in the views above.

The SNIA SFF TA-1002 specification defines 1.1 N/pin pair maximum. The insertion force required to install a DSFF is expected to be ~185 N max. For some applications this may be too high and as such system vendors will need to provide external mechanical assistance (i.e., factory jig) to overcome this risk as required.

2.4.4 TDSFF Faceplate Configurations

The TDSFF implementation uses the same PCB outline as DSFF. The faceplate and top-side Z-height envelope grows to 14.20 mm to support taller heatsink and line side I/O cage implementations. A TDSFF faceplate may be used on a DSFF PBA. The TDSFF NIC front, and side views are shown in Figure 34 for the internal lock and the pull tab implementations. All the DSFF requirements, except for those relating to the Z-height, are applicable to the TDSFF. Refer to the DSFF discussion in Section 2.4.3 for additional details.

Figure 34: TDSFF NIC Configuration Views



2.5 Card Top Level Assemblies

Top level assemblies for each of the board form-factors are shown below.

Diagram callouts #12 through #15 are installed at the NIC assembly level:

Item #12 & #13 – Screws used to attach the faceplate assembly to the OCP NIC 3.0 PBA.
Item #14 – 2x SMT nuts installed on to the PBA assembly using the reflow process.
Item #15 – Insulator or backing plate is located on the secondary side and is installed on the PBA prior to the faceplate.

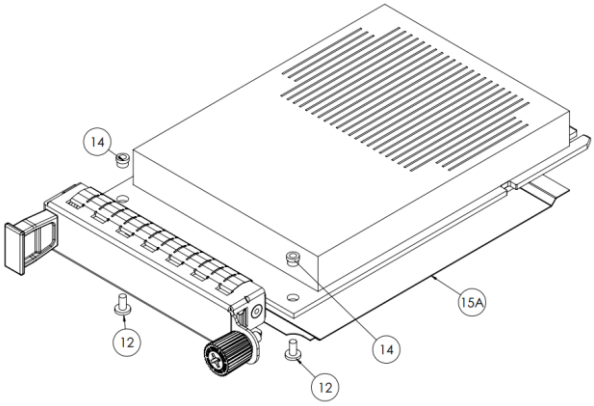
2.5.1 SFF / TSFF Top Level Assemblies

The images in Figure 35 illustrate the exploded top-level assemblies for the SFF and TSFF.

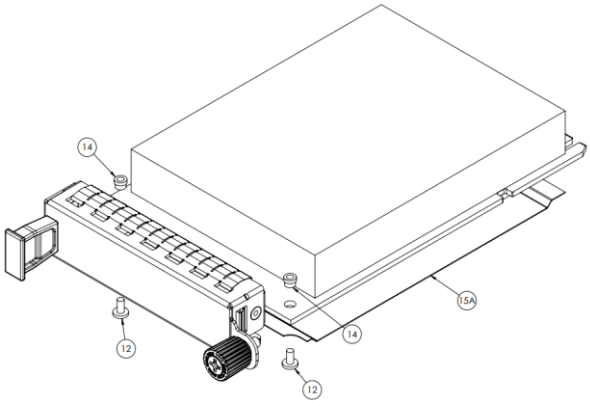
> **Note:** The TSFF implementation uses the same PCB outline as the SFF. The faceplate and top-side Z-height envelope grows to 14.20 mm. Refer to the faceplate subassembly drawings in Section 2.6 for more details.

Figure 35: PBA Exploded Views (SFF, and TSFF)

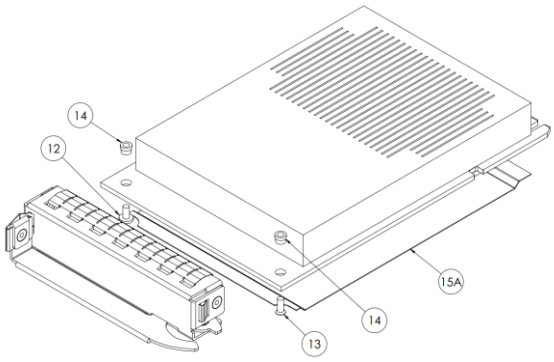
SFF with Pull Tab



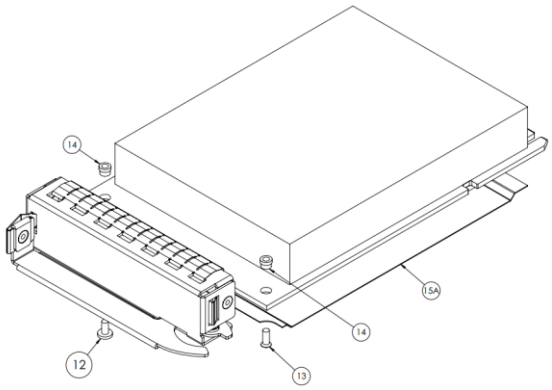
TSFF with Pull Tab



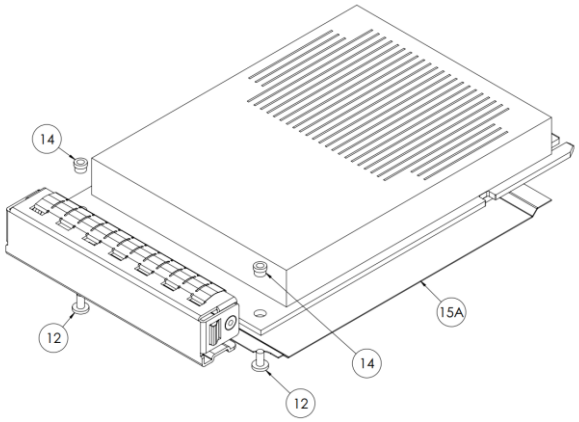
SFF with Ejector Latch



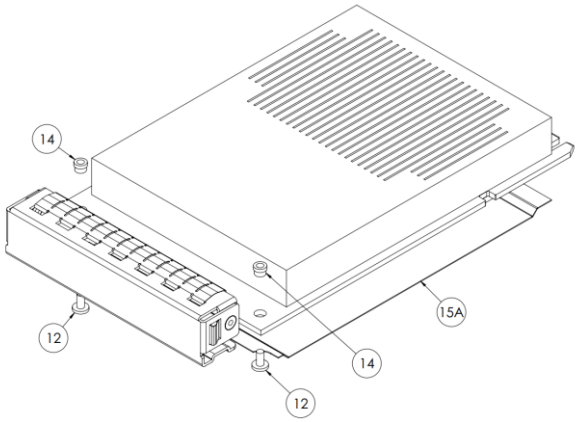
TSFF with Ejector Latch



SFF with Internal Lock



TSFF with Internal Lock



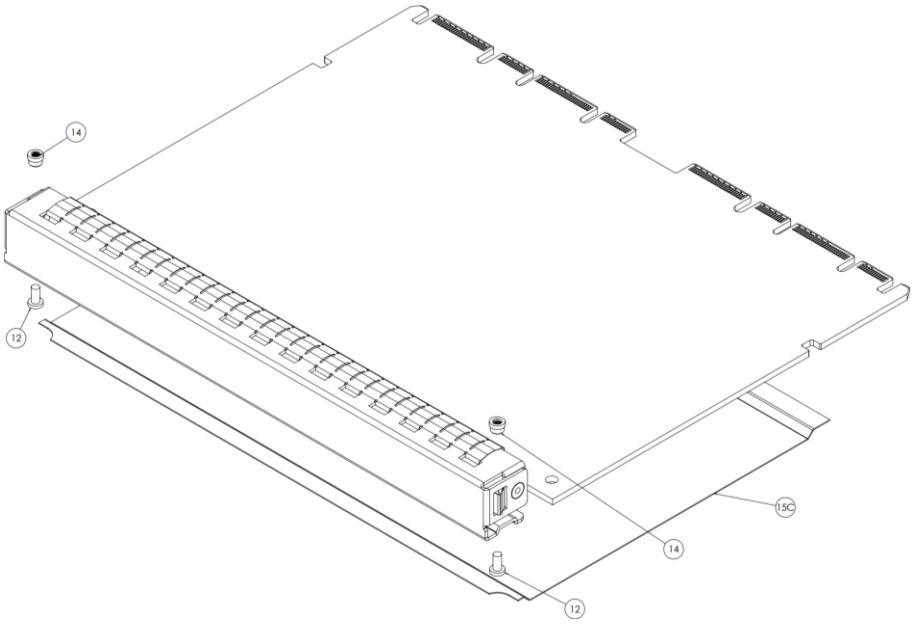
2.5.2 DSFF / TDSFF Top Level Assemblies

The images in Figure 36 illustrate the exploded top-level assemblies for the DSFF with an insulator and a DSFF with a backing plate.

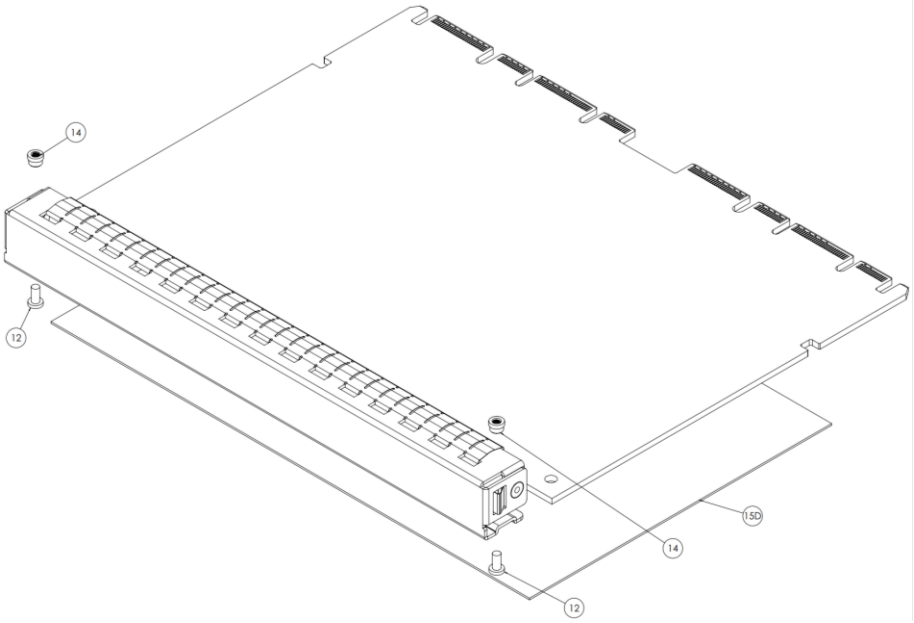
> **Note:** The TDSFF implementation uses the same PCB outline as the DSFF. The faceplate and top-side Z-height envelope grows to 14.20 mm. Refer to the faceplate subassembly drawings in Section 2.6 for more details.

Figure 36: PBA Exploded Views (DSFF with Insulator and Backing Plate Options)

DSFF with Insulator



DSFF with Backing Plate



2.6 Faceplate Subassembly

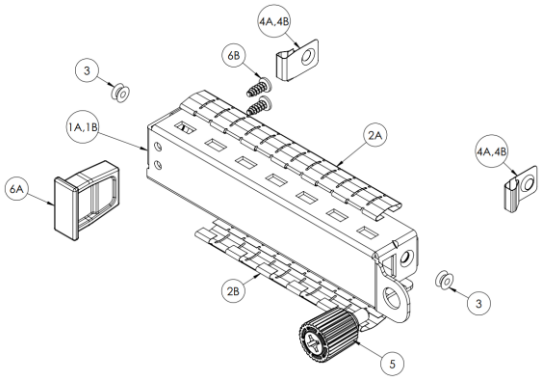
The following section defines the generic SFF, TSFF, DSFF and TDSFF faceplates.

2.6.1 Faceplate Exploded View – SFF/TSFF

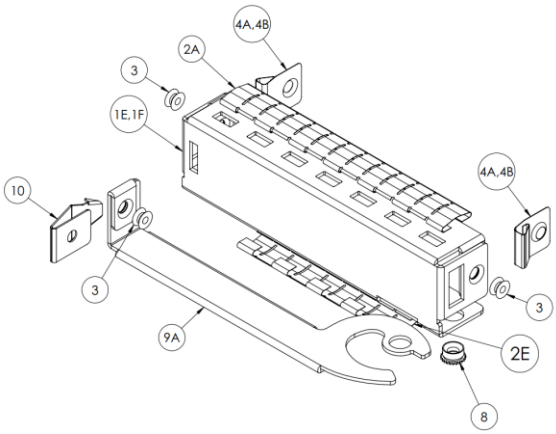
The images in Figure 37 illustrate the SFF/TSFF faceplate subassemblies as exploded views. The bill of materials is shown in Section 2.6.5.

Figure 37: Faceplate Assembly Exploded Views (SFF, TSFF)

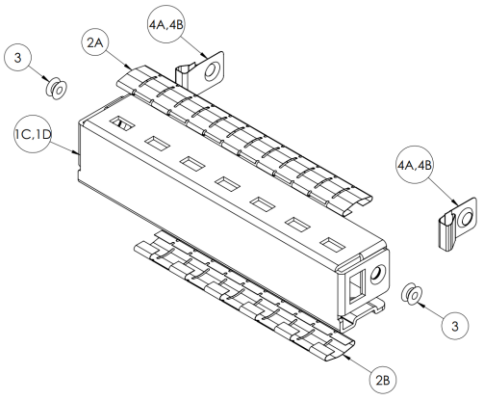
SFF, TSFF with Pull Tab



SFF, TSFF with Ejector Latch



SFF, TSFF with Internal Lock

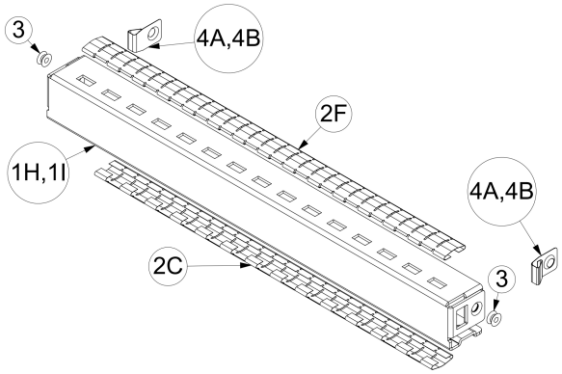


2.6.2 Faceplate Exploded View – DSFF/TDSFF

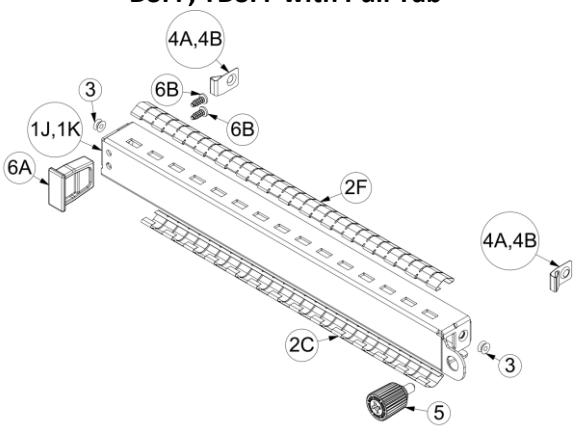
The image in Figure 38 illustrates the DSFF/TDSFF faceplate subassemblies as exploded views. The bill of materials is shown in Section 2.6.5.

Figure 38: Faceplate Assembly Exploded Views (DSFF, TDSFF)

DSFF, TDSFF with Internal Lock



DSFF, TDSFF with Pull Tab

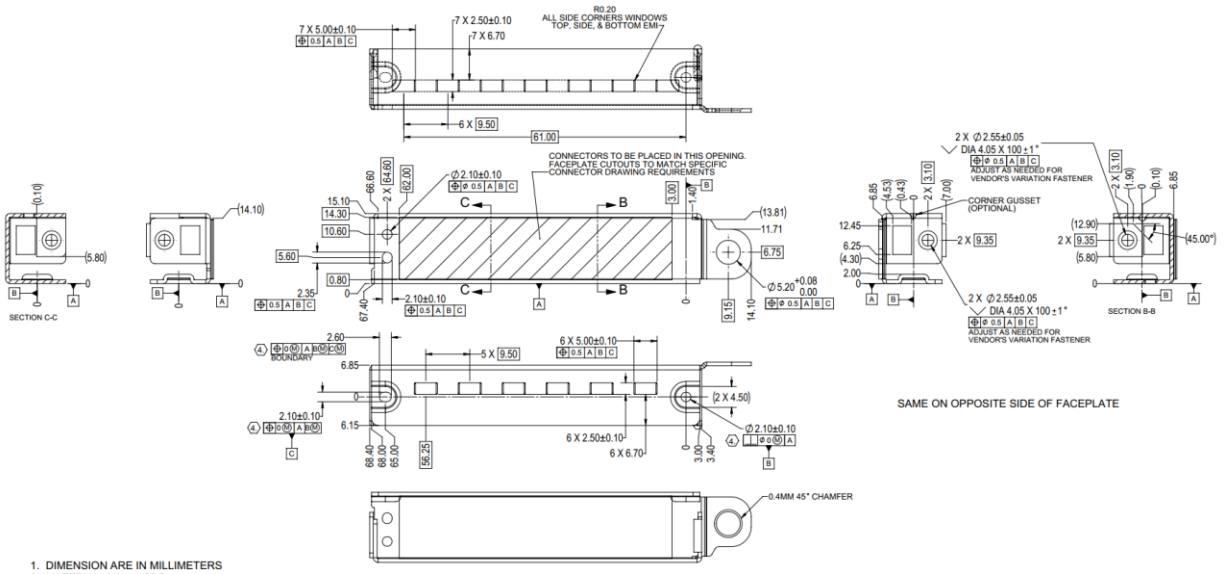


2.6.3 Generic I/O Faceplates

2.6.3.1 SFF Generic I/O Faceplates

Figure 39 shows the standard SFF I/O bracket with a thumbscrew and pull-tab assembly.

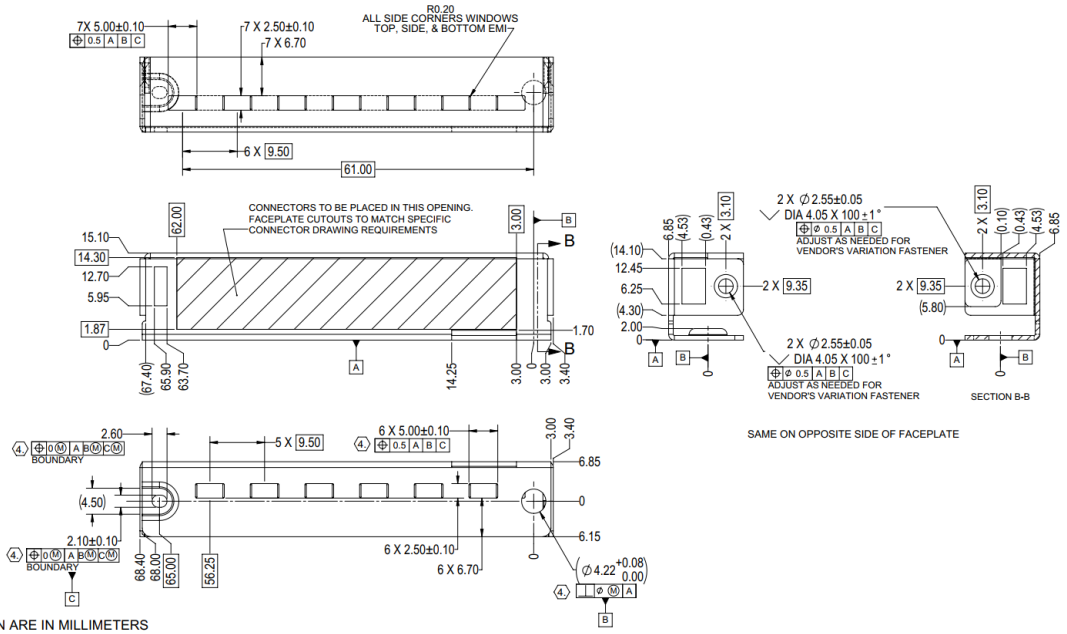
Figure 39: SFF Generic I/O Faceplate – Pull Tab Version (2D View)



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm CRS
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.25mm, MAX BEND RADIUS 0.30mm
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS ALLOWED. FACEPLATE GEOMETRY MUST BE MAINTAINED.
6. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

Figure 40 shows the standard SFF I/O bracket with an ejector latch assembly.

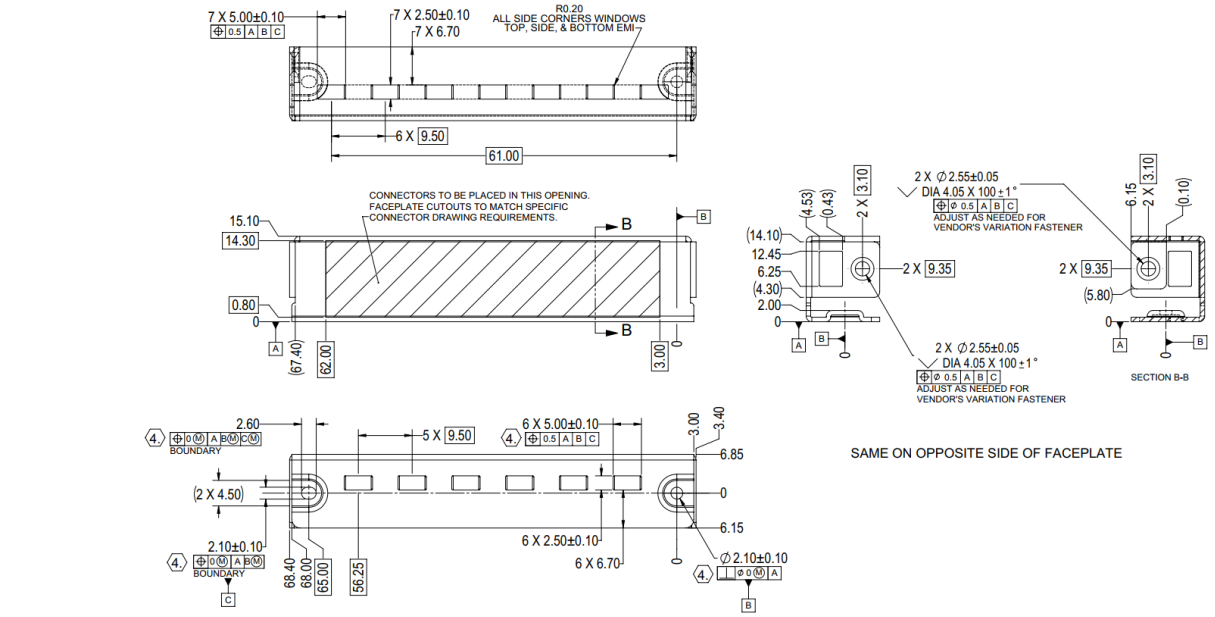
Figure 40: SFF Generic I/O Faceplate – Ejector Version (2D View)



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm CRS
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, MAX BEND RADIUS 0.30mm
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS ALLOWED. FACEPLATE GEOMETRY MUST BE MAINTAINED.
6. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

Figure 41 shows the standard SFF I/O bracket with an internal lock assembly.

Figure 41: SFF Generic I/O Faceplate – Internal Lock Version (2D View)



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm CRS
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS AS REQUIRED. ALL CRITICAL DIMENSIONS MUST BE MAINTAINED.
6. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.6.3.2 TSFF Generic I/O Faceplates

The TSFF diagrams call out the deltas from the SFF diagrams. Refer to the SFF diagrams in Section 2.6.3.1 for the remaining details.

Figure 42: TSFF Generic I/O Faceplate – Pull Tab Version (2D View)

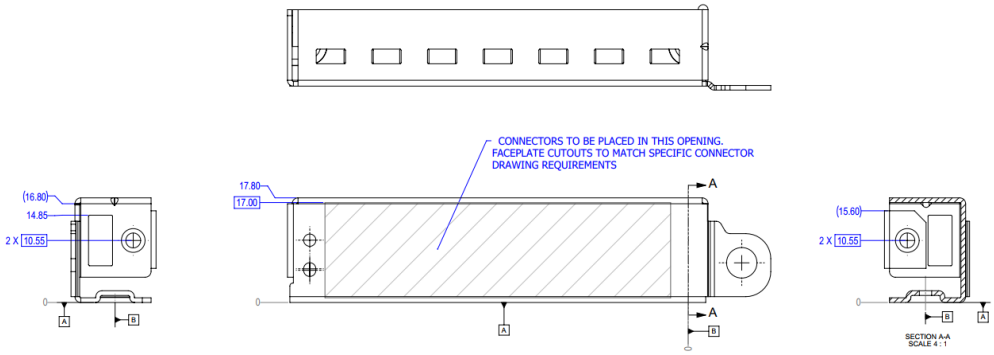


Figure 43: TSFF Generic I/O Faceplate – Ejector Version (2D View)

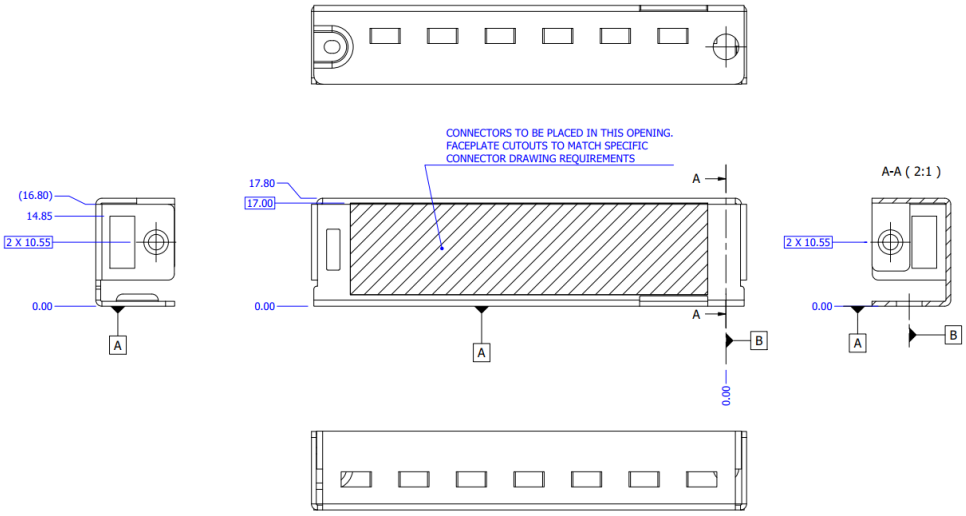
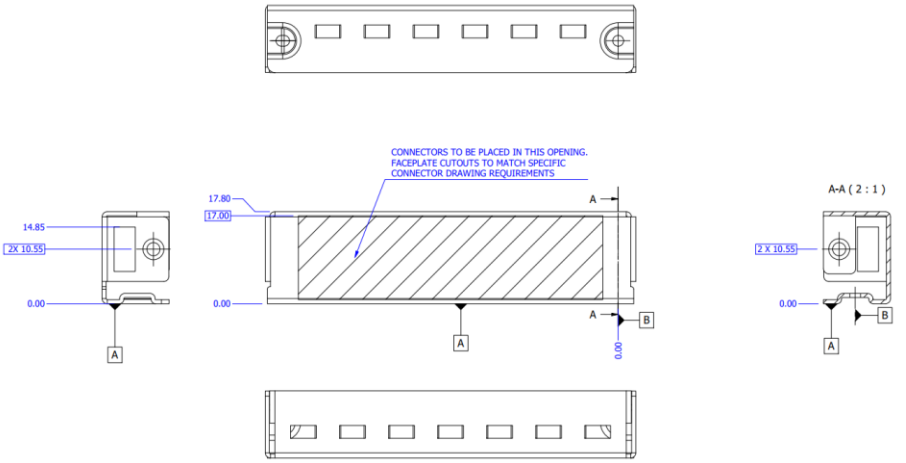


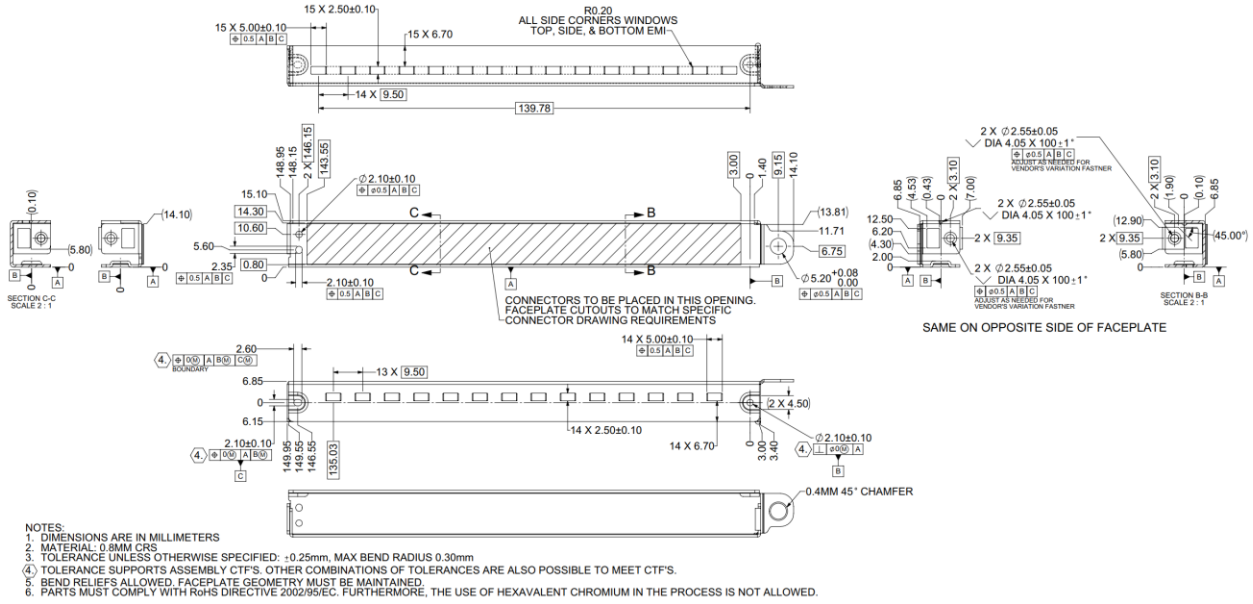
Figure 44: TSFF Generic I/O Faceplate – Internal Lock Version (2D View)



2.6.3.3 DSFF Generic I/O Faceplate

Figure 45 shows the standard DSFF I/O bracket with a thumbscrew and pull-tab assembly.

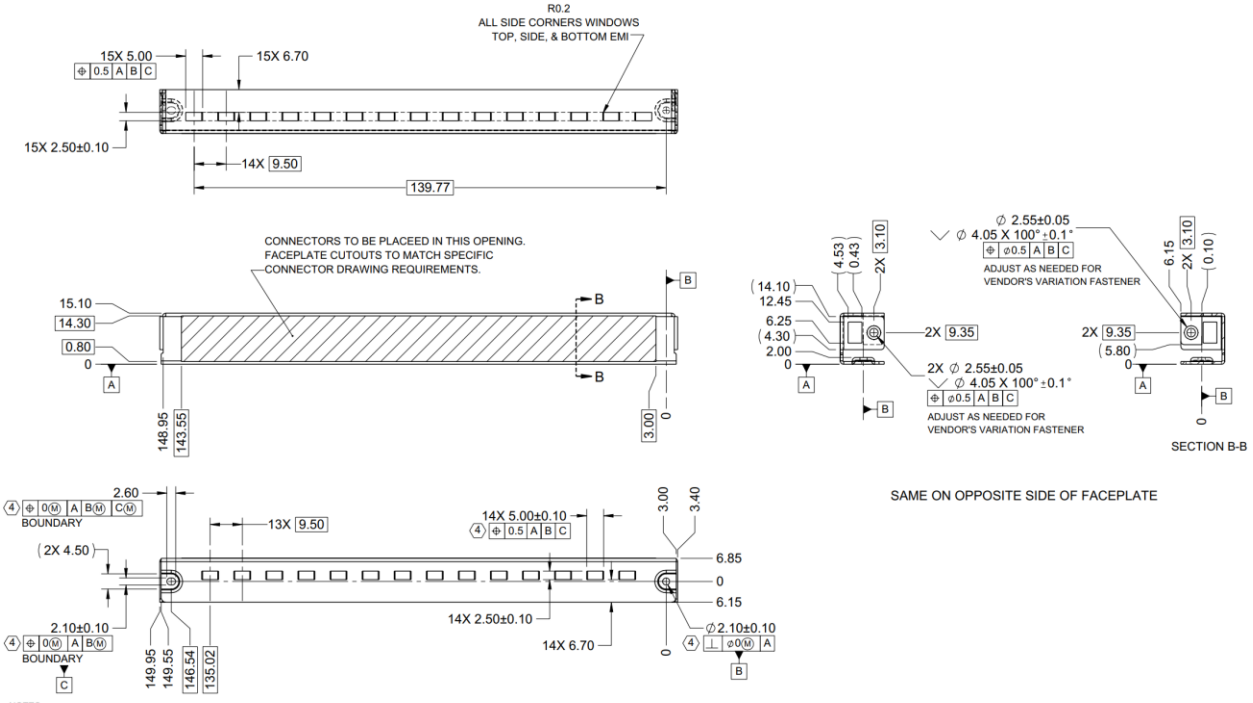
Figure 45: DSFF Generic I/O Faceplate – Pull Tab Version (2D View)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS
2. MATERIAL: 0.8MM CRS
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.25mm, MAX BEND RADIUS 0.30mm
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS ALLOWED. FACEPLATE GEOMETRY MUST BE MAINTAINED.
6. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE PROCESS IS NOT ALLOWED.

Figure 46 shows the standard DSFF I/O bracket with an internal lock assembly.

Figure 46: DSFF Generic I/O Faceplate – Internal Lock Version (2D View)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. MATERIAL: 0.8mm CRS.
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: +/- 0.25mm.
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S, OTHER COMBINATIONS OF TOLERANCE ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS AS REQUIRED. ALL CRITICAL DIMENSIONS MUST BE MAINTAINED.
6. PARTS MUST COMPLY WITH RoSH DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.6.3.4 TDSFF Generic I/O Faceplate

Figure 47 shows the standard TDSFF I/O bracket with a thumbscrew and pull-tab assembly.

Figure 47: TDSFF Generic I/O Faceplate – Pull Tab Version (2D View)

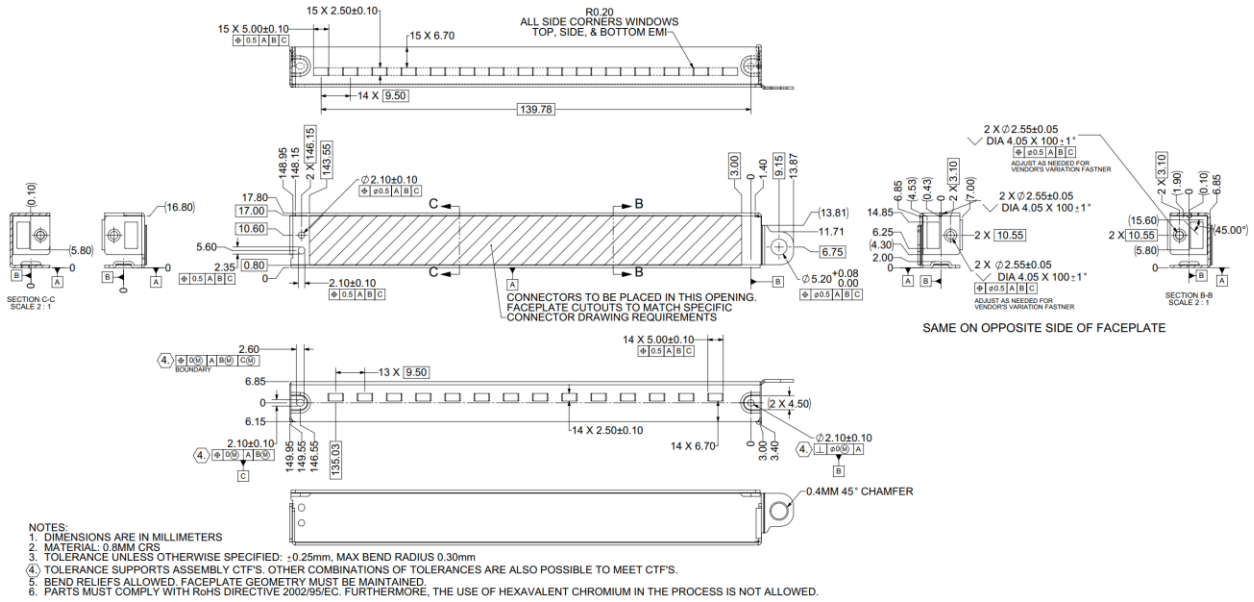
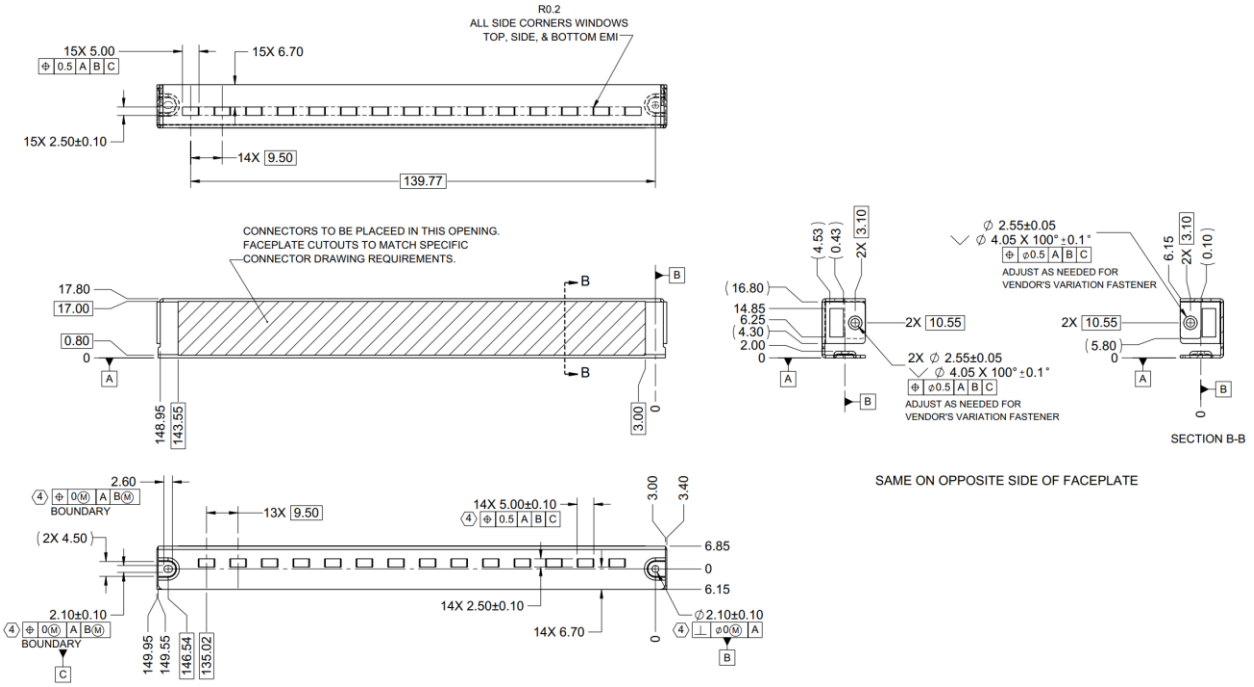


Figure 48 shows the standard TDSFF I/O bracket with an internal lock assembly.

Figure 48: TDSFF Generic I/O Faceplate – Internal Lock Version (2D View)



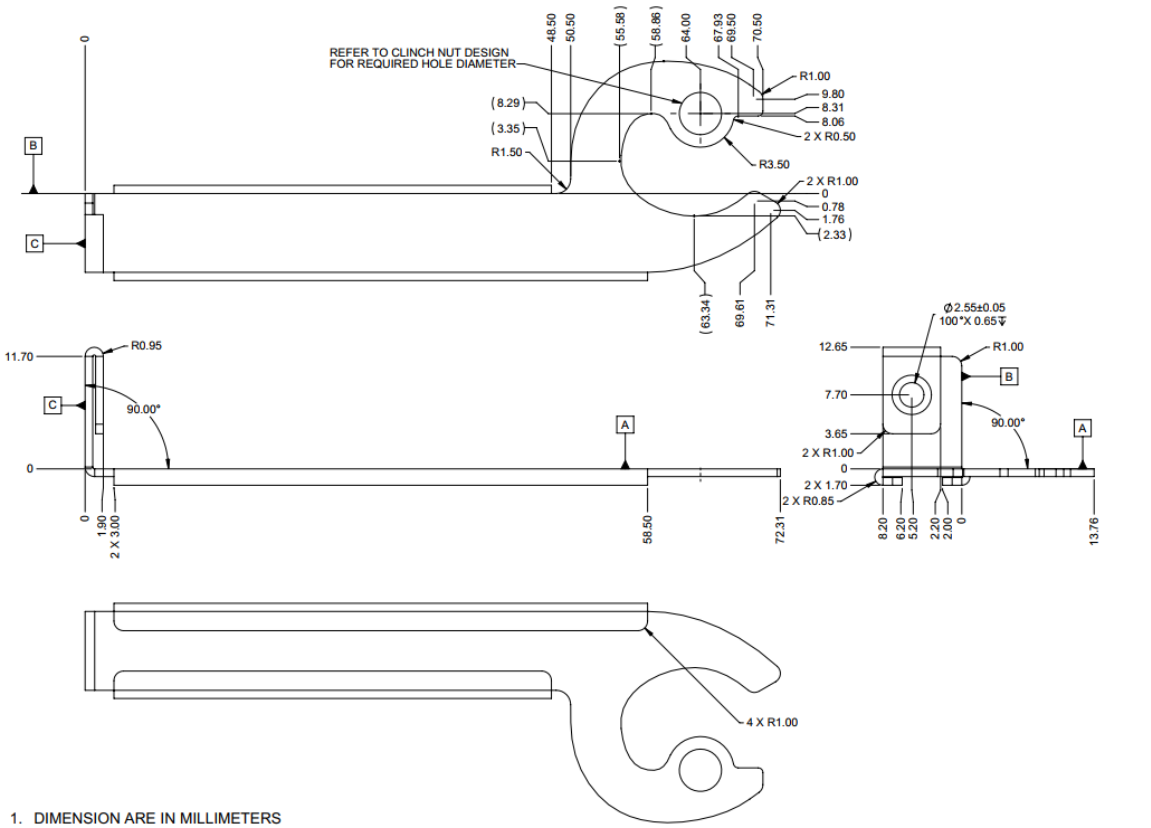
2.6.4 Ejector Levers

2.6.4.1 Ejector Lever (SFF)

This section defines the SFF lever dimensions. The TSFF uses the same lever dimensions.

Note: This SFF ejector lever may also be used on the non-shadowed LFF faceplate configuration.

Figure 49: SFF I/O Faceplate – Ejector Lever (2D View)

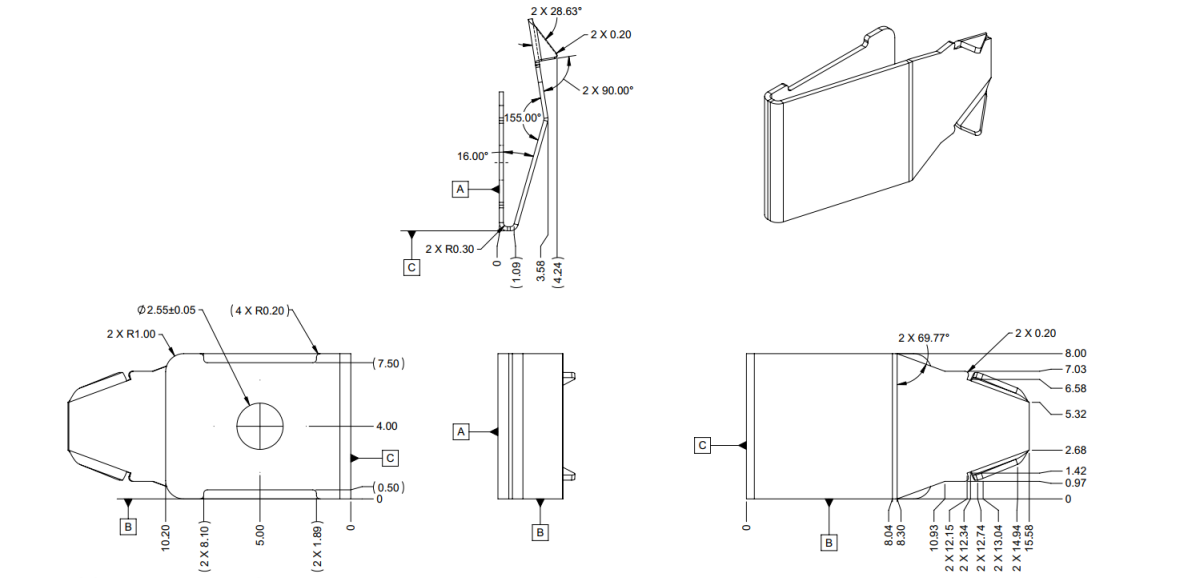


1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm 301 SS 1/4 HARD
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, ±1.0°
4. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.6.4.2 Ejector Lock

The SFF and LFF ejector uses a locking mechanism at the end of the handle to retain the lever position. This is shown in Figure 50.

Figure 50: Ejector Lock



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.3mm 301 SS 1/2 HARD
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, ±1.0°
4. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.6.4.3 Clinch Nut (For Ejector Levers)

The SFF and LFF card ejector handle uses a clinch nut as a spacer and rotation anchor. The clinch nut binds the ejector handle to the faceplate. Two clinch nut options are available to accommodate supplier manufacturing processes. These are shown in Figure 51 and Figure 52.

Figure 51: Clinch Nut Option A

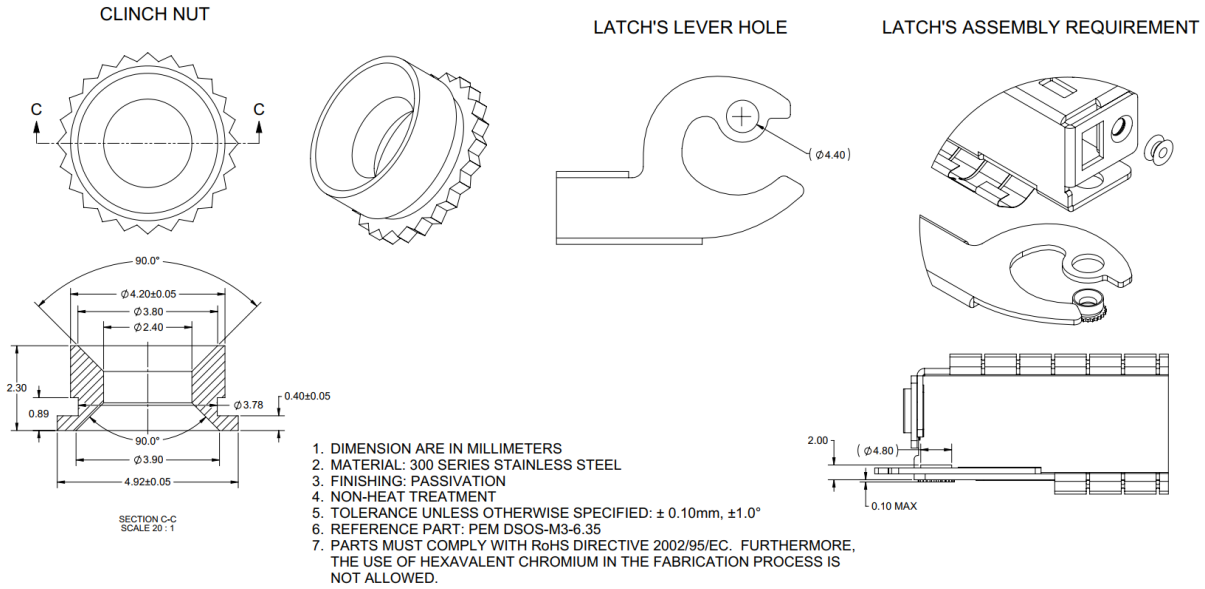
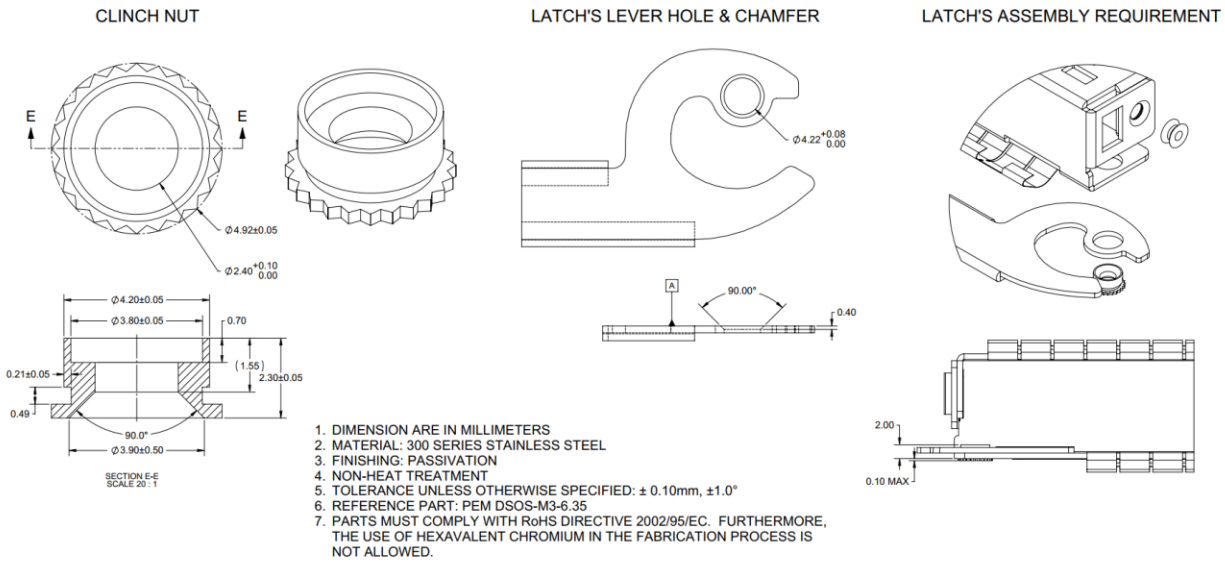


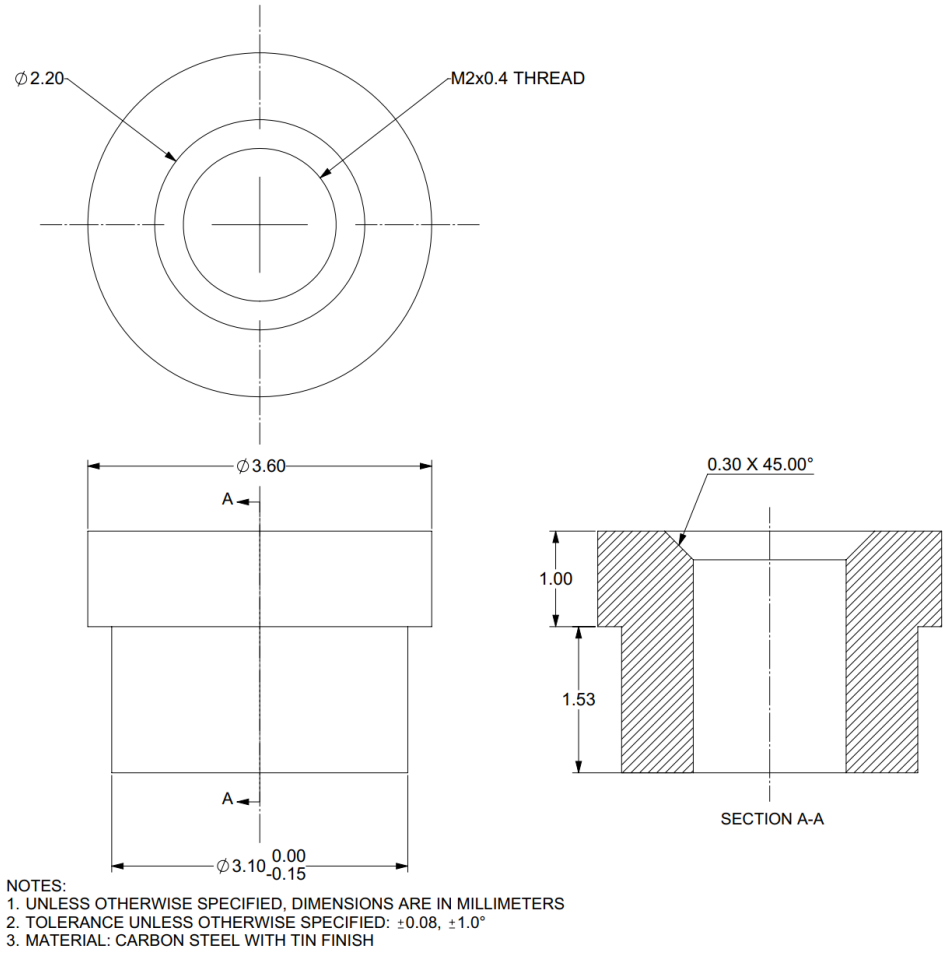
Figure 52: Clinch Nut Option B



2.6.5 SMT Nut

All OCP NIC form-factors utilize two SMT nuts to secure the faceplate to the PCB. The critical-to-function (CTF) dimensions of the SMT nut are shown in Figure 53.

Figure 53: SMT Nut CTF Dimensions



2.6.6 Faceplate Subassemblies – Bill of Materials (BOM)

Table 9 shows the bill of materials for the card SFF and TSFF assemblies. Table 10 shows the bill of materials for the DSFF and TDSFF assemblies. Item number call outs align with the item numbering in Section 2.6.1 and Section 2.6.2.

Note: Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers of Table 9. Refer to the 3D CAD files for hardware specifics not covered by this table.

Table 9: Bill of Materials for the SFF and TSFF Faceplate Assemblies

Item #	Item description	Part Number / Drawing	Supplier
1A 1B 1C 1D 1E 1F	Faceplate	See Section 2.6.3: 1A NIC_OCPv3_SFF_Faceplate_Pulltab_20190303.pdf 1B NIC_OCPv3_TSFF_Faceplate_Pulltab_20210527.pdf 1C NIC_OCPv3_SFF_Faceplate_Latch_20190719.pdf 1D NIC_OCPv3_TSFF_Faceplate_Latch_20210527.pdf 1E NIC_OCPv3_SFF_Faceplate_IntLatch_20190303.pdf 1F NIC_OCPv3_TSFF_Faceplate_IntLatch_20210527.pdf	Custom
2A 2B 2E	Top and Bottom EMI Fingers	2A LT18CJ1921 – 13 fingers (Laird) TF187VE32F11-2.41-08 (Tech-Etch) 2B LT18CJ1920 – 11 fingers (Laird) TF187VE32F11-2.04-08 (Tech-Etch) 2E LT18CJ4430 – 9 fingers (Laird) TF187VE32F11-1.67-08 (Tech-Etch)	Laird, Tech-ETCH
3	Rivet	1-AC-2424-01	Dong Guan KSETT Hardware Technology
4A 4B	Side EMI Fingers	4A LT18DP1911 (for SFF) 4B LT21DP2320 (for TSFF)	Laird
5	Thumbscrew	4C-99-343-K081	Southco, Inc.
6A 6B	Pull tab w/2x screws	CN-99-459	Southco, Inc.
8	Clinch Nut	See Section 2.6.4.3 and drawing NIC_OCPv3_ClinchNut_20190719.pdf	Custom
9A	Ejector Handle	**SFF Ejector**: See Section 2.6.4 and drawing 9A NIC_OCPv3_EjectorHandle_Short_20190719.pdf	Custom
10	Ejector Lock	See Section 2.6.4.2 and drawing NIC_OCPv3_EjectorLock_20190719.pdf	Custom
12*	Screw for securing faceplate to NIC	Phillips screw: ICMMBS200403N Torx screw: ITMMAE200402X	WUJIANG Screw Tech Precision Industry
13*	Screw for attaching faceplate and ejector to NIC	Phillips screw: FCMMQ200503N Torx screw: FTMMC200502X	WUJIANG Screw Tech Precision Industry

Item #	Item description	Part Number / Drawing	Supplier
14	SMT nut (on NIC)	See Section 2.6.5 and drawing: nic_v3_SMT_Nut_M2x0.4.pdf 82-950-22-010-05-RL (Fivetech)	Custom or Fivetech Technology Inc.
15A	Insulator	Refer to Section 2.7 for the SFF (15A) insulator mechanical requirements	Custom

Note: * Phillips and Torx screws are allowed. Head types should not be mixed on the same assembly.

Table 10: Bill of Materials for the DSFF and TDSFF Faceplate Assemblies

Item #	Item description	Part Number / Drawing	Supplier
1H 1I 1J 1K	Faceplate	See Section 2.6.3: 1H nic_v3_dsff_faceplate_int_lock.pdf 1I nic_v3_tdsff_faceplate_int_lock.pdf 1J nic_v3_dsff_faceplate_pulltab.pdf 1K nic_v3_tdsff_faceplate_pulltab.pdf	Custom
2C 2F	Top and Bottom EMI Fingers	2C LT18CJ1923 – 27 fingers (Laird) TF187VE32F11-5.03-08 (Tech-Etch) 2F LT24CJ3440 – 29 fingers (Laird)	Laird, Tech-ETCH
3	Rivet	1-AC-2424-01	Dong Guan KSETT Hardware Technology
4A 4B	Side EMI Fingers	4A LT18DP1911 (for DSFF) (Laird) 4B LT21DP2320 (for TDSFF) (Laird) TF187VE32F11-5.41-08 (Tech-Etch)	Laird, Tech-Etch
5	Thumbscrew	4C-99-343-K081	Southco, Inc.
6A 6B	Pull tab w/2x screws	CN-99-459	Southco, Inc.
12*	Screw for securing faceplate to NIC	Phillips screw: ICMMBS200403N Torx screw: ITMMAE200402X	WUJIANG Screw Tech Precision Industry
14	SMT nut (on NIC)	See Section 2.6.5 and drawing: nic_v3_SMT_Nut_M2x0.4.pdf 82-950-22-010-05-RL (Fivetech)	Custom or Fivetech Technology Inc.
15C 15D	Insulator Backing Plate	Refer to Section 2.7 for the DSFF insulator (15C) and backing plate (15D) mechanical requirements	Custom

Note: * Phillips and Torx screws are allowed. Head types should not be mixed on the same assembly.

2.7 Card Insulator / Backing Plate Requirements

All OCP NIC 3.0 cards shall implement an insulator or backing plate with insulative properties to prevent the card bottom side components from shorting out to the baseboard chassis. The backing plate also offers the advantage of allowing components to be placed closer to gold finger edge to improve signal integrity and offers other possible thermal and mechanical benefits.

The recommended insulator thickness is 0.25 mm and shall reside within the following mechanical envelopes for the SFF, TSFF, DSFF and TDSFF. An alternate insulator thickness of 0.127 mm is permitted. The total stack up height of the secondary side components, insulator and the labels shall not exceed the 2 mm keep-in dimension. A maximum of four circular holes with a 4 mm maximum diameter are permitted for access to mechanical retention components. Any components exposed by these holes must be non-conductive.

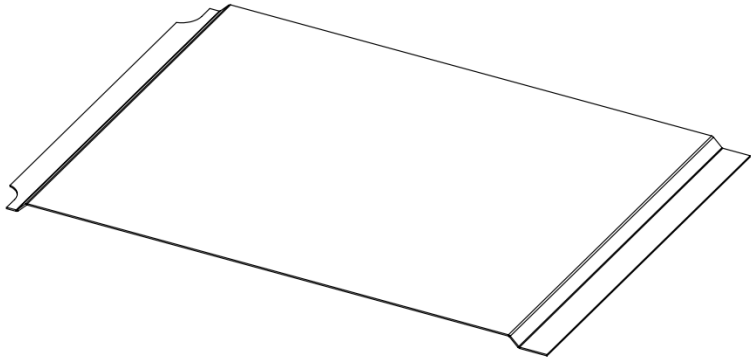
The recommended backing plate thickness is 0.8mm and shall reside within the following mechanical envelopes for the SFF, TSFF, DSFF and TDSFF. An alternate backing plate thickness is permitted at the designer's discretion. The total stack up height of the secondary side components, card side insulator, backing plate and the labels shall not exceed the 2 mm keep-in dimension.

The backing plate material is recommended to be nickel plated steel with an insulating material applied to the inside of backing plate surface to prevent electrical shorts. Examples of insulation materials that could be used include; 3M 521 conformal coating or LEXAN FR700 insulating material, among many others available on the market. Other backing plate materials are permitted at the designer's discretion so long as the shorting risk is addressed.

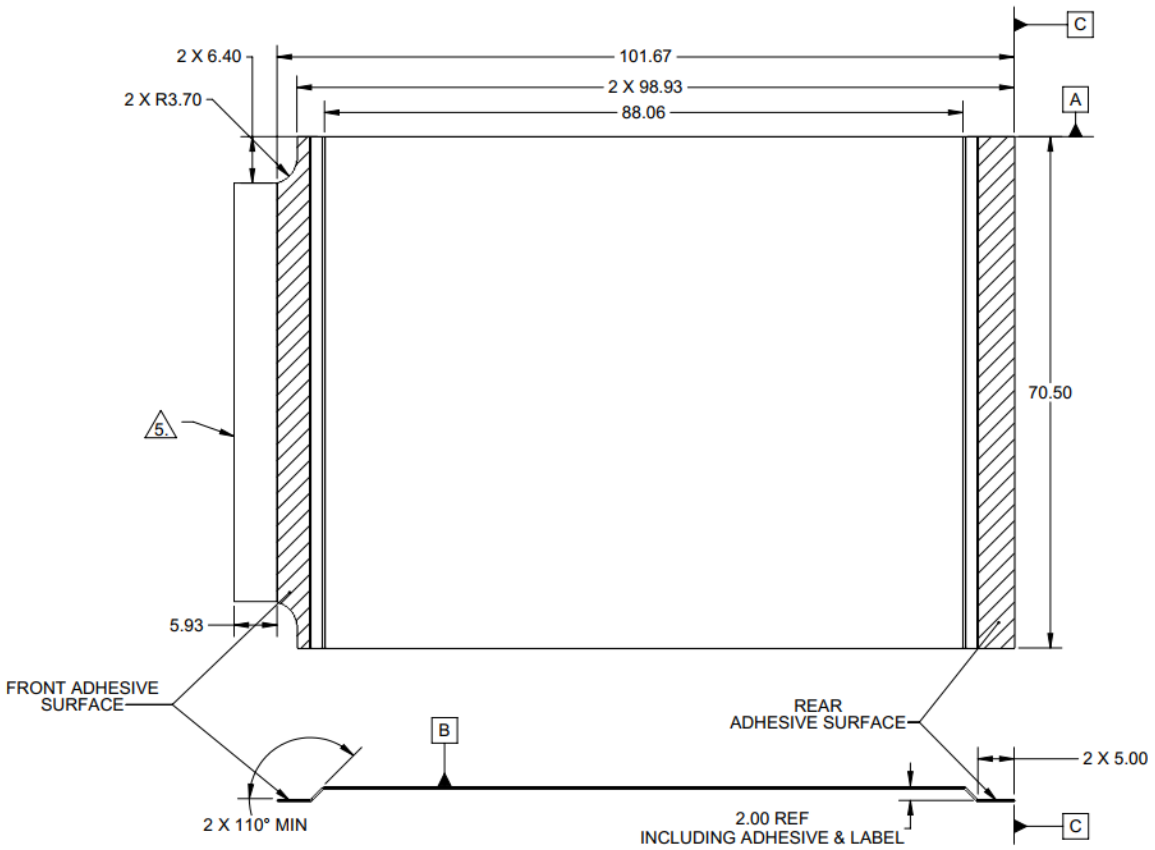
Holes may be added through backing plate to enable taller components, but components shall not be allowed to protrude through the bottom surface of the backing plate under any circumstances. It is recommended that a sufficient number of standoffs be incorporated into the backing plate design to affix the backing plate to the PCB and also to reduce the risk of flexure of the backing plate

2.7.1 SFF, TSFF Insulator

Figure 54: SFF, TSFF Bottom Side Insulator (3D View)



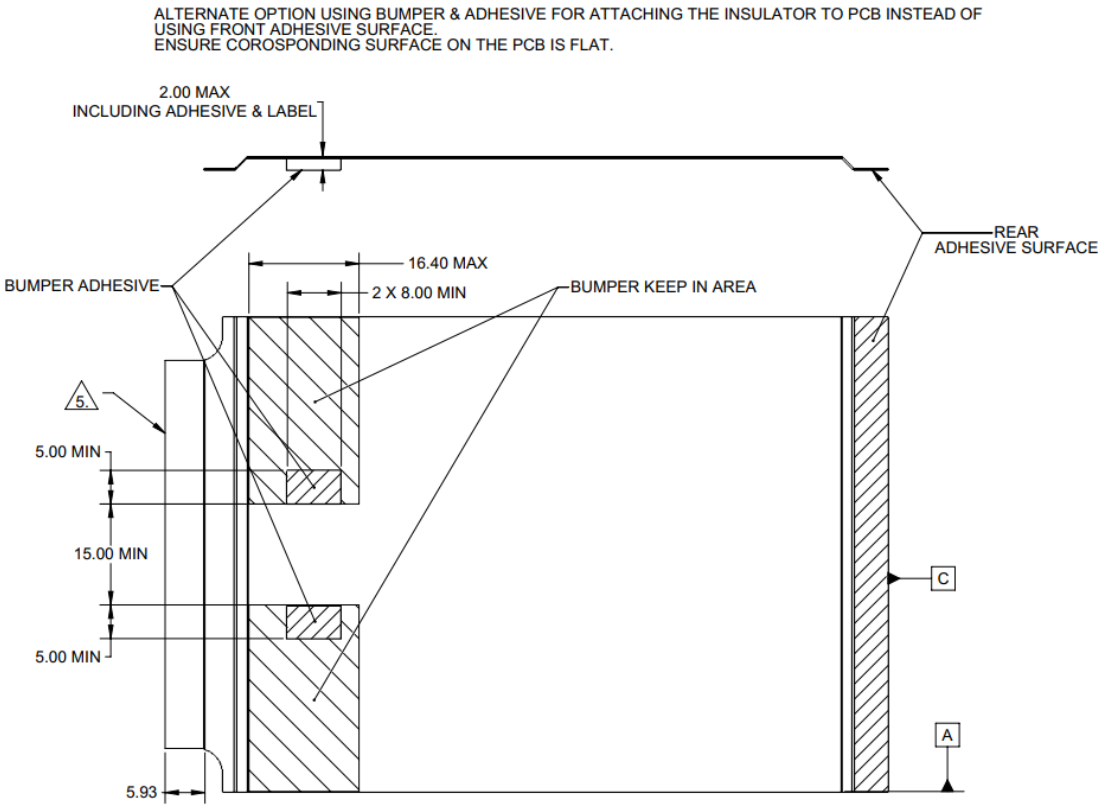
1384 Figure 55: SFF, TSFF Bottom Side Insulator (Top and Side View)



1. DIMENSIONS ARE IN MILLIMETERS
2. MATERIAL:
   1. FORMEX GK-10BK or FORMEX N3 (HALOGEN FREE, BLACK OR NATURAL), 0.25mm THICKNESS
   2. FORMEX GK-5BK (HALOGEN FREE, BLACK), 0.127mm THICKNESS
3. MATERIAL SHALL CONFORM TO 94VTM-0
4. ADHESIVE 3M 467MP 0.05mm THICKNESS
5. FRONT EDGE OF INSULATOR AND ADHESIVE MAY EXTEND TO 107.60MM IF NECESSARY TO PROTECT LEDS ON SECONDARY SIDE OF PCBA.
6. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.30mm, ±1.0°

1385
1386

Figure 56: SFF, TSFF Bottom Side Insulator (alternate) (Top and Side View)



2.7.2 DSFF, TDSFF Insulator

Figure 57: DSFF, TDSFF Bottom Side Insulator (3D View)

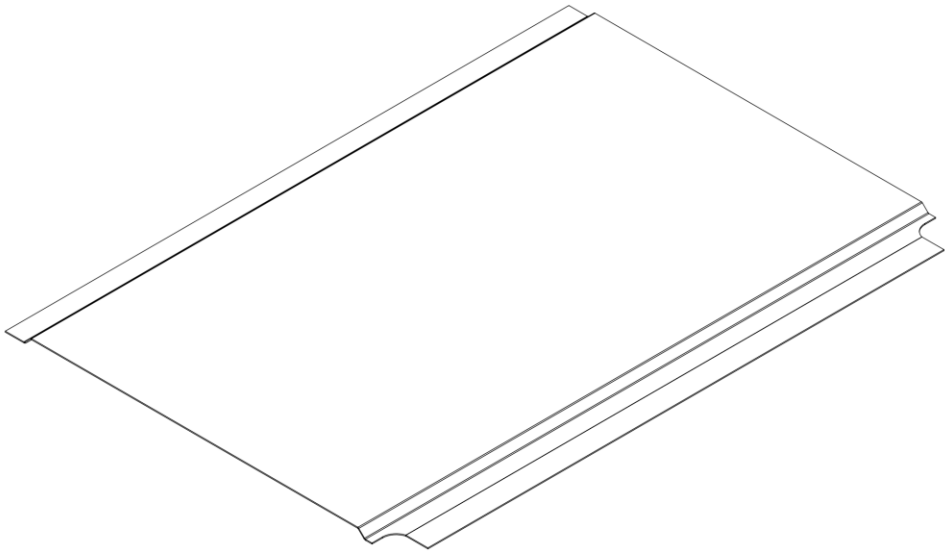
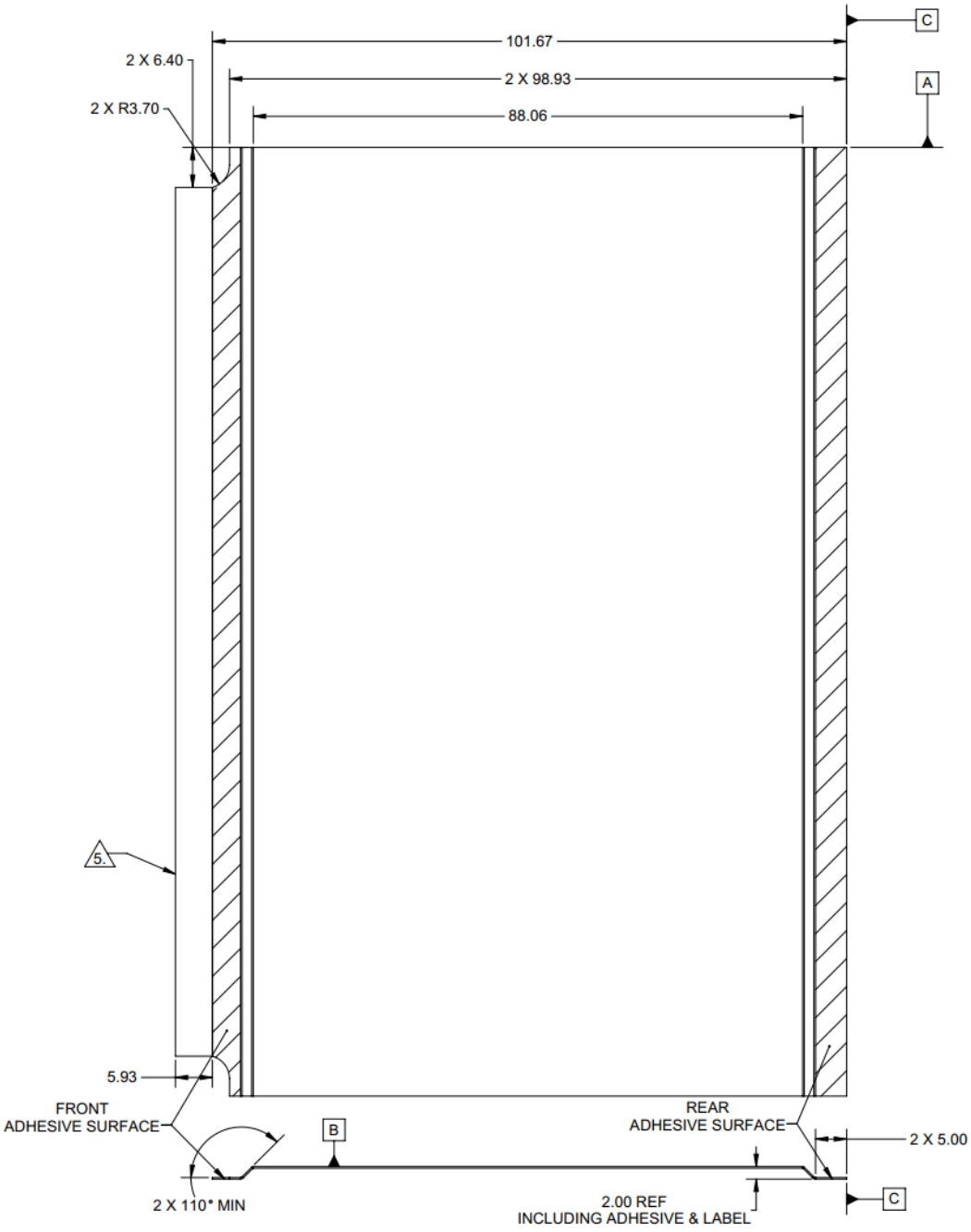


Figure 58: DSFF, TDSFF Bottom Side Insulator (Top and Side View)



1. DIMENSIONS ARE IN MILLIMETERS
2. MATERIAL:
   1. FORMEX GK-10BK or FORMEX N3 (HALOGEN FREE, BLACK OR NATURAL), 0.25mm THICKNESS
   2. FORMEX GK-5BK (HALOGEN FREE, BLACK), 0.127mm THICKNESS
3. MATERIAL SHALL CONFORM TO 94VTM-0
4. ADHESIVE 3M 467MP 0.05mm THICKNESS
5. FRONT EDGE OF INSULATOR AND ADHESIVE MAY EXTEND TO 107.60mm IF NECESSARY TO PROTECT LEDS ON SECONDARY SIDE OF PCB
6. TOLERANCE UNLESS OTHERWISE SPECFIED: ±0.30mm, ±1.0°

2.7.3 DSFF, TDSFF Backing Plate

Figure 59: DSFF, TDSFF Bottom Side Backing Plate (3D View)

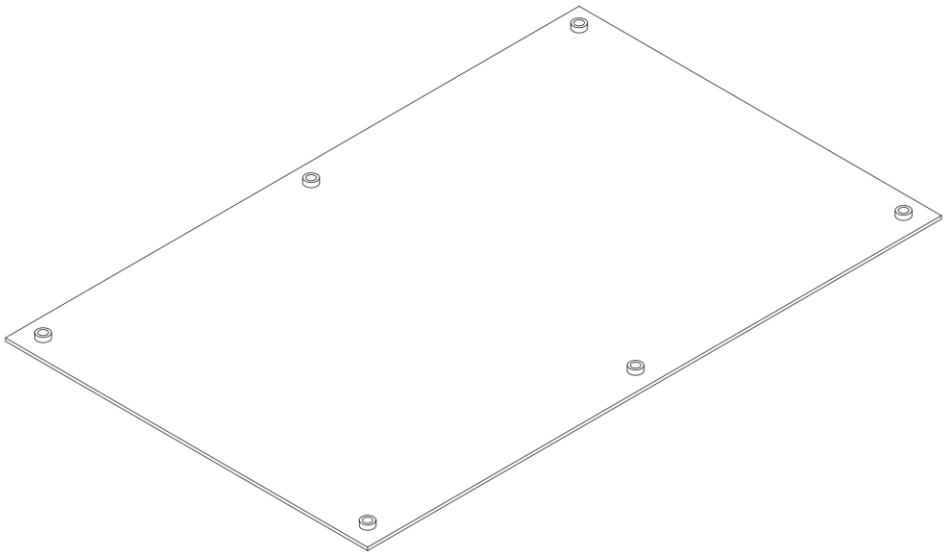
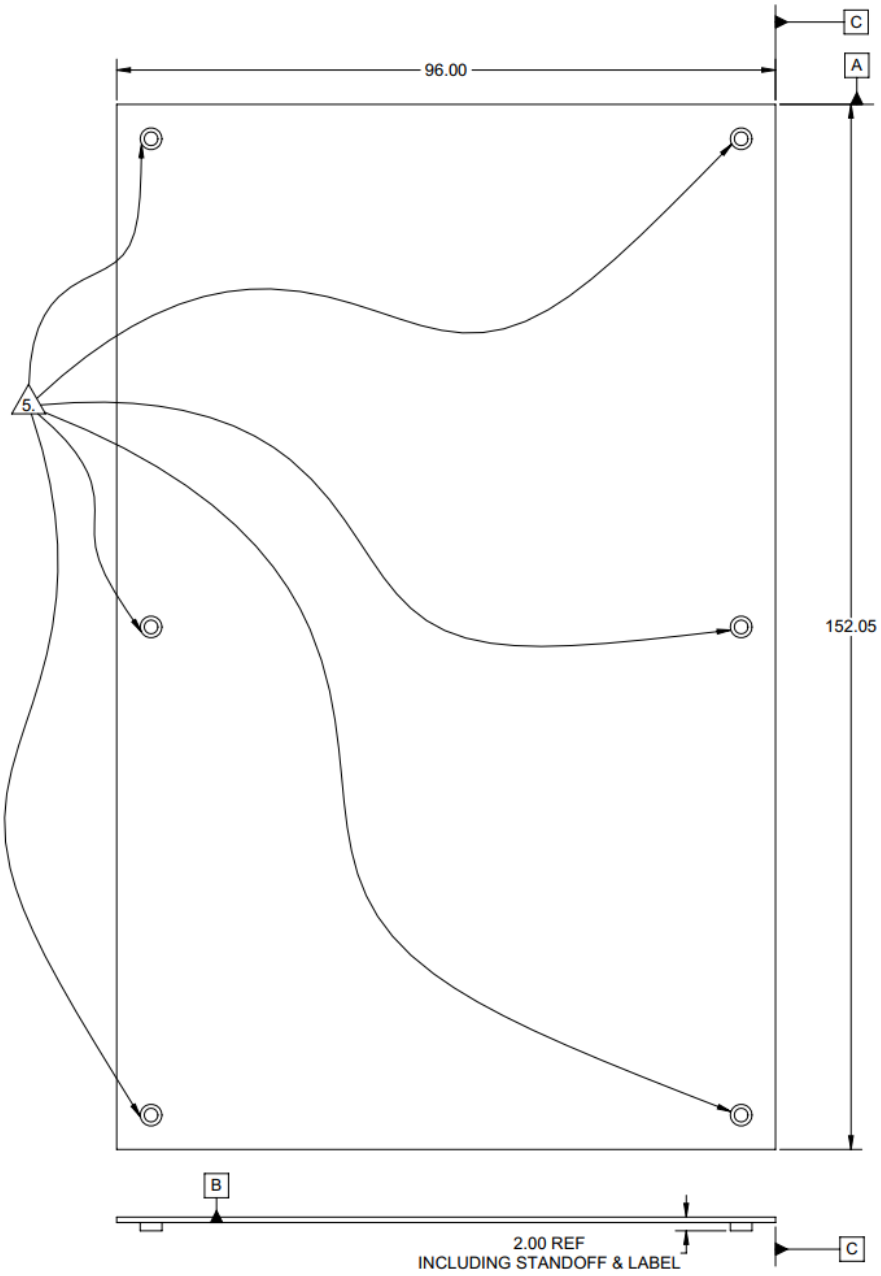


Figure 60: DSFF, TDSFF Bottom Side Backing Plate (Top and Side View)



1. DIMENSIONS ARE IN MILLIMETERS
2. BACKING PLATE MATERIAL:
   1. NICKEL PLATED STEEL, 0.8mm THICKNESS
   2. RIGID MATERIAL OF DESIGNER'S CHOICE
3. INSULATOR MATERIAL:
   1. LEXAN FR700, 0.25mm THICKNESS
   2. 3M 521 CONFORMAL COATING
   3. INSULATING MATERIAL OF DESIGNER'S CHOICE
4. MATERIAL SHALL CONFORM TO 94VTM-0
5. STANDOFFS CAN BE PLACED AS NEEDED TO REDUCE BACKING PLATE FLEXURE
6. TOLERANCE UNLESS OTHERWISE SPECFIED: ±0.30mm, ±1.0°

2.8 Card Critical-to-Function (CTF) Dimensions

2.8.1 CTF Tolerances

The CTF tolerances shown in Table 11 are used in this section and are applicable for all the board form-factors and heights.

Table 11: CTF Default Tolerances

CTF DEFAULT TOLERANCES	
DIMENSION RANGE	TOLERANCE
	TWO PLACE DECIMALS: X.XX
LINEAR:	± 0.30
ANGULAR:	± 1.00 DEGREES
HOLE DIAMETER:	± 0.13

2.8.2 SFF CTF Dimensions

2.8.2.1 SFF Pull Tab CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF OCP NIC 3.0 card with a pull tab and thumbscrew. The CTF default tolerances are shown in Section 2.8.1.

Figure 61: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View)

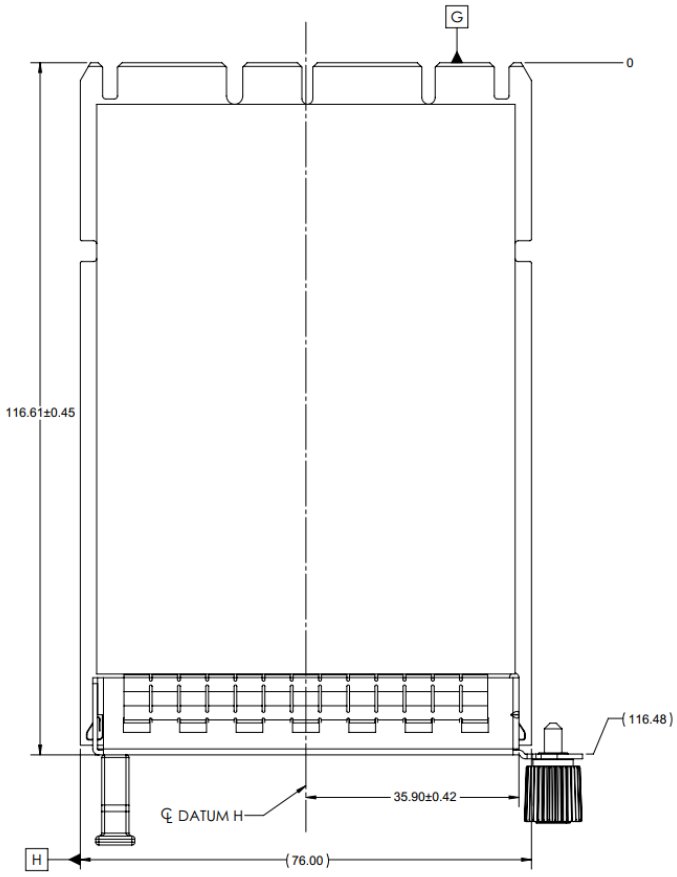


Figure 62: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Front View)

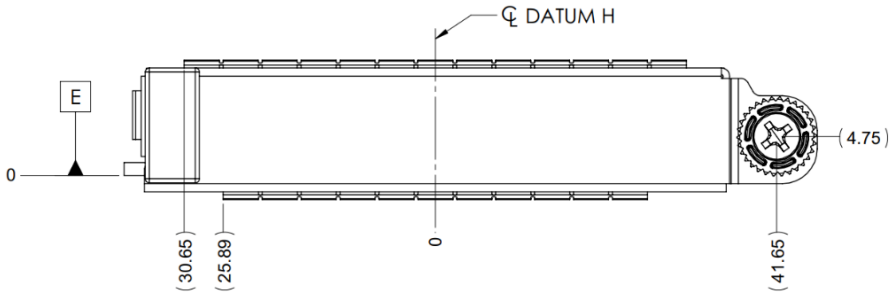
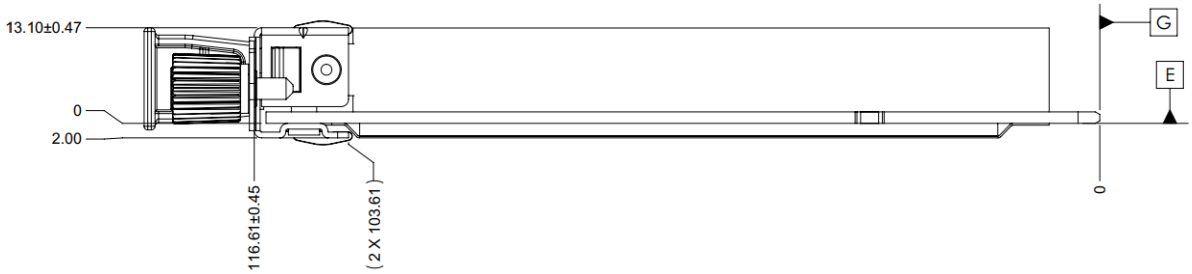


Figure 63: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Side View)



2.8.2.2 SFF Ejector Latch CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF OCP NIC 3.0 card with an ejector latch. The CTF default tolerances are shown in Section 2.8.1.

Figure 64: SFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View)

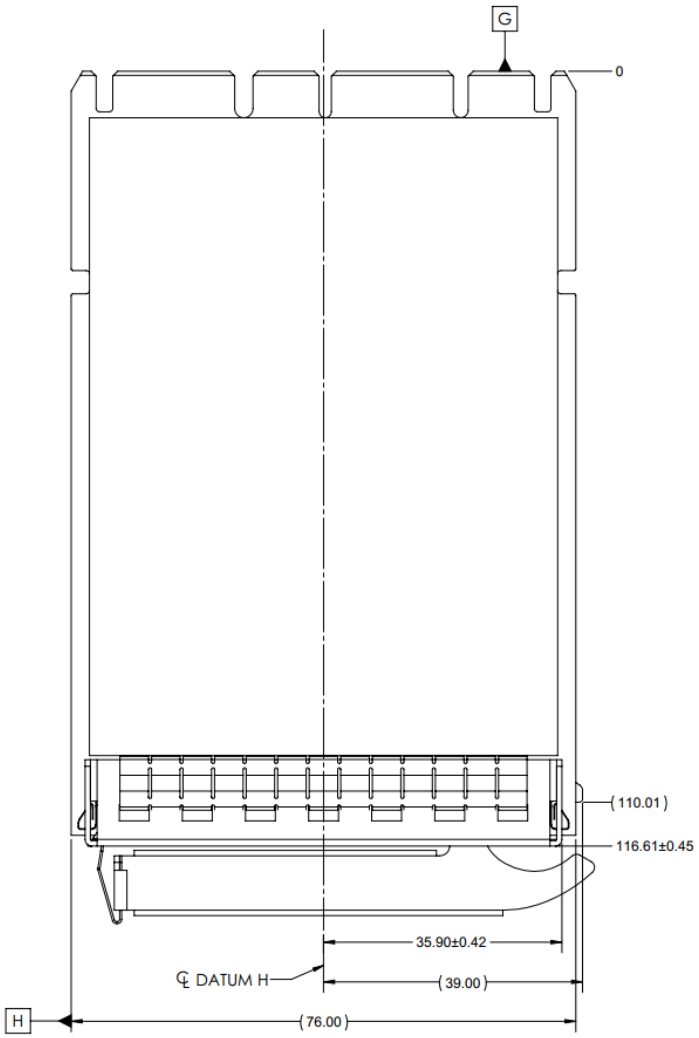


Figure 65: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View)

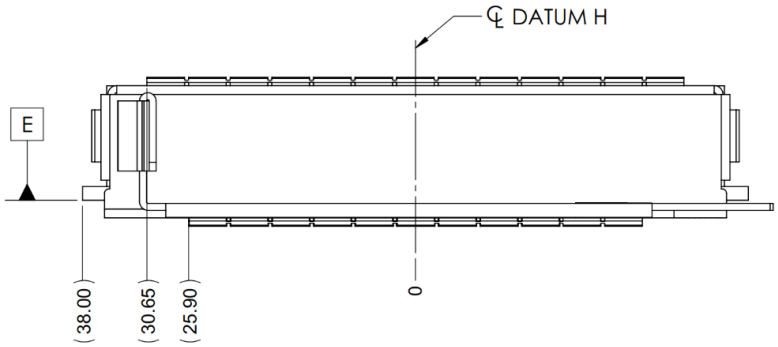


Figure 66: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View)



2.8.2.3 SFF Internal Lock CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF OCP NIC 3.0 card with an internal lock. The CTF default tolerances are shown in Section 2.8.1.

Figure 67: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View)

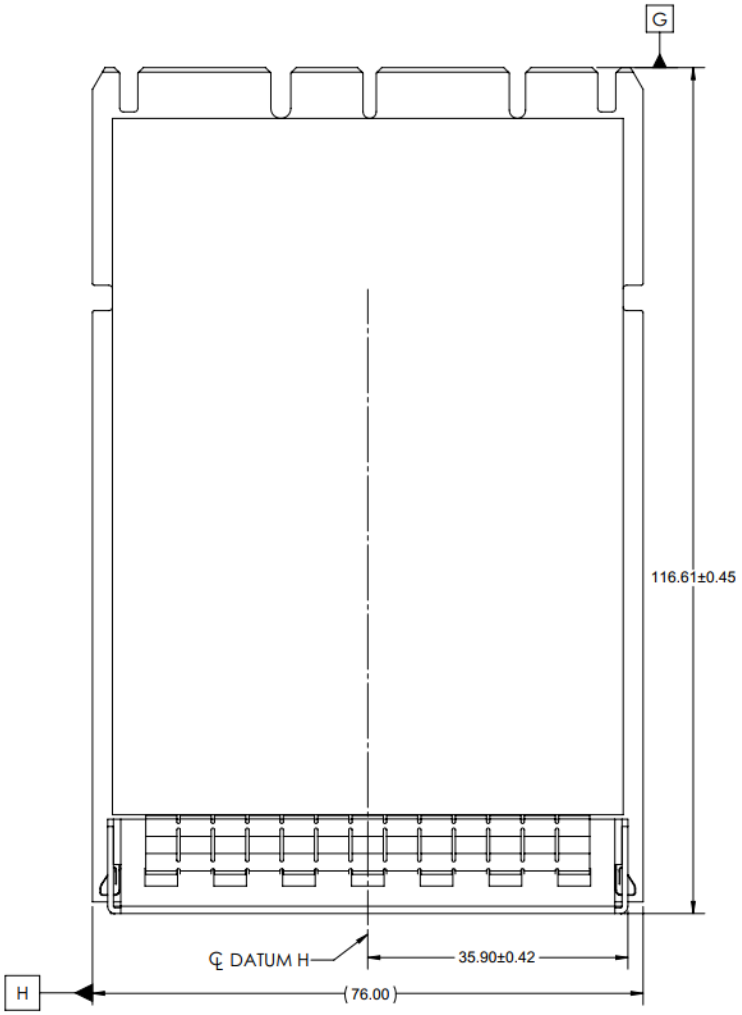


Figure 68: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Front View)

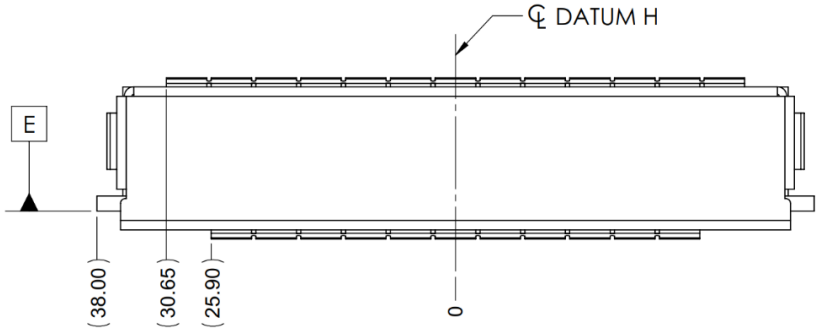
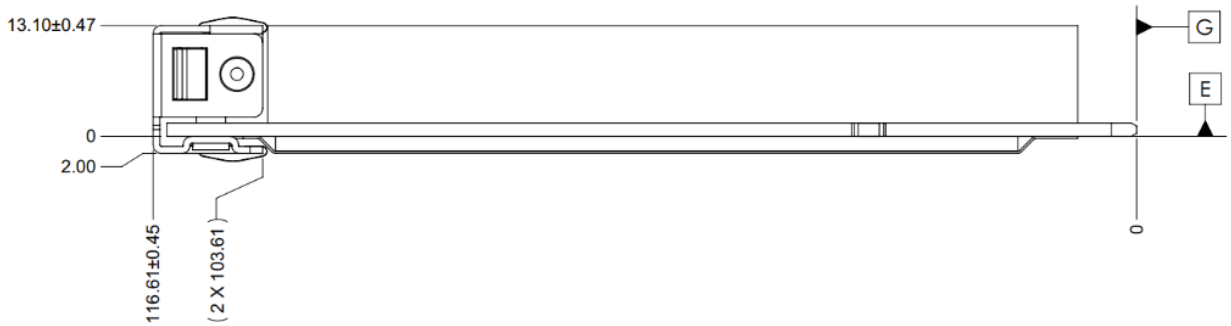


Figure 69: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View)

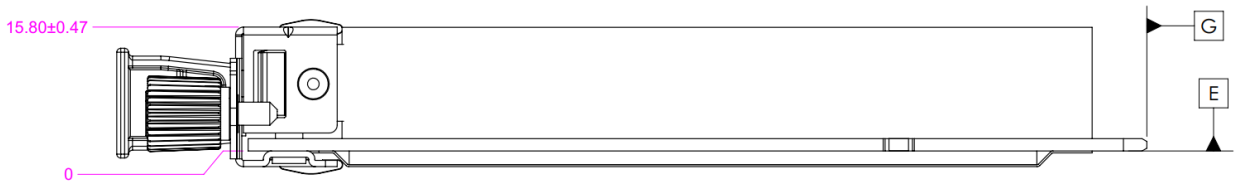


2.8.3 TSFF CTF Dimensions

2.8.3.1 TSFF Pull Tab CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

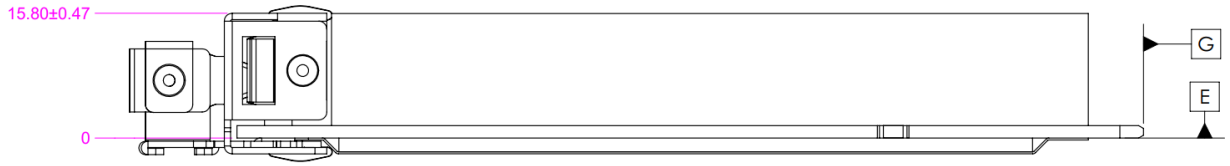
Figure 70: TSFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View)



2.8.3.2 TSFF Ejector Latch CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

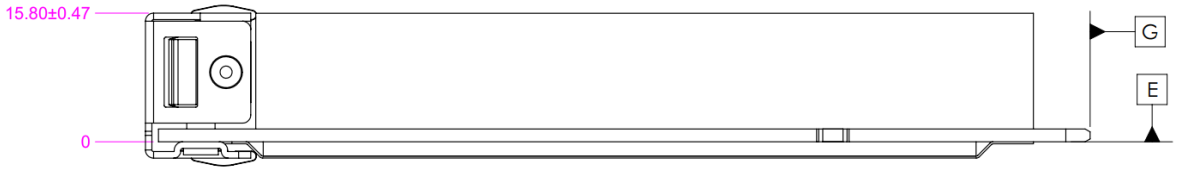
Figure 71: TSFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View)



2.8.3.3 TSFF Internal Lock CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

Figure 72: TSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View)



2.8.4 DSFF CTF Dimensions

2.8.4.1 DSFF Internal Lock CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each DSFF OCP NIC 3.0 card with an internal lock. The CTF default tolerances are shown in Section 2.8.1.

Figure 73: DSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View)

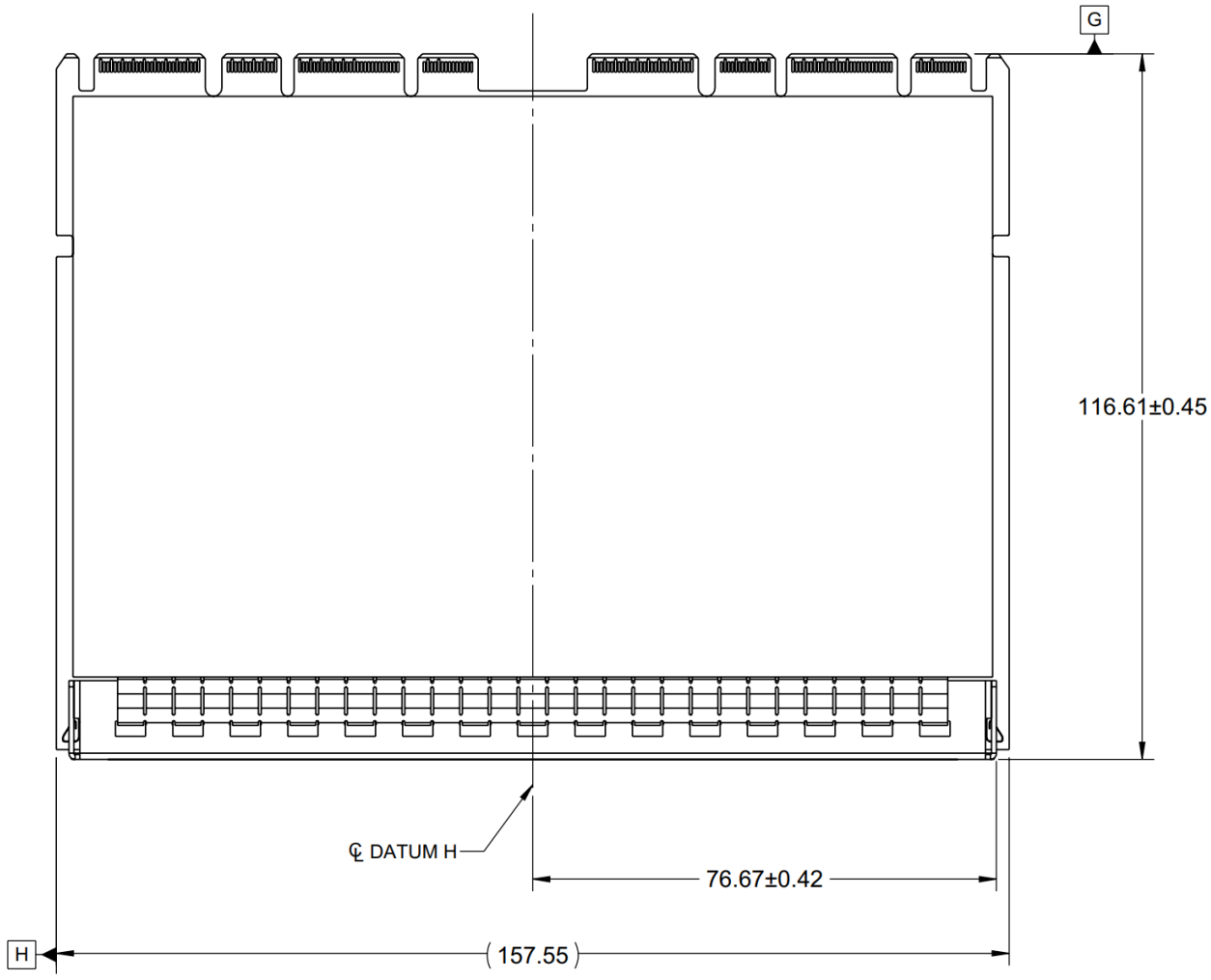


Figure 74: DSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Front View)

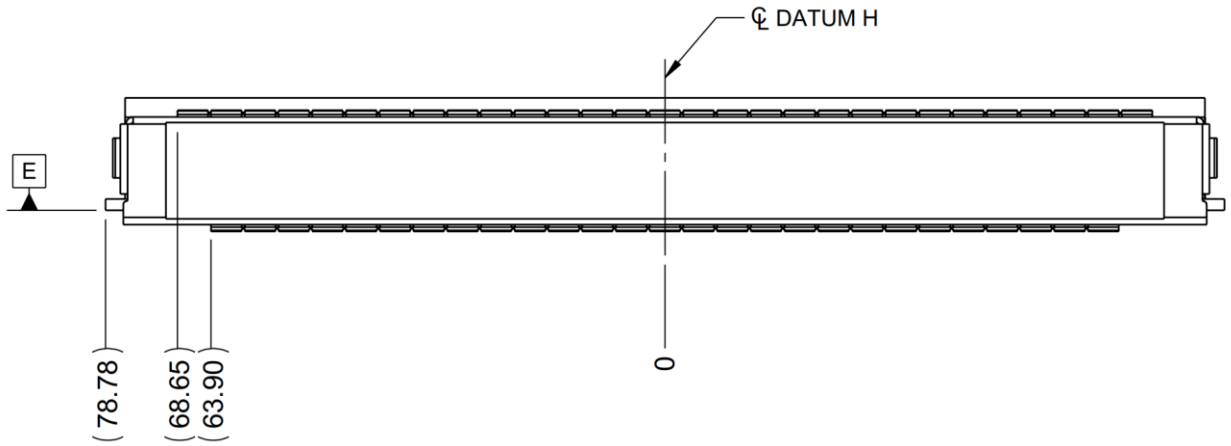


Figure 75: DSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View)



2.8.5 TDSFF CTF Dimensions

2.8.5.1 TDSFF Internal Lock CTF Dimensions

The TDSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding DSFF drawing for the remaining dimensions. The CTF default tolerances are shown in Section 2.8.1.

Figure 76: TDSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View)



2.9 Labeling Requirements

OCP NIC 3.0 cards shall implement all (or a subset of) label items listed below as required by each customer. All labels shall be placed on the exposed face of the insulator or backing plate and within their designated zones. All labels shall be placed within the insulator edge and insulator bend lines to prevent labels from peeling or interfering with the faceplate, chassis card guides and card gold finger edge.

The insulator or backing plate shall be divided into three different zones:

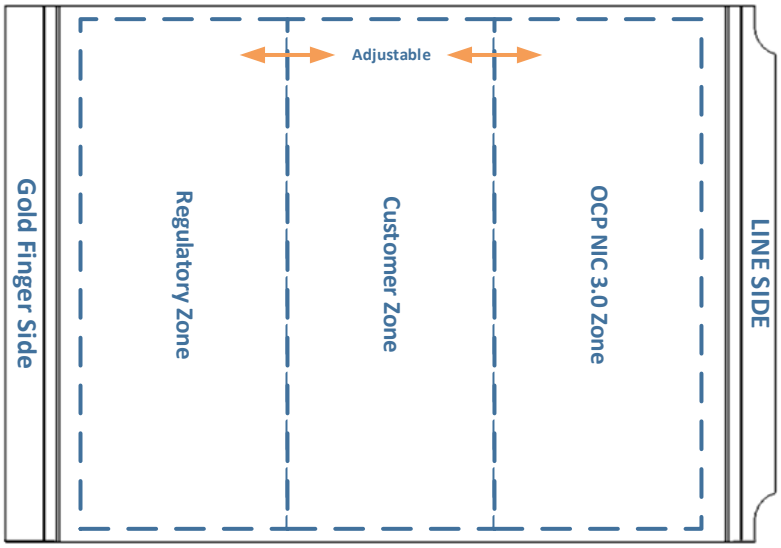
- **Regulatory Zone** – Used for all regulatory markings and filing numbers
- **Customer Zone** – Used for manufacturer markings or any ODM specific labels
- **OCP NIC 3.0 Zone** – Used for MAC addresses, part number labels and optionally the board serial number label if there are no manufacturer requirements to place it on the primary side

Notes:

- Some NIC vendor(s) may require serial number labels to be placed on the primary side of the PBA. This is permitted but it is up to the NIC vendor(s) to find the appropriate location(s) to affix the label. If a label is to be adhered to the PCB, then the label must be ESD safe as defined by ANSI/ESD S541-2008 (between 10^4 Ω and 10^{11} Ω).
- Regulatory marks may be printed on the insulator or affixed via a label
- Each zone size shall be adjustable to accommodate each vendor's labeling requirements
- All labels shall be oriented and readable in the same direction. The readable direction should be with the line side I/O interfaces facing "up"
- Additional labels may be placed on the primary side or on the PCB itself. This is up to the NIC vendor(s) to find the appropriate location(s)

Figure 77 shows an example label area for the SFF. Similar implementations may be used on the LFF and DSFF.

Figure 77: SFF Label Area Example



2.9.1 General Guidelines for Label Contents

Each board shall have a unique label for identification. The label information shall be both in human readable and machine-readable formats (linear or 2D data matrix). The labels may include:

- Serial number
- Part Number
- MAC Address
- Manufacturing Date
- Manufacturing Site Information

Barcode Requirements

- Linear Barcodes
- Code 93, Code 128 Auto or Code 128 Subset B
- Minimum narrow bar width X ≥5 mil (0.127 mm)
- 2D data matrix
- Data matrix shall use ECC200 error correction
- Minimum cell size X ≥10 mil (0.254 mm)
- All linear barcode and data matrix labels shall meet the contrast and print growth requirements per ISO/IEC 16022
- All linear barcode and data matrix labels shall have a quality level C or higher per ISO/IER 15415
- All linear barcode and data matrix labels shall define a minimum Quiet Zone (QZ) to ensure the label is correctly registered by the scanner per ISO/IEC 15415
- Linear barcode labels shall use a QZ that is 10 times the width of the narrowest bar or 1/8th inch, whichever is greater
- Data matrix labels shall have a Quiet Zone (QZ) that is at least one module (in the X-dimension) around the perimeter of the data matrix
- Multiple Serial Numbers, MAC address may exist in one 2D data matrix, each separated by a comma

Human Readable Font

- Arial or printer font equivalent
- Minimum 5 point font size. 3 point font is acceptable when using 600 DPI printers
- Text must be easily legible under normal lighting 6-to-8 inches away

The label size and typeface may vary based on each vendor and/or customer's label content and requirements.

2.9.2 MAC Address Labeling Examples

For an OCP NIC 3.0 card with *m* line side interfaces and *n* RBT management interfaces, the MAC address label shall list the MAC addresses in sequential order starting with line side port 1 to port *m* followed by the controller #0 MAC address to controller *n*. For cards that support multi-host configurations, the label shall associate each MAC address with a host number. The examples below show the MAC addresses presented as a single column, for labels with many MAC addresses, the label may also be formatted in multiple columns for greater readability. Labels may optionally use ellipses for the human readable text to individually indicate a range of Port and ME MAC addresses. In all cases, the 2D data matrix shall include all the card assigned MAC addresses.

2.9.2.1 MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller

As an example, the label content of a quad SFP OCP NIC 3.0 card with a single management MAC address shall be constructed to show human readable data per the Label Data column of Table 12. The constructed label is shown in Figure 78. For each human readable line, there is a MAC prefix "Px:" for a line side Port, or "Mex:" for a managed controller instance, followed by the MAC address. The port/controller association for each row is shown in the far-right column.

Table 12: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller

Label Data	MAC Prefix	MAC Address	Association
P1: AA:BB:CC:DD:EE:F0	P1:	AA:BB:CC:DD:EE:F0	Port 1
P2: AA:BB:CC:DD:EE:F1	P2:	AA:BB:CC:DD:EE:F1	Port 2
P3: AA:BB:CC:DD:EE:F2	P3:	AA:BB:CC:DD:EE:F2	Port 3
P4: AA:BB:CC:DD:EE:F3	P4:	AA:BB:CC:DD:EE:F3	Port 4
ME1: AA:BB:CC:DD:EE:F4	ME1:	AA:BB:CC:DD:EE:F4	Controller #0

Figure 78: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller



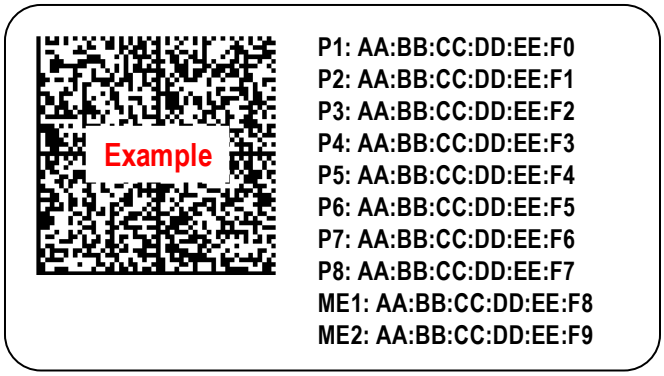
2.9.2.2 MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controllers

As a second example, the label content of an octal port (2xQSFP with "breakout" support) OCP NIC 3.0 card with two managed silicon instances is constructed per Table 13. The constructed label is shown in Figure 79. The MAC address label shall also list the four MAC addresses associated with QSFP lanes [1:4] for QSFP connectors that allow "breakout" modes. The Host-MAC address presentation may also be formatted horizontally for easier readability.

Table 13: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller

Label Data	MAC Prefix	MAC Address	Association
P1: AA:BB:CC:DD:EE:F0	P1:	AA:BB:CC:DD:EE:F0	QSFP1, Port 1
P2: AA:BB:CC:DD:EE:F1	P2:	AA:BB:CC:DD:EE:F1	QSFP1, Port 2
P3: AA:BB:CC:DD:EE:F2	P3:	AA:BB:CC:DD:EE:F2	QSFP1, Port 3
P4: AA:BB:CC:DD:EE:F3	P4:	AA:BB:CC:DD:EE:F3	QSFP1, Port 4
P5: AA:BB:CC:DD:EE:F4	P5:	AA:BB:CC:DD:EE:F4	QSFP2, Port 5
P6: AA:BB:CC:DD:EE:F5	P6:	AA:BB:CC:DD:EE:F5	QSFP2, Port 6
P7: AA:BB:CC:DD:EE:F6	P7:	AA:BB:CC:DD:EE:F6	QSFP2, Port 7
P8: AA:BB:CC:DD:EE:F7	P8:	AA:BB:CC:DD:EE:F7	QSFP2, Port 8
ME1: AA:BB:CC:DD:EE:F8	ME1:	AA:BB:CC:DD:EE:F8	Controller #0
ME2: AA:BB:CC:DD:EE:F9	ME2:	AA:BB:CC:DD:EE:F9	Controller #1

Figure 79: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller



2.9.2.3 MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers

For multi-host implementations, each MAC address shall be prefixed with the host association "H*x*" prior to the port number, where *x* represents the host number. An example of this is shown in Table 14 and Figure 80.

Table 14: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controller

Label Data	Host	MAC Prefix	MAC Address	Association
P1: AA:BB:CC:DD:EE:F0	H1	P1:	AA:BB:CC:DD:EE:F0	Port 1
P2: AA:BB:CC:DD:EE:F1	H1	P2:	AA:BB:CC:DD:EE:F1	Port 2
P3: AA:BB:CC:DD:EE:F2	H2	P3:	AA:BB:CC:DD:EE:F2	Port 3
P4: AA:BB:CC:DD:EE:F3	H2	P4:	AA:BB:CC:DD:EE:F3	Port 4
ME1: AA:BB:CC:DD:EE:F4	n/a	ME1:	AA:BB:CC:DD:EE:F4	Controller #0
ME2: AA:BB:CC:DD:EE:F5	n/a	ME2:	AA:BB:CC:DD:EE:F5	Controller #1

Figure 80: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers



2.9.2.4 MAC Address Label Example 4 – Singe Port with Quad Host, Single Managed Controller

The following example shows a single port device with quad hosts. To conserve space on the MAC address label, this example only shows the MAC addresses for Port 1 through Port 4. The MAC address for each managed host is P*x*+1. This is shown in Table 15 and Figure 81.

Table 15: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller

Label Data	Host	MAC Prefix	MAC Address	Association
P1: AA:BB:CC:DD:EE:F0	H1	P1:	AA:BB:CC:DD:EE:F0	Port 1
ME1: AA:BB:CC:DD:EE:F1	ME1	P1:	AA:BB:CC:DD:EE:F1	Port 1
P2: AA:BB:CC:DD:EE:F2	H2	P1:	AA:BB:CC:DD:EE:F2	Port 1
ME2: AA:BB:CC:DD:EE:F3	ME2	P1:	AA:BB:CC:DD:EE:F3	Port 1
P3: AA:BB:CC:DD:EE:F4	H3	P1:	AA:BB:CC:DD:EE:F4	Port 1
ME3: AA:BB:CC:DD:EE:F5	ME3	P1:	AA:BB:CC:DD:EE:F5	Port 1
P4: AA:BB:CC:DD:EE:F6	H4	P1:	AA:BB:CC:DD:EE:F6	Port 1
ME4: AA:BB:CC:DD:EE:F7	ME4	P1:	AA:BB:CC:DD:EE:F7	Port 1

Figure 81: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller



Table 16: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller

Label Data	MAC Prefix	MAC Address	Association
P1: AA:BB:CC:DD:EE:F0	P1:	AA:BB:CC:DD:EE:F0	Port 1
P8: AA:BB:CC:DD:EE:F7	P8:	AA:BB:CC:DD:EE:F7	Port 8
ME1: AA:BB:CC:DD:EE:F8	ME1:	AA:BB:CC:DD:EE:F8	P1
ME8: AA:BB:CC:DD:EE:FF	ME8:	AA:BB:CC:DD:EE:FF	P8

For labels with a high MAC address count, the use of ellipses in the human readable text to individually indicate a range of Port and Management MAC addresses is permissible. This is shown in Figure 82. In this example, the 2D data matrix shall contain all 16 MAC addresses.

Figure 82: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller



2.10 Mechanical CAD Package Examples

Typical OCP NIC 3.0 implementation examples are included in the 3D CAD package. The purpose of these examples is to demonstrate the implementation feasibility. Additional use cases beyond the implementation examples are possible as long they adhere to the OCP NIC 3.0 specification.

Note: For brevity, references to QSFP+, and QSFP28 shall be referred to as QSFP in this document. Similarly, references to SFP+, and SFP28 shall be referred to as SFP.

The 3D CAD files may be obtained from the OCP NIC 3.0 Wiki:
https://www.opencompute.org/wiki/Server/NIC

3 Mechanical Requirements – Baseboard Side

The baseboard level mechanical requirements specific to the OCP NIC 3.0 slot are discussed in this section. System level requirements are driven by each baseboard vendor and are outside the scope of this specification.

3.1 Baseboard Connector Requirements

The OCP NIC 3.0 baseboard use a 4C+ and 4C connectors as defined in the SFF-TA-1002 specification. Right angle and straddle mount connector options are available depending on the preference of the baseboard vendor implementation, or higher-level specification, such as DC-MHS. All diagram units are in millimeters unless otherwise noted.

> **Note:** The SFF-TA-1002 specification R1.5 defines a Type 1 and Type 2 connector. Type 1 connectors use a discrete pin interface for allowing pins to be repurposed outside of the predefined SFF-TA-1002 GSSGSSG pin configuration. Type 2 connectors designate specific pins for power/control pin sideband and may have some of the defined ground pins bonded together within the connector body.
>
> SFF-TA-1002 Type 1 and Type 2 connectors are both compatible with OCP NIC 3.0 baseboard implementations. Type 2 connectors are best suited for baseboard implementations for PCIe Gen 6 margin improvement. Refer to the SFF-TA-1002 specification for details.

3.1.1 Connector Options

Right-angle and straddle mount connector options are available for baseboard implementations. The same connector type shall be used within platform slots that support multi-connector cards, such as the DSFF.

3.1.1.1 Right-angle Connector

The right-angle connectors are available in the 4C+ and 4C sizes and are shown in Table 17 and Figure 83. They have a 4.05 mm offset from the baseboard surface as shown in Figure 84. Usage of the right-angle connectors does not require a baseboard side cutout for the NIC and allows components to be placed between the motherboard and the secondary side of the NIC. The right-angle connector does not require a specific PCB thickness.

The mating NIC side PCB shall be 1.57 mm (0.062”) ±8.2%. Refer to the SFF-TA-1002 spec for details.

Table 17: Baseboard Right Angle Connector Options

Type	Pins	Style and Baseboard Thickness	NIC PCB Thickness	Offset (mm)
4C+	168 pins	Right Angle	1.57 mm (0.062”)	4.05 mm
4C	140 pins	Right Angle	1.57 mm (0.062”)	4.05 mm

Figure 83: Baseboard 4C+ and 4C Connectors – Right Angle

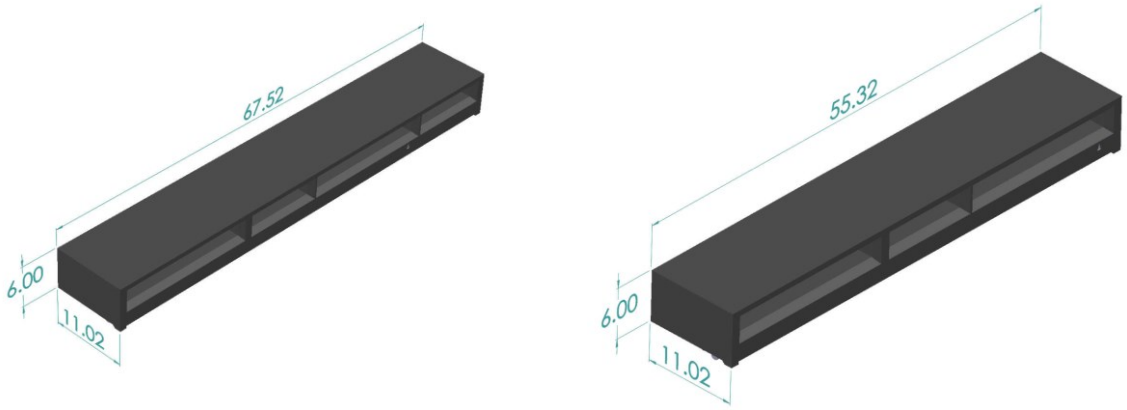
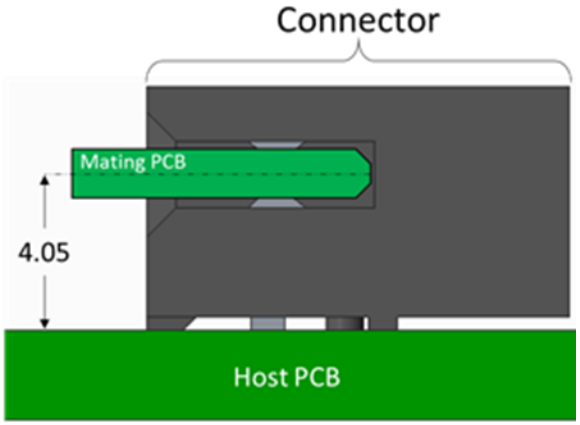


Figure 84: OCP NIC 3.0 Card and Host Offset for Right Angle Connectors



3.1.1.2 Straddle Mount Connector

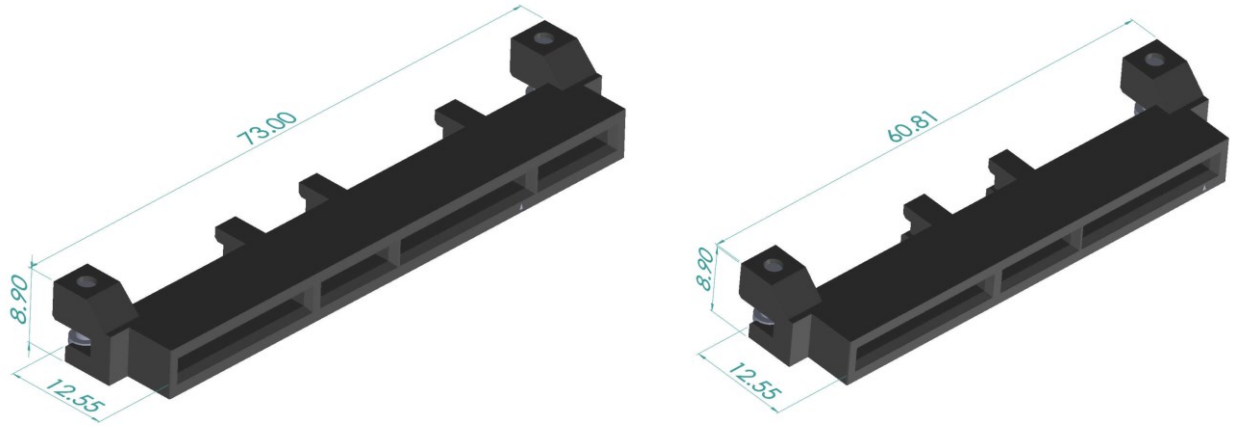
The straddle mount connectors are available in the 4C+ and 4C sizes and are shown in Table 18 and Figure 85. Baseboard thicknesses of 1.57 mm, 1.93 mm and 2.36 mm (0.062'', 0.076'', and 0.093'', respectively) may be used with the corresponding connector. The baseboard PCBs must be controlled to a thickness of ±10%.

The mating NIC side PCB shall be 1.57 mm (0.062") ±8.2% in all cases. Refer to the SFF-TA-1002 spec for details. Usage of the straddle mount connectors require a baseboard side cutout for the NIC.

Table 18: Baseboard Straddle Mount Connector Options

Type	Pins	Style and Baseboard Thickness	NIC PCB Thickness	Offset (mm)
4C+	168 pins	Straddle Mount for 1.57 mm (0.062")	1.57 mm (0.062")	Coplanar (0 mm)
4C+	168 pins	Straddle Mount for 1.93 mm (0.076")	1.57 mm (0.062")	-0.3 mm
4C+	168 pins	Straddle Mount for 2.36 mm (0.093")	1.57 mm (0.062")	Coplanar (0 mm)
4C	140 pins	Straddle Mount for 1.57 mm (0.062")	1.57 mm (0.062")	Coplanar (0 mm)
4C	140 pins	Straddle Mount for 1.93 mm (0.076")	1.57 mm (0.062")	-0.3 mm
4C	140 pins	Straddle Mount for 2.36 mm (0.093")	1.57 mm (0.062")	Coplanar (0 mm)

Figure 85: Baseboard 4C+ and 4C Connectors – Straddle Mount



The straddle mount connectors come in two offset options – a 0 mm offset for the 1.57 mm and 2.36 mm thick baseboards, or with a -0.3 mm offset for a 1.93 mm thick baseboard. The offset is measured from the center line of the baseboard. Both options are shown in Figure 86 and Figure 87.

Figure 86: Straddle Mount Connector with 0 mm Offset (Coplanar) for 1.57 mm and 2.36 mm (0.062” and 0.093”) Thick Baseboards

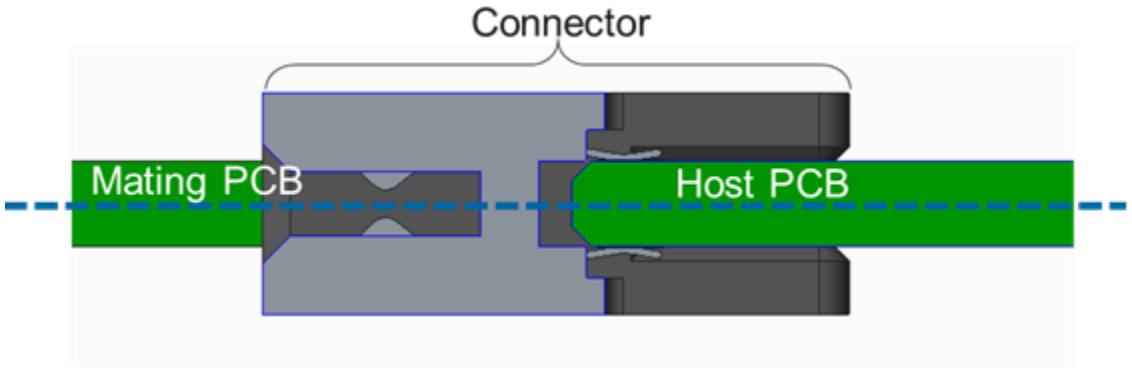
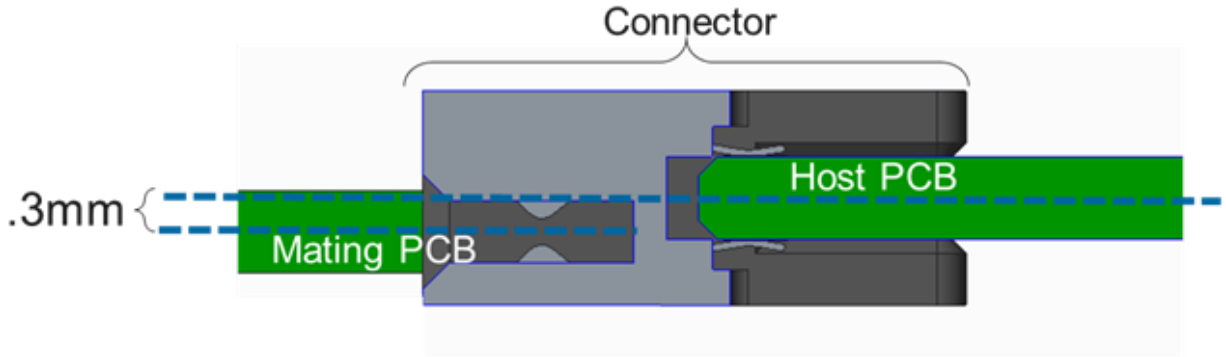


Figure 87: Straddle Mount Connector with -0.3 mm Offset for 1.93 mm (0.076”) Thick Baseboards



3.1.2 Connector Locations

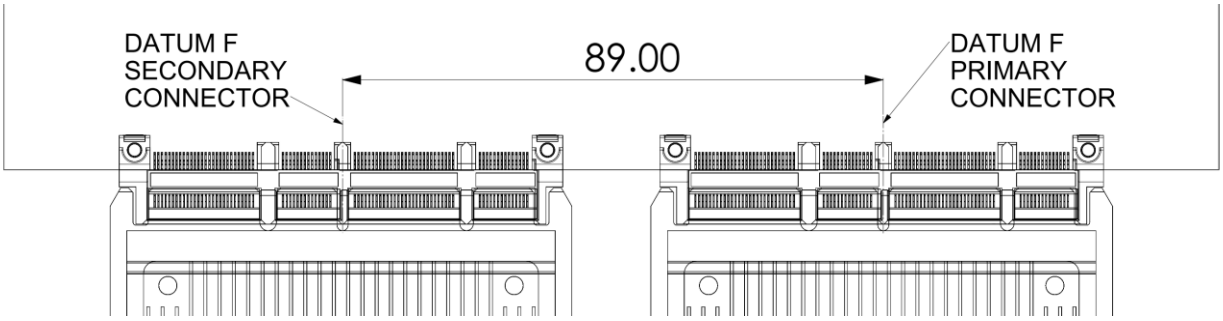
For all implementations, properly positioned baseboard connectors ensure a good mechanical fit. The connector pitch in defined in the following sub-sections. Baseboard implementations shall not mix connector types (right angle or straddle mount) within a DSFF capable slot.

3.1.2.1 SFF Connector Pitch

To support multiple SFF cards, the connector pitch on the baseboard shall not be less than 89 mm as measured from Datum F of each connector as shown in Figure 88. This minimum distance ensures all SFF card faceplate implementations may be used in the baseboard. Datum F is the same for right angle and straddle mount connector options.

Note: The exception to this pitch requirement is for DSFF compatible implementations which has a fixed connector pitch at 81.55 mm. Refer to Section 3.1.2.2.

Figure 88: SFF Connector Pitch for multiple SFF slots

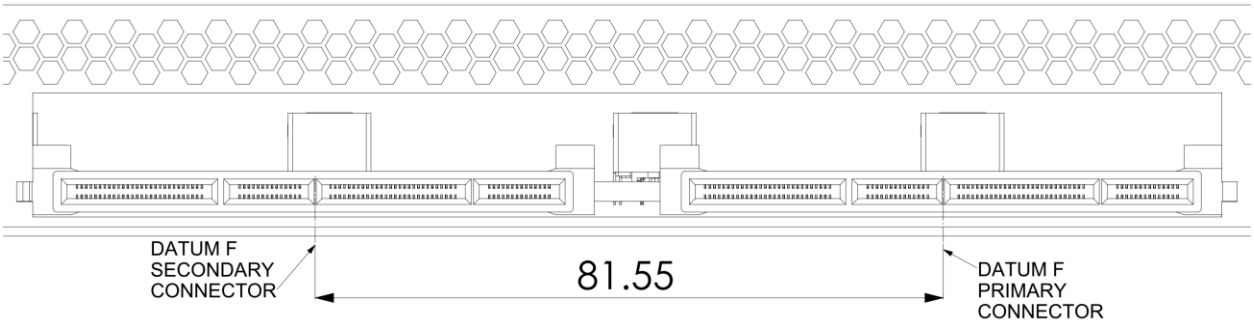


3.1.2.2 DSFF Connector Pitch

To support the DSFF, systems must locate the Primary and Secondary Connectors per the mechanical drawings shown in Figure 89. This view shows the connector orientation when looking “into” the slot from the chassis faceplate. The Primary Connector is located on the right. The Secondary Connector is located on the left. The Secondary Connector is a repurposed Primary Slot when used in the DSFF use case. The connector pitch is 81.55 mm as measured from Datum F of each connector. Datum F is the same for right angle and straddle mount connector options.

Baseboard vendors may optionally implement a DSFF slot with only with the Primary Connector populated for reduced PCIe lane and power envelope support. A single Primary Connector implementation is limited to 80W of delivered power. Usage of the ID Mode Power State is mandatory to ensure the inserted OCP NIC stays within this envelope. In such use cases, system level shock and vibration testing shall be conducted to ensure no damage is incurred to the NIC level components.

Figure 89: DSFF Connector Pitch



3.2 Baseboard Keep Out Zones

Refer to the 3D CAD files for the baseboard keep out zones. The 3D CAD files are available for download on the OCP NIC 3.0 Wiki: https://www.opencompute.org/wiki/Server/NIC

3.3 Baseboard Critical-to-Function (CTF) Requirements

3.3.1 CTF Tolerances

The CTF tolerances shown in Table 19 are used in this section and are applicable for all supported OCP NIC 3.0 slots and heights.

Table 19: CTF Default Tolerances

CTF DEFAULT TOLERANCES	
DIMENSION RANGE	TOLERANCE
	TWO PLACE DECIMALS: X.XX
LINEAR:	± 0.30
ANGULAR:	± 1.00 DEGREES
HOLE DIAMETER:	± 0.13

3.3.2 SFF Baseboard CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF baseboard chassis. The CTF default tolerances are shown in Section 3.3.1.

Note: The SFF baseboard CTF dimensions are applicable to both the right angle and straddle mount connector configurations. The faceplate opening relative to the baseboard changes due to the connector vertical offset, but all CTF dimensions remain identical.

Figure 90: SFF Baseboard Chassis CTF Dimensions (Rear View)

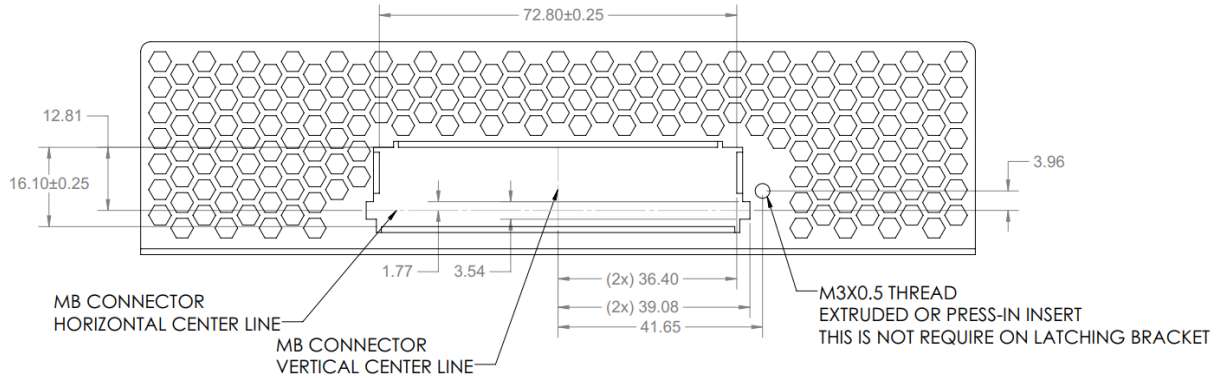


Figure 91: SFF Baseboard Chassis to Card Thumb Screw CTF Dimensions (Side View)

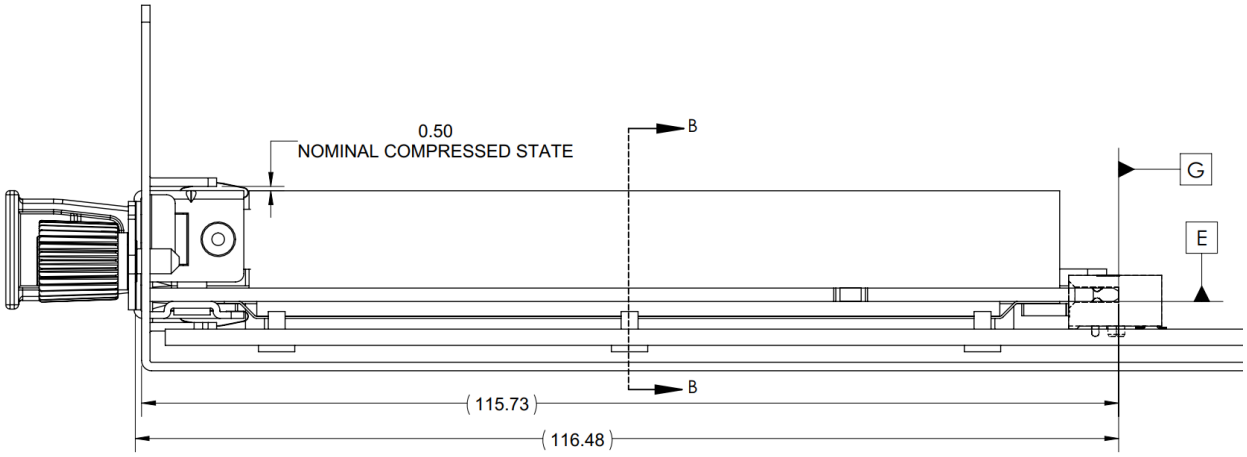


Figure 92: SFF Baseboard Chassis to Ejector lever Card CTF Dimensions (Side View)

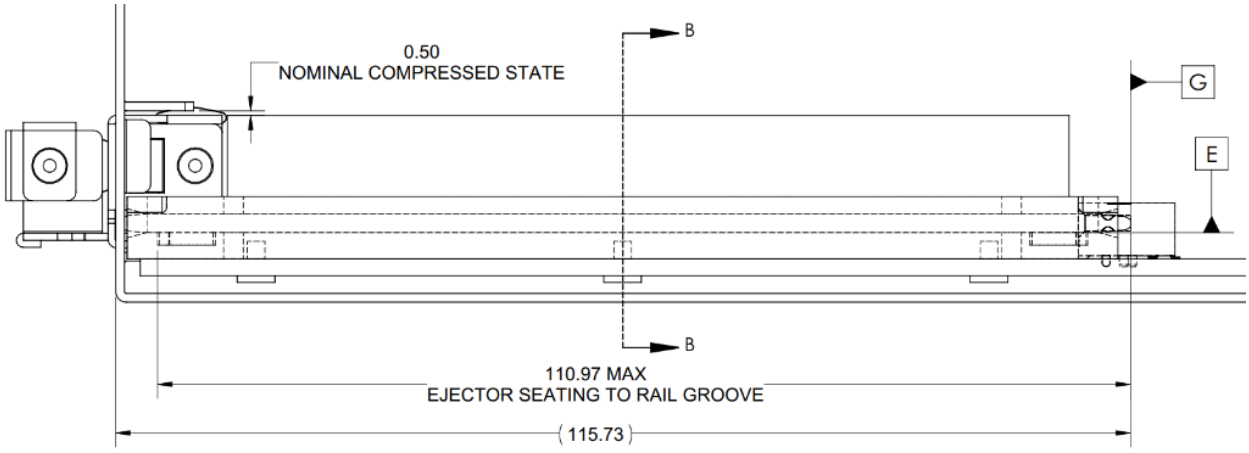
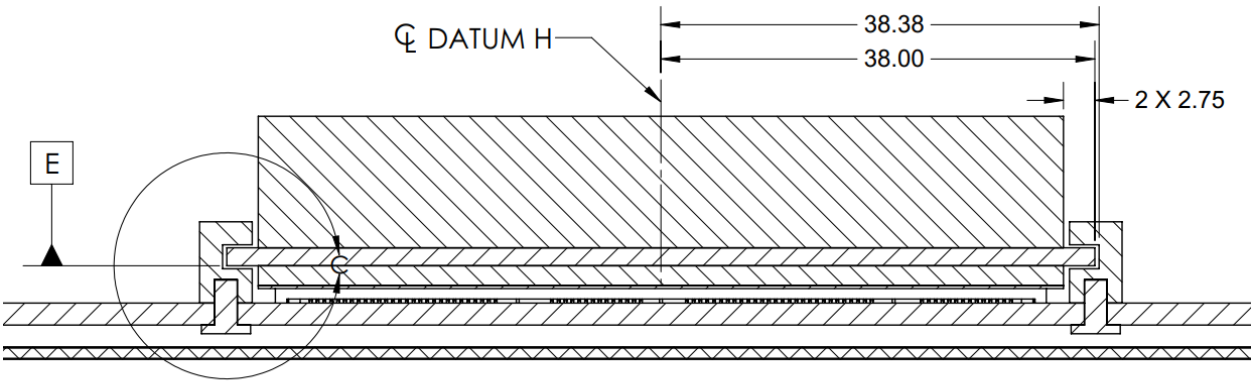
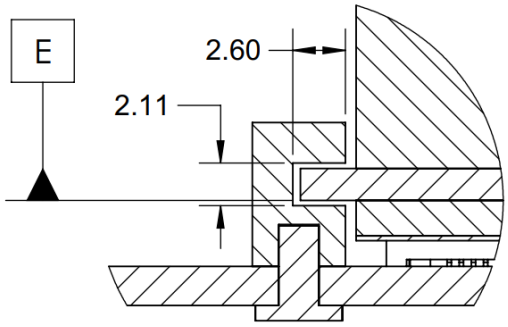


Figure 93: SFF Baseboard Chassis CTF Dimensions (Rear Guide Rail View)



SECTION B-B

Figure 94: SFF Baseboard Chassis CTF Dimensions (Guide Rail Detail) – Detail C



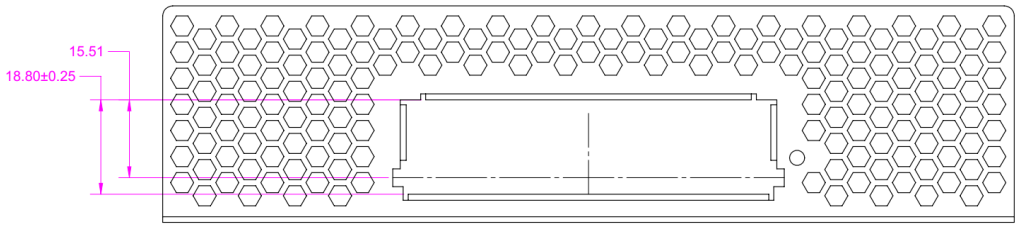
DETAIL C

The right angle and straddle mount card guides are identical between the SFF, DSFF and LFF cards. The card guide model is included in the 3D CAD packages and may be downloaded from the OCP NIC 3.0 Wiki site: https://www.opencompute.org/wiki/Server/NIC.

3.3.3 TSFF Baseboard CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

Figure 95: TSFF Baseboard Chassis CTF Dimensions (Rear View)



3.3.4 DSFF Baseboard CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each DSFF baseboard chassis. The CTF default tolerances are shown in Section 3.3.1.

Note: The SFF baseboard CTF dimensions are applicable to both the right angle and straddle mount connector configurations. The faceplate opening relative to the baseboard changes due to the connector vertical offset, but all CTF dimensions remain identical.

Figure 96: DSFF Baseboard Chassis CTF Dimensions (Rear View)

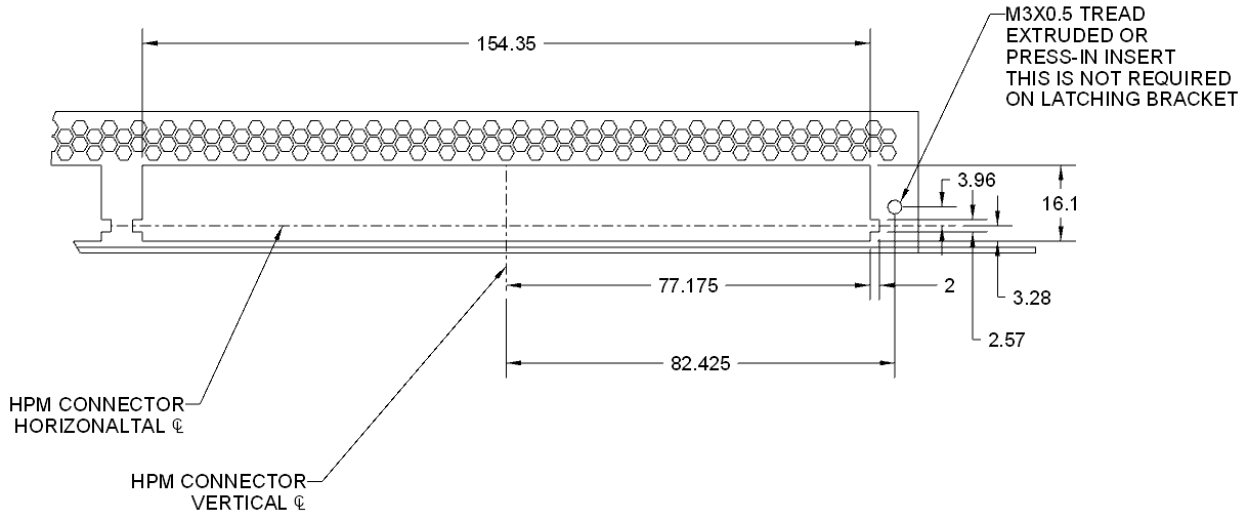


Figure 97: DSFF Baseboard Chassis CTF Dimensions (Rear Rail Guide View)

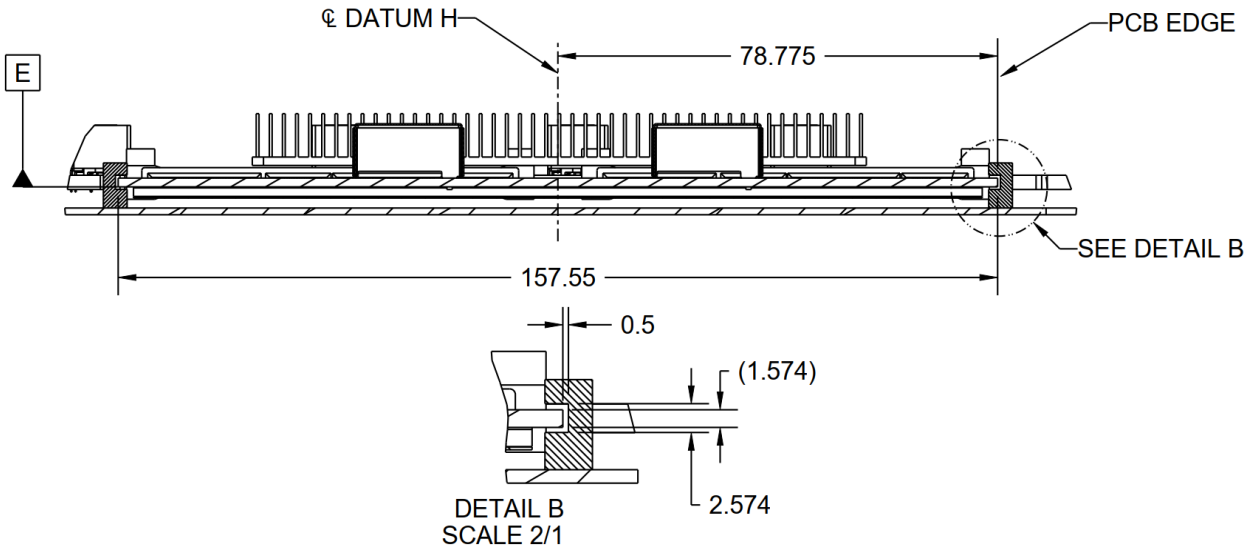
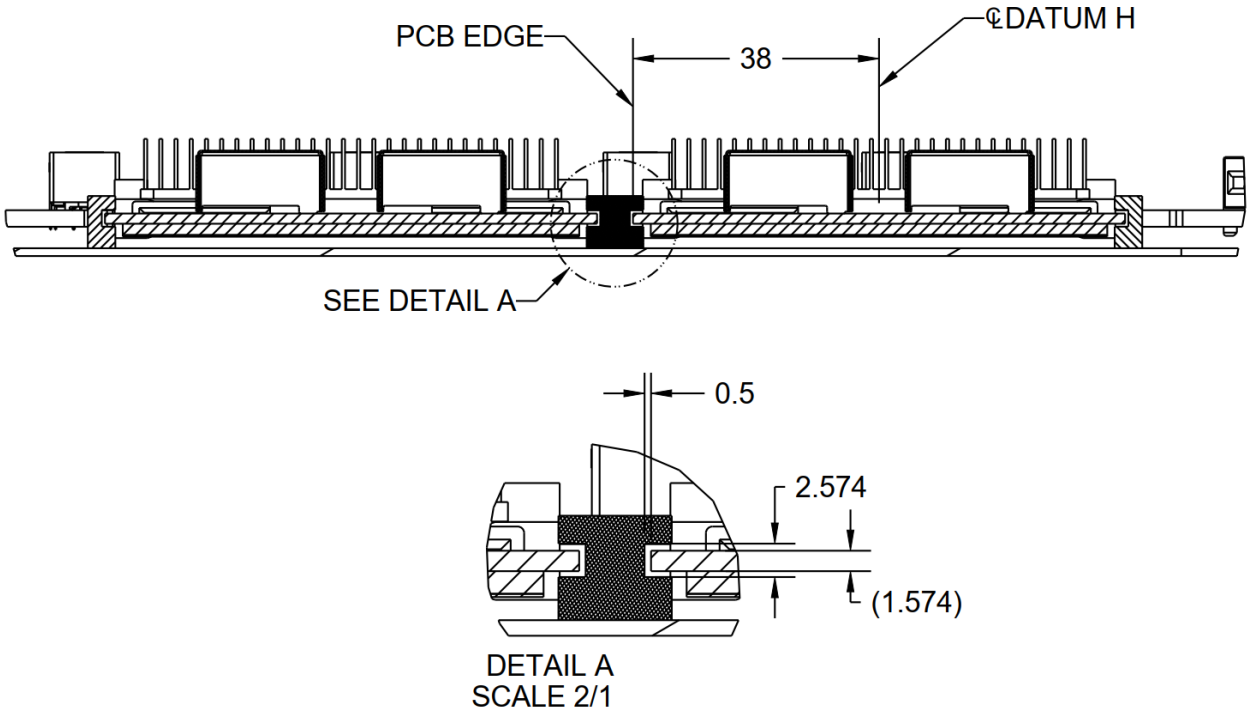


Figure 98: 2xSFF in DSFF Baseboard Chassis CTF Dimensions (Rear Rail Guide View)

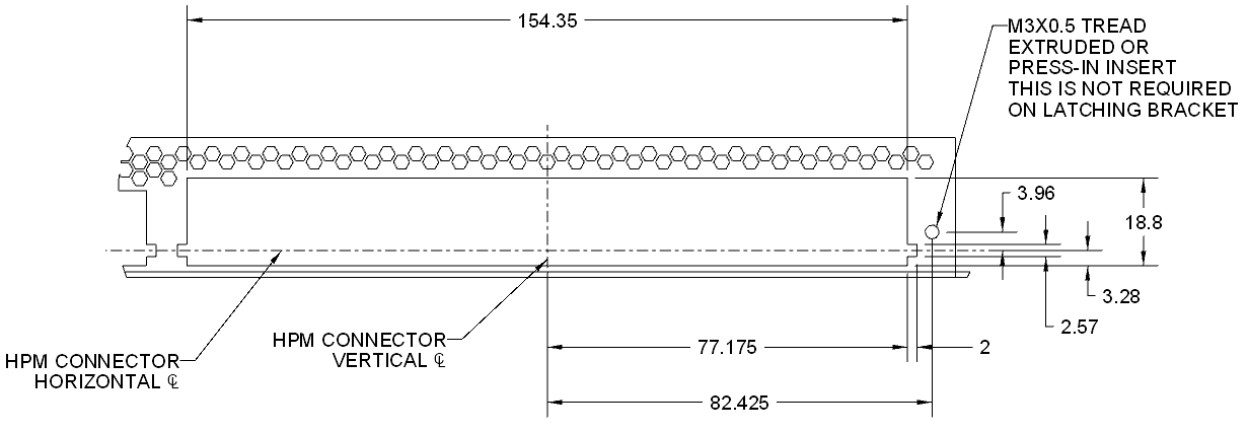


The right angle and straddle mount card guides are identical between the SFF, DSFF and LFF cards. The card guide model is included in the 3D CAD packages and may be downloaded from the OCP NIC 3.0 Wiki site: https://www.opencompute.org/wiki/Server/NIC.

3.3.5 TDSFF Baseboard CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each TDSFF baseboard chassis. The CTF default tolerances are shown in Section 3.3.1.

Figure 99: TDSFF Baseboard Chassis CTF Dimensions (Rear View)



3.4 Card Guides

The card guide models are included in the 3D CAD packages and may be downloaded from the OCP NIC 3.0 Wiki site: https://www.opencompute.org/wiki/Server/NIC.

For the DSFF and TDSFF implementations, the center guide rail is removable. It is up to the system designers to implement and must not violate the mechanical keep out zones and CTF dimensions.

4 Electrical Interface Definition

4.1 Electrical Overview

This specification defines the electrical interface between the baseboard and the OCP NIC 3.0 card. Each card may implement a Primary Connector or Primary and a Secondary Connector. Cards using only the Primary Connector support up to 16 lanes of PCIe. Cards with the Primary Connector and the Secondary Connector allows for DSFF implementations with support for up to 32 lanes of PCIe.

4.1.1 Primary Connector

The Primary Connector provides OCP specific management functions as well as up to 16 lanes of PCIe between the OCP NIC and the system motherboard. The Primary Connector is on all OCP NIC 3.0 card form-factors. For multi-connector implementations, the Primary Connector is located on the right-hand side when looking into the baseboard slot. The Primary Connector is a 4C+ as defined in SFF-TA-1002 and consists of an OCP Bay for management and sideband signals, and a 4C region.

4.1.2 Secondary Connector

The Secondary Connector provides an additional 16 lanes of PCIe and their respective control signals. The Secondary Connector is located on the left-hand side when looking into the baseboard slot. For a DSFF implementation, the secondary connector is a 4C+ and has the same pinout as the Primary Connector.

4.1.3 Connector Features

A 4C+ connector is comprised of a 28pin OCP Bay for management functions, and a 4C section for power, sideband and high speed signaling. The OCP bay is the “+” designation in the connector name.

Management Function Overview (On the OCP Bay of the 4C+ connectors):

- DMTF DSP0222 compliant Network Controller Sideband Interface (NC-SI) RMII Based Transport (RBT) Physical Interface with support for hardware arbitration
- Power management and status reporting
  - Power state change control pins
  - NIC main power enable
  - NIC power good status
- Scan Chain (Control / status serial bus)
  - Port LED Link/Activity
  - Environmental temperature indicators
- Host-to-NIC configuration information
- Additional multi-host PCIe support signals for quad host capable cards (additional 2x PCIe resets, 2x reference clocks)
  - The OCP bay provides PERST2#, PERST3#, REFCLK2 and REFCLK3. This enables support for up to four hosts when used in conjunction with PERST0#, PERST1#, REFCLK0 and REFCLK1 in the Primary 4C region
- PCIe WAKE# signal

Refer to Section 4.2 for a complete list of pin and function descriptions for the OCP Bay portion of the Primary Connector. The OCP Bay pins are prefixed with “OCP_” in the pin location column.

Interface Overview (4C region per connector):

- 16x differential transmit/receive pairs
  - Up to PCIe Gen 5 (32 GT/s) support
- 2x 100 MHz differential reference clocks (REFCLK0 and REFCLK1)
- Control signals
  - 2x PCIe Resets (PERST0# and PERST1#)
  - Link bifurcation control pins
  - Power Brake for emergency power reduction
  - PRSNT identification
  - Aux power enable
- SMBus 2.0
- USB 2.0 interface
- Power
  - +12V_EDGE
  - +3.3V_EDGE

See Section 4.2 for a complete list of pin and function descriptions for the 4C+ connector.

4.2 Pinout Definition

The OCP NIC 3.0 card pinouts are shown in the sections below. All signal directions are specified from the baseboard perspective.

A baseboard system may provide a combination of Primary Connectors only for supporting SFF, or Primary and Secondary Connectors for supporting the DSFF. Both connectors share common functionality with power, SMBus 2.0, 16-lanes of PCIe and bifurcation control.

The Primary Connector 4C+ definition includes the OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI over RBT connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it. Depending on the baseboard form factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The DSFF uses a 4C+ Secondary Connector. Its pinout is identical to that of the Primary Connector. The pinout for busses, like PCIe, are the same, but the numbering indexes have been appropriately incremented to uniquely identify the pin.

The Primary and Secondary Connector pin descriptions are shown in Section 4.5. The OCP Bay pins on the 4C+ connectors are explicitly called out with the “OCP_” prefix in the pin location column.

Cards that do not require the use of a PCIe x16 connection may optionally implement a subset of electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Section 2 for mechanical details.

The physical baseboard connectors must be implemented with the appropriate targeted Primary and Secondary connectors.

4.2.1 SFF Pinout

For the SFF, the baseboard shall implement a 4C+ connector. The card side implementation supports up to 16 PCIe lanes. Cards may implement less than the full set of PCIe lanes (e.g. with a 2C+ style of gold finger). The pinout is shown below. Refer to Section 4.5 for signal description details.

Table 20: SFF Pin Definition (x16)

Primary Connector (4C+)			
Side B		Side A	
OCP_B1	NIC_PWR_GOOD0	PERST2#	OCP_A1
OCP_B2	MAIN_PWR_EN0	PERST3#	OCP_A2
OCP_B3	SCAN0_LD#	WAKE0#	OCP_A3
OCP_B4	SCAN0_DATA_IN	RBT0_ARB_IN	OCP_A4
OCP_B5	SCAN0_DATA_OUT	RBT0_ARB_OUT	OCP_A5
OCP_B6	SCAN0_CLK	SLOT_ID1	OCP_A6
OCP_B7	SLOT_ID0	FLEXIO_0_3	OCP_A7
OCP_B8	FLEXIO_0_2	FLEXIO_0_5	OCP_A8
OCP_B9	FLEXIO_0_1	FLEXIO_0_4	OCP_A9
OCP_B10	GND	GND	OCP_A10
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11
OCP_B12	REFCLKp2	REFCLKp3	OCP_A12
OCP_B13	GND	GND	OCP_A13
OCP_B14	FLEXIO_0_0	RBT0_CLK_IN	OCP_A14
Mechanical Key			
B1	+12V_EDGE	GND	A1
B2	+12V_EDGE	GND	A2
B3	+12V_EDGE	GND	A3
B4	+12V_EDGE	GND	A4
B5	+12V_EDGE	GND	A5
B6	+12V_EDGE	GND	A6
B7	BIF0#	SMCLK0	A7
B8	BIF1#	SMDAT0	A8
B9	BIF2#	SMRST0#	A9
B10	PERST0#	PRSNTA0#	A10
B11	+3.3V_EDGE	PERST1#	A11
B12	AUX_PWR_EN0	PRSNTB2#	A12
B13	GND	GND	A13
B14	REFCLKn0	REFCLKn1	A14
B15	REFCLKp0	REFCLKp1	A15
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28
Mechanical Key			
B29	GND	GND	A29
B30	PETn4	PERn4	A30
B31	PETp4	PERp4	A31
B32	GND	GND	A32
B33	PETn5	PERn5	A33
B34	PETp5	PERp5	A34
B35	GND	GND	A35
B36	PETn6	PERn6	A36
B37	PETp6	PERp6	A37
B38	GND	GND	A38
B39	PETn7	PERn7	A39
B40	PETp7	PERp7	A40
B41	GND	GND	A41
B42	PRSNTB0#	PRSNTB1#	A42
Mechanical Key			

Primary Connector (4C+)			
Side B		Side A	
B43	GND	GND	A43
B44	PETn8	PERn8	A44
B45	PETp8	PERp8	A45
B46	GND	GND	A46
B47	PETn9	PERn9	A47
B48	PETp9	PERp9	A48
B49	GND	GND	A49
B50	PETn10	PERn10	A50
B51	PETp10	PERp10	A51
B52	GND	GND	A52
B53	PETn11	PERn11	A53
B54	PETp11	PERp11	A54
B55	GND	GND	A55
B56	PETn12	PERn12	A56
B57	PETp12	PERp12	A57
B58	GND	GND	A58
B59	PETn13	PERn13	A59
B60	PETp13	PERp13	A60
B61	GND	GND	A61
B62	PETn14	PERn14	A62
B63	PETp14	PERp14	A63
B64	GND	GND	A64
B65	PETn15	PERn15	A65
B66	PETp15	PERp15	A66
B67	GND	GND	A67
B68	RFU1, N/C	USB_DAT0n	A68
B69	RFU2, N/C	USB_DAT0p	A69
B70	PRSNTB3#	PWRBRK0#	A70

1898
1899

4.2.2 DSFF Pinout

For the DSFF, the baseboard shall implement a 4C+ Primary Connector and 4C+ Secondary Connector. The card side implementation supports up to 32 PCIe lanes. Cards may implement less than the full set of PCIe lanes (e.g. 16 lanes with only a 4C+ gold finger). The pinout is shown below. Refer to Section 4.5 for signal description details.

> **Note:** For DSFF implementations, the Secondary Connector is a second SFF slot repurposed for the DSFF implementation. Refer to Section 2.1.3 for examples. The repurposed SFF slot is physically located to the left (when looking into the chassis faceplate) and has a SLOT_ID incremented by +1.

Table 21: DSFF Pin Definition (x32)

Primary Connector (4C+)			
Side B		Side A	
OCP_B1	NIC_PWR_GOOD0	PERST2#	OCP_A1
OCP_B2	MAIN_PWR_EN0	PERST3#	OCP_A2
OCP_B3	SCAN0_LD#	WAKE0#	OCP_A3
OCP_B4	SCAN0_DATA_IN	RBT0_ARB_IN	OCP_A4
OCP_B5	SCAN0_DATA_OUT	RBT0_ARB_OUT	OCP_A5
OCP_B6	SCAN0_CLK	SLOT_ID1	OCP_A6
OCP_B7	SLOT_ID0	FLEXIO_0_3	OCP_A7
OCP_B8	FLEXIO_0_2	FLEXIO_0_5	OCP_A8
OCP_B9	FLEXIO_0_1	FLEXIO_0_4	OCP_A9
OCP_B10	GND	GND	OCP_A10
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11
OCP_B12	REFCLKp2	REFCLKp3	OCP_A12
OCP_B13	GND	GND	OCP_A13
OCP_B14	FLEXIO_0_0	RBT0_CLK_IN	OCP_A14
Mechanical Key			
B1	+12V_EDGE	GND	A1
B2	+12V_EDGE	GND	A2
B3	+12V_EDGE	GND	A3
B4	+12V_EDGE	GND	A4
B5	+12V_EDGE	GND	A5
B6	+12V_EDGE	GND	A6
B7	BIF0#	SMCLK0	A7
B8	BIF1#	SMDAT0	A8
B9	BIF2#	SMRST0#	A9
B10	PERST0#	PRSNTA0#	A10
B11	+3.3V_EDGE	PERST1#	A11
B12	AUX_PWR_EN0	PRSNTB2#	A12
B13	GND	GND	A13
B14	REFCLKn0	REFCLKn1	A14
B15	REFCLKp0	REFCLKp1	A15
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28
Mechanical Key			
B29	GND	GND	A29
B30	PETn4	PERn4	A30
B31	PETp4	PERp4	A31
B32	GND	GND	A32
B33	PETn5	PERn5	A33
B34	PETp5	PERp5	A34
B35	GND	GND	A35

Secondary Connector (4C+)			
Side B		Side A	
OCP_B1	NIC_PWR_GOOD1	PERST6#	OCP_A1
OCP_B2	MAIN_PWR_EN1	PERST7#	OCP_A2
OCP_B3	SCAN1_LD#	WAKE1#	OCP_A3
OCP_B4	SCAN1_DATA_IN	RBT1_ARB_IN	OCP_A4
OCP_B5	SCAN1_DATA_OUT	RBT1_ARB_OUT	OCP_A5
OCP_B6	SCAN1_CLK	SLOT_ID3	OCP_A6
OCP_B7	SLOT_ID2	FLEXIO_1_3	OCP_A7
OCP_B8	FLEXIO_1_2	FLEXIO_1_5	OCP_A8
OCP_B9	FLEXIO_1_1	FLEXIO_1_4	OCP_A9
OCP_B10	GND	GND	OCP_A10
OCP_B11	REFCLKn6	REFCLKn7	OCP_A11
OCP_B12	REFCLKp6	REFCLKp7	OCP_A12
OCP_B13	GND	GND	OCP_A13
OCP_B14	FLEXIO_1_0	RBT1_CLK_IN	OCP_A14
Mechanical Key			
B1	+12V_EDGE	GND	A1
B2	+12V_EDGE	GND	A2
B3	+12V_EDGE	GND	A3
B4	+12V_EDGE	GND	A4
B5	+12V_EDGE	GND	A5
B6	+12V_EDGE	GND	A6
B7	BIF3#	SMCLK1	A7
B8	BIF4#	SMDAT1	A8
B9	BIF5#	SMRST1#	A9
B10	PERST4#	PRSNTA1#	A10
B11	+3.3V_EDGE	PERST5#	A11
B12	AUX_PWR_EN1	PRSNTB6#	A12
B13	GND	GND	A13
B14	REFCLKn4	REFCLKn5	A14
B15	REFCLKp4	REFCLKp5	A15
B16	GND	GND	A16
B17	PETn16	PERn16	A17
B18	PETp16	PERp16	A18
B19	GND	GND	A19
B20	PETn17	PERn17	A20
B21	PETp17	PERp17	A21
B22	GND	GND	A22
B23	PETn18	PERn18	A23
B24	PETp18	PERp18	A24
B25	GND	GND	A25
B26	PETn19	PERn19	A26
B27	PETp19	PERp19	A27
B28	GND	GND	A28
Mechanical Key			
B29	GND	GND	A29
B30	PETn20	PERn20	A30
B31	PETp20	PERp20	A31
B32	GND	GND	A32
B33	PETn21	PERn21	A33
B34	PETp21	PERp21	A34
B35	GND	GND	A35

Primary Connector (4C+)			
Side B		Side A	
B36	PETn6	PERn6	A36
B37	PETp6	PERp6	A37
B38	GND	GND	A38
B39	PETn7	PERn7	A39
B40	PETp7	PERp7	A40
B41	GND	GND	A41
B42	PRSNTB0#	PRSNTB1#	A42
Mechanical Key			
B43	GND	GND	A43
B44	PETn8	PERn8	A44
B45	PETp8	PERp8	A45
B46	GND	GND	A46
B47	PETn9	PERn9	A47
B48	PETp9	PERp9	A48
B49	GND	GND	A49
B50	PETn10	PERn10	A50
B51	PETp10	PERp10	A51
B52	GND	GND	A52
B53	PETn11	PERn11	A53
B54	PETp11	PERp11	A54
B55	GND	GND	A55
B56	PETn12	PERn12	A56
B57	PETp12	PERp12	A57
B58	GND	GND	A58
B59	PETn13	PERn13	A59
B60	PETp13	PERp13	A60
B61	GND	GND	A61
B62	PETn14	PERn14	A62
B63	PETp14	PERp14	A63
B64	GND	GND	A64
B65	PETn15	PERn15	A65
B66	PETp15	PERp15	A66
B67	GND	GND	A67
B68	RFU1, N/C	USB_DAT0n	A68
B69	RFU2, N/C	USB_DAT0p	A69
B70	PRSNTB3#	PWRBRK0#	A70

Secondary Connector (4C+)			
Side B		Side A	
B36	PETn22	PERn22	A36
B37	PETp22	PERp22	A37
B38	GND	GND	A38
B39	PETn23	PERn23	A39
B40	PETp23	PERp23	A40
B41	GND	GND	A41
B42	PRSNTB4#	PRSNTB5#	A42
Mechanical Key			
B43	GND	GND	A43
B44	PETn24	PERn24	A44
B45	PETp24	PERp24	A45
B46	GND	GND	A46
B47	PETn25	PERn25	A47
B48	PETp25	PERp25	A48
B49	GND	GND	A49
B50	PETn26	PERn26	A50
B51	PETp26	PERp26	A51
B52	GND	GND	A52
B53	PETn27	PERn27	A53
B54	PETp27	PERp27	A54
B55	GND	GND	A55
B56	PETn28	PERn28	A56
B57	PETp28	PERp28	A57
B58	GND	GND	A58
B59	PETn29	PERn29	A59
B60	PETp29	PERp29	A60
B61	GND	GND	A61
B62	PETn30	PERn30	A62
B63	PETp30	PERp30	A63
B64	GND	GND	A64
B65	PETn31	PERn31	A65
B66	PETp31	PERp31	A66
B67	GND	GND	A67
B68	RFU3, N/C	USB_DAT1n	A68
B69	RFU4, N/C	USB_DAT1p	A69
B70	PRSNTB7#	PWRBRK1#	A70

4.3 DSFF Architectures

The DSFF form factor was introduced in version 1.4.5 of this specification. The DSFF allows for a compatible baseboard to repurpose two adjacent SFF slots as a single DSFF slot by removing the baseboard card guide rail. The initial targets for this are the OCP M-FLW and M-SDNO form-factors and may be adopted for other vendor specific applications. The DSFF mechanical overview is covered in Section 2.

Note: The DSFF connector pitch is less than two “normal” SFF slots. At a baseboard level, this precludes the use of thumbscrew retention mechanisms.

Electrically, the DSFF card is treated as a single monolithic card with additional board area. The card implements a single +12V_EDGE power domain. Baseboards shall simultaneously enable +12V_EDGE to both connectors when a DSFF is detected in the system. Like the SFF, one or more silicon devices are permitted to exist the NIC design. Only one FRU EEPROM shall be implemented on the PCB and accessible from the Primary Connector as this is one physical field replaceable unit. The Extended OEM Record details out the card specific requirements. Refer to the Section 5.10.3.4.

An example DSFF card with a single silicon instance is illustrated in Figure 100. Similarly, a dual silicon implementation is illustrated in Figure 101. This implementation has a single power domain for all the

board components. There may be one or more network controllers in the single power domain. The Primary Connector SMBus0 and RBT0 are routed as multi-drop. The Primary Connector Scan Chain0 is shared between all the network controllers. The line side I/O port numbering is sequential per Section 4.8. A single FRU EEPROM is present to declare the entire card characteristics. All these management interfaces are all accessible from the Primary Connector.

Note: Baseboard designers shall provision RBT circuitry to maintain a continuous hardware arbitration loop when two SFF cards, or a single DSFF card is installed in the system. Refer to Section 4.5.4 for signaling details and Figure 108 for an example implementation.

Figure 100: DSFF Architecture With a Single Silicon Device

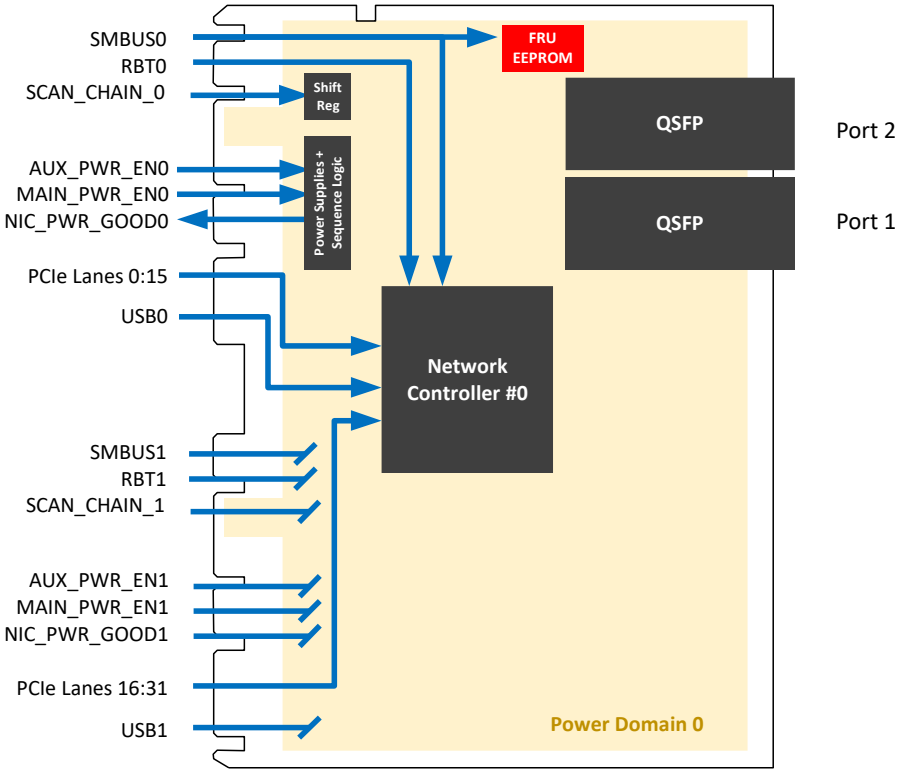
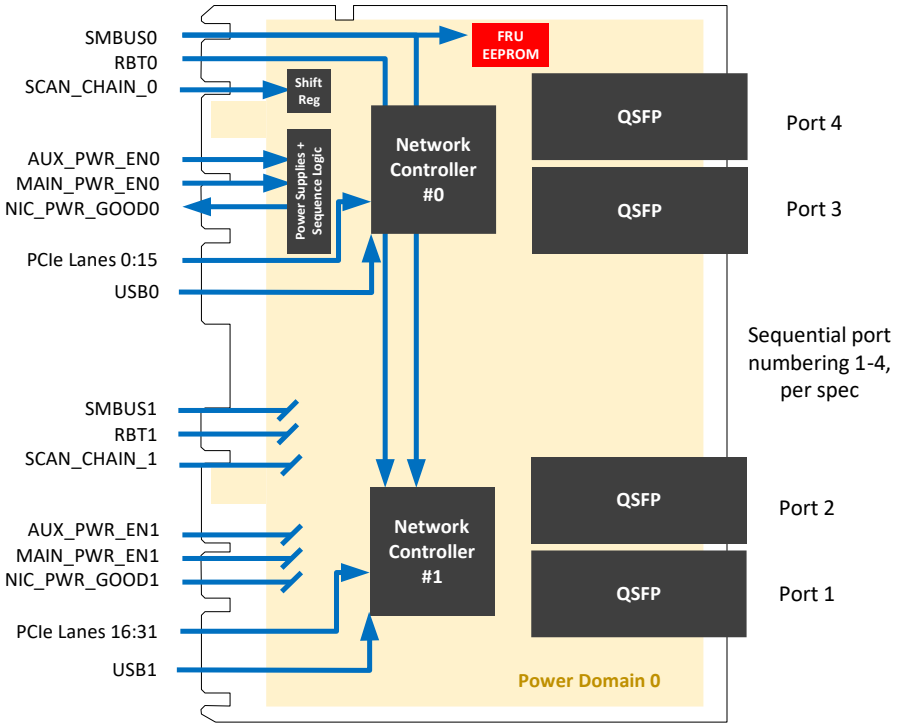


Figure 101: DSFF Architecture With Dual Silicon Devices



Usage of the duplicated sideband signals on the Secondary Connector is optional. The default use case is to use the signals from the Primary Connector. Usage of the duplicated pins on the Secondary Connector is declared in the OEM 0xD2 record. Actual use cases of the duplicated pins are outside the scope of this specification.

For the SFF and LFF cards, the PCIe link topology is declared by the PRSNTA/PRSNTB pins and is a hardcoded table. The PCIe bifurcation mechanism and decoder table as discussed in Section 4.6. This feature remains the same for this version of the specification.

For DSFF detection, the PRSNTB pin encoding shall be PRSNTB[3:0]==0b0010, and PRSNTB[7:4]==0b0010. For DSFF cards that only implement the Primary Connector edge, only PRSNTB[3:0]=0b0010 shall be used. To accommodate more diverse PCIe link topologies, the static configuration table has been moved into the card side 0xD0 and 0xD1 OEM records. The 0xD0 record may control lanes 0-15, or lanes 0-31. This width is declared in 0xD2. Record 0xD1 is only applicable to lanes 16-31 for cards with independent control of their PCIe interfaces. The 0xD0 / 0xD1 usage declarations are identified in the 0xD3 record.

When a DSFF PRSNTB encoding is detected by the baseboard in ID mode, the baseboard queries the 0xD0, 0xD1 and 0xD2 records to determine the supported PCIe link topologies. This information includes: the default PCIe mode, the number of supported modes, the number of supported link subdivisions in each mode, and the associated REFCLK/PERST signaling required from the baseboard. Additionally, the 0xD0 and 0xD1 records also allow DSFF cards to declare if a link is a PCIe endpoint or root port from the NIC perspective.

For clarity, the card edge pin names have been revised for the supported form factors. Any duplicated pins (such as PWRBRK, SMBUS, RBT, REFCLK, PERST, etc) now have a unique pin name to differentiate them from the Primary or Secondary Connector. See Section 4.2 for the respective pin names.

4.4 Line Side I/O Implementations

OCP NIC 3.0 cards support common Ethernet I/O cages. Table 22 shows a few of these implementations. At minimum, the SFF cards were optimized to support 2xQSFP, 4xSFP and 4xRJ45 implementations. The TSFF enabled the use of OSFP-RHS cages. Larger form-factors, like the DSFF and "tall" card variants, have additional faceplate board area to accommodate a larger quantity of I/O connectors, or taller connector options. OCP NIC 3.0 card vendors may implement a subset or superset of connectors to fit the target application.

Table 22: OCP NIC 3.0 Line Side I/O Implementations

Form Factor	Optimized Connector Topology
SFF, TSFF	2x QSFP+/QSFP28/QSFP-DD
SFF, TSFF	4x SFP+/SFP28
SFF, TSFF	4x RJ45
TSFF	1x OSFP-RHS
DSFF	8x SFP
DSFF, TDSFF	4x QSFP+/QSFP28, 2x QSFP-DD
TDSFF	2x OSFP-RHS

Cards are permitted to have additional (non-network related) connectors on the faceplate. The connector keep-in height and maximum protrusions shall be not exceeded. Refer to Section 2.6 for details.

Note: For brevity, references to QSFP+, QSFP28 and QSFP56 shall be referred to as QSFP in this document. Similarly, references to SFP+, SFP28 and SFP56 shall be referred to as SFP. This is also applicable to future connector naming schemes based on speed.

The following specifications may be used to cross reference the associated line side I/O form-factor and module management specifications. This is not an exhaustive list. Refer to Table 3-1 in SFF-8024 – SFF Cross Reference to Industry Products for additional details. Additional combinations and connector types are permissible as I/O form factor technologies and thermal capabilities continue to evolve.

Table 23: Line Side I/O Cross Reference to Industry Standards

Form Factor	Pluggable Form-Factor Specification	Common Management Specification
SFP	INF-8074 (MSA)	SFF-8472
SFP+	SFF-8084	SFF-8472
SFP28	SFF-8402	SFF-8472
OSFP-RHS	OSFP MSA	OSFP management Interface Specification
QSFP	INF-8438 (MSA)	SFF-8636
QSFP+	SFF-8436	SFF-8636
QSFP28	SFF-8665	SFF-8636
QSFP-DD	QSFP-DD MSA	CMIS 5.0

SFP and QSFP cables come in passive and active variants. An active cable contains equalization or optical transceiver components. For cards that support active cables, appropriate thermal considerations shall made per Section 7. A passive direct-attach, and RJ45 cable are purely passive elements with zero thermal contribution.

4.5 Signal Descriptions

The pins shown in this section are common for both the Primary and Secondary Connectors unless otherwise noted. Refer to Section 4.2 to determine the pins applicable to the target board form-factor.

In general, the following rules apply:

- SFF implementations shall follow the 4C+ Primary Connector descriptions.
- DSFF implementations shall follow the 4C+ Primary and 4C+ Secondary Connector descriptions. A total of 8 PERST and 8 REFCLKs are available. The Secondary Connector in this case may be a repurposed SFF Primary Connector slot for the DSFF use-case.
- USB is defined on the 4C+ Connector(s) for SFF/DSFF.

Pins that exist only for the 4C+ Connector OCP Bay are explicitly called out in the pin location column with the prefix “OCP_xxx” and are only applicable to the SFF and DSFF implementations using 4C+ connectors. All pin directions are from the perspective of the baseboard.

For DSFF implementations, the Primary and Secondary connectors are two SFF slots – when these slots are configured as a DSFF, the Secondary Connector is the left SFF slot (when looking into the baseboard SFF slots). Refer to Section 2.1.3 for a visual representation. For nomenclature consistency, the Primary Connector uses PCIe lanes [0:15], PERST[0:3]#, and REFCLK[0:3]. The Secondary Connector uses PCIe lanes [16:31], PERST[4:7]# and REFCLK[4:7]. These are reflected in the signal names in the sections below.

Signal descriptions are grouped by function. Each function contains a pin list and brief description of each pin function. Subsections within each function describe each pin in detail, and if applicable, how it is used on a per form-factor basis. Lastly, an interface example topology diagram is also provided.

Note 1: The OCP NIC 3.0 card shall implement protection methods to prevent leakage or low impedance paths between the V_{AUX} and V_{MAIN} power domains if a powered-down NIC is physically present in a powered-up baseboard. This specification provides example isolation implementations in the signal description text and appropriate figures. OCP NIC 3.0 implementers may choose a different implementation if the isolation requirements are met, and the same results are achieved.

Note 2: The terms Aux Power Mode and Main Power Mode are used within this specification and define the corresponding ACPI power states of the system. Refer to Section 4.5.7 for pin details.

- Aux Power Mode corresponds to the S5 ACPI power state and may also include ACPI power states S3 or S4 depending on the implementation. In Aux Power Mode, AUX_PWR_EN==1, and MAIN_PWR_EN==0.
- Main Power Mode corresponds to the S0 ACPI power state on the system and may also correspond to ACPI power state S1 depending on the implementation. In Main Power Mode, AUX_PWR_EN==1, and MAIN_PWR_EN==1.

4.5.1 PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The PCIe signals have unique names on the Primary and Secondary connector. The Primary Connector uses the REFCLK[0:3], TX/RX[0:15], and PERST[0:3] signal names. The Secondary Connector uses the REFCLK[4:7], TX/RX[16:31] and PERST[4:7] signal names. Where applicable, the Primary/Secondary connector naming convention is shown as a pair. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 5.0. Example connection diagrams for are shown in Section 4.6.

Table 24: Pin Descriptions – PCIe

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
REFCLKn0/REFCLKn4 REFCLKp0/REFCLKp4 REFCLKn1/REFCLKn5 REFCLKp1/REFCLKp5 REFCLKn2/REFCLKn6 REFCLKp2/REFCLKp6 REFCLKn3/REFCLKn7 REFCLKp3/REFCLKp7	B14 B15 A14 A15 OCP_B11 OCP_B12 OCP_A11 OCP_A12	Output	100 MHz PCIe compliant differential reference clocks. Note: The 100 MHz reference clocks are always outputs from the baseboard, regardless of the OCP NIC end point or root port topologies. Note: REFCLK[4:7] are only available on the DSFF.
PETn0 / PETn16 PETp0 / PETp16 PETn1 / PETn17 PETp1 / PETp17 PETn2 / PETn18 PETp2 / PETp18 PETn3 / PETn19 PETp3 / PETp19 PETn4 / PETn20 PETp4 / PETp20 PETn5 / PETn21 PETp5 / PETp21 PETn6 / PETn22 PETp6 / PETp22 PETn7 / PETn23 PETp7 / PETp23 PETn8 / PETn24 PETp8 / PETp24 PETn9 / PETn25 PETp9 / PETp25 PETn10 / PETn26 PETp10 / PETp26 PETn11 / PETn27 PETp11 / PETp27 PETn12 / PETn28 PETp12 / PETp28	B17 B18 B20 B21 B23 B24 B26 B27 B30 B31 B33 B34 B36 B37 B39 B40 B44 B45 B47 B48 B50 B51 B53 B54 B56 B57	Output	PCIe transmitter differential pairs [0:15] (Primary Connector), and differential pairs [16:31] (Secondary Connector). Note: PET[16:31] are only available on the DSFF.

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
PETn13 / PETn29 PETp13 / PETp29 PETn14 / PETn30 PETp14 / PETp30 PETn15 / PETn31 PETp15 / PETp31	B59 B60 B62 B63 B65 B66		
PERn0 / PERn16 PERp0 / PERp16 PERn1 / PERn17 PERp1 / PERp17 PERn2 / PERn18 PERp2 / PERp18 PERn3 / PERn19 PERp3 / PERp19 PERn4 / PERn20 PERp4 / PERp20 PERn5 / PERn21 PERp5 / PERp21 PERn6 / PERn22 PERp6 / PERp22 PERn7 / PERn23 PERp7 / PERp23 PERn8 / PERn24 PERp8 / PERp24 PERn9 / PERn25 PERp9 / PERp25 PERn10 / PERn26 PERp10 / PERp26 PERn11 / PERn27 PERp11 / PERp27 PERn12 / PERn28 PERp12 / PERp28 PERn13 / PERn29 PERp13 / PERp29 PERn14 / PERn30 PERp14 / PERp30 PERn15 / PERn31 PERp15 / PERp31	A17 A18 A20 A21 A23 A24 A26 A27 A30 A31 A33 A34 A36 A37 A39 A40 A44 A45 A47 A48 A50 A51 A53 A54 A56 A57 A59 A60 A62 A63 A65 A66	Input	PCIe receiver differential pairs [0:15] (Primary Connector), and differential pairs [16:31] (Secondary Connector). Note: PER[16:31] are only available on the DSFF.
PERST0# / PERST4# PERST1# / PERST5# PERST2# / PERST6# PERST3# / PERST7#	B10 A11 OCP_A1 OCP_A2	Output	PCIe Reset #[0:7]. Active low. Note: PERST[4:7]# are only available on the DSFF. Note: These signals are typically outputs from the Baseboard. The only exception is for DSFF, where the OCP NIC 3.0 card declares the PERST direction

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
			(in cases of a root port link from the card) in the 0xD0/0xD1 OEM Record(s).
WAKE0# / WAKE1#	OCP_A3	Input, OD	PCIe WAKE#. Open drain. Active low. Note: WAKE1# is only available on the DSFF.
PWRBRK0# / PWRBRK1#	A70	Output, OD	PCIe Power Brake. Open drain. Active low. Note: PWRBRK1# is only available on the DSFF.

4.5.1.1 REFCLK[n/p][0:7]

These pins are the 100 MHz reference clocks are used for the OCP NIC 3.0 card PCIe core logic. The 100 MHz reference clocks are always outputs from the baseboard, regardless of the OCP NIC end point or root port topologies.

REFCLK0 is always available to all OCP NIC 3.0 cards. The card should not assume additional REFCLKs are available until the bifurcation negotiation process is complete.

For baseboards, the REFCLK[0:3] signals shall be available at the Primary Connector for supported designs. For the DSFF, REFCLK[4:7] are available on the Secondary Connector.

- REFCLK0 is required for all OCP NIC 3.0 cards.
- REFCLK[1:3] are required for designs that support 2 x*n*, and 4 x*n* bifurcation implementations in SFF.
- REFCLK[4:7] are required for designs that support bifurcation implementations in a DSFF.

For baseboard implementations that use REFCLK[1:7], the baseboard should disable the appropriate REFCLKs not used by the OCP NIC 3.0 card.

The baseboard shall not advertise the corresponding bifurcation modes if the card requested REFCLKs[1:7] are not implemented.

For OCP NIC 3.0 cards, the required REFCLKs shall be connected per the endpoint datasheet. Unused REFCLKs on the OCP NIC 3.0 card shall be left as no connects.

Note: For SFF cards that only support 1 x16, REFCLK0 is used. For SFF cards that support 2 x8, REFCLK0 is used for the first eight PCIe lanes, and REFCLK1 is used for the second eight PCIe lanes. REFCLK2 and REFCLK3 are only used for cards that only support a four link PCIe bifurcation mode. For DSFF, REFCLK usage definitions are declared in the FRU OEM Record(s) 0xD0/0xD1.

Refer to Section 2.1 in the PCIe CEM Specification, Rev 5.0 for electrical details.

4.5.1.2 PET[n/p][0:31]

The PCIe transmit pins are connected from the baseboard transmitter differential pairs to the receiver differential pairs on the OCP NIC 3.0 card.

The PCIe transmit pins shall be AC coupled on the baseboard with capacitors. The AC coupling capacitor value shall use the C_{TX} parameter value specified in the PCIe Base Specification Rev 5.0 Section 8.3.9.

For baseboards, the PET[0:15] signals are required at the Primary Connector for the SFF slots. PET[0:15] and PET[16:31] are required for the DSFF slots.

For SFF OCP NIC 3.0 cards, the required PET[0:15] signals shall be connected to the endpoint silicon. For silicon that uses less than a x16 connection, the appropriate PET[0:15] signals shall be connected per the endpoint datasheet.

For DSFF implementations, PET[0:15] are assigned to the Primary Connector, and PET[16:31] are assigned to the Secondary Connector.

Unused pins shall be left as a no connect.

Refer to Section 6.1 in the PCIe CEM Specification, Rev 5.0 for details.

4.5.1.3 PER[n/p][0:31]

The PCIe receive pins are connected from the OCP NIC 3.0 card transmitter differential pairs to the receiver differential pairs on the baseboard.

The PCIe receive pins shall be AC coupled on the OCP NIC 3.0 card with capacitors. The AC coupling capacitor value shall use the C_{TX} parameter value specified in the PCIe Base Specification Rev 5.0 Section 8.3.9.

For baseboards, the PER[0:15] signals are required at the Primary Connector for the SFF slots. PER[0:15] and PER[16:31] are required for the DSFF slots.

For SFF OCP NIC 3.0 cards, the required PER[0:15] signals shall be connected to the endpoint silicon. For silicon that uses less than a x16 connection, the appropriate PER[0:15] signals shall be connected per the endpoint datasheet.

For DSFF implementations, PER[0:15] are assigned to the Primary Connector, and PER[16:31] are assigned to the Secondary Connector.

Unused pins shall be left as a no connect.

Refer to Section 6.1 in the PCIe CEM Specification, Rev 5.0 for details.

4.5.1.4 PERST[0:7]#

When PERSTn# is deasserted, the signal shall indicate the power state is already in Main Power Mode and is within tolerance and stable for the OCP NIC 3.0 card to bring up the PCIe link. The default pin direction is an output from the baseboard for SFF. In DSFF, the pin direction is declared in the DSFF PCIe Link Subdivision OEM Record(s) 0xD0/0xD1.

PERST0# is always available to all OCP NIC 3.0 cards. The card should not assume PERST[1:7]# are available until the bifurcation negotiation process is complete.

PERST[0:7]# shall be asserted low on the baseboard until the platform is ready to deassert reset. Deassertion shall occur at least 1s after NIC_PWR_GOOD and the transition to the Main Power Mode state. This ensures the card power rails are within the operating limits and all PCIe REFCLKs become stable. This value is longer than the minimum value specified in the PCIe CEM Specification.

For baseboards that support bifurcation, the PERST[0:3]# signals are required on the Primary Connector, PERST[4:7]# are required on the Secondary Connector.

For OCP NIC 3.0 cards, the required PERST[0:7]# signals shall be connected to the endpoint silicon. Unused PERST[1:7]# signals shall be left as no connects or terminated per the target silicon recommendations.

> **Note:** For cards that only support 1 x16, PERST0# is used. For cards that support 2 x8, PERST0# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes. PERST2# and PERST3# are only used for cards that support a four link PCIe bifurcation mode.
>
> For DSFF, REFCLK usage definitions are declared in the FRU OEM Record 0xD0/0xD1.

For baseboards with unused PERST[1:7]# signals, a 10 kΩ pull down resistor shall be provided by the baseboard for each unused pin.

For baseboard that support DSFF, the PERST signals may be driven by the card. The direction of the PERST signals are defined in the 0xD0 and 0xD1 OEM Records for PCIe Link Subdivision. The baseboard shall parse the OEM Record content and, if necessary, reconfigure the PERST signal direction as requested by the card. The baseboard shall not select incompatible topologies.

Refer to Section 2.2 in the PCIe CEM Specification, Rev 5.0 for details.

4.5.1.5 WAKE[0:1]#

The WAKE[0:1]# signals shall be driven by the OCP NIC 3.0 card to notify the baseboard to restore PCIe link. For OCP NIC 3.0 cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR. For multi-homed host configurations, the WAKE# signal assertion shall wake all nodes.

For baseboards, this signal shall be pulled up to +3.3V_EDGE on the baseboard with a 10 kΩ resistor. This signal shall be connected to the system WAKE# signal.

For OCP NIC 3.0 cards, this signal shall be connected between the endpoint silicon WAKE# pin(s) and the card edge through an isolation buffer. The WAKE# signal shall not assert until the PCIe card is in the D3 state according to the PCIe CEM specification to prevent false WAKE# events. For OCP NIC 3.0, the WAKE# pin shall be buffered or otherwise isolated from the host until the aux voltage source is present. Examples of this are shown in Section 4.6.5 by gating via an on-board “AUX_PWR_GOOD” signal to indicate all the NIC Aux power rails are stable. The PCIe CEM specification also shows an example in the WAKE# signal section.

This pin shall be left as a no connect if WAKE# is not supported by the NIC side silicon device(s).

Refer to Section 2.3 in the PCIe CEM Specification, Rev 5.0 for details.

4.5.1.6 PWRBRK[0:1]#

This signal(s) shall be pulled up to +3.3V_EDGE on the OCP NIC 3.0 card with 95 kΩ or larger resistance. A baseboard that supports this function must provide a stronger pull up on PWRBRK#. A baseboard pull up value between 4.7 kΩ and 10 kΩ is recommended. The pull up shall meet the T_{PWRBRK} timing parameter as shown in the PCIe CEM Specification.

When this signal is driven low by the baseboard, the Emergency Power Reduction State is requested. The OCP NIC 3.0 card shall move to a lower power consumption state.

For baseboards, the PWRBRK0# pin shall be implemented and available on the Primary Connector for the SFF slots. In addition, the PWRBRK1# pin shall be implemented on the Secondary connector for DSFF slots.

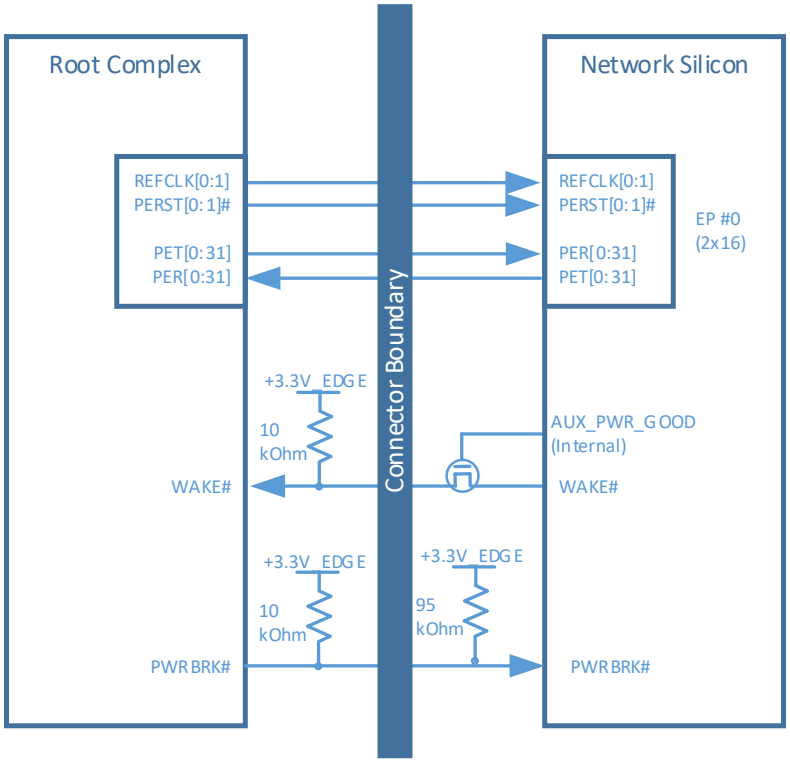
For OCP NIC 3.0 cards, the PWRBRK[0:1]# pin usage is optional. If used, the PWRBRK0# on the Primary Connector should be connected to the network silicon to enable reduced power state. If not used, the PWRBRK0# signal shall be left as a no connect. PWRBRK1# shall be left as a no connect and reserved for a future use case.

> **Note:** The PWRBRK[0:1]# pins are only available for OCP NIC 3.0 cards that implement 4C+ gold finger(s). For cards that implement at 2C+ gold fingers, the respective PWRBRK[0:1]# functionality is not available.

4.5.1.7 PCIe Interface Topology Example

An example PCIe interface topology is shown in Figure 102.

Figure 102: PCIe Interface Topology Example



4.5.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section 4.12. Example connection diagrams are shown in Section 4.5.2.4.

The PRSNTA0#/PRSNTB[3:0]# pins are available on the Primary Connector. PRSNTA1#/PRSNTB[7:4]# are available on the Secondary Connector. The state of these pins shall be used to determine if a card has been physically plugged in. Similarly, the BIF[2:0]# pins are available on the Primary Connector and the BIF[5:3]# pins are available on the Secondary Connector. The BIF# pins signal to the NIC silicon which PCIe mode is expected.

The BIF pins shall be driven by the baseboard along with the rising edge of AUX_PWR_EN. The appropriate BIF[5:0]# pins shall be latched by the OCP NIC 3.0 card when AUX_PWR_EN=1 and NIC_PWR_GOOD=1 to ensure the correct values are detected by the OCP NIC 3.0 card. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section 4.12 for details.

For the SFF, the baseboard shall only read the Primary Connector PRSNTB[3:0]# to determine the card type. For the DSFF, the baseboard shall read both the Primary and Secondary connector PRSNTB[7:0]# pins to determine the card type. The card type matrix is discussed in Section 4.6.

Table 25: Pin Descriptions – PCIe Present and Bifurcation Control Pins

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
PRSNTA0#/PRSNTA1#	A10	Output	Present A[1:0]# are used for OCP NIC 3.0 card presence and PCIe capabilities detection. Note: PRSNTA1# is only available on the DSFF.
PRSNTB0#/PRSNTB4# PRSNTB1#/PRSNTB5# PRSNTB2#/PRSNTB6# PRSNTB3#/PRSNTB7#	B42 A42 A12 B70	Input	Present B [7:0]# are used for OCP NIC 3.0 card presence and PCIe capabilities detection. Note: PRSNTB[4:7]# are only available on the DSFF.
BIF0# / BIF3# BIF1# / BIF4# BIF2# / BIF5#	B7 B8 B9	Output	Bifurcation [5:0]# pins allow the baseboard to force configure the OCP NIC 3.0 card bifurcation. Note: BIF[5:3]# are only available on the DSFF.

4.5.2.1 PRSNTA[1:0]#

For baseboards, this pin shall be directly connected to GND.

For OCP NIC 3.0 SFF, the PRSNTA0# pin shall be directly connected to the respective PRSNTB[3:0]# pins. For the DSFF, the additional PRSNTA1# pin shall be connected to the respective PRSNTB[7:4]# pins.

4.5.2.2 PRSNTB[7:0]#

For baseboards, these pins shall be connected to the I/O hub and pulled up to +3.3V_EDGE using 1 kΩ resistors.

For OCP NIC 3.0 cards, PRSNTB[3:0]# pins shall be strapped to PRSNTA0#, and PRSNTB[7:4]# shall be strapped to PRSNTA1# per the encoding definitions described in Section 4.6. The card side shall implement a series resistor between the PRSNTA and each connected PRSNTB pin in the range of 0 Ω to ~200 Ω to protect the baseboard logic.

When no OCP NIC 3.0 card is installed, the baseboard shall see this value as PRSNTB[3:0]#=0b1111 and, if applicable, PRSNTB[7:4]#=0b1111.

Note: PRSNTB[7,3]# are located at the bottom of the 4C+ connector and is only applicable for OCP NIC 3.0 cards with a PCIe width of x16 (or greater). OCP NIC 3.0 cards that implement a 2C+ card edge do not use the PRSNTB[7,3]# pin(s) for capabilities or present detection.

4.5.2.3 BIF[5:0]#

For baseboards, the BIF[5:0]# pins shall be driven from the baseboard I/O hub on the rising edge of AUX_PWR_EN. This allows the baseboard to force the OCP NIC 3.0 card bifurcation. The baseboard may optionally pull the BIF[5:0]# signals to AUX_PWR_EN or to ground per the definitions described in Section 4.6 if no dynamic bifurcation configuration is required. The BIF[5:0]# pins shall be set to a voltage low (0b000000) until AUX_PWR_EN is asserted. The BIF[5:0]# pins shall remain static after AUX_PWR_EN is asserted. The pins are not allowed to change states when the OCP NIC 3.0 card is powered on.

For baseboards that allow dynamic bifurcation, the BIF[5:0]# pins are driven to a voltage low (0b000000) prior to AUX_PWR_EN. The required state of the BIF[5:0]# pins are driven with the rising edge of AUX_PWR_EN when bifurcation is requested. Refer to Figure 103 for an example configuration.

For baseboards with static bifurcation, the BIF# pins that are intended to be a voltage high level shall be connected to a pull up to AUX_PWR_EN. BIF# pins that are voltage low level may be directly tied to ground. Refer to Figure 104 for an example configuration.

For baseboards that support a DSFF slot, the PRSNTA and PRSNTB pins span across the Primary and Secondary Connectors. Figure 105 shows such an example with controlled BIF[5:0]#.

For OCP NIC 3.0 cards, these signals shall connect to the endpoint bifurcation pins if it is supported. The BIF[5:0]# signals shall be left as no connects if end point bifurcation is not supported. The value of the BIF[5:0]# pins are latched by the OCP NIC 3.0 card upon entering Aux Power Mode (when AUX_PWR_EN=1 and NIC_PWR_GOOD=1).

Note 1: The required output logic for endpoint bifurcation decoding is dependent on the specific silicon and is not defined in this specification. This logic may be implemented within the silicon firmware.

Note 2: BIF[5:0]# encodings shown in the PCIe Bifurcation Decoder show the expected electrical levels of the pins for each bifurcation mode. Refer to Section 4.6.3 for details.

4.5.2.4 PCIe Present and Bifurcation Example Topologies

The following diagrams illustrate SFF and DSFF examples of the PCIe PRSNTA/PRSNTB connections for card present detection and the BIF pins for bifurcation control.

Figure 103: SFF PCIe Present and Bifurcation Pins (Baseboard Controlled BIF[2:0]#)

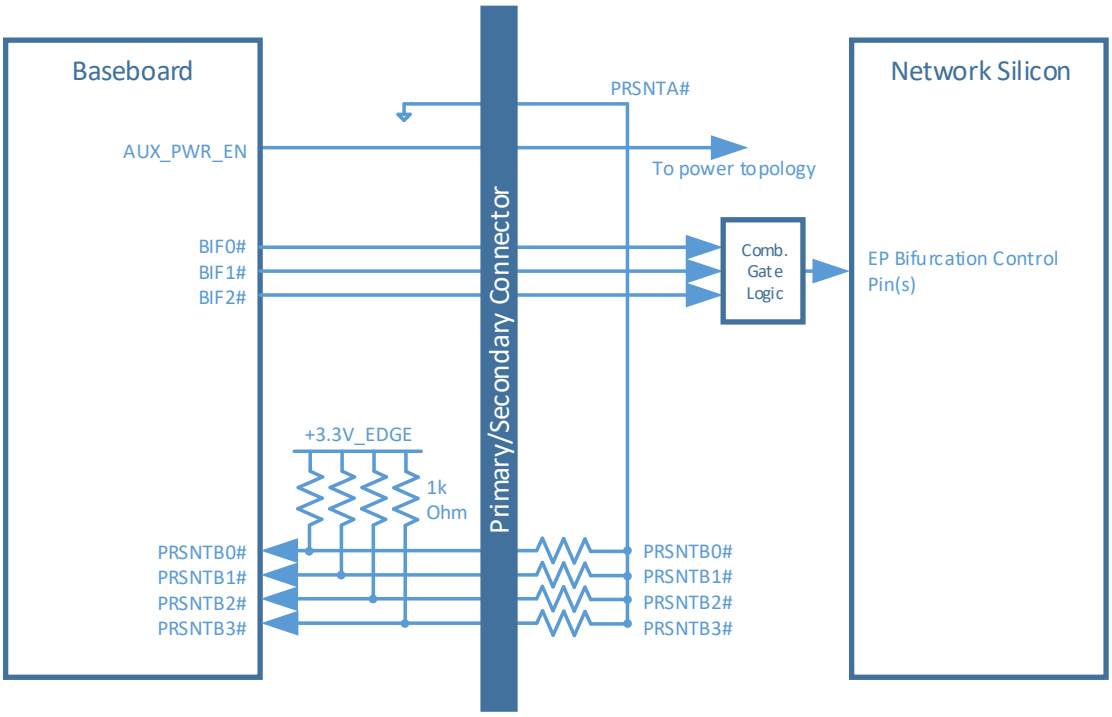


Figure 104: SFF PCIe Present and Bifurcation Pins (Static BIF[2:0]#)

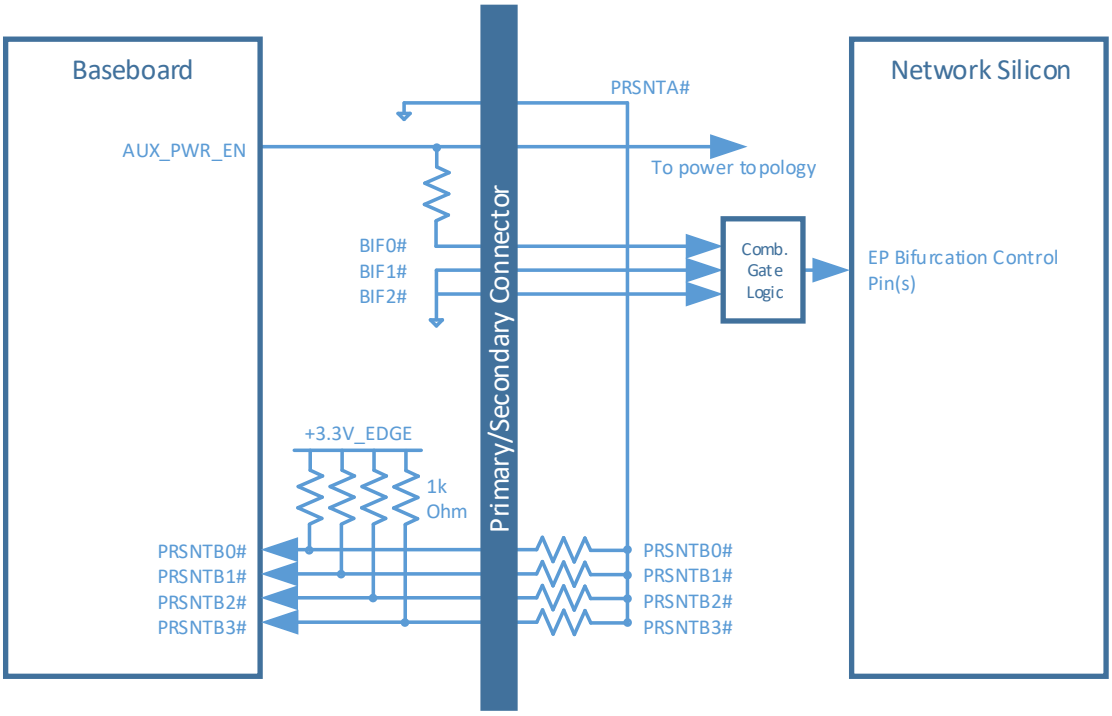
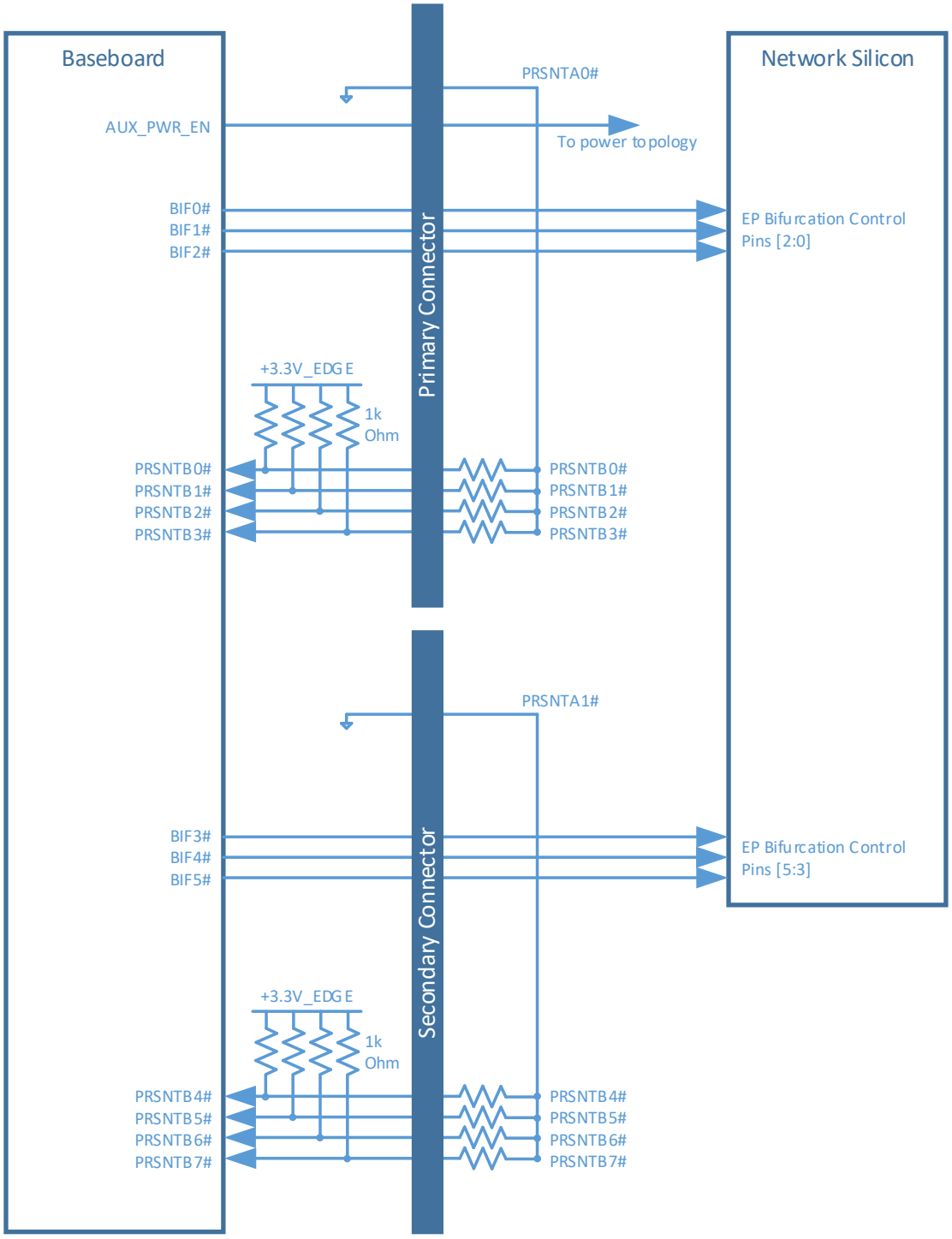


Figure 105: DSFF PCIe Present and Bifurcation Pins (Controlled BIF[5:0]#)



4.5.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. SMBus is a multi-initiator protocol. Commands may originate from the baseboard or the NIC. The AC/DC specifications are defined in the SMBus 2.0 specification. The SMBus[0:1] interfaces are pinned out on the Primary and Secondary Connectors.

For SFF and DSFF OCP NIC 3.0 card implementations, FRU EEPROM accesses and MCTP over SMBus transactions shall use the Primary Connector only. This specification does not preclude additional use cases of the SMBus[1] interface on a DSFF, but it is outside the scope of this specification. An example connection diagram is shown in Figure 106.

> **Note:** The SMBus pins form an internal interface between the OCP NIC Card and the Baseboard. These signals are not meant to be directly connected to external devices outside of the system and may pose a security risk or expose the system to damage from ESD exposure.

Table 26: Pin Descriptions – SMBus

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
SMCLK0/SMCLK1	A7	Output, OD	SMBus clock. Open drain, pulled up to +3.3V_EDGE on the baseboard. Note: SMCLK1 is only available on the DSFF.
SMDAT0/SMCLK1	A8	Input / Output, OD	SMBus Data. Open drain, pulled up to +3.3V_EDGE on the baseboard. Note: SMDAT1 is only available on the DSFF.
SMRST0#/SMRST1#	A9	Output, OD	SMBus reset. Open drain. Note: SMRST1# is only available on the DSFF.

4.5.3.1 SMCLK[0:1]

For baseboards, the SMCLK from the platform SMBus controller shall be connected to the connector(s).

For OCP NIC 3.0 cards, the SMCLK from the endpoint silicon and FRU EEPROM shall be connected to the card edge gold fingers. SMCLK[0:1] is on the +3.3V_EDGE power domain. Isolation logic may be required for the target silicon device(s) to prevent a leakage path. The SMBus isolation logic shall be enabled by the local card indication of “Aux Power Good.” Refer to Figure 106 for an example topology and isolation logic.

4.5.3.2 SMDAT[0:1]

For baseboards, the SMDAT from the platform SMBus controller shall be connected to the connector(s).

For OCP NIC 3.0 cards, the SMDAT from the endpoint silicon and FRU EEPROM shall be connected to the card edge gold fingers. SMDAT[0:1] is on the +3.3V_EDGE power domain. Isolation logic may be required for the target silicon device(s) to prevent a leakage path. The SMBus isolation logic shall be enabled by the local card indication of "Aux Power Good." Refer to Figure 106 for an example topology and isolation logic.

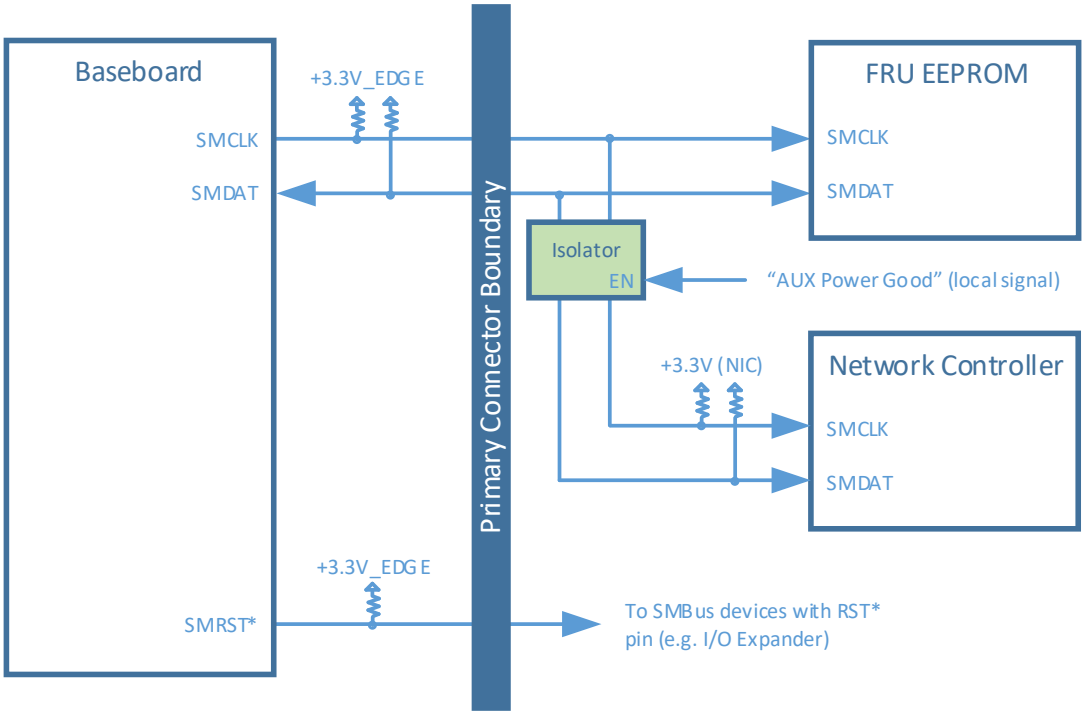
4.5.3.3 SMRST[0:1]#

For baseboards, this pin shall be pulled up to +3.3V_EDGE. The SMRST pin may be used to reset optional downstream SMBus devices (such as temperature sensors). The SMRST# implementation shall be mandatory for baseboard implementations.

For OCP NIC 3.0 cards, SMRST[0]# is optional and is dependent on the OCP NIC 3.0 card implementation. If used, the SMRST[0]# is on the +3.3V_EDGE power domain. Isolation logic may be required if the target device(s) exist on a different power domain to prevent a leakage path. The SMBus isolation logic shall be enabled by the local card indication of "Aux Power Good." Refer to Figure 106 for an example topology and isolation logic. The SMRST[0]# signal shall be left as a no connect if it is not used on the OCP NIC 3.0 card.

4.5.3.4 SMBus Example Topology

Figure 106: Example SMBus Connections (SFF, DSFF)



4.5.4 NC-SI over RBT Interface / Flex I/O Pins

This section provides the pin assignments for the NC-SI over RBT and Flex I/O interface signals on the Primary and Secondary Connector OCP bays.

All card form-factors shall use the Primary Connector RBT pins (if RBT is enabled). For DSFF, RBT or Flex I/O (timing pins) on the Secondary Connector is outside the scope of this specification. The AC/DC specifications for NC-SI over RBT are defined in the DMTF DSP0222 NC-SI specification. Example connection diagrams are shown in Section 4.5.4.3.8.

The RBT pins may also be used as a Flex I/O pins, which allows repurposing them for future use cases. The Baseboard BMC may query the OCP NIC FRU EEPROM for supported Flex I/O capabilities. This may be done via the 0xD3 Flex I/O OEM Record as described in Section 5.10.3.5. In doing so, the Baseboard and NIC selects a compatible Flex I/O mode upon entering Aux Power Mode. Dynamically changing the Flex I/O mode at run-time is not supported by this specification. If the Baseboard and OCP NIC support reconfiguration, the system may select a different Flex I/O option upon transitioning back to ID Mode. The OEM Command required to select a supported non-default Flex I/O mode is outside the scope of this specification.

The supported Flex I/O options are shown in Table 28. One usage of the Flex I/O feature is to support discrete timing synchronization signals across the OCP NIC connector and eliminates internal cabling between the NIC and Baseboard assemblies. This feature is discussed in in Section 4.5.4.4 and may be used to propagate high precision clock profiles such as G.8265.1, G.8275.1, and G.8275.2.

RBT only systems that do not support the Flex I/O features shall assume these pins are for RBT interface only.

4.5.4.1 Interface Isolation Requirements

The baseboard shall possess the ability to isolate all the RBT pins. Isolation prevents a leakage path through unpowered silicon as well as allowing the baseboard to determine which Flex I/O features are supported. Example isolation implementations are shown in Section 4.5.4.3.8 and 4.5.4.4.9.

The isolation logic shall be controlled with baseboard generated signal(s) called FLEXIO_SEL[1:0]. For systems that only support RBT, the signal is referred to as RBT_ISOLATE# which maps to FLEXIO_SEL[0]. These FLEXIO_SEL[1:0] signals are not pinned out the Primary or Secondary Connectors. The FLEXIO_SEL[1:0] modes are defined in Table 27.

Table 27: Flex I/O Mode Selection Truth Table

FLEXIO_SEL[1:0]	Selected Mode
0b00	Full Isolation (default)
0b01	RBT Bus Active
0b10	Timing Sync Active
0b11	Reserved

4.5.4.2 Flex I/O Pin Architecture

The Flex I/O pin architecture was introduced in version 1.5.0 of this specification. It allows repurposing of the RBT pins for additional use cases. Timing Synchronization is one of those options. Further use cases may be added in future releases.

The Flex I/O pin mapping to the RBT and Timing Synchronization modes are shown in Table 28. A NIC may implement any mode supported in the 0xD3 OEM Record shown in Section 5.10.3.5. The Baseboard shall incorporate circuitry to select between RBT and Flex I/O implementations.

Table 28: Pin Descriptions – Flex I/O Pin Architecture

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	RBT Mode (Primary / Secondary)	Timing Synchronization Mode (Primary / Secondary)
RBT0_CLK_IN / RBT1_CLK_IN	OCP_A14	Output	RBT0_CLK_IN / RBT1_CLK_IN	TS0_RESERVED_NC / TS1_RESERVED_NC
FLEXIO_0_0 / FLEXIO_1_0	OCP_B14	Input	RBT0_CRS_DV / RBT1_CRS_DV	TS0_GPI / TS1_GPI
FLEXIO_0_1 / FLEXIO_1_1	OCP_B9	Input	RBT0_RXD0 / RBT1_RXD0	TS0_RX_FREQ / TS1_RX_FREQ
FLEXIO_0_2 / FLEXIO_1_2	OCP_B8	Input	RBT0_RXD1 / RBT1_RXD1	TS0_RX_SYNC / TS1_RX_SYNC
FLEXIO_0_3 / FLEXIO_1_3	OCP_A7	Output	RBT0_TX_EN / RBT1_TX_EN	TS0_GPO / TS1_GPO
FLEXIO_0_4 / FLEXIO_1_4	OCP_A9	Output	RBT0_TXD0 / RBT1_TXD0	TS0_TX_FREQ / TS1_TX_FREQ
FLEXIO_0_5 / FLEXIO_1_5	OCP_A8	Output	RBT0_TXD1 / RBT1_TXD1	TS0_TX_SYNC / TS1_TX_SYNC
RBT0_ARB_OUT / RBT1_ARB_OUT	OCP_A5	Output	RBT0_ARB_OUT / RBT1_ARB_OUT	RBT0_ARB_OUT / RBT1_ARB_OUT
RBT0_ARB_IN / RBT1_ARB_IN	OCP_A4	Input	RBT0_ARB_IN / RBT1_ARB_IN	RBT0_ARB_IN / RBT1_ARB_IN

4.5.4.3 RBT Mode

The following subsections describe the Flex I/O Pins for use as NC-SI Over RBT.

The baseboard shall isolate the RBT pins, including RBT_CLK_IN. The isolation requirements are shown in Section 4.5.4.1. The isolation logic shall be controlled with a baseboard generated signal called RBT_ISOLATE# (this is mapped to FLEXIO_SEL[0]). This signal is not pinned out on the Primary or Secondary Connector. RBT_ISOLATE# shall be low when AUX_PWR_EN=0 or before the card side supplies have been fully enabled (AUX_PWR_EN=1 and NIC_PWR_GOOD=0). RBT_ISOLATE# shall become high when AUX_PWR_EN=1 and the first rising edge of NIC_PWR_GOOD=1 (upon entering Aux Power Mode). RBT_ISOLATE# shall remain high during the transition to Main Power Mode when the NIC_PWR_GOOD signal is in the don't care state. RBT_ISOLATE# shall be high when (AUX_PWR_EN=1, MAIN_PWR_EN=1 and NIC_PWR_GOOD=1). The truth table that describes the RBT_ISOLATE# behavior is illustrated in Table 29 and shown in Figure 132.

Table 29: RBT_ISOLATE# Truth Table

AUX_PWR_EN	MAIN_PWR_EN	NIC_PWR_GOOD	RBT_ISOLATE#
0	X	X	0
1	X	0	0
1	X	Rising edge on entering Aux Power Mode	1
1	1	X	1

RBT reference clock buffers are permitted on the OCP NIC for multi-endpoint implementations if the NIC timing budget is not violated. Refer to the signal integrity requirements in Section 6.1 for timing budget details.

Baseboards shall discover if the OCP NIC card(s) support hardware arbitration. This is done through the Get Capabilities command. The response indicates if the network package supports hardware arbitration and if the package has it implemented. Refer to the Hardware Arbitration Capability (bit 0) and Hardware Arbitration Implementation Status (bit 5..6) fields for details. If hardware arbitration is supported, and is implemented, the associated OCP NIC slot shall be included in the hardware arbitration ring. Refer to the DSP0222 “Summary of scheme for the MC without prior knowledge of hardware arbitration” section for details. If hardware arbitration is not supported by the OCP NIC slot, the Baseboard is responsible for maintaining a continuous circuit to the remaining cards.

Command-based (software) arbitration is also permissible per DSP0222. Baseboards may choose to use the Select Package and Deselect Package commands to allow a network controller to transmit on the shared bus when more than one device is present or when hardware arbitration is not supported.

Table 30: Pin Descriptions – NC-SI over RBT

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
RBT0_CLK_IN / RBT1_CLK_IN	OCP_A14	Output	Reference clock input.
RBT0_CRS_DV / RBT1_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid.
RBT0_RXD0 / RBT1_RXD0	OCP_B9	Input	Receive data. Data signals from the network controller to the BMC.
RBT0_RXD1 / RBT1_RXD1	OCP_B8	Input	Receive data. Data signals from the network controller to the BMC.
RBT0_TX_EN / RBT1_TX_EN	OCP_A7	Output	Transmit enable.
RBT0_TXD0 / RBT1_TXD0	OCP_A9	Output	Transmit data. Data signals from the BMC to the network controller.
RBT0_TXD1 / RBT1_TXD1	OCP_A8	Output	Transmit data. Data signals from the BMC to the network controller.
RBT0_ARB_OUT / RBT1_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output.

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
RBT0_ARB_IN / RBT1_ARB_IN	OCP_A4	Input	NC-SI hardware arbitration input.

Note: The RBT pins form an internal interface between the OCP NIC Card and the Baseboard. These signals are not meant to be directly connected to external devices outside of the system and may pose a security risk or exposes the system to damage from ESD exposure.

4.5.4.3.1 RBT[0:1]_CLK_IN

Synchronous clock reference for receive, transmit and control interface. The clock shall have a typical frequency of 50MHz ±50 ppm.

For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the Primary Connector OCP bay. The RBT_CLK_IN shall not be driven until the card has transitioned into Aux Power Mode. The RBT_CLK_IN shall be continuous once it has started and while RBT_ISOLATE# is high.

If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to ground through a 100 kΩ pull down resistor.

For OCP NIC 3.0 cards, this pin shall be connected between the card gold finger and the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.

4.5.4.3.2 RBT[0:1]_CRS_DV

This signal is used to indicate to the baseboard that the carrier sense/receive data is valid.

For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed.

If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to ground through a 100 kΩ pull down resistor.

For OCP NIC 3.0 cards, this pin shall be connected between the card gold finger and the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.

4.5.4.3.3 RBT[0:1]_RXD[0:1]

For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed.

If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to GND through a 100 kΩ pull down.

For OCP NIC 3.0 cards, this pin shall be connected between the card gold fingers and the RBT_RXD[0:1] pins on endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.

4.5.4.3.4 RBT[0:1]_TX_EN

For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to ground on the baseboard between the RBT isolator and the OCP connector to prevent the card-side signals from floating when the RBT signals are isolated.

If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to ground through a 100 kΩ pull down.

For OCP NIC 3.0 cards, this pin shall be connected between the card gold finger and the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.

4.5.4.3.5 RBT[0:1]_TXD[0:1]

For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the RBT isolator and the OCP connector to prevent the card-side signals from floating when the RBT signals are isolated.

If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to GND through a 100 kΩ pull down.

> **Note:** Some BMC vendors use the RBT_TXD[0:1] pins as hardware configuration straps. A 4.7 kΩ to 10 kΩ pull up/pull down resistor is permitted between the BMC and the RBT isolator for this purpose. The resulting network will not violate the NC-SI V_{IHMIN} of 2.0V.

For OCP NIC 3.0 cards, this pin shall be connected between the card gold fingers and the RBT_TXD[0:1] pins on the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.

4.5.4.3.6 RBT[0:1]_ARB_OUT

If the baseboard supports multiple OCP NIC 3.0 cards connected to the same RBT interface, it shall implement logic that connects the RBT_ARB_OUT pin of the first populated OCP NIC 3.0 card to its RBT_ARB_IN pin if it is the only card present or to the RBT_ARB_IN pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic shall bypass slots that are not populated, powered off, or in ID mode. A two OCP NIC 3.0 card example using an analog mux is shown in Figure 108 and Figure 109.

If the baseboard does not support NC-SI over RBT or implements only one OCP NIC 3.0 interface, this signal shall be directly connected to the RBT_ARB_IN pin to complete the hardware arbitration ring on the OCP NIC 3.0 card.

For OCP NIC 3.0 cards that support hardware arbitration, this pin shall be connected between the card gold finger and the RBT_ARB_IN pin on the endpoint silicon. If the card implements two controllers, both must be connected internally to complete the ring, see Figure 108 and Figure 109. If hardware arbitration is not supported, then this pin shall be directly connected to the card edge RBT_ARB_IN pin. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.

4.5.4.3.7 RBT[0:1]_ARB_IN

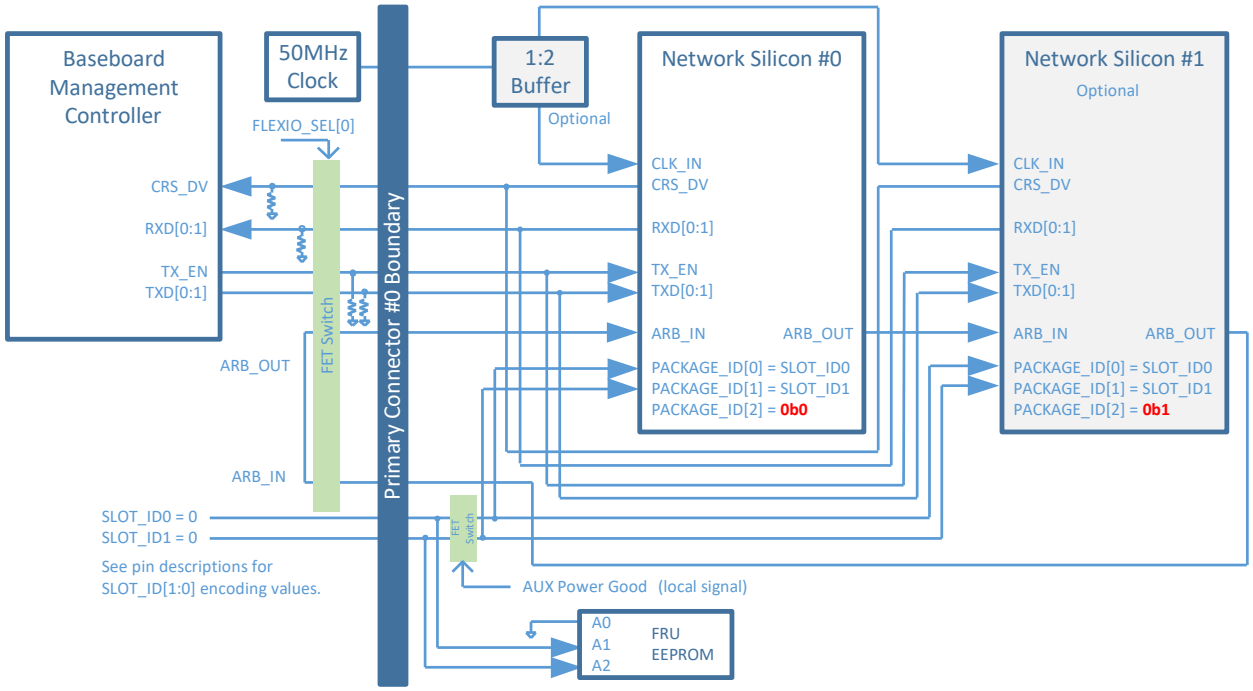
If the baseboard supports multiple OCP NIC 3.0 cards connected to the same RBT interface, it shall implement logic that connects the RBT_ARB_IN pin of the first populated OCP NIC 3.0 card to its RBT_ARB_OUT pin if it is the only card present or to the RBT_ARB_OUT pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic shall bypass slots that are not populated, powered off, or in ID mode. A two OCP NIC 3.0 card example using an analog mux is shown in Section 4.5.4.3.8.

If the baseboard does not support NC-SI over RBT or implements only one OCP NIC 3.0 interface, this signal shall be directly connected to the RBT_ARB_OUT pin to complete the hardware arbitration ring on the OCP NIC 3.0 card.

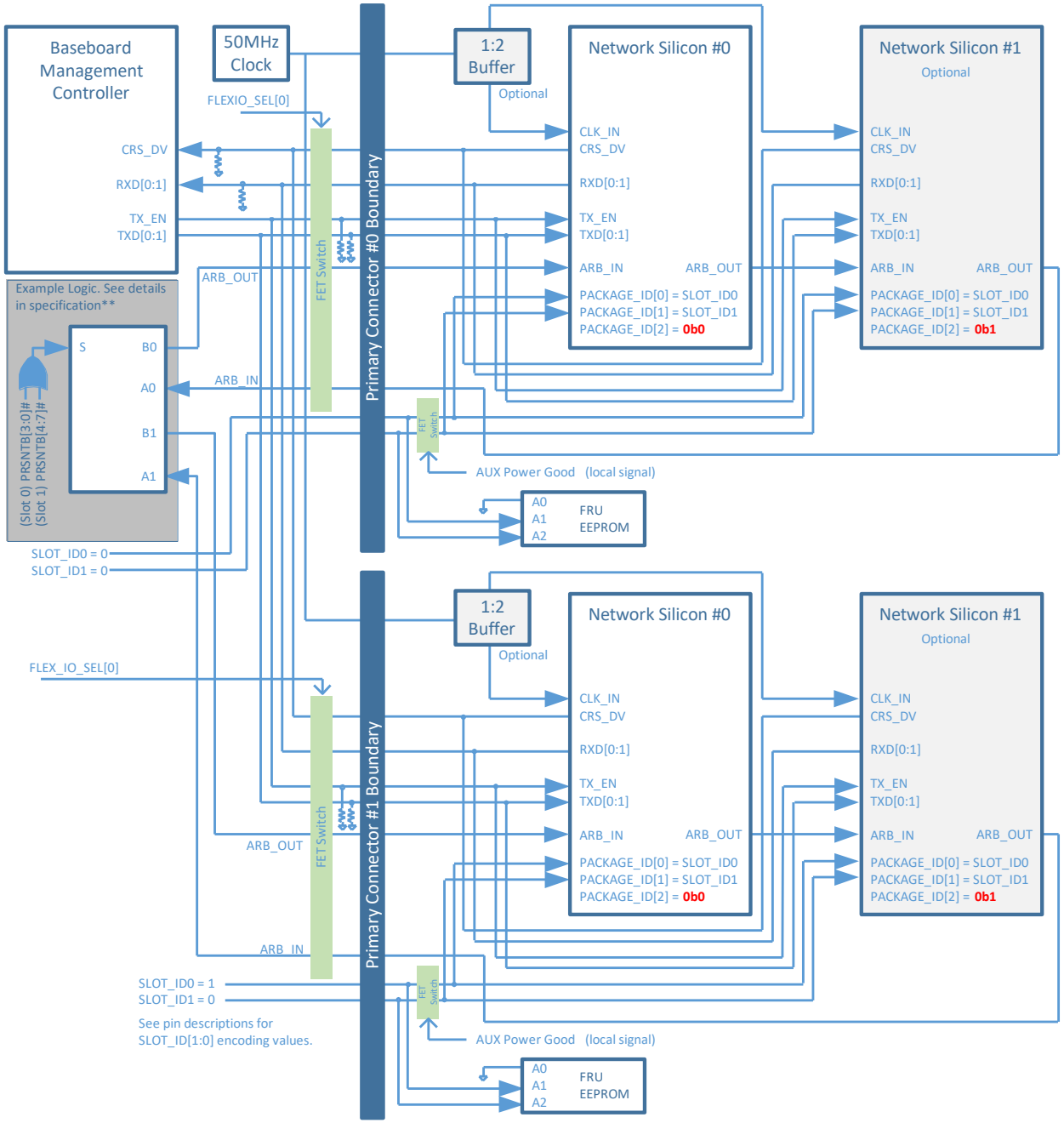
For OCP NIC 3.0 cards that support hardware arbitration, this pin shall be connected between the card gold finger and the RBT_ARB_OUT pin on the endpoint silicon. If the card implements two controllers, both must be connected internally to complete the ring, see Figure 108 and Figure 109. If hardware arbitration is not supported, then this pin shall be directly connected to the card edge RBT_ARB_OUT pin. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.

4.5.4.3.8 RBT Example Topologies

Figure 107: NC-SI over RBT Connection Example – Single Primary Connector



2482 Figure 108: NC-SI over RBT Connection Example – Dual Primary Connectors



2483
2484

Note 1: For baseboard designs with a single Primary Connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For designs with multiple Primary Connectors (supporting multiple SFF cards, or a configurable DSFF slot), connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system. An example dual Primary Connector implementation is shown in Figure 108. Detailed combinatorial logic is shown in Figure 110 along with a truth table in Table 31.

Note 2: For baseboard implementations having two or more RBT busses, the baseboard hardware arbitration rings shall remain within their respective bus and shall not cross RBT bus domains.

Note 3: The baseboard implementation shall maintain the arbitration ring integrity when there exists one or more cards that are not present, plugged in but are powered off, or in ID Mode.

Note 4: For OCP NIC 3.0 cards with two discrete endpoint silicon, the Package ID[2] bit shall be statically set based on the silicon instance. For example, the figure above shows Network Silicon #0 and Network Silicon #1. Network Silicon #0 has Package ID[2] = 0b0, Network Silicon #1 has Package ID[2] = 0b1.

Note 5: Designs that implement a clock fan out buffer will affect the RBT timing budget. Careful analysis of the timing budget is required. Refer to Section 6.1 for RBT signal integrity and timing budget considerations.

Note 6: RBT timing analysis shall include the propagation delay of any hardware arbitration muxes, and any resampling of the ARB_IN signal on the baseboard.

Note 7: The NIC PRSNTB# pin states may be read by the system in ID Mode. The PRSNTB# pins are high by default. One or more pins are pulled down when a card is installed in the respective slot(s). The baseboard shall use the PRSTNB# states to setup the hardware arbitration ring path upon entering Aux Power mode and remain static in Main Power Mode.

Figure 109: Example Hardware Arbitration Mux Logic – Dual Primary Connectors

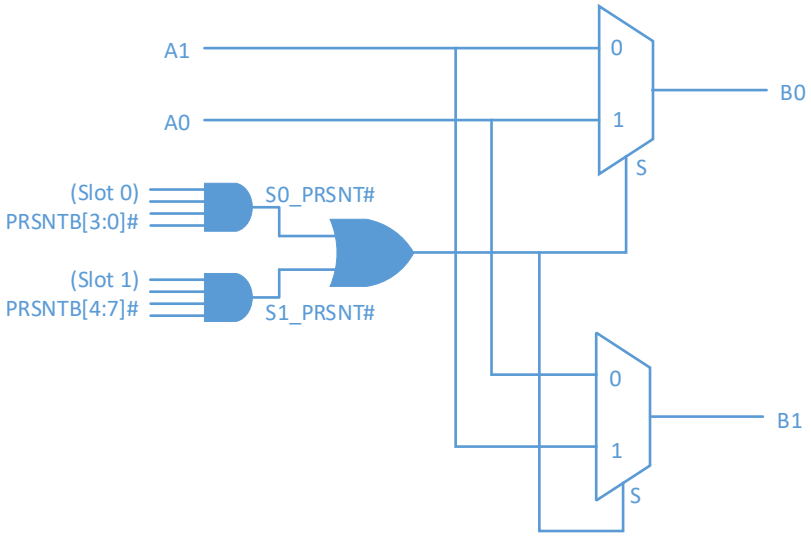


Table 31: Hardware Arbitration Mux Logic Truth Table

Slot 0 Card	Slot 1 Card	S0_PRSNT#	S1_PRSTN#	S	B0	B1
Installed	Installed	0	0	0	A1	A0
Installed	Not Installed	0	1	1	A0	X
Not Installed	Installed	1	0	1	X	A1
Not Installed	Not Installed	1	1	1	X	X

4.5.4.4 Timing Synchronization Mode (Flex I/O)

The following subsections describe the Flex I/O Pins for use as a Timing Synchronization interface.

The baseboard shall isolate the timing pins. The isolation requirements are shown in Section 4.5.4.1. FLEXIO_SEL[1:0] signals shall be low when AUX_PWR_EN=0 or before the card side supplies have been fully enabled (AUX_PWR_EN=1 and NIC_PWR_GOOD=0). FLEXIO_SEL[1:0] shall become asserted as 0b10 when AUX_PWR_EN=1 and on the first rising edge of NIC_PWR_GOOD=1 (upon entering Aux Power Mode). FLEXIO_SEL[1:0] shall remain asserted as 0b10 during the transition to Main Power Mode when the NIC_PWR_GOOD signal is in the don't care state. FLEXIO_SEL[1:0] shall remain asserted as 0b10 when (AUX_PWR_EN=1, MAIN_PWR_EN=1 and NIC_PWR_GOOD=1). The truth table that describes the FLEXIO_SEL[1:0] behavior is illustrated in Table 32 and shown in Figure 132.

Table 32: FLEXIO_SEL[1:0] Truth Table

AUX_PWR_EN	MAIN_PWR_EN	NIC_PWR_GOOD	FLEXIO_SEL[1:0]
0	X	X	0b00
1	X	0	0b00
1	X	Rising edge on entering Aux Power Mode	0b10
1	1	X	0b10

The FLEXIO_SEL[1:0] pins are not allowed to dynamically change state once the baseboard enters Aux Power Mode or Main Power Mode. Assertion of a different FLEXIO_SEL[1:0] state requires transitioning back to ID Mode. Refer to Section 4.9 for the Power State Machine details.

The Baseboard shall query the 0xD3 Flex I/O OEM Record to determine the supported clocking frequency. The preferred option is 10 MHz with an embedded 1PPS (ePPS), the second option is 10 MHz with a separate 1PPS. These two options allow interoperability with a wide range of devices. The timing general purpose input (TS_GPI) and timing general purpose output (TS_GPO) allow the OCP NIC to define permissible functions that are used to communicate high priority status information (such as loss of link on the OCP NIC line side interface). Refer to Section 5.10.3.5 for details.

Table 33: Pin Descriptions – Time Synchronization Mode

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
TS0_RX_FREQ / TS1_RX_FREQ	OCP_B9	Input	Timing application receive frequency Clock.
TS0_RX_SYNC / TS1_RX_SYNC	OCP_B8	Input	Timing application receive synchronization.
TS0_TX_FREQ / TS1_TX_FREQ	OCP_A9	Output	Timing application transmit frequency Clock.
TS0_TX_SYNC / TS1_TX_SYNC	OCP_A8	Output	Timing application transmit synchronization.
TS0_GPI / TS1_GPI	OCP_B14	Input	Timing application general purpose input.
TS0_GPO / TS1_GPO	OCP_A7	Output	Timing application general purpose output.

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
			Note: TS_GPO is not supported in this release of the specification. Leave this pin as a no connect on the Baseboard and NIC.
TS0_RESERVED_NC / TS1_RESERVED_NC	OCP_A14	Output	Not used for timing applications in this specification release.
RBT0_ARB_OUT / RBT1_ARB_OUT	OCP_A5	Output	These pins are not used for the Time Synchronization mode but are required to maintain RBT hardware arbitration loop compatibility with RBT only baseboard implementations. Directly wire ARB_IN to ARB_OUT. See description in Section4.5.4.4.9.
RBT0_ARB_IN / RBT1_ARB_IN	OCP_A4	Input	

Note 1: The timing pins shall be routed as 50 Ohm single-ended nets. Portions of the timing path may be shared with the Baseboard side RBT signals with the same impedance.

Note 2: The default state of the TS_RX_FREQ and TS_RX_SYNC pins shall be High-Z prior to being enabled by the Baseboard to prevent issues when plugged into RBT only baseboards.

Note 3: The timing pins form an internal interface between the OCP NIC Card and the Baseboard. These signals are not meant to be directly connected to external devices outside of the system and may pose a security risk or exposes the system to damage from ESD exposure. System designers are responsible for additional protection logic if the timing signals are directly cabled to 50 Ohm coax. A buffer shall limit the card-side IOH to no more than 3 mA to prevent damage.

4.5.4.4.1 TS[0:1]_TX_FREQ

Timing application transmit frequency clock. This pin is an output from the baseboard and typically drives a single ended 10 MHz reference clock with an ePPS (embedded 1PPS) signal. The 10 MHz carrier frequency duty cycle is defined to be 50%; the ePPS duty cycle is defined to be 25%. This pin may optionally carry a 10 MHz reference clock with a separate 1PPS signal on the TS_TX_SYNC pin. The NIC shall advertise the supported option(s) in the 0xD3 OEM Record.

The baseboard shall isolate this signal until the 0xD3 OEM Record has been queried and the TS_TX_FREQ functionality has been determined. This pin operates as a 3.3V TTL level single ended clock. If the baseboard does not support the TS[0:1]_TX_FREQ pins, then they shall be terminated through a 100 kΩ pull down resistor to ground.

For OCP NIC 3.0 cards, these pins shall be left as a no connect if the TS[0:1]_TX_FREQ pins are not supported.

4.5.4.4.2 TS[0:1]_TX_SYNC

Timing application transmit synchronization pin. This pin is an output from the baseboard and typically drives a 1PPS signal when used in conjunction with the TS_TX_FREQ pin operating solely as a 10 MHz reference clock. The TS_TX_SYNC pin is also permitted to operate as a separate 10 MHz frequency source. The NIC shall advertise the supported option(s) in the 0xD3 OEM Record.

The baseboard shall isolate this signal until the 0xD3 OEM Record has been queried and the TS_TX_SYNC functionality has been determined. This pin is 3.3V TTL level logic. If the baseboard does not support the TS[0:1]_TX_SYNC pins, then, then they shall be terminated through a 100 kΩ resistor to ground.

For OCP NIC 3.0 cards, these pins shall be left as a no connect if the TS[0:1]_TX_SYNC pins are not supported.

4.5.4.4.3 TS[0:1]_RX_FREQ

Timing application receive frequency pin. This pin is an input to the baseboard and typically receives a single ended 10 MHz reference clock with an ePPS (embedded 1PPS) signal. The 10 MHz carrier frequency duty cycle is defined to be 50%; the ePPS duty cycle is defined to be 25%. This pin may optionally carry a 10 MHz reference clock with a separate 1PPS signal on the TS_RX_SYNC pin. The NIC shall advertise the supported option(s) in the 0xD3 OEM Record.

The NIC shall keep this signal high impedance until the host enables the TS_RX_FREQ timing pin functionality. This pin shall be left as a no connect on the NIC if the TS[0:1]_RX_FREQ functionality is not supported.

The baseboard shall isolate this signal until the 0xD3 OEM Record has been queried and the TS_RX_FREQ functionality has been determined. This pin operates as a 3.3V TTL level single ended clock. If the baseboard does not support the TS[0:1]_RX_FREQ pins, then this pin shall be terminated through a 100 kΩ pull down to ground.

4.5.4.4.4 TS[0:1]_RX_SYNC

Timing application receive synchronization pin. This pin is an input to the baseboard and typically receives a 1PPS signal when used in conjunction with the TS_RX_FREQ pin operating solely as a 10 MHz reference clock. The TS_RX_SYNC pin is also permitted to operate as a separate 10 MHz frequency source. The NIC shall advertise the supported option(s) in the 0xD3 OEM Record.

The NIC shall keep this signal high impedance until the host enables the TS_RX_SYNC timing pin functionality. This pin shall be left as a no connect on the NIC if the TS[0:1]_RX_SYNC functionality is not supported.

The baseboard shall isolate this signal until the 0xD3 OEM Record has been queried and the TS_RX_SYNC functionality has been determined. This pin is 3.3V TTL level logic. If this pin is not used, it shall be terminated at the OCP NIC side card edge with a 100 kΩ resistor to ground.

4.5.4.4.5 TS[0:1]_GPI

Timing application pin GPI (general purpose input). This pin is defined to be an input to the baseboard and is driven active high by the OCP NIC. The function of this signal is declared in the 0xD3 OEM Record.

The TS_GPI pin supports Loss of Signal and Loss of Lock Indication. In this context, these functions are defined as:

- **Loss of Signal** – Indication that a network port currently used to propagate timing synchronization is either down or unconnected to a remote network partner.

- **Loss of Lock** – Indication that the timing synchronization signals are not synchronized to a primary clock / primary time server. For example, a network link is up but PTP packets are not detected by the OCP NIC. This could be due to the local DPLL is operating in free-run mode. The physical timing signal may still be present, but no longer locked to a known external source.

The NIC shall keep this signal high impedance until the host enables the TS_GPI timing pin functionality.

The baseboard shall isolate this signal until the 0xD3 OEM Record has been queried and the TS_GPI functionality has been determined. This pin is 3.3 V.

If TS_GPI is not supported by the baseboard, it shall be terminated at the Baseboard side connector with a 100 kΩ resistor to ground.

If TS_GPI is not supported by the OCP NIC card, it shall be left as a no connect.

4.5.4.4.6 TS[0:1]_GPO

Timing application pin GPO (general purpose output). This pin is defined to be an active high output from the baseboard and received by the OCP NIC. The function of this signal is declared in the 0xD3 OEM Record.

> **Note:** TS_GPO is not supported in this release of the specification. Leave this pin as a no connect on the NIC. The baseboard shall terminate this pin to ground through a 100 kΩ pull down.

4.5.4.4.7 TS[0:1]_RESERVED_NC

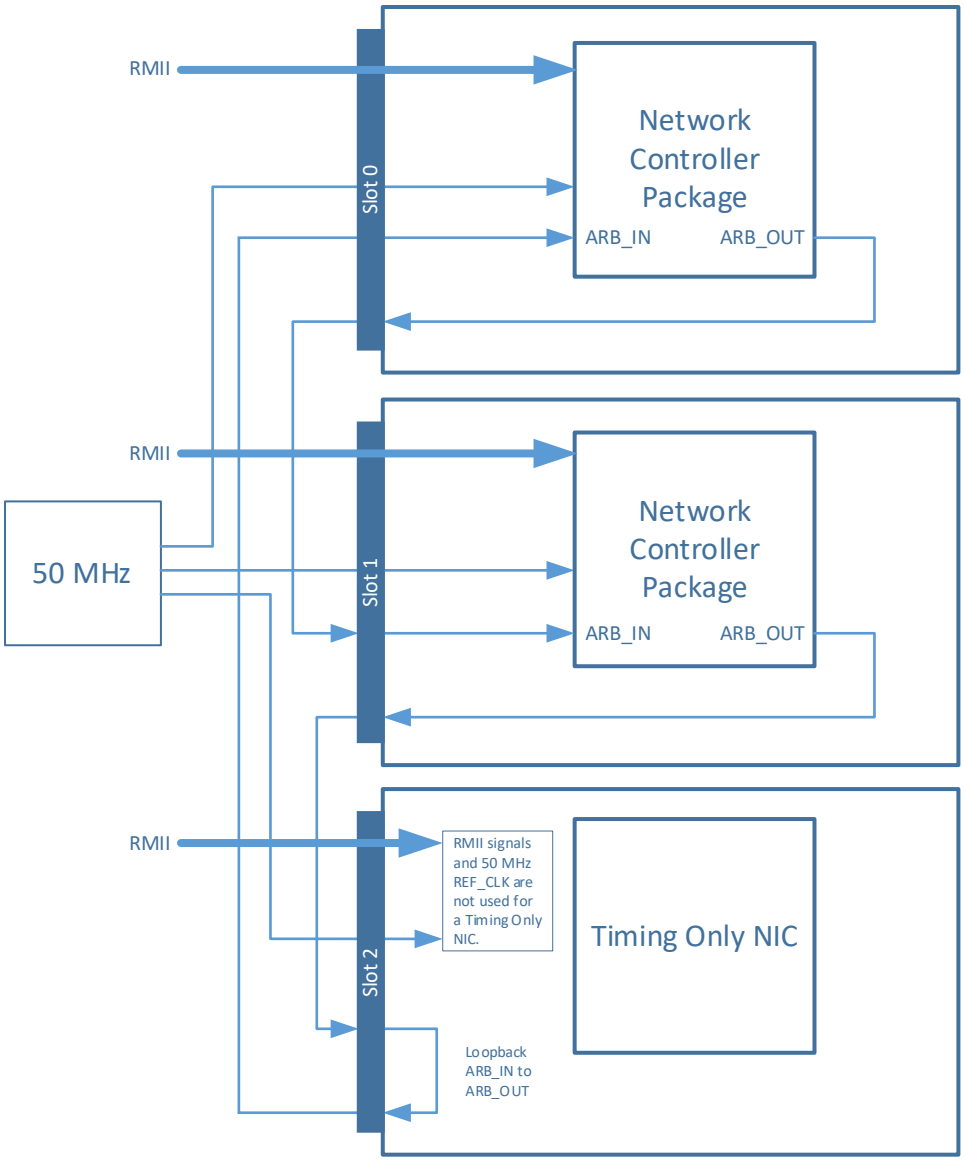
The TS[0:1]_RESERVED_NC pins are not defined for use in this release of the OCP NIC 3.0 specification. For OCP NIC 3.0 cards, these pins shall be left as a no connect.

4.5.4.4.8 RBT[0:1]_ARB_OUT, RBT[0:1]_ARB_IN for SFF Timing NICs

For maintaining compatibility with RBT only SFF baseboard implementations, the RBT ARB_OUT and ARB_IN pins continue to be used in the Timing Synchronization Mode. The OCP NIC shall connect the RBT[0]_ARB_OUT to RBT[0]_ARB_IN. The example NIC side implementation is shown in Figure 110. These pins are used to maintain a complete hardware arbitration ring for RBT implementations in adjacent OCP NIC slots. The baseboard may require RBT signal conditioning logic for a multi-SFF card implementation.

RBT only SFF baseboard implementations may connect the hardware arbitration logic solely based on card presence. New SFF and DSFF compatible baseboard implementations shall use the detection flow described in Section 4.5.4.3 to determine if the NIC supports hardware arbitration before adding the NIC slot to the hardware arbitration ring.

Figure 110: RBT Hardware Arbitration Logic Example for OCP Timing NIC Implementations



Note: Baseboard side signal conditioning logic may be required for the hardware arbitration ring to ensure timing requirements are met. Refer to Section 6.1 for details.

4.5.4.4.9 Timing Synchronization Example Topology

Figure 111: Flex I/O Baseboard with Timing NIC - Connection Example

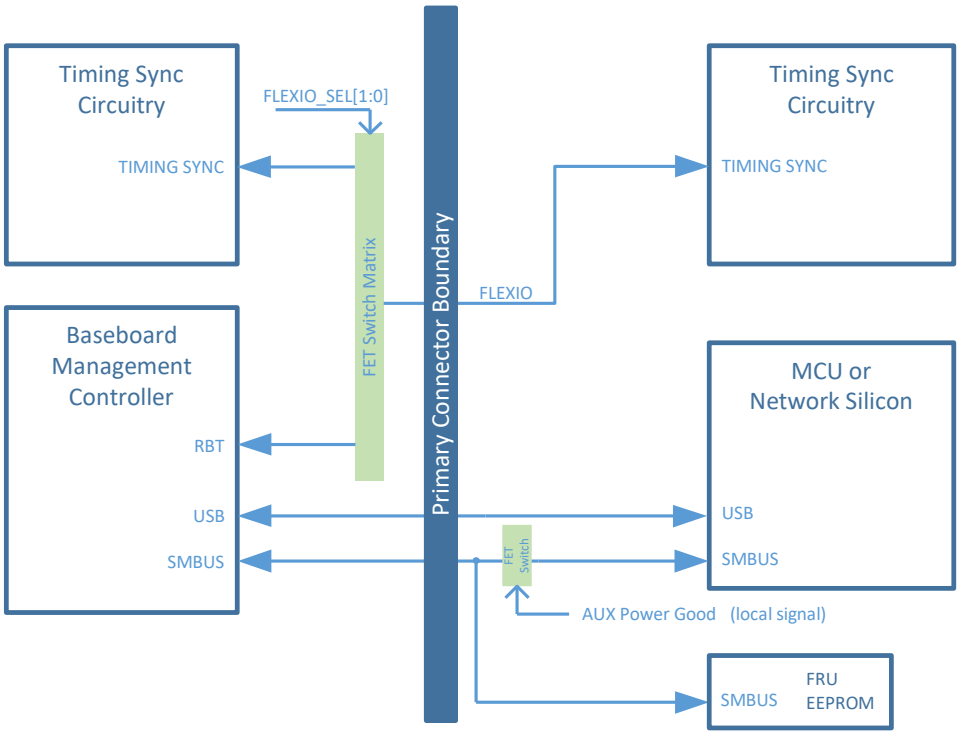


Figure 112: Flex I/O Baseboard with RBT NIC - Connection Example

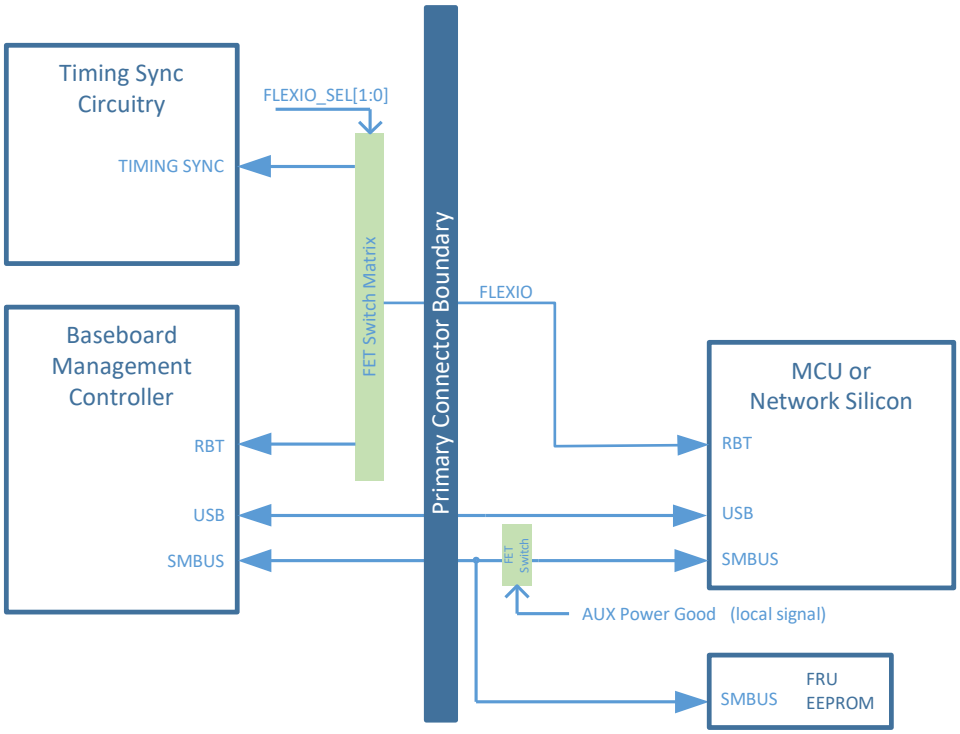
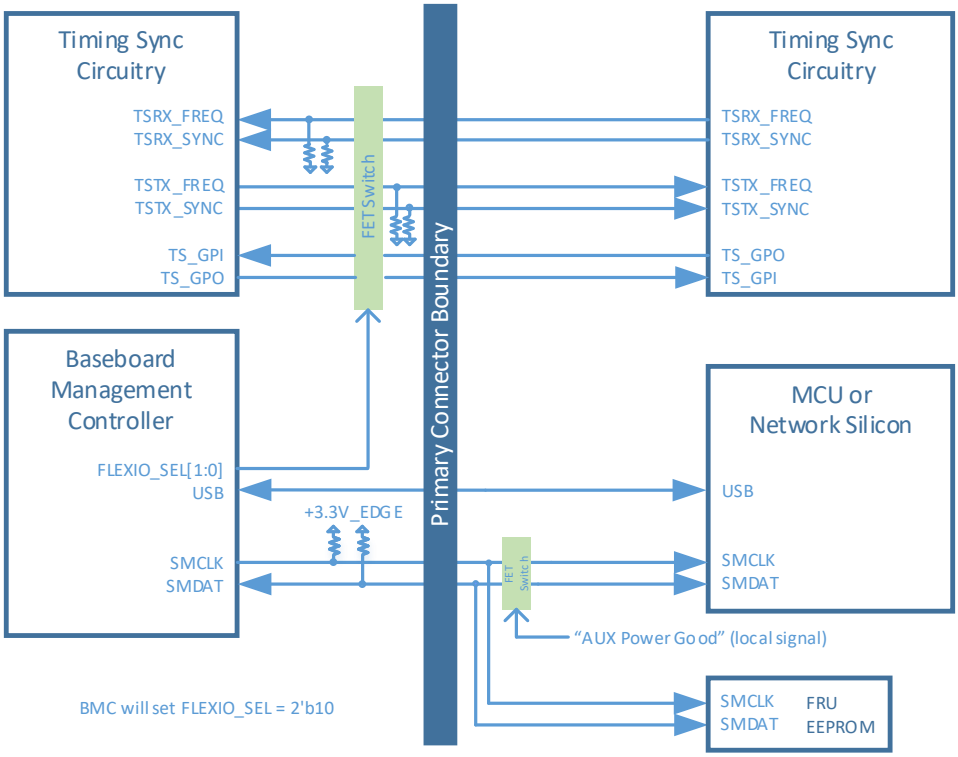


Figure 113: Timing Synchronization (Flex I/O) Connection Example (No RBT)



4.5.5 Slot ID Pins

This section provides the pin assignments for the SLOT_ID signals. The SLOT_ID[1:0] pins are used for setting the card FRU EEPROM, RBT Package ID for "Fixed and Discoverable" SMBus Address implementations. DSFF implementations do not use SLOT_ID[3:2]. For 2xSFF implementations, the SLOT_ID[3:2] pins are used for the "left" OCP NIC (when viewing into the NIC) as SLOT_ID[1:0].

Table 34: Pin Descriptions – SLOT_ID[1:0]

Signal Name (Primary & Secondary)	Pin #	Baseboard Direction	Signal Description
SLOT_ID0 / 2 SLOT_ID1 / 3	OCP_B7 OCP_A6	Output	Used to set the FRU EEPROM, RBT Package ID and Fixed SMBus Address 0/1.

4.5.5.1 SLOT_ID[3:0]

For baseboards, the SLOT_ID[3:0] pins shall be connected to GND through a 100 Ω pull down or to +3.3V_EDGE through a 4.7 kΩ pull up. For SFF, the SLOT[1:0] values are based on the following mapping on a per slot basis:

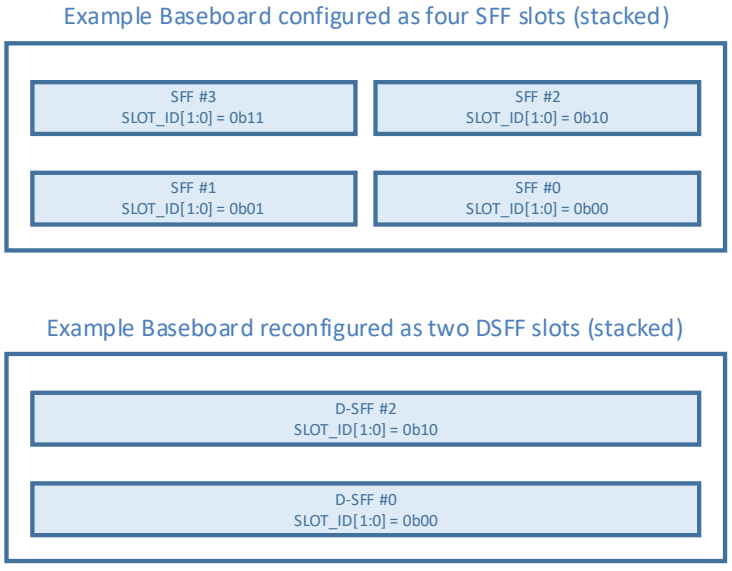
Table 35: Slot ID Numbering

Physical Slot (Decimal)	SLOT_ID1 OCP_A6	SLOT_ID0 OCP_B7
0	0	0
1	0	1
2	1	0
3	1	1

DSFF cards repurpose two SFF slots as a single DSFF implementation, baseboard designers shall ensure that that the slot ID numbering is sequential when converting two SFF slots into a DSFF slot. Slot 0 shall be associated with the Primary Connector and uses SLOT_ID[1:0]. Slot 1 shall be associated with the Secondary Connector and uses SLOT_ID[3:2]. The DSFF RBT package addresses are only set with the SLOT_ID[1:0] pins. The SLOT_ID[3:2] pins are not used to set the package address on the DSFF card.

Further, DSFF baseboards that support a second DSFF card shall have Slot 2 associated with the Primary Connector and Slot 3 associated with the Secondary Connector. The positioning of the slots is implementation specific. An example of this is shown in Figure 114.

Figure 114: Slot ID Numbering for reconfigurable DSFF Baseboards



For OCP NIC 3.0 cards, the SLOT_ID[1:0] pins shall be used to set the RBT Package ID and the FRU EEPROM address on the OCP NIC 3.0 card. The OCP NIC 3.0 card may optionally implement weak pull up or pull down resistors (>47 kΩ) to prevent the silicon pins from floating prior to the local silicon “Aux power good.”

For OCP NIC 3.0 cards, SLOT_ID0 shall be connected to the endpoint device GPIO associated with Package ID[0]. SLOT_ID1 shall be associated with Package ID[1]. Refer to Section 5.8.1 and the device datasheet for details.

For OCP NIC 3.0 cards with multiple endpoint devices, Package ID[2] shall be used to identify a second physical RBT capable controller on the same physical card.

For Package ID addressing, the SLOT_ID[1:0] pins shall be buffered on NIC side with a FET switch (or a similar implementation) to prevent a leakage path when the OCP NIC 3.0 card is in ID mode. The SLOT_ID[1:0] buffers shall isolate the signals to the network silicon until an "Aux Power Good" is generated locally from the NIC. This indication shall be generated from an on-board voltage monitor or similar logic. OCP NIC 3.0 designers may omit isolation logic for the Package ID addressing if the target silicon properly isolates the signals when it is unpowered.

For FRU EEPROM addressing, the SLOT_ID0 pin shall be directly connected to the EEPROM A1 address pin; SLOT_ID1 shall be connected to the EEPROM A2 address pin. No isolation shall be used for the FRU EEPROM connections.

For endpoint devices without NC-SI over RBT support, these pins shall only be connected to the FRU EEPROM as previously described.

4.5.5.2 SLOT_ID[3:0] Implementation Example

Refer to the RBT Example Topologies in Section 4.5.4.3.8 for the SLOT_ID connectivity.

4.5.6 Scan Chain Pins

This section provides the pin assignments for the Scan Chain interface signals on the Primary Connector OCP Bay. The scan chain is a point-to-point bus on a per OCP slot basis. For DSFF implementations, the Scan Chain is only implemented on the Primary Connector. A Scan Chain implementation on the Secondary Connector is outside the scope of this specification.

The scan chain consists of two unidirectional busses, a common clock and a common load signal. The SCAN_DATA_OUT signal serially shifts control signals from the baseboard to the OCP NIC 3.0 card. The SCAN_DATA_IN signal serially shifts bits from the OCP NIC 3.0 card to the baseboard. The SCAN_DATA_OUT and SCAN_DATA_IN chains are independent of each other. The scan chain SCAN_CLK is driven from the baseboard. The SCAN_LD# pin, when asserted by the baseboard, allows loading of the data on to the shift registers. An example timing diagram is shown in Figure 115 and Figure 116. An example connection diagram is shown in Figure 117.

Note 1: The SCAN_DATA_OUT chain is provisioned but is not used on OCP NIC 3.0 cards for this revision of the specification.

Note 2: The Scan Chain pins form an internal interface between the OCP NIC Card and the Baseboard. These signals are not meant to be directly connected to external devices outside of the system and may pose a security risk or expose the system to damage from ESD exposure.

Table 36: Pin Descriptions – Scan Chain

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
SCAN_CLK0 / SCAN_CLK1	OCP_B6	Output	Scan clock. The SCAN_CLK is an output pin from the baseboard to the OCP NIC 3.0 card. The SCAN_CLK may run up to 12.5MHz.
SCAN_DATA_OUT0 / SCAN_DATA_OUT1	OCP_B5	Output	Scan data output from the baseboard to the OCP NIC 3.0 card. This bit stream is used to shift configuration data out to the NIC.
SCAN_DATA_IN0 / SCAN_DATA_IN1	OCP_B4	Input	Scan data input to the baseboard. This bit stream is used to shift out NIC status bits to the baseboard.
SCAN_LD0# / SCAN_LD1#	OCP_B3	Output	Scan shift register load. Used to latch configuration data on the OCP NIC 3.0 card.

4.5.6.1 SCAN_CLK

For baseboard implementations, the SCAN_CLK pin shall be connected to the Primary Connector. The SCAN_CLK pin shall be tied directly to GND if the scan chain is not used. The SCAN_CLK may run up to 12.5 MHz.

For NIC implementations, the SCAN_CLK pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 117, below. The SCAN_CLK pin shall be pulled up to +3.3V_EDGE through a 1 kΩ resistor.

4.5.6.2 SCAN_DATA_OUT

For baseboard implementations, the SCAN_DATA_OUT pin shall be connected to the Primary Connector. The SCAN_DATA_OUT pin shall be pulled down to GND through a 1 kΩ resistor if the scan chain is not used.

For NIC implementations, the SCAN_DATA_OUT pin shall be pulled down to GND on the OCP NIC 3.0 card through a 10 kΩ resistor.

4.5.6.3 SCAN_DATA_IN

For baseboard implementations, the SCAN_DATA_IN pin shall be pulled up to +3.3V_EDGE through a 10 kΩ resistor to prevent the input signal from floating if a card is not installed. This pin may be left as a no connect if the scan chain is not used.

For NIC implementations, the SCAN_DATA_IN scan chain is required. The SCAN_DATA_IN pin shall be connected to Shift Register 0, as defined in the text and Figure 117.

4.5.6.4 SCAN_LD#

For baseboard implementations, the SCAN_LD# pin shall be pulled up to +3.3V_EDGE through a 1 kΩ resistor if the scan chain is not used to prevent the OCP NIC 3.0 card from erroneous data latching.

For NIC implementations, the SCAN_LD# pin implementation is required. The SCAN_LD# pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as

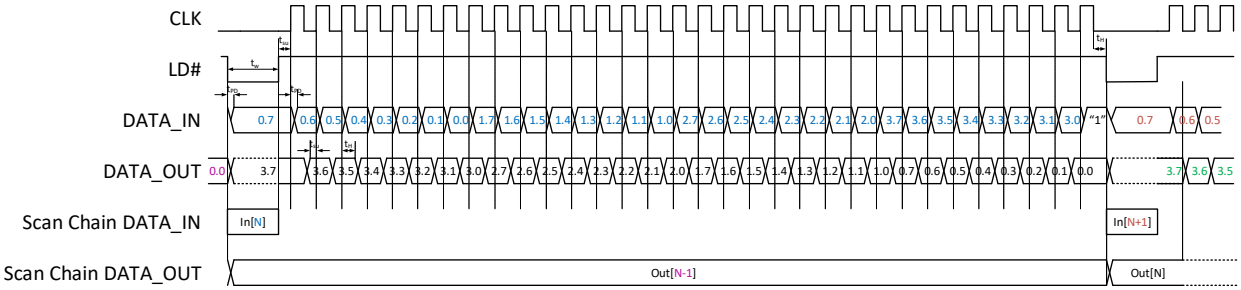
defined in the text and Figure 117. The SCAN_LD# pin shall be pulled up to +3.3V_EDGE through a 10 kΩ resistor.

4.5.6.5 Scan Chain Data Stream

Two possible implementations for the Scan Chain timing diagram are shown in Figure 115 and Figure 116. The specific timing parameters guaranteed by the Baseboard are shown in Table 37 and timing parameters guaranteed by the OCP NIC 3.0 card are shown in Table 38. The parameters assume operation with a 15 pF load between 0 °C and 85 °C. The values are relaxed when compared to the 74LV165 datasheet and allows system implementers to use alternate implementations (such as a CPLD) instead of discrete logic parts.

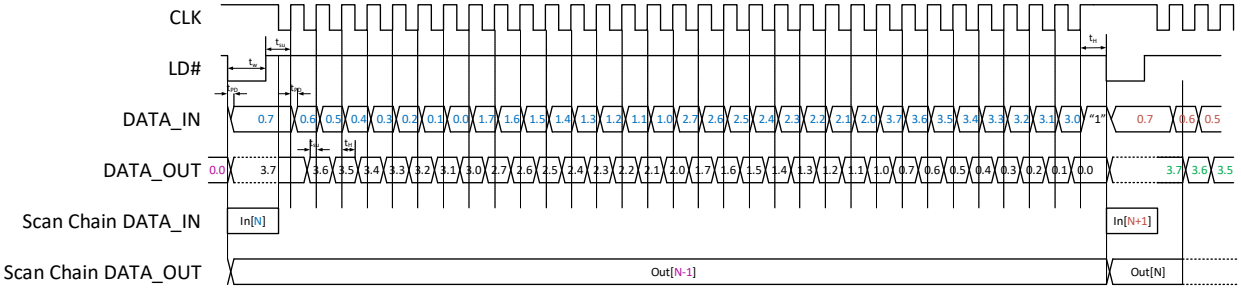
If the waveform in Figure 115 is implemented, the first SCAN_DATA_IN bit (bit 7 on Byte 0) shall be sampled before the first rising edge of the clock that follows SCAN_LD# signal rising edge.

Figure 115: Scan Chain Timing Diagram Implementation 1



If the waveform in Figure 116 is implemented, the first SCAN_DATA_IN bit shall be latched by the baseboard on the falling edge of the clock.

Figure 116: Scan Chain Timing Diagram Implementation 2



For both implementations, each subsequent SCAN_DATA_IN bit shall be latched by the baseboard on the falling edge of the clock. SCAN_DATA_OUT shall be driven by the baseboard such that that sufficient setup/hold time is assured to the OCP NIC 3.0 card. Note that the first bit that is shifted on SCAN_DATA_IN is 0.7 (bit 7 on the least significant Byte) while the first bit that is shifted on SCAN_DATA_OUT is 3.7 (bit 7 on the most significant Byte).

Table 37: Scan Chain Timing Requirements – Baseboard Side

Parameter	Test Condition	Min	Max	Unit
t_W Pulse Duration	SCAN_LD# low	15[1]	-	ns
t_{SU} Setup Time	SCAN_LD# high before SCAN_CLK↑	10	-	ns
	SCAN_DATA_OUT valid before SCAN_CLK↑			
t_H Hold Time	SCAN_LD# high after SCAN_CLK↑	5	-	ns
	SCAN_LD# high after SCAN_CLK↓			
	SCAN_DATA_OUT valid after SCAN_CLK↑			
f_{max}	SCAN_CLK frequency	-	12.5	MHz

Table 38: Scan Chain Timing Requirements – OCP NIC 3.0 Card Side

Parameter	From (Input)	To (Output)	Max	Unit
t_{PD} Propagation Delay	SCAN_CLK[2]	SCAN_DATA_IN	30	ns
	SCAN_LD#[3]	SCAN_DATA_IN	30	ns

Note 1: When $t_w < t_{PD}$ then SCAN_DATA_IN may only be valid after SCAN_LD# rising edge.

Note 2: Applies when SCAN_LD# is high.

Note 3: When SCAN_LD# is low, the SCAN_CLK signal is ignored by the Scan Chain SCAN_DATA_IN.

The Scan Chain provides sideband status indication between the OCP NIC 3.0 card and the baseboard. The Scan Chain bit definition is defined in the two tables below. The Scan Chain data stream is 32-bits in length for both the SCAN_DATA_OUT and the SCAN_DATA_IN streams. The Scan Chain implementation is optional on the host, but its implementation is mandatory per Table 39 and Table 40 on all OCP NIC 3.0 cards. The Scan Chain components operate in the +3.3V_EDGE power domain.

The Scan Chain SCAN_DATA_OUT bus is an output from the host. The Scan Chain SCAN_DATA_OUT bus provides initial configuration options to the OCP NIC 3.0 card. At the time of this writing, the Scan Chain SCAN_DATA_OUT bus is not used. All baseboard systems that implement the Scan Chain shall connect SCAN_DATA_OUT between the platform and the Primary Connector for subsequent revisions of this specification. The SCAN_DATA_OUT data stream shall shift out all 0's prior to AUX_PWR_EN assertion to prevent leakage paths into unpowered silicon.

Table 39: Pin Descriptions – Scan Chain SCAN_DATA_OUT Bit Definition

Byte.bit	SCAN_DATA_OUT Field Name	Default Value	Description
0.[0..7]	Reserved	0h00	Reserved. Byte 0 value is 0h00.
1.[0..7]	Reserved	0h00	Reserved. Byte 1 value is 0h00.
2.[0..7]	Reserved	0h00	Reserved. Byte 2 value is 0h00.
3.[0..7]	Reserved	0h00	Reserved. Byte 3 value is 0h00.

The Scan Chain SCAN_DATA_IN bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel into serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform. Alternatively, an OCP NIC 3.0 card vendor may choose to

implement this chain using an active device (such as a microcontroller or CPLD), if it implements the function of the 74LV165, supporting circuitry for the Scan Chain and meets all the timing specifications given in this specification. For active device implementations, there is an associated device start-up time. Refer to Section 4.12 for details on the +3.3V_EDGE stable to the first data valid read in ID Mode.

The Scan Chain SCAN_DATA_IN shift register 0 shall be mandatory for scan chain implementations for the card present, WAKE_N and thermal threshold features. Scan Chain SCAN_DATA_IN shift registers 1, 2 & 3 are optional depending on the line side I/O and LED fields being reported to the host. Dual port LED applications require shift register 1. Quad port LED applications require shift registers 1 & 2. Octal port applications require shift registers 1, 2 & 3.

The host should read the Scan Chain SCAN_DATA_IN bus multiple times to qualify the incoming data stream. The number of data qualification reads is dependent on the baseboard implementation.

On the OCP NIC 3.0 card, a 1 kΩ pull up resistor shall be connected to the SER input of the last SCAN_DATA_IN shift register. Doing so ensures the default bit value of 0b1 for implementations using less than four shift registers.

Note: SCAN_DATA_IN is shifted out of the 74LV165 with MSB (bit 7) first, and LSB (bit 0) last. Refer to the timing diagrams in Figure 115 and Figure 116 for details.

Table 40: Pin Descriptions – Scan Chain SCAN_DATA_IN Bit Definition

Byte.bit	SCAN_DATA_IN Field Name	Default Value	Description
0.0	PRSNTB[0]_P#	0bX	PRSNTB[3:0]# bits shall reflect the same state as the signals on the Primary Connector. Connect these scan chain signals directly to the OCP NIC 3.0 card edge PRSNTB[3:0]# pins. The OCP NIC 3.0 implementer may alternatively choose to locally populate pull up and pull down resistors to these scan chain inputs as long as the PRSNTB[3:0]# values are the same on the scan chain and card edge.
0.1	PRSNTB[1]_P#	0bX	
0.2	PRSNTB[2]_P#	0bX	
0.3	PRSNTB[3]_P#	0bX	
0.4	WAKE_N / PRSNTB[4]#	0bX / 0bX	PCIe WAKE_N signal shall reflect the same state as the signal on the Primary Connector. For DSFF designs, this bit shall also serve as the PRSNTB[4]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 117 for details.
0.5	TEMP_WARN_N / PRSNTB[5]#	0b1 / 0bX /	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when the network silicon or transceiver module temperature sensors exceed the temperature warning threshold.

Byte.bit	SCAN_DATA_IN Field Name	Default Value	Description
			For cards that do not require temperature reporting, the TEMP_WARN_N value shall be statically set to 0b1. Refer to Section 5.3.1 for details on temperature reporting. For DSFF designs, this bit shall also serve as the PRSNTB[5]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 117 for details.
0.6	TEMP_CRIT_N / PRSNTB[6]#	0b1 / 0bX	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when the network silicon or transceiver module temperature sensors exceed the temperature critical threshold. For cards that do not require temperature reporting, the TEMP_CRIT_N value shall be statically set to 0b1. Refer to Section 5.3.1 for details on temperature reporting. For DSFF designs, this bit shall also serve as the PRSNTB[6]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 117 for details.
0.7	FAN_ON_AUX / PRSNTB[7]# /	0b0 / 0bX	When high, FAN_ON_AUX shall request the system fan to be enabled for extra cooling in Aux Power Mode. The FAN_ON_AUX bit shall be asserted when the network silicon or transceiver module cooling requested threshold has been exceeded. The temperature at which this assertion occurs is device dependent. The FAN_ON_AUX bit shall deassert when the network silicon or transceiver module temperature is at least 5 °C below the assertion threshold. 0b0 – The system fan is not requested/off in Aux Power Mode.

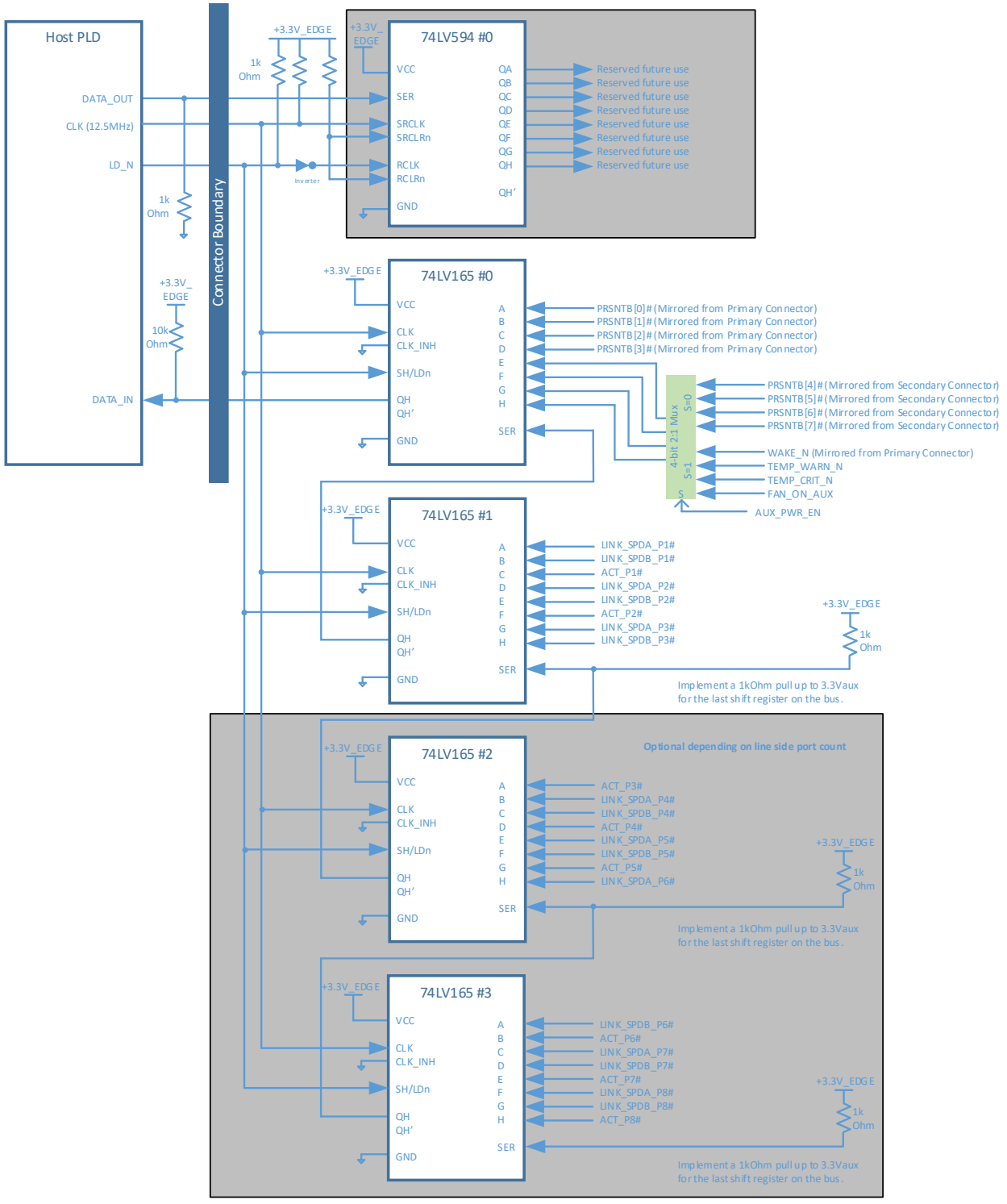
Byte.bit	SCAN_DATA_IN Field Name	Default Value	Description
			0b1 – The system fan is requested/on in Aux Power Mode. For cards that do not require temperature reporting, the FAN_ON_AUX value shall be statically set to 0b0. Refer to Section 5.3.1 for details on temperature reporting. For DSFF designs, this bit shall also serve as the PRSNTB[7]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 117 for details.
1.0	LINK_SPDA_P1#	0b1	Port 1 link and speed A indication (max speed). Active low. 0b0 – Link LED is illuminated on the host platform. 0b1 – Link LED is not illuminated on the host platform. **On** = link is detected on the port and is at the maximum speed. **Off** = the physical link is down, the link is not operating at the maximum speed or the port is disabled. Note: The link and speed A LED may also be blinked for use as port identification.
1.1	LINK_SPDB_P1#	0b1	Port 1 link and speed B indication (not max speed). Active low. 0b0 – Link LED is illuminated on the host. 0b1 – Link LED is not illuminated on the host. **On** = link is detected on the port and is not at the maximum speed. **Off** = the physical link is down, the link is operating at the maximum speed, or the port is disabled. Note: The link and speed B LED may also be blinked for use as port identification.
1.2	ACT_P1#	0b1	Port 1 activity indication. Active low. 0b0 – ACT LED is illuminated on the host.

Byte.bit	SCAN_DATA_IN Field Name	Default Value	Description
			0b1 – ACT LED is not illuminated on the host. **Blinking** = activity is detected on the port. The LED should blink at the rate of 0.5 Hz to 5 Hz. **Off** = no activity is detected on the port.
1.3	LINK_SPDA_P2#	0b1	Port 2 link and speed A indication (max speed). Active low.
1.4	LINK_SPDB_P2#	0b1	Port 2 link and speed B indication (not max speed). Active low.
1.5	ACT_P2#	0b1	Port 2 activity indication. Active low.
1.6	LINK_SPDA_P3#	0b1	Port 3 link and speed A indication (max speed). Active low.
1.7	LINK_SPDB_P3#	0b1	Port 3 link and speed B indication (not max speed). Active low.
2.0	ACT_P3#	0b1	Port 3 activity indication. Active low.
2.1	LINK_SPDA_P4#	0b1	Port 4 link and speed A indication (max speed). Active low.
2.2	LINK_SPDB_P4#	0b1	Port 4 link and speed B indication (not max speed). Active low.
2.3	ACT_P4#	0b1	Port 4 activity indication. Active low.
2.4	LINK_SPDA_P5#	0b1	Port 5 link and speed A indication (max speed). Active low.
2.5	LINK_SPDB_P5#	0b1	Port 5 link and speed B indication (not max speed). Active low.
2.6	ACT_P5#	0b1	Port 5 activity indication. Active low.
2.7	LINK_SPDA_P6#	0b1	Port 6 link and speed A indication (max speed). Active low.
3.0	LINK_SPDB_P6#	0b1	Port 6 link and speed B indication (not max speed). Active low.
3.1	ACT_P6#	0b1	Port 6 activity indication. Active low.
3.2	LINK_SPDA_P7#	0b1	Port 7 link and speed A indication (max speed). Active low.
3.3	LINK_SPDB_P7#	0b1	Port 7 link and speed B indication (not max speed). Active low.
3.4	ACT_P7#	0b1	Port 7 activity indication. Active low.
3.5	LINK_SPDA_P8#	0b1	Port 8 link and speed A indication (max speed). Active low.
3.6	LINK_SPDB_P8#	0b1	Port 8 link and speed B indication (not max speed). Active low.
3.7	ACT_P8#	0b1	Port 8 activity indication. Active low.

2805

4.5.6.6 Scan Chain Example Topology

Figure 117: Scan Chain Connection Example



4.5.7 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC and DC specifications are defined in the PCIe CEM Specification, Rev 5.0 and amended in Section 4.10. An example connection diagram is shown in Figure 118 for an SFF and Figure 119 for a DSFF.

For DSFF implementations, the form-factor is treated as single monolithic entity. The AUX_PWR_EN0, MAIN_PWR_EN0 and NIC_PWR_GOOD0 signals are used for power control of the entire card. These signals are associated with the Primary Connector. Power rails come from both the Primary and Secondary Connectors to obtain the full power budget as defined in Section 4.10.

+12V_EDGE and +3.3V_EDGE may be used from both connectors depending on the form factor, with the Primary Connector power pins as mandatory in all instances. For DSFF, power shall be simultaneously applied to both connectors.

Table 41: Pin Descriptions – Power (Per Connector)

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
GND	Various	GND	Ground return.
+12V_EDGE	B1, B2, B3, B4, B5, B6	Power	+12 V main or +12 V aux power; total of 6 pins per connector.
+3.3V_EDGE	B11	Power	+3.3 V main or +3.3 V aux power; total of 1 pin per connector.
AUX_PWR_EN0 / AUX_PWR_EN1	B12	Output	Aux Power enable. Active high.
MAIN_PWR_EN0 / MAIN_PWR_EN1	OCP_B2	Output	Main Power Enable. Active high.
NIC_PWR_GOOD0/ NIC_PWR_GOOD1	OCP_B1	Input	NIC Power Good. Active high. This signal is driven by the OCP NIC 3.0 card.

4.5.7.1 GND

A total of 46 ground pins are on the main 140-pin connector area. Additionally, a total of 4 ground pins are in the OCP bay area. Refer to Section 4.2 for details.

4.5.7.2 +12V_EDGE

The +12V_EDGE pins shall be rated to 1.1 A per pin with a maximum derated power delivery of 80 W.

The +12V_EDGE power pins shall be within the rail tolerances as defined in Section 4.10 when the PWR_EN pin is driven high by the baseboard.

The OCP NIC 3.0 card may optionally implement a fuse on +12V_EDGE to protect against electrical faults.

For DSFF, +12V_EDGE is available on both the Primary and Secondary Connectors. When a DSFF card is detected in the system, +12V_EDGE shall be simultaneously applied to both connectors.

4.5.7.3 +3.3V_EDGE

The +3.3V_EDGE pin shall be rated to 1.1 A for a maximum derated power delivery of 3.63 W.

The +3.3V_EDGE power pin shall be within the rail tolerances as defined in Section 4.10 when the PWR_EN pin is driven high by the baseboard.

The OCP NIC 3.0 card may optionally implement a fuse on +3.3V_EDGE to protect against electrical faults.

For DSFF, +3.3V_EDGE is available on both the Primary and Secondary Connectors. When a DSFF card is detected in the system, +3.3V_EDGE shall be simultaneously applied to both connectors.

4.5.7.4 AUX_PWR_EN[0:1]

This pin indicates that the baseboard +12V_EDGE and +3.3V_EDGE power are supplied per the Aux Power Mode requirements described in Section 4.10. Additionally, this signal notifies the OCP NIC 3.0 card to enable any power supplies that run only in the Aux Power Mode.

AUX_PWR_EN is pinned out on both the Primary and Secondary Connector. The AUX_PWR_EN0 connection shall be implemented on the Primary Connector only. For the DSFF, the AUX_PWR_EN1 connection on the Secondary Connector is reserved for a future use case. Leave AUX_PWR_EN1 as a no connect on the NIC side.

This signal shall be pulled down to GND through a 10 kΩ resistor on the baseboard. This ensures the OCP NIC 3.0 card power is disabled until instructed to turn on by the baseboard.

When low, the OCP NIC 3.0 card supplies running on aux power shall be disabled.

When high, the OCP NIC 3.0 card supplies running on aux power shall be enabled.

For OCP NIC 3.0 cards that do not use a separate “main power” domain circuitry (or can operate in a single power domain), the AUX_PWR_EN signal serves as the primary method to enable all the card power supplies.

For OCP NIC 3.0 cards that support the Programming Mode power state, the condition AUX_PWR_EN==0 and MAIN_PWR_EN==1 shall prevent the aux power supplies from being enabled. An example of this logic is shown in Figure 118.

It is expected that a baseboard will not drive signals other than SMBus and the Scan Chain to the OCP NIC 3.0 card when this signal is low.

4.5.7.5 MAIN_PWR_EN[0:1]

This pin indicates that the baseboard +12V_EDGE and +3.3V_EDGE power are supplied per the Main Power Mode requirements described in Section 4.10. Additionally, this signal notifies the OCP NIC 3.0 card to enable any power supplies that run only in the Main Power Mode.

MAIN_PWR_EN is pinned out on both the Primary and Secondary Connector. The MAIN_PWR_EN0 connection shall be implemented on the Primary Connector only. For the DSFF, the MAIN_PWR_EN1 connection on the Secondary Connector is reserved for a future use case. Leave MAIN_PWR_EN1 as a no connect on the NIC side.

The MAIN_PWR_EN pin is driven by the baseboard for normal operation and may only be asserted when AUX_PWR_EN and NIC_PWR_GOOD are already asserted. The MAIN_PWR_EN pin must be implemented on baseboard systems but may optionally be used to control main power rail power supplies by the OCP NIC 3.0 card depending on the end point silicon implementation. Depending on the silicon vendor, end point devices may be able to operate in a single power domain or may require separate power domains to function.

For OCP NIC 3.0 cards that support the Programming Mode power state, the condition AUX_PWR_EN == 0 and MAIN_PWR_EN == 1 shall prevent the main power supplies from being enabled. An example of this gating logic is shown in Figure 118.

For baseboard implementations, this signal shall be pulled down to GND through a 10 kΩ resistor on the baseboard. This ensures the OCP NIC 3.0 card power is disabled until instructed to turn on by the baseboard.

When low, the OCP NIC 3.0 card supplies running on main power shall be disabled.

When high, the OCP NIC 3.0 card supplies running on main power shall be enabled.

This pin may be left as a no connect for OCP NIC 3.0 cards that do not use a separate “main power” domain VR circuitry.

4.5.7.6 NIC_PWR_GOOD[0:1]

The NIC_PWR_GOOD[0:1] signals are used to indicate when the aux power domain, and main power domain rails are within operational tolerances.

NIC_PWR_GOOD is pinned out on both the Primary and Secondary Connector. The NIC_PWR_GOOD0 connection shall be implemented on the Primary Connector only. For the DSFF, the NIC_PWR_GOOD1 connection on the Secondary Connector is reserved for a future use case. Leave NIC_PWR_GOOD1 as a no connect on the NIC side.

Table 42 shows the expected NIC_PWR_GOOD state for power up sequencing. This is dependent on the values of AUX_PWR_EN, MAIN_PWR_EN and the enabled power domains operating within design tolerances.

Table 42: NIC_PWR_GOOD Pin States

AUX_PWR_EN	MAIN_PWR_EN	Enabled Power Domain Nominal	NIC_PWR_GOOD	State Name
0	0	N/A	0	ID Mode
1	0	Yes	1	Aux Power Mode
0	1	N/A	0	Programming Mode
1	1	Yes	1	Main Power Mode
1	0	No	0	Transition state (non-operational)
1	1	No	0	Transition state (non-operational)

Refer to the power up and power down sequencing diagrams (Figure 132 and Figure 133) for timing details.

Where appropriate, designs that have a separate Main Power domain should also connect to the main power good indication to the NIC_PWR_GOOD signal via a FET to isolate the domains. Refer to Figure 118 for an example implementation.

When low, this signal shall indicate that the OCP NIC 3.0 card power supplies are not yet within nominal tolerances or are in a fault condition after the power ramp times (T_{APL} and T_{MPL}) have expired.

For cards that support the Programming Mode power state, the NIC_PWR_GOOD signal shall remain low when the OCP NIC 3.0 card is in Programming Mode as both the Aux Power Mode and Main Power Mode power supplies are disabled. Programming Mode shall only be used on OCP NIC 3.0 cards that advertise that the Programming Mode power state is supported per Section 5.10.3.

For baseboards, this pin may be connected to the platform I/O hub as a NIC power health status indication. This signal shall be pulled down to ground with a 100 kΩ resistor on the baseboard to prevent a false power good indication if no OCP NIC 3.0 card is present.

For OCP NIC 3.0 cards this signal shall indicate the OCP NIC 3.0 card power is “good” for the given power mode. This signal may be implemented by combinatorial logic, a cascaded power good tree or a discrete power good monitor output.

When high, this signal should be treated as V_{REF} is available for NC-SI communications. Refer to timing parameter T4 in the DMTF DSP0222 specification for details.

4.5.7.7 Power Supply Pins Example Topology

Figure 118: Example SFF Power Supply Topology

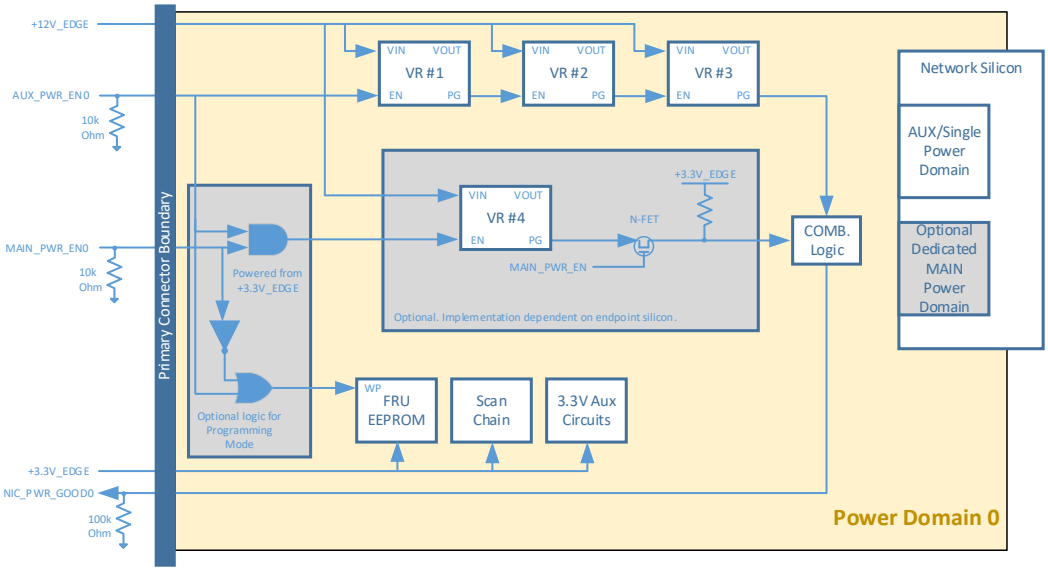
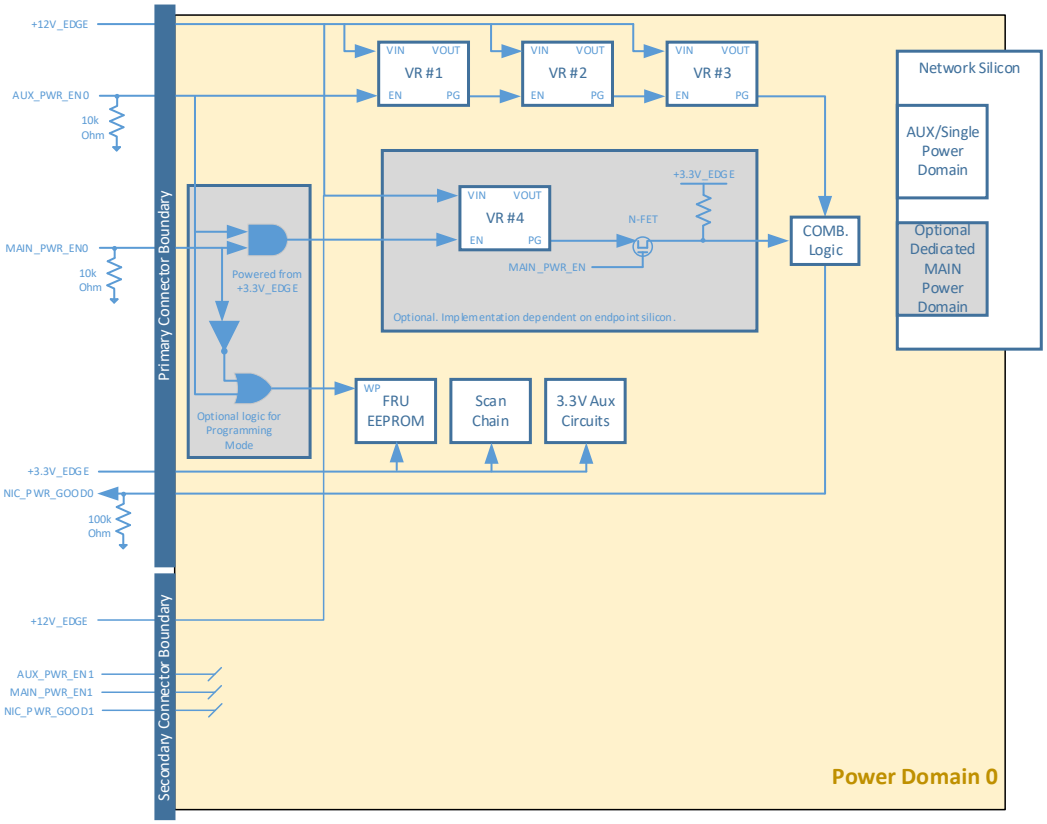


Figure 119: Example DSFF Power Supply Topology, Single Power Domain



4.5.8 USB 2.0 (A68/A69)

This section provides the pin assignments for the USB 2.0 interface signals. USB 2.0 is only defined for operation on the Primary Connector for the SFF. For DSFF, an additional USB bus is available on the 4C+ Secondary Connector as well. Refer to the Extended OEM Record 0xD2 for support indication.

USB 2.0 may be used for card manageability, as well as applications with end point silicon that requires a USB connection to the baseboard. Implementations may also allow for a USB-Serial or USB-JTAG translator for serial or JTAG applications. If multiple USB devices are required, an optional USB hub may be implemented on the OCP NIC 3.0 card. Downstream device discovery is completed as part of the bus enumeration per the USB 2.0 specification. A basic example connection diagram is shown in Figure 120. An example depicting USB-Serial and USB-JTAG connectivity with an USB hub is shown in Figure 121.

Note: The USB pins form an internal interface between the OCP NIC Card and the Baseboard. These signals are not meant to be directly connected to external devices outside of the system and may pose a security risk or expose the system to damage from ESD exposure.

Table 43: Pin Descriptions – USB 2.0 – 4C+ Connector only

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
USB_DAT[0:1]n USB_DAT[0:1]p	A68 A69	Bi-directional	USB 2.0 Differential Pair – Primary Connector Only.

4.5.8.1 USB_DAT[0:1]_p/n

A baseboard implementation shall provide a USB 2.0 connection to the OCP NIC 3.0 primary connector.

NIC implementations that require USB shall connect the bus to the end point silicon. This pin shall be left as a no connect if it is not used on the OCP NIC 3.0 card.

The USB pins shall be directly connected between the end point silicon or USB device and the card gold fingers.

When implemented, the Baseboard and NIC side USB interface shall be compliant to the electrical signaling requirements in the USB 2.0 specification. The USB interface shall be isolated by the Baseboard until AUX_PWR_EN=1 and the first rising edge NIC_PWR_GOOD=1. eUSB level interfaces are not supported facing the connector edge. Differential termination (V_{TERM}) pull-up values on the D+ line, if implemented, shall also be 3.3 V compliant. The OCP NIC 3.0 card may implement protection diodes and is up to the adapter vendor for placement.

To prevent leakage paths, a baseboard shall not use USB pull up resistors on the USB_DATp/n lines to indicate the bus data transmission rate. If used, pull up resistors shall only exist on the NIC side.

The AUX_PWR_EN0 signal may be used for downstream USB devices that require a V_{BUS} detection indication. Designers would have to ensure the V_{BUS} detection threshold supports 3.3 V signaling. Examples of this may include USB-serial converting devices.

Depending on the NIC architectural requirements, the USB bus may be required for operation in Aux Power Mode, Main Power Mode, or both. This is declared in the Extended OEM Record in Section 5.10.3.4.

4.5.8.2 USB Example Topology

Figure 120: USB 2.0 Connection Example – Basic Connectivity

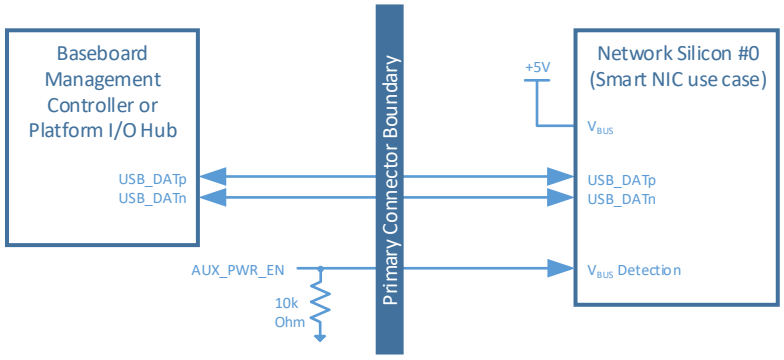
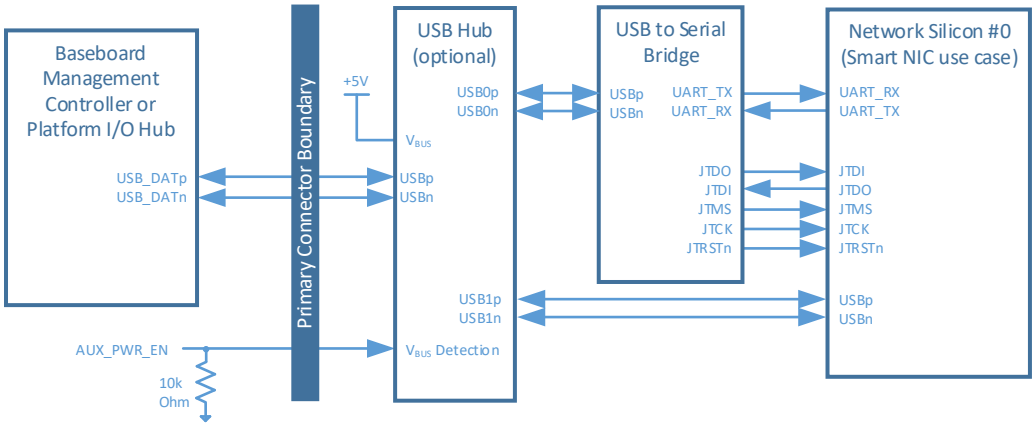


Figure 121: USB 2.0 Connection Example – USB-Serial / USB-JTAG Connectivity



4.5.9 RFU[1:4] Pins

This section provides the pin assignments for the RFU[1:4] interface signals.

Table 44: Pin Descriptions – RFU[1:4]

Signal Name (Primary / Secondary)	Pin #	Baseboard Direction	Signal Description
RFU1 / RFU3, N/C	B68	Input / Output	Reserved future use pins.
RFU2 / RFU4, N/C	B69		

4.5.9.1 RFU[1:4] Detailed Description

In this release of the OCP NIC 3.0 specification, the RFU[1:2] pins are defined on the Primary Connector. RFU[3:4] are defined on the Secondary Connector. These pins shall be left as no connect. A total of two reserved pins are available for the SFF; a total of four reserved pins are available for the DSFF cards.

4.6 PCIe Bifurcation Mechanism

OCP NIC 3.0 baseboards and OCP NIC 3.0 cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports are supported. The bifurcation mechanism also supports OCP NIC 3.0 cards with a single or multiple end points. These features are accomplished via the PRSTNB[7:0]# and BIF[5:0]# pins on the Primary and Secondary Connectors.

A high-level bifurcation connection diagram is shown in Section 4.5.2.4.

4.6.1 PCIe Present Configuration (PRSNTA[1:0]#, PRSNTB[7:0]#)

The OCP NIC 3.0 card configuration mechanism consists of up to eight dual use pins PRSNTB# pins and up to two PRSNTA# pins on the card edge. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities.

The signals PRSNTA0# and PRSNTB[3:0]# are associated with the Primary Connector. While PRSNTA1# and PRSNTB[7:4]# are associated with the Secondary Connector. PRSNTA[1:0]# signals are grounded on the baseboard. All of the PRSNTB[7:0]# pins are pulled up to +3.3V_EDGE on the baseboard and are active low signals.

4.6.1.1 SFF PRSNTA0#, PRSNTB[3:0]#

For an SFF card, the card side PRSNTA0# pin shall connect to one or more of the PRSNTB[3:0]# pins according to the bifurcation decoder defined in Section 4.6.3. The connections shall match the card PCIe link subdivision capabilities.

For an SFF slot, the baseboard shall read the PRSNTB[3:0]# pins associated with the Primary Connector. The default state of PRSNTB[3:0]#==0b1111 indicates that no card is present in the card slot. A value other than 0b1111 indicates that a card is present. The Baseboard shall use the look up table defined in Section 4.6.3 to determine the supported card PCIe link subdivisions.

4.6.1.2 DSFF PRSNTA, PRSNTB

For a DSFF card, the card side PRSNTA0# pin shall connect to the PRSNTB[3:0]# pins with an encoding of 0b0010. Similarly, the PRSNTA1# pin shall also connect PRSNTB[7:4]# with an encoding of 0b0010. This identifies the card as a DSFF.

For a DSFF slot, the baseboard shall read the PRSNTB[3:0]# pins associated with the Primary Connector, and read the PRSNTB[7:4]# pins associated with the Secondary Connector. The default state of PRSNTB[3:0]#==0b1111 and PRSNTB[7:4]#==0b1111 indicates that no card is present in the card slot. A value of PRSNTB[7:0]#==0b0010_0010 indicates that a DSFF card is present. For DSFF cards with only 16 PCIe lanes, the gold fingers are permitted to connect PRSNTB[3:0]#==0b0010 for a valid indication of a DSFF.

Unlike the SFF and LFF, a DSFF card does not have a predefined lookup table to determine the supported PCIe link subdivisions. Instead, the card declares its supported link subdivision table in the FRU EEPROM. When this encoding is detected, the baseboard shall read the OEM Records 0xD0, 0xD1 and 0xD2 to determine the PCIe link subdivision capabilities. Refer to Section 4.6.4 for the detection flow.

4.6.2 PCIe Card Bifurcation Configuration (BIF[5:0]#)

Up to six signals (BIF[5:0]#) are driven by the baseboard to notify requested bifurcation on the OCP NIC 3.0 card silicon. This allows the baseboard to set the lane configuration on the OCP NIC 3.0 card that supports multiple bifurcation options. Three BIF# pins exist on each connector. The BIF pin encoding is defined in Section 4.6.3.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table 45 and indicate to the SFF OCP NIC 3.0 card silicon to setup a 4 x4 configuration. The values shown in Table 45 show the BIF pin electrical levels for the 3.3V logic. '0' is an electrical low, '1' is an electrical high.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

4.6.2.1 SFF BIF[2:0]#

For an SFF card that supports bifurcation, the card shall use the BIF[2:0]# pins from the Primary connector according to the bifurcation decoder defined in Section 4.6.3. The BIF encoding values shall match the card PCIe link subdivision capabilities.

For an SFF slot, the baseboard may assert the appropriate BIF pin encoding to obtain the requested bifurcation mode associated with the Primary Connector. The Baseboard shall use the look up table defined in Section 4.6.3 to determine the supported card PCIe link subdivisions. Asserting invalid BIF values may result in undefined behavior.

4.6.2.2 DSFF BIF[5:0]

For a DSFF card that supports bifurcation, the card shall use the BIF[2:0]# pins from the Primary connector and BIF[5:3]# pins from the Secondary Connector. The BIF encoding values shall match the card PCIe link subdivision capabilities.

Unlike the SFF and LFF, a DSFF card does not have a predefined lookup table to determine the supported PCIe link subdivisions. Instead, the card declares its supported link subdivision table in the FRU EEPROM, including the BIF encoding. When a DSFF card is detected by the PRSNTA[7:0]# bits, the baseboard shall read the OEM Records 0xD0, 0xD1 and 0xD2 to determine the PCIe link subdivision capabilities. Refer to Section 4.6.4 for the detection flow.

Additionally, the BIF encoding width may be three or six bits wide. The encoding width is declared in OEM Record 0xD2. If the encoding width is set to 6 bits, the BIF values are driven to both the Primary and Secondary Connectors. If the encoding width is set to 3 bits, the BIF value is to driven to both connectors as well, but the BIF encoding is applicable on a per connector basis. This allows for cards to configure PCIe Link Subdivision across all 32 lanes or configured PCIe link subdivision as x16 data slices independently for the Primary and Secondary Connectors.

For the DSFF, the BIF[5:0] pin encoding is declared in the 0xD0 and 0xD1 OEM Records. The baseboard shall read the OEM record and assert the BIF encoding to obtain the requested card side bifurcation. Refer to Section 4.6.4 for the detection flow.

4.6.3 PCIe Bifurcation Decoder

For the SFF, the combination of the PRSNTB# and BIF# pins deterministically set the PCIe lane width for a given combination of baseboard and OCP NIC 3.0 cards. Table 45 shows the resulting number of PCIe links and its width for known combinations of baseboards and OCP NIC 3.0 cards. A copy of this bifurcation decoder, which includes the detailed PCIe lane, PERST# and REFCLCK assignments, is available on the OCP NIC 3.0 Wiki site. Please refer to: https://www.opencompute.org/wiki/Server/NIC.

For the DSFF, OEM record 0xD0, 0xD1 and 0xD2 needs to be read by the baseboard in ID Mode. Record 0xD1 is implemented if the card side independently configures PCIe lanes 0-15 and 16-31. The record contains the required BIF assertion to select a PCIe bifurcation mode. These values are not static (like those found in the SFF/LFF implementations). Instead, these values are declared by the card.

Note 1: Baseboard vendors do not have to support the full complement of cases enumerated in the bifurcation table. Instead, baseboard vendors may choose to support only a subset of cases that is applicable to their hardware topology.

Note 2: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the OCP NIC 3.0 card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.

Note 3: Due to separate PCIe REFCLKs and power state timing differences in multi-host configurations, Table 45 shows the expected resulting links for a given baseboard and OCP NIC 3.0 card combination.

3114

Table 45: PCIe Bifurcation Decoder for x32, x16, x8, x4, x2 and x1 Card Widths

								Single Host				Dual Host				Dual Host	
				SFF (2C+/4C+): Host CPU Sockets -->	1 Upstream Socket	2 Upstream Sockets	4 Upstream Sockets	4 Sockets First 8 PCIe lanes	This configuration is not applicable for SFF -32 lanes is only available in the LFF implementation.	This configuration is not applicable for SFF -32 lanes is only available in the LFF implementation.	2 Upstream Sockets (1 Socket per Host)	This configuration is not applicable for SFF -32 lanes is only available in the LFF implementation.	4 Upstream Sockets (1 Socket per Host)	4 Sockets (1 Socket per Host) First 8 PCIe lanes
				SFF: Total PCIe Links (1 connector) -->	1, 2, or 4 Links	2 Links	4 Links	4 x2 links	1 Link (No Bifurcation)	1, 2, or 4 Links	2 Links	4 Links	4 Links	4 x2 links
				LFF: Host CPU Sockets -->	2 Upstream Sockets	4 Upstream Sockets (2 sockets per host)	8 Upstream Sockets (Note 1)	8 Upstream Sockets First 8 PCIe lanes per connector (Note 1)	1 Upstream Socket	2 Upstream Sockets (1 Socket per Host)	4 Upstream Sockets (2 Socket per Host)	4 Upstream Sockets (1 socket per Host)	8 Upstream Sockets (2 Socket per Host) (Note 1)	8 Upstream Sockets (2 Socket per Host) First 8 PCIe lanes per connector (Note 1)
				LFF: Total PCIe Links (Across 2 connectors) -->	1, 2, 4, or 8 Links	4 Links	8 Links	8 x2 links	1 Link (No Bifurcation)	1, 2, or 4 Links	4 Links	4 Links	8 Links	8 x2 links
				System Link Width Support per Connector -->	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	4 x4, 4 x2, 4x1	4 x2, 4 x1	1 x32 (w/back connector) 1 x16, 1 x8, 1 x4, 1 x2, 1 x1	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	2 x8, 2 x4, 2 x2, 2 x1	4 x4, 4 x2, 4 x1		4 x2, 4 x1
	Network Card - Supported PCIe Configurations			Primary Connector BIF[2:0]# (SFF & LFF) -->	0b000	0b001	0b010	0b011	0b100	0b100	0b101	0b110	0b110	0b111
				Secondary Connector BIF[2:0]# (LFF only) -->	0b000	0b001	0b010	0b011	0b000	0b100	0b101	0b101	0b110	0b111
Min Card Width	Card Short Name	Supported Bifurcation Modes	Primary Connector PRSNTB[3:0]# (SFF, LFF) Secondary Connector PRSNTB[3:0]# (LFF only)													
n/a	Not Present	Card Not Present	0b1111 (not used) 0b1111 (not used)													
SFF 2C+	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110 0b1111 (not used)	1 x8	1 x8 (Socket 0 only)	1 x4 (Socket 0 only)	1 x2 (Socket 0 only)	-	-	-	1 x8 (Host 0 only)	-	1 x4 (Host 0 only)	1 x2 (Host 0 only)
SFF 2C+	1 x4	1 x4, 1 x2, 1 x1	0b1110 0b1111 (not used)	1 x4	1 x4 (Socket 0 only)	1 x2 (Socket 0 only)	1 x2 (Socket 0 only)	-	-	-	1 x4 (Host 0 only)	-	1 x4 (Host 0 only)	1 x2 (Host 0 only)
SFF 2C+	1 x2	1 x2, 1 x1	0b1110 0b1111 (not used)	1 x2	1 x2 (Socket 0 only)	1 x2 (Socket 0 only)	1 x2 (Socket 0 only)	-	-	-	1 x2 (Host 0 only)	-	1 x2 (Host 0 only)	1 x2 (Host 0 only)
SFF 2C+	1 x1	1 x1	0b1110 0b1111 (not used)	1 x1	1 x1 (Socket 0 only)	1 x1 (Socket 0 only)	1 x1 (Socket 0 only)	-	-	-	1 x1 (Host 0 only)	-	1 x1 (Host 0 only)	1 x1 (Host 0 only)
SFF 2C+	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101 0b1111 (not used)	1 x8	1 x8 (Socket 0 only)	2 x4 (Socket 0 & 1)	2 x2 (Socket 0 & 2 only) (Note 4)	-	-	-	1 x8 (Host 0 only)	-	2 x4 (Host 0 & 1)	2 x2 (Host 0 & 2 only) (Note 4)
SFF 4C+	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101 0b1111 (not used)	2 x8	2 x8	4 x4	2 x2 (Socket 0 & 2 only) (Note 4)	-	-	-	2 x8 (Host 0 & 1)	-	4 x4	2 x2 (Host 0 & 2 only) (Note 4)
SFF 2C+	1 x8 Option D	1 x8, 1 x4 2 x4, 1 x2, 1 x1 4 x2 (First 8 lanes), 4 x1	0b1100 0b1111 (not used)	1 x8	1 x8 (Socket 0 only)	2 x4 (Socket 0 & 1)	4 x2	-	-	-	1 x8 (Host 0 only)	-	2 x4 (Host 0 & 1)	4 x2
SFF 2C+	4 x2	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100 0b1111 (not used)	1 x16	2 x8	4 x4	4 x2	4 x2	-	-	2 x8 (Host 0 & 1)	-	4 x4	4 x2
RSVD	1 x16 Option D	RSVD	0b1011 (not used) 0b1111 (not used)	-	-	-	-	-	-	-	-	-	-	-
SFF 4C+	1 x16 Option A	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1000 0b1111 (not used)	2 x4	1 x4 (Socket 0 only)	2 x4 (Socket 0 & 1)	2 x2 (Socket 0 & 2 only) (Note 4)	-	-	-	1 x4 (Host 0 only)	-	2 x4 (Host 0 & 1)	2 x2 (Host 0 & 2 only) (Note 4)
SFF 2C+	2 x4	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001 0b1111 (not used)	2 x2	1 x2 (Socket 0 only)	2 x2 (Socket 0 & 1)	4 x2	-	-	-	1 x2 (Host 0 only)	-	2 x2 (Host 0 & 1)	4 x2
SFF 2C+	4 x2	RSVD for fixture x8	0b1000 (not used) 0b1111 (not used)	-	-	-	-	-	-	-	-	-	-	-
SFF 4C+	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111 0b1111 (not used)	1 x16	1 x8 (Socket 0 only)	1 x4 (Socket 0 only)	1 x2 (Socket 0 only)	-	-	-	1 x8 (Host 0 only)	-	1 x4 (Host 0 only)	1 x2 (Host 0 only)
SFF 4C+	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110 0b1111 (not used)	2 x8	2 x8	2 x4 (Socket 0 & 2 only) (Note 4)	2 x2 (Socket 0 only)	-	-	-	2 x4 (Host 0 & 1)	-	2 x4 (Host 0 & 2 only)	2 x2 (Host 0 only)
SFF 4C+	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101 0b1111 (not used)	1 x16	2 x8	2 x4 (Socket 0 & 2 only) (Note 4)	1 x2 (Socket 0 only)	-	-	-	2 x8 (Host 0 & 1)	-	2 x4 (Host 0 & 2 only)	1 x2 (Host 0 only)
SFF 4C+	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100 0b1111 (not used)	1 x16	2 x8	4 x4	2 x2 (Socket 0 & 2 only) Note 4	-	-	-	2 x8 (Host 0 & 1)	-	4 x4	2 x2 (Host 0 & 2 only) Note 4
SFF 4C+	4 x4	4 x4, 4 x2, 4 x1	0b0011 0b1111 (not used)	4 x4	2 x4 (EP 0 and 2 only)	4 x4	1 x2 (Socket 0 only)	-	-	-	2 x4 (Host 0 & 1)	-	4 x4	1 x2 (Host 0 only)
LFF	2x16 Option A	2x 16, 2 x8, 2 x4, 2 x2, 2 x1	0b0111 0b1111	2 x16	2 x8 (Socket 0 & 2 only)	2 x4 (Socket 0 & 4 only)	2 x2 (Socket 0 & 4)	1 x16	2 x16	2 x16	2 x8 (Host 0 & 2)	2 x8 (Host 0 & 2)	2 x4 (Socket 0 on each Host 0 & 2)	2 x2 (Socket 0 on each Host 0 & 2)
LFF	4 x8 Option A	4 x8, 4 x4, 4 x2, 4 x1	0b0110 0b1111	4 x8	4 x8	4 x4 (Sockets 0, 2, 4 & 6)	2 x2 (Sockets 0 & 4)	1 x8	4 x8	4 x8	4 x8	4 x8	4 x4 (Socket 0 on each Host 0, 1, 2 & 3)	2 x2 (Socket 0 on each Host 0 & 2)
LFF	2 x16 Option B	2 x16, 2 x8, 2 x4, 2 x2, 2 x1 4 x8, 4 x4, 4 x2, 4 x1	0b0101 0b1111	2 x16	4 x8	4 x8 (Sockets 0, 2, 4 & 6)	2 x2 (Sockets 0 & 4)	1 x16	2 x16	4 x8	4 x8	4 x8	4 x4 (Socket 0 on each Host 0, 1, 2 & 3)	2 x2 (Host 0 & 2)
LFF	2 x16 Option C	2 x16, 2 x8, 2 x4, 2 x2, 2 x1 4 x8, 4 x4, 4 x2, 4 x1 8 x4, 8 x2, 8 x1	0b0100 0b1111	2 x16	4 x8	8 x4 (Note 1)	4 x2 (Sockets 0, 2, 4 & 6)	1 x16	2 x16	4 x8	4 x8	4 x8	8 x4 (Note 1)	2 x2 (Host 0 & 2)
RSVD	1 x32 Option A	RSVD	0b0001 (not used) 0b1111 (not used)	-	-	-	-	-	-	-	-	-	-	-
LFF	1 x32 Option A	1 x32 1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x 16, 2 x8, 2 x4, 2 x2, 2 x1 4 x8, 4 x4, 4 x2, 4 x1 8 x4, 8 x2, 8 x1	0b0000 0b1111	2 x16	4 x8	8 x4 (Note 1)	4 x2 (Sockets 0, 2, 4 & 6)	1 x32	2 x16	4 x8	4 x8	8 x4 (Note 1)	2 x2 (Host 0 & 2)
LFF	1 x32 Option B	1 x32 1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0000 0b0001	1 x16	1 x8 (Socket 0 only)	1 x4 (Socket 0 only)	1 x2 (Socket 0 only)	1 x32	1 x16 (Socket 0 only)	1 x8 (Host 0 only)	1 x8 (Host 0 only)	1 x4 (Host 0 only)	1 x4 (Host 0 only)	1 x2 (Host 0 only)
DSFF	DSFF	Read FRU EEPROM	0b0010	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM	Read FRU EEPROM

3115

4.6.4 Bifurcation Detection Flow

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and OCP NIC 3.0 card configurations.

- The baseboard shall read the state of the PRSNTB[3:0]# pins for the Primary Connector and the state of the PRSNTB[7:4]# pins on the Secondary Connector (if applicable).
  - An OCP NIC 3.0 card is present in the system if the resulting value is not 0b1111 on the Primary Connector, and, if applicable, not 0b1111 on the Secondary Connector.
- Firmware determines the OCP NIC 3.0 card PCIe lane width capabilities per Table 45 by reading the PRSNTB[3:0]# pins.
- **SFF Cards:**
  - The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card. This information is decoded from Section 4.6.3.
- **DSFF Cards:**
  - If PRSNTB[7:0]#==0b0010_0010, a D-SFF card is present in the system. For DSFF cards with only 16 PCIe lanes, the gold fingers are permitted to connect PRSNTB[3:0]#==0b0010 for a valid indication of a DSFF. The PCIe Link Subdivision capabilities are advertised on the card FRU EEPROM at OEM Record 0xC0, 0xD0 and optionally 0xD1.
- For cases where the baseboard request a link subdivision override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[2:0]# pins shall be asserted as appropriate based on the decoding table in Section 4.6.3 or the FRU EEPROM (for the DSFF case). Asserting the BIF[2:0]# pins assumes the OCP NIC 3.0 card supports the requested link override.
  - Note: For cards that are already powered up, BIF[2:0]# reconfiguration requires a transition back to ID Mode. During this transition, the card power rails are inactive and manageability links may be briefly lost due to the RBT isolation state.
- The BIF[2:0]# pins must be in their valid states upon the assertion of AUX_PWR_EN. The BIF[2:0]# pins shall remain static after AUX_PWR_EN is asserted. The pins are not allowed to change states when the OCP NIC 3.0 card is powered on.
- AUX_PWR_EN is asserted. An OCP NIC 3.0 card is allowed a max ramp time T_{APL} between AUX_PWR_EN assertion and NIC_PWR_GOOD assertion.
- MAIN_PWR_EN is asserted. An OP NIC 3.0 card is allowed a max ramp time T_{MPL} between MAIN_PWR_EN assertion and NIC_PWR_GOOD reassertion. For cards that do not have a separate Aux and Main power domain, this state is an unconditional transition to NIC_PWR_GOOD.
- The PCIe REFCLK shall become valid a minimum of 100 µs before the deassertion of PERST#.
- PERST# shall be deasserted >1 s after NIC_PWR_GOOD assertion as defined in Figure 132. Refer to Section 4.12 for timing details.

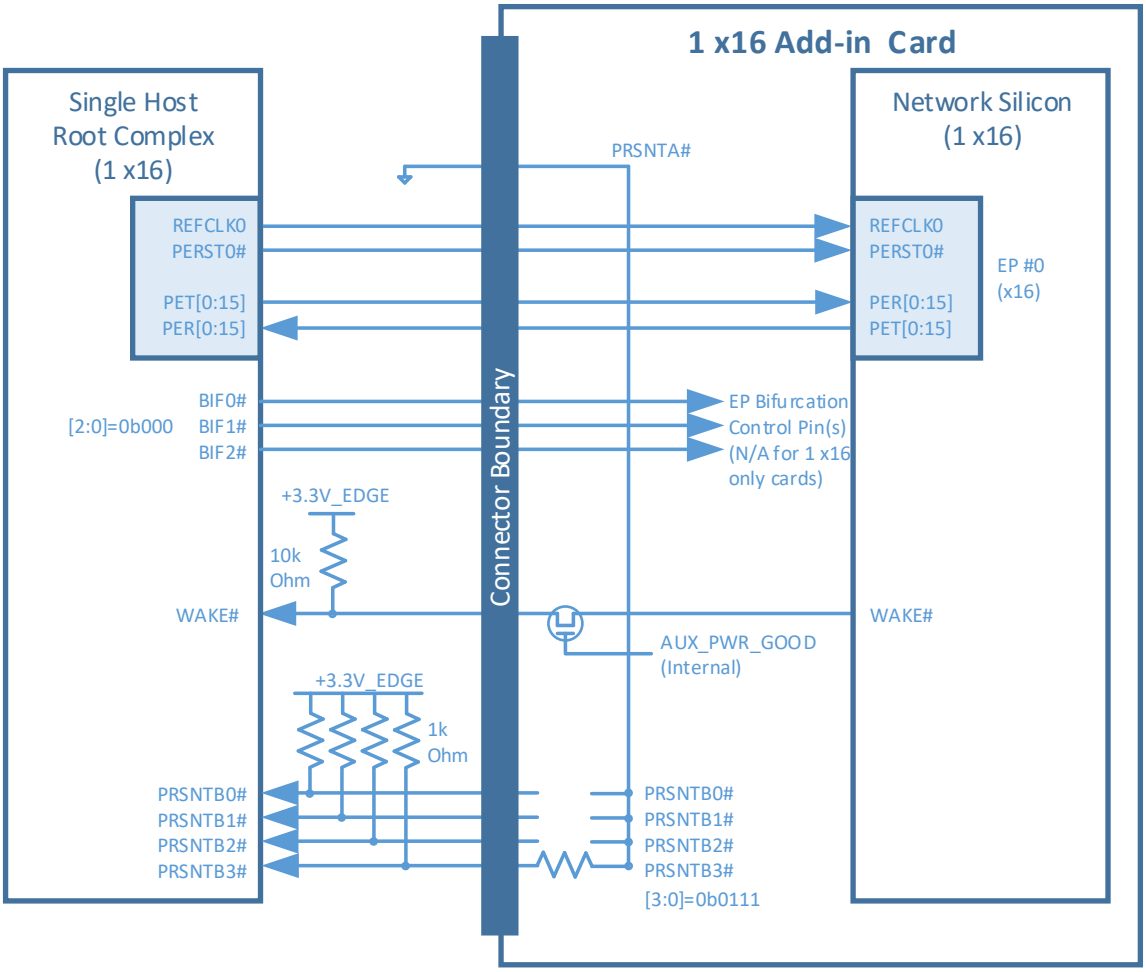
4.6.5 PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations using an SFF.

4.6.5.1 Single Host (1 x16) Baseboard with a 1 x16 OCP NIC 3.0 Card (Single Controller)

Figure 122 illustrates a single host baseboard that supports x16 with a single controller OCP NIC 3.0 card that also supports x16. The PRSNTB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 to set the card as a 1x16 for bifurcation capable controllers. For controllers without bifurcation support, the BIF[2:0] pin connections are not required on the card. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

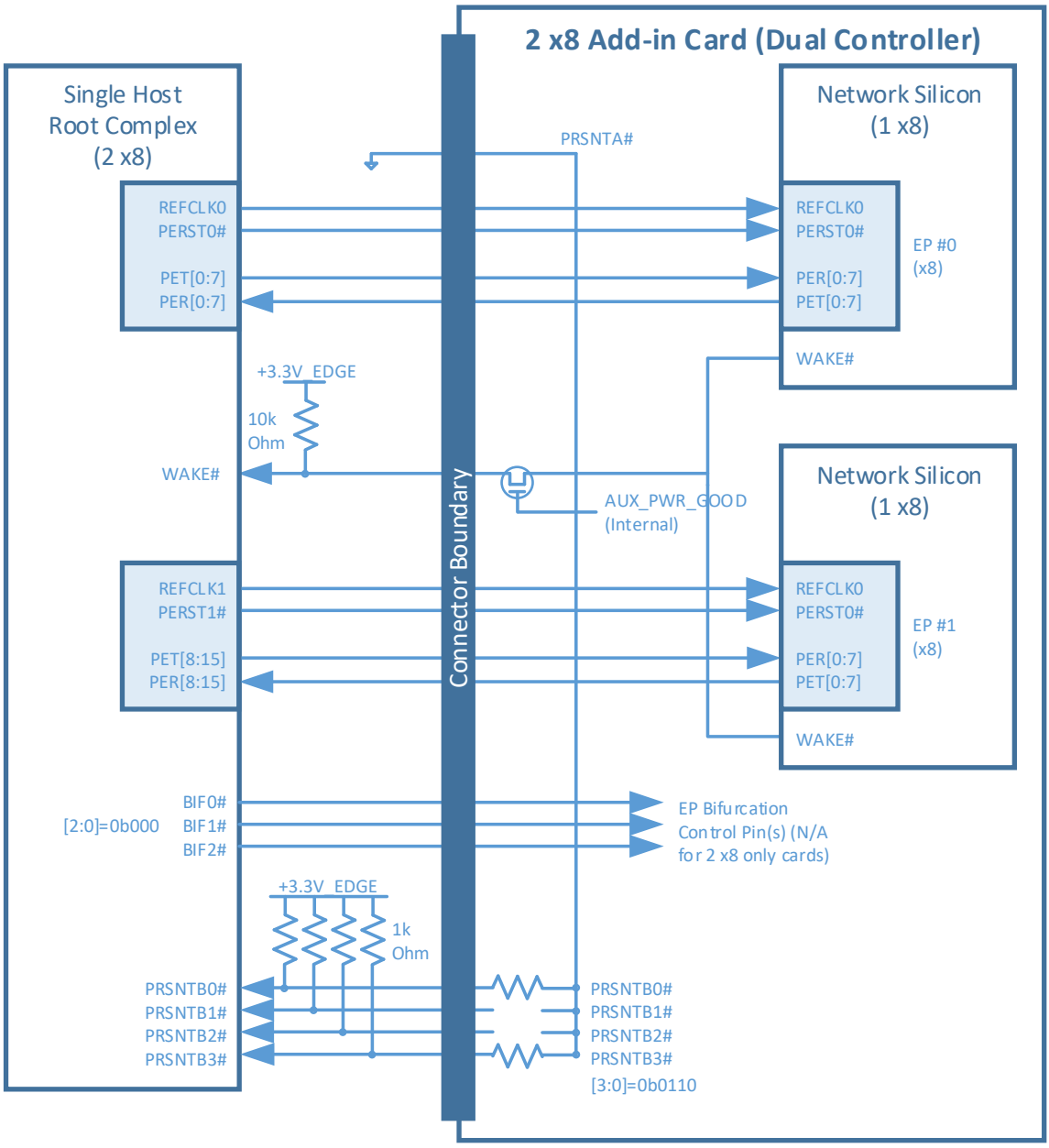
Figure 122: Single Host (1 x16) and 1 x16 OCP NIC 3.0 Card (Single Controller)



4.6.5.2 Single Host (2 x8) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controllers)

Figure 123 illustrates a single host baseboard that supports 2 x8 with a dual controller OCP NIC 3.0 card that also supports 2 x8. The PRSNTB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b000 in this example because the network card only supports a 2x8. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

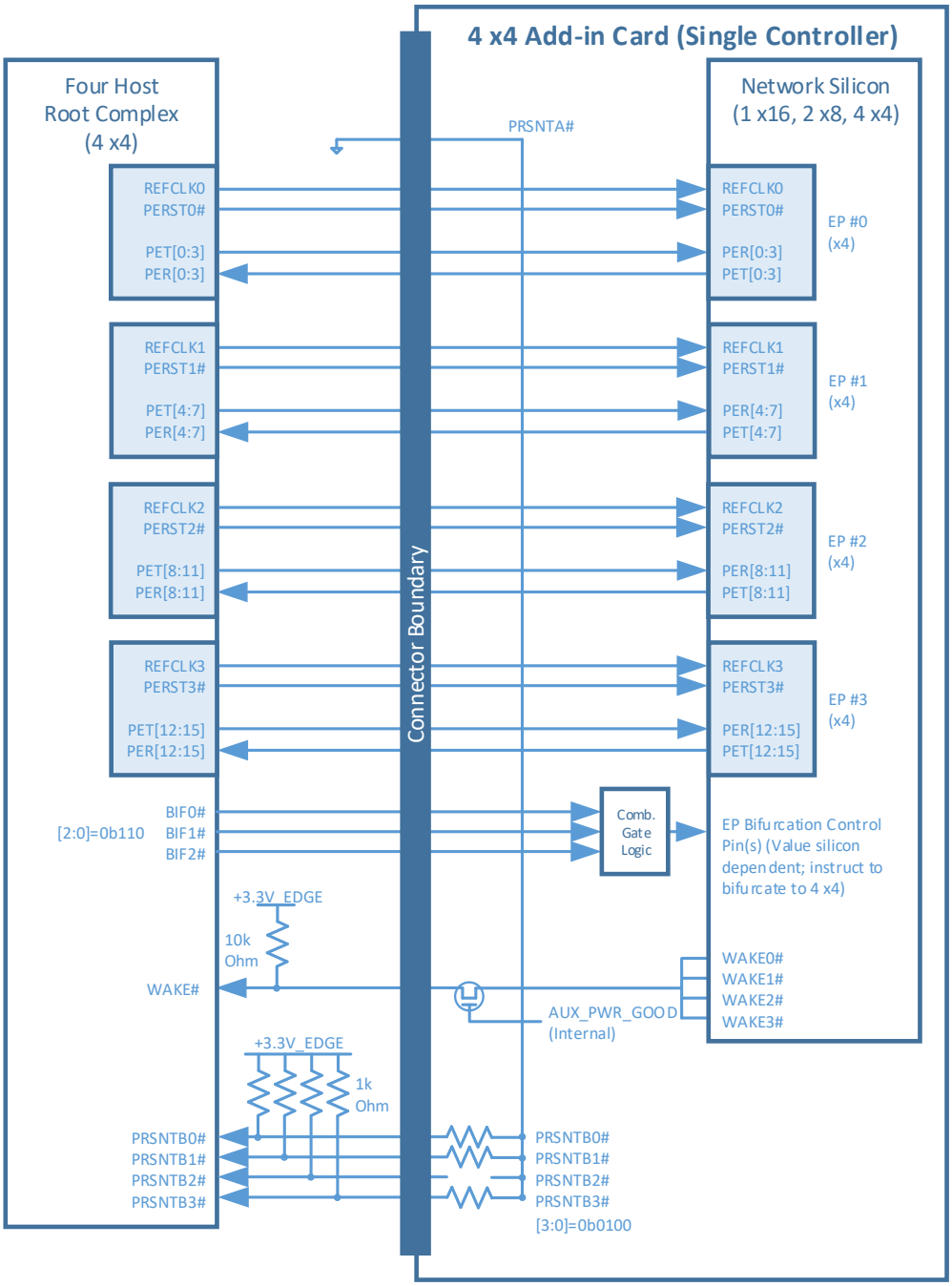
Figure 123: Single Host (2 x8) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)



4.6.5.3 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Single Controller)

Figure 124 illustrates a quad host baseboard that supports 4 x4 with a single controller OCP NIC 3.0 card that supports 1 x16, 2 x8 and 4 x4. The PRSNTB[3:0]# state is 0b0100. The BIF[2:0]# state in this example is 0b110 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

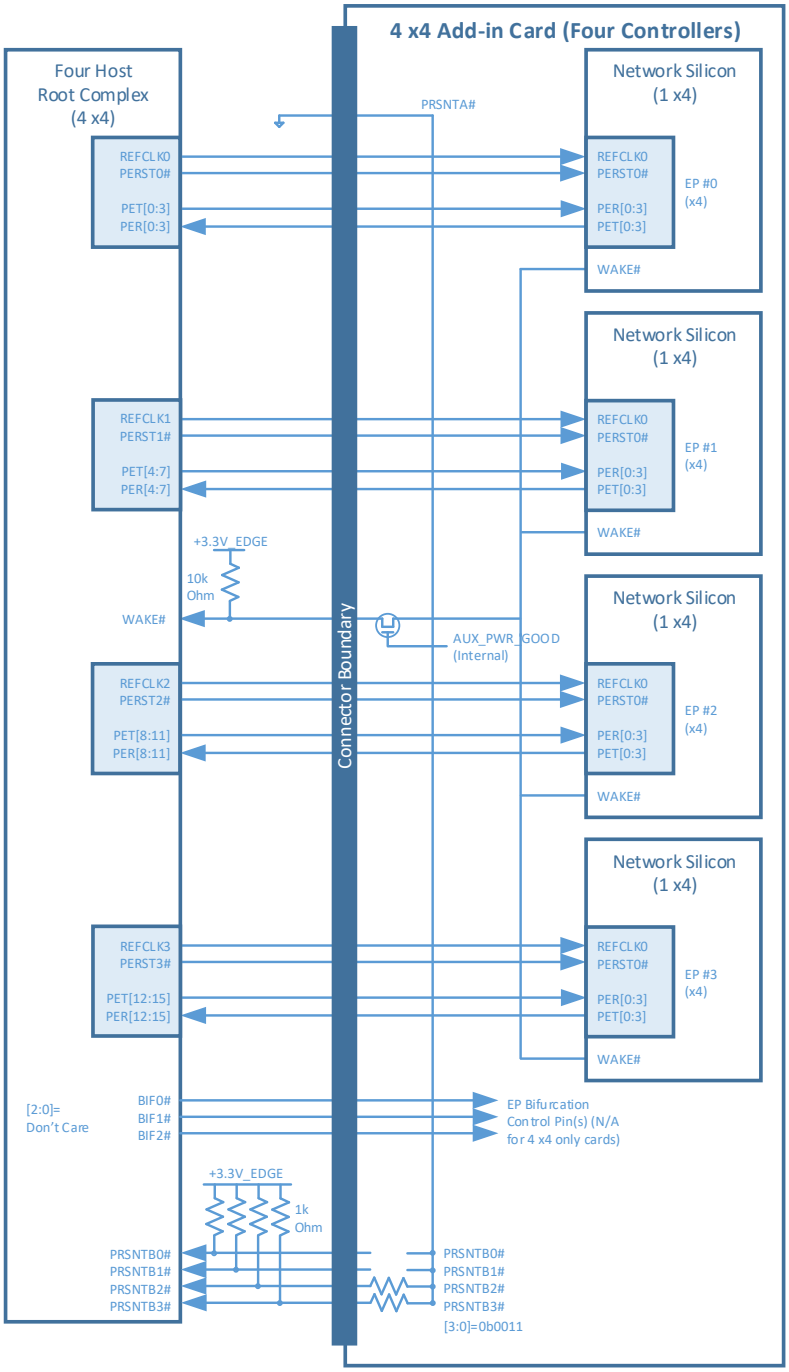
Figure 124: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Single Controller)



4.6.5.4 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Quad Controllers)

Figure 125 illustrates a quad host baseboard that supports 4 x4 with a quad controller OCP NIC 3.0 card that supports 4 x4. The PRSNTB[3:0]# state is 0b0011. The BIF[2:0]# state is a don't care value as there is no need to instruct the end-point network controllers to a specific bifurcation (each controller only supports 1x4 in this example). The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

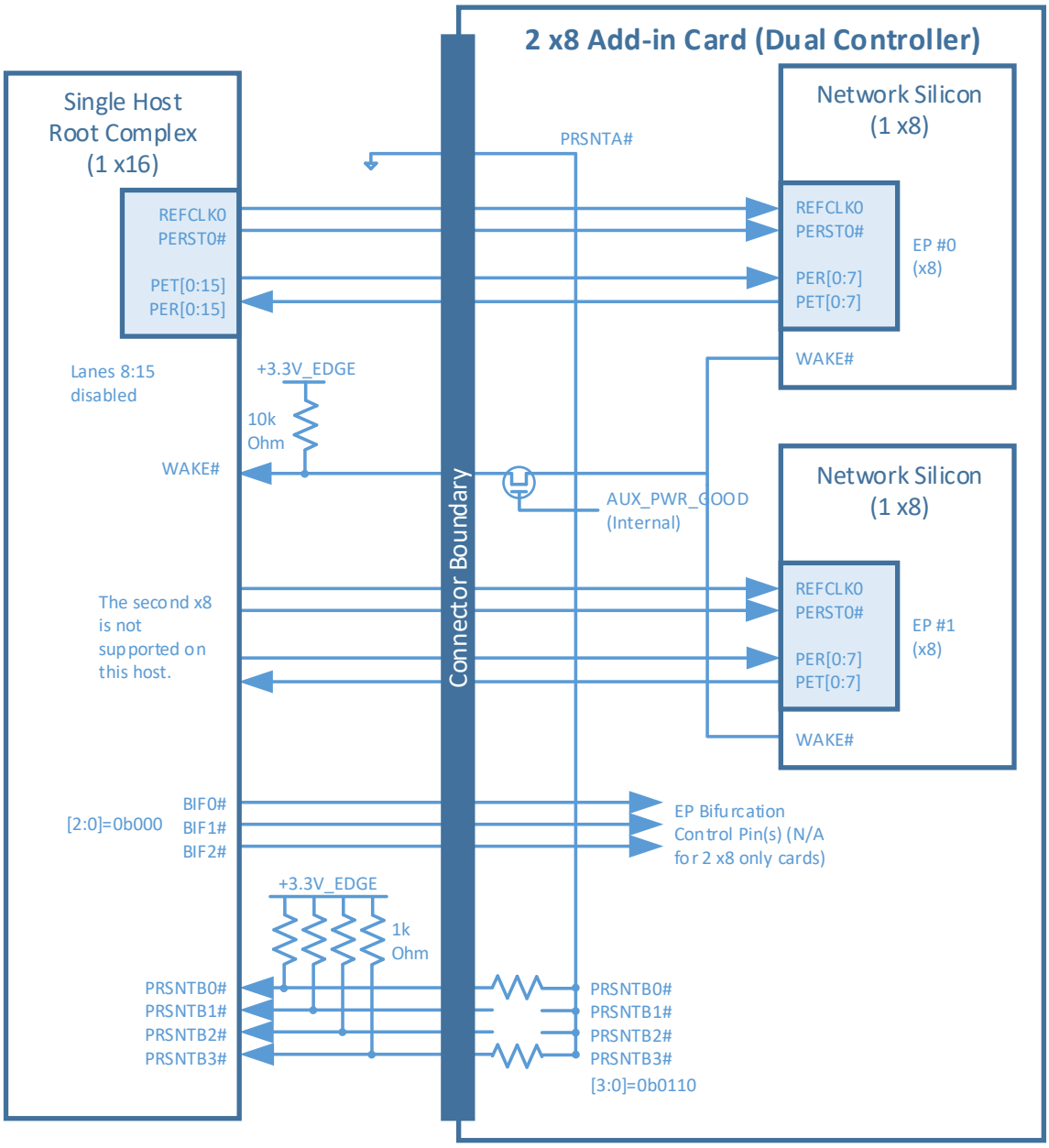
Figure 125: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Quad Controllers)



4.6.5.5 Single Host (1 x16, no Bifurcation) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controller)

Figure 126 illustrates a single host baseboard that supports 1 x16 with a dual controller OCP NIC 3.0 card that supports 2 x8. The PRSNTB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b000 as each silicon instance only supports 1x8. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The quad host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.

Figure 126: Single Host with no Bifurcation (1 x16) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)



4.6.6 DSFF Bifurcation Discovery

For DSFF, the PCIe link subdivision discovery fundamentally differs from the SFF implementations. The card no longer relies on a static bifurcation table as defined in Section 4.6.3. Instead, the FRU EEPROM contains OEM records that describe the supported PCIe link modes and BIF pin encoding values to enter each mode. This allows for baseboards to dynamically discover supported PCIe modes.

A DSFF card may be identified with the PRSNTB encoding. The DSFF encoding is defined to be PRSNTB[7:0]#==0b0010_0010. For DSFF cards with only 16 PCIe lanes, the gold fingers are permitted to connect PRSNTB[3:0]#==0b0010 for a valid indication of an DSFF. Once this PRSNTB encoding is discovered, the baseboard shall read the FRU EEPROM records 0xC0 (Base OEM Record), 0xD2 (Extended OEM Record) to further identify the DSFF OCP NIC 3.0 card capabilities. Record 0xD2 indicates if the PCIe link subdivision is described as a 32-lanes entity (as a single record) or split across two OEM records – each describing independent operation of each x16 data slice. The PCIe link subdivision records are described in 0xD0 (DSFF PCIe Link Subdivision Record 0) and 0xD1 (DSFF PCIe Link Subdivision Record 1).

4.7 PCIe REFCLK and PERST# Mapping

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs and PERST# signals on the Primary Connector and up to four additional PCIe REFCLKs and PERST# signals on the Secondary Connector. The association of each REFCLK and PERST# is based on the card PCIe Link number and is shown in Table 46. DSFF cards that implement both the Primary and Secondary Connectors have a total of up to eight REFCLKs/PERST# signals.

REFCLK[0:3] and PERST[0:3]# are defined for use in this release of the specification for the SFF only. REFCLK[4:7] and PERST[4:7]# are only used in the DSFF Secondary Connector implementations. The following tables enumerate the REFCLK and PERST# mapping for SFF cards for 1, 2 and 4 links and DSFF cards for 1, 2, 4 and 8 links. For DSFF with 8 links, no 1:2 clock driver circuit is required.

Asymmetric link combinations are also supported for the DSFF. For example, a x16x8x8. The link numbering, and PERST/REFCLK mapping from the Baseboard side is defined in Table 48. The NIC side silicon may use any of the clocks that are available.

For multi-host use cases, the baseboard may require a multiplexer circuit to direct the Host 1, Host 2 PCIe reference clock to the connector REFCLK1 signal to maintain proper REFCLK associations for a card with two links. Refer to the diagrams in Section 4.7.3.

Table 46: PCIe REFCLK and PERST Associations

REFCLK #	PERST #	Description	Availability (Connector)
REFCLK0	PERST0#	Associated with Link 0.	Primary Connector only.
REFCLK1	PERST1#	Associated with Link 1.	Primary Connector only.
REFCLK2	PERST2#	Associated with Link 2.	Primary Connector only.
REFCLK3	PERST3#	Associated with Link 3.	Primary Connector only.
REFCLK4	PERST4#	Associated with Link 4.	Secondary Connector only.
REFCLK5	PERST5#	Associated with Link 5.	Secondary Connector only.
REFCLK6	PERST6#	Associated with Link 6.	Secondary Connector only.
REFCLK7	PERST7#	Associated with Link 7.	Secondary Connector only.

4.7.1 SFF REFCLK and PERST# Requirements

Table 47 shows the Link/REFCLK/PERST# mapping requirements with respect to an SFF platform.

The SFF Link, REFCLK and PERST# connectivity shall meet the following requirements:

- PERST and REFCLK associations shall belong to the same index as defined in Table 46.
  - For example, REFCLK0/PERST0# is permitted, but REFCLK0/PERST2# is not.
- All clocks shall start on a x4 boundary.
  - For example, a silicon device may have the REFCLK associated with lane 0, lane 4, lane 8, etc.
- Within each x16 connector, links are permitted to be x16, x8, x4 in width.
  - Asymmetric subdivisions, such as [1x4, 2x2, 1x8] are permitted within the x16.
  - This specification does not provide an exhaustive list.
- Link widths may be smaller than x4 within a x4 clock boundary.
  - Widths smaller than a x4 require sharing of the REFCLK signals within the x4 boundary.
  - Additional board level components or internal (to the silicon) distribution paths are required.
  - For example, a 2x2 link is defined on lanes [0:1] and [2:3], these links shall share REFCLK0.
  - PERST# connectivity for a 2x2 link is implementation specific. They may be shared within the boundary or implemented as separate resets.

Table 47: SFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2 and 4 Links

Primary Connector			
Lanes [0:3]	**Lanes [4:7]**	**Lanes [8:11]**	**Lanes [12:15]**
Link 0 – x16, REFCLK0, PERST0#			
Link 0 – x8, REFCLK0, PERST0#		Link 1 – x8, REFCLK1, PERST1#	
Link 0 – x4, REFCLK0, PERST0#	Link 1 – x4, REFCLK1, PERST1#	Link 2 – x4, REFCLK2, PERST2#	Link 3 – x4, REFCLK3, PERST3#

4.7.2 DSFF REFCLK and PERST# Requirements

Table 48 shows the Baseboard side connectivity with respect to a DSFF platform. The DSFF slot is comprised of two 2xSFF slots and follows the SFF Link/REFCLK/PERST# mapping of Table 47.

Depending on the Baseboard and NIC side silicon capabilities, the PCIe links on the Primary and the Secondary Connectors may be independently configurable. Asymmetric links – such as [1x16, 2x8], [2x8, 4x4], [4x4, 1x16], etc. are supported. The NIC side PCIe Link Subdivision Capabilities are advertised in the 0xD0 and 0xD1 OEM Records.

Note: While DSFF cards may support a total of 32 PCIe lanes, DC-MHS M-FLW and M-SDNO topologies may share the 32 lanes (as 2x16) across two CPU complexes. As such, a 1x32 PCIe link outside the scope of this specification.

The DSFF Link, REFCLK, and PERST# connectivity shall meet the following requirements:

- All links shall start and terminate within the same connector.
  - For example, a link on the Primary Connector may span from lanes 0:15, or 4:11. While a starting on lane 8 and terminate on lane 23 is not permitted.
- PERST and REFCLK associations shall belong to the same index as defined in Table 46.

- For example, REFCLK0/PERST0# is permitted, but REFCLK0/PERST2#, and REFCLK2/PERST7 are not.
- All clocks shall start on a x4 boundary.
  - For example, a silicon device may have the REFCLK associated with lane 0, lane 4, lane 8, etc.
- Within each x16 connector, links are permitted to be x16, x8, or x4 in width.
  - Asymmetric subdivisions, such as [1x4, 2x2, 1x8] are permitted within the x16.
  - This specification does not provide an exhaustive list.
- Link widths may be smaller than x4 within a x4 clock boundary.
  - Widths smaller than a x4 require sharing of the REFCLK signals within the x4 boundary.
  - Additional board level components or internal (to the silicon) distribution paths are required.
  - For example, a 2x2 link is defined on lanes [0:1] and [2:3], these links shall share REFCLK0.
  - PERST# connectivity for a 2x2 link is implementation specific. They may be shared within the boundary or implemented as separate resets.

Table 48: DSFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2, 4 and 8 Links

<table>
<tr><th colspan="4">Primary Connector</th><th colspan="4">Secondary Connector</th></tr>
<tr><th>Lanes [0:3]</th><th>Lanes [4:7]</th><th>Lanes [8:11]</th><th>Lanes [12:15]</th><th>Lanes [16:19]</th><th>Lanes [20:23]</th><th>Lanes [24:27]</th><th>Lanes [28:31]</th></tr>
<tr><td colspan="4">Link 0 – x16, REFCLK0, PERST0#</td><td colspan="4">Link 4 – x16, REFCLK4, PERST4#</td></tr>
<tr><td colspan="2">Link 0 – x8, REFCLK0, PERST0#</td><td colspan="2">Link 1 – x8, REFCLK1, PERST1#</td><td colspan="2">Link 4 – x8, REFCLK4, PERST4#</td><td colspan="2">Link 5 – x8 REFCLK5, PERST5#</td></tr>
<tr><td>Link 0 – x4, REFCLK0, PERST0#</td><td>Link 1 – x4, REFCLK1, PERST1#</td><td>Link 2 – x4, REFCLK2, PERST2#</td><td>Link 3 – x4, REFCLK3, PERST3#</td><td>Link 4 – x4, REFCLK4, PERST4#</td><td>Link 5 – x4, REFCLK5, PERST5#</td><td>Link 6 – x4, REFCLK6, PERST6#</td><td>Link 7 – x4, REFCLK7, PERST7#</td></tr>
</table>

4.7.3 SFF PCIe REFCLK and PERST# Mapping Examples

The following figures show the Link n, REFCLKn, PERSTn mapping for the SFF with 1, 2 and 4 links as single, dual and quad host configurations. For clarity, the PCIe sideband signals are not illustrated in this section. Please refer to the signal descriptions and associated diagrams for connectivity requirements.

Note: The SFF PCIe REFCLK and PERST# mapping examples are also applicable to the DSFF Primary and Secondary connectors.

Figure 127: SFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links

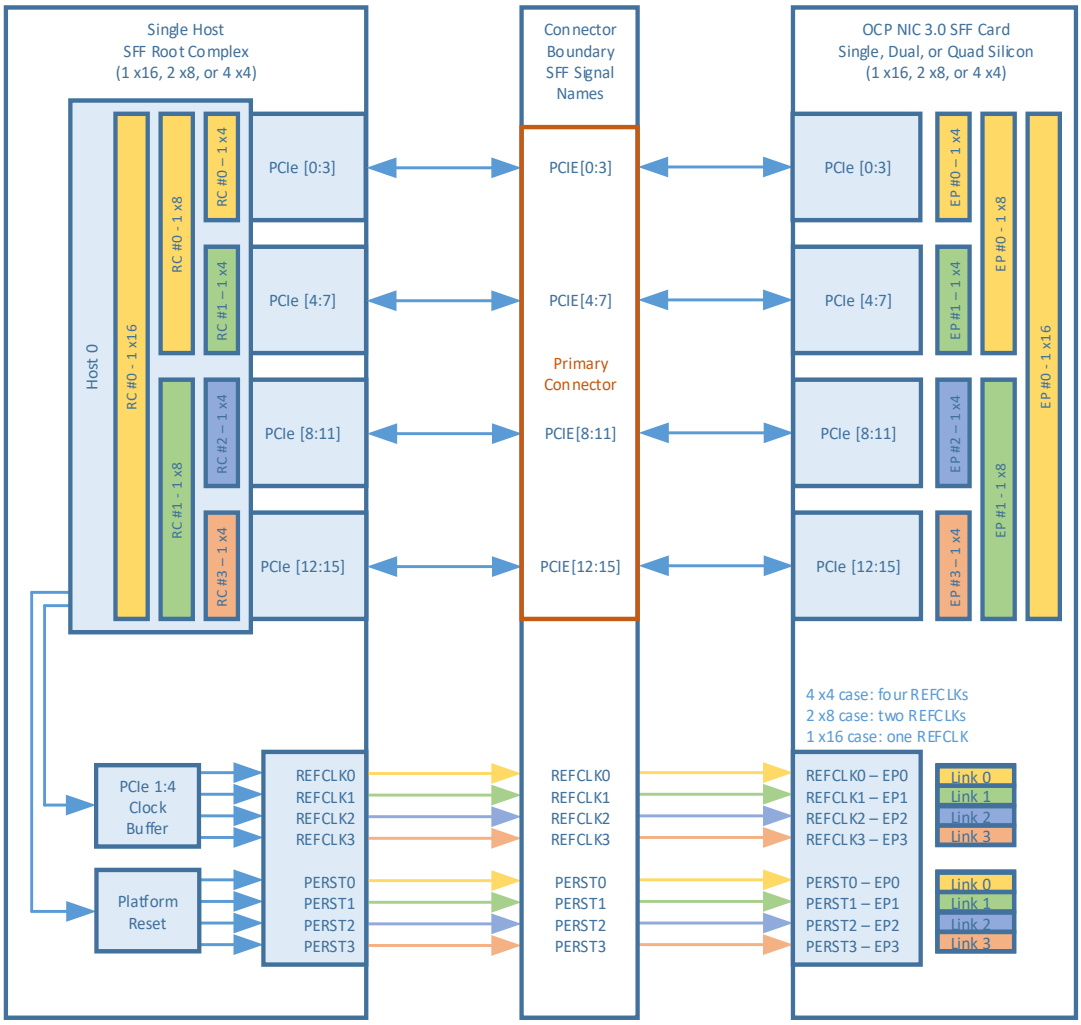
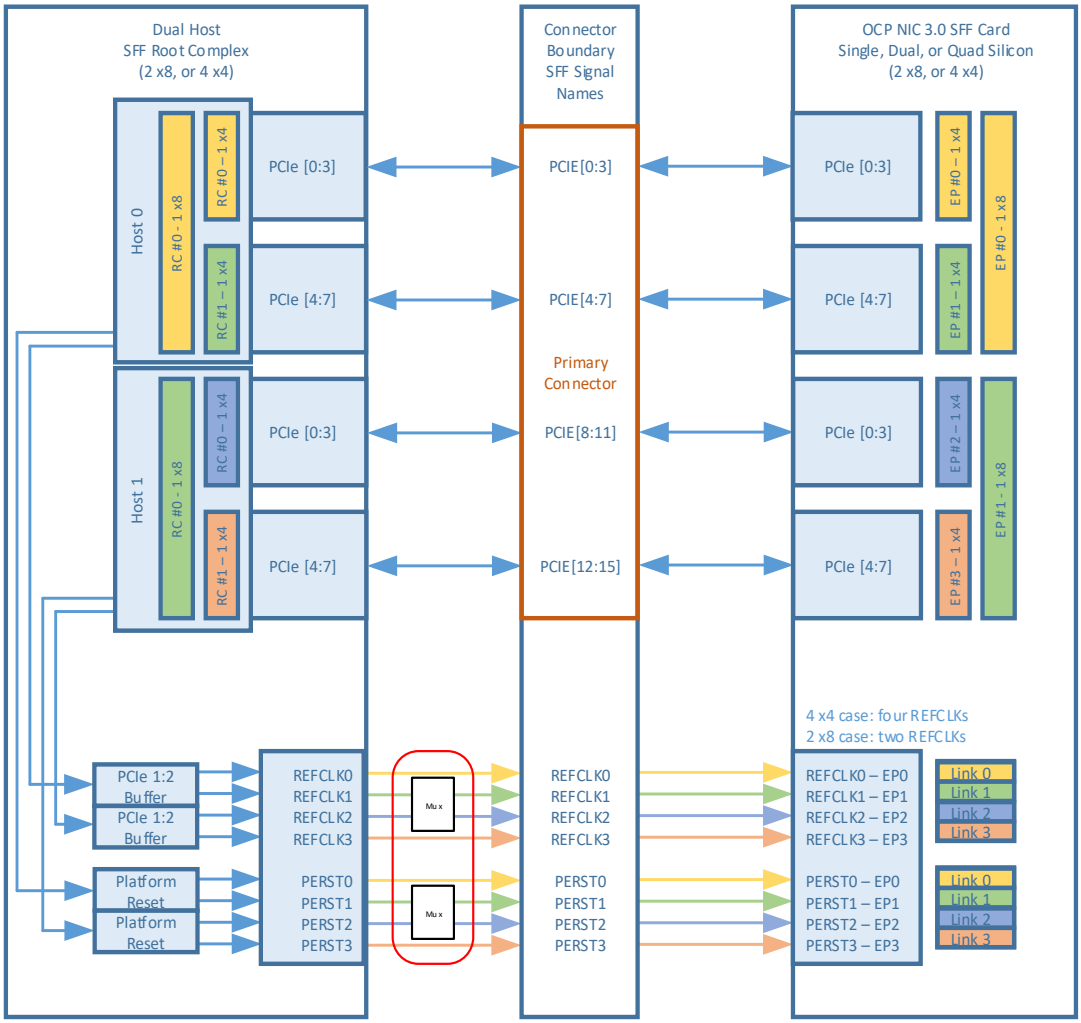
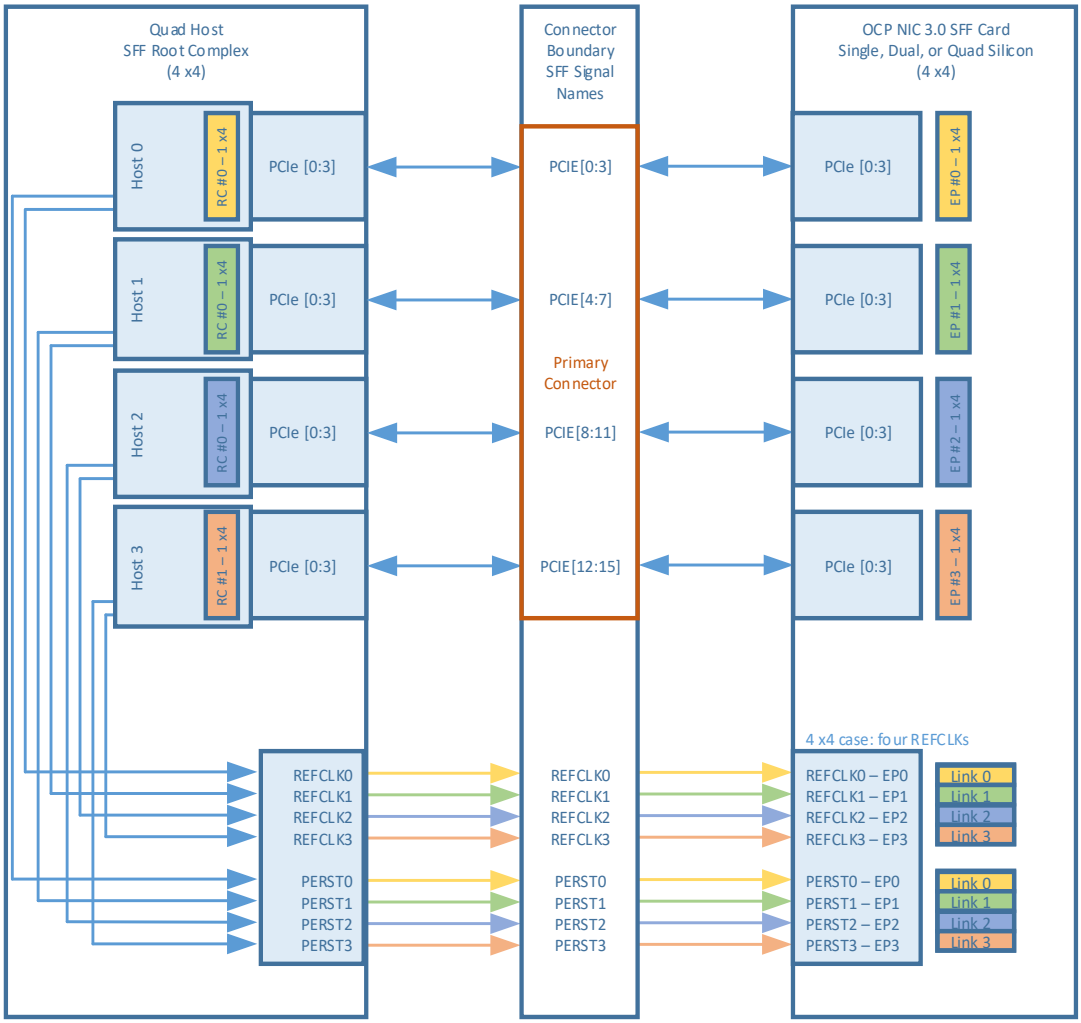


Figure 128: SFF/ PCIe REFCLK Mapping – Dual Host – 2 and 4 links



Note: For dual host applications that connect to a two-link endpoint, the baseboard Host 1 REFCLK0 and PERST0 signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

Figure 129: SFF PCIe REFCLK Mapping – Quad Host – 4 Links



Note: For quad host applications that connect to a two-link endpoint, the baseboard Host 2 REFCLK and PERST signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

4.7.4 REFCLK and PERST# Mapping Expansion

For the SFF and LFF cases where bifurcation is permissible on the baseboard and OCP NIC 3.0 card, an expanded PCIe Bifurcation spreadsheet is available on the OCP Wiki site: https://www.opencompute.org/wiki/Server/NIC.

Implementers shall use the spreadsheet version that is aligned with this version of the OCP NIC 3.0 specification.

The spreadsheet enumerates all the PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 4.6.3.

This expansion table does not apply to the DSFF. DSFF cards declare the PCIe Link Subdivision capabilities in the 0xD0/0xD1 OEM Records.

4.8 Port Numbering and LED Implementations

The OCP NIC 3.0 I/O bracket shall provide port labeling for user identification.

LEDs shall be implemented on the OCP NIC 3.0 I/O bracket when there is sufficient space for local indication. LEDs are typically placed on the primary side. LEDs may be optionally implemented on the secondary side of the card for space constrained implementations. LEDs may be remotely implemented on the card Scan Chain (as defined in Section 4.5.4.4) for link/activity indication on the baseboard. LED configurations for the local and remote cases are described in the sections below. In all cases, the actual link rate may be directly queried through the management interface.

4.8.1 OCP NIC 3.0 Port Naming and Port Numbering

The numbering of all OCP NIC 3.0 external ports shall start from Port 1. When oriented with the primary side components facing up and viewing directly into the port, Port 1 shall be located on the left-hand side. The port numbers shall sequentially increase to the right. Refer to Figure 130 as an example implementation.

4.8.2 OCP NIC 3.0 Card LED Configuration

For low I/O count SFF cards without built in light pipes (such as 1x QSFP, 2x QSFP, 2x SFP, or 2x RJ45), or DSFF cards, where additional I/O bracket area is available, the card shall locally implement on-board link/activity indications. The card may additionally implement LEDs on the optional Scan Chain data stream.

For 4x SFP, a permissible LED implementation may include right angle SMT mount LEDs placed on the secondary side of the OCP NIC 3.0 card. The LEDs shall be located below the line side I/O cages.

A QSFP typically operates in a single port mode but may be optionally configured to operate in dual or quad port modes. The LED definition extends to these modes to indicate the overall operating status of the cage.

Note: Depending on the end faceplate implementation (e.g., with an ejector latch), the secondary side LED implementation may be obstructed and biased to the left to prevent interference with the ejector cam mechanism.

The recommended local (on-card) LED implementation uses two physical LEDs (a bicolored Speed A/Speed B Link LED and a discrete Activity LED). Table 49 describes the OCP NIC 3.0 card LED implementations.

The LEDs shall be uniformly illuminated across the indicator surface. LED surfaces with a diffusion treatment are preferred. For ease of indication within the operating environment, all OCP NIC 3.0 cards shall implement measures to prevent bleed-through between LED indicators and their surrounding chassis components.

3372
3373
3374

Table 49: OCP NIC 3.0 Card LED Configuration with Two Physical LEDs per Port

LED Pin	LED Color	Description
Link	Green Amber Off	Active low. The LED is illuminated when the signal is low. Bicolor multifunction LED. This LED shall be used to indicate the link status. When the link is up, then this LED shall be lit and solid. This indicates that the link is established, there are no local or remote faults, and the link is ready for data packet transmission/reception. For all single port cage implementations (SFP, QSFP and BASE-T), the LED indication shall operate as follows: • The LED is Green when the port is linked at its maximum speed. • The LED is Amber when the port is linked but not operating at the highest speed. • The LED is off when no link is present. When a multi-lane cage is configured for dual port or quad port operation (e.g., QSFP breakout), the LED indication shall operate as follows: • The LED is Green when all ports of the multi-lane cage are linked at its maximum speed. • The LED is Amber when one or more ports of the multi-lane cage are linked, but not operating at the highest speed, or one or more ports are down. • The LED is off when no link is present on all ports of the multi-lane cage. For silicon with limited I/O, the Amber LED may be omitted. In this case, the Green LED shall simply indicate link is up at any configured speed. The illuminated Link LED indicator may be blinked and used for port identification through vendor specific link diagnostic software. The Link LED shall be located on the left-hand side or located on the top for each port when the OCP NIC 3.0 card is viewed in the horizontal plane. For serviceability, green LEDs shall emit light at a wavelength between 513 nm and 537 nm while amber LEDs shall emit light at a wavelength between 580 nm and 589 nm.

LED Pin	LED Color	Description
		For uniformity across OCP NIC 3.0 products, all link LEDs should have their luminous intensity measured in millicandelas (mcd) with an average value between 12 mcd to 18 mcd. A recommended measurement methodology is a work-in-progress by the OCP NIC 3.0 electrical subgroup and will be added in a future release.
Activity	Green Off	Active low. The LED is illuminated when the signal is low. For all single port cage implementations (SFP, QSFP and BASE-T), the LED indication shall operate as follows: • The LED is off when there is no activity. • The LED should blink at the rate of 0.5 Hz to 5 Hz when there is activity. • The LED shall not blink when the link state is down. When a multi-lane cage is configured for dual port or quad port operation (e.g., QSFP breakout), the LED indication shall operate as follows: • The LED is off when there is no activity on all ports of the multi-lane cage. • The LED should blink at the rate of 0.5 Hz to 5 Hz when there is activity on one or more ports of the multi-lane cage. • The LED shall not blink when the link state is down for all ports of the multi-lane cage. The activity LED shall be located on the right-hand side or located on the bottom for each port when the OCP NIC 3.0 card is viewed in the horizontal plane. For serviceability, green LEDs shall emit light at a wavelength between 513 nm and 537 nm. For uniformity across OCP NIC 3.0 products, all activity LEDs should have their luminous intensity measured in millicandelas (mcd) with an average value between 12 mcd and 18 mcd. A recommended measurement methodology is a work-in-progress by the OCP NIC 3.0 electrical subgroup and will be added in a future release.

4.8.3 OCP NIC 3.0 Card LED Ordering

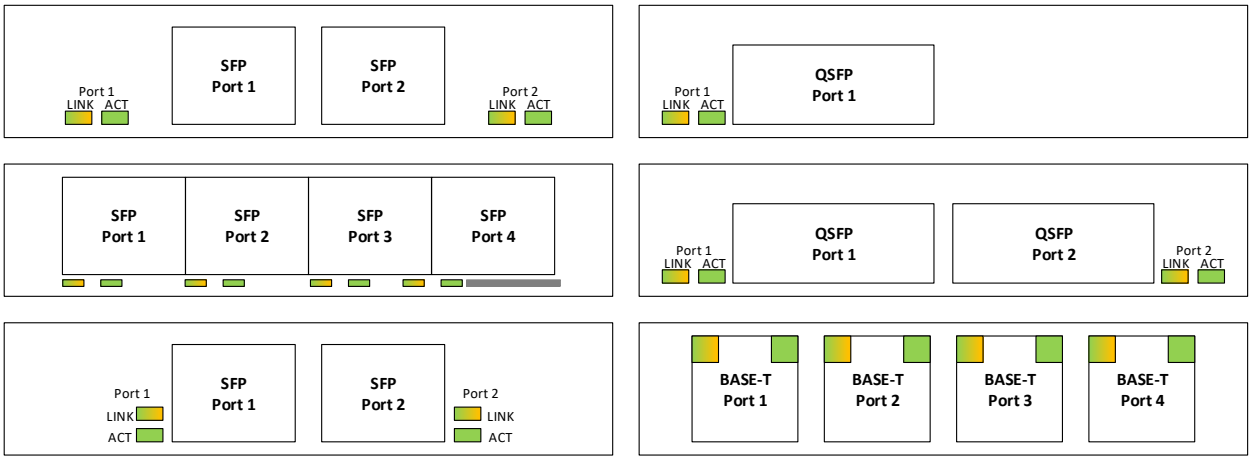
For all OCP NIC 3.0 card use cases, each port shall implement the green/amber Link LED and a green activity LED. For I/O limited silicon, the amber LED may be omitted.

When the OCP NIC 3.0 card is viewed from the horizontal position, and with the primary component side facing up, the Link LED shall be located on the left side and the activity LED shall be located on the right. The LED placement may also make use of a stacked LED assembly, or light pipe in the vertical axis. In this case, the Link Activity LED shall be on the top of the stack, and the Activity LED shall be on the bottom of the stack when viewed from the horizontal position. In all cases, the port ordering shall increase from left to right when viewed from the same horizontal position.

The actual placement of the Link and Activity LEDs on the faceplate may be left up to the discretion of the OCP NIC 3.0 card designer. The LED port association should be clearly labeled on the OCP NIC 3.0 card if the space allows. Similarly, the LED for link and the LED for Activity indication should also be marked on the faceplate. Vendors shall use the largest text permissible for increased readability.

For 4xSFP configurations, the LEDs may be placed on the secondary side of the card using right-angle SMT components. OCP NIC 3.0 designers may opt to use the scan chain LEDs instead or in addition to the on-card indicators.

Figure 130: Port and LED Ordering – Example SFF Link/Activity and Speed LED Placement



Note 1: The example port and LED ordering diagrams shown in Figure 130 are viewed with the card in the horizontal position and the primary side is facing up.

Note 2: The 4xSFP LED implementation is biased to the left to allow clearance for the ejector latch cam.

Note 3: For TSFF, there may be sufficient space to place LEDs above the port depending on the I/O configuration. Light pipes may be used in this configuration at the discretion of the OCP NIC 3.0 card designer.

4.8.4 Baseboard LEDs Configuration over the Scan Chain

A SFF OCP NIC 3.0 card with a fully populated I/O bracket (2x QSFP, 4x SFP or 4x RJ45) does not have sufficient space for primary-side discrete on-board (faceplate) LED indicators. Section 4.8.2 presents an implementation for placing LEDs on the secondary side.

In this scenario, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain for remote indication. The Scan Chain bit stream is defined in Section 4.5.4.4.

The baseboard LED implementation uses two discrete LEDs – a green/amber Link LED and a discrete green Activity. The physical baseboard LED implementation is left up to the baseboard vendor and is not defined in this specification. The LED implementation is optional for baseboards.

For serviceability, green LEDs shall emit light at a wavelength between 513 nm and 537 nm while amber LEDs shall emit light at a wavelength between 580 nm and 589 nm.

At the time of this writing, the Scan Chain definition allows for up to two link and one activity LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (on). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP NIC 3.0 compliant chassis (e.g., front LED indicators with rear I/O cards).

4.9 Power State Machine

There are a total of five power states for an OCP NIC 3.0 card. Four power states are for normal operation of the card: NIC Power Off, ID Mode, Aux Power Mode, and Main Power Mode. These four power states are mandatory for each OCP NIC 3.0 card. An optional fifth power state is Programming Mode and allows the FRU EEPROM to be updated in the field under the baseboard control. The normal transition order for these states is shown in Figure 131 and described in detail in the sections below. For simplicity, only the signal transitions resulting in a state change are shown. The NIC side available functions per power state are defined in Table 50. The minimum transition time between power states is defined in Section 4.12.

Note: For a DSFF card, the AUX_PWR_EN0, MAIN_PWR_EN0 and NIC_PWR_GOOD0 signals from the Primary Connector are used for the power state controls.

Figure 131: Baseboard Power States

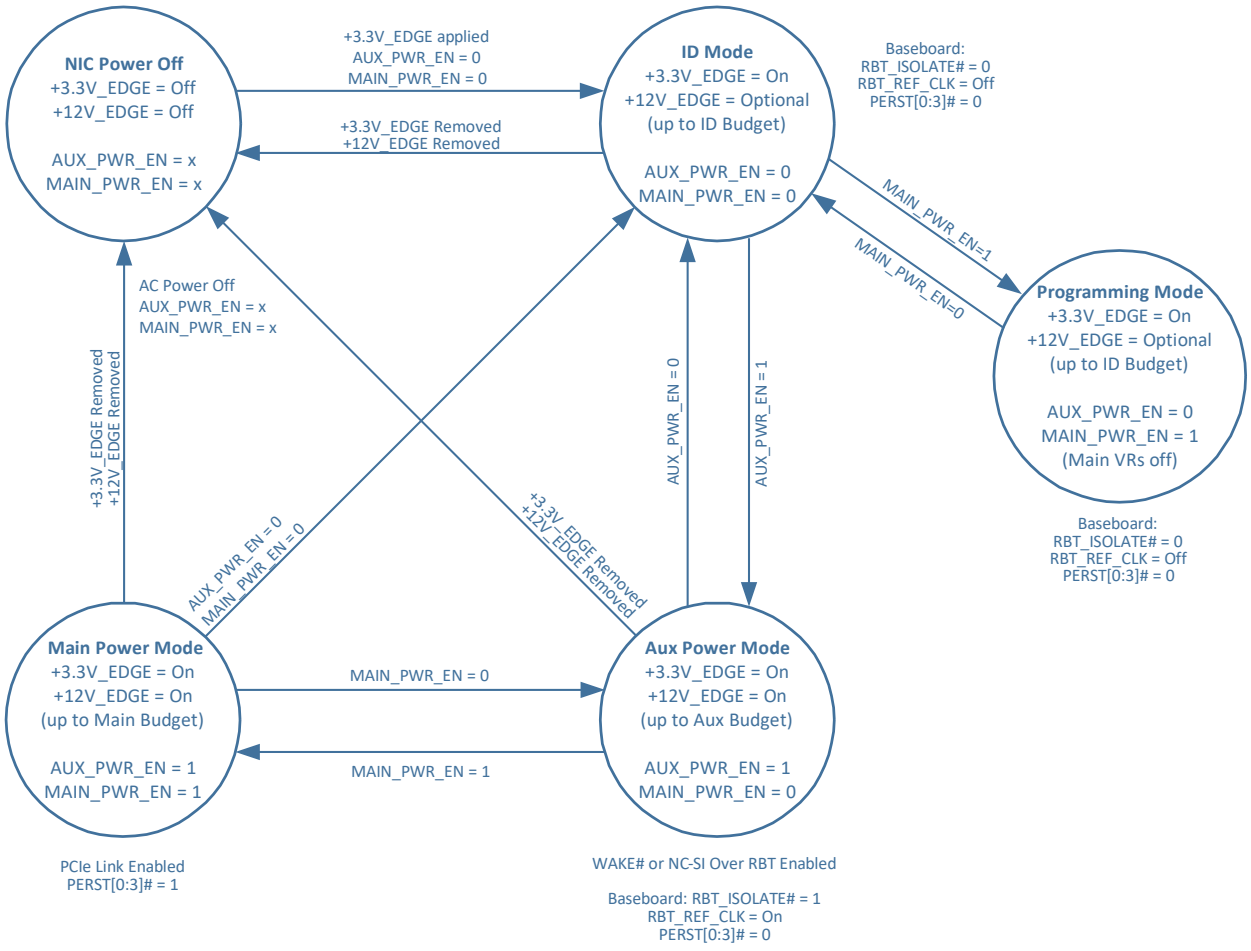


Table 50: Available Card Functions per Power State

Power State / Signal Group	NIC Power Off	ID Mode	Programming Mode	Aux Power Mode	Main Power Mode
+3.3V _EDGE	Powered Off	Power Applied	Power Applied	Power Applied	Power Applied
+12V_EDGE	Powered Off	Power Optional[2]	Power Optional[2]	Power Applied[3]	Power Applied
AUX_PWR_EN	Low	Low	Low	High	High
MAIN_PWR_EN	Low	Low	High	Low	High
PERSTn	Low	Low	Low	Low	High
PCIe Link	No Link	Link in reset	Link in reset	Link in reset	Link up
FRU	Isolated on Baseboard	Mandatory	Mandatory[4]	Mandatory	Mandatory
Scan Chain	Scan Clock & Data low	Mandatory [1]	Mandatory [1]	Mandatory	Mandatory
Optional Interfaces					
WAKEn	Isolated on NIC	Isolated on NIC	Isolated on NIC	Mandatory[5]	Mandatory[5]
RBT Link	Isolated on Baseboard	Isolated on Baseboard	Isolated on Baseboard	Mandatory[5]	Mandatory[5]
Flex I/O				Mandatory[5]	Mandatory[5]
USB				Mandatory[5]	Mandatory[5]

Mandatory = Function is required on the NIC in the designated power state.

Note 1: Only the PRSNTB[7:0]# scan chain signals are valid in ID mode as the OCP NIC 3.0 card power rails have not yet been enabled via the AUX_PWR_EN/MAIN_PWR_EN signals.

Note 2: The +12V_EDGE rail is optionally disabled by the baseboard during this power state. The max permissible leakage is up to the ID Mode / Programming Mode current limit defined in Section 4.10. The NIC shall not rely on +12V_EDGE power in this state and shall not malfunction if +12V_EDGE is present or absent.

Note 3: The +12V_EDGE rail is on. The max permissible current draw is up to the Aux Power Mode current limit defined in Section 4.10.

Note 4: The FRU EEPROM WP pin is low (not write protected) to enable programming using any of the defined methods for controlling the EEPROM WP signal. Refer to the FRU Write Protection Mechanism field in Section 5.10.3.1.

Note 5: If the interface is supported by the OCP NIC 3.0 card, otherwise the interface is driven by the default pull-up/pull-down resistors in the Aux Power Mode and Main Power Mode states.

4.9.1 NIC Power Off

In NIC Power Off mode, all power delivery has been turned off or the card is not physically plugged into the baseboard. Transition to this state can be from any other state.

4.9.2 ID Mode

In the ID Mode, only +3.3V_EDGE is available for powering up the FRU EEPROM and the Scan Chain devices. All OCP NIC 3.0 cards must enter the ID Mode state for FRU EEPROM and scan chain queries immediately following the NIC Power Off state. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN0==0 and MAIN_PWR_EN0==0.

The baseboard queries the EEPROM and determines the OCP NIC 3.0 device capabilities. The FRU EEPROM content requirements are defined in Section 5.10. Only the card PRSNTB[7:0]# bits are valid on the scan chain in this mode as the OCP NIC 3.0 card power rails have not yet been enabled via the AUX_PWR_EN0 and MAIN_PWR_EN0 signals. The WAKE#, TEMP_WARN#, TEMP_CRIT#, Link and Activity bits are invalid and should be masked by the baseboard in ID Mode.

Baseboards may disable +12V_EDGE in this power state. OCP NIC 3.0 cards are not intended to use +12V_EDGE in ID Mode, however leakage current may be present. If +12V_EDGE is not provided by the baseboard and leakage is present, the max voltage leakage from the OCP NIC 3.0 card to the baseboard shall be limited to 300 mV when a 1 kΩ bleed resistor is present on the baseboard. The baseboard bleed resistor is optional if the baseboard can tolerate leakage. If +12V_EDGE is present in ID Mode, the max current is defined in Section 4.10.

4.9.3 Aux Power Mode

The Aux Power Mode provides both +3.3V_EDGE and +12V_EDGE across the OCP Connector. +12V_EDGE in Aux mode may be used to deliver power to the OCP NIC 3.0 card, but only up to the Aux mode budget as defined in Table 51. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN0==1, MAIN_PWR_EN0==0, NIC_PWR_GOOD0==1 and the duration (T_{APL}) has passed for the ID-Aux Power Mode ramp. This guarantees the ID mode to Aux Power Mode transition (as shown in Figure 132) has completed and all Aux Power Mode rails are within operating tolerances. The WAKE#, TEMP_WARN#, and TEMP_CRIT# bits shall not be sampled until these conditions are met.

For OCP NIC 3.0, Aux Power Mode corresponds to ACPI power state S5 on the system. This could also correspond to ACPI power state S3 or S4 depending on the implementation.

4.9.4 Main Power Mode

The Main Power Mode provides both +3.3V_EDGE and +12V_EDGE across the OCP connector. The OCP NIC 3.0 card operates in full capacity. Up to 80 W may be delivered on +12V_EDGE for an SFF Card and up to 160 W for a DSFF Card. Additionally, up to 3.63 W is delivered on each +3.3V_EDGE pin. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN0==1, MAIN_PWR_EN0==1, NIC_PWR_GOOD0==1 and the duration (T_{MPL}) has passed for the Aux-Main Power Mode ramp. This guarantees the Aux Power Mode to Main Power Mode transition (as shown in Figure 132) has completed and all Main Power Mode rails are within operating tolerances. The WAKE#, TEMP_WARN#, and TEMP_CRIT# bits shall not be sampled until these conditions are met.

For OCP NIC 3.0, Main Power Mode corresponds to ACPI power state S0 on the system. This could also correspond to ACPI power state S1 depending on the implementation.

4.9.5 Programming Mode

The Programming Mode provides +3.3V_EDGE for powering up the FRU EEPROM. This is an optional state that disables the FRU EEPROM write protection mechanism via combinatorial logic and allows the baseboard to reprogram the FRU EEPROM. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN0==0, MAIN_PWR_EN0==1, and NIC_PWR_GOOD0==0. This state shall only be entered from ID mode if the FRU EEPROM advertises support for this power state as defined in Section 5.10.3.1.

Baseboards may disable +12V_EDGE in this power state. OCP NIC 3.0 cards are not intended to use +12V_EDGE in Programming Mode, however leakage current may be present. If +12V_EDGE is not

provided by the baseboard and leakage is present, the max voltage leakage from the OCP NIC 3.0 card to the baseboard shall be limited to 300 mV when a 1 kΩ bleed resistor is present on the baseboard. The baseboard bleed resistor is optional if the baseboard can tolerate leakage. If +12V_EDGE is present in Programming Mode, the max current is defined in Section 4.10.

Additionally, the Aux Power Mode and Main Power Mode VRs need to remain disabled and NIC_PWR_GOOD0 shall remain low while the card is in this state. An example discrete logic circuit to accomplish this gating is shown in Figure 118. NIC vendors may implement their own gating circuitry if the same result is achieved.

Devices which use GPIO, NC-SI or PLDM for FRU EEPROM WP control may allow programming of the FRU EEPROM when in operating in the Aux Power or Main Power Modes. Usage of the GPIO signal, NC-SI or PLDM to control the write protect mechanism are implementation specific and are outside the scope of this specification.

4.10 Power Supply Rail Requirements and Slot Power Envelopes

The baseboard provides +3.3V_EDGE and +12V_EDGE to both the Primary and Secondary Connectors. The rail requirements are leveraged from the PCIe CEM 4.0 specification. For OCP NIC 3.0 implementations, there are six total power envelopes. Five power envelopes are defined for use on the SFF only and seven for the DSFF.

The max current draw is defined in Table 51 for OCP NIC 3.0 cards. This is shown for each state and power envelope and is inclusive of the line side transceivers installed on the card. The slot power values are the max supportable power delivered to the card for each slot type. This is independent of the +3.3V_EDGE and +12V_EDGE rails deviating from their nominal values.

For dual connector DSFF implementations, the max current for +3.3V_EDGE, +12V_EDGE are doubled for Aux Power Mode and Main Power Mode for the 160 W power slot. This also applies for the max capacitive load. For DSFF cards that implement a downshifted connector (Primary Connector only), a DSFF card shall not exceed the specifications for an 80 W slot. Refer to Table 51 for details and Section 4.10.1 for connector power sharing requirements.

Table 51: Baseboard Power Supply Rail Requirements – Slot and Card Power Envelopes

Power Rail	15 W Slot	25 W Slot	35 W Slot	50 W Slot	80 W Slot	80 W Slot	160 W Slot
	SFF and DSFF					Single Conn. DSFF	Dual Conn. DSFF
+3.3V_EDGE							
Voltage Tolerance	±9%	±9%	±9%	±9%	±9%	±9%	±9%
Max Supply Current							
ID Mode	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA
Programming Mode	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA
Aux Power Mode	1.1 A	1.1 A	1.1 A	1.1 A	1.1 A	1.1 A	2.2 A
Main Power Mode	1.1 A	1.1 A	1.1 A	1.1 A	1.1 A	1.1 A	2.2 A
Max Capacitive Load	150 µF	150 µF	150 µF	150 µF	150 µF	150 µF	300 µF
+12V_EDGE							
Voltage Tolerance[6]	+8%/-12%	+8/-12%	+8/-12%	+8/-12%	+8/-12%	+8/-12%	+8/-12%
Max Supply Current							
ID Mode[5]	50 mA	50 mA	50 mA	50 mA	50 mA	50 mA	50 mA
Programming Mode[5]	50 mA	50 mA	50 mA	50 mA	50 mA	50 mA	50 mA
Aux Power Mode	0.7 A	1.1 A	1.5 A	2.1 A	3.3 A	3.3 A	6.6 A
Main Power Mode	1.25 A	2.1 A	2.9 A	4.1 A	6.6 A	6.6 A	13.2 A
Max Capacitive Load[3]	500 µF	500 µF	500 µF	1200 µF	2000 µF	2000 µF	4000 µF

Note 1: While cards may draw up to the published power ratings, the baseboard vendor shall evaluate its cooling capacity for each slot power envelope to determine if a transition to Aux Power Mode is allowed.

Note 2: The maximum slew rate for each OCP NIC 3.0 card shall be no more than 0.1 A/µs per the PCIe CEM specification.

Note 3: Each OCP NIC 3.0 card shall limit the bulk capacitance to the max published values.

Note 4: For systems that implement hot plug, the baseboard shall limit the voltage slew rate such that the instantaneous inrush current shall not exceed the specified max current. The equation is defined in the PCIe CEM specification and is dV/dt = I/C; where:

I = max allowed current (A)
C = max allowed bulk capacitance (F)
dV/dt = maximum allowed voltage slew rate (V/s)

Note 5: +12V_EDGE may optionally be disabled during ID Mode and Programming mode. Refer to Section 4.9 for details.

Note 6: The SFF-TA-1002 connectors permit up to 1.1 A/pin for 6 adjacent pins for continuous operation. This allows 80 W of delivered power through the connector with +12V_EDGE at nominal voltages. Total delivered power is reduced when the +12V_EDGE rail is operating at voltages lower than nominal (e.g. -12%) and must be accounted for by the baseboard telemetry prior to enabling card power.

The OCP NIC 3.0 FRU definition provides a record for the max power consumption of the card. This value shall be used to aid in determining if the card may be enabled for a given OCP slot. Refer to Section 5.10.3 for the available FRU records.

Additionally, the baseboard shall advertise its slot power limits to aid in the overall board power budget allocation to prevent a high-power card from being enabled in a lower power class slot. This is implemented via the Slot Power Limit Control mechanism as defined in the PCIe Base Specification. The end point silicon will power up in a low power state until power is negotiated.

4.10.1 DSFF Current Sharing

For DSFF NIC designs that utilize both the Primary and Secondary connector, the OCP NIC card designer is responsible for ensuring the power draw is equal from each connector for the +12V_EDGE and +3.3V_EDGE rails. This section does not apply to DSFF designs that only implement the Primary Connector edge.

NIC vendors shall ensure the card power shall not exceed 80 W per connector (per SFF-TA-1002); and that the total card power is balanced to within 6% of each other.

For baseboards capable of operating in 2xSFF and 1xDSFF deployments, both SFF slots should provide the same max power budget to prevent asymmetric power draw. If the baseboard supplies asymmetric power budgets to the DSFF capable slots, then the baseboard shall limit the total power consumption to no more than two times of the smaller power budget of the SFF slots.

For example: The Baseboard provides Slot 0 (Primary Connector) with 35 W power envelope; and Slot 1 (Secondary Connector) with a 15 W power envelope. The Baseboard is responsible for determining its own power limit when used as a DSFF slot and shall limit the max permissible power to be 2*min(Slot 0, Slot 1) = 2*min(35 W, 15 W) = 30 W. The Baseboard shall then query the NIC 0xC0 OEM record to ensure the card requested power in Main Power Mode does not exceed the max allowed Baseboard power.

4.11 Hot Swap Considerations for +12V_EDGE and +3.3V_EDGE Rails

Hot swap support is optional for baseboard implementers. However, the OCP NIC 3.0 form factor lends itself to potential card insertion and removal events while the baseboard is powered on. These events need to be carefully orchestrated with the operating system and system management entity to prevent a system hang. A surprise extraction may occur in some instances when resources have not been quiesced and the card is removed. Many aspects of the system are involved in processing such an event in both cases. The current scope of this specification does not define an overall hardware or software system architecture to support hot swap. Instead, this specification only highlights the hardware elements that can be utilized to support hot swap for implementations.

The system implementer shall consider the use of hot swap controllers on both the +12V_EDGE and +3.3V_EDGE pins to prevent damage to the baseboard or the OCP NIC 3.0 card. Hot swap controllers limit the in-rush current while also providing overcurrent, undervoltage and overvoltage protection capabilities.

The hot swap controller may gate the +12V_EDGE and +3.3V_EDGE on the card connector(s) based on the PRSNTB pin states. The PRSNTB[7:0]# pins are used to detect an OCP 3.0 NIC card insertion and removal event. The card type detection is described in Section 4.6. A card is present in the system when

the detected PRSNTB pin states have one or more zeros. Specifically, an SFF card is present in the system when the PRSNTB[3:0]# value is not 0b1111. An LFF card is present when PRSNTB[7:0]# is not 0b1111_1111. A DSFF card is present when PRSNTB[7:0]# is 0b0010_0010. For DSFF cards with only 16 PCIe lanes, the gold fingers are permitted to connect PRSNTB[3:0]#==0b0010 for a valid indication of a DSFF. The power rails on the Primary and Secondary connectors need to be simultaneously enabled for the DSFF cards.

The PRSNTB# pins may be OR'ed together and connected to the hot swap controller to detect card insertion and removal. Per the OCP NIC 3.0 mechanical definition (Section 2), the present pins are short pins and engage only when the card is positively seated.

For SFF, the PCIe link subdivision is encoded in the PRSNTB pins. For DSFF, PCIe link subdivision is encoded in the 0xD0/0xD1 OEM Records which need to be read in ID mode. Using in-band signaling, the PCIe link may be enabled to periodically train when a card is plugged in and powered on. The card type is determined by querying the FRU data over the SMBus.

At the time of this writing, the DSP0222 Network Controller Sideband Interface (NC-SI) Specification 1.1 and 1.2 does not define a mechanism to discover hot-plug support. Future work is needed for supporting this feature on NC-SI over RBT interfaces.

Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

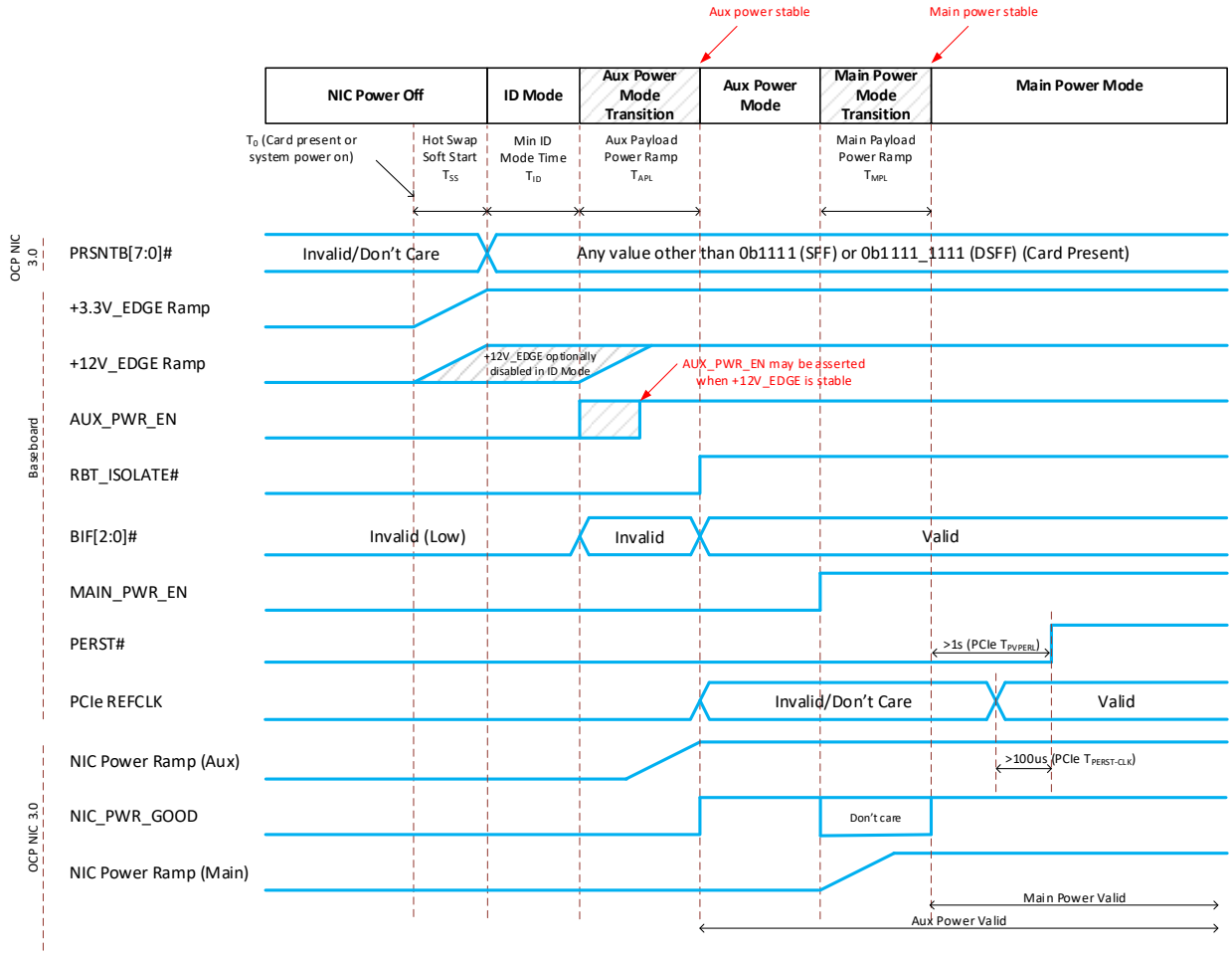
4.12 Power Sequence Timing Requirements

4.12.1 Power Up Sequence Timing

The following figure shows the power sequence of PRSNTB[3:0]#, +3.3V_EDGE, +12V_EDGE relative to AUX_PWR_EN, RBT_ISOLATE#, BIF[2:0]#, MAIN_PWR_EN, PERSTn*, and PCIe REFCLK stable on the baseboard. Additionally, the OCP NIC 3.0 card power ramp, and NIC_PWR_GOOD are shown. Please refer to Section 4.5.7 for the NIC_PWR_GOOD definition. Refer to DMTF DSP0222 for details on the NC-SI controller and clock startup requirements.

A DSFF card has a single +12V_EDGE and +3.3V_EDGE power domain that is sourced from both connectors. As such, the baseboard shall provide power to both the Primary and Secondary Connectors for each power state transition. The timing of +12V_EDGE and +3.3V_EDGE shall be coincident. The baseboard shall ensure the power rail ampacity is available for each power state and prior to deasserting PERST#.

Figure 132: Power-Up Sequencing – Normal Operation

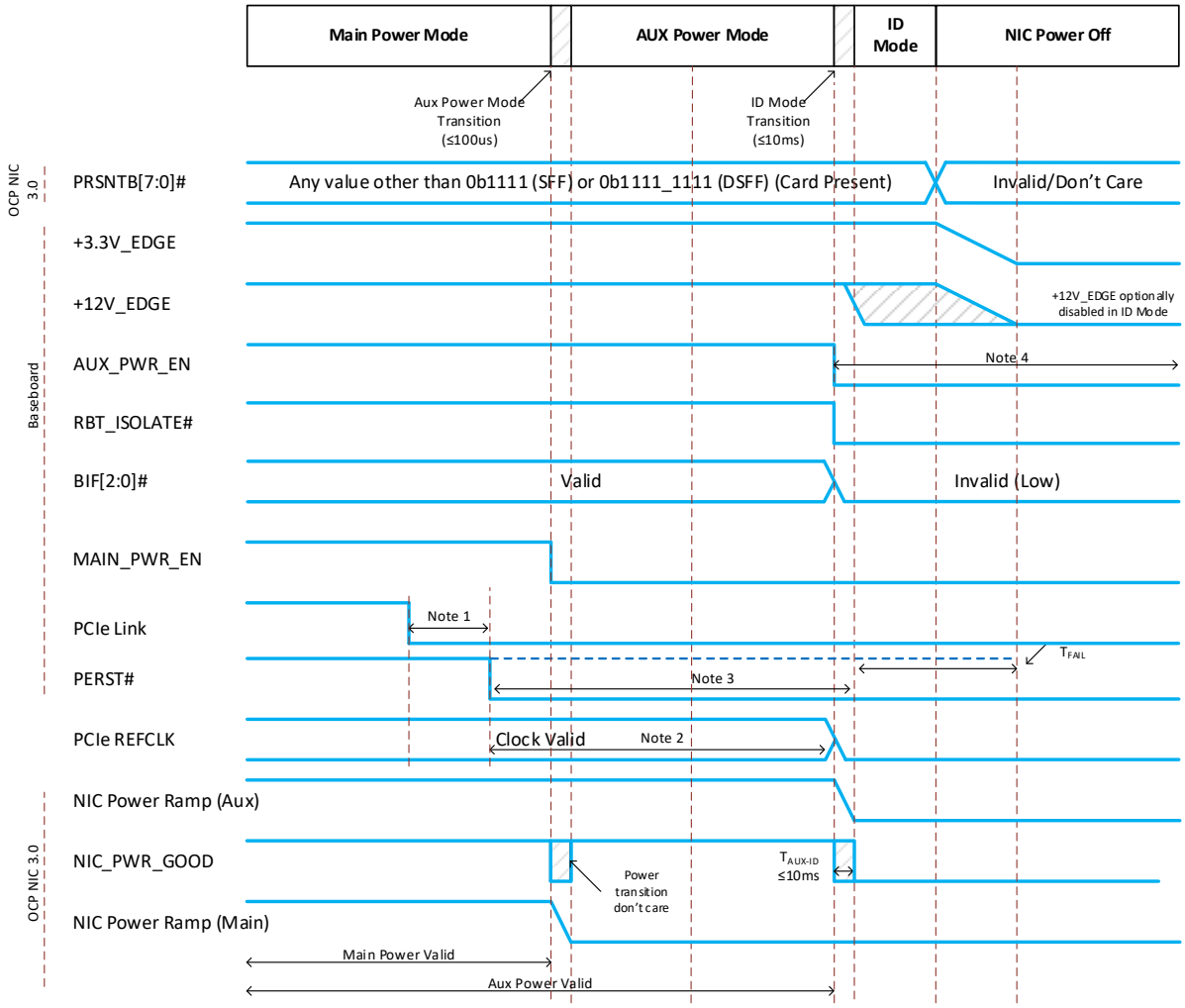


Note 1: The RBT isolation state is controlled with the baseboard RBT_ISOLATE# signal. This controls the baseboard RBT isolator.
Note 2: For NC-SI over RBT, the rising edge of NIC_PWR_GOOD shall be treated as V_{REF} is available for NC-SI communication. Refer to timing parameter T4 in the DMTF DSP0222 specification for details.

4.12.2 Power Down Sequence Timing

The normal power down sequencing requirements is shown in Figure 133.

Figure 133: Power-Down Sequencing – Normal Operation

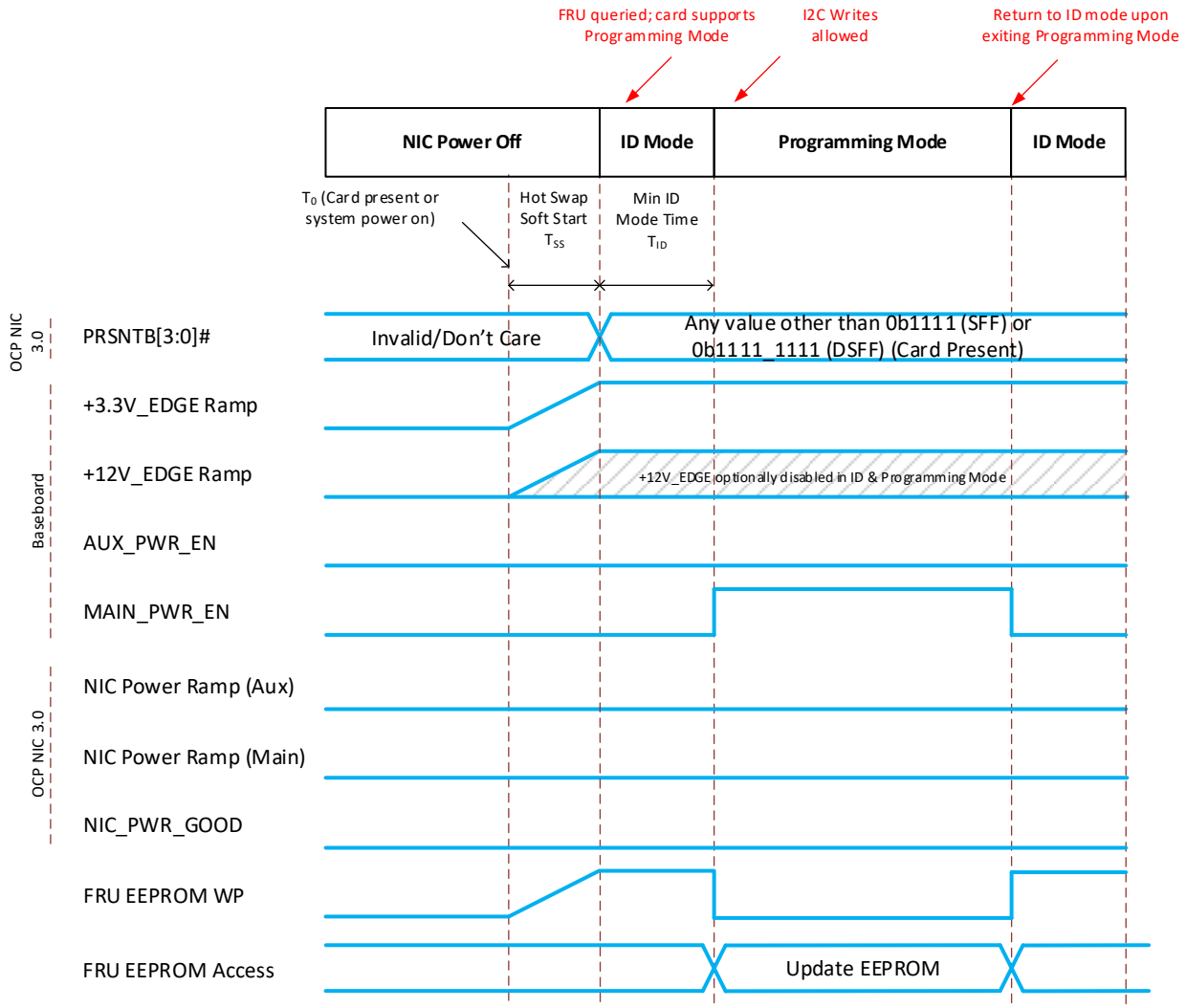


Note 1: When possible, the PCIe link should be put into an inactive state (Device in $D3_{hot}$) prior to PERST# going active. (PCIe CEM Section 2.2.3)
Note 2: REFCLK goes inactive after PERST# goes active. (PCIe CEM Section 2.2.3)
Note 3: PERST# goes active before or soon as possible but not later than T_{FAIL} following power on any of the rails on the OCP connector(s) becoming unstable. (PCIe CEM Section 2.2.3)
Note 4: The baseboard shall have a minimum delay of T_{CYCLE_SFF} and T_{CYCLE_LFF} for the respective form-factors between AUX_PWR_EN deassertion (power off) and subsequent AUX_PWR_EN assertion (power on) to prevent powering up into a pre-biased condition. T_{CYCLE_SFF} is applicable to both the SFF and DSFF.

4.12.3 Programming Mode Sequencing

The power sequencing required for entering Programming Mode is shown in Figure 134.

Figure 134: Programming Mode Sequencing



Note 1: All other signals are electrically low and are not shown.

4.12.4 Power Sequencing Timing Parameters

The power sequencing timing parameters are shown in Table 52.

Table 52: Power Sequencing Parameters

Parameter	Value	Units	Description
T_{ss}	20	ms	Maximum time between system +3.3V_EDGE and +12V_EDGE ramp to power stable. This parameter is only applicable to hot swap controller-based implementations. For non-hot swap applications, the +3.3V_EDGE and +12V_EDGE ramp is system dependent.
T_{SCAN_RDY}	1	ms	Minimum time required between +3.3V_EDGE stable to the first scan chain data valid read.
T_{ID}	20	ms	Minimum time per spec to spend in ID mode.
T_{APL}	50	ms	Maximum time between AUX_PWR_EN assertion and NIC_PWR_GOOD assertion.
T_{MPL}	50	ms	Maximum time between MAIN_PWR_EN assertion and NIC_PWR_GOOD assertion.
T_{PVPERL}	1	s	Minimum time between NIC_PWR_GOOD assertion in Main Power Mode and PERST# deassertion. For OCP NIC 3.0 applications, this value is >1 second. This is longer than the minimum value specified in the PCIe CEM Specification, Rev 5.0.
T4	2	s	Maximum time interval from when the network controller NC-SI over RBT interface is able to respond to commands. The parameter T4 is defined in the DSP0222 specification and is measured from when V_{REF} becomes available. For OCP NIC 3.0, the value T4 is measured from the deassertion of RBT_ISOLATE#.
$T_{PERST\#-CLK}$	100	µs	Maximum Time PCIe REFCLK is stable before PERST# inactive.
T_{FAIL}	500	ns	In the case of a surprise power down, PERST# goes active at minimum T_{FAIL} after power is no longer stable.
T_{AUX-ID}	10	ms	Maximum time from AUX_PWR_EN deassertion to NIC_PWR_GOOD deassertion.
T_{CYCLE_SFF}	30	ms	Minimum time between AUX_PWR_EN deassertion to AUX_PWR_EN reassertion for SFF and DSFF cards. Delay time allows for OCP NIC 3.0 card capacitors to discharge and prevent reapplying power into a pre-biased condition.
T_{CYCLE_LFF}	60	ms	Minimum time between AUX_PWR_EN deassertion to AUX_PWR_EN reassertion for LFF cards. Delay time allows for OCP NIC 3.0 card capacitors to discharge and prevent reapplying power into a pre-biased condition.

4.13 Digital I/O Specifications

This section is for informative reference only. All digital I/O pins on the connector boundary are +3.3 V signaling levels. The following tables provide the absolute max levels. Refer to the appropriate specifications for the RBT, PCIe and SMBus DC/AC specifications for any superseded values.

Table 53: Digital I/O DC specifications

Symbol	Parameter	Min	Max	Units	Note(s)
V_{OH}	Output voltage		3.6	V	6
V_{OL}	Output low voltage		0.8	V	6
V_{IH1}	Input voltage	2.0	3.6	V	1, 3, 4, 6
V_{IL1}	Input low voltage	-	0.8	V	1, 3, 4, 6
V_{IH2}	Input voltage	2.1	3.6	V	2
V_{IL2}	Input low voltage	-	0.8	V	2
V_{IH3}	Input voltage	2.1	3.6	V	5
V_{IL3}	Input low voltage	-	1.0	V	5

Note 1: Applies to PCIe CEM signals PERST[5:0]#, WAKE#, PWRBRK[1:0]#.

Note 2: Applies to SMBus signals SMCLK, SMDAT and SMRST#.

Note 3: Applies to RBT signals defined by DSP0222.

Note 4: Applies to OCP NIC 3.0 card edge signals (AUX_PWR_EN, MAIN_PWR_EN, SLOT_ID[1:0], NIC_PWR_GOOD, BIF[2:0]#, PRSNTB[3:0]#.

Note 5: Applies to scan chain shift register signals (SCAN_LD#, SCAN_DATA_IN, SCAN_DATA_OUT, SCAN_CLK).

Note 6: Applies to single ended Time Synchronization signals (TS_TX_SYNC, TS_TX_FREQ, TS_RX_SYNC, TS_RX_FREQ, TS_GPI and TS_GPO)

5 Management and Pre-OS Requirements

OCP NIC 3.0 card management is an important aspect to overall system management. This section specifies a common set of management requirements for OCP NIC 3.0 implementations. There are three types of implementations (RBT+MCTP Type, RBT Type, and MCTP Type) depending on the physical sideband management interfaces, transports, and traffic supported over different transports. An OCP NIC 3.0 implementation shall support at least one type of implementation for card management. For a given type of implementation, an OCP NIC 3.0 card shall support type specific requirements described in Sections 5.1 through 5.7.

Table 54: OCP NIC 3.0 Management Implementation Definitions

Management Type	Definition
RBT Type	The RBT Type management interface is exclusive to the Reduced Media Independent Interface (RMII) Based Transport (RBT). The NIC card is required to support the DSP0222 Network Controller Sideband Interface (NC-SI) Specification for this management.
RBT+MCTP Type	The RBT+MCTP management interface supports both the RBT and MCTP standards, specifically the DSP0222 Network Controller Sideband Interface (NC-SI) Specification, DSP0236 Management Component Transport Protocol (MCTP) Base Specification, and the associated binding specifications. This is the preferred management implementation for baseboard NIC cards. See MCTP Type below for more details.
MCTP Type	The MCTP management interface supports MCTP standards specifically the DSP0236 Management Component Transport Protocol (MCTP) Base Specification and the associated binding specifications.

5.1 Sideband Management Interface and Transport

OCP NIC 3.0 sideband management interfaces are used by a Management Controller (MC) or Baseboard Management Controller (BMC) to communicate with the OCP NIC 3.0 card. Table 55 summarizes the sideband management interface and transport requirements.

Table 55: Sideband Management Interface and Transport Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
NC-SI compliant RMII Based Transport (RBT) including physical interface defined in Section 10 of DMTF DSP0222	Required	Required	N/A
Management Component Transport Protocol (MCTP) Base Transport (DSP0236 compliant)	Required	N/A	Required
I^2C compliant physical interface for FRU EEPROM	Required	Required	Required
SMBus 2.0 compliant physical interface	Required	N/A	Required
Management Component Transport Protocol (MCTP) over MCTP/SMBus Binding (DSP0237 compliant)	Required	N/A	Required
Management Component Transport Protocol (MCTP) over MCTP/PCIe VDM Binding (DSP0238 compliant)	Optional	N/A	Optional
Management Component Transport Protocol (MCTP) over USB Binding (DSP0283 compliant)	Optional	N/A	Optional

5.2 NC-SI Traffic

DMTF DSP0222 defines two types of NC-SI traffic: Pass-Through and Control. Table 56 summarizes the NC-SI traffic requirements.

Table 56: NC-SI Traffic Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
NC-SI Control over RBT (DMTF DSP0222 compliant)	Required	Required	N/A
NC-SI Control over MCTP (DMTF DSP0261 compliant)	Required	N/A	Required
NC-SI Pass-Through over RBT (DMTF DSP0222 compliant)	Required	Required	N/A
NC-SI Pass-Through over MCTP (DMTF DSP0261 compliant)	Optional	N/A	Optional

Note: A Management Controller (MC) is allowed to use NC-SI Control traffic only without enabling NC-SI pass-through.

5.3 Management Controller (MC) MAC Address Provisioning

An OCP NIC 3.0 compliant card that supports NC-SI pass-through shall provision one or more MAC addresses per Package (refer to the Package definition as detailed in the DMTF DSP0222 specification) for Out-Of-Band (OOB) management traffic. The number of MC MAC addresses provisioned is implementation dependent. These MAC addresses are not exposed to the host(s) as available MAC addresses. The MC is not required to use these provisioned MAC addresses. Table 57 summarizes the MC MAC address provisioning requirements. A MAC address algorithm calculator is provided on the OCP NIC 3.0 wiki page and may be downloaded from: https://www.opencompute.org/wiki/Server/NIC.

Table 57: MC MAC Address Provisioning Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
One or more MAC Addresses per package shall be provisioned for the MC. The OCP NIC 3.0 platform may choose to use the NIC vendor allocated MAC addresses for the BMC. The usage of provisioned MAC addresses is BMC implementation specific and is outside the scope of this specification. Refer to Section 5.3.1 for the recommended MAC address allocation scheme.	Required	Required	Optional
For multi-host capable OCP NIC 3.0 cards, the MAC addresses shall be provisioned for the maximum number of supported hosts. Refer to Section 5.3.2 for the recommended MAC address allocation scheme.	Required	Required	Required
Support at least one of the following mechanisms for provisioned MC MAC Address retrieval:	Required	Required	Optional

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
• NC-SI Control/RBT (DMTF DSP0222 compliant) • NC-SI Control/MCTP (DMTF DSP0261 compliant) **Note:** This capability is planned to be included in revision 1.2 of the DSP0222 NC-SI specification. For DMTF DSP0222 1.1 compliant OCP NIC 3.0 implementations, MC MAC address retrieval shall be supported using NC-SI OEM commands. An OCP NIC 3.0 implementation, that is compliant with DMTF DSP0222 that defines standard NC-SI commands for MC MAC address retrieval, shall support those NC-SI commands.			

5.3.1 MAC Address Allocation Scheme

The recommended MAC address allocation scheme is stated below. This algorithm assumes all of the port MAC addresses are sequentially allocated first, followed by the BMC MAC addresses. For multi-host capable cards, the MAC addresses shall be provisioned for the maximum number of supported hosts.

Assumptions:

1. The number of BMCs or virtual BMCs is the same as the number of hosts (1:1 relationship between each host and the BMC).
2. The maximum number of partitions on each port is the same.

Variables:

- `num_ports` – Number of Ports on the OCP NIC 3.0 card
- `max_parts` – Maximum number of partitions on a port per host
- `num_hosts` – Number of hosts supported by the NIC
- `first_addr` – The MAC address of the first host for the first partition on the first port
- `host_addr[i]` – base MAC address of ith host (`0 ≤ i ≤ num_hosts-1`)
- `bmc_addr[i]` – base MAC address of ith BMC (`0 ≤ i ≤ num_hosts-1`)

Formula:

- host_addr[i] = first_addr + i*num_ports*max_parts

The assignment of MAC address used by i^{th} host on port j for the partition k is out of the scope of this specification.

- bmc_addr[i] = first_addr + num_ports*max_parts*num_hosts + i*num_ports

The MAC address used by i^{th} BMC on port j, where 0 ≤ i ≤ num_hosts-1 and 0 ≤ j ≤ num_ports -1 is bmc_addr[i] + j

5.3.2 MAC Address Allocation Scheme for Multi-Host Capable NICs

This algorithm is used for multi-host capable OCP NIC 3.0 NICs. The algorithm assumes each host and port MAC address combination shall have a corresponding BMC MAC address allocated in sequential order.

Variables:

- `num_ports` – Number of Ports on the OCP NIC 3.0 card
- `max_parts` – Maximum number of partitions on a port per host
- `num_hosts` – Number of hosts supported by the NIC
- `first_addr` – The MAC address of the first host for the first partition on the first port
- `host_addr[i][j]` – base MAC address of ith host for the jth port
- `bmc_addr[i][j]` – base MAC address of ith BMC for the jth port
- `i` is the host number (`0 ≤ i ≤ num_hosts-1`)
- `j` is the port number (`0 ≤ j ≤ num_ports-1`)
- `k` is the partition number (`0 ≤ k ≤ max_parts-1`)

Formula:

- host_addr[i][j] = first_addr + i*(max_parts+1)*num_ports + j
- bmc_addr[i][j] = first_addr + i*(max_parts+1)*num_ports + max_parts*num_ports + j

The assignment of MAC address used by i^{th} host on port j for the partition k is out of the scope of this specification.

5.4 ASIC Die Temperature Reporting

An OCP NIC 3.0 implementation can have several silicon components including one or more ASICs implementing NIC functions. For the system management, it is important that the die temperatures of these ASIC components can be retrieved over sideband interfaces. The ASIC die temperature reporting requirements of this section are independent of the transceiver module temperature reporting discussed in Section 5.6.

The temperature reporting interface shall be accessible in Aux Power Mode, and Main Power Mode. Table 59 summarizes temperature reporting requirements. These requirements improve the system thermal management and allow the baseboard management device to access key component temperatures on an OCP NIC 3.0 card. When the temperature reporting function is implemented, it is required that the temperature reporting accuracy is within ±3 °C.

As an example, the assumed hysteresis value for any threshold deassertion is 2 °C. For the three upper severity levels (Warning, Critical and Fatal), the thresholds shall be no less than the reporting accuracy of the temperature sensor (±3 °C) plus the hysteresis value. Therefore, the minimum temperature delta between thresholds should be 5 °C. Larger temperature deltas between severity levels are permitted.

- The Fatal threshold should be set to the temperature at which the silicon may experience permanent failures.
- The Critical threshold should be set to the temperature at which degraded performance or transient errors may occur for the silicon. The life span of the product may be impacted. At minimum, the Critical threshold shall be at least 5 °C below Fatal.

- The Warning threshold should be set to at least 5 °C below Critical and set accordingly to the NIC vendor to give an early indication that the server needs to take remedial action to increase cooling capacity.

To illustrate this concept, the following example shows a silicon device with an operating Tj of 105 °C per the device datasheet and card temperature reporting accuracy of ±3 °C. The Upper Fatal threshold is fixed to the upper device temperature before immediate physical damage is incurred. These threshold values can be adjusted when the card temperature sensor reporting accuracy is better than ±3 °C.

Table 58: Threshold Severity Level vs Example Threshold Values

Threshold Severity Level	Example Threshold Value (°C)
Upper Fatal	115
Upper Critical	105
Upper Warning	100

For the severity levels above, each baseboard shall ensure the card fatal thermal limit is not exceeded. In ID Mode, baseboard shall determine if the card present in the OCP NIC 3.0 slot is thermally supportable for the thermal tier as defined in the FRU contents.

Table 59: Temperature Reporting Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
ASIC die temperature reporting for a component with TDP ≥5 W	Required	Required	Required
ASIC die temperature reporting for a component with TDP < 5 W	Recommended	Recommended	Recommended
When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall support PLDM for Platform Monitoring and Control (DSP0248 compliant) for temperature reporting. Additionally, refer to DSP2054 for the PLDM NIC Modeling scheme.	Required	Required	Required
When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall report upper warning, upper critical, and upper fatal thresholds for PLDM numeric sensors. Note: Refer to DSP0248 for definitions of the upper warning, upper critical, and upper fatal thresholds. Additionally, refer to DSP2054 for the PLDM NIC Modeling scheme.	Required	Required	Required
When the temperature reporting function is implemented using PLDM numeric sensors, the temperature tolerance shall be reported as part of the sensor Platform Descriptor Record (PDR) format.	Required	Required	Required
Support for self-shutdown. Refer to Section 5.4.1 for the feature description.	Optional	Optional	Optional

5.4.1 Self-Shutdown

The purpose of the self-shutdown feature is to “self-protect” the NIC ASIC from permanent damage due to high operating temperatures. The NIC may accomplish this by reducing the power consumed by the ASIC. A BMC may continuously monitor the NIC ASIC temperature and shutdown the NIC ASIC as soon as the temperature reaches a threshold value.

There may be scenarios and implementations where the OCP NIC ASIC may be required to self-shutdown without depending on an external entity like the BMC. For those scenarios and implementations, the self-shutdown feature is a final effort in preventing permanent damage to the NIC ASIC at the expense of potential data loss.

If the self-shutdown feature is implemented, the NIC ASIC shall monitor its temperature and shutdown itself as soon as the self-shutdown threshold value is reached. The value of the self-shutdown threshold is implementation specific. It is recommended that the self-shutdown threshold value is higher than the maximum junction temperature of the ASIC implementing the NIC function. It is also recommended that the self-shutdown threshold value is between the critical and fatal temperature thresholds of the ASIC.

If the self-shutdown feature is implemented, care shall be taken to ensure that the board power down state is latched, and the board does not autonomously resume normal operation.

The OCP NIC 3.0 card does not need to know the reason for the NIC ASIC self-shutdown threshold crossing (e.g., fan failure). After the NIC ASIC enters the self-shutdown state, the OCP NIC 3.0 card may not be operational. This might cause the system with the OCP NIC 3.0 card to become unreachable via the NIC.

To recover the NIC ASIC from the self-shutdown state, the OCP NIC 3.0 card shall go through the NIC ID Mode state as described in Section 4.9.1.

If the self-shutdown feature is implemented, the implementation shall provide a mechanism to enable/disable the feature.

Note: It is assumed that a system management function will prevent a component from reaching its fatal threshold temperature.

5.5 Power Consumption Reporting

An OCP NIC 3.0 implementation may be able to report the power consumed at the board level. It is important for the system management that the information about the power consumption can be retrieved over sideband interfaces. Table 60 summarizes the power consumption reporting requirements.

Table 60: Power Consumption Reporting Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
Board Only Estimated Power Consumption Reporting. The value of this field is encoded into the FRU EEPROM contents. This field reports the board max power consumption value without transceivers plugged into the line side receptacles.	Required	Required	Required

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
Pluggable Transceiver Module Power Reporting. The pluggable transceivers plugged into the line side receptacles shall be inventoried (via an EEPROM query) and the Power Class of the module shall be reported.	Required	Required	Required
Board Runtime Power Consumption Reporting. This value shall be optionally reported over the management binding interface. The runtime power value shall report the card edge power.	Optional	Optional	Optional
PLDM for Platform Monitoring and Control (DSP0248 compliant) shall be used for transceiver and board power consumption reporting.	Required	Required	Required

5.6 Pluggable Transceiver Module Status and Temperature Reporting

A pluggable transceiver module is a compact, hot-pluggable transceiver used to connect the OCP 3.0 NIC to an external physical medium. It is important for proper system operation to know the presence and temperature of pluggable transceiver modules. Table 61 summarizes pluggable module status reporting requirements. The transceiver temperature is always reported and is independent of the ASIC die temperature reporting requirements as discussed in Section 5.3.1. The temperature reporting interface shall be accessible in Aux Power Mode, and Main Power Mode.

Table 61: Pluggable Module Status Reporting Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
Pluggable Transceiver modules Presence Status and Temperature Reporting	Required	Required	Required
PLDM for Platform Monitoring and Control (DSP0248 compliant) for reporting the pluggable transceiver module presence status and pluggable transceiver module temperature	Required	Required	Required

5.7 Management and Pre-OS Firmware Inventory and Update

An OCP NIC 3.0 implementation can have different types of firmware components for data path, control path, and management path operations. It is desirable that OCP NIC 3.0 implementations support an OS-independent mechanism for the management firmware update. It is desirable that the management firmware update does not require a system reboot for the new firmware image to become active. Table 62 summarizes the firmware inventory and update requirements.

Table 62: Management and Pre-OS Firmware Inventory and Update Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
Network boot in UEFI driver (supporting both Ipv4 and Ipv6 addressing for network boot)	Required	Required	Required
UEFI secure boot for UEFI drivers	Required	Required	Required
UEFI Firmware Management Protocol (FMP)	Required	Required	Required
PLDM for Firmware Update (DSP0267 compliant)	Required	Recommended	Required

5.7.1 Secure Firmware

It is highly recommended that an OCP NIC 3.0 card supports a secure firmware feature. In the future versions of the OCP NIC 3.0 specification, the secure firmware feature is intended to be required. When the secure firmware feature is enabled and where export compliance permits, the OCP NIC 3.0 card shall verify firmware components prior to the execution, execute only signed and verified firmware components, and only allow authenticated firmware updates. Where applicable, an OCP NIC 3.0 implementation shall use the guidelines provided in NIST SP 800-193 Platform Resiliency Guidelines for the following secure firmware functions:

- Signed Firmware Updates
- Ensure only valid/authenticated firmware updates can be applied. Refer to: NIST 800-193 Section 3.5 Firmware Update Mechanisms, and 4.1.2 Root of Trust for Update (RTU) and Chain of Trust for Update (CTU)
- Ensure authentication mechanisms cannot be bypassed. Refer to NIST 800-193 Section 4.2 Protection.
- Secure Boot
- Only boot trusted/authenticated firmware: NIST 800-193 4.1.3 Root of Trust for Detection (RTD) and Chain of Trust for Detection (CTD), and Section 4.3 Detection
- Recovery mechanism in case of boot failure: NIST 800-193 Section 4.4 Recovery

5.7.2 Firmware Inventory

The OCP NIC 3.0 card shall allow queries to obtain the firmware component versions, device model, and device ID via in-band and out-of-band interfaces without impacting NIC function and performance of said paths.

5.7.3 Firmware Inventory and Update in Multi-Host Environments

A multi-host capable OCP NIC 3.0 card shall gracefully handle concurrent in-band queries from multiple hosts and out-of-band access from the BMC for firmware component versions, device model, and device ID information.

A multi-host capable OCP NIC 3.0 card shall only permit one entity to perform write accesses to NIC firmware at a time, without creating contention.

A multi-host capable OCP NIC 3.0 card shall gracefully handle exceptions when more than one entity attempts to perform concurrent NIC firmware writes.

5.8 NC-SI Package Addressing and Hardware Arbitration Requirements

NC-SI over RBT is implemented via RMII pins between the MC and the OCP NIC 3.0 card. Protocol and implementation details of NC-SI over RBT can be found in the DMTF DSP0222 standard.

5.8.1 NC-SI over RBT Package Addressing

NC-SI over RBT capable OCP NIC 3.0 cards shall use a unique Package ID per ASIC when multiple ASICs share the single NC-SI physical interconnect to ensure there are no addressing conflicts.

Baseboards use the Slot_ID[1:0] values on the Primary Connector for this identification. The value of Slot_ID[1:0] is determined by the encoding shown in Table 63. SLOT_ID[1:0] is statically set high or low on the baseboard and is available on the OCP Bay portion of the Primary Connector.

Table 63: Slot_ID[1:0] to Package ID[2:0] Mapping

Physical Slot (Dec.)	SLOT_ID[1:0]		Package ID[2:0]		
	Pin OCP_A6	Pin OCP_B7	Package ID[2]	Package ID[1]	Package ID[0]
	SLOT_ID1	SLOT_ID0	PhysDev#	SLOT_ID1	SLOT_ID0
Slot 0	0	0	0/1	0	0
Slot 1	0	1	0/1	0	1
Slot 2	1	0	0/1	1	0
Slot 3	1	1	0/1	1	1

Package ID[2:0] is a 3-bit field and is encoded in the NC-SI Channel ID as bits [7:5]. SLOT_ID1 is associated with Package ID[1]. SLOT_ID0 is associated with Package ID[0]. The Package ID[2] value is based on the silicon instance on the same physical OCP NIC 3.0 card. Package ID[2]==0b0 is assigned for physical controller #0. Package ID[2]==0b1 is assigned for physical controller #1. In this case, physical controller #1 on the same card is at an address offset of +0x4. Refer to the specific endpoint device datasheet for details on the Package ID configuration options.

Note: The Package ID[2] field is optionally configurable in the NC-SI specification. If the target silicon hard codes this bit to 0b0, then a card must only implement a single silicon instance to prevent addressing conflicts when RBT is enabled.

Refer to the DMTF DSP0222 standard for more information on package addressing and Package ID.

5.8.2 Arbitration Ring Connections

For baseboards that implement two or more Primary Connectors, the NC-SI over RBT arbitration ring shall be connected to each other. The arbitration ring shall support operation with one card, or multiple cards installed. Figure 108 shows an example connection with dual Primary Connectors.

5.9 SMBus 2.0 Addressing Requirements

The SMBus provides a low-speed management bus for the OCP NIC 3.0 card. The FRU EEPROM is directly connected to the OCP NIC 3.0 card edge on this bus and can be read by the baseboard in the ID Mode, Aux Power Mode and Main Power Mode. Network controllers may utilize the SMBus 2.0 interface for MCTP communications. OCP NIC 3.0 does not support MCTP over I^2C due to the use of specific SMBus 2.0 addressing. Proper power domain isolation shall be implemented on the NIC.

5.9.1 SMBus Address Map

OCP NIC 3.0 cards shall support the SMBus Address Resolution Protocol (ARP). This allows for dynamic assignment of target device addresses. This method automatically resolves address conflicts and eliminates the need for manual address configuration. The SMBus address type can be either a Dynamic and Persistent Address or a Dynamic and Volatile Address. Refer to the SMBus 2.0 specification and Section 6.11 of DSP0237 for details on SMBus address assignment. Due to the prevalent use of SMBus multiplexers in many baseboard designs, the OCP NIC 3.0 card is discouraged from sending unsolicited messages, which includes the optional "Notify ARP Controller" command.

A baseboard implementation may choose to only use fixed addresses for OCP NIC 3.0 cards. The assignment of these fixed addresses is system dependent and is outside the scope of this specification. When fixed addresses are used, then the OCP NIC 3.0 card shall be a "Fixed and Discoverable" SMBus device. Refer to the SMBus 2.0 specification for more details.

All predefined SMBus addresses for OCP NIC 3.0 are shown in Table 64. Baseboard and OCP NIC 3.0 card designers must ensure additional devices do not conflict (such as on a multi-controller NIC on SMBus0). The addresses shown are in 8-bit format and represent the read/write address pair.

For a DSFF implementation, the FRU EEPROM address are only set by the Slot 0 and Slot 2 SLOT_ID[1:0] pins. DSFF cards physically occupy the space for Slot 0 + Slot 1, and Slot 2 + Slot 3 as shown in Figure 114. The SLOT_ID[3:2] pins are not used to set the FRU EEPROM address.

Table 64: FRU EEPROM Address Map

Physical Slot (Dec.)	SLOT_ID[1:0]		FRU EEPROM Address				
	Pin OCP_A6	Pin OCP_B7	A2	A1	A0	Binary Address	Hex Address
	SLOT_ID1	SLOT_ID0	SLOT_ID1	SLOT_ID0	Fixed		
Slot 0	0	0	0	0	0	0b1010_000X	0xA0/0xA1
Slot 1	0	1	0	1	0	0b1010_010X	0xA4/0xA5
Slot 2	1	0	1	0	0	0b1010_100X	0xA8/0xA9
Slot 3	1	1	1	1	0	0b1010_110X	0xAC/0xAD

5.10 FRU EEPROM

5.10.1 FRU EEPROM Addressing and Size

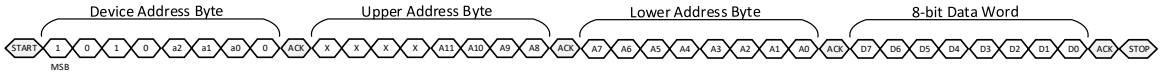
A FRU EEPROM is implemented on the OCP NIC 3.0 cards and is used by the baseboard to determine the card type and capabilities. The FRU EEPROM is directly connected to the SMBus on the card edge. Only one EEPROM is required for a single physical OCP NIC 3.0 card regardless of the PCIe width or number of physical card edge connectors it occupies. The FRU EEPROM is mandatory and shall be connected to the Primary Connector SMBus.

The FRU EEPROM is readable in all four power states: ID mode, Programming mode, Aux Power Mode, and Main Power Mode.

The permissible EEPROM addresses are indicated in Table 64. The write/read pair is presented in 8-bit format. The EEPROM shall use double byte addressing and, at minimum, shall be of sufficient size to hold the base FRU contents and any vendor specific information. The double byte write and read accesses are shown in Figure 135 and Figure 136. Refer to the I^2C specification for timing details.

Figure 135: FRU EEPROM Writes with Double Byte Addressing

Byte Write



Page Write

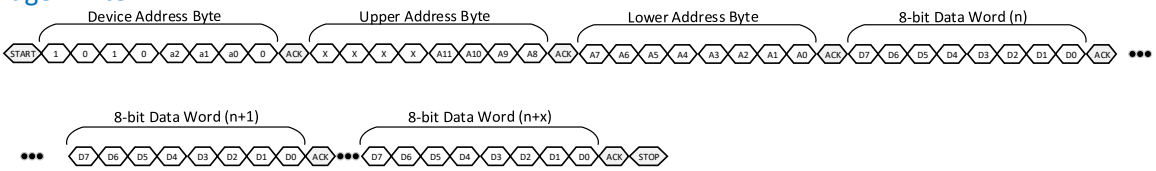
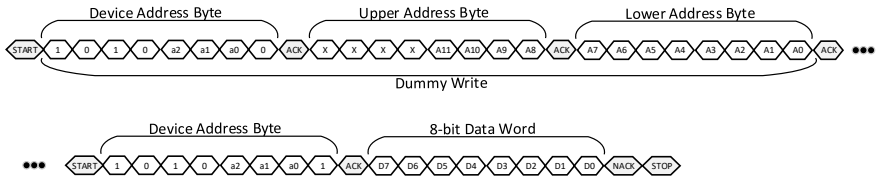


Figure 136: FRU EEPROM Reads with Double Byte Addressing

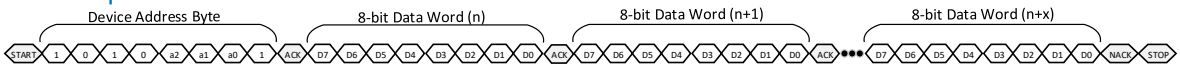
Random Read



Current Address Read



Current Sequential Read

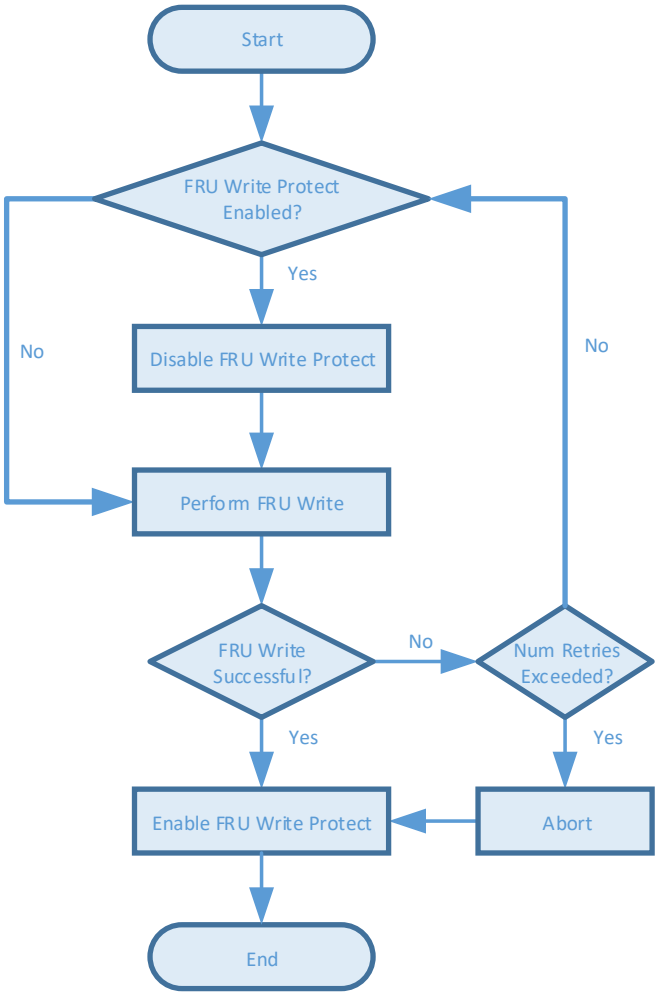


5.10.2 FRU EEPROM Write Protection

The FRU EEPROM should be write-protected for production cards. The FRU write protection may optionally be overridden for field updates via the use of a mechanical jumper or switch, a GPIO, controlled via a NC-SI or PLDM based mechanism, or the Programming Mode Power state. An OCP NIC 3.0 card may implement one or more of these write protection implementations. The definitions of these mechanisms are outside the scope of this specification. The NIC vendor write protection mechanism(s) shall be noted in the OEM Record. The FRU shall be writable for Programming mode power state, manufacturing test and during the card development cycle.

The FRU update flow is shown in Figure 137.

Figure 137: FRU Update Flow



5.10.3 FRU EEPROM Content Requirements

The FRU EEPROM shall follow the data format specified in Section 1 of the IPMI Platform Management FRU Information Storage Definition specification. For OCP NIC 3.0, the FRU Information Device shall, at a minimum, contain the Common Header, Board Info Area, Product Info Area and a MultiRecord Area for storing the OCP NIC OEM record(s). These fields shall be populated in the FRU EEPROM. Where applicable, fields common to the Board Info and Product Info records shall be populated with the same values so they are consistent.

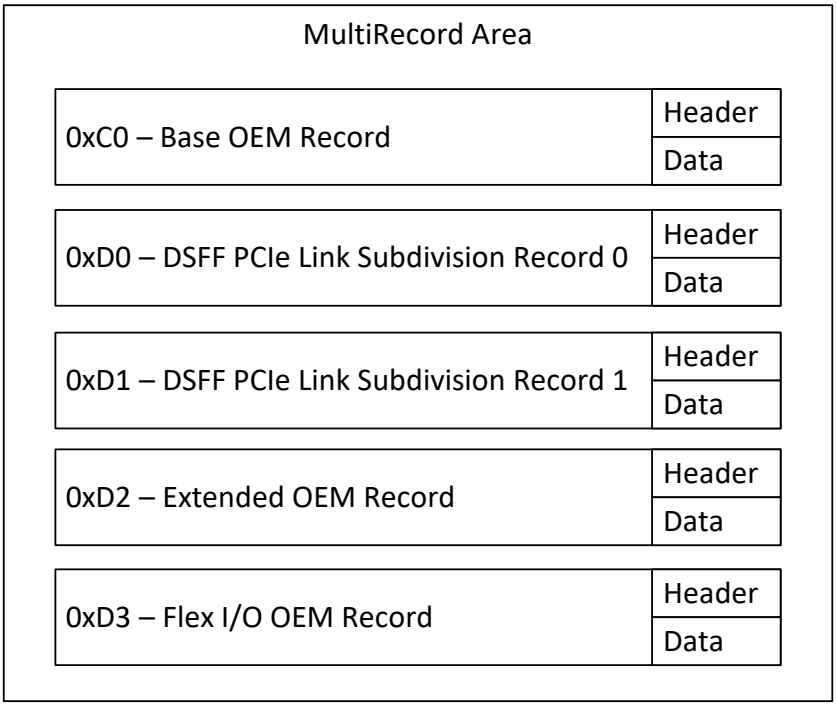
There are several defined records in the OCP NIC 3.0 MultiRecord Area. Table 65 shows the OEM record requirements for each form factor.

For offsets that span multiple bytes, the lower ordered offset is the least significant byte, and the upper ordered offset is the most significant byte.

Table 65: OCP NIC 3.0 MultiRecord Requirements

Record Offset / Name	SFF	DSFF	LFF
0xC0 – Base OEM Record	Required	Required	Required
0xD0 – DSFF PCIe Link Subdivision Record 0	Not Used	Required	Not Used
0xD1 – DSFF PCIe Link Subdivision Record 1	Not Used	Optional	Not Used
0xD2 – Extended OEM Record	Not Used	Required	Not Used
0xD3 – Flex I/O OEM Record	Optional	Optional	Not Used

Figure 138: OCP NIC 3.0 MultiRecord Structure



Note 1: Figure 138 only show the MultiRecord Area OEM Records. The complete MultiRecord is defined in Section 16 of the IPMI Platform Management FRU Information Storage Definition specification.

Note 2: Each OEM Record contains an OCP NIC 3.0 OEM Record Version field. This field shall be read by the Baseboard and compared against the corresponding version of the OCP NIC 3.0 specification as the OEM Record field definition(s) may have changed between specification revisions.

Note 3: As of version 1.6.0 of this specification, the OEM Record offsets are now maintained by the OCP Modular Hardware Systems (MHS) Type ID allocation document. A link to this file can be found on the MHS Hardware Management GitHub repository. See: https://github.com/opencomputeproject/OCP-HM-Hardware_Management

5.10.3.1 Base OEM Record (0xC0)

OEM record 0xC0 is used to store specific data fields for the OCP NIC 3.0 card form-factors and is in the MultiRecord Area of the FRU EEPROM. For an OCP NIC 3.0 card, the Base OEM record content is defined in Table 66. This record shall be populated on all card versions.

Table 66: Base OEM Record – 0xC0

Offset	Length	Description
0	3	Manufacturer ID. For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 42623 in decimal or 0x00A67F in hexadecimal. The least significant byte (0x7F) is first at offset 0 and the most significant byte (0x00) is at offset 2.
3	1	OCP NIC 3.0 OEM Record Version. This field indicates the card OEM Record Version. Baseboards shall read this field to determine the OEM Record format. OCP NIC 3.0 cards compliant to this version of the specification shall be set to the latest entry noted in this field. Future changes to the OEM Record format will result in an additional record version value added to this list. 0x00 – Reserved 0x01 – OCP NIC 3.0 card FRU record released with version 0.9.0 0x02 – OCP NIC 3.0 card FRU record released with version 1.1.0 0x03 – OCP NIC 3.0 card FRU record released with version 1.3.0 0x04 – OCP NIC 3.0 card FRU record released with version 1.4.5 0x05 – OCP NIC 3.0 card FRU record released with version 1.5.0 0x06 – OCP NIC 3.0 card FRU record released with version 1.6.0 0x07 – 0xFF – Reserved
4	1	Card Max power (in Watts) in Main Power Mode. The encoded value is the calculated max power of the OCP NIC 3.0 card in the Main Power Mode only and does not include the consumed power by transceivers plugged into the line side receptacle(s). 0x00 – 0xFE – Card power rounded up to the nearest Watt for fractional values. 0xFF – Unknown
5	1	Card Max power (in Watts) in Aux Power Mode.

Offset	Length	Description
		The encoded value is the calculated max power of the OCP NIC 3.0 card in the Aux Power Mode only and does not include the consumed power by transceivers plugged into the line side receptacle(s). 0x00 – 0xFE – Card power rounded up to the nearest Watt for fractional values. 0xFF – Unknown
6	1	Hot Aisle Card Cooling Tier with Passive Cables or RJ45. The encoded value reports the OCP NIC 3.0 Card Hot Card Cooling Tier as defined in Section 7.6 for cards with passive pluggable cables or with RJ45 for the line side I/O. 0x00 – Reserved 0x01 – Hot Aisle Cooling Tier 1 0x02 – Hot Aisle Cooling Tier 2 0x03 – Hot Aisle Cooling Tier 3 0x04 – Hot Aisle Cooling Tier 4 0x05 – Hot Aisle Cooling Tier 5 0x06 – Hot Aisle Cooling Tier 6 0x07 – Hot Aisle Cooling Tier 7 0x08 – Hot Aisle Cooling Tier 8 0x09 – Hot Aisle Cooling Tier 9 0x0A – Hot Aisle Cooling Tier 10 0x0B – Hot Aisle Cooling Tier 11 0x0C – Hot Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown
7	1	Cold Aisle Card Cooling Tier with Passive Cables or RJ45. The encoded value reports the OCP NIC 3.0 Card Cold Aisle Cooling Tier as defined in Section 7.6 for cards with passive pluggable cables or with RJ45 for the line side I/O. 0x00 – Reserved 0x01 – Cold Aisle Cooling Tier 1 0x02 – Cold Aisle Cooling Tier 2 0x03 – Cold Aisle Cooling Tier 3 0x04 – Cold Aisle Cooling Tier 4 0x05 – Cold Aisle Cooling Tier 5 0x06 – Cold Aisle Cooling Tier 6 0x07 – Cold Aisle Cooling Tier 7 0x08 – Cold Aisle Cooling Tier 8 0x09 – Cold Aisle Cooling Tier 9 0x0A – Cold Aisle Cooling Tier 10 0x0B – Cold Aisle Cooling Tier 11 0x0C – Cold Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown
8	1	Card active/passive cooling. This byte defines if the card has passive cooling (there is no fan on the card) or active cooling (a fan is located on the card). 0x00 – Passive Cooling 0x01 – Active Cooling 0x02 – 0xFE – Reserved 0xFF – Unknown

Offset	Length	Description
9	2	Hot aisle standby airflow requirement with Active Cables. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with active cables while operating in a hot aisle environment with an approach air temperature of 45 °C. Refer to Section 7 for more information about the thermal and environmental requirements. 0x0000 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) 0x0001 – 0xFFFE – LFM required for cooling card in Hot Aisle Operation. 0xFFFF – Unknown.
11	2	Cold aisle standby airflow requirement with Active Cables. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with active cables while operating in a cold aisle environment with an approach air temperature of 35 °C. Refer to Section 7 for more information about the thermal and environmental requirements. Byte 11 is the least significant byte, byte 12 is the most significant byte. 0x0000 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) 0x0001 – 0xFFFE – LFM required for cooling card in Cold Aisle Operation. 0xFFFF – Unknown.
13	1	UART Configuration 1 – Secondary Connector. **Note:** SFF and DSFF cards do not have UART pins, and this byte shall be set to 0x00. This field was only applicable to the LFF and has since been deprecated. This byte denotes the UART configuration 1. A value 0x00 means no serial connection is implemented on the Secondary Connector card edge. Bits [2:0] denotes the UART baud rate per the encoding table below. If implemented, the encoded field value defines the default baud rate of the OCP NIC 3.0 card serial port. 0b000 – No serial connection 0b001 – 115200 baud 0b010 – 57600 baud 0b011 – 38400 baud 0b100 – 19200 baud 0b101 – 9600 baud 0b110 – 4800 baud 0b111 – 2400 baud Bits [4:3] denotes the number of data bits. 0b00 – No serial connection 0b01 – 7 data bits 0b10 – 8 data bits 0b11 – Reserved Bits [7:5] denotes the parity bit character. 0b000 – No serial connection 0b001 – None (N) 0b010 – Odd (O) 0b011 – Even (E) 0b100 – Mark (M) 0b101 – Space (S) 0b110 – Reserved 0b111 – Reserved
14	1	UART Configuration 2 – Secondary Connector.

Offset	Length	Description
		Note: SFF and DSFF cards do not have UART pins, and this byte shall be set to 0x00. This field was only applicable to the LFF and has since been deprecated. This byte denotes the UART configuration 2. A value 0x00 means no serial connection is implemented on the Secondary Connector card edge. Bits [1:0] denotes the number of stop bits. 0b00 – No serial connection 0b01 – 1 stop bit 0b10 – 1.5 stop bits 0b11 – 2 stop bits Bits [3:2] denotes the flow control method. 0b00 – No serial connection 0b01 – Software handshaking 0b10 – No handshaking 0b11 – Reserved Bits [7:4] are reserved and shall be encoded to a value of 0b0000.
15	1	USB Present – Primary Connector. This byte denotes a USB 2.0 connection is implemented on the Primary Connector card edge. 0x00 – No USB 2.0 is present or is not implemented on the card edge. 0x01 – A USB 2.0 connection is implemented on the card edge. 0x02 – 0xFE – Reserved for future use. 0xFF – Unknown
16	1	Manageability Type. This byte denotes the card manageability type and interface used. A value of 0x00 means there is no manageability. More than one manageability type may be simultaneously enabled. Refer to Section 5 for valid combinations and supported MCTP bindings. Bit 0 – RBT Type Bit 1 – MCTP/SMBus (DSP0237 compliant) Bit 2 – MCTP/PCIe VDM (DSP0238 compliant) Bit 3 – MCTP/USB (DSP0283 compliant) Bit 4 – USB Communication Device Class **Note:** The USB Communication Device Class shall be queried and discovered from the NIC once the interface is enabled, and the card is in the Aux Power Mode and Main Power Mode states. Refer to the USB 2.0 specification for details. Bits [5:7] – Reserved for future use. Set to 0b000. 0xFF – Unknown
17	1	FRU Write Protection Mechanism. This byte defines the FRU write protection mechanism implemented on the OCP NIC 3.0 card. Multiple FRU write projection mechanisms may be simultaneously supported on the OCP NIC 3.0 card. Refer to Section 5.10.2 for details. Bit 0 – FRU EEPROM is not write-protected. Bit 1 – FRU EEPROM is statically write-protected. No field updates permissible. Bit 2 – FRU EEPROM is write-protected via a mechanical jumper or switch. Bit 3 – FRU EEPROM write protection is controlled via network silicon GPIO. Bit 4 – FRU EEPROM write protection is controlled via an NC-SI or PLDM based mechanism.

Offset	Length	Description
		Bit 5 – FRU EEPROM write protection is controlled by the Programming Mode power state. Bits [6:7] – Reserved for future use. 0xFF – Unknown.
18	1	Programming Mode Power State Supported. This byte defines support for the Programming Mode power state. If supported, the FRU EEPROM write protect mechanism is disabled for field updates. Refer to Section 4.9 for details on the Programming Mode power state. 0x00 – Programming Mode power state not supported. 0x01 – Programming Mode power state supported. 0x02 – 0xFE – Reserved for future use. 0xFF – Unknown.
19	1	Hot Aisle Card Cooling Tier with Active Cables. The encoded value reports the OCP NIC 3.0 Card Hot Aisle Card Cooling Tier as defined in Section 7.6 for cards with active pluggable cables for the line side I/O. 0x00 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) 0x01 – Hot Aisle Cooling Tier 1 0x02 – Hot Aisle Cooling Tier 2 0x03 – Hot Aisle Cooling Tier 3 0x04 – Hot Aisle Cooling Tier 4 0x05 – Hot Aisle Cooling Tier 5 0x06 – Hot Aisle Cooling Tier 6 0x07 – Hot Aisle Cooling Tier 7 0x08 – Hot Aisle Cooling Tier 8 0x09 – Hot Aisle Cooling Tier 9 0x0A – Hot Aisle Cooling Tier 10 0x0B – Hot Aisle Cooling Tier 11 0x0C – Hot Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown
20	1	Cold Aisle Card Cooling Tier with Active Cables. The encoded value reports the OCP NIC 3.0 Card Cold Aisle Card Cooling Tier as defined in Section 7.6 for cards with active pluggable cables for the line side I/O. 0x00 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) 0x01 – Cold Aisle Cooling Tier 1 0x02 – Cold Aisle Cooling Tier 2 0x03 – Cold Aisle Cooling Tier 3 0x04 – Cold Aisle Cooling Tier 4 0x05 – Cold Aisle Cooling Tier 5 0x06 – Cold Aisle Cooling Tier 6 0x07 – Cold Aisle Cooling Tier 7 0x08 – Cold Aisle Cooling Tier 8 0x09 – Cold Aisle Cooling Tier 9 0x0A – Cold Aisle Cooling Tier 10 0x0B – Cold Aisle Cooling Tier 11 0x0C – Cold Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown

Offset	Length	Description
21	1	Transceiver Reference Power Level. The encoded value denotes the reference power envelope in Watts for active transceivers that was used to determine the card thermal tier. This field is applicable for all supported transceiver types in the OCP NIC form-factor (e.g. SFP, QSFP, OSFP). The encoded value is an unsigned decimal with a resolution of 0.25 W. For example: If the value is encoded is 0x40, then this would represent decimal 64 x 0.25 W = 16.0 W. The active cable power class is defined in the respective module management interface specifications. 0x00 – Field is not used. 0x01 – 0xFE – Represents the maximum supported board transceiver power as an unsigned integer. This field has a resolution of 0.25 W. 0xFF – Unknown.
22	1	Transceiver Reference Temperature Level. The encoded value denotes the reference active transceiver temperature limit, in degrees Celsius, that was used to determine the card thermal tier. 0x00 – Passive Cable 0x01 – 0xFE – Transceiver max operating temperature 0xFF – Unknown
23	1	Card Thermal Tier with Local Fan Fail. The encoded value denotes the required thermal tier when the OCP NIC 3.0 active cooling fails. 0x00 – Card requires the same thermal tier when the active cooling fan fails or the OCP NIC 3.0 card uses passive cooling. 0x01 – Card requires Cooling Tier 1 with card fan failure 0x02 – Card requires Cooling Tier 2 with card fan failure 0x03 – Card requires Cooling Tier 3 with card fan failure 0x04 – Card requires Cooling Tier 4 with card fan failure 0x05 – Card requires Cooling Tier 5 with card fan failure 0x06 – Card requires Cooling Tier 6 with card fan failure 0x07 – Card requires Cooling Tier 7 with card fan failure 0x08 – Card requires Cooling Tier 8 with card fan failure 0x09 – Card requires Cooling Tier 9 with card fan failure 0x0A – Card requires Cooling Tier 10 with card fan failure 0x0B – Card requires Cooling Tier 11 with card fan failure 0x0C – Card requires Cooling Tier 12 with card fan failure 0x0D – 0xFE – Reserved 0xFF – Unknown
24	1	Aux Power Supported Ports. Each bit indicates if the corresponding port can be active in Aux Power Mode. This is a bit map representation. The LSB represents Port 1, the MSB represents Port 8. Refer to Section 4.8.1 for the port numbering nomenclature. Examples: 0b00000000 – No ports are active in Aux Power Mode. 0b00000001 – Only Port 1 can be active in Aux Power Mode. 0b00000010 – Only Port 2 can be active in Aux Power Mode. 0b00000011 – Ports 1 and 2 can be active in Aux Power Mode. Etc.

Offset	Length	Description
25	2	Hot aisle standby airflow requirement with Passive Cables or RJ45. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with passive cables or RJ45 while operating in a hot aisle environment with an approach air temperature of 45 °C. Refer to Section 7 for more information about the thermal and environmental requirements. 0x0000-0xFFFE – LFM required for cooling card in Hot Aisle Operation. 0xFFFF – Unknown.
27	2	Cold aisle standby airflow requirement with Passive Cables or RJ45. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with passive cables or RJ45 while operating in a cold aisle environment with an approach air temperature of 35 °C. Refer to Section 7 for more information about the thermal and environmental requirements. 0x0000-0xFFFE – LFM required for cooling card in Cold Aisle Operation. 0xFFFF – Unknown.
29	1	Maximum Supported Transceiver Power. This byte shall indicate the maximum supported board transceiver power in Watts. This field is applicable for all supported transceiver types in the OCP NIC form-factor (e.g. SFP, QSFP, OSFP). The encoded value is an unsigned decimal with a resolution of 0.25 W. For example: If the value is encoded is 0x40, then this would represent decimal 64 x 0.25 W = 16.0 W. **Note:** This field is purely used as an indicator of maximum supported transceiver power. It is not used for determining the card thermal performance. 0x00 – Field is not used. 0x01 – 0xFE – Represents the maximum supported board transceiver power as an unsigned integer. This field has a resolution of 0.25 W. 0xFF – Unknown.
30	1	Reserved for future use. Set byte to 0xFF for this version of the specification.
31	1	Number of Physical Controllers (N). This byte denotes the number of SMBus connected physical controllers on the OCP NIC 3.0 card. If N=0, no SMBus connected controllers exist on this OCP NIC 3.0 card and this is the last byte in the FRU OEM Record. If N≥1, then the controller UDID records below shall be included for each controller N.
32:47	16	Controller 1 UDID (if applicable). This field reports the Controller 1 Unique Device Identifier (UDID) and is used to aid in the dynamic target address assignment over the SMBus Address Resolution Protocol. The format of the UDID string is defined in the SMBus 2.0 specification. This field shall list the most significant byte first (to align the FRU order to the reported UDID order on the SMBus). This field is populated with the UDID for Controller 1. This field is omitted and is of zero length if controller 1 is not present.
48:63	16	**Controller 2 UDID (if applicable)**. See Controller 1 UDID description above.

Offset	Length	Description
64:79	16	**Controller 3 UDID (if applicable)**. See Controller 1 UDID description above.
80:95	16	**Controller 4 UDID (if applicable)**. See Controller 1 UDID description above.
96:111	16	**Controller 5 UDID (if applicable)**. See Controller 1 UDID description above.
112:127	16	**Controller 6 UDID (if applicable)**. See Controller 1 UDID description above.
128:143	16	**Controller 7 UDID (if applicable)**. See Controller 1 UDID description above.
144:159	16	**Controller 8 UDID (if applicable)**. See Controller 1 UDID description above.

5.10.3.2 DSFF PCIe Link Subdivision Record 0 (0xD0)

OEM record 0xD0 is used to store PCIe Link Subdivision fields for the DSFF card and is shown in Table 67. This record shall only be populated in the FRU on DSFF cards. This record is not used on other card form-factors.

A DSFF card may have one or more PCIe link modes. These link modes are described in an OEM Record instead of a static table. The 0xD0 OEM record allows the baseboard to dynamically parse and comprehend supported modes on the card.

Depending on the card implementation and silicon capabilities, record 0xD0 may apply to 16-lanes (0-15), or to 32-lanes (0-31). This selection is defined in record 0xD2 offset 8. If record 0xD0 only applies to lanes 0-15, and additional record located at 0xD1 may apply.

A PCIe Mode is a specific configuration with PCIe links, the type of link (endpoint or root port from the NIC perspective), and widths of each link. For example, a card that supports 2x16, and each link is an end point. For each PCIe Mode, the link direction, starting/ending lanes of each link are declared.

Table 67: DSFF PCIe Link Subdivision Record 0 – 0xD0

Offset	Length	Description
0	3	Manufacturer ID. For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 42623 in decimal or 0x00A67F in hexadecimal. The least significant byte (0x7F) is first at offset 0 and the most significant byte (0x00) is at offset 2.
3	1	DSFF PCIe Link Subdivision Record Version. This field indicates the card DSFF PCIe Link Subdivision Record 0 Version. Baseboards shall read this field to determine the DSFF PCIe Link Subdivision Record 0 format. OCP NIC 3.0 cards compliant to this version of the specification shall be set to the latest entry noted in this field. Future changes to the OEM Record format will result in an additional record version value added to this list. 0x00 – Reserved. 0x01 – OCP NIC 3.0 card DSFF FRU record released with version 1.4.5. 0x02 – 0xFF – Reserved.
4	1	Number of supported PCIe link Modes. This field defines the number of supported PCIe link modes for this record. This is field is encoded in hexadecimal.

Offset	Length	Description
Implementation Specific	Implementation Specific	PCIe Mode 0 descriptor. See Table 68. This field describes the first PCIe mode descriptor. This field is mandatory.
…	…	…
Implementation Specific	Implementation Specific	Additional PCIe Mode *n* descriptor fields may be added to describe the permissible PCIe configurations for the DSFF card. Refer to Table 68.

The PCIe Mode Descriptor in Table 68 declares the lane to link assignment details. The table does not prevent a NIC to declare invalid lane combinations or detect lane overlaps in link declarations. Board implementers and system designers shall verify the lane declarations are correct after parsing.

Table 68: PCIe Mode Descriptor

Offset	Length	Description
0	1	**PCIe Mode Descriptor Length** (in bytes, including this field)
1	1	PCIe Mode – Number of Supported PCIe Links This field indicates the number of supported PCIe links in this mode. The value range of 1 through 8 are supported. For example, a value 1 indicates a single link (such as 1x32, 1x16, etc.), a value of 2 indicates two links (such as 2x8), a value of 8 indicates eight links (such as 8x4).
2	1	PCIe Mode – BIF Encoding. The BIF encoding may be 3- or 6-bits wide. Refer to the BIF Encoding Width field in Table 70, Offset 9 for details. If the BIF Encoding width is 6-bits wide, all bits shall be defined by the NIC vendor. For cards that support a 3-bit wide BIF encoding: OEM Record 0xD0 shall use Bits[2:0] for defining the bifurcation encoding on the Primary Connector. Bits[5:3] are set to 0b000. OEM Record 0xD1, the BIF encoding shall use bits [5:3] for defining the bifurcation encoding on the Secondary Connector. Bits [2:0] are set to 0b000. Bit [7:6] – Reserved. Set to 0b00. Bits [5:0] – BIF encoding to activate this PCIe Mode. 0xFF – Unknown / Reserved.
3	1	PCIe Mode – Link 0 Configuration. Bit [7:5] – Declares the associated controller instance in the OEM record 0xC0 for Link 0. Bit 4 – Declares if the link is an end point or root port from the NIC perspective. 0b0: Link 0 is an endpoint. 0b1: Link 0 is a root port. Bit 3 – Declares the PERST# signal direction for Link 0. 0b0: PERST# is an input to the NIC. 0b1: PERST is an output from the NIC.

Offset	Length	Description
		Bits [2:0] – Defines the PERST#/REFCLK Association for Link 0. Refer to Section 4.7 for permissible Link to PERST#/REFCLK mapping combinations.
4	1	PCIe Mode – PCIe lane associated with the start of Link 0. Valid values are 0 through 31, encoded in hexadecimal (0x00 through 0x1F).
5	1	PCIe Mode – PCIe lane associated with the end of Link 0. Valid values are 0 through 31, encoded in hexadecimal (0x00 through 0x1F).
…	…	…
(Link *3n* + 3)	1	PCIe Mode – Link *n* Configuration (where n ≥1) Bit [7:5] – Declares the associated controller instance in the OEM record 0xC0 for Link *n*. Bit 4 – Declares if the link is an end point or root port from the NIC perspective. 0b0: Link *n* is an endpoint. 0b1: Link *n* is a root port. Bit 3 – Declares the PERST# signal direction for Link *n*. 0b0: PERST# is an input to the NIC. 0b1: PERST is an output from the NIC. Bits [2:0] – Defines the PERST#/REFCLK Association for Link *n*. Refer to Section 4.7 for permissible Link to PERST#/REFCLK mapping combinations.
(Link 3*n* +4)	1	PCIe Mode – PCIe lane associated with the start of Link *n* (where n ≥1). Valid values are 0 through 31, encoded in hexadecimal (0x00 through 0x1F).
(Link *3n* + 5)	1	PCIe Mode – PCIe lane associated with the end of Link *n* (where n ≥1). Valid values are 0 through 31, encoded in hexadecimal (0x00 through 0x1F).

3994

5.10.3.3 DSFF PCIe Link Subdivision Record 1 (0xD1)

OEM record 0xD1 is used to store PCIe Link Subdivision fields for the DSFF card and is shown in Table 69. This record shall only be populated in the FRU on DSFF cards. SFF and LFF cards do not use this record and shall not be implemented in the respective card FRUs.

This field is only applicable to DSFF cards that have independent control of lanes 16-31. This selection is defined in record 0xD2 offset 8. For further information on the PCIe Link Subdivision record, refer to 5.10.3.5.

Table 69: DSFF PCIe Link Subdivision Record 1 – 0xD1

Offset	Length	Description
0	3	Manufacturer ID. For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 42623 in decimal or 0x00A67F in hexadecimal. The least significant byte (0x7F) is first at offset 0 and the most significant byte (0x00) is at offset 2.
3	1	DSFF PCIe Link Subdivision Record Version. This field indicates the card DSFF PCIe Link Subdivision Record 1 Version. Baseboards shall read this field to determine the DSFF PCIe Link Subdivision Record 1 format. OCP NIC 3.0 cards compliant to this version of the specification shall be set to the latest entry noted in this field. Future changes to the OEM Record format will result in an additional record version value added to this list. 0x00 – Reserved. 0x01 – OCP NIC 3.0 card DSFF FRU record released with version 1.4.5. 0x02 – 0xFF – Reserved.
4	1	Number of supported PCIe link Modes. This field defines the number of supported PCIe link modes for this record. This is field is encoded in hexadecimal.
Implementation Specific	Implementation Specific	PCIe Mode 0 descriptor. See Table 68. This field describes the first PCIe mode descriptor. This field is mandatory.
…	…	…
Implementation Specific	Implementation Specific	Additional PCIe Mode n descriptor fields may be added to describe the permissible PCIe configurations for the DSFF card. Refer to Table 68.

5.10.3.4 Extended OEM Record (0xD2)

OEM record 0xD2 is used to store specific data fields for the DSFF card. The Extended OEM record is shown in Table 70. This record shall only be populated in the FRU on DSFF cards. SFF and LFF cards do not use this record and shall not be implemented in the respective card FRUs.

Table 70: Extended OEM Record – 0xD2

Offset	Length	Description
0	3	Manufacturer ID. For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 42623 in decimal or 0x00A67F in hexadecimal. The least significant byte (0x7F) is first at offset 0 and the most significant byte (0x00) is at offset 2.
3	1	OCP NIC 3.0 OEM Record Version. This field indicates the card Extended OEM Record Version. Baseboards shall read this field to determine the Extended OEM Record format. OCP NIC 3.0 cards compliant to this version of the specification shall be set to the latest entry noted in this field. Future changes to the OEM Record format will result in an additional record version value added to this list. 0x00 – Reserved. 0x01 – OCP NIC 3.0 card DSFF FRU record released with version 1.4.5. 0x02 – OCP NIC 3.0 card DSFF FRU record released with version 1.6.0. 0x03 – 0xFF – Reserved.
4	1	USB Interface Availability. This field defines if the USB 2.0 interface on the DSFF Primary Connector is operational in Aux Power Mode, Main Power Mode, or both. Set the appropriate bit(s) to 0b1 if the appropriate power mode is supported. Bit 0 – The USB 2.0 interface is supported in Aux Power Mode. Bit 1 – The USB 2.0 interface is supported in Main Power Mode. Bits [2:7] – Reserved. Set to 0b00_0000. 0xFF – Unknown.
5	1	DSFF Card Edge Type. This field defines the DSFF card edge definition for power and PCIe connectivity. DSFF cards may have connectivity to the Primary Connector only, or simultaneously to the Primary and Secondary Connectors. DSFF cards implementing up to 16 PCIe lanes and power requirements of less than 80 W, may elect to only require connectivity on the Primary Connector only. Card present connectivity is detected with PRSNTB[3:0]#. PCIe bifurcation may be declared with up to three BIF[2:0]# pins. DSFF cards implementing more than 16 PCIe lanes, or has power requirements of greater than 80 W, are required to connect to the Primary and Secondary Connectors. Card present connectivity is detected with PRSNTB[7:0]#. PCIe bifurcation may be declared with up to all six BIF[5:0]# pins. 0x01 – If set, the DSFF card indicates the card edge connectivity is only on the Primary Connector.

Offset	Length	Description
		0x02 – If set, the DSFF card indicates that the card edge connectivity is on both the Primary and Secondary Connectors. 0xFF – Unknown.
6	1	DSFF Sideband Signal Connectivity on the Secondary Connector. This field defines the sideband signal connectivity on the Secondary Connector for a DSFF card. These bits should be set to 0b0 for most DSFF implementations. Vendor specific implementations may deviate. Set the appropriate bit(s) to 0b1 if the interface is supported on the Secondary Connector. Refer to the specific pinout sections for use case discussions in the DSFF. SMBus, RBT and Scan Chain busses are defined to be used on the Primary Connector only and are not included in this bit field. Note: This field is not applicable if OEM Record 0xD2 Offset 5 declares card edge connectivity only on the Primary Connector. Bit 0 – PWRBRK[1]# supported on Secondary Connector. Bit 1 – WAKE[1]# supported on Secondary Connector. Bit 2 – USB 2.0 [1] is supported on the Secondary Connector. Bits [3:7] – Reserved. Set to 0b00. 0xFF – Unknown.
7	1	Number of PCIe Lanes. This field declares the number of PCIe lanes implemented on the DSFF card. The valid range is 1 through 32. This is field is encoded in hexadecimal.
8	1	PCIe Link Subdivision OEM Record Count. This field declares the number of PCIe link subdivision OEM records used on the card. 0x00 – Reserved. 0x01 – A single PCIe Link Subdivision OEM Record at offset 0xD0 is declared for lanes 0 through 31. 0x02 – Two PCIe Link Subdivision OEM Records at offset 0xD0 for lanes 0 through 15 and at offset 0xD1 lanes 16 through 31. 0x03-0xFF – Reserved.
9	1	BIF Encoding Width. This field defines the BIF encoding width to activate a given PCIe Mode. The BIF encoding may be 3- or 6-bits wide. This field is applicable to the entire card. The actual value and is defined in the BIF Encoding field for each PCIe Mode *n* descriptor in record 0xD0/0xD1 (Refer to Sections 5.10.3.2 and 5.10.3.3). Bits [2:0] correspond to BIF[2:0] from the Primary Connector and is mandatory on the DSFF. Bits [5:3] correspond to BIF[5:3] from the Secondary Connector and is optionally implemented on the DSFF. 0x00 – Reserved. 0x01 – BIF encoding width is 6-bits. The baseboard shall assert the BIF pins on both the Primary and Secondary Connector when selecting a PCIe Mode. BIF bits [5:0] correspond to 0xD0. 0xD1 is not used. 0x02 – BIF encoding width is 3-bits. The baseboard may assert independent BIF pin values between the Primary and Secondary Connector when selecting appropriate PCIe Modes. BIF bits [2:0] in 0xD0 are used to select the PCIe bifurcation on the Primary Connector, bits [5:3] in 0xD1 are used to select the PCIe bifurcation on the

Offset	Length	Description
		Secondary Connector. 0x03-0xFF – Reserved.

5.10.3.5 Flex I/O OEM Record (0xD3)

OEM record 0xD3 is used to store specific data that describe the Flex I/O feature. The Flex I/O OEM Record is shown in Table 71. This record shall only be populated in the FRU on OCP NIC cards that support Flex I/O on the RBT pins.

The propagation delay fields may optionally be used by systems to account for the transmit and receive frequency and synchronization delays of the OCP NIC card.

Table 71: Flex I/O OEM Record – 0xD3

Offset	Length	Description
0	3	Manufacturer ID. For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 42623 in decimal or 0x00A67F in hexadecimal. The least significant byte (0x7F) is first at offset 0 and the most significant byte (0x00) is at offset 2.
3	1	OCP NIC 3.0 OEM Record Version. This field indicates the card Flex I/O OEM Record Version. Baseboards shall read this field to determine the Flex I/O OEM Record format. OCP NIC 3.0 cards compliant to this version of the specification shall be set to the latest entry noted in this field. Future changes to the OEM Record format will result in an additional record version value added to this list. 0x00 – Reserved. 0x01 – OCP NIC 3.0 card Flex I/O FRU record released with version 1.5.0. 0x02 – OCP NIC 3.0 card Flex I/O FRU record released with version 1.6.0. 0x03 – 0xFF – Reserved.
4	1	Flex I/O mode support. **Note:** If RBT and Timing Sync Modes are supported by the card, the interface shall enable RBT mode by default. The process of switching modes on such cards is outside the scope of this specification. Bit 0 – RBT Mode supported. Bit 1 – Timing Sync Mode supported. Bit [2:6] – Reserved (future use). Set to 0b0_0000. Bit 7 – Not supported. 0xFF – Unknown.
5	1	Timing Sync Mode – Receive Frequency (TS_RX_FREQ). This field defines how the TS_RX_FREQ signal operates. The clock is sent by the OCP NIC and received by the Baseboard. The clock is a +3.3 V single ended signal. By default, this signal on the NIC will be set to unused requiring the system to configure the signal from the available signal configuration options. Bit 0 – 10 MHz with ePPS. Bit 1 – 10 MHz only.

Offset	Length	Description
		Bit [2:6] – Reserved (future use). Set to 0b0_0000. Bit 7 – Single-ended clock mode not supported. 0xFF – Unknown.
6	1	Timing Sync Mode – Receive Sync Pulse (TS_RX_SYNC). This field defines how the TS_RX_SYNC signal can operate. This clock is sent by the OCP NIC and received by the Baseboard. By default, this signal on the NIC will be set to unused requiring the system to configure the signal from the available signal configuration options. Bit 0 – 1 pulse per second (1PPS). Bit 1 – 10 MHz. Bit [2:6] – Reserved (future use). Set to 0b0_0000. Bit 7 – Not supported. 0xFF – Unknown.
7	1	Timing Sync Mode – Transmit Frequency (TS_TX_FREQ). This field defines how the TS_TX_FREQ signal operates. The clock is sent by the OCP baseboard and received by the NIC. The clock is a +3.3 V single ended signal. By default, this signal on the NIC will be set to unused requiring the system to configure the signal from the available signal configuration options. Bit 0 – 10 MHz with ePPS. Bit 1 – 10 MHz only. Bit [2:6] – Reserved (future use). Set to 0b0_0000. Bit 7 – Single-ended clock mode not supported. 0xFF – Unknown.
8	1	Timing Sync Mode – Transmit Sync Pulse (TS_TX_SYNC). This field defines how the TSTX_SYNC signal can operate. This clock is sent by the Baseboard and received by the OCP NIC. By default, this signal on the NIC will be set to unused requiring the system to configure the signal from the available signal configuration options. Bit 0 – 1 pulse per second (1PPS). Bit 1 – 10 MHz. Bit [2:6] – Reserved (future use). Set to 0b0_0000. Bit 7 – Not supported. 0xFF – Unknown.
9	1	Timing Sync Mode – Timing Sync GPI. This field defines the pin function of the TS_GPI signal when asserted by the OCP NIC. The baseboard shall read this value to provision for the supported function(s). By default, the GPI on the NIC will be set to unused and requires the system to configure the NIC side function through the NIC driver/firmware configuration. Bit 0 – NIC side loss-of-signal (LOS). Bit 1 – NIC side loss of lock (LOL). Bits [2:6] – Reserved for future use. Set to 0b0_0000. Bit 7 – Not supported. 0xFF – Unknown.
10	1	Timing Sync Mode – Timing Sync GPO.

Offset	Length	Description
		This field defines the pin function of the TS_GPO signal when received by the OCP NIC. **Note:** TS_GPO is not supported in this release of the specification. This field is Reserved for future use. Set this field to 0xFF. 0xFF – Reserved for future use.
11	2	TS_TX_FREQ Propagation Delay. This field indicates the nominal propagation delay of the TS_TX_FREQ pin on the OCP NIC. This is characterized from the gold finger to the local receiver (e.g. DPLL) and includes any components in the clock path. This value is rounded to the nearest integer and encoded as a hexadecimal value. The units are in picoseconds. 0x0000 – 0xFFFD – Nominal propagation delay on the card. 0xFFFE – Not defined. 0xFFFF – Unknown.
13	2	TS_RX_FREQ Propagation Delay. This field indicates the nominal propagation delay of the TS_RX_FREQ pin on the OCP NIC. This is characterized from the local transmitter (e.g. DPLL) to the card gold finger and includes any components in the clock path. This value is rounded to the nearest integer and encoded as a hexadecimal value. The units are in picoseconds. 0x0000 – 0xFFFD – Nominal propagation delay on the card. 0xFFFE – Not defined. 0xFFFF – Unknown.
15	2	TS_TX_SYNC Propagation Delay. This field indicates the nominal propagation delay of the TS_TX_SYNC pin on the OCP NIC. This is characterized from the gold finger to the local receiver (e.g. DPLL) and includes any components in the clock path. This value is rounded to the nearest integer and encoded as a hexadecimal value. The units are in picoseconds. 0x0000 – 0xFFFD – Nominal propagation delay on the card. 0xFFFE – Not defined. 0xFFFF – Unknown.
17	2	TS_RX_SYNC Propagation Delay. This field indicates the nominal propagation delay of the TS_RX_SYNC pin on the OCP NIC. This is characterized from the local transmitter (e.g. DPLL) to the card gold finger and includes any components in the clock path. This value is rounded to the nearest integer and encoded as a hexadecimal value. The units are in picoseconds. 0x0000 – 0xFFFD – Nominal propagation delay on the card. 0xFFFE – Not defined. 0xFFFF – Unknown.
19	2	Front Panel External Timing Interface 1 Propagation Delay. If present, this field indicates the nominal propagation delay for OCP NIC front panel external timing interface 1. The left most external timing interface (when looking directly at the OCP NIC front panel) starts with “1” and sequentially increases by 1 to *n*, where *n* is the number of front panel external timing interfaces.

Offset	Length	Description
		This is characterized from the local ASIC (e.g. DPLL) to the front panel interface connector. This value is rounded to the nearest integer and encoded as a hexadecimal value. The units are in picoseconds. 0x0000 – 0xFFFD – Nominal propagation delay for Ext. Timing Interface 1. 0xFFFE – Not defined. 0xFFFF – Unknown.
…	…	…
21 + (2*n)	2*n	Additional Front Panel External Timing Interface n Propagation Delay fields may be added to describe the remaining front panel timing interfaces. Refer to 0xC4 Offset 19 for details.

5.10.4 FRU Template

A FRU template is provided online as a baseline implementation example. This FRU template contains the IPMI Platform Management FRU Information Storage Definition Product Info, Board Info records as well as the OEM record for OCP NIC 3.0.

The FRU template file may be downloaded from the OCP NIC 3.0 Wiki site: https://www.opencompute.org/wiki/Server/NIC.

6 Routing Guidelines and Signal Integrity Considerations

6.1 NC-SI over RBT

The NC-SI over RBT requirements in this section apply to all OCP NIC 3.0 card form-factors. Designers shall use the appropriate timing parameters for the design calculations of an SFF/DSFF or LFF card.

The overall end-to-end timing budget is computed by the formula below. The values of each parameter are shown in Table 72 and in DSP0222. The overall BMC pad to ASIC pad timing budget is 3 ns assuming the values shown. This value is inclusive of the RBT isolation buffer on the baseboard, propagation delay through the OCP connector, clock jitter or any clock buffers that may be implemented on the OCP NIC 3.0 card. The addition of these components subtracts from the total available budget.

Total timing budget $= T_{CLK} - T_{CO(max)} - T_{SU(min)} - T_{SKEW(max)}$
$= 20\text{ ns} - 12.5\text{ ns} - 3\text{ ns} - 1.5\text{ ns}$
$= 3\text{ ns}$

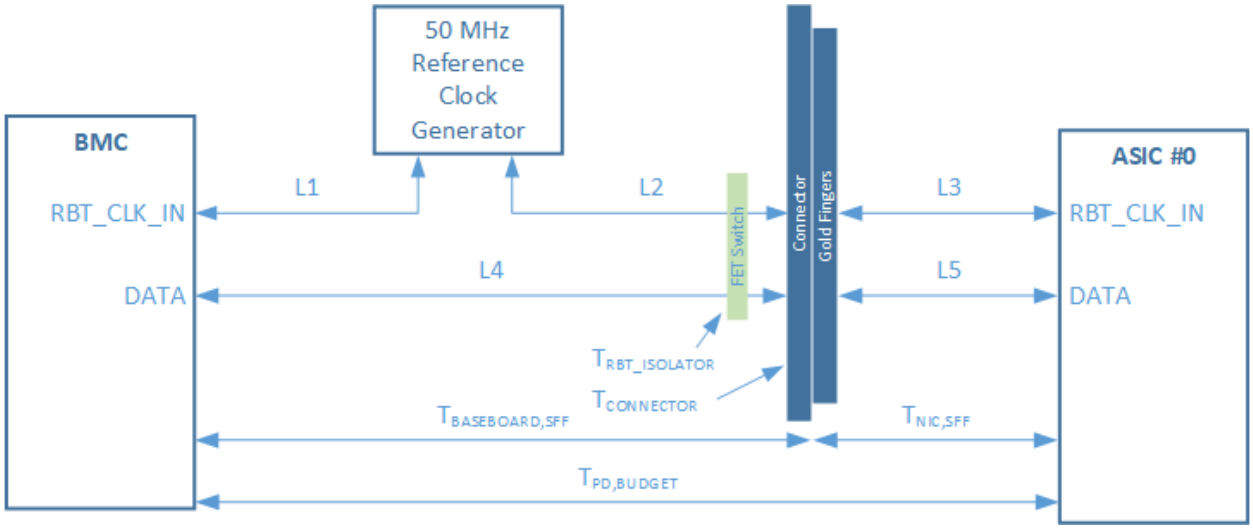
Note: The end-to-end RBT timing budget may be improved by minimizing $T_{SKEW(actual)}$. The formula above assumes the maximum permissible skew per the DSP0222 specification.

Table 72: NC-SI over RBT Timing Parameters

Parameter	Value	Description
$T_{PD,BUDGET}$	3000 ps	Total propagation delay budget between BMC and the target ASIC.
$T_{BASEBOARD,SFF}$	2100 ps	Max permissible propagation delay on an SFF/DSFF baseboard.
$T_{BASEBOARD,LFF}$	1650 ps	Max permissible propagation delay on an LFF baseboard.
$T_{NIC,SFF(MIN)}$	350 ps	Min permissible propagation delay for an SFF/DSFF OCP NIC 3.0 card.
$T_{NIC,SFF(MAX)}$	900 ps	Max permissible propagation delay for an SFF/DSFF OCP NIC 3.0 card.
$T_{NIC,LFF(MIN)}$	350 ps	Min permissible propagation delay for an LFF OCP NIC 3.0 card.
$T_{NIC,LFF(MAX)}$	1350 ps	Max permissible propagation delay for an LFF OCP NIC 3.0 card.
T_{CLK}	20 ns	50 MHz RBT_CLK_IN frequency period.
$T_{CO(max)}$	12.5 ns	Clock-to-out value per DSP0222
$T_{SU(min)}$	3 ns	RBT single ended signal data setup (RBT_TXD[0:1], RBT_TX_EN, RBT_RXD[0:1], RBT_CRS_DV, and RBT_ARB_IN) to RBT_CLK_IN rising edge.
$T_{hd(min)}$	1 ns	RBT single ended signal data hold (RBT_TXD[0:1], RBT_TX_EN, RBT_RXD[0:1], RBT_CRS_DV, and RBT_ARB_OUT) to RBT_CLK_IN rising edge.
$T_{SKEW(max)}$	1.5 ns	Max permissible clock RBT_CLK_IN skew between any two devices in the system – BMC and target NIC ASIC(s).
$T_{RBT_ISOLATOR(max)}$	-	Baseboard RBT isolator propagation delay. Value is dependent on device selection. Baseboard implementers shall include this value in the timing budget calculations.

Parameter	Value	Description
$T_{CONNECTOR,STRADDLE}$	110 ps	OCP NIC 3.0 straddle mount connector propagation delay. This value is the assumed worst case value for all straddle mount connector configurations.
$T_{CONNECTOR,RA}$	130 ps	OCP NIC 3.0 right angle connector propagation delay. This value is the assumed worst case value for all right angle connector configurations.
$T_{CLK_BUF(max)}$	-	OCP NIC 3.0 clock buffer propagation delay. Value is dependent on device selection. OCP NIC 3.0 implementers shall include this value in the timing budget calculations.
T_{JITTER_REF}	-	Baseboard reference clock generator cycle-to-cycle clock jitter. Value is dependent on device selection. Baseboard implementers shall include this value in the timing budget calculations.
T_{JITTER_NIC}	-	OCP NIC 3.0 clock buffer cycle-to-cycle clock jitter (if implemented on the NIC). Value is dependent on device selection. OCP NIC 3.0 implementers shall include this value in the timing budget calculations.

Figure 139: NC-SI over RBT Timing Budget Topology



Note: This is a representative system topology. System implementors shall ensure all propagation delays (such as implementation specific connectors) are accounted for between the 50 MHz reference clock and the target ASICs, as well as propagation delays between data paths.

The following sections define the portion of the overall propagation delay budget allocated to the baseboard and to the OCP NIC 3.0 card, as well as additional requirements for each. Baseboard and NIC implementers shall analyze their design to ensure the timing budget is not violated.

The traces shall be implemented as 50 Ω ±15% impedance-controlled nets. Baseboard and NIC designers are encouraged to follow the guidelines defined in the RMII and NC-SI specifications for physical routing. Refer to Section 4.5.4 and the DSP0222 specification for example interconnect topologies.

6.1.1 SFF/DSFF Baseboard Requirements

The SFF/DSFF baseboard is allocated a maximum propagation time of 2100 ps between the BMC and the connector edge. NC-SI over RBT isolation buffers are required on the baseboard. The requirements for additional add-in card loading are reduced. The available timing budget for the SFF baseboard is computed by the formula below.

$$T_{BASEBOARD,SFF} = 2100\ ps - T_{RBT_ISOLATOR} - T_{CONNECTOR}$$

The skew requirement defines the max permissible clock skew (T_{SKEW}) between the 50 MHz clock generator and any two system devices. The T_{SKEW} calculation is computed by the formula below. This applies to both the devices on the baseboard and the NIC.

- L1 is the RBT_CLK_IN segment from the baseboard 50 MHz reference clock generator to the BMC.
- L2 is the RBT_CLK_IN segment between the baseboard clock generator to the OCP NIC 3.0 connector. L2 includes the propagation delay through the RBT isolation logic.
- L3 is the segment between the SFF OCP NIC 3.0 card gold fingers and the target ASIC.

Refer to Figure 139 for details. The max permissible value of L3 is $T_{NIC,SFF}$ = 900 ps as discussed in Section 6.1.2. Baseboard vendors shall take this value into consideration when analyzing the available timing budget.

$$T_{SKEW(max)} \geq | L1 - (L2 + T_{CONNECTOR} + L3) |$$

Note 1: The end-to-end RBT timing budget may be improved by minimizing $T_{SKEW(actual)}$. The largest gains may be accomplished by closely matching the RBT budget on the baseboard side while accounting for the permissible NIC side minimum/maximum lengths.

Note 2: The timing budget also applies to the RBT hardware arbitration signals RBT_ARB_IN and RBT_ARB_OUT. Both signals are synchronous to RBT_CLK_IN. For NIC implementations that do not support hardware arbitration, the NIC side connection has a loopback between ARB_IN and ARB_OUT. Baseboard vendors shall ensure all the timing requirements are met regardless of if the NIC supports hardware arbitration. The use of signal conditioning logic may be required to ensure the hardware arbitration signals meet the setup and hold time requirements shown in Table 72.

6.1.2 SFF/DSFF OCP NIC 3.0 Card Requirements

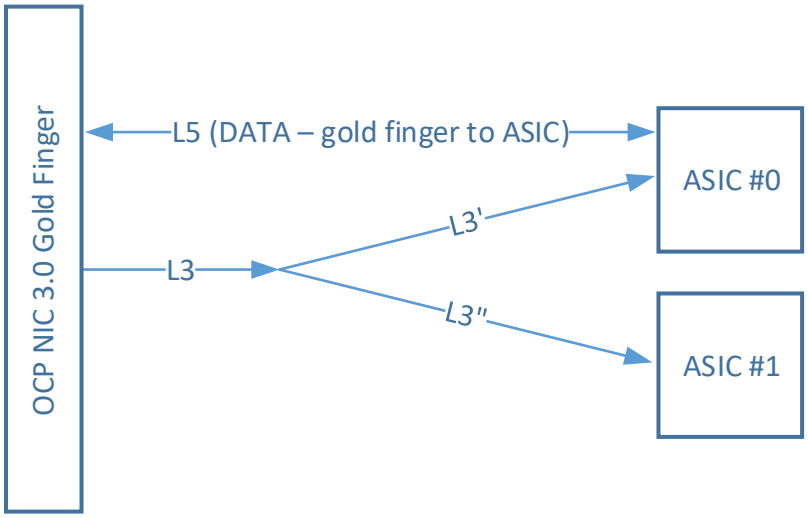
The SFF/DSFF OCP NIC 3.0 card is allocated a maximum propagation time of $T_{NIC,SFF}$ = 900 ps between the card gold finger and the ASIC pad for both the clock and data signals. The total card propagation delay from the RBT clock input towards the card to the RBT outputs from the card shall be less than 14.3 ns ($T_{CO(max)}$ + 2 x $T_{NIC,SFF}$) when measured at the corresponding SFF OCP NIC 3.0 gold fingers. This can be achieved by using an ASIC with the worst case Clock-to-Out ($T_{CO,MAX}$) value of 12.5 ns specified by DSP0222, and each SFF OCP NIC 3.0 card-side RBT signal not exceeding a max propagation time of 900 ps.

This propagation delay is equivalent to a max length of 5.1 inches assuming standard FR4 material with a propagation delay of 175 ps/in. Additional trace length may be achieved with the use of a higher propagation velocity material (e.g., material with a lower dielectric constant) on the baseboard and OCP NIC 3.0 card or simultaneously using both BMC and ASIC devices with an improved timing from Clock-to-Out ($T_{CO,MAX}$) value compared to the published value of 12.5 ns in DSP0222. For NIC implementations

with clock buffers, the propagation delay of the buffer needs to be included in this timing budget (i.e., L3 + T_{CLK_BUF} + L3' + $T_{CO,MAX}$ + L5 shall be less than 14.3 ns) as shown in Figure 141.

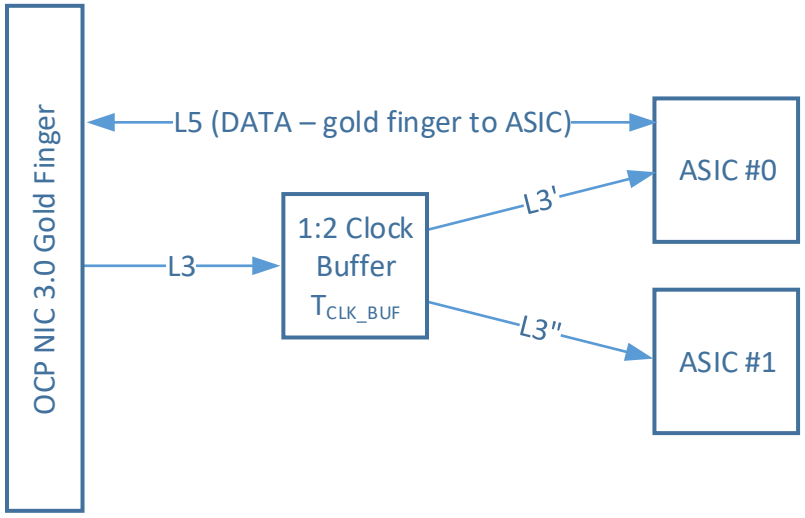
If multiple ASICs are utilized on the same card, the RBT_CLK_IN signal may be routed with a T-topology as shown in Figure 140. The trace length would be calculated as the delay summation of segment L3 + L3' for ASIC #0 and L3 + L3" for ASIC #1. The data path delay to the ASIC is L5.

Figure 140: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – No Clock Buffer



A clock buffer is optionally permitted if the NIC timing budget is not violated. This is shown in Figure 141. In this case, the trace length would be calculated as the delay summation of trace segment L3 + T_{CLK_BUF} + L3' for ASIC #0, and L3 + T_{CLK_BUF} + L3" for ASIC #1.

Figure 141: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – Clock Buffer



For OCP NIC 3.0 cards that do not support hardware arbitration, the RBT_ARB_IN pin shall be directly connected to the RBT_ARB_OUT pin on the NIC.

6.2 SMBus 2.0

For the SMBus 2.0 interface, both the baseboard and OCP NIC 3.0 designers shall follow the applicable requirements found in the SMBus, and PCIe CEM specifications. This applies to the routing guidelines, SI considerations, bus operational speed range, capacitive loading, and range of pull up resistance values. Doing so allows the baseboard suppliers to design a SMBus interface that is compatible with OCP NIC 3.0 products.

6.3 PCIe

OCP NIC 3.0 card suppliers shall follow the PCIe routing specifications. Refer to the PCIe CEM and PCIe Base specifications for end-to-end channel signal integrity considerations.

6.3.1 Channel Requirements

The OCP NIC 3.0 PCIe channel requirements for PCI Express® Gen 4.0 align with the electrical budget and constraints as detailed in the PCI Express® CEM 4.0 Rev 1.0 and PCI Express Base Specification Rev 4.0. Exceptions or clarifications to the referenced specifications are noted in the sections below.

The OCP NIC 3.0 PCIe channel requirements for PCI Express® Gen 5.0 differ from the PCI Express® CEM 5.1 Rev 1.0 for Insertion Loss Values as the loss was reduced on the OCP NIC 3.0 to provide the baseboard additional margin for SFF and DSFF implementations. The OCP NIC 3.0 LFF aligns with the PCI Express® CEM specification. Refer to Section 6.3.1.2 for details.

The OCP NIC 3.0 PCI Express® Gen 6.0 channel requirements are under investigation.

6.3.1.1 REFCLK requirements

REFCLK requirements are detailed in the PCI Express CEM 5.1 Rev 1.0 Section 2.1.

6.3.1.2 Add-in Card Electrical Budgets

This section defines the OCP NIC 3.0 card side PCIe channel budget. This includes the silicon die, package vias, AC caps and traces. The card side gold finger pad is not included as part of the card side PCIe channel budget and should not be included in the card side budget calculations; it is considered part of the mated host side connector interface. The values listed below are shown for reference and mirrors that of the respective PCIe CEM specifications.

Table 73: PCIe Electrical Budgets

Parameter	PCIe CEM 4.0 Rev 1.0 Specification Section	PCIe CEM 5.1 Rev 1.0 Specification Section	PCIe CEM 6.0 Rev 0.9 Specification Section
AC coupling capacitors	Section 4.7.1	PCIe Base Specification 5.0 Section 8.3.9 Symbol C_{TX}	PCIe Base Specification 6.2 Section 8.3.10 Symbol C_{TX}
Insertion Loss Values (Voltage Transfer Function)	Section 4.7.2 and Appendix A. Section 4.7.10 for 16 GT/s	Section 4.7.2 and Appendix A. -7.0 dB at 16 GHz for SFF and DSFF(See Note 1) Section 4.7.11 for LFF	Section 4.7.2 and Appendix A. -7.0 dB at 16 GHz for SFF and DSFF(See Note 2)
Jitter Values	Section 4.7.3 for 8 GT/s and 16 GT/s. Also refer to the PCIe Base Specification 4.0 Section 8.3.5	Section 4.7.3 for 8 GT/s, 16 GT/s and 32 GT/s. Also refer to the PCIe Base Specification 5.0 Section 8.3.5	Section 4.7.3 Also refer to the PCIe Base Specification 6.2 Section 8.3.5
Crosstalk	Section 4.7.4	Section 4.7.4	Section 4.7.4
Lane-to-lane skew (S_A) for Add-in cards	Section 4.7.5	Section 4.7.5	Section 4.7.5

Parameter	PCIe CEM 4.0 Rev 1.0 Specification Section	PCIe CEM 5.1 Rev 1.0 Specification Section	PCIe CEM 6.0 Rev 0.9 Specification Section
Transmitter Equalization	Section 4.7.6 and PCIe Base Spec Chapter 9	Section 4.7.6 and PCIe Base Spec Chapter 9	Section 4.7.6 and PCIe Base Spec Chapter 9
Skew within a differential pair	Section 4.7.7	Section 4.7.7	Section 4.7.7
Differential data trace impedance	Section 4.7.8	Section 4.7.8	Section 4.7.8
Differential data trace propagation delay	Section 4.7.9	Section 4.7.9	Section 4.7.9

Note 1: The OCP NIC 3.0 SFF/DSFF deviates from the PCIe CEM specification on Insertion Loss Values at PCIe Gen5 speeds (32GT/s).

Note 2: The OCP NIC 3.0 SFF/DSFF deviates from the PCIe CEM specification on Insertion Loss Values at PCIe Gen6 speeds (64GT/s).

6.3.1.3 PCIe Gen 6 Informative Limits

The following are informative limits for PCIe Gen 6 at 64 GT/s. For details refer to CEM 6.0 Section 4.9 for guidelines on Insertion Loss, Return Loss, PSNEXT and PSFEXT for 64 GT/s rates. The OCP NIC 3.0 specification will leverage this section with the following deviations for each Add-in Card as shown in Table 74.

Table 74: PCIe Gen 6 Informative Limits

Parameter	Limits
Insertion Loss	≥ [-1.75 - 0.32815 * f] dB for f ≤ 16 GHz; ≥ [2 - 0.563 * f] dB for 16 GHz < f ≤ 24 GHz
Return Loss	≤ [-13.5 + 0.25 * f] dB for f ≤ 24GHz
PSNEXT[1]	Equation 1: ≤ -60 dB for f ≤ 16 GHz; ≤ [-70 +0.625 * f] dB for 16 GHz < f ≤ 24 GHz Equation 2: $ccICN_{NEXT}$ ≤ 300 µV for $f$max = 24 GHz
PSFEXT[1]	Equation 1: ≤ [-50 + 0.208 * f] dB for f ≤ 24GHz Equation 2: $ccICN_{FEXT}$ ≤ 275 µV for $f$max = 24 GHz

Note 1: Following in-line with the PCIe CEM specification guidelines, the provided frequency-based requirements (Equation 1) and ccICN limit for crosstalk energy in the given frequency bands (Equation 2) is provided for OCP NIC 3.0 cards. Refer to CEM 6.0 on how these equations are used to determine if the OCP NIC card meets the guidelines.

6.3.1.4 Baseboard Channel Budget

The baseboard channel budget directly follows the PCI Express CEM 5.0 Rev 1.0 specification. Details of the budget are outside of the scope of this specification.

6.3.1.5 SFF-TA-1002 Connector Channel Budget

Reference the SFF-TA-1002 Revision 1.1 or later.

6.3.1.6 Differential Impedance (Informative)

For PCIe transmit and receive differential pairs, the target impedance is 85 Ω ±10%.

For the PCIe REFCLKs, the target impedance is 100 Ω ±10%.

6.3.2 Test Fixtures

Test Fixtures are designed using the PCIe CEM CLB and CBB. The fixtures host interface has been modified to the OCP connector standard and there are three versions of the fixtures for both the SFF and LFF OCP NIC 3.0 cards for Gen 3, Gen 4 and Gen 5 PCIe rates. Careful attention has been placed on these fixtures to help ensure that standard test equipment automation should work without significant modification.

PCIe Gen 5 automation scripts may need to be modified as the OCP NIC 3.0 insertion loss budget differs from the PCIe CEM 5.1 32GT/s values.

PCIe Gen 6 automation scripts may need to be modified as the OCP NIC 3.0 insertion loss budget differs from the PCIe CEM 6.0 64GT/s values.

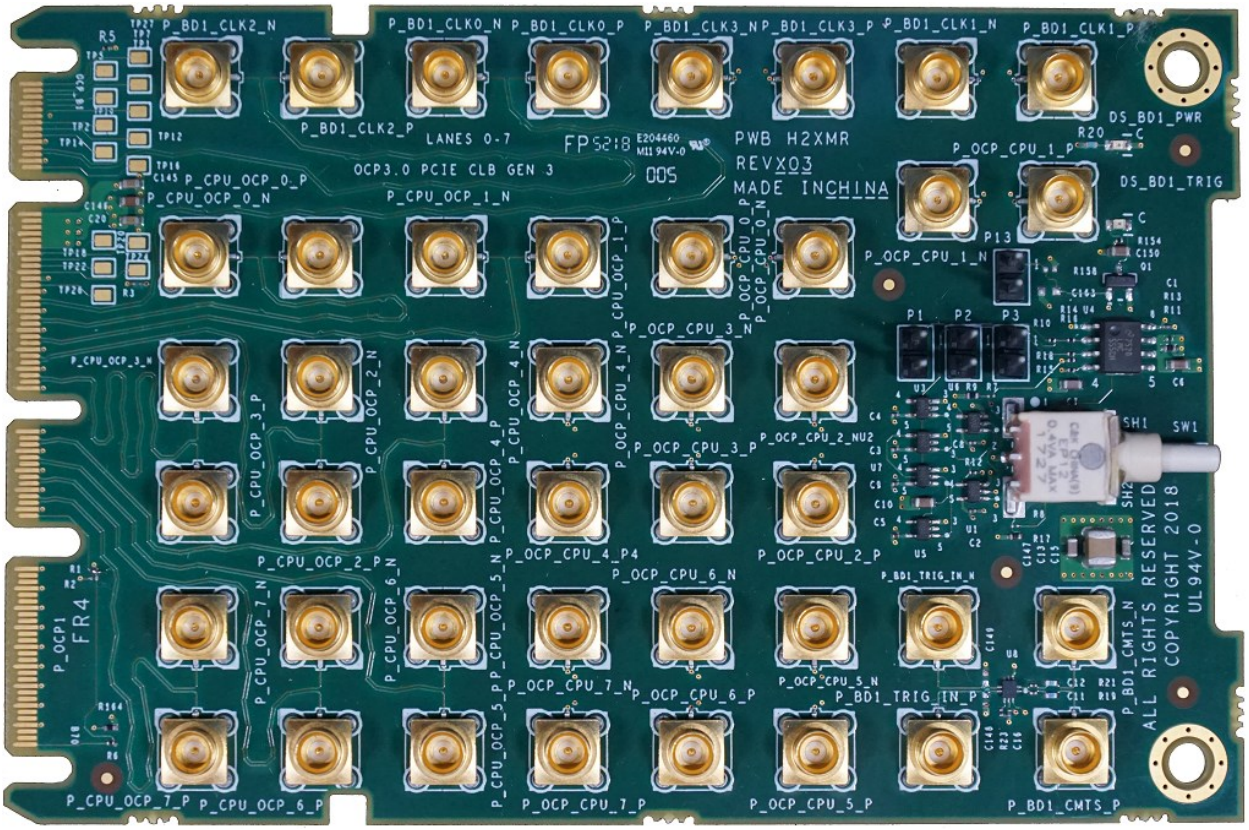
Table 75: PCIe Test Fixtures for OCP NIC 3.0

PCIe Generation	Load Board Test Fixture PCB Material	Base Board Test Fixture PCB Material
Gen 3	TU863	TU863
Gen 4	TU883	TU883 (+vISI board)
Gen 5	R-5775(G)	R-5775(G)
Gen 6	R-5775(G)	R-5775(G)

6.3.2.1 Compliance Load Board (CLB)

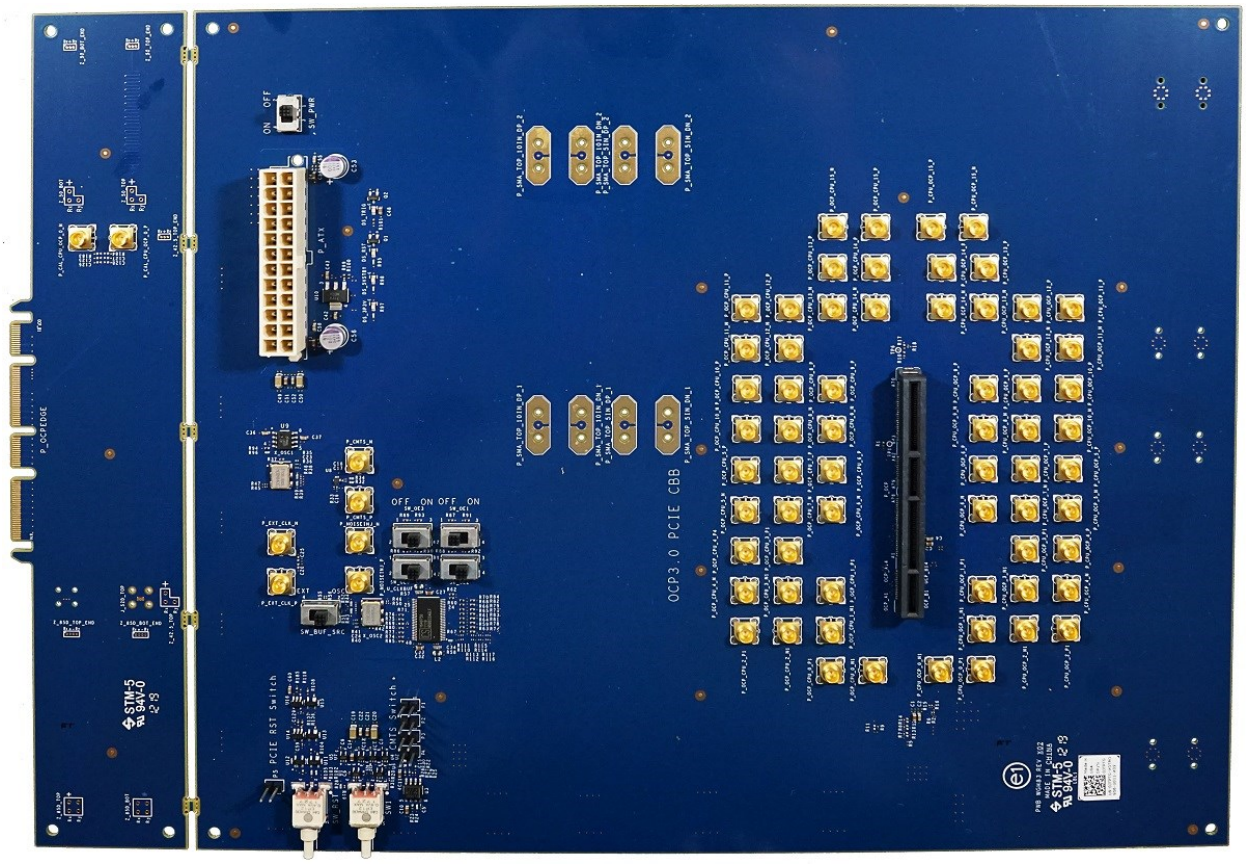
Note: The SFF CLB may be used for testing DSFF slots lanes 0:15 and 16:31. There is no separate DSFF CLB.

Figure 142: PCIe Load Board Test Fixture for OCP NIC 3.0 SFF and DSFF



6.3.2.2 Compliance Baseboard (CBB)

Figure 143: PCIe Base Board Test Fixture for OCP NIC 3.0 SFF



6.3.3 Test Methodology

OCP NIC 3.0 is compliant to the applicable PCIe specifications. The electrical interface may be tested against the PCI Express® Architecture PHY Test Specification Revision 4.0, providing that the appropriate test fixtures from Section 6.3.2 are used.

For PCIe Gen 5.0, OCP NIC 3.0 modifies the insertion loss budget on the SFF as shown in Table 73 and the test methodology may need to be adjusted to compensate for this difference. The electrical interface may be tested against the PCI Express® Architecture PHY Test Specification Revision 5.0, providing that the appropriate test fixtures from Section 6.3.2 are used and the insertion loss difference is compensated.

For PCIe Gen 6.0, the test methodology is currently under investigation.

6.3.3.1 Test Setup

This section is a work-in-progress by the OCP NIC 3.0 SI Subgroup. The following information will be added in a future document release:

- Description of the OCP NIC 3.0 CLB and CBB test figure for use in the PCIe Architecture PHY Test Specifications.

- A user guide is in development through UNH at the time of publication.
- The test procedure is based on the PCIe procedures. The differences between the procedures for PCIe Adapters and OCP NIC 3.0 cards will be documented in the user guide.

7 Thermal and Environmental

7.1 Airflow Direction

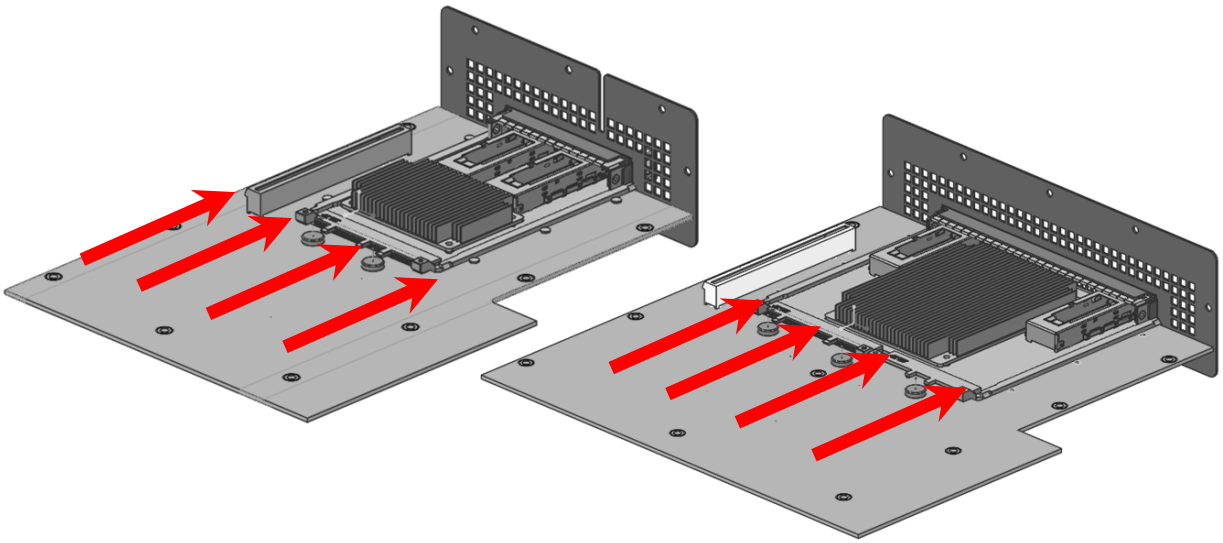
The OCP NIC 3.0 card is designed to operate in either of two different airflow directions which are referred to as Hot Aisle and Cold Aisle. In both Hot Aisle and Cold Aisle configurations all airflow is directed over the topside of the card. Component placement must assume that there will be no airflow on the bottom side of the card. The local approach air temperature and velocity to the card is dependent on the capability of the system adopting OCP NIC 3.0 card. These parameters may be impacted by the operational altitude and relative humidity in Hot Aisle or Cold Aisle configurations. Design boundary conditions for Hot Aisle and Cold Aisle cooling are included below in Sections 7.1.1 and 7.1.2 respectively.

The two airflow directions of the Hot and Cold Aisle cases should not result in multiple thermal solutions to separately satisfy the varying thermal boundary conditions. Ideally, any specific OCP NIC 3.0 card design should function in systems with either Hot Aisle or Cold Aisle cooling. Thermal analysis in support of this specification have shown the Hot Aisle configuration to be more challenging than Cold Aisle but card vendors should make that determination for each card that is developed.

7.1.1 Hot Aisle Cooling

The airflow in typical server systems will approach from the card edge or heatsink side of the card. This airflow direction is referred to as Hot Aisle cooling and is illustrated below in Figure 144. The term Hot Aisle refers to the card being located at the rear of the system where the local inlet airflow is preheated by the upstream system components (e.g., HDD, CPU, DIMM, etc.).

Figure 144: Airflow Direction for Hot Aisle Cooling (Shown for SFF and LFF)



The boundary conditions for Hot Aisle cooling are shown below in Table 76 and Table 77. The low temperature is listed at 5 °C and assumes fresh air could be ducted to the back of the system from the front. More typically the inlet temperature to the OCP NIC 3.0 card will be in the same range as PCIe cards located at the back of the system (55 °C local inlet temperature). Depending on the system design, power density, and airflow the inlet temperature to the OCP NIC 3.0 card may be as high as 60 °C or 65 °C. The airflow velocities listed in Table 77 represent the airflow velocities typical in mainstream

servers. Higher airflow velocities are available within the Hot Aisle cooling tiers listed in Table 81 but card designers must be sure to understand the system level implications of such high card LFM requirements.

Table 76: Hot Aisle Air Temperature Boundary Conditions

	Low	Typical	High	Max
Local Inlet air temperature	5 °C (system inlet)	55 °C	60 °C	65 °C

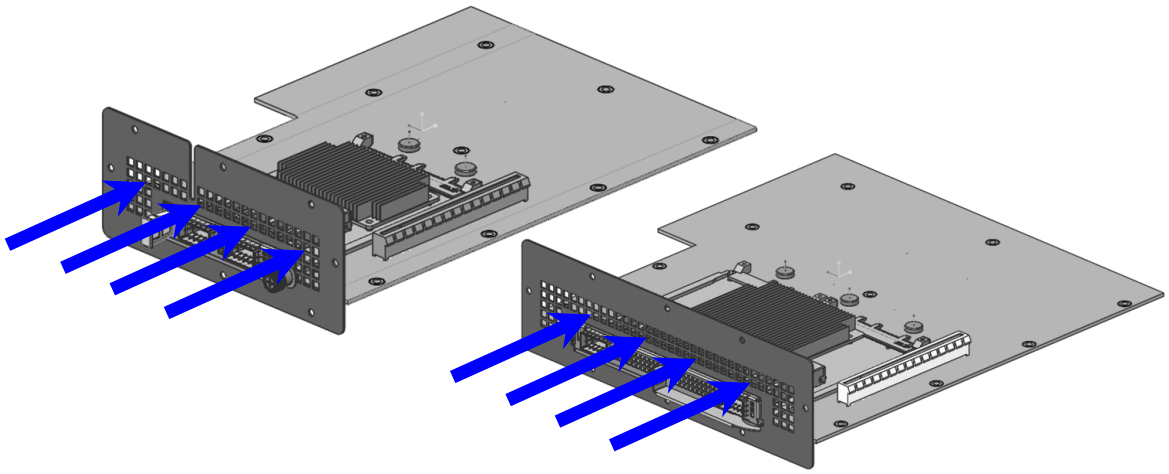
Table 77: Hot Aisle Airflow Boundary Conditions

	Low	Typical	High	Max
Local inlet air velocity	50 LFM	100-200 LFM	300 LFM	System Dependent

7.1.2 Cold Aisle Cooling

When installed in the front of a server the airflow will approach from the I/O connector (e.g., SFP, QSFP or RJ45) side of the card. This airflow direction is referred to as Cold Aisle cooling and is illustrated below in Figure 145. The term Cold Aisle refers to the card being located at the front of the system where the local inlet airflow is assumed to be the same temperature as the system inlet airflow.

Figure 145: Airflow Direction for Cold Aisle Cooling (Shown for SFF and LFF)



The boundary conditions for Cold Aisle cooling are shown below in Table 78 and Table 79. The temperature values listed in Table 78 assume the inlet temperature to the OCP NIC 3.0 card to be the same as the system inlet. The low, typical, high, and max temperatures listed align with the ASHRAE A1, A2, A3, and A4 environmental classes. Depending on the system, the supported ASHRAE class may limit the maximum temperature to the OCP 3.0 NIC card. However, for more broad industry support, cards should be designed to the upper end of the ASHRAE classes (e.g., class A4).

Table 78: Cold Aisle Air Temperature Boundary Conditions

	Low	Typical	High	Max
Local Inlet Air Temperature	5 °C	25-35 °C ASHRAE A1/A2	40 °C ASHRAE A3	45 °C ASHRAE A4

Table 79: Cold Aisle Airflow Boundary Conditions

	Low	Typical	High	Max
Local Inlet Air Velocity	50 LFM	100 LFM	200 LFM	System Dependent

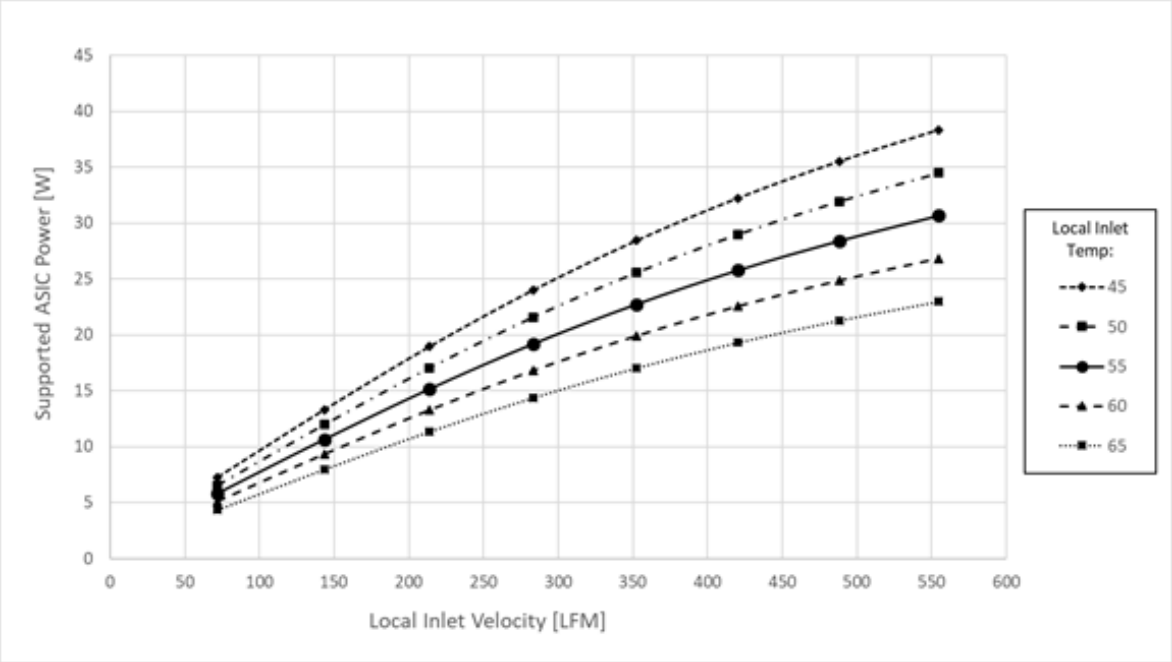
7.2 Thermal Design Guidelines

The information in this section is intended to serve as a quick reference guide for OCP NIC 3.0 designers early in the design process. The information should be used as a reference for upfront thermal design and feasibility and should not replace detailed card thermal design analysis. The actual cooling capability of the card shall be defined based on the testing with the OCP NIC 3.0 thermal test fixture as defined in Section 7.4.

7.2.1 SFF Card ASIC Cooling – Hot Aisle

The ASIC or controller chip is typically the highest power component on the card. Thus, as OCP NIC 3.0 cards are developed it is important to understand the ASIC cooling capability. Figure 146 below provides an estimate of the maximum ASIC power that can be supported as a function of the local inlet velocity for the SFF card in a hot aisle cooling configuration. Each curve in Figure 146 represents a different local inlet air temperature from 45 °C to 65 °C.

Figure 146: ASIC Supportable Power for Hot Aisle Cooling – SFF



The curves shown in Figure 146 were obtained using CFD analysis of a reference OCP NIC 3.0 SFF card. The reference card has a 20 mm x 20 mm ASIC with two QSFP connectors. Figure 147 shows a comparison of the 3D CAD and CFD model geometry for the reference OCP NIC 3.0 card. Additional card geometry parameters and boundary conditions used in the reference CFD analysis are summarized in Table 80. The OCP NIC 3.0 simulation was conducted within a virtual version of the test fixture defined in Section 7.4.

Figure 147: OCP NIC 3.0 SFF Reference Design and CFD Geometry

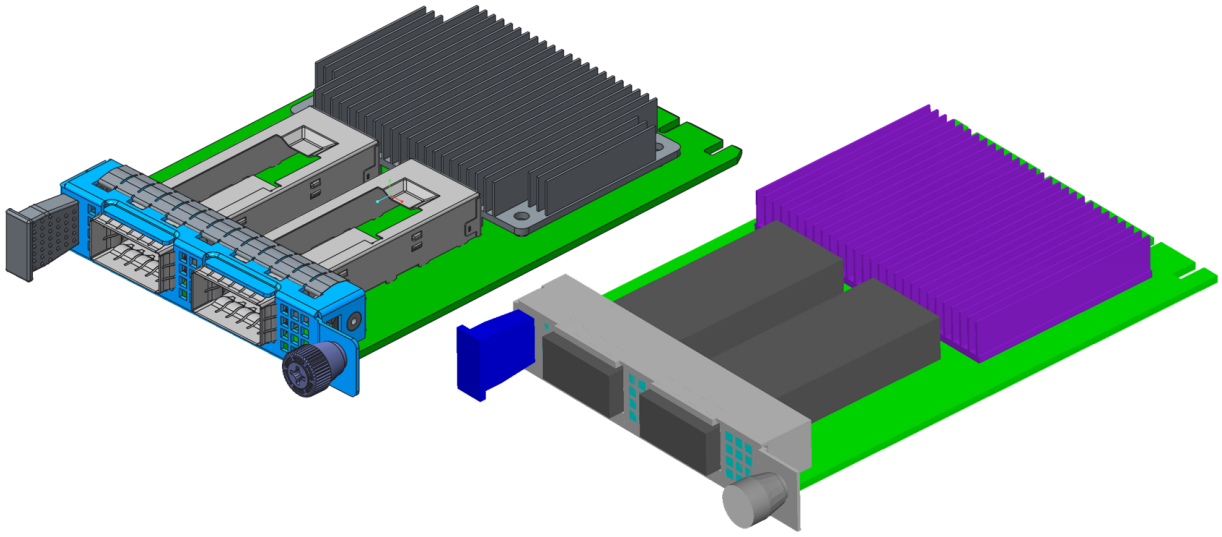


Table 80: Reference OCP NIC 3.0 SFF Card Geometry

OCP NIC 3.0 Form Factor	SFF Card
Heatsink Width	65 mm
Heatsink Length	45 mm
Heatsink Height	9.24 mm
Heatsink Base Thickness	1.5 mm
Fin Count/Thickness	28/0.5 mm
Heatsink Material	Extruded Aluminum
ASIC Width	20
ASIC Length	20
ASIC Height	2.26
ASIC Theta-JC	0.17 C/W
ASIC Theta-JB	10 C/W
OCP PCB In-Plane Conductivity	34 W/mK
OCP PCB Normal Conductivity	0.33 W/mK
ASIC Max T-case	95 °C
OCP NIC 3.0 I/O Connectors	Two QSFP @ 3.5 W each

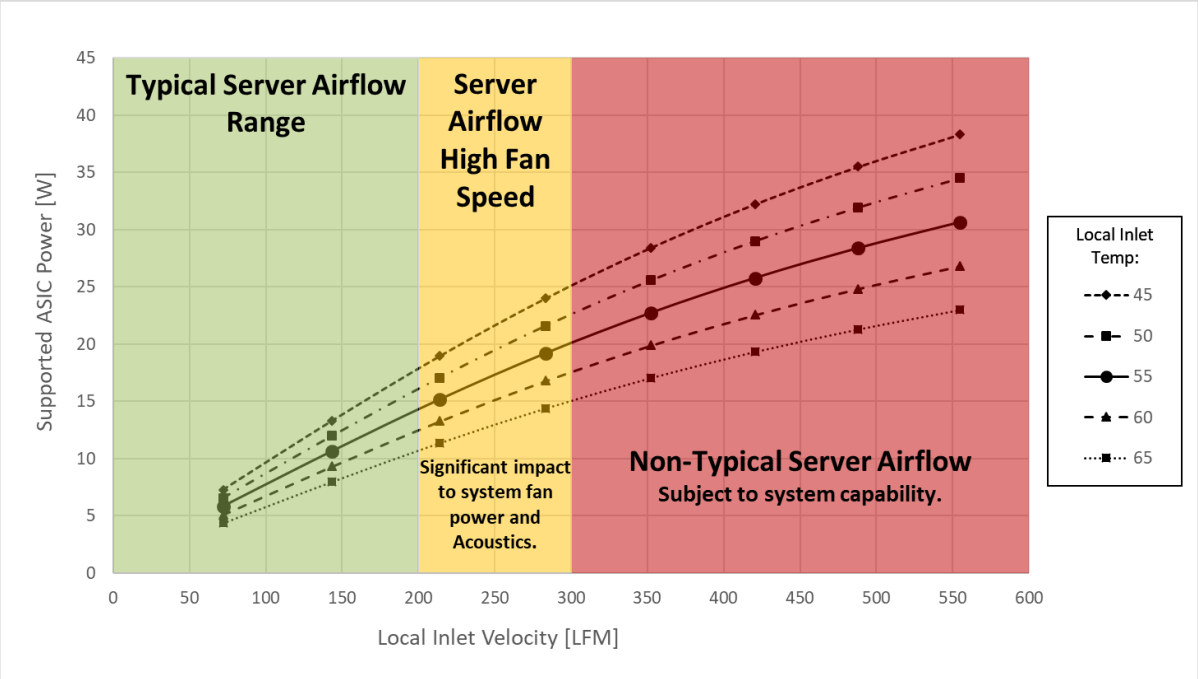
An increase in the supported ASIC power or a decrease in the required airflow velocity may be achieved through heatsink size and material changes. For example, a larger heatsink or a heatsink made from copper could improve ASIC cooling and effectively shift up the supportable power curves shown in Figure 146.

It is important to point out that the curves shown in Figure 146 represent only the maximum ASIC power that can be supported vs. the supplied inlet velocity. Other heat loads on the card may require airflow velocities above and beyond that required to cool the ASIC. SFP or QSFP optical transceivers located downstream of the AISC will in many cases pose a greater cooling challenge than the ASIC cooling.

Cooling the optical transceivers becomes even more difficult as the ASIC power is increased due to additional preheating of the air as it moves through the ASIC heatsink. OCP NIC 3.0 designers must consider all heat sources early in the design process to ensure the card thermal solution is sufficient for the feature set. In addition, OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 5.10.3.

Card designers must also consider the airflow capability of the server systems that the cards are targeted for use within. Figure 148 below shows the SFF ASIC supportable power curves with an overlay of three server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions.

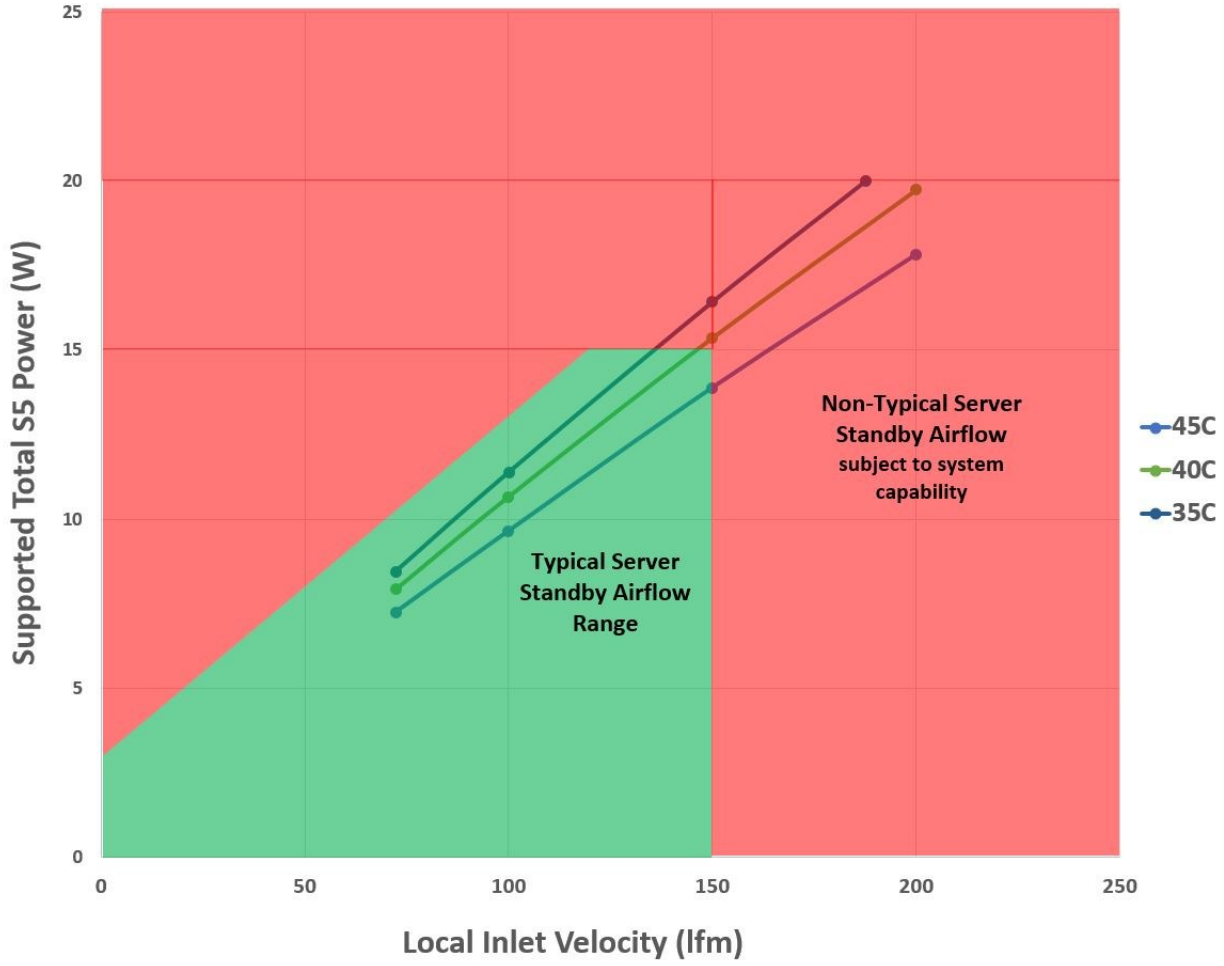
Figure 148: Server System Airflow Capability – SFF Card Hot Aisle Cooling



The server airflow capability is typically more restrictive when the OCP card is operating in Aux Power Mode. The airflow available from the system cooling solution is often more restrictive due to limited power budget available in Aux Power Mode. The graph below emphasizes that though the local OCP NIC 3.0 air temperature is typically lower in Main Power Mode (since preheating from upstream components should be greatly reduced while in standby), the upper bound of local air velocity is a fraction of what can be generated when the system is in Main Power Mode. Card vendors must test for these conditions, making sure that the provided cooling is sufficient for both the ASIC and any installed transceivers (which will still be receiving preheat from the ASIC in Aux Power Mode).

The NIC vendor shall provide the required LFM during for Aux Power Mode in the FRU EEPROM (see Section 4.10.3). The cold aisle should be tested at 35 °C; the hot aisle should be tested at 45 °C.

Figure 149: Server System Airflow Capability – SFF Card Hot Aisle Cooling in Aux Power Mode



7.2.2 TSFF Card ASIC Cooling – Hot Aisle (TBD)

This section is a work in progress.

7.2.3 DSFF Card ASIC Cooling – Hot Aisle (TBD)

This section is a work in progress.

7.2.4 TDSFF Card ASIC Cooling – Hot Aisle (TBD)

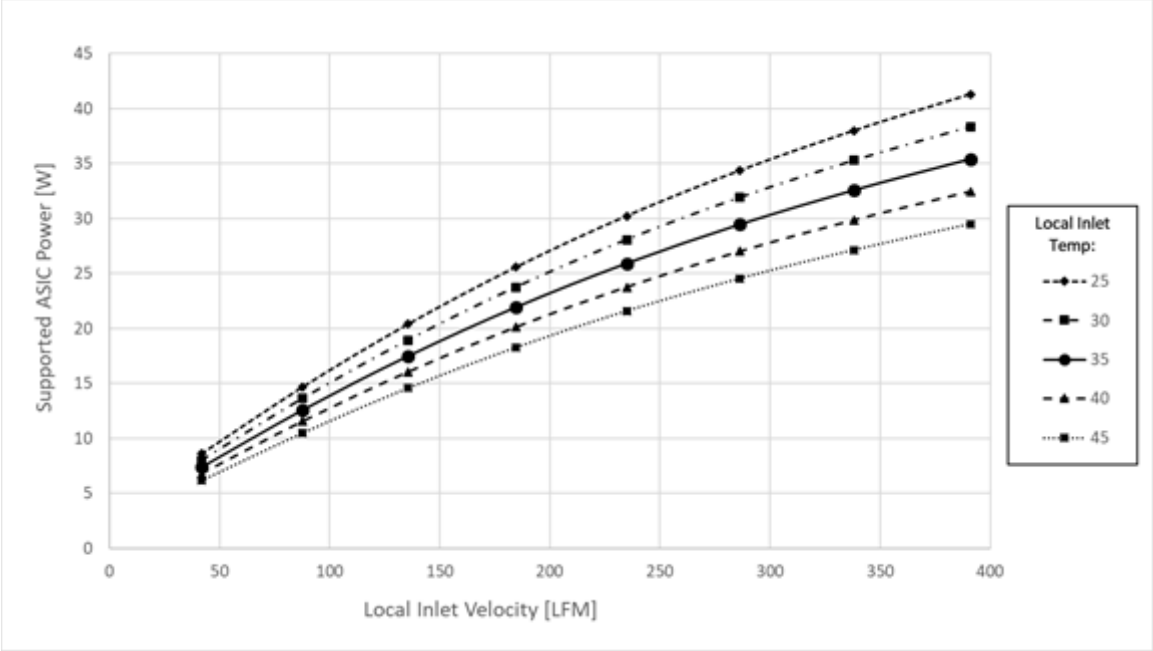
This section is a work in progress.

7.2.5 SFF Card ASIC Cooling – Cold Aisle

Compared to the Hot Aisle cooling configuration, there are several key differences for Cold Aisle ASIC cooling. With Cold Aisle cooling the airflow is pulled from the I/O connector side of the card. The I/O connectors and faceplate venting may affect the airflow through the ASIC heatsink. The I/O connectors may also preheat the airflow by some amount. In a Cold Aisle cooling configuration, other parallel airflow paths may result in less airflow passing over and through the OCP NIC 3.0 card compared to the Hot Aisle.

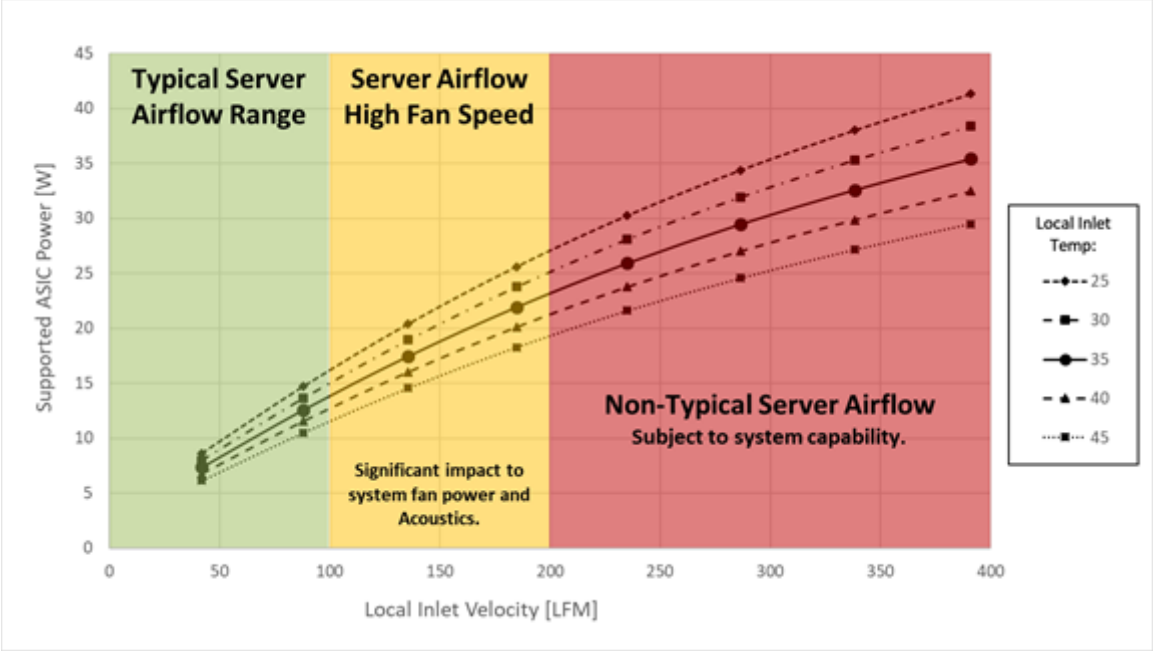
The ASIC cooling analysis for the SFF Card in the Cold Aisle configuration was conducted utilizing the same geometry and boundary conditions described in Figure 147 and Table 80 with airflow moving from I/O connector to ASIC (opposite to the Hot Aisle analysis). Figure 150 below shows the results of this analysis for the Cold Aisle cooling configuration. Each curve in Figure 150 represents a different system inlet air temperature from 25 °C to 45 °C.

Figure 150: ASIC Supportable Power for Cold Aisle Cooling – SFF Card



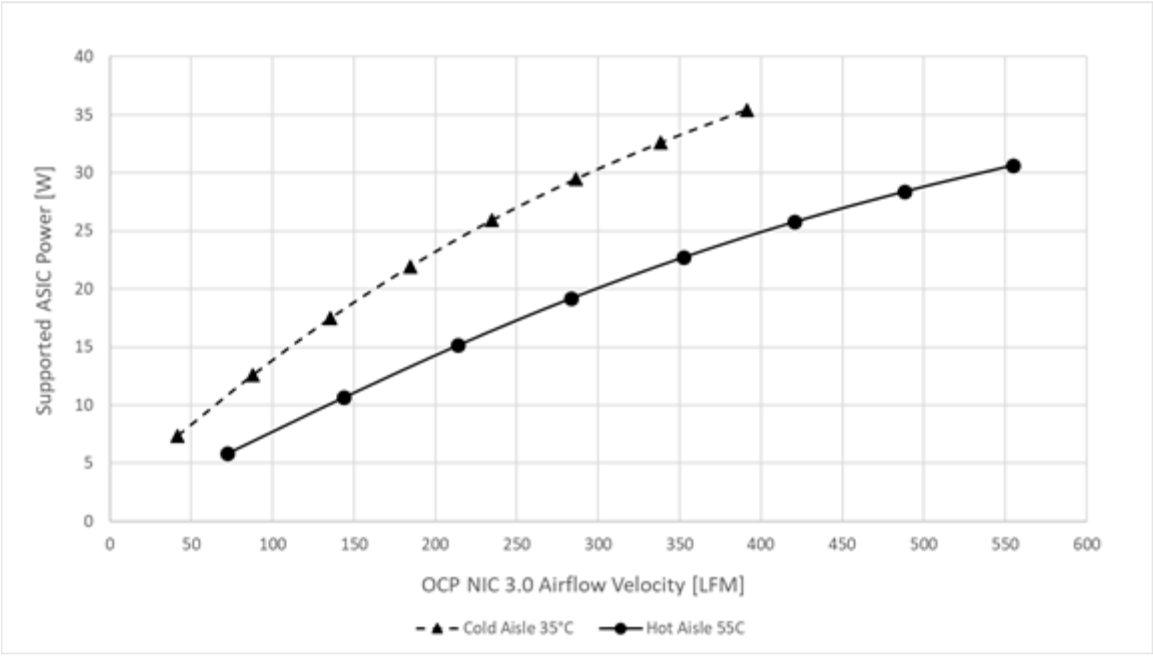
Similar to Figure 148 for Hot Aisle cooling, Figure 151 below shows the ASIC supportable power curves with an overlay of three Cold Aisle server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable Cold Aisle system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Similar to the Hot Aisle cases, cooling of the optical transceivers need to be taken into consideration even though they are not preheated by the ASIC in the Cold Aisle case. OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 5.10.3. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions for both Hot and Cold Aisle cooling.

Figure 151: Server System Airflow Capability – SFF Cold Aisle Cooling



A comparison of Hot Aisle (55 °C) and Cold Aisle (35 °C) SFF ASIC cooling capability curves is shown below in Figure 152. The comparison shows the Hot Aisle ASIC cooling capability at 12 W at 150 LFM while the cold Aisle cooling capability shows support for 19 W at 150 LFM. In general, based on the reference geometry, the Cold Aisle cooling configuration allows for higher supported ASIC power at lower velocities due primarily to the lower inlet temperatures local to the OCP NIC 3.0 card when in the Cold Aisle cooling configuration.

Figure 152: ASIC Supportable Power Comparison – SFF Card



7.2.6 TSFF Card ASIC Cooling – Cold Aisle (TBD)

This section is a work in progress.

7.2.7 DSFF Card ASIC Cooling – Cold Aisle (TBD)

This section is a work in progress.

7.2.8 TDSFF Card ASIC Cooling – Cold Aisle (TBD)

This section is a work in progress.

7.3 Thermal Simulation (CFD) Modeling

CFD models of the SFF, TSFF and LFF cards developed for the analysis detailed in Section 7.2 are available for download on the OCP NIC 3.0 Wiki: https://www.opencompute.org/wiki/Server/NIC

The thermal models available on the wiki site are in Icepak format. CAD step file exports from those models are also available to aid in re-creation of the models in other CFD software tools. Note that the geometry utilized in the CFD models is based on the OCP NIC 3.0 thermal test fixture detailed in Section 7.4.

Thermal simulation of OCP NIC 3.0 cards using the provided CFD models is recommended. Ideally, vendors developing OCP NIC 3.0 cards would perform CFD analysis to validate card thermal solutions using the provided CFD models prior to building card prototypes. Once prototypes are available, vendors would then perform thermal testing on the functional cards using the thermal test fixtures detailed in Section 7.4.

7.4 Thermal Test Fixture

Thermal test fixtures have been developed for SFF, TSFF and LFF OCP NIC 3.0 cards. The test fixtures are intended to provide a common thermal test platform for card vendors, server vendors, and other industry groups planning to develop or utilize the OCP NIC 3.0 card form factors. Details of the thermal test fixtures are as follows:

- Sheet metal side walls, base, faceplate, and top cover
- Thumbscrew top cover access
- PCB sandwiched between base and side walls
- Intended for attachment to wind tunnel or flow bench such as those available at: http://www.fantester.com/
- Allows for thermal testing of functional OCP NIC 3.0 cards in a metered airflow environment
- Input power from external power supplies allows for OCP NIC 3.0 card power measurement
- SFF, TSFF fixture power connections for 3.3 V, GND, and 12 V
- LFF fixture power connections for 3.3 V, GND, and 12 V
- RJ45 connector for NC-SI pass-through
- USB Type-C connector for microprocessor connectivity and Micro-B to the USB pins on the primary connector

- Functions as a remote PCIe extension with intent to position host server under the fixture for connection to system PCIe slot
- Single x16 connection to server host on bottom side of the fixture PCB (SFF, TSFF)
- Dual x16 connection to server host on bottom side of the fixture PCB (LFF)
- Predefined locations for fixture airflow/temperature sensors on fixture PCB silkscreen. Quantity 3x per SFF board – see Figure 155.
- Candlestick style sensors are available at: https://www.qats.com/Products/Instruments/Temperature-and-Velocity-Measurement/Sensors/Candlestick-Sensor
- Candlestick sensors must be procured separately, not integrated with fixture PCB
- Low profile PCIe card serves as blockage above OCP NIC 3.0 card to mimic system geometry and prevent airflow bypass
- LFF fixture uses a sheet metal obstruction built into the top cover

CAD Files for the current revision of the test fixture are available for download on the OCP NIC 3.0 Wiki: https://www.opencompute.org/wiki/Server/NIC.

7.4.1 Test Fixture for SFF Card

Images of the SFF thermal test fixture are shown in Figure 153 and Figure 154. The SFF fixture PCB is shown in Figure 155. Note the three candlestick sensor locations directly next to the OCP NIC 3.0 connectors.

Figure 153: SFF Thermal Test Fixture Preliminary Design

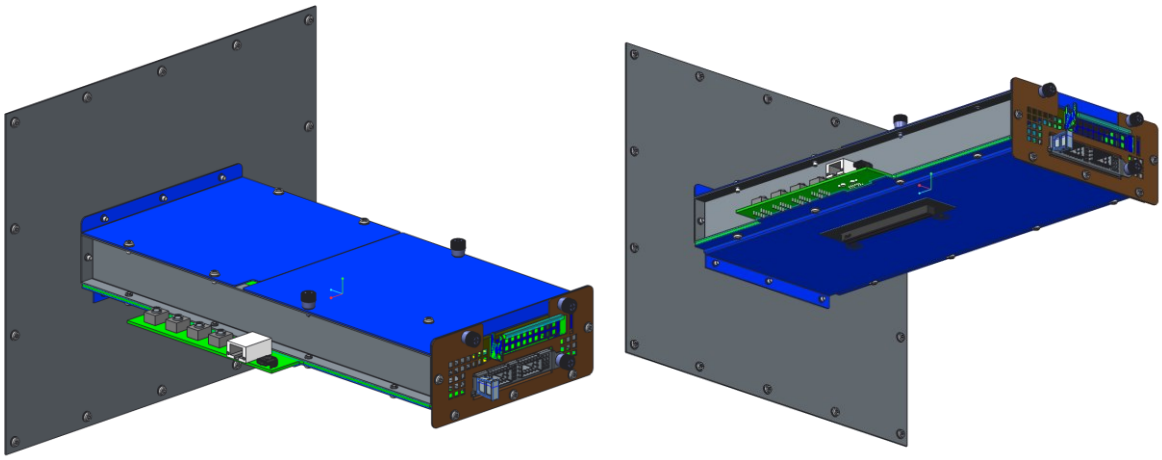


Figure 154: SFF Thermal Test Fixture Preliminary Design – Cover Removed

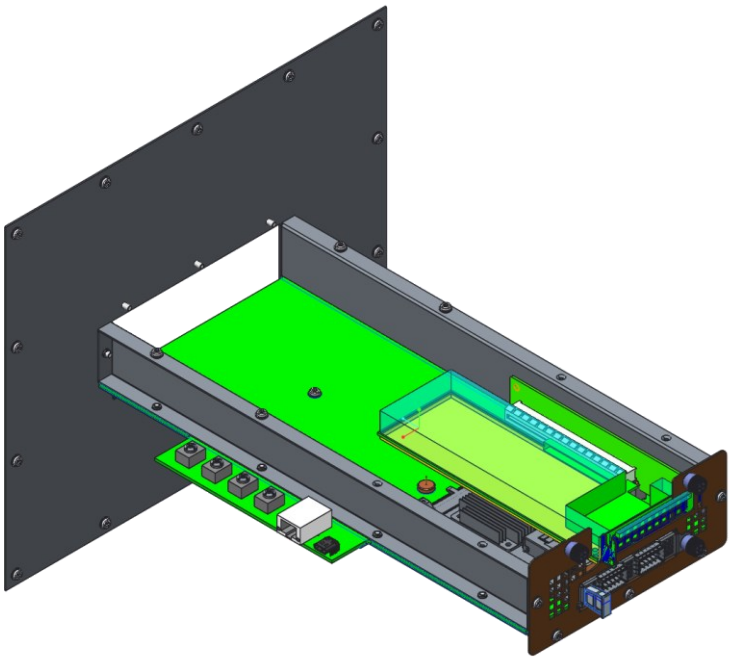
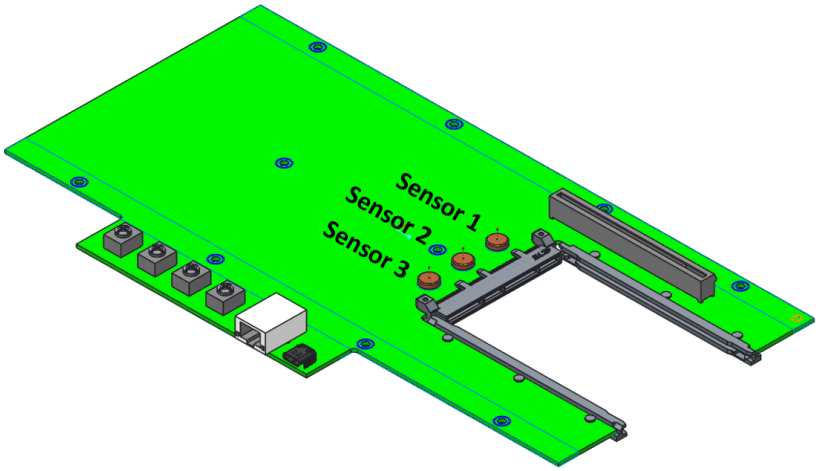


Figure 155: SFF Card Thermal Test Fixture PCB



4466

4467 ### 7.4.2 Test Fixture for TSFF Card (TBD)

4468 This section is a work in progress.

4469 ### 7.4.3 Test Fixture for DSFF Card (TBD)

4470 This section is a work in progress.

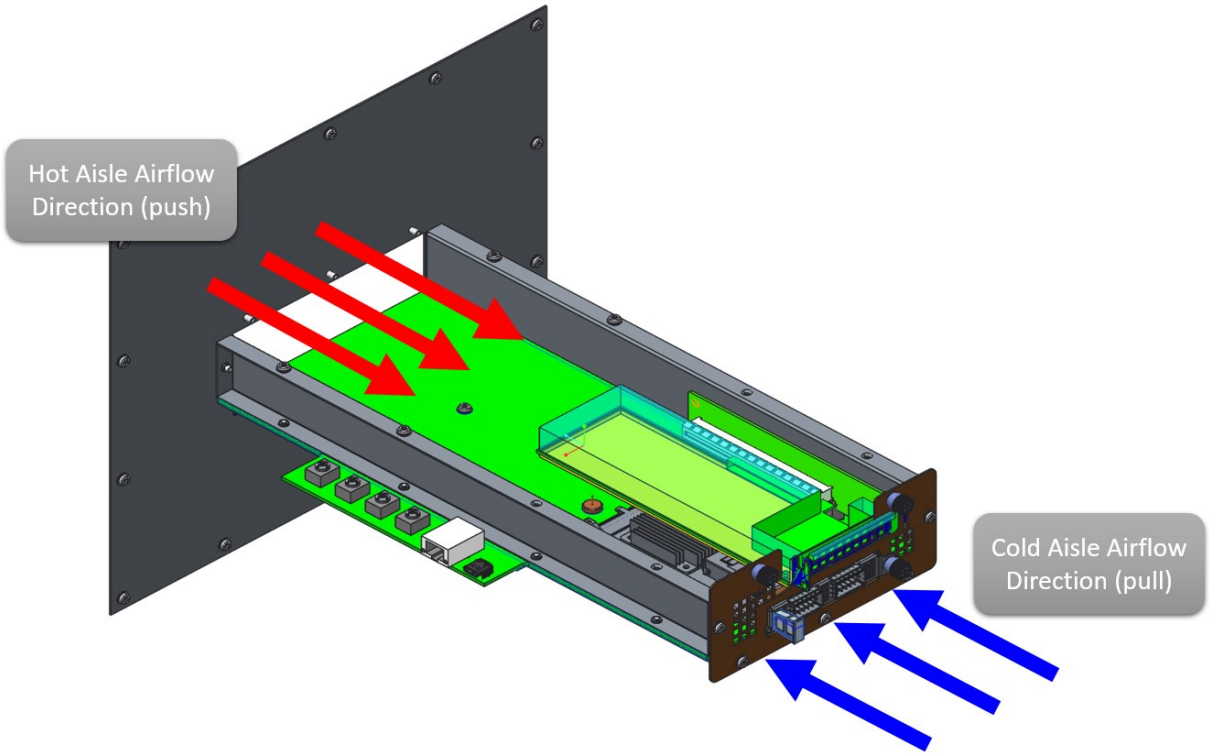
4471 ### 7.4.4 Test Fixture for TDSFF Card (TBD)

4472 This section is a work in progress.
4473
4474
4475
4476

7.4.5 Test Fixture Airflow Direction

When utilizing the OCP NIC 3.0 thermal test fixture, the wind tunnel or flow bench must be configured to push airflow for Hot Aisle cooling or to pull airflow for Cold Aisle cooling as shown in Figure 156.

Figure 156: Thermal Test Fixture Airflow Direction



7.4.6 Thermal Test Fixture Candlestick Sensors

As noted previously, candlestick sensor locations are included on the fixture PCB silkscreen. These candlestick sensors provide point measurements for both airflow velocity (LFM) and air temperature. The airflow at the inlet to the OCP NIC 3.0 will differ from the fixture mean velocity due to the obstructions above the OCP NIC 3.0 cards within the fixture. Thus, the fixture flow rate and cross-sectional area should not be used to determine the local velocity at the OCP NIC 3.0 card. Instead, the candlestick velocity/temperature sensors should be utilized to directly measure the local inlet velocity to the cards for hot aisle cooling.

When measuring the cold aisle inlet temperature, a separate thermocouple in front of the faceplate should be used instead of using the candlestick sensors on-board the thermal test fixture. The thermocouple should be centered on the faceplate area and placed 25 ±2 mm away from the surface. This method is more representative of the cold aisle inlet temperature compared to using the on-board thermal-test fixture candlestick sensors which may be affected by the heat dissipated from the ASIC.

Figure 157: External Thermocouple Placement for Cold Aisle Inlet Temperature Measurement

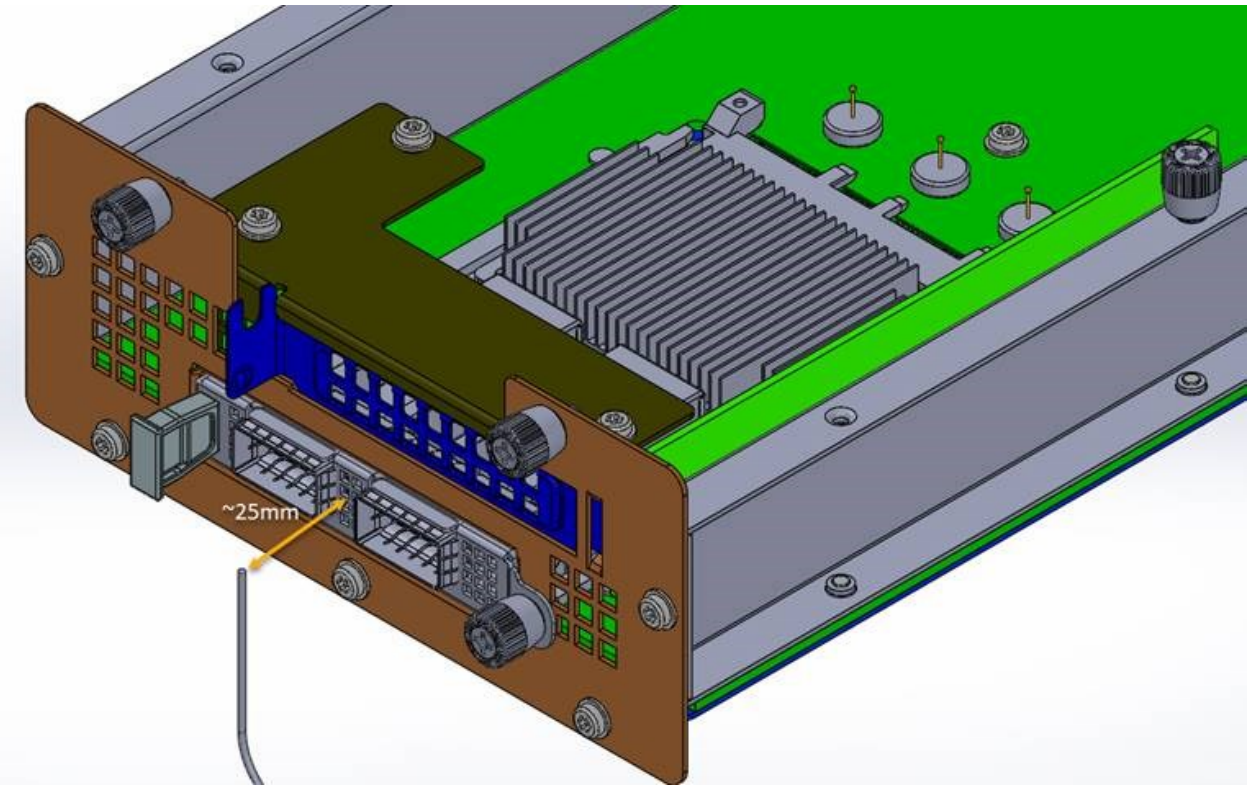


Figure 158, and Figure 159 show the air velocity at each sensor location vs. the total fixture flow rate in CFM. The curves shown in these figures are based on the data collected from the CFD models discussed in Section 7.3. Note the error between the velocities obtained from the sensor locations vs. the velocity based on the duct cross-sectional area.

Figure 158: SFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow

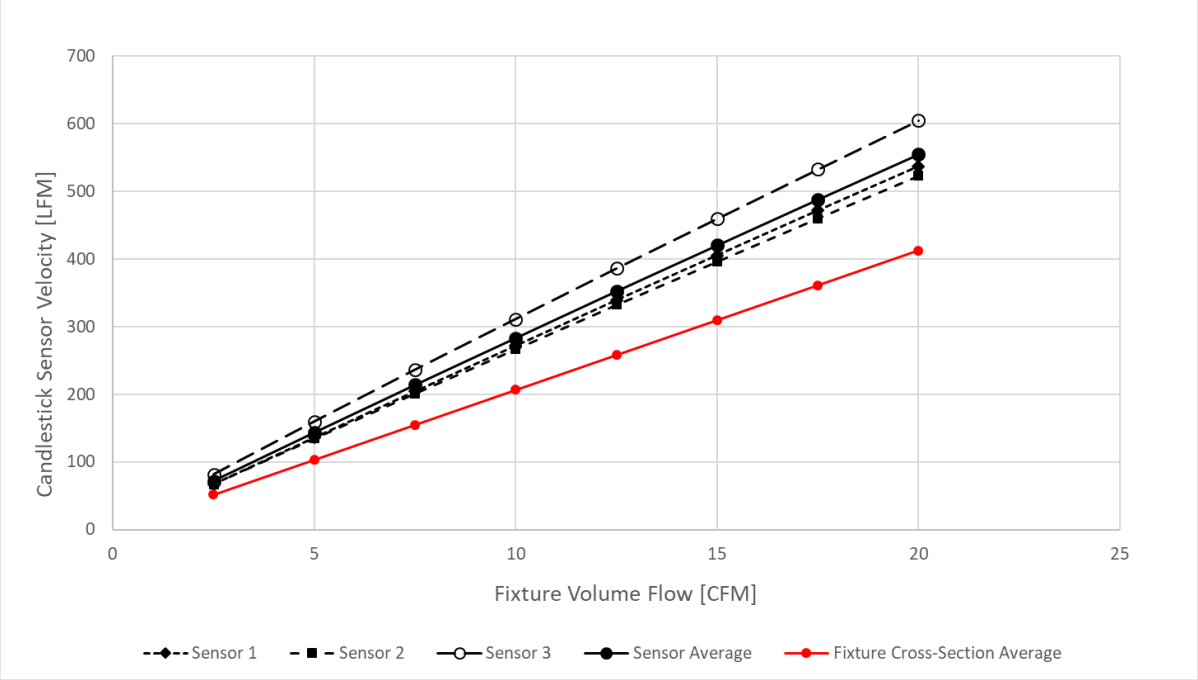


Figure 159: TSFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow (TBD)

This section is a work in progress

7.4.7 Software

The thermal test fixture software is available on the Open Compute Project GitHub repository:
https://github.com/opencomputeproject/OCP-NET-NIC3-TTF-MCU

7.5 Card Sensor Requirements

See Sections 5.3.1 to 5.6 for information relating to temperature sensor and reporting requirements.

7.6 Card Cooling Tiers

Section 5.10.3 defines several FRU fields that may be read by the baseboard management controller (BMC). Two of these fields provide the Hot Aisle and Cold Aisle Card Cooling Tiers that may be used for open loop fan speed control. The Card Cooling Tiers relate the card local inlet temperature to the required local inlet velocity in linear feet per minute (LFM) which allows the system to set fan speeds according to the cooling requirements of the card.

The Card Cooling Tier FRU fields are particularly useful for systems that do not implement temperature sensor monitoring (open loop fan control). The FRU fields may also be used as a backup for systems that implement fan control based on temperature sensor monitoring (closed loop control).

Card Cooling Tiers for Hot and Cold Aisle Cooling configurations are defined in Table 81. The values in the table are listed with units shown in LFM. Future releases of this specification will provide more detail to the Card Cooling Tier curve definition.

Table 81: Card Cooling Tier Definitions (LFM)

	Target Operating Region				Server Airflow High Fan Speed		Non-Typical Server Airflow - Subject to System Capability					
OCP NIC 3.0 Local Inlet Temperature [°C]	Tier 1	Tier 2	Tier 3	Tier 4	Tier 5	Tier 6	Tier 7	Tier 8	Tier 9	Tier 10	Tier 11	Tier 12
5	0	100	100	100	100	100	110	150	200	255	320	395
10	0	100	100	100	100	100	118	159	211	271	341	426
15	0	100	100	100	100	105	128	170	226	291	366	461
20	0	100	100	100	100	109	137	181	241	311	391	496
25	0	100	100	100	100	114	147	198	260	337	420	532
30	0	100	100	100	110	130	167	215	283	363	453	578
35	0	100	100	100	120	146	186	236	308	393	488	623
40	0	100	100	111	139	172	212	260	335	430	525	673
45	0	100	100	125	161	200	242	290	370	472	575	736
50	0	100	110	155	198	243	288	335	425	530	645	838
55	0	100	150	200	250	300	350	400	500	625	750	1000
60	0	150	200	255	315	380	450	525	643	796	936	1241
65	0	200	260	330	410	500	600	710	850	1025	1200	1550

A graphical view of the Card Cooling Tiers is shown in Figure 160. The Tiers range from 0 LFM to as high as 1000 LFM at 55 °C local inlet temperature. It is important to understand that the cooling tiers extend well beyond the airflow range of most server systems. As noted in Section 7.2, card designers must consider the airflow capability of the systems that the cards are to be used in when designing the card thermal solution and component placement. Figure 161 and Figure 162 below show the range of typical system capability for Hot Aisle and Cold Aisle configurations. Cards designed to these typical ranges (Tiers 1-6) will be low risk to support in most if not all server systems. Alternatively, cards that require Tier 7 or greater may still work in many server systems but may require extra validation testing, specific system slot location requirements, and potentially ambient temperature and hardware restrictions.

Figure 160: Graphical View of Card Cooling Tiers

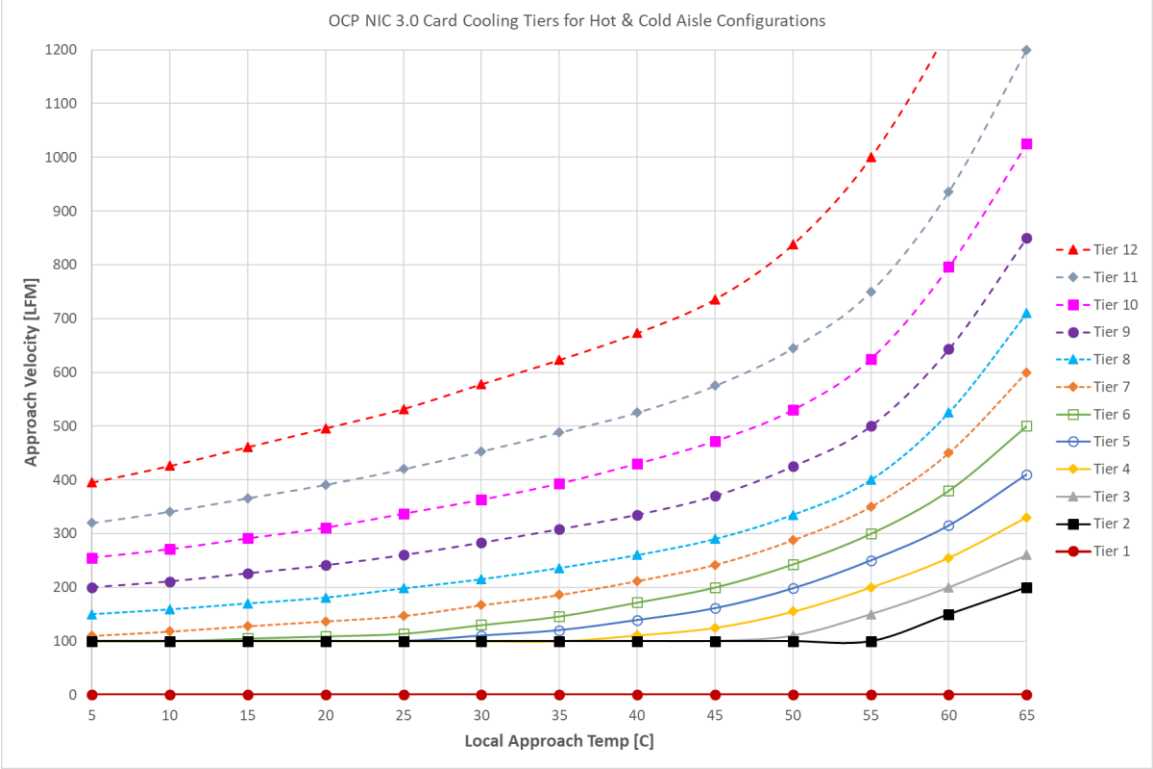


Figure 161: Typical Operating Range for Hot Aisle Configurations

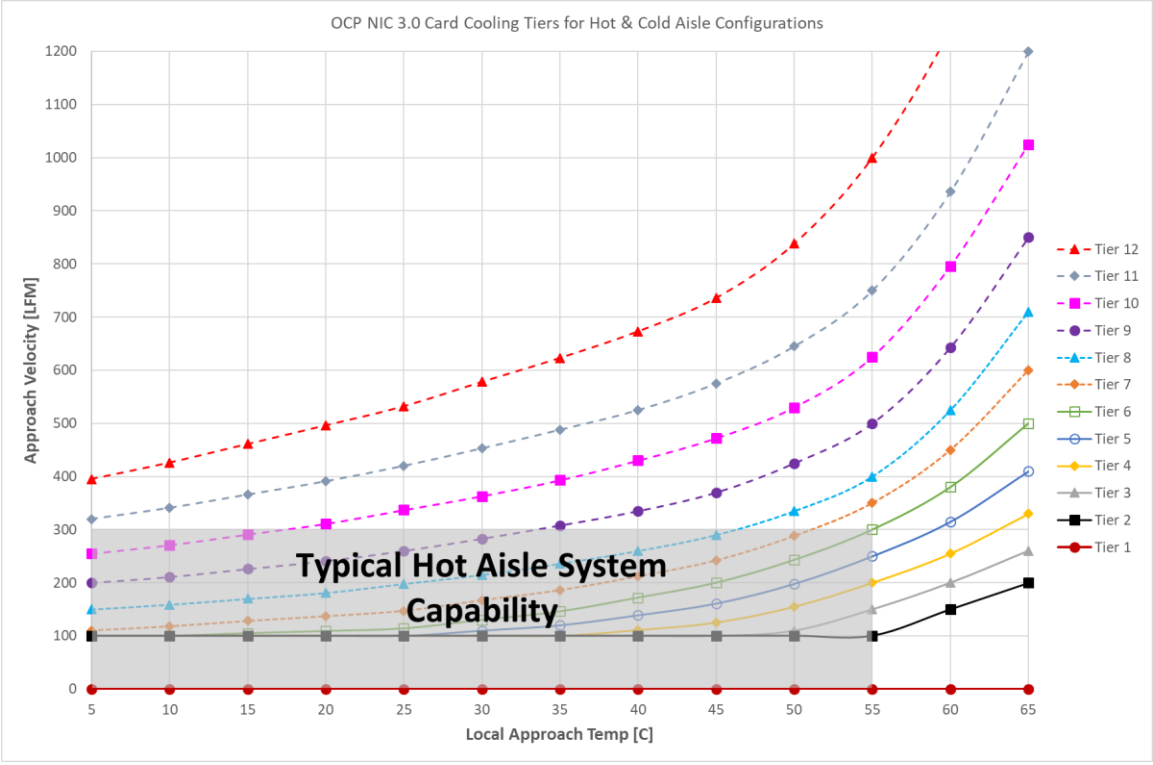
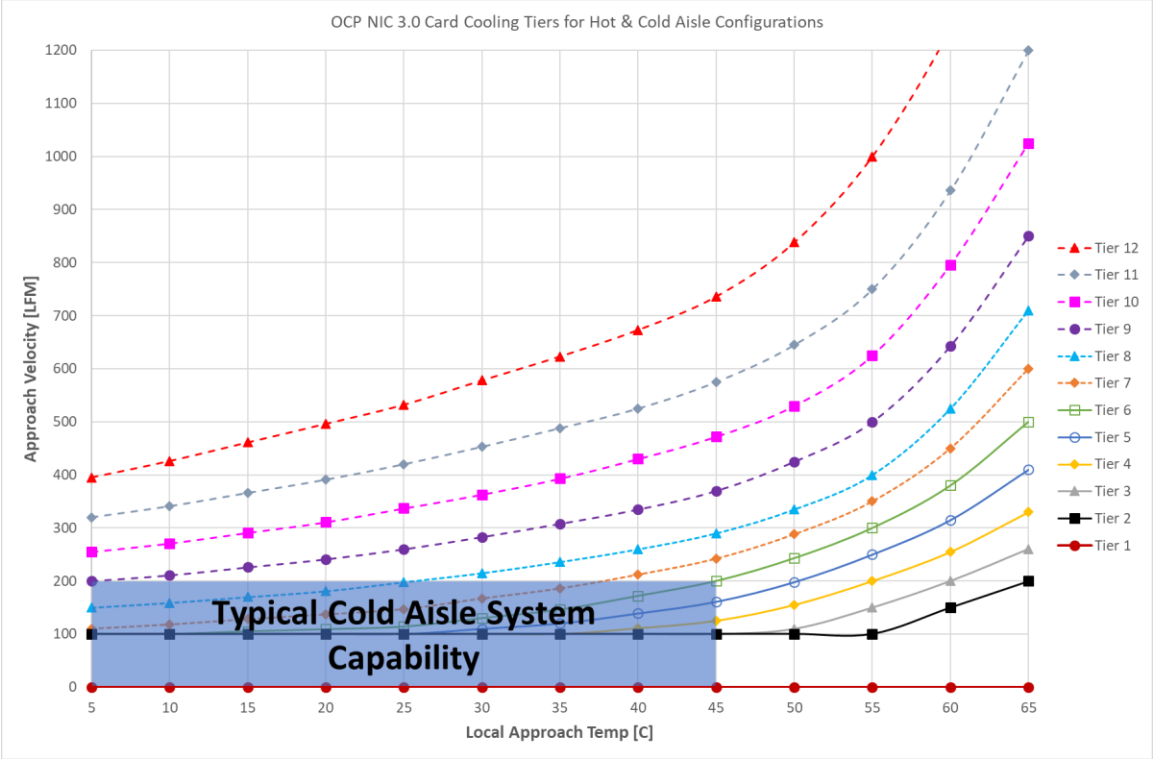


Figure 162: Typical Operating Range for Cold Aisle Configurations



7.7 Non-Operational Shock & Vibration Testing

OCP NIC 3.0 components are deployed in various environments. As such, all OCP NIC 3.0 cards shall be subjected to shock and vibration testing to ensure products do not sustain damage during normal operational or transportation conditions. While end customer deployments may require an additional final system level test, this section sets the minimum shock and vibration requirements for an OCP NIC 3.0 card that must also be considered.

Shock and vibration testing shall be done in accordance with the procedures listed below. The tests shall be conducted using a vertical shock table. The OCP NIC 3.0 card shall be secured in the standard test fixture as described in Section 7.7.1.

7.7.1 Shock & Vibe Test Fixture

The OCP NIC 3.0 shock and vibe fixture supports simultaneous testing of up to four SFF, or four DSFF cards. The SFF fixture accepts card configurations that utilize the pull tab, ejector lever and internal lock mechanisms. The DSFF fixture accepts the pull tab and internal latch faceplate.

The fixture is comprised of a universal baseplate that allows for attaching SFF or DSFF guide rails and simulated chassis faceplates. The baseplate includes an industry standard vibration table hole pattern for securing the UUT for test. Figure 163 shows the SFF fixture.

CAD files for the current revision of the text fixture are available for download from the OCP NIC 3.0 wiki: https://www.opencompute.org/wiki/Server/NIC.

Figure 163: SFF Shock and Vibe Fixture

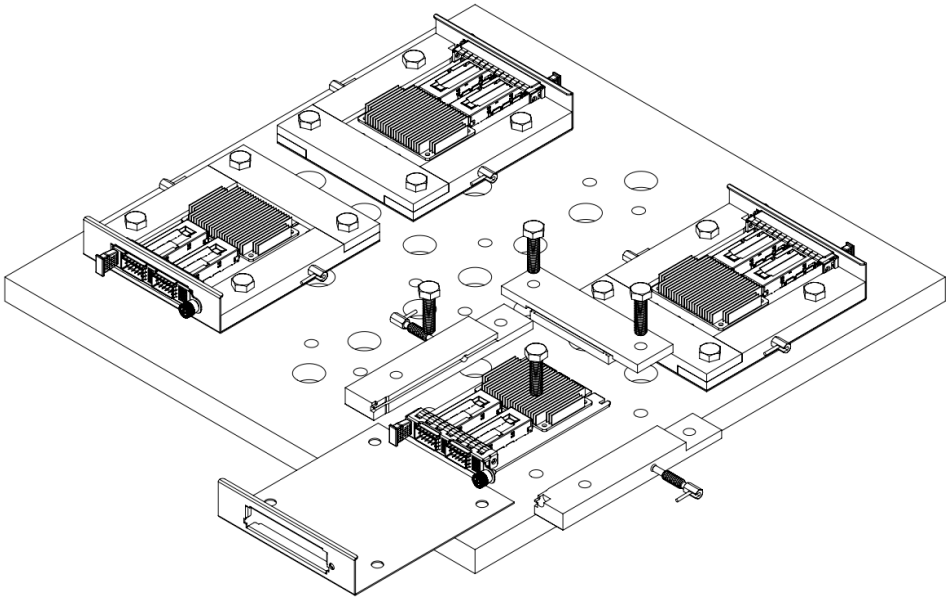
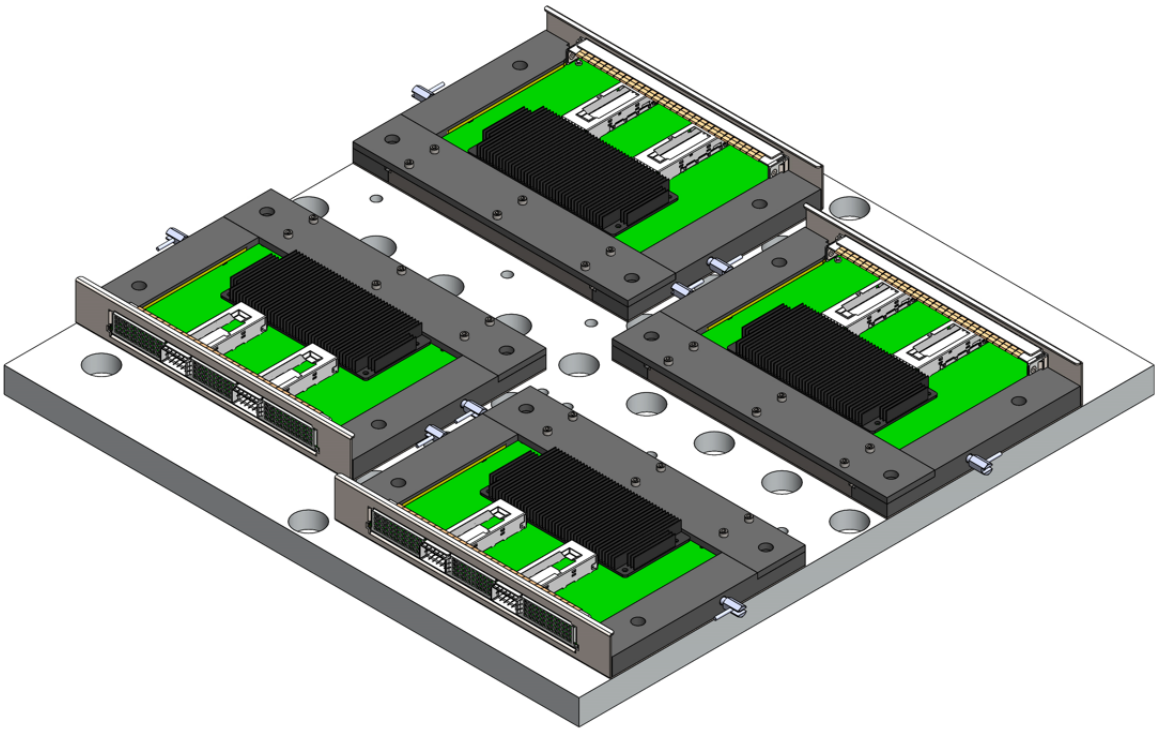


Figure 164: DSFF Shock and Vibe Fixture



7.7.2 Test Procedure

The following procedures shall be followed for the shock and vibration testing:

- A minimum sample size of three OCP NIC 3.0 cards shall be subjected to shock and vibration. Each sample shall be subjected to testing in the order listed below.
- All samples shall be verified for functionality prior to test.
- The OCP NIC 3.0 card shall be fixtured to simulate how the card will be mounted within a system. For example, the OCP NIC 3.0 card may be fixtured in the horizontal plane with the primary component side facing up for certain chassis configurations.
- The fixture shall be tested on all 6 sides. Each side shall be clearly labeled as 1-6 for test identification purposes. Testing shall be performed in the vertical axis only. The fixture shall be rotated until all six sides have been tested as the product may be dropped from any orientation during handling. Testing shall not be conducted on a three axis slip table.
- Non-operational vibration testing is performed at 1.88 G_{RMS} for a duration of 15 minutes per side per Table 82.

Table 82: Random Vibration Testing 1.88 G_{RMS} Profile

Frequency (Hz)	G^2/Hz
10	0.13
20	0.13
70	0.004
130	0.004
165	0.0018
500	0.0018

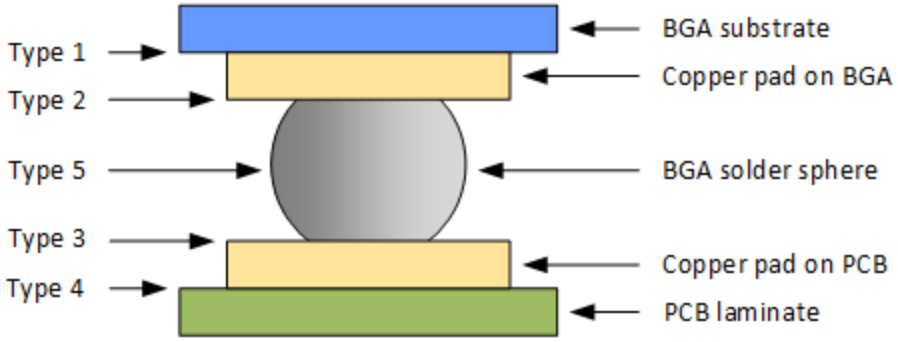
- Non-operational half-sine shock test at 71 G ±10% with a 2 ms duration per surface.
- Non-operational trapezoidal wave shock test at 50 G ±10% at a rate of 170 inches/sec per surface.
- All cards shall be checked for proper operation after the shock and vibration tests have been conducted. All three samples must be in full operating order to consider the product as a pass.

7.8 Dye and Pull Test Method

All Dye and Pull test methods shall be implemented per the IPC-TM-650 method 2.4.53 (Dye and Pull Test Method – formerly known as Dye and Pry). The Dye and Pull test uses a colored dye penetrant to visually indicate cracked solder joints on BGA devices. The test shall only be conducted after the Shock and Vibration testing has been conducted on the test samples. The Dye and Pull Test Method is a destructive test.

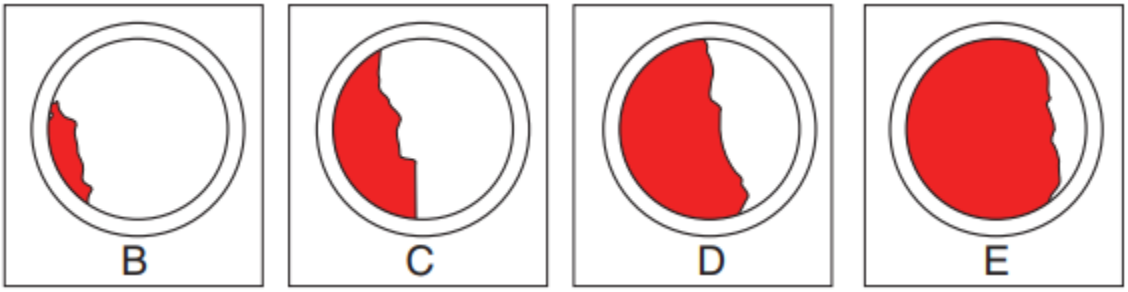
- A minimum sample size of three OCP NIC 3.0 cards shall be subjected to the Dye and Pull Test Method.
- All samples shall be first subjected to the Shock and Vibration testing outlined in Section 7.7.
- All samples shall be subjected to the preparation and test procedures of IPC-TM-650 method 2.4.53.
- Following the pull-test operation, the board sample shall be examined for dye indication at the target BGA area. Separation locations are categorized in to the following five areas:
  - Type 1 – Separation between the BGA copper pad and the BGA substrate.
  - Type 2 – Separation between the BGA copper pad and the BGA solder sphere.
  - Type 3 – Separation between the BGA solder sphere and the copper pad on the PCB.
  - Type 4 – Separation between the copper pad on the PCB and the PCB laminate.
  - Type 5 – Separation of the BGA solder sphere.

Figure 165: Dye and Pull Type Locations



- Samples shall be subjected to the following failure criteria:
  - Dye coverage of >50% (“D” and “E” in Figure 166) of any Type 2 or Type 3 BGA cracks are present in the test sample.
  - One or more Type 1 or Type 4 BGA cracks are present in the test sample.

Figure 166: Dye Coverage Percentage



The following exceptions are allowed:

- For “via-in-pad” designs, dye is allowed on the laminate surface (under the pad), as long as the dye has not entered the inner-via laminate area or is found on the separated via-barrel wall.
- Allowances for dye indications on mechanical (non-electrical) BGA corner locations or multiple use locations (grounds, powers) may be determined by the appropriate Engineering Team.

7.9 Gold Finger Plating Requirements

This section defines the minimum plating/quality requirements for the OCP NIC 3.0 gold fingers.

7.9.1 Host Side Gold Finger Plating Requirements

Per Section 6.4 (Environmental Requirements) of the PCIe CEM specification, the minimum host side gold finger plating is 30 microinches of gold over 50 microinches of nickel. OCP NIC 3.0 card vendors shall individually evaluate the minimum plating required.

The recommendation for OCP NIC 3.0 is to 30 microinches of gold over 150 microinches of nickel.

7.9.2 Line Side Gold Finger Durability Requirements

The line side connectors must be designed to support a minimum of 250 error free insertion cycles. In order to accomplish this, it is required that the minimum contact plating be as follows:

- SFP and QSFP connectors: 30 microinches of gold over 50 microinches of nickel
- RJ45 connectors have a minimum of 50 microinches of gold over 50 microinches of nickel

8 Regulatory

8.1 Required Compliance

An OCP NIC 3.0 card shall meet the following Environmental, EMC and safety requirements.

> **Note:** Emissions and immunity tests in Section 8.1.4 are to be completed at the system level. The OCP NIC 3.0 vendors should work with the system vendors to achieve the applicable requirements listed in this section.

8.1.1 Required Environmental Compliance

- China RoHS Directive
- **EU RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. The substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates.
- **EU REACH Regulation (EC) No 1907/2006** addresses the production and use of chemical substances and their potential impact on human health and the environment.
- **EU Waste Electrical and Electronic Equipment ("WEEE")** Directive (2012/19/EU) – mandates the treatment, recovery and recycling of EEE.
- **The Persistent Organic Pollutants Regulation (EC) No. 850/2004** bans production, placing on the market and use of certain persistent organic pollutants.
- **The California Safe Drinking Water and Toxic Enforcement Act of 1986 ("Proposition 65")** sets forth a list of regulated chemicals that require warnings in the State of California.
- **The Packaging and Packaging Waste Directive 94/62/EC** limits certain hazardous substances in the packaging materials
- **Batteries Directive 2006/66/EC** regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances.

8.1.2 Required EMC Compliance

- Radiated and Conducted Emissions requirements are based on deployed geographical locations. Refer to Table 83 for details.

Table 83: FCC Class A Radiated and Conducted Emissions Requirements Based on Geographical Location

Targeted Geography	Applicable Specifications
USA	FCC, 47 CFR Part 15, Class A digital device (USA)
Canada	ICES-003, class A (CAN)
EU	EN 55032: 2015+AC:2016 Class A Radiated and Conducted Emissions requirements for European Union EN 55035: 2017 Immunity requirements for the European Union (EU) EN 55024: 2010+A1:2015 Immunity requirements for European Union (EU) may alternatively be reported. **Note:** EN55024 has been superseded by EN55035 as of March 24th, 2021. OCP NIC 3.0 implementers are encouraged to test to EN55035.
Australia/New Zealand	AS/NZS CISPR 32:2015 Class A CISPR 32:2015 for Radiated and Conducted Emissions requirements

Targeted Geography	Applicable Specifications
Japan	VCCI 32-1 Class A Radiated and Conducted Emissions requirements
Korea	KN32 – Radiated and Conducted Emissions KN35- Immunity
Taiwan	BSMI CNS13438: 2006 (complete) Class A Radiated and Conducted Emissions requirements

- **CE** – Equipment must pass the CE specification
- All technical requirements covered under **EMC Directive (2014/30/EU)**

8.1.3 Required Product Safety Compliance

- Safety – requirements are listed in Table 84.

Table 84: Safety Requirements

Targeted Category	Applicable Specifications
Safety	UL 62368-1 and CAN/CSA C22.2 No. 62368-1-14, 3rd Edition. Audio/video, information and communication technology equipment Part 1: Safety requirements, dated 2019/12/13.

8.1.4 Required Immunity (ESD) Compliance

The OCP NIC 3.0 card shall meet or exceed the following ESD immunity requirements listed in Table 85.

Table 85: Immunity (ESD) Requirements

Targeted Category	Applicable Specifications
Immunity (ESD)	EN 55035 2017, and IEC 61000-4-2 2008 for ESD. EN 55024 may alternatively be reported. Required ±4 kV contact discharge and ±8 kV air discharge. **Note:** EN55024 has been superseded by EN55035. OCP NIC 3.0 implementers are encouraged to test to EN55035.
NEBS Level 3 (optional)	Optionally test devices to NEBS Level 3 – Required ±8 kV contact discharge and ±15 kV air discharge with interruptions not greater than 2 seconds. The device shall self-recover without operator intervention. Note: NEBS compliance is part of the system level testing. The OCP NIC 3.0 specification is providing a baseline minimum recommendation for ESD immunity.

8.2 Recommended Compliance

All OCP NIC 3.0 cards are required to meet the requirements specified in Section 8.1. Card vendors should also consider meeting the requirements below.

8.2.1 Recommended Environmental Compliance

- **Halogen Free:** IEC 61249-2-21 Definition of halogen free: 900ppm for Bromine or Chlorine, or 1500ppm combined total halogens.
- **Arsenic:** 1000 ppm (or 0.1% by weight)
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act** requires companies using tin, tantalum, tungsten, and gold (“3TG”) in their products to verify and disclose the mineral source.

While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntary reporting of this information.

8.2.2 Recommended EMC Compliance

- FCC, 47 CFR Part 15, Subpart B Class A digital device (USA) with 10dB margin. Refer to the baseline requirements shown in Section 8.1.2 for details.

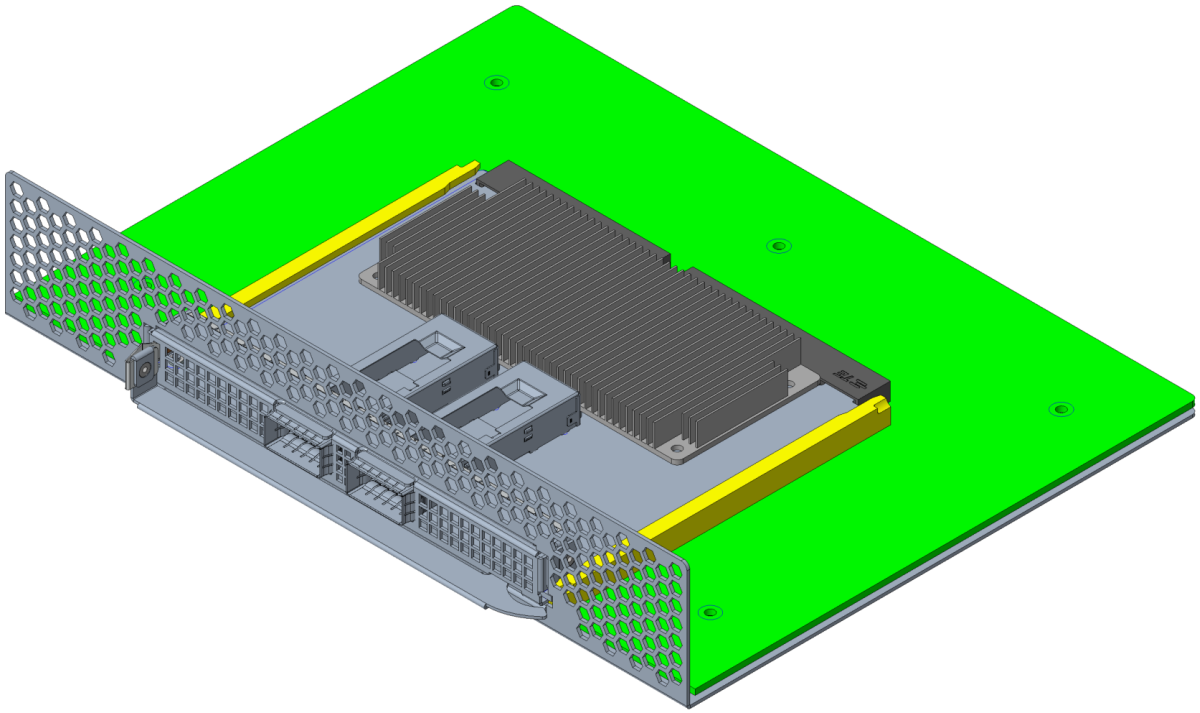
9 Appendix – LFF

The LFF has been deprecated. The OCP NIC 3.0 workgroup strongly encourages the use of SFF and DSFF instead. This section contains the LFF electrical and mechanical requirements from version 1.3.0 of the specification for historical reasons and will no longer be maintained. For full context, refer to the appropriate sections in the main specification.

9.1 Mechanical Requirements – Card Side – LFF

Figure 167 shows a representative LFF. LFF baseboard implementations are not compatible with DSFF slots due to the connector differences. The LFF uses a 4C+ Primary Connector and a 4C Secondary Connector.

Figure 167: Representative LFF OCP NIC 3.0 Card with Dual QSFP Ports



9.1.1 Large Form Factor (LFF)

The Large Form Factor (LFF) uses the 4C+ Primary Connector and a 4C Secondary Connectors, with corresponding 4C+ and 4C gold fingers. The LFF supports higher power envelopes and provides additional board area for more complex designs.

The LFF supports up to 150 W of delivered power to the card edge across the two connectors. The actual cooling capacity for a LFF card is dependent on the ambient conditions over the NIC. An example LFF block diagram is shown in Figure 168. The components shown in the figure are for illustrative purposes only.

The LFF slot may accept a SFF NIC when using a guide rail adapter – this adapter is outside the scope of this specification.

The LFF Card may utilize both the Primary and Secondary Connectors (as shown in Figure 169), or just the Primary Connector (as shown in Figure 170) for lower PCIe lane count applications.

Figure 168: LFF Block Diagram (not to scale)

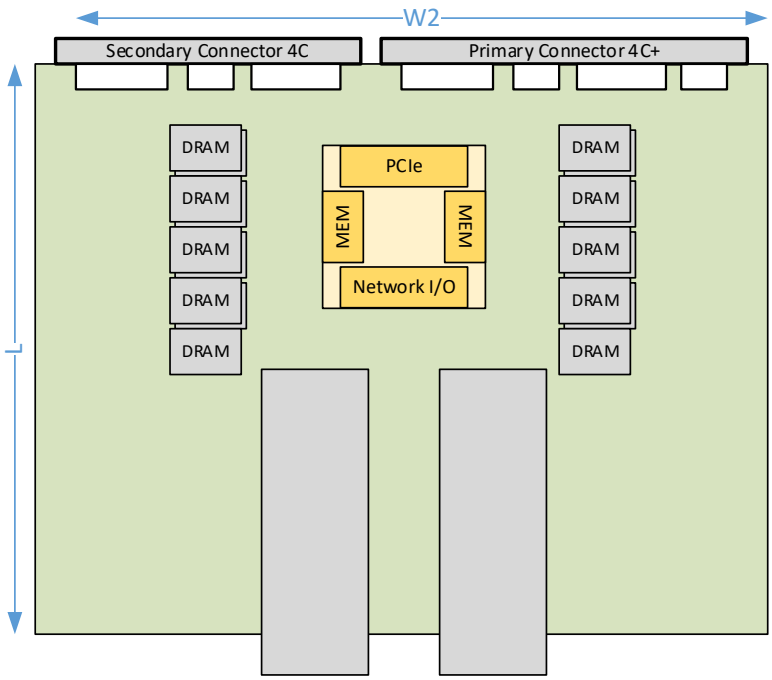


Figure 169: Primary Connector (4C+) and Secondary Connector (4C) LFF OCP NIC 3.0 Cards

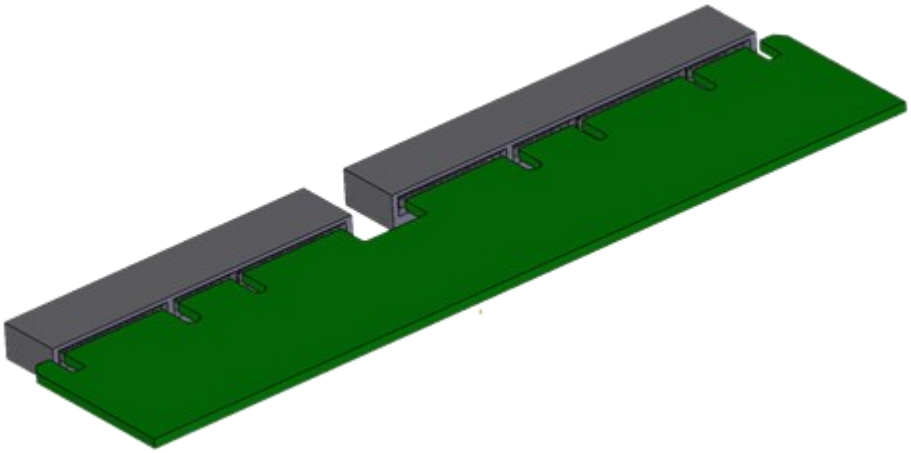
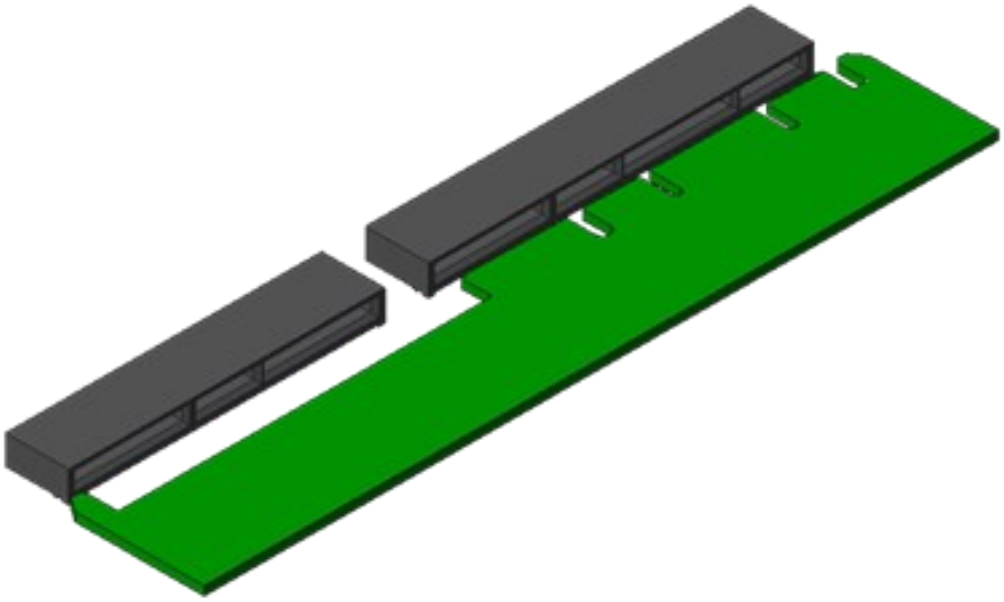
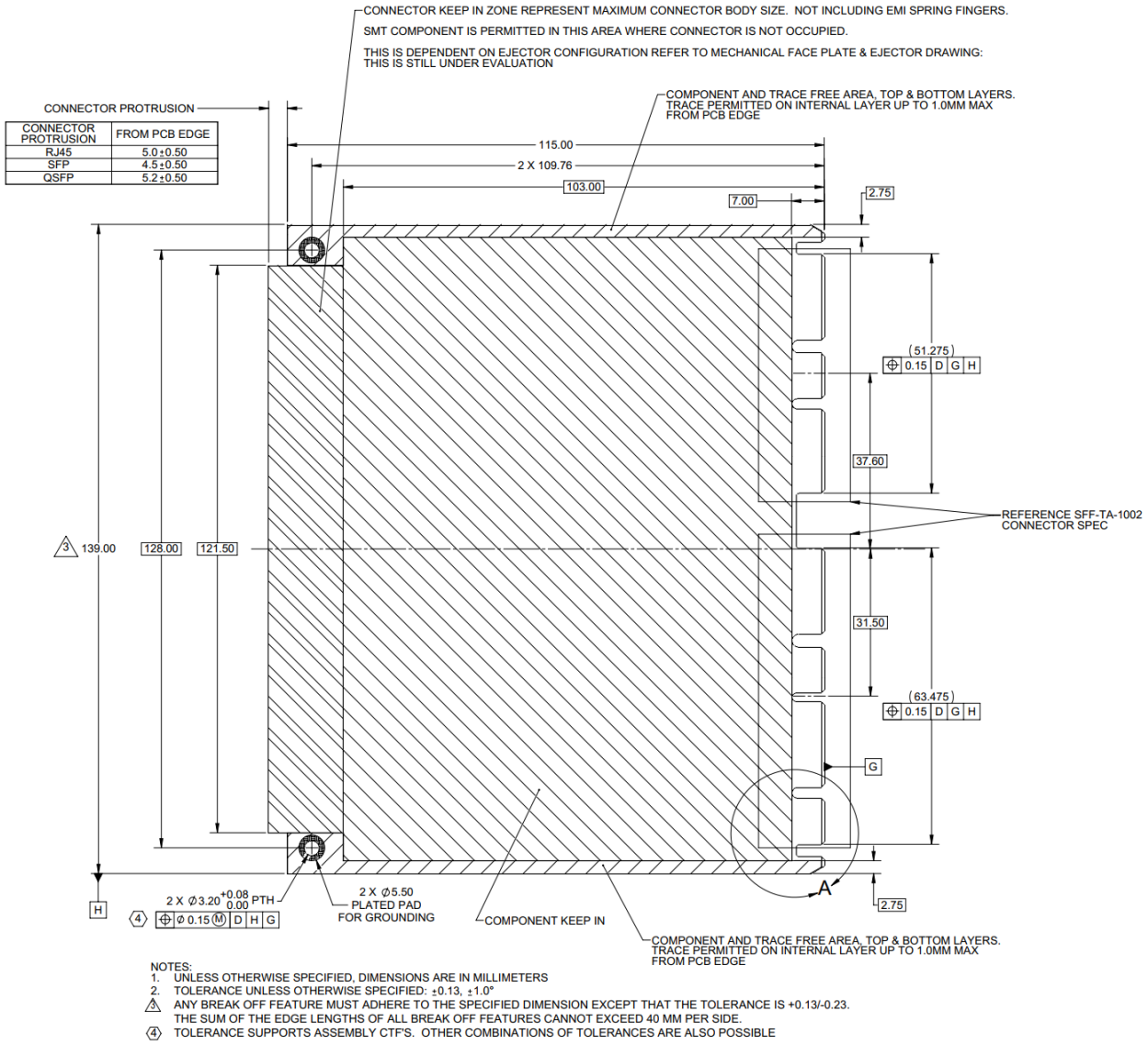


Figure 170: Primary Connector (4C+) Only LFF OCP NIC 3.0 Cards



9.1.2 LFF Dimensions and Keep Out Zones

Figure 171: LFF Keep Out Zone – Top View



NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1.0°
3. ANY BREAK OFF FEATURE MUST ADHERE TO THE SPECIFIED DIMENSION EXCEPT THAT THE TOLERANCE IS +0.13/-0.23. THE SUM OF THE EDGE LENGTHS OF ALL BREAK OFF FEATURES CANNOT EXCEED 40 MM PER SIDE.
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE

Figure 172: LFF Keep Out Zone – Top View – Detail A

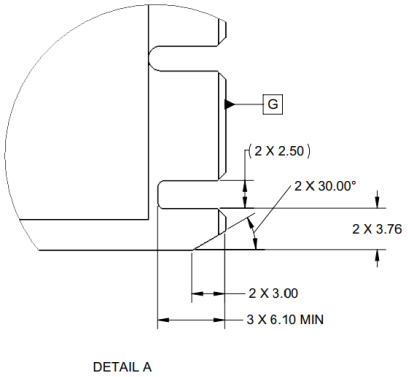


Figure 173: LFF Keep Out Zone – Bottom View

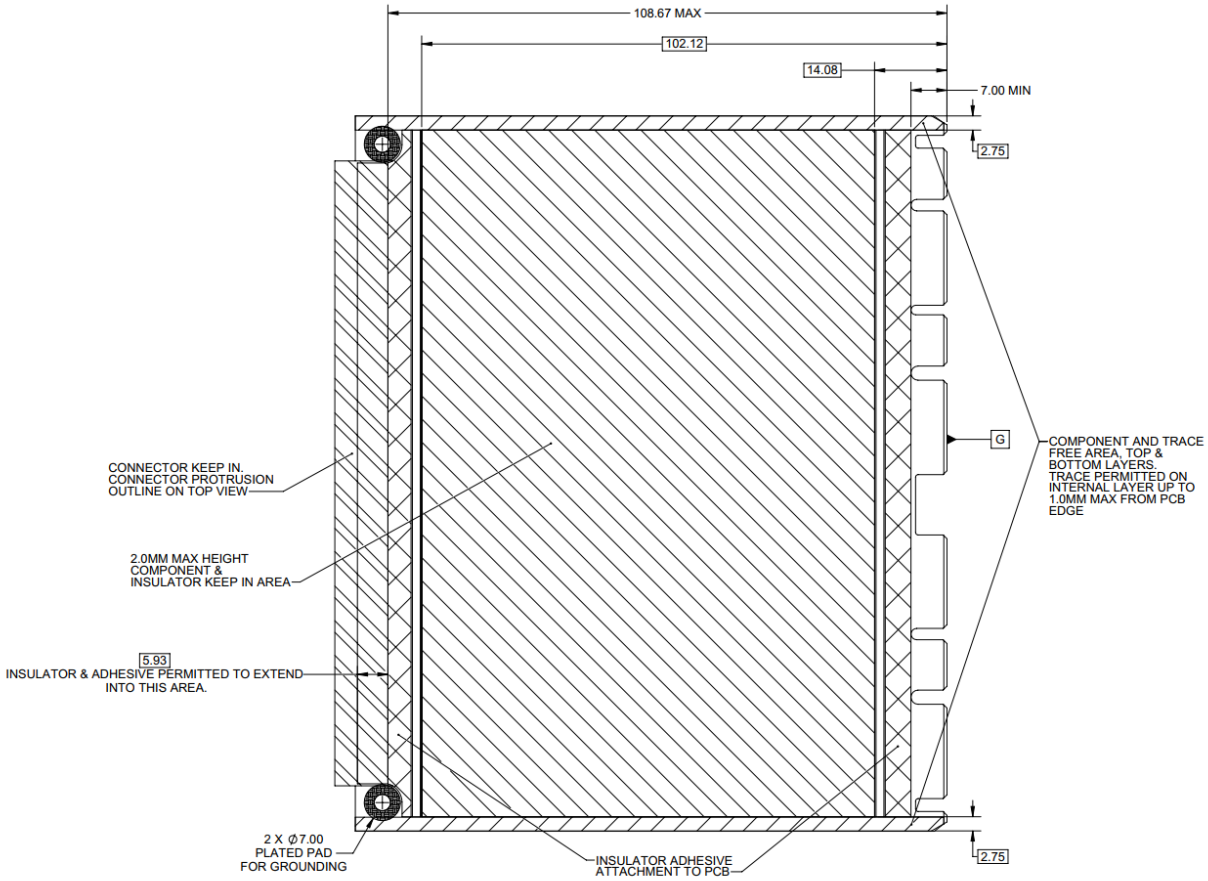
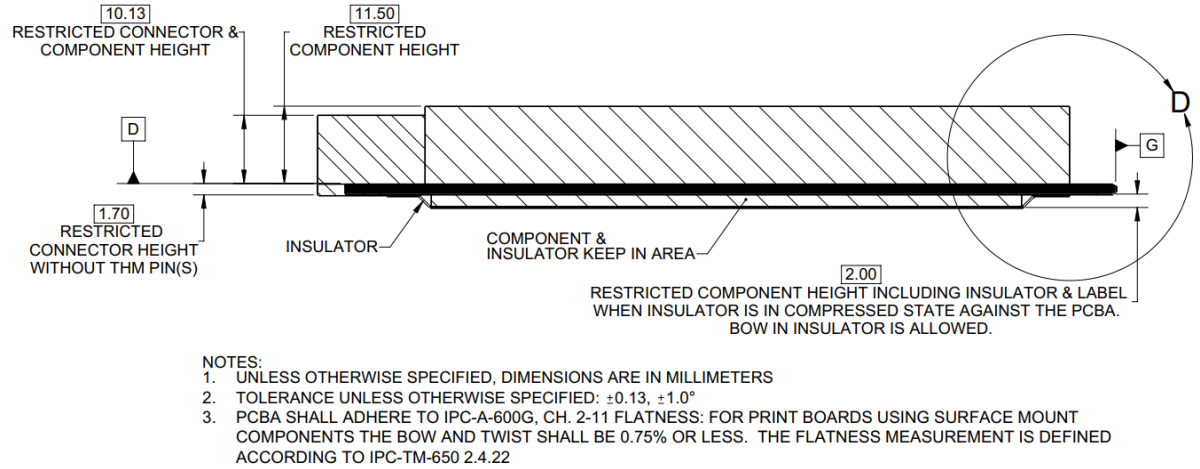
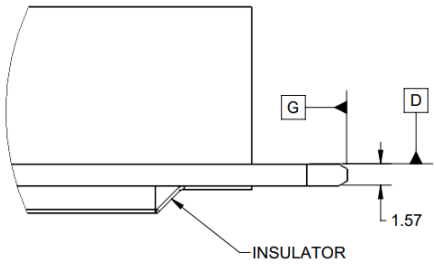


Figure 174: LFF Keep Out Zone – Side View



NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1.0°
3. PCBA SHALL ADHERE TO IPC-A-600G, CH. 2-11 FLATNESS: FOR PRINT BOARDS USING SURFACE MOUNT COMPONENTS THE BOW AND TWIST SHALL BE 0.75% OR LESS. THE FLATNESS MEASUREMENT IS DEFINED ACCORDING TO IPC-TM-650 2.4.22

Figure 175: LFF Keep Out Zone – Side View – Detail D



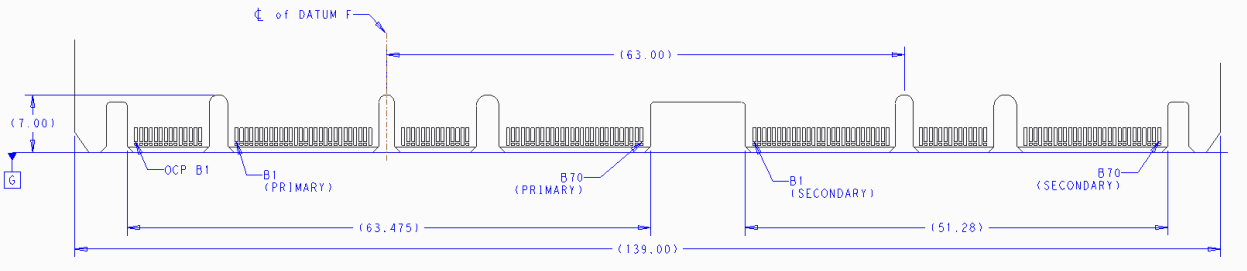
DETAIL D

9.1.3 LFF Gold Finger Requirements

Refer to SFF-TA-1002 and Section 2.3.3 for the 4C+ (Primary Connector) and 4C (Secondary Connector) gold finger requirements.

The full complement of the LFF pins span across two connectors and its respective card gold fingers. The connector pitch is defined in Figure 176. The pitch is measured from Datum F of each connector.

Figure 176: LFF (4C+ & 4C) Gold Finger Pitch – x32 – Top Side (“B” Pins)



9.1.4 LFF Faceplate Configurations

The LFF configuration views are shown below. A single faceplate implementation is available for the LFF – with a single ejector latch. The long ejector is the default configuration; however, a short ejector version is available for non-shadowed front I/O configurations and is being considered for future development. The internal locking mechanism is not available on LFF cards. Like the SFF and TSFF, if additional LFF faceplate implementations become available, the same LFF OCP NIC 3.0 PBA accepts up to three faceplate types depending on the end application. Faceplates are attached to the PCBA at the time of manufacture. The drawings shown in Figure 177 below illustrate a representative front, side and top views of the LFF.

Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 mm x 3.0 mm may be added to help optimize airflow while maintaining the integrity of the faceplate structure. EMI considerations should also be considered during the design process. Refer to the images shown in Figure 178 for example square vent configurations depending on the line side I/O connectors.

Depending on the OCP NIC 3.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep in regions as defined by the PBA mechanical drawings and faceplate drawings.

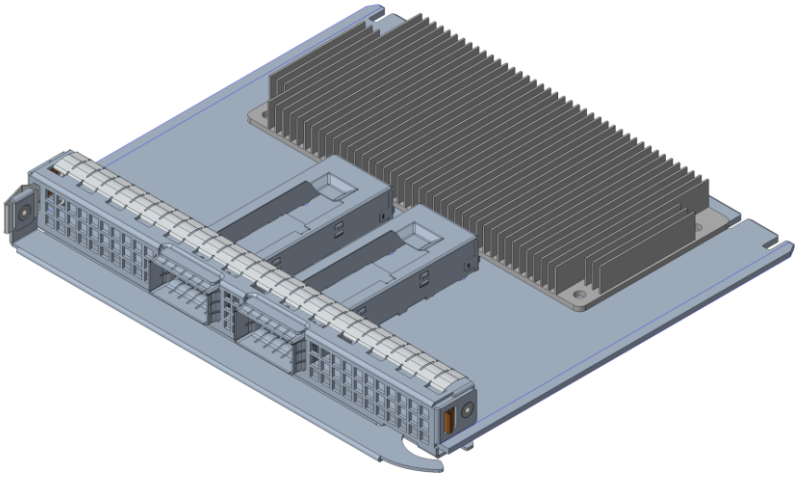
Note: The OCP NIC 3.0 card supplier shall add port identification on the faceplate assembly that meet their manufacturing and customer requirements.

All the OCP NIC 3.0 CAD files are available for download and use on the OCP NIC 3.0 Wiki site:
https://www.opencompute.org/wiki/Server/NIC

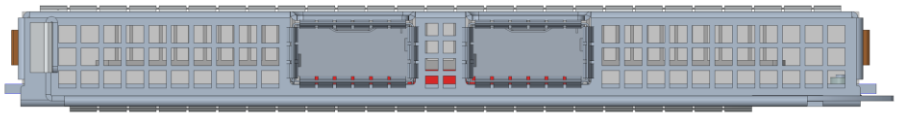
4812

Figure 177: LFF NIC Configuration Views

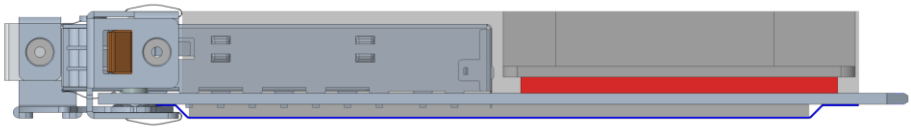
LFF with Ejector Latch



Front View



Side View



Top View

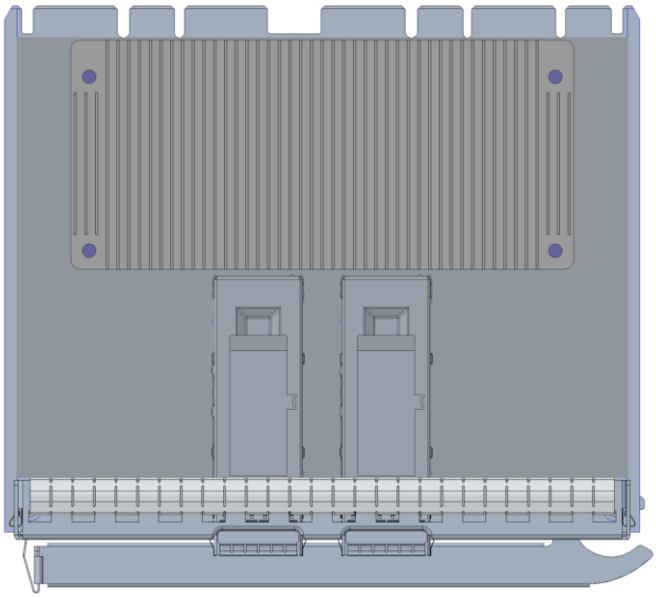


Figure 178 illustrates example LFF 3D views for the supported line side I/O implementations. The line side I/O implementations are discussed in Section 4.4.

Figure 178: LFF NIC Line Side 3D Views

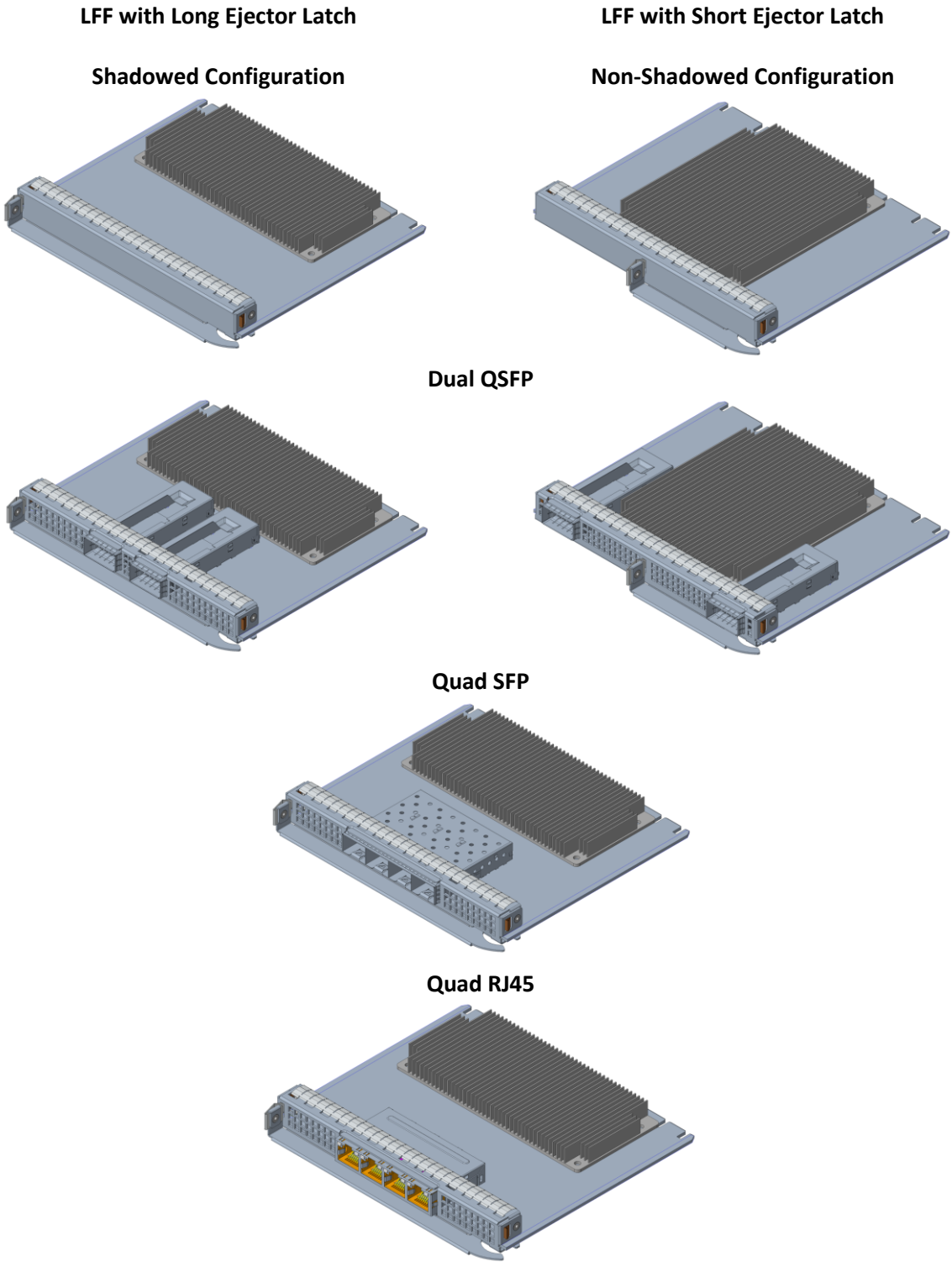
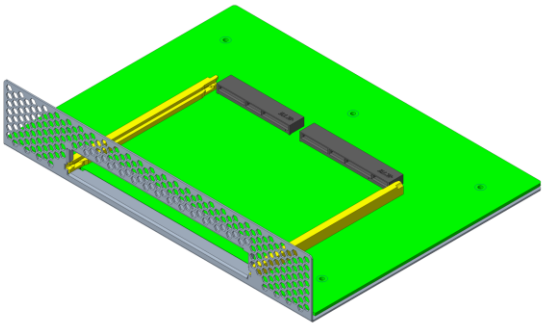
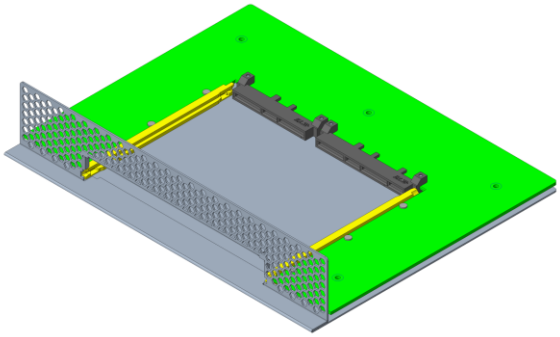


Figure 179 illustrates example LFF 3D views of the ejector latch assembly mounted in a chassis utilizing a straddle mount connector and a right-angle connector. The baseboard connector options are discussed in Section 3.1. The LFF OCP NIC 3.0 card is identical for both chassis connector options.

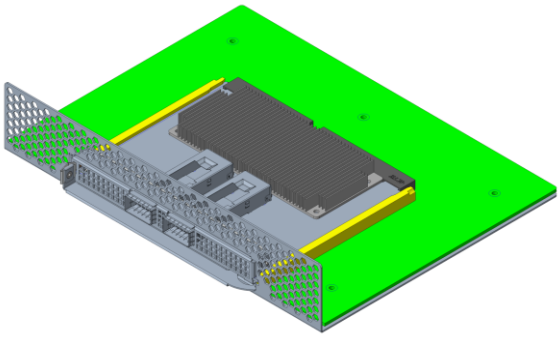
Figure 179: LFF NIC Chassis Mounted 3D Views



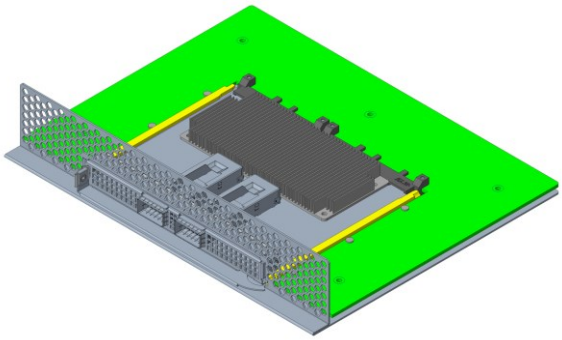
Right Angle Baseboard Connector



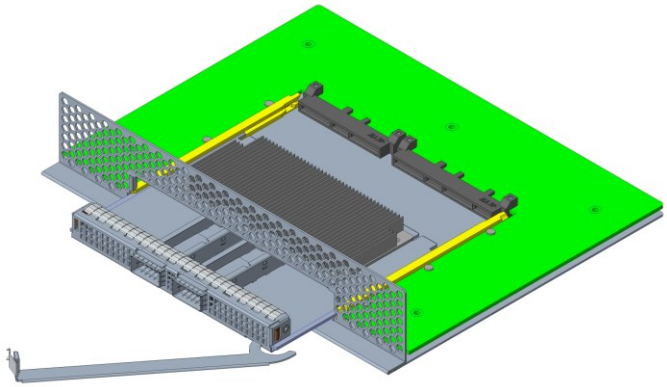
Straddle Mount Baseboard Connector



NIC Installed in Baseboard with Right Angle



NIC Installed in Baseboard with Straddle Mount



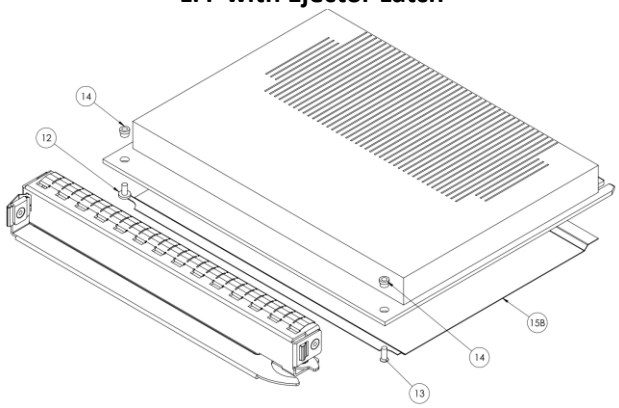
NIC Insertion / Removal (As shown with a Straddle Mount Connector)

9.1.5 LFF Top Level Assembly

The image in Figure 180 illustrate the exploded top-level assemblies for the LFF.

Figure 180: PBA Exploded Views (LFF)

LFF with Ejector Latch

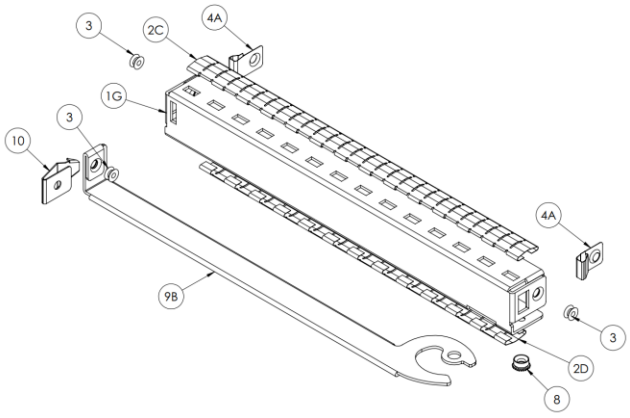


9.1.6 Faceplate Subassembly – LFF

The image in Figure 181 illustrates LFF faceplate subassembly as an exploded view. The LFF bill of materials is shown in Section 9.1.7.

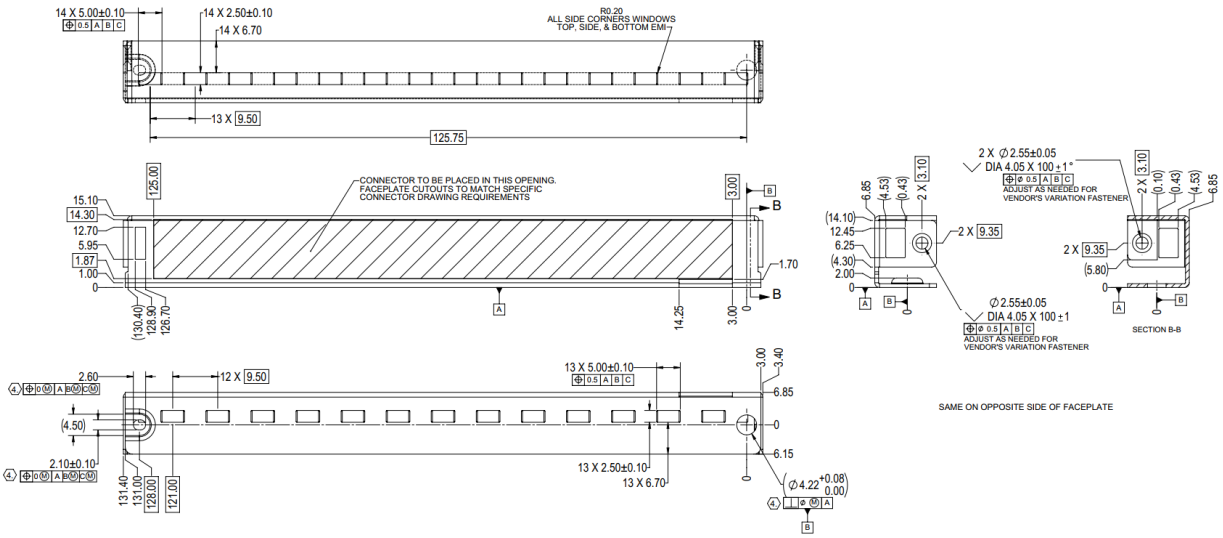
Figure 181: Faceplate Assembly Exploded Views (LFF)

LFF with Ejector Latch



9.1.6.1 LFF Generic I/O Faceplate

Figure 182: LFF Generic I/O Faceplate – Ejector Version (2D View)

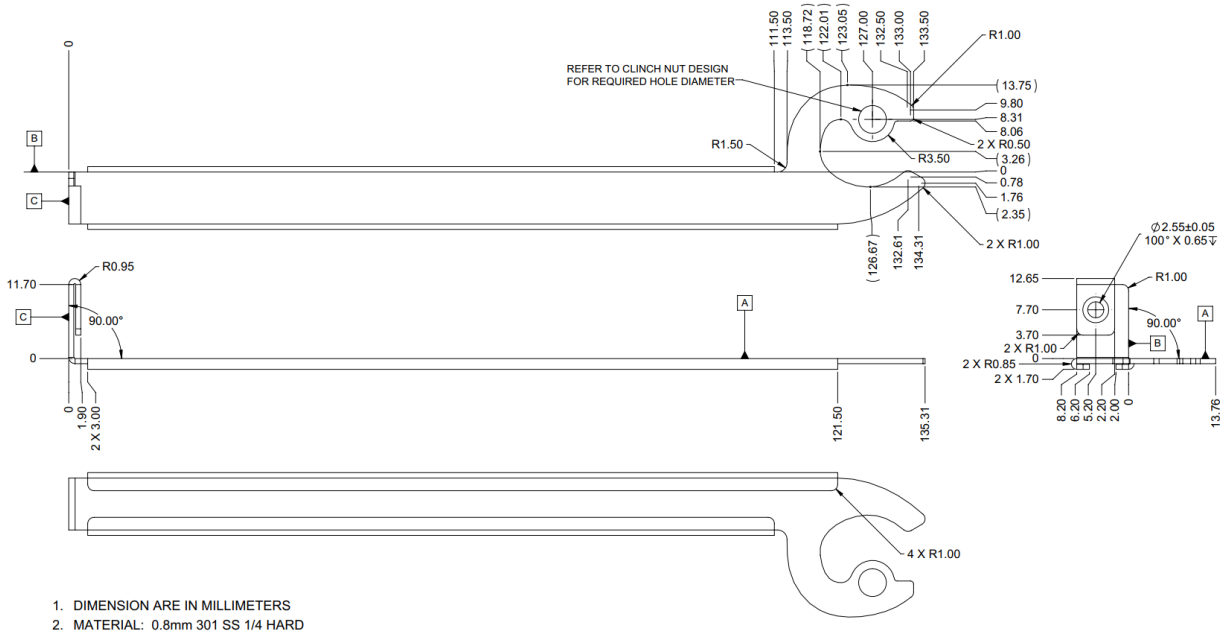


1. DIMENSION ARE IN MILIMETER
2. MATERIAL: 0.8mm CRS
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, MAX BEND RADIUS 0.30mm
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS ALLOWED. FACEPLATE GEOMETRY MUST BE MAINTAINED. ANY DEVIATIONS MUST BE APPROVED.
6. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

9.1.6.2 Ejector Levers (LFF)

This section defines the LFF ejector lever dimensions.

Figure 183: LFF I/O Faceplate – Ejector Lever (2D View)



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm 301 SS 1/4 HARD
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, ±1.0°
4. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

9.1.7 Faceplate Subassemblies – Bill of Materials (BOM) – LFF

Table 86 shows the bill of materials for the card assemblies. Item number call outs align with the item numbering in Section 2.6.1

Note: Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers of Table 86. Refer to the 3D CAD files for hardware specifics not covered by this table.

Table 86: Bill of Materials for LFF Faceplate Assemblies

Item #	Item description	Part Number / Drawing	Supplier
1G	Faceplate	See Section 2.6.3.2: 1G NIC_OCPv3_LFF_Faceplate_Latch_20190719.pdf	Custom
2C 2D	Top and Bottom EMI Fingers	2C LT18CJ1923 – 27 fingers (Laird) TF187VE32F11-5.03-08 (Tech-Etch) 2D LT18CJ1922 – 25 fingers (Laird) TF187VE32F11-4.66-08 (Tech-Etch)	Laird, Tech-ETCH
3	Rivet	1-AC-2424-01	Dong Guan KSETT Hardware Technology
4A	Side EMI Fingers	4A LT18DP1911 (for LFF)	Laird
5	Thumbscrew	4C-99-343-K081	Southco, Inc.
6A 6B	Pull tab w/2x screws	CN-99-459	Southco, Inc.
8	Clinch Nut	See Section 2.6.4.3 and drawing NIC_OCPv3_ClinchNut_20190719.pdf	Custom
9B	Ejector Handle	**LFF Ejector**: See Section 9.1.9 & Drawing 9B NIC_OCPv3_EjectorHandle_Long_20190719.pdf	Custom
10	Ejector Lock	See Section 2.6.4.2 and drawing NIC_OCPv3_EjectorLock_20190719.pdf	Custom
12*	Screw for securing faceplate to NIC	Phillips screw: ICMMBS200403N Torx screw: ITMMAE200402X	WUJIANG Screw Tech Precision Industry
13*	Screw for attaching faceplate and ejector to NIC	Phillips screw: FCMMQ200503N Torx screw: FTMMC200502X	WUJIANG Screw Tech Precision Industry
14	SMT nut (on NIC)	82-950-22-010-05-RL	Fivetech Technology Inc.
15B	Insulator	Refer to Section 2.7 for LFF (15B) insulator mechanical requirements	Custom

Note: * Phillips and Torx screws are allowed. Head types should not be mixed on the same assembly.

9.1.8 LFF Insulator

Figure 184: LFF Bottom Side Insulator (3D View)

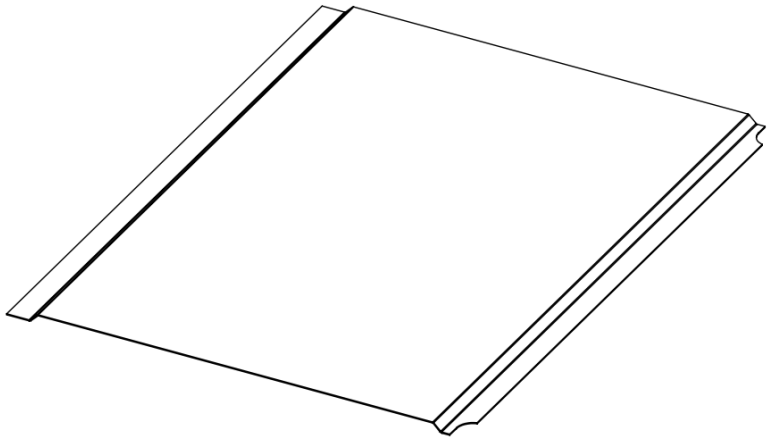
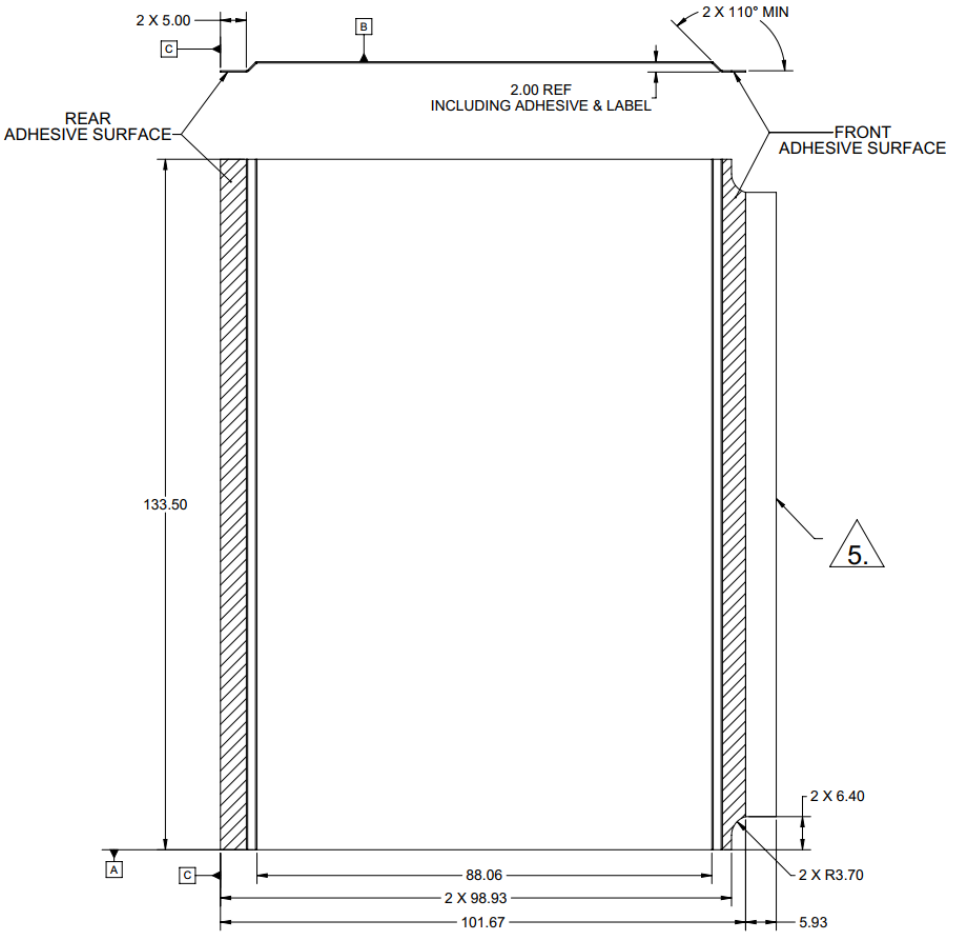
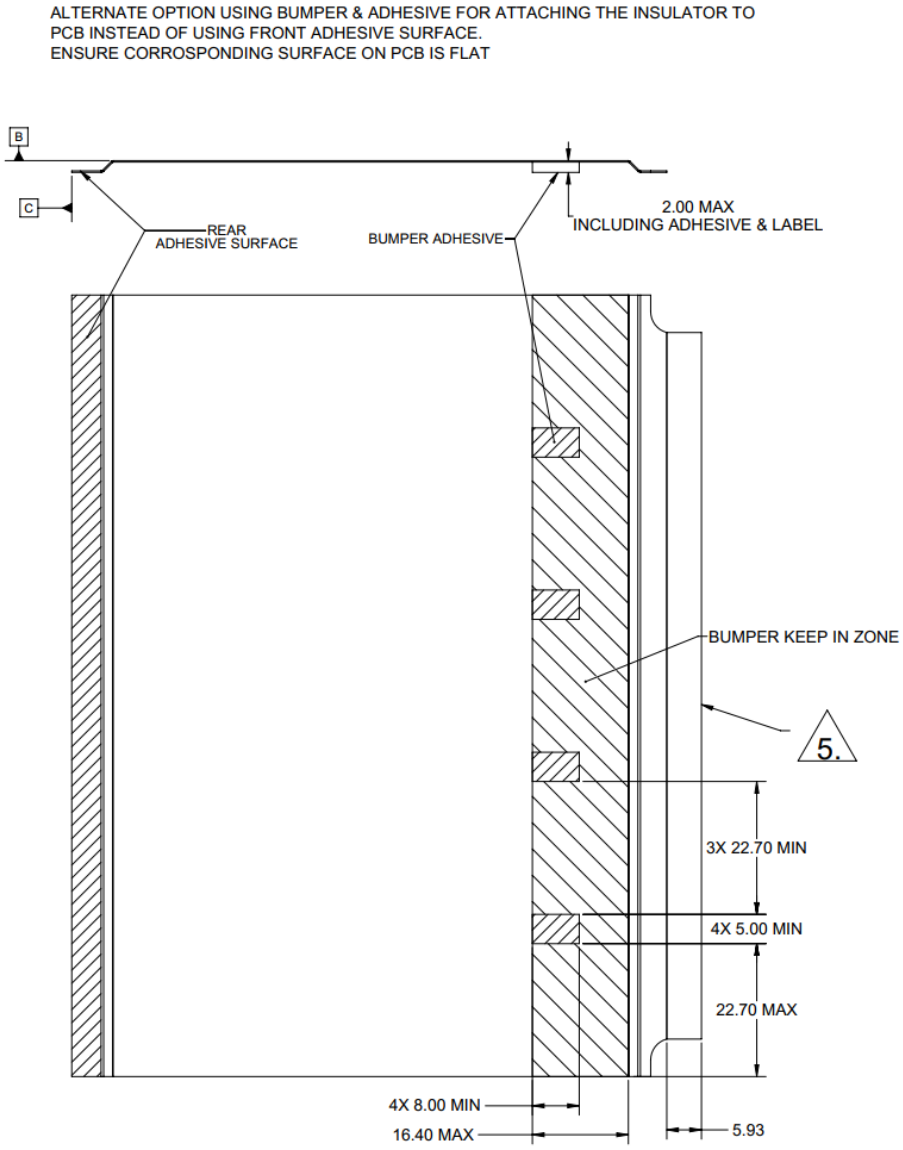


Figure 185: LFF Bottom Side Insulator (Top and Side View)



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: FORMEX GK-10BK, FORMEX N3 (HALOGEN FREE, BLACK OR NATURAL), 0.25mm THICKNESS
3. MATERIAL SHALL CONFORM TO 94VTM-0
4. ADHESIVE 3M 467MP 0.05mm THICKNESS
5. FRONT EDGE OF INSULATOR AND ADHESIVE MAY EXTEND TO 107.60MM IF NECESSARY TO PROTECT LEDS ON SECONDARY SIDE OF PCBA.
6. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.30mm, ±1.0°

4862 Figure 186: LFF Bottom Side Insulator (alternate) (Top and Side View)



4863

4864 ### 9.1.9 LFF Ejector Latch CTF Dimensions

4865 The following dimensions are considered critical-to-function (CTF) for each LFF OCP NIC 3.0 card. The
4866 CTF default tolerances are shown in Section 2.8.1.
4867

Figure 187: LFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View)

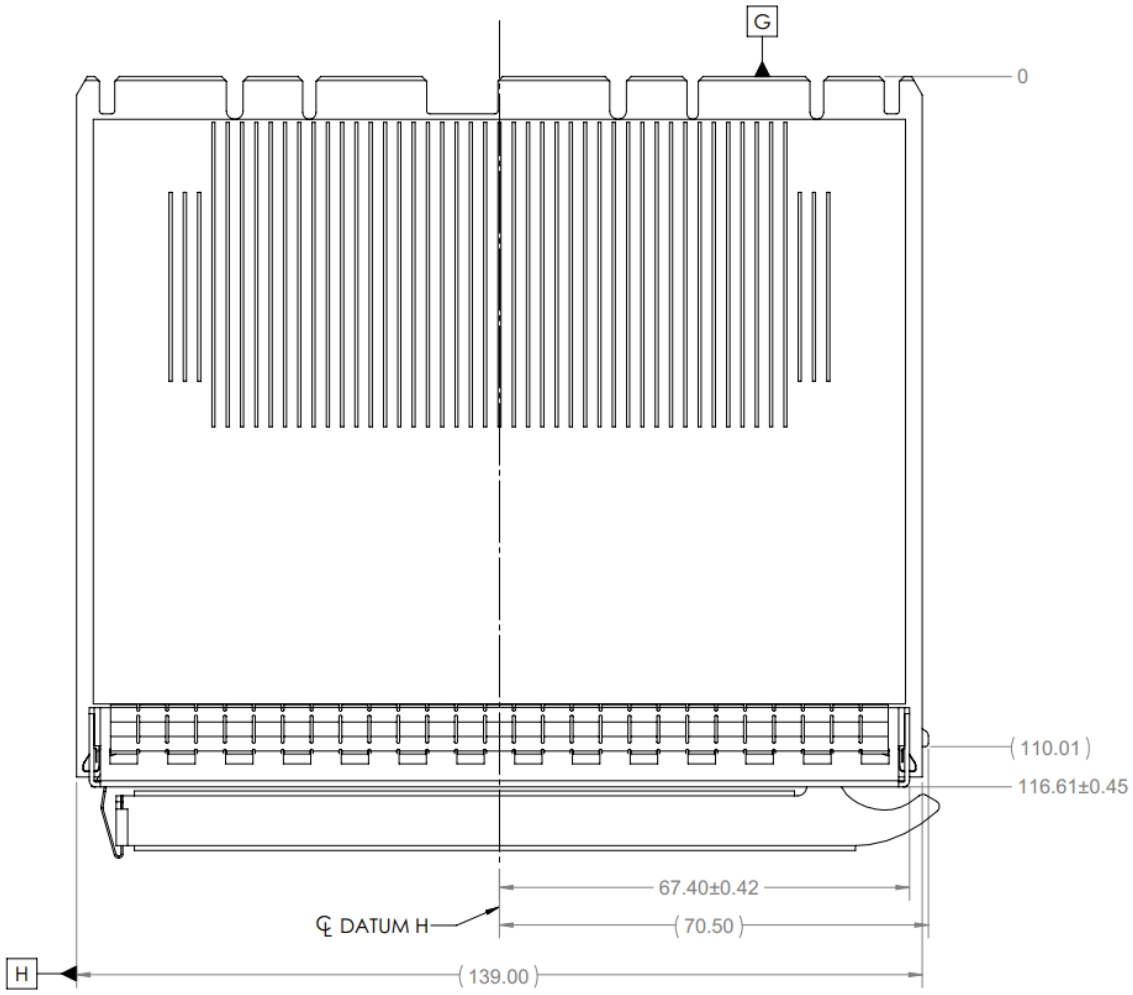


Figure 188: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View)

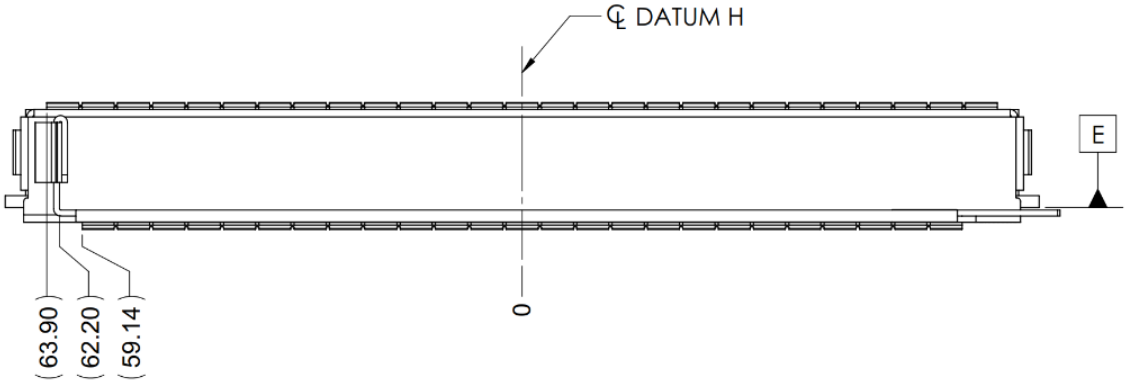


Figure 189: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View)



9.2 Mechanical Requirements – Baseboard Side – LFF

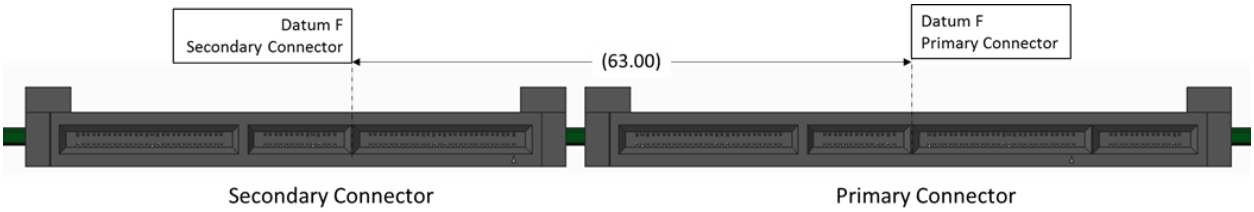
9.2.1 LFF Connector Pitch

To support the LFF, systems must locate the Primary and Secondary Connectors per the mechanical drawings shown in Figure 190 and Figure 191. These views show the connector orientation when looking "into" the slot from the chassis faceplate. The Primary Connector is located on the right. The Secondary Connector is located on the left. The connector pitch is 63.00 mm as measured from Datum F of each connector. Datum F is the same for right angle and straddle mount connector options.

Figure 190: LFF Connector Pitch with Right Angle Connectors



Figure 191: LFF Connector Pitch with Straddle Mount Connectors



9.2.2 LFF Baseboard CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each LFF baseboard chassis. The CTF default tolerances are shown in Section 3.3.1.

Note: The LFF baseboard CTF dimensions are applicable to both the right angle and straddle mount connector configurations. The faceplate opening relative to the baseboard changes due to the connector vertical offset, but all CTF dimensions remain identical.

Figure 192: LFF Baseboard Chassis CTF Dimensions (Rear View)

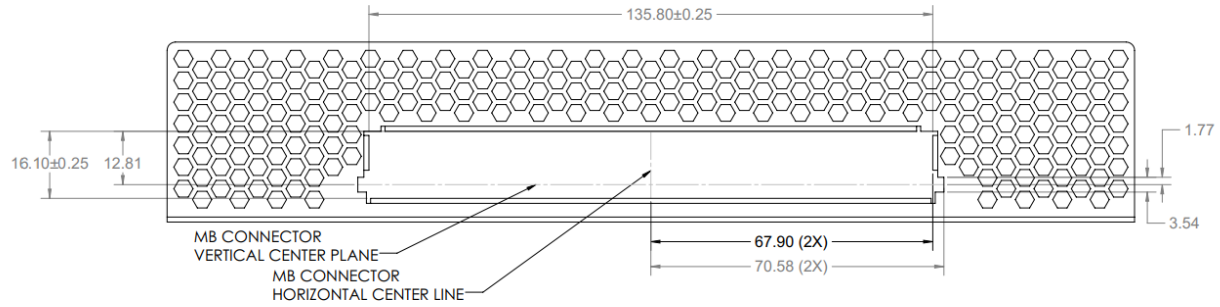


Figure 193: LFF Baseboard Chassis CTF Dimensions (Side View)

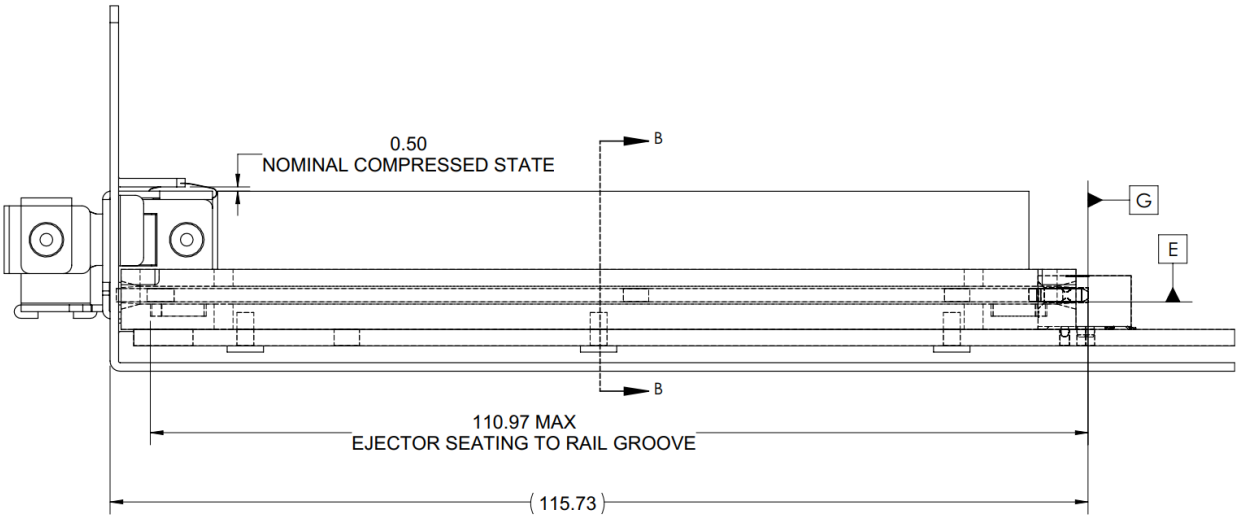
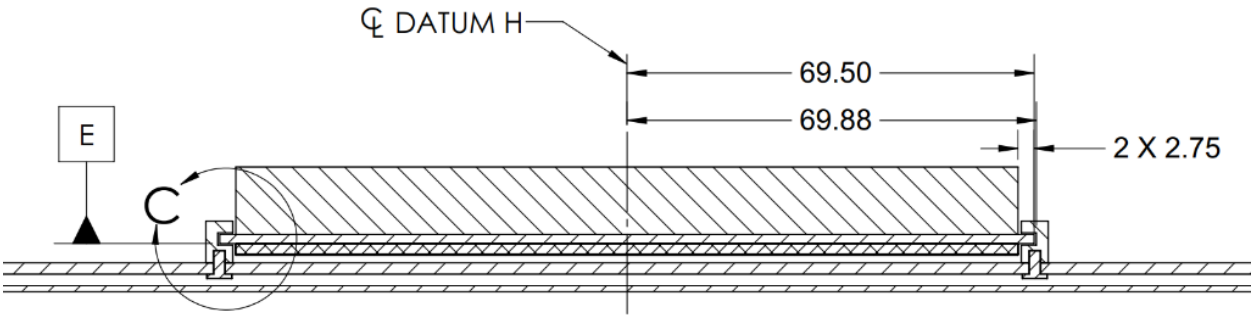
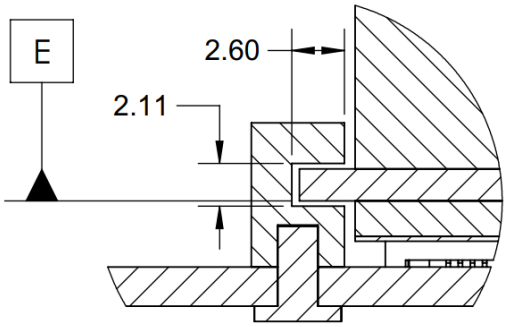


Figure 194: LFF Baseboard Chassis CTF Dimensions (Guide Rail View)



SECTION B-B

Figure 195: LFF Baseboard Chassis CTF Dimensions (Guide Rail – Detail C)



9.3 Electrical – LFF

LFF cards with a Secondary Connector allow for implementations with support for up to 32 lanes of PCIe. For an LFF implementation, the Secondary Connector is a 4C as defined in SFF-TA-1002 and does not include the OCP Bay Pins as found in the 4C+ definition.

9.3.1 LFF Pinout

For the LFF, the baseboard shall implement a 4C+ Primary Connector and 4C Secondary Connector. The card side implementation supports up to 32 PCIe lanes. Cards may implement less than the full set of PCIe lanes (e.g. 16 lanes with only a 4C+ gold finger). The pinout is shown below. Refer to Section 4.5 for signal description details.

Table 87: LFF Pin Definition (x32)

Primary Connector (4C+)			
Side B		Side A	
OCP_B1	NIC_PWR_GOOD0	PERST2#	OCP_A1
OCP_B2	MAIN_PWR_EN0	PERST3#	OCP_A2
OCP_B3	SCAN0_LD#	WAKE0#	OCP_A3
OCP_B4	SCAN0_DATA_IN	RBT0_ARB_IN	OCP_A4
OCP_B5	SCAN0_DATA_OUT	RBT0_ARB_OUT	OCP_A5
OCP_B6	SCAN0_CLK	SLOT_ID1	OCP_A6
OCP_B7	SLOT_ID0	FLEXIO_0_3	OCP_A7
OCP_B8	FLEXIO_0_2	FLEXIO_0_5	OCP_A8
OCP_B9	FLEXIO_0_1	FLEXIO_0_4	OCP_A9
OCP_B10	GND	GND	OCP_A10
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11
OCP_B12	REFCLKp2	REFCLKp3	OCP_A12
OCP_B13	GND	GND	OCP_A13
OCP_B14	FLEXIO_0_0	RBT0_CLK_IN	OCP_A14
Mechanical Key			
B1	+12V_EDGE	GND	A1
B2	+12V_EDGE	GND	A2
B3	+12V_EDGE	GND	A3
B4	+12V_EDGE	GND	A4
B5	+12V_EDGE	GND	A5
B6	+12V_EDGE	GND	A6
B7	BIF0#	SMCLK0	A7
B8	BIF1#	SMDAT0	A8
B9	BIF2#	SMRST0#	A9

Secondary Connector (4C)			
Side B		Side A	
B1	+12V_EDGE	GND	A1
B2	+12V_EDGE	GND	A2
B3	+12V_EDGE	GND	A3
B4	+12V_EDGE	GND	A4
B5	+12V_EDGE	GND	A5
B6	+12V_EDGE	GND	A6
B7	BIF3#	SMCLK1	A7
B8	BIF4#	SMDAT1	A8
B9	BIF5#	SMRST1#	A9

Primary Connector (4C+)			
Side B		Side A	
B10	PERST0#	PRSNTA0#	A10
B11	+3.3V_EDGE	PERST1#	A11
B12	AUX_PWR_EN0	PRSNTB2#	A12
B13	GND	GND	A13
B14	REFCLKn0	REFCLKn1	A14
B15	REFCLKp0	REFCLKp1	A15
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28
Mechanical Key			
B29	GND	GND	A29
B30	PETn4	PERn4	A30
B31	PETp4	PERp4	A31
B32	GND	GND	A32
B33	PETn5	PERn5	A33
B34	PETp5	PERp5	A34
B35	GND	GND	A35
B36	PETn6	PERn6	A36
B37	PETp6	PERp6	A37
B38	GND	GND	A38
B39	PETn7	PERn7	A39
B40	PETp7	PERp7	A40
B41	GND	GND	A41
B42	PRSNTB0#	PRSNTB1#	A42
Mechanical Key			
B43	GND	GND	A43
B44	PETn8	PERn8	A44
B45	PETp8	PERp8	A45
B46	GND	GND	A46
B47	PETn9	PERn9	A47
B48	PETp9	PERp9	A48
B49	GND	GND	A49
B50	PETn10	PERn10	A50
B51	PETp10	PERp10	A51
B52	GND	GND	A52
B53	PETn11	PERn11	A53
B54	PETp11	PERp11	A54
B55	GND	GND	A55
B56	PETn12	PERn12	A56
B57	PETp12	PERp12	A57
B58	GND	GND	A58
B59	PETn13	PERn13	A59
B60	PETp13	PERp13	A60
B61	GND	GND	A61
B62	PETn14	PERn14	A62
B63	PETp14	PERp14	A63
B64	GND	GND	A64
B65	PETn15	PERn15	A65
B66	PETp15	PERp15	A66
B67	GND	GND	A67
B68	RFU1, N/C	USB_DAT0n	A68
B69	RFU2, N/C	USB_DAT0p	A69
B70	PRSNTB3#	PWRBRK0#	A70

Secondary Connector (4C)			
Side B		Side A	
B10	PERST4#	PRSNTA1#	A10
B11	+3.3V_EDGE	PERST5#	A11
B12	AUX_PWR_EN1	PRSNTB6#	A12
B13	GND	GND	A13
B14	REFCLKn4	REFCLKn5	A14
B15	REFCLKp4	REFCLKp5	A15
B16	GND	GND	A16
B17	PETn16	PERn16	A17
B18	PETp16	PERp16	A18
B19	GND	GND	A19
B20	PETn17	PERn17	A20
B21	PETp17	PERp17	A21
B22	GND	GND	A22
B23	PETn18	PERn18	A23
B24	PETp18	PERp18	A24
B25	GND	GND	A25
B26	PETn19	PERn19	A26
B27	PETp19	PERp19	A27
B28	GND	GND	A28
Mechanical Key			
B29	GND	GND	A29
B30	PETn20	PERn20	A30
B31	PETp20	PERp20	A31
B32	GND	GND	A32
B33	PETn21	PERn21	A33
B34	PETp21	PERp21	A34
B35	GND	GND	A35
B36	PETn22	PERn22	A36
B37	PETp22	PERp22	A37
B38	GND	GND	A38
B39	PETn23	PERn23	A39
B40	PETp23	PERp23	A40
B41	GND	GND	A41
B42	PRSNTB4#	PRSNTB5#	A42
Mechanical Key			
B43	GND	GND	A43
B44	PETn24	PERn24	A44
B45	PETp24	PERp24	A45
B46	GND	GND	A46
B47	PETn25	PERn25	A47
B48	PETp25	PERp25	A48
B49	GND	GND	A49
B50	PETn26	PERn26	A50
B51	PETp26	PERp26	A51
B52	GND	GND	A52
B53	PETn27	PERn27	A53
B54	PETp27	PERp27	A54
B55	GND	GND	A55
B56	PETn28	PERn28	A56
B57	PETp28	PERp28	A57
B58	GND	GND	A58
B59	PETn29	PERn29	A59
B60	PETp29	PERp29	A60
B61	GND	GND	A61
B62	PETn30	PERn30	A62
B63	PETp30	PERp30	A63
B64	GND	GND	A64
B65	PETn31	PERn31	A65
B66	PETp31	PERp31	A66
B67	GND	GND	A67
B68	RFU3, N/C	UART_RX	A68
B69	RFU4, N/C	UART_TX	A69
B70	PRSNTB7#	PWRBRK1#	A70

9.3.2 Signal Descriptions

Where applicable, the LFF specific signal descriptions were moved into this section. A full description of all the card edge signals is described in Section 4.5. This section is not intended to replicate all of the pins that are common between the SFF/DSFF and the LFF. Any discrepancies between this version of the specification and version 1.3.0 (the last version of the spec supporting LFF) shall be reconciled by referring to version 1.3.0.

In general, the following rules apply:

- LFF implementations shall follow the 4C+ Primary and 4C Secondary Connector descriptions. The LFF Secondary Connector is limited to PERST[4:5]# and REFCLK[4:5].
- REFCLK[4:5] are available on the Secondary Connector for the LFF, but are not defined for use in the LFF definition.
- PERST[4:5] are available on the Secondary Connector for the LFF, but are also not defined for use in the LFF definition.
- The PERST direction is always an output from the baseboard for an LFF.
- UART is only defined on the 4C secondary connector for LFF.

9.3.3 UART (A68/A69) – LFF Secondary Connector Only

This section provides the pin assignments for the UART interface signals. UART is only defined for operation on the Secondary Connector for the LFF. It is not applicable to the SFF or the DSFF implementations. The UART pins may be used with end point silicon that require console redirection over the baseboard – such as LFF SmartNICs. An example connection diagram is shown in Figure 196.

Table 88: Pin Descriptions – UART – LFF Secondary Connector Only

Signal Name	Pin #	Baseboard Direction	Signal Description
UART_RX	A68	Input	UART Receive. +3.3 V signaling levels. LFF Secondary Connector Only.
UART_TX	A69	Output	UART Transmit. +3.3 V signaling levels. LFF Secondary Connector Only.

9.3.3.1 UART_RX

A baseboard implementation shall provide a UART receive connection from the OCP NIC 3.0 connector. The UART_RX pin shall be pulled up to +3.3 VAUX on the baseboard to prevent erroneous data reception when the OCP NIC 3.0 card is powered off or not present.

NIC implementations that require a UART shall connect the network silicon UART_RX pin to the UART_TX pin on the OCP NIC 3.0 connector. This pin shall be left as a no connect if it is not used on the OCP NIC 3.0 card.

The UART_RX pin shall be buffered on the NIC to prevent a leakage path into unpowered silicon when the card is in ID Mode. The buffer may be controlled via a local “Power Good” indicator.

9.3.3.2 UART_TX

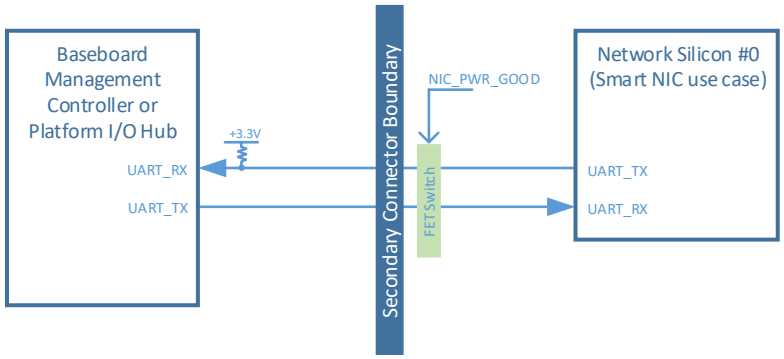
A baseboard implementation shall provide a UART transmit connection to the OCP NIC 3.0 connector.

NIC implementations that require a UART shall connect the UART_TX pin from the OCP NIC 3.0 connector to the target silicon UART_RX pin. This pin shall be left as a no connect if it is not used on the OCP NIC 3.0 card.

The UART_TX pin shall be buffered on the NIC to prevent a leakage path into unpowered silicon when the card is in ID Mode. The buffer may be controlled via a local “Power Good” indicator.

9.3.3.3 UART Example Topology

Figure 196: UART Connection Example (LFF Secondary Connector only)



9.3.4 PCIe Pins for LFF

9.3.4.1 LFF PRSNTA[1:0]#, PRSNTB[7:0]#

For an LFF card, the card side PRSNTA0# pin shall connect to one or more of the PRSNTB[3:0]# pins, and PRSNTA1# shall connect to one or more of the PRSNTB[7:4]# pins according to the bifurcation decoder defined in Section 4.6.3. The connections shall match the card PCIe link subdivision capabilities.

For an LFF slot, the baseboard shall read the PRSNTB[3:0]# pins associated with the Primary Connector, and read the PRSNTB[7:4]# pins associated with the Secondary Connector. The default state of PRSNTB[3:0]#==0b1111 and PRSNTB[7:4]#==0b1111 indicates that no card is present in the card slot. A value other than PRSNTB[7:0]#==0b1111_1111 indicates that a card is present. The Baseboard shall use the look up table defined in Section 4.6.3 to determine the supported card PCIe link subdivisions.

The condition where the Primary Connector PRSNTB[3:0]# equals 0b1111 and the Secondary Connector PRSNTB[3:0]# pins is not equal to 0b1111 is invalid for LFF.

9.3.4.2 LFF BIF[5:0]#

For an LFF card that supports bifurcation, the card shall use the BIF[2:0]# pins from the Primary connector and BIF[5:3]# pins from the Secondary Connector according to the bifurcation decoder defined in Section 4.6.3. The BIF encoding values shall match the card PCIe link subdivision capabilities.

For an LFF slot, the baseboard may assert the appropriate BIF pin encoding to obtain the requested bifurcation mode associated with the Primary Connector and Secondary Connectors. The Baseboard shall use the look up table defined in Section 4.6.3 to determine the supported card PCIe link subdivisions. Asserting invalid BIF values may result in undefined behavior.

9.3.4.3 PCIe REFCLK and PERST# Mapping – LFF

Although REFCLK[4:5] and PERST[4:5]# are pinned out in the LFF, these signals are not currently defined for use. For a LFF 8 link scenario, the lower x4 "link-a" and upper x4 "link-b" of each x8 lanes are expected to use the same REFCLK and PERST (see Table 89). A 1:2 clock driver circuit is expected on the OCP NIC 3.0 card in this case.

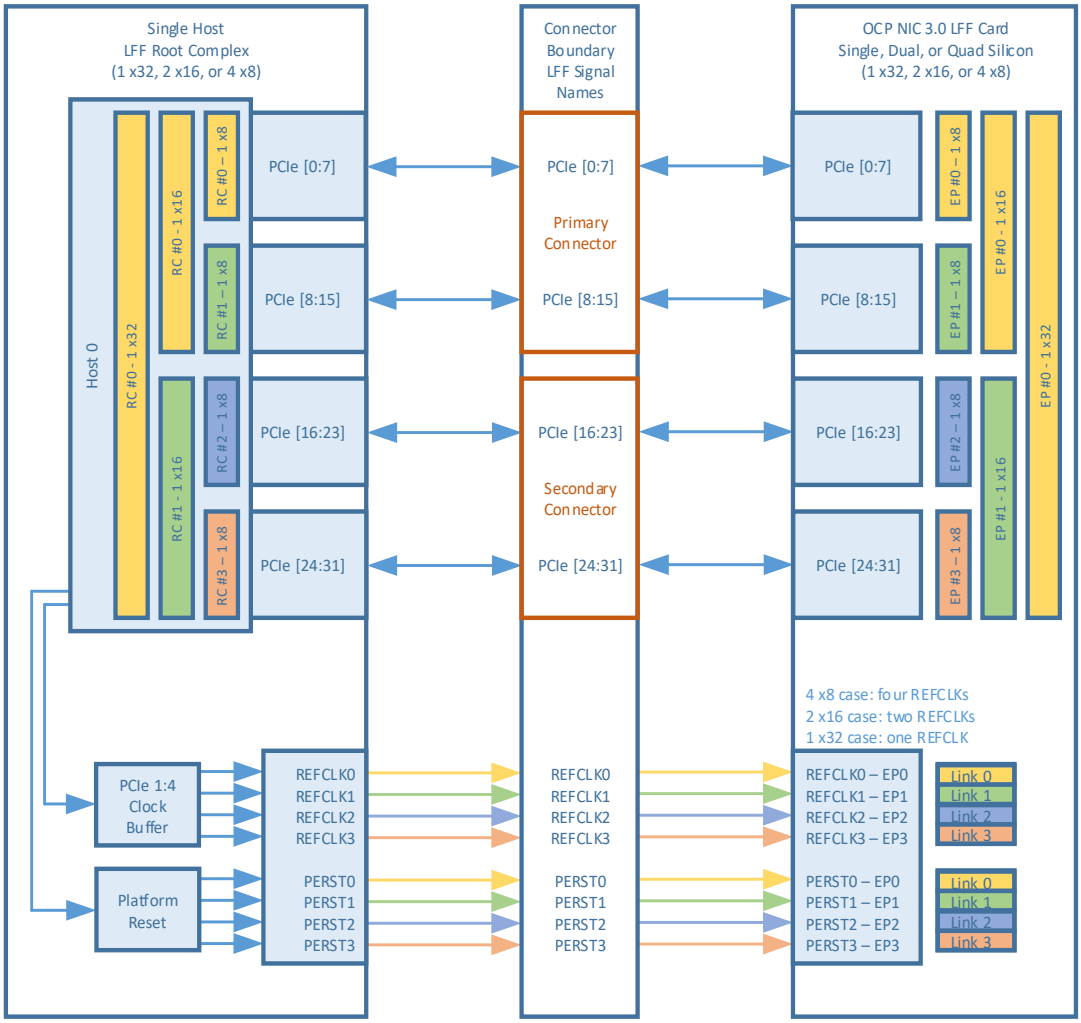
Table 89: LFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2, 4 and 8 Links

<table>
<tr><th colspan="4">Primary Connector</th><th colspan="4">Secondary Connector</th></tr>
<tr><th>Lanes [0:3]</th><th>Lanes [4:7]</th><th>Lanes [8:11]</th><th>Lanes [12:15]</th><th>Lanes [16:19]</th><th>Lanes [20:23]</th><th>Lanes [24:27]</th><th>Lanes [28:31]</th></tr>
<tr><td colspan="8">Link 0 – x32, REFCLK0, PERST0#</td></tr>
<tr><td colspan="4">Link 0 – x16, REFCLK0, PERST0#</td><td colspan="4">Link 2 – x16, REFCLK2, PERST2#</td></tr>
<tr><td colspan="2">Link 0 – x8, REFCLK0, PERST0#</td><td colspan="2">Link 1 – x8, REFCLK1, PERST1#</td><td colspan="2">Link 2 – x8, REFCLK2, PERST2#</td><td colspan="2">Link 3 – x8 REFCLK3, PERST3#</td></tr>
<tr><td>Link 0a – x4, REFCLK0, PERST0#</td><td>Link 0b – x4, REFCLK0, PERST0#</td><td>Link 1a – x4, REFCLK1, PERST1#</td><td>Link 1b – x4, REFCLK1, PERST1#</td><td>Link 2a – x4, REFCLK2, PERST2#</td><td>Link 2b – x4, REFCLK2, PERST2#</td><td>Link 3a – x4, REFCLK3, PERST3#</td><td>Link 3b – x4, REFCLK3, PERST3#</td></tr>
</table>

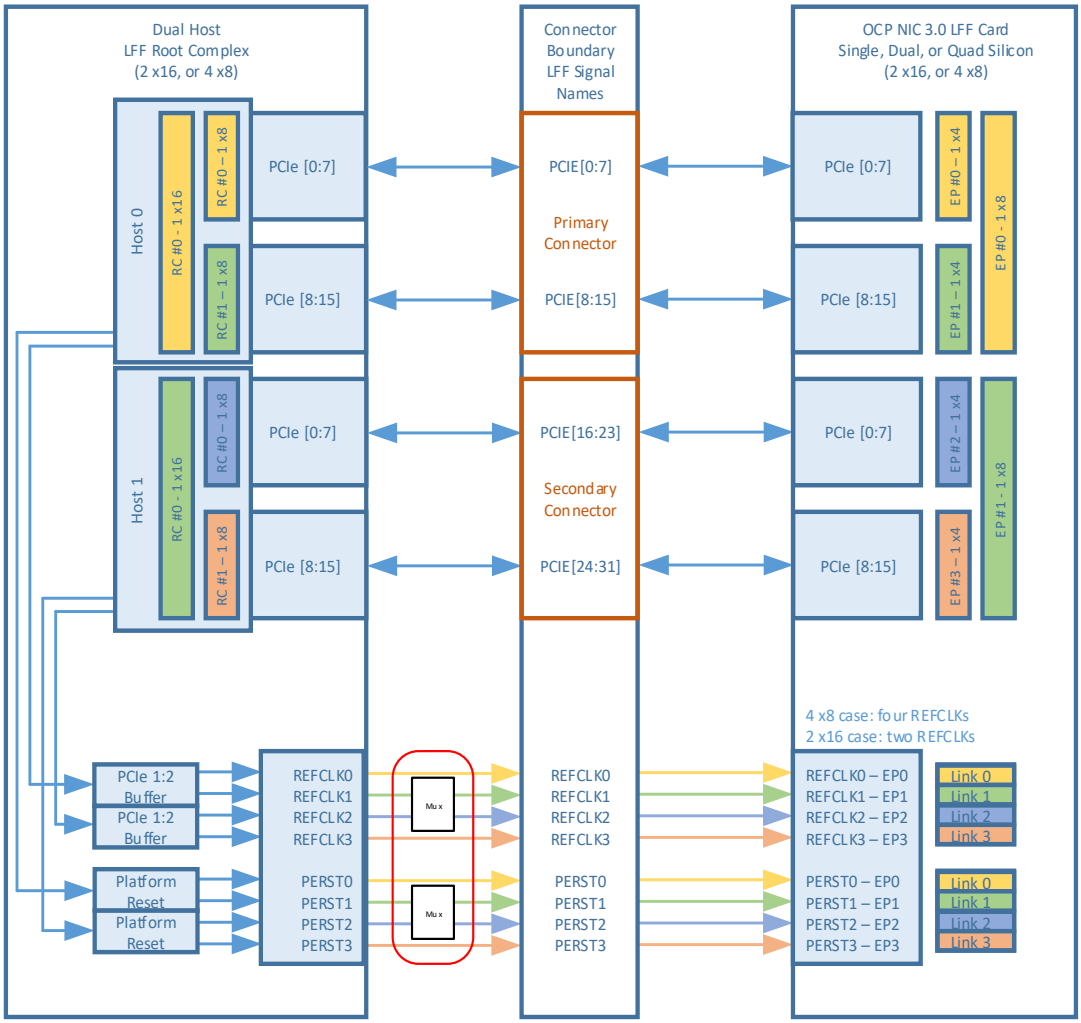
9.3.4.4 LFF PCIe REFCLK and PERST# Mapping

The following figures show the Link n, REFCLKn, PERSTn mapping for the LFF with 1, 2 and 4 links as single, dual and quad host configurations. For clarity, the PCIe sideband signals are not illustrated this section. Please refer to the signal descriptions and associated diagrams for connectivity requirements.

Figure 197: LFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links



5008 Figure 198: LFF PCIe REFCLK Mapping – Dual Host – 2 and 4 links

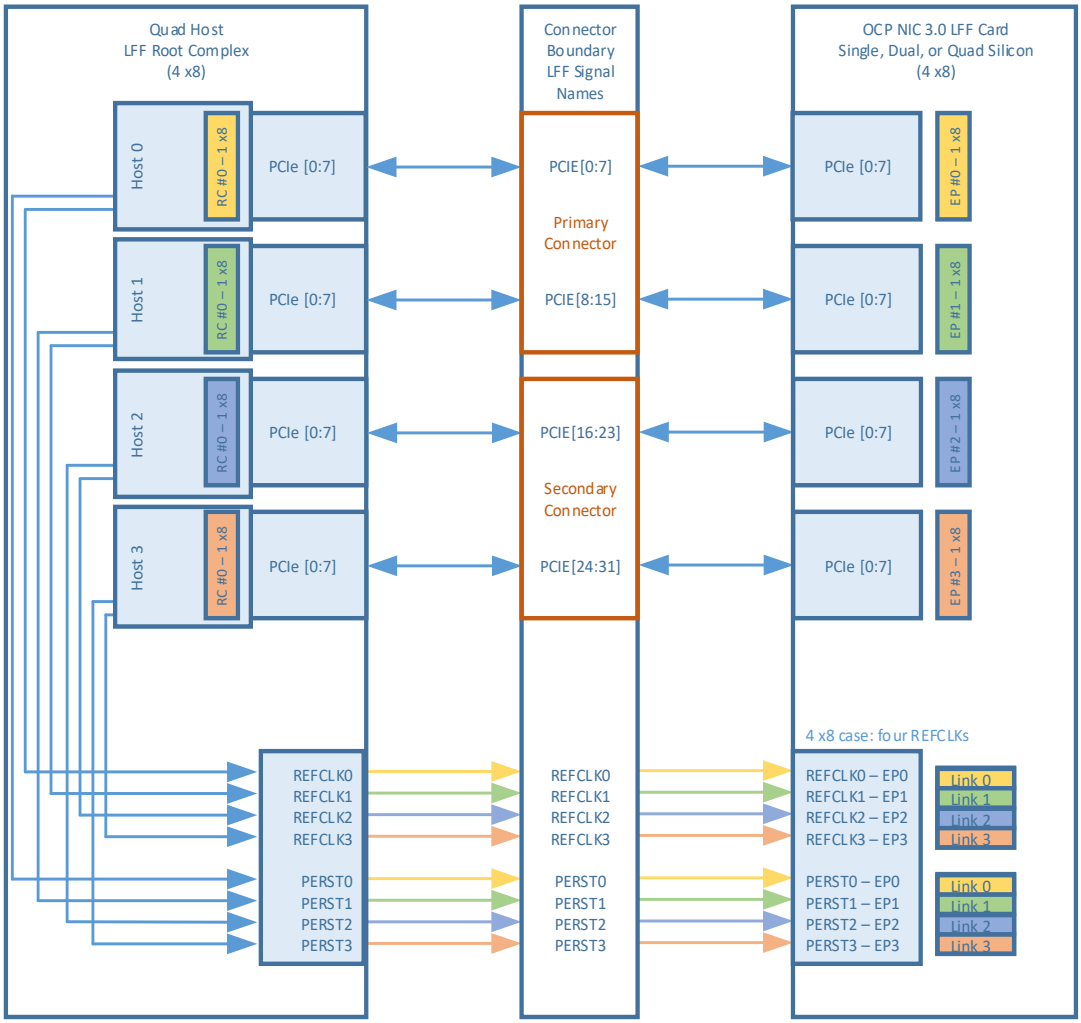


5009
5010

Note: For dual host applications that connect to a two link endpoint, the baseboard Host 1 REFCLK0 and PERST0 signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

5011

5012 Figure 199: LFF PCIe REFCLK Mapping – Quad Host – 4 Links



5013
5014

Note: For quad host applications that connect to a two link endpoint, the baseboard Host 2 REFCLK and PERST signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

5015
5016

9.3.5 Power Supply Rail Requirements and Slot Power Envelopes for LFF

The following table details out the LFF slot power envelopes. Refer to Section 4.10 for the table notes in superscript.

Table 90: Baseboard Power Supply Rail Requirements – LFF Slot Power Envelopes

Power Rail	150 W LFF Slot
+3.3V_EDGE	
Voltage Tolerance	±9%
Max Supply Current	
ID Mode	100 mA
Programming Mode	100 mA
Aux Power Mode	2.2 A
Main Power Mode	2.2 A
Max Capacitive Load	300 µF
+12V_EDGE	
Voltage Tolerance	+8/-12%
Max Supply Current	
ID Mode[5]	50 mA
Programming Mode[5]	50 mA
Aux Power Mode	6.3 A
Main Power Mode	12.5 A
Max Capacitive Load[3]	2000 µF

9.4 Signal Integrity Considerations – NC-SI over RBT – LFF

9.4.1 LFF Baseboard Requirements

The LFF baseboard is allocated a maximum propagation time of 1650 ps between the BMC and the connector edge. NC-SI over RBT isolation buffers are required on the baseboard. The requirements for additional add-in card loading are reduced. The available timing budget for the LFF/DSFF baseboard is computed by the formula below.

$$T_{BASEBOARD,LFF} = 1650\ ps - T_{RBT_ISOLATOR} - T_{CONNECTOR}$$

Similar to the SFF implementation, the LFF clock skew parameter $T_{SKEW(max)}$ must not be exceeded. The max permissible value of L3 is $T_{NIC,LFF}$ = 1350 ps. Refer to Section 6.1.1 for the skew computation requirements.

9.4.2 LFF OCP NIC 3.0 Card Requirements

Similar to the SFF, a LFF OCP NIC 3.0 Card is allocated a maximum propagation time of $T_{NIC,LFF}$ = 1350 ps between the card gold finger and the ASIC pad for both the clock and data signals. The segment L3 between the LFF OCP NIC 3.0 card gold fingers and the ASIC shall not exceed this propagation delay for single and multi-ASIC target implementations. Refer to Section 6.1.2 for computation and topology considerations.

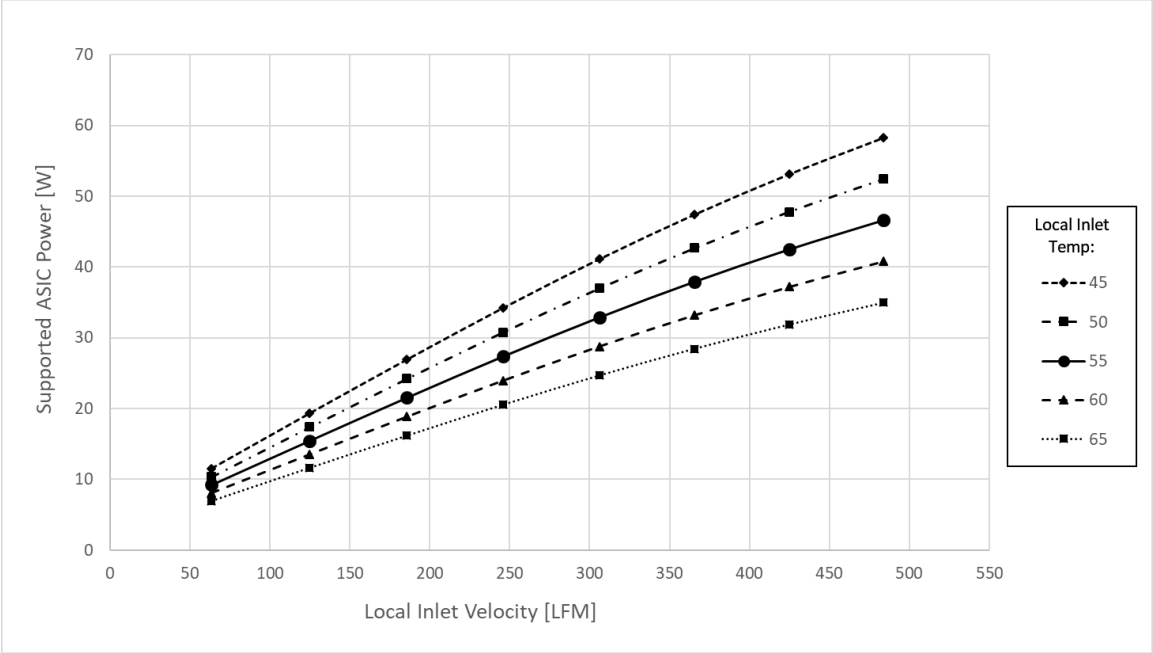
9.5 Thermal and Environmental – LFF

9.5.1 Thermal Design Guidelines – LFF

9.5.1.1 LFF Card ASIC Cooling – Hot Aisle

Figure 200 below provides an estimate of the maximum ASIC power that can be supported as a function of the local inlet velocity for the LFF card in a hot aisle cooling configuration. Each curve in Figure 200 represents a different local inlet air temperature from 45 °C to 65 °C.

Figure 200: ASIC Supportable Power for Hot Aisle Cooling – LFF Card



The curves shown in Figure 201 were obtained using CFD analysis of the reference OCP NIC 3.0 LFF card. The reference card has a 45 mm x 45 mm ASIC with two QSFP connectors. Additional card geometry parameters and boundary conditions used in the reference CFD analysis are summarized in Table 91. Figure 201 shows a comparison of the 3D CAD and CFD model geometry for the reference OCP NIC 3.0 card.

Figure 201: OCP NIC 3.0 LFF Reference Design and CFD Geometry

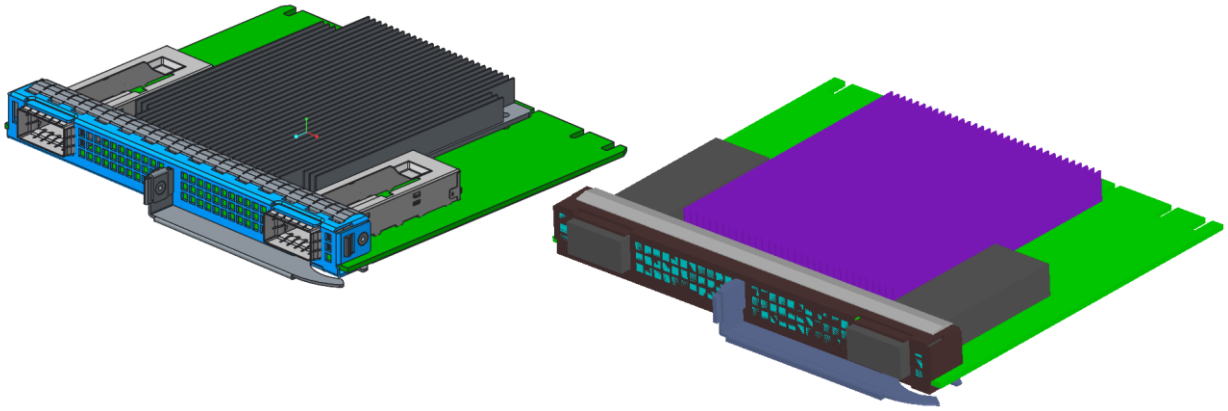


Table 91: Reference OCP NIC 3.0 LFF Card Geometry

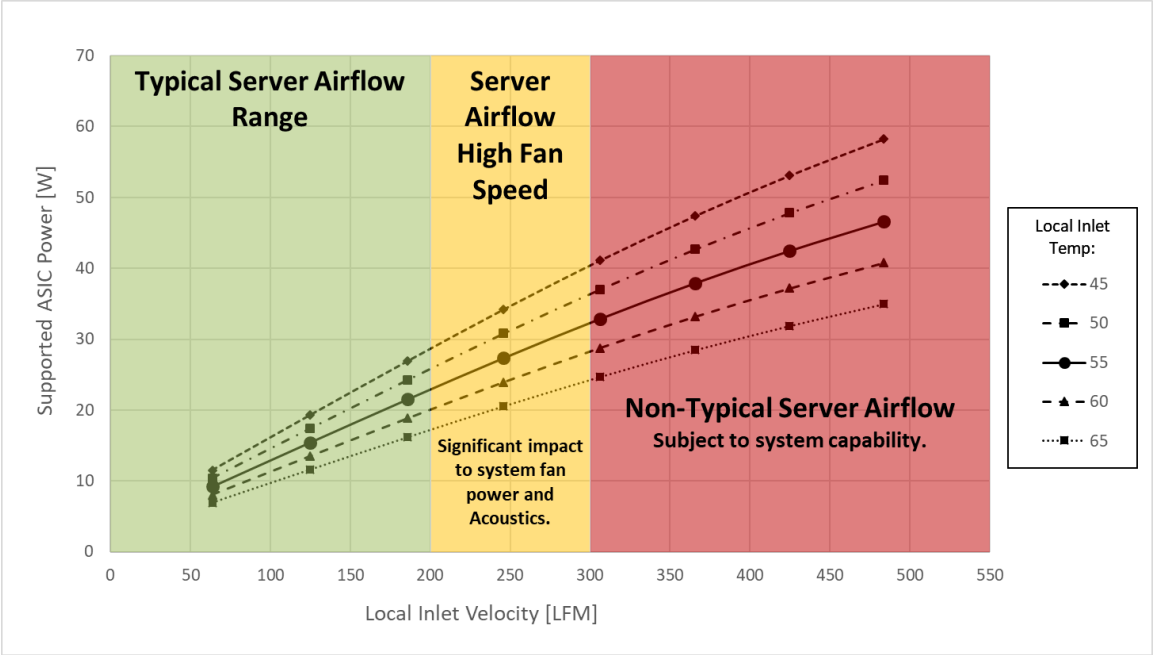
OCP NIC 3.0 Form Factor	LFF Card
Heatsink Width	75 mm
Heatsink Length	85 mm
Heatsink Height	9.3 mm
Heatsink Base Thickness	1.5 mm
Fin Count/Thickness	33/0.5 mm
Heatsink Material	Extruded Aluminum
ASIC Width	45
ASIC Length	45
ASIC Height	2.13
ASIC Theta-JC	0.17 C/W
ASIC Theta-JB	10 C/W
OCP PCB In-Plane Conductivity	34 W/mK
OCP PCB Normal Conductivity	0.33 W/mK
ASIC T-case Max	95 °C
OCP NIC 3.0 I/O Connectors	Two QSFP @ 3.5 W each

It is important to note that the supportable power for the LFF card is considerably higher than for the SFF card due to the increased size of the ASIC heatsink. In addition, optics module cooling on the LFF card will also be considerably improved due to the arrangement of the optics in parallel to the ASIC heatsink rather than in series. These thermal advantages are key drivers for the LFF card geometry. The OCP NIC 3.0 simulation was conducted within a virtual version of the LFF card test fixture defined in Section 7.4. In addition, OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 5.10.3.

Figure 202 below shows the LFF ASIC supportable power curves with an overlay of three server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the

server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions.

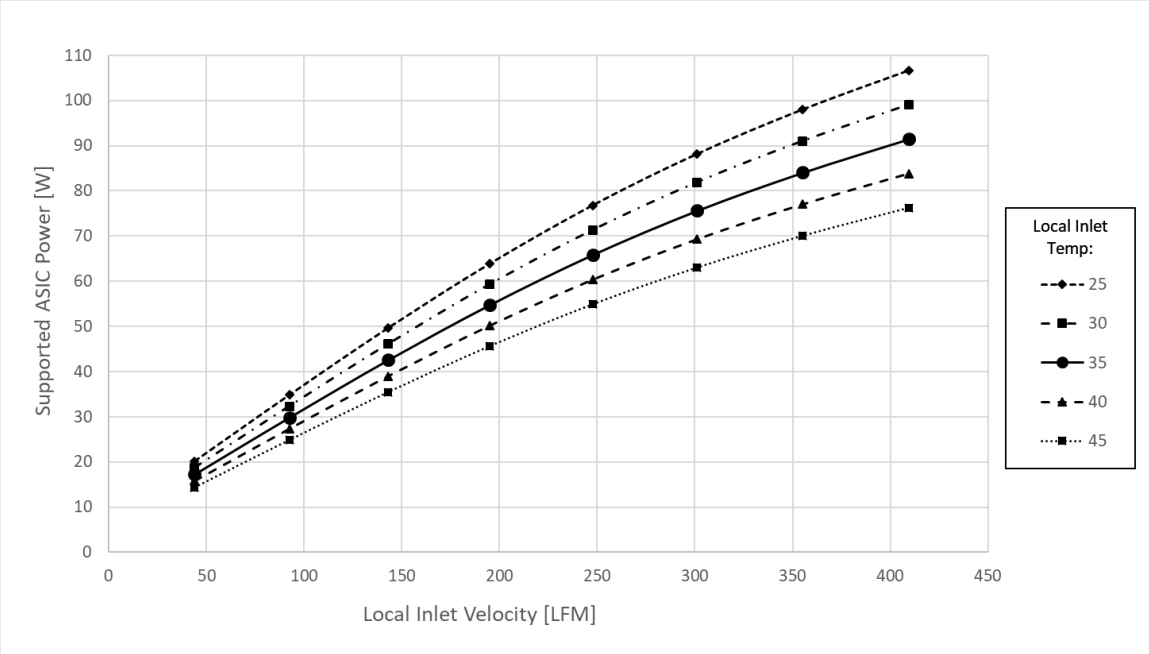
Figure 202: Server System Airflow Capability – LFF Card Hot Aisle Cooling



9.5.1.2 LFF Card ASIC Cooling – Cold Aisle

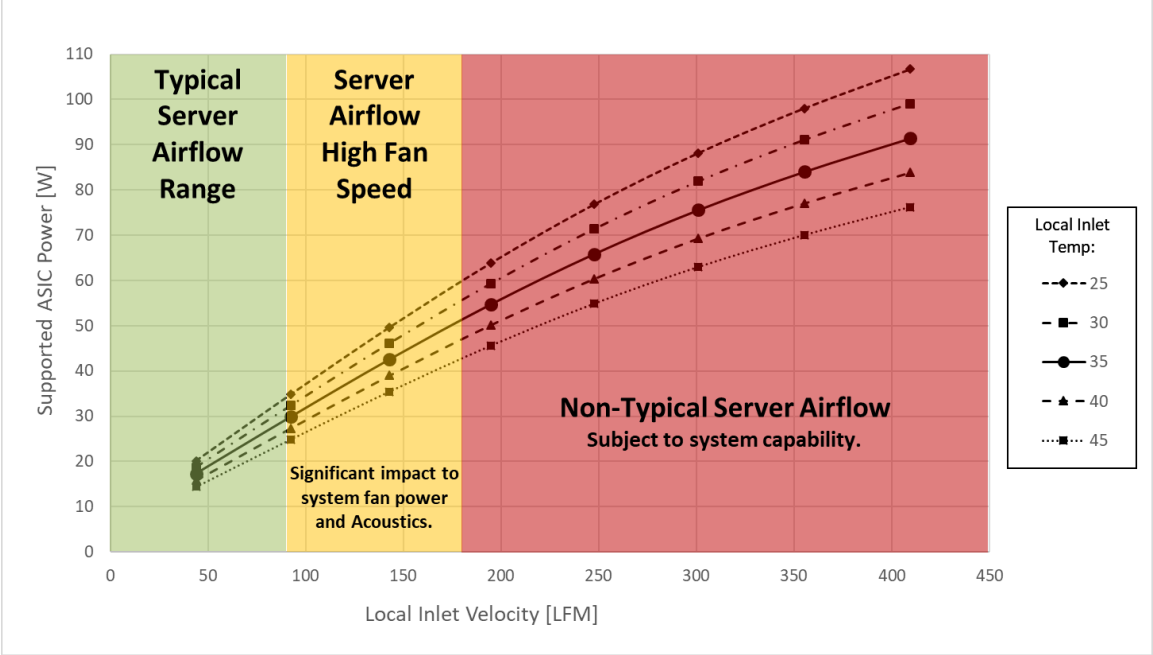
The ASIC cooling analysis for the LFF card in Cold Aisle configuration was conducted utilizing the same geometry and boundary conditions described in Section 7.2.5 with airflow moving from I/O connector to ASIC (opposite to the Hot Aisle analysis). Figure 203 below shows the results of this analysis for the Cold Aisle cooling configuration. Each curve in Figure 203 represents a different system inlet air temperature from 25 °C to 45 °C.

Figure 203: ASIC Supportable Power for Cold Aisle Cooling – LFF Card



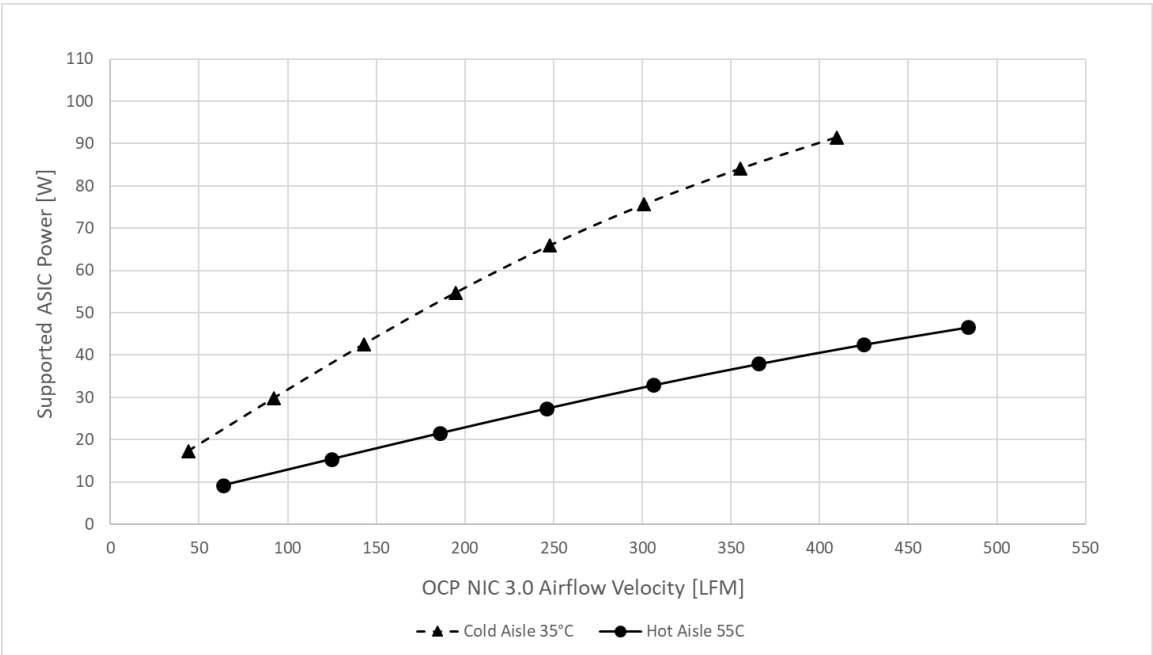
Similar to Figure 151 for LFF Hot Aisle cooling, Figure 204 below shows the LFF ASIC supportable power curves with an overlay of three Cold Aisle server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable Cold Aisle system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Similar to the Hot Aisle cases, cooling of the optical transceivers need to be taken into consideration even though they are not preheated by the ASIC in the Cold Aisle case. OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 5.10.3. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions for both Hot and Cold Aisle cooling.

Figure 204: Server System Airflow Capability – LFF Cold Aisle Cooling



A comparison of Hot Aisle (55 °C) and Cold Aisle (35 °C) LFF ASIC cooling capability curves is shown below in Figure 205. The comparison shows the Hot Aisle ASIC cooling capability at 19 W at 150 LFM while the cold Aisle cooling capability shows support for 42 W at 150 LFM. In general, based on the reference geometry, the Cold Aisle cooling configuration allows for higher supported ASIC power at lower velocities due primarily to the lower inlet temperatures local to the OCP NIC 3.0 card when in the Cold Aisle cooling configuration.

Figure 205: ASIC Supportable Power Comparison – LFF Card



9.5.2 Test Fixture for LFF Card

Images of the LFF thermal test fixture are shown in Figure 206 and Figure 207. The LFF fixture PCB is shown in Figure 208. Note the three candlestick sensor locations directly next to the OCP NIC 3.0 connectors.

Figure 206: LFF Card Thermal Test Fixture Design

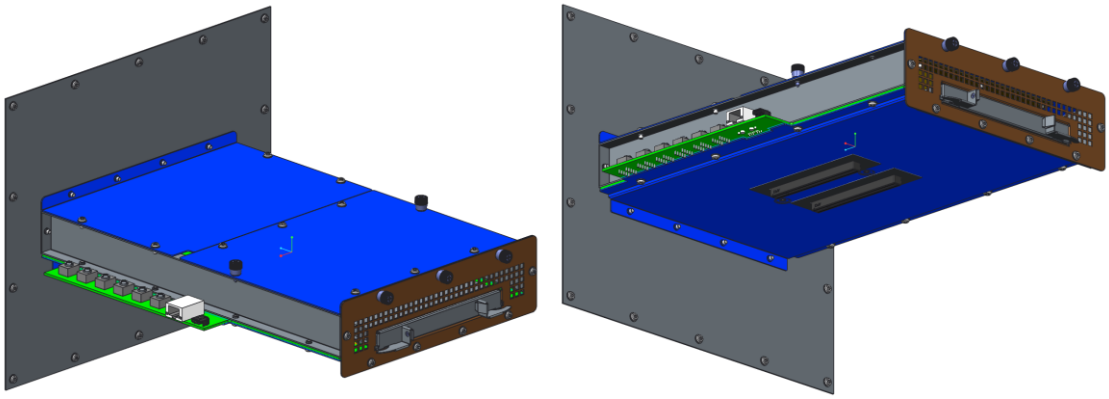


Figure 207: LFF Card Thermal Test Fixture Design – Cover Removed

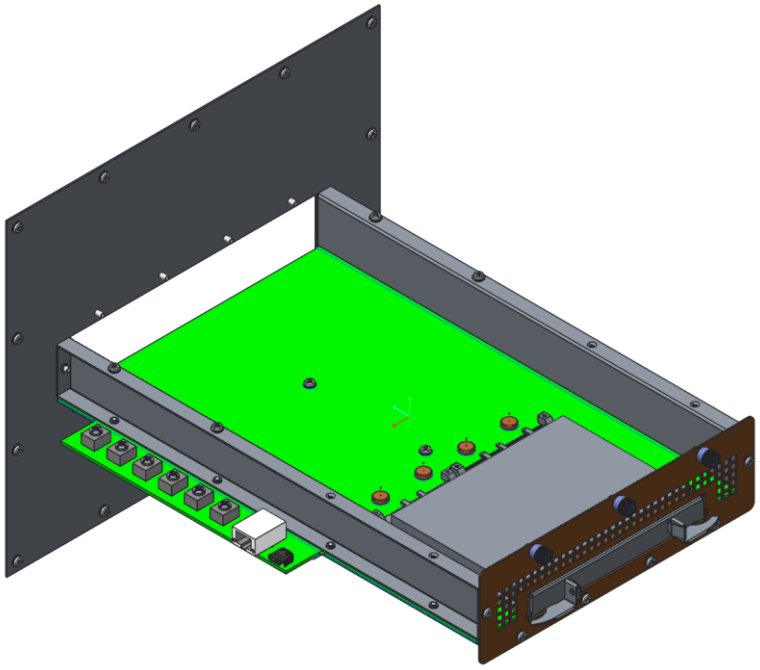
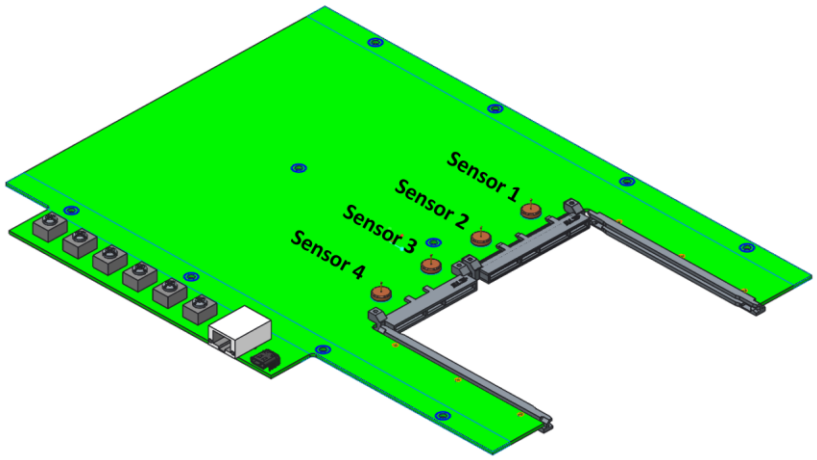
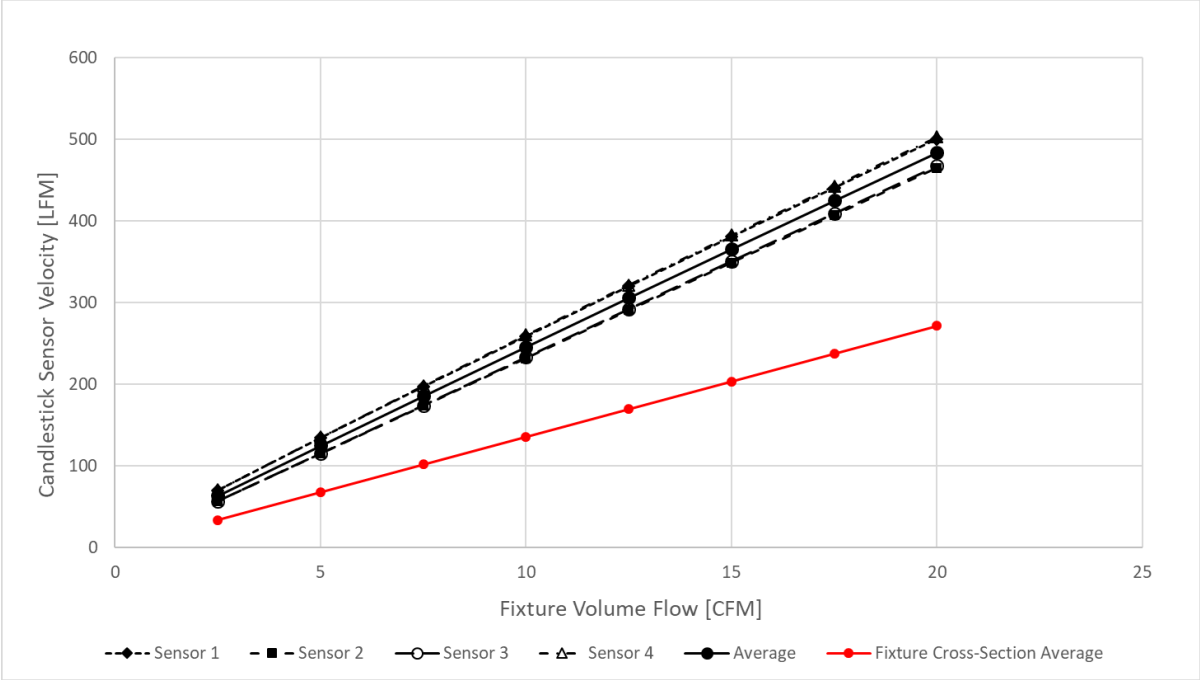


Figure 208: LFF Card Thermal Test Fixture PCB



9.5.3 Thermal Test Fixture Candlestick Sensors – LFF

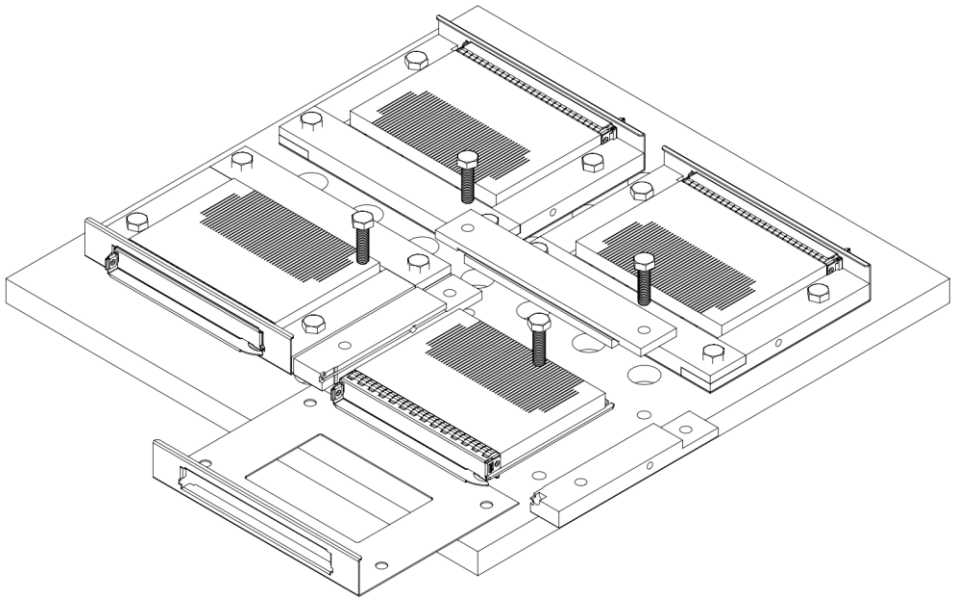
Figure 209: LFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow



9.5.4 Shock and Vibe Fixture – LFF

The following figure shows the LFF shock and vibe fixture. For details, refer to the procedure and fixture usage in Section 7.7.

Figure 210: LFF Shock and Vibe Fixture



10 Revision History

10.1 Document Revision History

Revision	Date	Change Description
0.70	01/25/2018	Initial public review.
0.71	02/06/2018	- Implemented comments from 0.70 review. - LED implementation updated. - Gold finger lengths updated. All pins are full length except for PCIe TX/RX, REFCLKS and PRSNT pins.
0.72	02/21/2018	- Updates to Section 4.x per the working group session.
0.73	05/01/2018	- Change NC-SI over RBT RXD/TXD pins to a pull-up instead of a pull down. - Update power sequencing diagram. REFCLK is disabled before silicon transitions to Aux Power Mode. - Merge pinout sections 3.4 and 3.5 together for structural clarity. - Add text to gate WAKE# signal on AUX_PWR_GOOD (internal) assertion; updated diagrams with WAKE# signals to reflect implementation. - Add initial signal integrity outline to document (WIP) - Add Initial draft of the Shock and Vibration, and Dye and Pull test requirements. - Rearrange Section 2 for structure; changed section name to Mechanical Card Form Factor - Move non-NIC use cases to Section 1.5. - Moved Port numbering and LED definitions to Section 3.8. - Add secondary side LED placement for 4x SFP and 2x QSFP implementations in Section 3.8. - Revised labeling section (Section 2.9). - Optimize the scan chain LED bit stream for dual port applications. - Add SLOT_ID[1]. Updated text and diagrams for mapping SLOT_ID[1:0] to Package ID[2:0] and FRU EEPROM A[2:0] fields. - Reduce ID Mode power consumption on +12V_EDGE
0.74	06/04/2018	- Text clean up. All minor / generally agreed upon items within the OCP NIC 3.0 Workgroup have been accepted. - Clarify PCIe bifurcation is on a per-slot basis. Add 1x32 and 2x16 implementation examples for a Large Form Factor card. - Removed reference to a x24 PCIe width LFF card from Table 5 – OCP NIC 3.0 Card Definitions. - Move SLOT_ID[1] to OCP_A6 for immediate power on indication of the card physical location for RBT and FRU EEPROM addressing. Updated RBT addressing and Scan Chain definition to match. - Updated diagrams and text in Section 6.x based on feedback from the OCP NIC 3.0 Thermal Workgroup. - Updated diagrams and text in Section 2.0 based on feedback received from the OCP NIC 3.0 Mechanical Workgroup.
0.80	06/04/2018	0v80 public release
0.81	07/06/2018	0v81 public release. Changes are as follows: - Section 1.3 – Update Figure 1 with latest thumbscrew design. - Section 2.4.2 – Mechanical corrections to BOM items 5, 6A/B, 8 & 11. - Section 3.4.3 – Add statement to isolate SMRST# if target device voltage is not powered from +3.3V_EDGE. - Section 3.4.4 – Clarified the RBT_ARB_IN and RBT_ARB_OUT pin descriptions. - Section 3.4.4 – Clarified SLOT_ID[1:0] description and example diagrams; move SLOT_ID[1:0] isolation to NIC and use direct connection to FRU EEPROM. - Section 3.4.5 – DATA_IN bit PRSNTB[3:0] definition to optionally use pull up/down to match PRSNTB[3:0]# card edge connections. - Section 3.4.7 – Add USB 2.0 definition to the Primary Connector.

Revision	Date	Change Description
		- Section 3.4.8 – Add UART definition to the Secondary Connector. - Section 3.4.9 – Changed Miscellaneous pins to RFU[1:2] pins. - Section 3.8 – Clarified LED placement. - Section 3.9.x – Clarified ID-Aux and Aux-Main Power Mode transition requirements to prevent sampling health status pins until cards have fully entered into Aux and Main Power Modes to prevent false indication. - Section 3.11 – Updated hot swap consideration text to highlight available hot swap mechanisms. Actual hot swap design is outside the scope of this specification. - Section 4 – Update MCTP Type management description. - Section 4.9 – Clarified the FRU EEPROM is directly connected to the card edge. No isolation is used for the FRU EEPROM.
0.82	08/03/2018	- Minor editorial changes. - Changed names to “SFF” and “LFF” when referencing the two board form factors for uniformity. - Section 3.4.1 – Changed PERST[3:0]# to be asserted low until the platform is ready to bring cards out of reset. - Section 3.5.3 – Corrected typos in the PCIe Bifurcation Decoder (Table 31) for hosts that implement 4 x2 links on the first 8 lanes when using a 4 x4 OCP NIC 3.0 card. - Section 3.5.5.3 & 3.5.5.4 – Corrected the BIF[2:0] values in the diagrams. - Section 3.7 – Corrected typos in the PCIe Bifurcation result and REFCLK mapping (Table 38 and Table 41) for single host/quad host cases with PCIe on the first 8 lanes. This change was due to propagating corrections from Table 31 from Section 3.5.3. - Section 3.8.3 – Changed faceplate LED placement for 2xQSFP to primary side. - Section 4.10.2 – Added FRU field to identify the card manageability type.
0.83	08/29/2018	- Section 5.3.4 – Removed subheadings for the PCIe test methodology. Replaced with reference text to the PCIe test specifications.
0.84	11/13/2018	- Editorial changes. - Add appropriate trademarks per entity usage guidelines - Section 1.x – Reorganized section, added list of acronyms. - Section 1.5, 2.x – Mechanical updates from ME team. Updates to Vendor PN, pull tab/thumbscrew color. - Section 3.1.x – Add card edge gold finger Detail D and profile dimensions. - Section 3.1.1 – Change gold finger lengths to align with SFF-TA-1002 and SFF-TA-1009. All ground pins mate first; power, single ended and differential pairs mate second. - Section 3.4.1, Section 3.5.x – Updated for LFF and applications with 32 lanes of PCIe. Included TX/RX lane indices for lanes[16:31], REFCLK[4:5], PERST[4:5]# and PWRBRK1 on the Secondary Connector. - Section 3.4.2 – Clarified BIF[2:0]# assertion timing. - Section 3.4.4 – Clarified RBT isolation state with respect to AUX_PWR_EN and NIC_PWR_GOOD assertion. - Section 3.4.5 – Clarified that the scan chain shift registers may also be implemented with a CPLD as long as the logic is equivalent. Clarified the FAN_ON_AUX bit. - Section 3.4.9 – Changed RFU[1:2] to RFU[3:4] for the Secondary Connector. - Section 3.7 – Removed bifurcation expansion tables. Redirected readers to the pinout/bifurcation spreadsheet on the OCP Mezz Wiki site instead. - Section 3.6 and Section 3.7 – Merged together as they both discuss PCIE REFCLK mapping. Add new diagrams depicting single, dual and quad host implementations with 1, 2, and 4 links. Diagrams show association of the link to the REFCLK and PERST signals. Update bifurcation table color codes to differentiate SFF (2C+ / 4C+) implementations from LFF implementations. - Section 3.11 – Add RBT_ISOLATE# to the power up/down sequencing diagrams. Changed BIF[2:0]# pins to ‘low’ state when AUX_PWR_EN is deasserted. Add timing value “T4” from DSP0222 to power up diagram and sequencing parameters table. Add T_{CYCLE_SFF} / T_{CYCLE_LFF} parameters to power down sequencing to prevent a pre-biased output condition when power cycling cards. - Section 4.4 – Clarified requirements for self-shutdown if the optional feature is implemented on the card.

Revision	Date	Change Description
		- Section 4.9 – Cleaned up SMBus 2.0 Address Map text. Add text to discourage the use of unsolicited SMBus messages including the optional 'Notify ARP Controller' command. - Section 4.10.2 – Clarified FRU data format requirements per the IPMI Platform Management FRU Information Storage Definition. List minimum FRU content requirements. - Section 5.1.x – Clarified NC-SI over RBT physical routing and length matching requirements. - Section 7.1.4 – Corrected typo on NEBS air discharge value for ESD testing. Changed from 16 kV to 15 kV.
0.85	11/20/2018	November release with all 0.84 subgroup changes
0.85b	12/14/2018	- December Hot fix release. Minor text corrections and clarifications. - Section 2.4.2 – Update faceplate and ejector handle drawing filenames - Sections 2.4.3, 2.4.4, and 2.7.x – Mechanical drawing updates. Fixed typos and updated critical dimension text. - Section 2.8.x – Mechanical drawing updates. Changed bottom of PCB datum from H to J. - Section 3.4.5 – Clarified the default scan chain pin states for TEMP_WARN_N, TEMP_CRIT_N and FAN_ON_AUX when temperature reporting is not required. - Section 3.4.7 – Clarified USB text on differential signaling voltage, termination voltage and V_{BUS} detection indication. Updated USB figures to include V_{BUS} and V_{BUS} detection inputs. - Section 3.8 – Updated power state machine. +12V_EDGE clarified as being "on, but limited up to the ID Mode budget." This clarification aligns with the existing text. Added clarification notes to Table 37 for permissible +12V_EDGE current draw in the ID Mode and Aux Power Mode states.
0.86	04/02/2019	- Section 1.2 – Change Cavium entity name to Marvell Semiconductor, Inc. - Section 1.3 – Added DSP0267 reference - Sections 1.5, 2.1.x – All 3D renderings have been updated - Section 2.4.2 – Mechanical BOM updated. Added notes for Phillips + Torx screw heads. - Sections 2.4.3, 2.4.4, 2.5.x, 2.7.x, 2.8.2 – Mechanical 2D drawings updated. - Section 2.7 – Added insulator note regarding the use of 0.127 mm material for constrained regions; 4x 4mm diameter holes permitted for non-metallic mechanical retention pin cutouts - Section 3.1 – Gold finger figure updated to clarify dimension from center of pad. - Section 3.4.4 – Add note that RBT clock buffers are permitted so long as the card timing budget is not violated. Clarify permitted baseboard and OCP NIC 3.0 side pull up/pull down implementations on SLOT_ID[1:0]. - Sections 3.4.5, 3.7.2 – Scan Chain LED definition updated. Activity LED is OFF when "idle" - Section 3.4.7 – USB figures now shown as a BMC or Platform I/O hub connectivity instead of just the BMC. - Section 3.4.8 – UART figures now shown as a BMC or Platform I/O hub connectivity instead of just the BMC. - Section 3.6 – Clarify REFCLK/PERST mapping for LFF (Table 35). - Section 4.4 – Temperature Reporting clarified as ASIC die temp reporting. Also clarified die temp reporting is independent of the transceiver temp reporting. - Section 4.6 – Transceiver module temperature reporting is always required and is independent of the network ASIC TDP 5W threshold. - Section 4.10.1 – Add double byte FRU EEPROM access diagrams for clarity. FRU EEPROM WP mechanism may optionally be over written in the field to allow for field updates. - Section 5.1 – Re-wrote NC-SI over RBT SI recommendations. Broke up into three sections: common, baseboard, and OCP NIC 3.0 requirements. - Section 5.2 – Reference SMBus and PCIe CEM specifications for SI, routing and signal requirements. - Sections 6.2.x – Add notes to consider airflow requirements in Aux and Main Power Modes for SFF & LFF in Hot & Cold Aisle implementations. - Section 6.7 – Non-operational shock fixture – CAD files on wiki. Updated test procedure requirements.
0.90	06/20/2019	- Section 1.1 – Update OCPHL-P license link due to opencompute.org site restructuring. - Section 1.3 – Update NIST Special Publication 800-193 to May 2018 release - Section 1.3.1 – Add I^2C as a trademark of NXP Semiconductor. - Section 2.1 – Add safety requirement text and cross reference Section 7.1.3.

Revision	Date	Change Description
		- Section 2.1.1 – Add requirement regarding maximum extraction force on heatsink for internal lock implementations. - Section 2.x – Update Mechanical 2D drawings from WG notes - Section 2.7 – Clarify insulator access hole requirements. - Section 3.4.1 – Clarify PWRBRK[0:1]# card pull up resistor value as 95kΩ or larger and must meet the T_{PWRBRK} timing parameter per PCIe CEM. Provided recommended Baseboard value between 4.7 kΩ and 10 kΩ. - Section 3.4.4 – Updated NC-SI over RBT signal list pull down requirements. TX_EN and TXD[1:0] pull downs moved between RBT isolation circuit and OCP NIC 3.0 connector to prevent NIC side signals from floating when RBT_ISOLATE# is asserted. Updated NC-SI diagrams to depict this change. Clarify HW ARB_IN / ARB_OUT ring integrity requirements for baseboards with multiple OCP NIC 3.0 slots. - Section 3.4.6 – Clarify +12V_EDGE and +3.3V_EDGE requirements when AUX_PWR_EN and MAIN_PWR_EN are asserted. - Section 3.4.6, 3.8.x, 3.9, 4.10.1 – Add optional Programming Mode power state. Add state of NIC_PWR_GOOD when in Programming Mode. Update Power state diagram with Programming Mode. - Section 3.5.3 – Bifurcation decoder table updated to align with bifurcation spreadsheet. - Section 3.8 – Rename section from “Power Capacity and Power Delivery” to “Power State Machine.” Add text about Programming Power State. Clarify normal power state flow. - Section 3.11 – Add Programming Mode sequencing diagram detailing transition from ID Mode to Programming Mode and back to ID Mode. - Section 4.10.2 – Move FRU write protection mechanism to a dedicated section heading. - Section 4.10.3 – Modify OEM Record Offsets for supporting FRU write protection, Programming Mode power state, and thermal requirements. Offset 03 – Values now advertise compliance to specification 0v90. Offset 06/07 – Changed Hot/Cold Aisle tier for use with passive cables. Offset 17 – advertise FRU write protection mechanism. Offset 18 – advertise if the Programming Mode Power State is supported. Offset 19/20 – Add Hot/Cold Aisle tier for use with active cables. Offset 21/22 – Add Reference module power and temperature level. Offset 23 – Add reference active cooling fan fail tier requirement. Offset 31 – Defined “controller” as a SMBus connected device in the context of the FRU UDID. - Section 5.1, 5.1.2, 5.1.4 – Add NC-SI over RBT requirements for LFF - Section 6.4 – Update thermal test fixture feature list. - Section 6.6 – Update card cooling tiers. Combined Hot Aisle and Cold Aisle airflow definition. - Section 6.7.2 – Clarified Shock and Vibe testing shall be tested in the order noted in the specification.
0.91	07/24/2019	- Section 2.2 – Clarified line side implementations may be a subset of I/O listed in Table 7. - Section 2.x – Update ejector lever and faceplate to support a clinch nut implementation. Updated Figure 13 & Figure 14 with new ejector lever diagrams Updated Table 9 with updated drawing & clinch nut. Removed bushing and wave washer from BOM. Updated Figures 16, 18 generic I/O plate for ejector clinch nut Updated Figures 19, 20 with Ejector Lever clinch nut updates. Updated Figure 21 with Ejector lock design. Renamed Section 2.4.8 (was Ejector Bushing, now Clinch Nut), Removed Section 2.4.9 (was Ejector Wave washer) - Section 3.4.1, 3.4.3 and 3.4.6 – Clarified the PWRBRK[0:1]#, SMBus and AUX_PWR_EN of SFF and LFF. These pins are defined on both the Primary and Secondary Connectors. SFF and LFF cards shall use the Primary Connector pin. The Secondary Connector pin is reserved for a future use case. - Section 4.3 – Clarified MC MAC address provisioning requirements for multi-host capable cards as the maximum number of supported hosts.

Revision	Date	Change Description
0.92	11/22/2019	- Section 3.2.4 – Figure 77 was inadvertently changed to include an “Option D” straddle mount connector for a host PCB thickness of 0.105”. This was an error and has been removed. - Section 3.4.3 – Add “AUX Power Good (local signal)” to the isolator figure. - Section 3.5.3 – Add implementation note to state baseboard vendors only need to implement PCIe bifurcation options applicable to their topology. - Section 3.10 – Clarified that RBT hot-plug is not supported in DSP0222 version 1.1 and 1.2. This is feature would be dependent on future revisions of the DSP0222 specification. - Section 3.11 – Change the max T_{APL} / T_{MPL} (AUX_PWR_EN to NIC_PWR_GOOD and MAIN_PWR_EN to NIC_PWR_GOOD) parameters from 25ms to 50ms. - Section 4.10.3 – Changed offset three to state “OCP NIC 3.0 card FRU record released with version 0.90”. The same FRU Record field may be used with incremental revisions of the specification. - Section 7.1.2, 7.1.4 – Add text for co-reporting testing for EN 55024 and EN 55035.
0.99	12/18/2019	- Section 2.1.1 – Update max permissible heatsink force applied for internal lock variant. - Section 2.3 – Removed faceplate callout #8 (wave washer), and #11 (no longer used) from the text under Figure 13 and from Table 9. - Section 2.4.3 – Update SFF Generic I/O faceplate – Figures 15-17 - Section 2.4.4 – Update LFF Generic I/O faceplate – Figure 18 - Section 2.4.8 – Update Clinch nut drawings – Figures 22 and 23 - Section 2.5.x – Update Keep Out zone drawings – Figures 24-33 - Section 2.7.1 – Update SFF insulator drawings – Figures 35 and 36 - Section 2.7.2 – Update LFF insulator drawings – Figures 38 and 39 - Section 2.8.2 – Update SFF Pull Tab CTF dimensions – Figures 40-42 - Section 2.8.3 – Update SFF Ejector latch CTF dimensions – Figs 43-45 - Section 2.8.4 – Update SFF Internal latch CTF dimensions – Figs 46-48 - Section 2.8.5 – Update SFF Baseboard CTF dimensions – Figs 50-53 - Section 2.8.6 – Update LFF Ejector latch CTF dimensions – Figs 54-56 - Section 2.8.7 – Update LFF Baseboard CTF dimensions – Figs 58-60 - Section 3.1 – Update SFF-TA-1002 card edge drawings – Figs 67-69 - Section 3.4.5 – For LFF, multiplex scan chain thermal pins (TEMP_WARN, TEMP_CRIT, FAN_ON_AUX) and WAKEn for PRSNTB[3:0] from the secondary connector. - Section 3.4.5 – Add NIC and baseboard timing requirement tables for the Scan Chain. - Section 3.7.2 – Update line side LED luminance range and add statement regarding the measurement methodology as a WIP. - Section 4.3 – Add second Management Controller MAC Address Algorithm. Add link to OCP NIC 3.0 wiki to download MAC Address algorithm calculator spreadsheet. - Section 4.10.3 – Offset 3 – Rearranged sentences for the OEM Record Format description. Technical content remains the same. Offset 15 – Add USB Present – Primary Connector field value 0x02-0xFE as Reserved for future use, and 0xFF as Unknown for consistency. Offset 16 – Change Manageability Type field value 0x04-0xFE as Reserved for future use, and 0xFF as Unknown for consistency. Offsets 17, 18, 21, 22, 23 – Change value 0xFF as Unknown instead of Reserved for consistency with offsets 0-16.
1.00	12/19/2019	Document release – version R1v00
1.0.9	10/28/2020	- General – Fixed Power Sequence Timing Requirements as Heading 2 (was incorrectly changed to Heading 3). Fixed index order for BIF pins as [2:0]. Previous versions of this document had mixed indexes represented as BIF[0:2], and incorrectly as BIF[3:0] in some instances. Fixed index order for PRSNTB pins as [3:0]. - General – Uniformly changed references for Aux Power Mode and Main Power Mode. Removed references to ACPI power states S5 and S0. Added additional text to Section 3.8.3 and 3.8.4 for the included ACPI power states. - Section 1.2 – Acknowledgements section updated. Company name updates. - Section 1.5 – Add Conventions section to define numerical representation in binary and hexadecimal radix. Standardized unit representations per the Bureau International des Poids et

Revision	Date	Change Description
		Mesures (BIPM). The number and unit are always separated with a space (example: for temperature “5 °C.” Units, where applicable, have been changed to their SI symbol. Most notably, “Ohm” is now represented with the uppercase letter omega “Ω”. - Section 1.7.2.1, 1.7.2.2 – Minor update to clarify Primary connector is a 4C+ as defined in SFF-TA-1002 and consists of an “OCP Bay” and a “4C” region. - Section 2.5.1, 2.5.2 – Figure 24 & 29 – Update PCB break off note #3 to include feature max tolerances. - Section 2.8.2 – Figure 40 – Updated dimension notation with parenthesis and add center line labeled as CL DATUM H for consistency across form-factor figures. - Section 2.8.3 – Figure 43 – Add center line labeled as CL DATUM H for consistency across form-factor figures. - Section 2.8.4 – Figure 46 – Add center line labeled as CL DATUM H for consistency across form-factor figures. - Section 3. 4 – Add clarification statement for Aux Power Mode and Main Power Mode in relation to ACPI power states. - Section 3.4.2 – Add recommendation on the PRSNTB{0:3] strapping resistors values as 0 Ω to 200 Ω. - Section 3.4.5 – Scan Chain text clarification and diagram updates. - Section 3.4.6 – Clarified the state of NIC_PWR_GOOD in relation to AUX_PWR_EN, MAIN_PWR_EN and the enabled power domain signals within operational tolerances in the truth table. - Section 3.8 – Power state machine diagram updated - +12V_EDGE in ID Mode and Programming Mode marked as optional. - Section 3.8.3 – Clarified that Aux Power Mode includes ACPI power states S3, S4 and S5 as they are equivalent from a power delivery and sequencing perspective. - Section 3.8.2, 3.8.5 – Clarifications to +12V_EDGE in ID/Programming mode. +12V_EDGE is now marked as optional in these two states. A max permissible leakage voltage is stated and the baseboard has an optional a bleed resistor. - Section 3.9 – Clarification on the slot power envelope definition (assuming that is the same path the PCI SIG is going). Add 50W power class. Increased +12V_EDGE capacitance limits on 50W, 80W and 150W power class cards. - Section 3.10.1 – Changed +12V_EDGE on normal power up sequence and programming mode power sequence diagrams to optional. - Section 4.1 – Change PCIe VDM and MCTP Base over MCTP/PCIe VDM to N/A for RBT Type cards. - Section 4.4 – Add Warning/Critical/Fatal temperature threshold example text as discussed in the June NIC 3.0 monthly meeting. Define Warning, Critical and Fatal criteria. - Section 4.10.3 – Modify FRU OEM Record. Offset 3 – Add new FRU record version for spec version 1.1. Offset 9 – Clarified this is the Hot aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables – similar to offset 19. Offset 11 – Clarified this is the Cold aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables – similar to offset 19. Offset 21 – Add QSFP Power Class 8 (10.0 W transceivers). Offset 24 – Add definition on which ports are supported in Aux Power Mode. Offset 25 – Add definition for Hot aisle standby air flow requirements when using passive cables or RJ45. Offset 27 – Add definition for Cold aisle standby air flow requirements when using passive cables or RJ45. - Section 5.3.x – Add PCIe Gen5 text/fixture/test methodology updates. PCIe Gen5 for SFF uses a max -7.0 dB insertion loss at 16 GHz. - Section 6.4.4 – Add thermocouple notes for cold-aisle inlet temperature measurements.
1.1.0	10/29/2020	Document release – version R1.1.0
1.2.0	09/13/2021	- General – Changed “SFF” references to “SFF/TSFF” where applicable. - General – Format all tables with repeated headers when they span multiple pages

Revision	Date	Change Description
		- Section 1.2 – Added Molex to the acknowledgements section. Changed NVIDIA to NVIDIA Corporation. - Section 1.4 – Added TSFF, OSFP-RHS and QSFP-DD to the acronyms section. - Section 1.6, 2.1.1 – Added text for TSFF and clarify TSFF shares the same mechanical outline as SFF. Add representative TSFF diagram. - Section 1.7.1 – Added TSFF to the OCP NIC 3.0 Form Factor Dimensions table; add Max Z-height information. Added note that SFF may fit in TSFF slot and in LFF slot, but the combination (and support mechanisms) are outside of the scope of the current specification. - Section 1.7.2.x – Updated text "Up to PCIe Gen 5 (32 GT/s) support" - Section 2.1 - Add TSFF. Add notes that actual cooling capacity for a SFF/TSFF/LFF card is dependent on the ambient conditions over the NIC. - Section 2.1.x – Clarified that faceplates are attached to the PCBA at the time of manufacture. - Section 2.1.1 – Add TSFF faceplate views to Figure 7. - Section 2.2 – Add QSFP-DD, OSFP-RHS in Line side implementation table. Add QSFP-DD, OSFP to standards cross reference table. - Section 2.3 – Add TSFF PBA exploded views to Figure 13. - Section 2.4.1, 2.4.2 – Updated faceplate subassembly drawing and BOM callouts for SFF/TSFF. - Section 2.4.4 – Added TSFF generic faceplate drawings. Drawings only contain dimensional deltas from SFF. - Section 2.5.2 – Added TSFF keep out zones. Drawings only contain dimensional deltas from SFF. - Section 2.8.5 - Replaced Figure 56 - SFF Baseboard Chassis CTF dimensions (Rear Guide Rail View) as it was clipped in the previous release. - Section 2.8.6, 2.8.7, 2.8.8, 2.8.9 – Added TSFF CTF dimensions for pull tab, ejector and internal lock board dimensions. Add TSFF baseboard CTF dimensions. Drawings only contain dimensional deltas from SFF. - Section 2.10 – Added TSFF Generic faceplate assembly CAD. - Section 3.4.1 – Clarified that hosts with unused PERST[1:5]# signals shall implement at 10kOhm pull down on the baseboard to prevent floating nets. - Section 3.4.2, 3.5.4 – Clarified that the BIF[2:0]# pins shall not change states after AUX_PWR_EN is asserted. - Section 3.4.4 – Clarified that the RBT_ISOLATE# signal shall not change state even when the NIC_PWR_GOOD signal is in the don't care state. - Section 3.7.3 – Added note regarding the use of light pipes above I/O cage assemblies for TSFF and cage implementations. - Section 3.11 – Clarified power down sequencing diagram - +12V_EDGE may optionally be disabled in ID Mode. This mirrors the same behavior for the power up sequencing diagram. - Section 5.1 – Added note stating the SFF and TSFF timing parameters are the same since the cards may share the same PBA. - Section 6.2.2, 6.2.5 – Added placeholder headings for the hot and cold aisle cooling graphs for TSFF. - Section 6.4.2 – Added placeholder heading for the TSFF thermal test fixture. - Section 6.4.5 – Added placeholder figure headings for the TSFF candlestick air velocity vs volume flow graphs. - Section 7.1.3 – Updated Safety requirements. 60950-1 was withdrawn as of 12/20/2020. 62368-1 replaced 60950-1. Document release version R1.2.0
1.2.1	12/22/2022	- Global change - RBT reference CLK is now uniformly "RBT_CLK_IN" - Global change - Corrected "PRSTNB" typos as "PRSNTB" - Global change - Scan chain signals now prefixed with "SCAN_" - Section 2.5.2 – Updated Figure 33 (TSFF Keep out zone) to be consistent with Figure 32 (SFF keep out zone). - Section 2.8.5 – Fixed Figure 57 - SFF Baseboard Chassis CTF dimensions. Image appears to be cropped in release 1.2.0. - Section 3.4.2 – Clarified in Table 24 (PCIE PRESENT and bifurcation control pins) that the default value is 0b1111 when there is no card installed.

Revision	Date	Change Description
		- Section 3.4.4 – Clarified the operation of RBT_ISOLATE# and the state of this signal based on the states of AUX_PWR_EN, MAIN_PWR_EN and NIC_PWR_GOOD. This update includes clarifications for what happens during the NIC_PWR_GOOD don't care state. Added truth table showing this relationship. - Section 3.4.4 – Table 27 – Clarified RBT_CLK_IN shall be continuous once it has started "and while RBT_ISOLATE# is high." - Section 3.7.2 – Clarified activity LED operation - the LED shall not blink when the link state is down (implied, but now explicit) - Section 3.8 – Clarified Note 2 that +12V_EDGE is optionally disabled by the baseboard in ID Mode and Programming modes. The NIC shall not rely on +12V_EDGE being present during these modes and shall not malfunction if +12V_EDGE is present or absent in said states. - Section 3.8 – Change Table 42 markings as "M" for mandatory, and "O" for optional in each power state. - Section 3.12 – Added explicit statement the DC I/O characteristics table is for informative reference only. - Section 3.12 – Removed rows for input/output current. The values are different between specs. Implementer shall refer to respective interface specifications. - Section 5.1.1 – Corrected inequality equation for RBT skew. Board channel skew is supposed to be less than the TSKEW(MAX) parameter, not greater than (as released in version 1.2.0).
1.3.0	11/01/2023	- Global change: Minor grammatical updates. - Global change: Updated the URL for the OCP NIC 3.0 wiki page. - Global change: Replaced the text "1/2 Hz" with "0.5 Hz" for consistency when representing decimal values. - Section 1.2 - Updated legal entity names. Facebook, Inc. changed to Meta Platforms, Inc and Dell, Inc. changed to Dell Technologies. - Section 1.3 – Remove DSP0222 version 1.1.0. This specification has been superseded by version 1.2.0. - Section 1.3 – Add DSP0283 revision 0.1.5 WIP (MCTP over USB binding). - Section 1.3 – Updated references list. Update PCIe Card Electromechanical Specification Revision 4.0 release date. Add Revision 5.1 spec. Add PCIe Base Specification Revision 1.0, version 1.0. - Section 2.9.2.4 - Table 15 - Fixed typo in example MAC addressing for Port 8. - Section 4.1 – Table 48 – Add DSP0283 as an optional sideband management binding. - Section 4.10.3 – Updated FRU EEPROM Record for specification release 1.3.0. Refer to Section for 10.2 change details. - Section 5.3.2 – Updated the PCIe Gen5 test fixture material as R-5775(G). Updated PCIe CEM 5 draft 0.7 references to CEM 5.1 version 1.0.
1.4.4	04/18/2024	- General: Reorganized mechanical description with separate NIC (Section 2.x) and Baseboard side descriptions (Section 3.x) - General: Added respective subsections for SFF, TSFF, DSFF, and TDSFF for easier document navigation - General: Reworked introduction text; Items specific to mechanical / electrical have been moved to the respective sections. - General: Moved LFF to Section 9. This form factor is deprecated. - General: Introduced Dual Small Form Factor into the specification. - General: For DSFF, duplicated low speed side band defaults to the Primary Connector unless otherwise declared in the 0xC1 OEM Record. - Section 4.2: Reworked pin out tables with separate sections for SFF and DSFF. Added pin number index for duplicated pins. - Section 4.3: Add section for DSFF Architectures to provide high level description of the form-factor electricals. - Section 4.4: Changed Line Side I/O implementation table and text to reflect minimum targets. LFF and DSFF cards have additional faceplate area to support additional I/O connectors. - Section 4.5.x: Added subsections for each interface description for easier navigation. Add additional pin names into the pin descriptions table for DSFF Secondary Connector

Revision	Date	Change Description
		- Section 4.5.5: Corrected Scan Chain Port numbering diagrams/text to start with "1" instead of "0" - Section 4.6: Add text describing the DSFF bifurcation and PCIe link subdivision. - Section 4.7: Add DSFF REFCLK/PERST# requirements for the Primary and Secondary Connectors. - Section 4.10: Add DSFF slot power envelope. DSFF cards are allowed to use all the SFF power slot/card envelopes in addition to the 160 W class. - Section 5.x: Reworked manageability requirement tables. Long descriptions have been moved to respective subsections and cross referenced. - Section 5.10.3: Add high level FRU OEM Record diagram, and table illustrating which OEM Records are required per form-factor - Section 5.10.3.x: Added OEM Records 0xC1 (DSFF), 0xD0/0xD1 (PCIe Link Subdivision) - Section 6.1: Add RBT NIC SFF/LFF min RBT propagation delay. - Section 6.3.1.2: Aligned DSFF with SFF PCIe Gen5 electrical budget (-7.0 dB).
1.4.5	06/05/2024	- General: Grammatical changes (non-technical), and context clarifications - Section 1.7: Defined VR - Voltage regulator; replaced 10 instances of "SVR" to "VR" - Section 2.1.3: Add diagram to illustrate 1xDSFF to 2xSFF conversion - Section 2.1.5, Table 5: Updated PCIe lane ordering now shown as 31:0, aligning with mechanical card representations. - Section 2.3.3: Moved Gold Finger Downshifting from Section 2.1.x (Mechanical Overview) to Section 2.3.x (Card Gold Finger Requirements) for better document flow. - Section 4.3: Added statement to maintain a continuous hardware arbitration loop on the HPM side when allowing the use of 2xSFF cards or 1xDSFF card. - Section 4.5.1.7: Add example PCIe interface topology diagram. - Section 4.5.3: Clarified that SMBus is a multi-initiator protocol. - Section 4.5.3.x, 5.9, 5.10.3.1: Updated protocol terminology as "controller" / "target." Clarified that isolation logic may be required for the target silicon devices to prevent leakage. Additionally clarified isolation logic is controlled by the local "Aux Power Good" signal on the card. - Section 4.5.3, 4.5.4 and 4.5.5 – Mandate usage of SMBus, RBT and Scan Chain on the Primary Connector only (for DSFF cases). Removed discovery cross references to the 0xC1 OEM Record. - Section 4.5.4.8, 5.9: Clarified for that SLOT_ID[3:2] are not used for the RBT package or FRU EEPROM address on the DSFF. - Section 4.9: Changed "AC Power Off" to "NIC Power Off" to include possibilities of controlled hot swap. Updated Power State Machine diagram to explicitly call out removal of +3.3V_EDGE and +12V_EDGE when transitioning to NIC Power Off. - Section 4.10: Merged DSFF power slot/card envelope with SFF table. Clarified DSFF may use all SFF slot/card envelopes in addition to the new 160 W class for DSFF only. - Section 4.12.2: Updated power down sequence diagram to align with PCIe CEM 6.0 footnotes. - Section 4.12.4: Updated TPERST-CLK to TPERST#-CLK to align with new CEM spec nomenclature. Corrected TPERST#-CLK definition from minimum to maximum. - Section 4.13: Removed Digital I/O AC specifications table. It was empty. Designers shall refer to the respective industry specs for details.
1.5.0 RC1	09/05/2024	- General: Global change for “rail guide” to “guide rail” - Section 2.x – Added DSFF NIC side mechanical drawings. - Section 3.x – Added DSFF Baseboard mechanical drawings. - Section 4.5.3, 4.5.4, 4.5.6 and 4.5.8 – Added new note for SMBus, RBT/Timing, Scan Chain and USB interfaces declaring these are internal use only. - Section 4.5.4.x – Reorganized section. Added support for Flex I/O implementation (as Timing Pins) – Flex I/O overloads the RBT pins. - Section 4.5.4.3 – Added text requiring Baseboards to discover if the OCP NIC cards support hardware arbitration before adding the NIC slot into the arbitration ring. Referenced DSP0222 “Summary of scheme for the MC without prior knowledge of hardware arbitration” as the discovery flow. - Section 4.5.4.4.x – Added Flex I/O Timing Pins to the specification.

Revision	Date	Change Description
		- Section 4.5.5.x – Moved the Slot ID pins to a dedicated section. - Section 4.9 – Updated Power State Machine diagram. Aux Power Mode: changed “WAKE# & NC-SI Over RBT Enabled” to “WAKE# or NC-SI Over RBT Enabled”. Main Power Mode: struck “WAKE# & NC-SI Over RBT enabled,” “Baseboard RBT_ISOLATE#=1” and “RBT_REFCLK = on”). Wake is not applicable in Main, and NC-SI related pin states didn’t change when moved into Main). - Section 4.10.1 – Added discussion on DSFF current sharing between the Primary and Secondary connector edge (NIC side); and Baseboard side requirements. - Section 4.13 – Added digital I/O DC specifications for the single ended timing signals. (TS_TX_SYNC, TS_TX_FREQ, TS_RX_SYNC, TS_RX_FREQ, TS_GPI and TS_GPO) - Section 5.10.3 – Added table entries for new 0xC2 OEM Record (Timing Pins) - Section 6.3.1 – Added PCIe Gen6 channel requirements. - Section 9.1.7 – Updated LFF faceplate Bill of Materials. - Section 10.1 & 10.2 – Updated Document and FRU Content Revision History table heading order. Revision, Date, then Change Description.
1.5.0 Release	09/20/2024	- General – Replaced Open Compute Project logo with a higher resolution version on page 1. - Section 2.6.6 – Add additional supplier to side EMI finger BOM. - Section 3.3.4 – Updated DSFF Baseboard CTF dimension drawings for 1x DSFF and 2x SFF. New drawings call out board Center Line and distance to PCB edge instead of inner feature of guide rail. - Section 4.4 – Included 4x QSFP-DD as supported line side I/O implementation for DSFF. - Section 4.5.4.x – Updated “Flex IO” nomenclature as “FLEXIO_[0:1]_IO[0:4]” and “FLEXIO_SEL[0:1]” to align with PCIe CEM 6.0 pin naming conventions. - Section 4.5.4.3.8 – Updated Figure 108 the NC-SI over RBT Connection Example – Dual Primary Connector. Addressed HW arbitration ring path with prior 74LVC1G3 logic when only Slot 1 OCP NIC card is installed. New Example combinatorial logic for hardware arbitration signal connections. Added Figure 109 showing detailed combinatorial logic. Added Table 30 to show combinatorial logic truth table. - Section 6.1 – Clarified timing parameters T_{CYCLE_SFF} also applies to the DSFF. - Section 7.2.x / 7.4.x – Added DSFF/TDSFF framework for TBD ASIC cooling/Test fixture sections. - Section 7.7.1 – Updated supported faceplate types for DSFF shock and vibe fixture (pull tab and internal lock).
1.6.0 Release	03/31/2025	- General – Resolved formatting issues with figure/table captions - General – Renamed DSFF OEM Record to Extended OEM Record. - General – Moved OEM Record 0xC1 (Extended OEM Record) to 0xD2 and OEM Record 0xC2 (Flex I/O OEM Record) to 0xD3 to prevent incompatibilities with the MHS M-PNP specification. Refer to the FRU Content Revision History for detailed changes. - Section 1.2 – Updated member companies in the Acknowledgements section - Section 1.3 – Add Open Compute Tenets. - Section 1.6 – Add the OSFP MSA, SNIA SFF-8472 and SNIA SFF-8636 specifications to the references section. Update SFF-TA-1002 to revision 1.5. - Section 3.1 – Add note about the SFF-TA-1002 R1.5 Type 1 and Type 2 4C+ connectors. - Section 4.2.2 – Corrected typo in the DSFF Side A/B connector pinout (no functional changes). - Section 4.3 – Clarified PRSNTB encoding requirements for DSFF cards that only use the Primary Connector gold fingers (PRSNTB[3:0]=0b0010). - Section 4.5.2.3, 4.6.2 – Clarified that the BIF# pin encodings shown in the specification and reference collateral depict the electrical high ("1") and electrical low ("0") values. - Section 4.5.4.4.x – Add termination requirements for the Flex I/O pins. Implementation matches that of an RBT enabled baseboard/NIC. - Section 4.5.6.5 – Changed Scan Chain "examples" to "implementations" as part of updating informative language to normative language. Clarified the SCAN_DATA_IN bit order is MSB first (bit 7), and LSB (bit 0) last. - Section 4.5.8.1 – Clarified that the USB interface shall be isolated by the baseboard until AUX_PWR_EN=1 and the first rising edge of NIC_PWR_GOOD=1.

Revision	Date	Change Description
		- Section 4.9 – Rotated the Available Card Functions per Power State table 90 degrees for readability. Added Flex I/o and USB interfaces to the table. Add row for “Optional Interfaces” (RBT, Wake, Flex I/O, USB). Moved PERSTn higher in the table between MAIN_PWR_EN and FRU. Changed PCIe “no Link” language to “Link in Reset” and “Link Up” to better describe the operational state of the platform. Clarified Note 5 as “if the interface is supported by the OCP NIC 3.0 card, otherwise the interface is driven by the default pull up/down resistors.” - Section 4.10 – Add Note 6 to the Slot and Card Power Envelopes stating that the SFF-TA-1002 connectors permit 1.1 A/pin for continuous operation. - Section 4.12.1 – Clarify power up requirements for the Primary and Secondary connector when powering on a DSFF card. - Section 5.10.3 – Updated MultiRecord Type IDs (0xC1 --> 0xD2, 0xC2 --> 0xD3). Clarified the least significant and most significant byte orders for offsets that span multiple bytes. Clarified the contents of each OEM record also includes a version field that the baseboard shall read and compare against released specification versions. Added the Type ID allocation link from the MHS Hardware Management GitHub repository.

5148

10.2 FRU Content Revision History

The following table summarizes the FRU content revision history and maps it to specification releases.

Revision	Date	Change Description
0.70	01/25/2018	- Initial FRU contents.
0.80	06/04/2018	- Offset 4, 5 – Clarified that the Card Max Power in Main Power Mode and the Card Max Power in Aux Power Mode do not include the power consumed by transceivers plugged into the line side receptacle(s). - Offset 8 – Corrected Card active/passive cooling) as a byte value (not bitwise). - Offset 13, 14 – Removed ASIC temperature target; replaced with UART Configuration 1 and UART Configuration 2. - Offset 15 – Added USB Present. - Offset 32-127 – Explicitly called out UDID offset ranges for controllers 1 through 6.
0.81	07/06/2018	- Offset 13, 14 – Clarified these offsets are only applicable to the Secondary Connector (LFF designs) - Offset 15 – Clarified this offset is only applicable to the Primary Connector (SFF designs)
0.85	11/20/2018	- Offset 3 – Corrected Manufacturer ID as 0x00A67F. - Offset 9, 10 – Clarified hot aisle standby airflow LSB, MSB byte order. - Offset 11, 12 – Clarified cold aisle standby airflow LSB, MSB byte order. - Offset 16 – Add card manageability type.
0.86	04/02/2019	- Offset 32-127 – Add note declaring the controller UDID fields may be omitted and left as zero length if no corresponding controller is present on the card.
0.90	06/20/2019	- Offset 3 – Updated FRU OEM Record Version compliance. Cards compliant to spec version 0v90 shall use the value 0x01. All other values reserved. - Offset 6 – Clarified Hot Aisle Card Cooling Tier offset is applicable to passive cable or RJ-45 implementations. - Offset 7 – Clarified Cold Aisle Card Cooling Tier offset is applicable to passive cable or RJ-45 implementations. - Offset 9, 10 – Clarified hot aisle standby airflow requirement with an approach air temperature of 45 °C. - Offset 11, 12 – Clarified cold aisle standby airflow requirement with an approach air temperature of 35 °C. - Offset 17 – Add FRU Write Protection Mechanism indication. - Offset 18 – Add Programming Mode Power State indication. - Offset 19 – Add Hot Aisle Cooling Tier with Active Cables indication. - Offset 20 – Add Cold Aisle Card Cooling Tier with Active Cables indication. - Offset 21 – Add Transceiver Reference Power Level indication. - Offset 22 – Add Transceiver Reference Temperature Level indication. - Offset 23 – Add Card Thermal Tier with local Fan Fail indication. - Offset 31 – Clarify Number of Physical Controllers as the number of SMBus connected controllers on the OCP NIC 3.0 card.
0.92	11/08/2019	- Offset 3 – Changed FRU OEM Record Version definition to declare “this FRU record is released with version x.xx” of the specification. This prevents revising the field to match future specification releases when no FRU changes have been made.
0.99	12/8/2019	- Offset 15 – Add USB Present – Primary Connector field value 0x02-0xFE as Reserved for future use, and 0xFF as Unknown for consistency within the OEM record. - Offset 16 – Change Manageability Type field value 0x04-0xFE as Reserved for future use, and 0xFF as Unknown for consistency within the OEM record.

Revision	Date	Change Description
		- Offsets 17, 18, 21, 22, 23 – Change value 0xFF as Unknown instead of Reserved for consistency with offsets 0-16.
1.1.0	10/28/2020	- Offset 3 - Add new FRU record version for spec version 1.1. - Offset 9 – Clarified this is the Hot aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables - similar to offset 19. - Offset 11 – Clarified this is the Cold aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables - similar to offset 19. - Offset 21 – Add QSFP Power Class 8 (10.0 W transceivers). - Offset 24 – Add definition on which ports are supported in Aux Power Mode. - Offset 25 – Add definition for Hot aisle standby air flow requirements when using passive cables or RJ45. - Offset 27 – Add definition for Cold aisle standby air flow requirements when using passive cables or RJ45.
1.3.0	11/01/2023	- Offset 3 – Add new FRU record version for spec version 1.3. - Offset 16 – Changed field to a bit map. Cards may support multiple manageability types. The bitmap allows for vendor specific combinations. Add USB CDC-EEM as a manageability option.
1.4.4	02/14/2024	**Base OEM Record (0xC0)** - Renamed record as the “base” OCP NIC 3.0 record. - Add controller #7, #8 to align with DSFF PERST/REFCLK count **DSFF OEM Record (0xC1)** - Add new record for supporting DSFF specific features **DSFF PCIe Link Subdivision Record 0 (0xD0)** - Add new record for supporting DSFF PCIe Link Subdivision. **DSFF PCIe Link Subdivision Record 1 (0xD1)** - Add new record for supporting DSFF PCIe Link Subdivision.
1.4.5	06/05/2024	**DSFF OEM Record (0xC1)** - Offset 5 – Clarified the DSFF Card Edge Type field only applies to power and PCIe connectivity. - Offset 6 – Clarified offset only applies to the secondary connector connection of duplicated sideband signals and is not applicable when Offset 5 declares the card edge is downshifted to x16. Removed support for SMBus[1], RBT[1] and Scan Chain[1] on the Secondary Connector Edge. **DSFF PCIe Link Subdivision Record 0 (0xD0)** - Offset 3 - Fixed typo in bits 7:5 for the associated controller instance from OEM Record 0xC0 for Link 0. - Offset (Link 3n + 3) - Fixed typo in bits 7:5 for the associated controller instance from OEM Record 0xC0 for Link *n*.
1.5.0 Release	09/20/2024	**Base OEM Record (0xC0)** - Redefined Offset 16 Bit 4 as “USB Communication Device Class”. Added note that the specific USB device class shall be queried. This was done in favor of explicitly defining USB CDC EEM, ECM and NCM to the FRU. **Flex I/O OEM Record – 0xC2** - Define initial OEM record for use with the Flex I/O Timing Pin application.
1.6.0 Release	03/31/2025	**Base OEM Record (0xC0)** - Offset 3 – Add encoding 0x06 for version 1.6.0 - Offset 13, 14 – Clarified these fields are only applicable to LFF cards. SFF and DSFF cards do not have UART pins.

Revision	Date	Change Description
		- Offset 21 – Removed cross references to the SFP Power Level/QSFP Power Classes. Changed encoding as an unsigned decimal with a resolution of 0.25 W. This value represents the active transceivers that were used to determine the card thermal tier. - Offset 24 – Changed encoding 0b0000_0000 to represent "No ports are active in Aux Power Mode" instead of "Configuration Unknown" - Offset 29 – Was reserved. Add support for declaring Maximum Supported Transceiver Power. Encoding as an unsigned decimal with a resolution of 0.25 W. This is only used as an indicator of the max power supported on the OCP NIC transceiver cage. It is not used for determining the card thermal performance. - Offset 31 – Clarified "N=0" case for "no SMBus connected controllers exist on this OCP NIC 3.0 card" **DSFF PCIe Link Subdivision Record 0 (0xD0)** - PCIe Mode Descriptor (sub table) - clarified the encoding of the PCIe Mode - Number of Supported PCIe Links field. **Extended OEM Record (0xD2)** - Renamed from DSFF OEM Record to Extended OEM Record. - Changed Type ID from 0xC1 to 0xD2 to maintain compatibility with MHS M-PNP specification. 0xC1 is used by the MHS DC-SCM specification. - Offset 3 – Add encoding 0x02 for specification version 1.6.0 since this record was changed from 0xC1 to 0xD2. - Offset 9 – Clarified BIF bits [5:0] correspond to record 0xD0 when the encoding is 0x01. - Offset 16 – Clarified note in this offset for query/discover requirements in the Aux and Main Power Modes. **Flex I/O OEM Record (0xD3)** - Clarified that the propagation delay fields may be optionally used by systems that can use it. - Changed Type ID from 0xC2 to 0xD3 to maintain compatibility with MHS M-PNP specification. 0xC2 is used by the MHS M-CRPS specification. - Offset 3 – Add encoding 0x02 for specification version 1.6.0 since this record was changed from 0xC2 to 0xD3. - Offset 4 – Clarified if RBT and Timing Sync Modes are both supported on the OCP NIC, the interface shall default to RBT.

5153