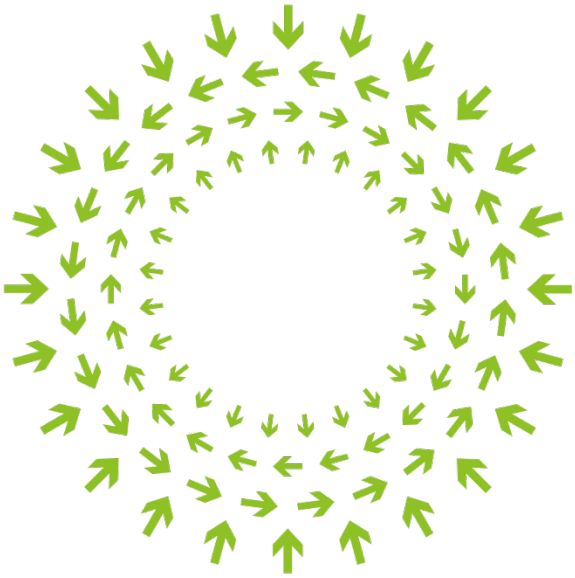

OPEN

Compute Project

Mezzanine Card for Intel v2.0 Motherboard

Authors:

Harry Li, Hardware Engineer

Jia Ning, Hardware Engineer

1 Contents

2 Overview 3

3 Mezzanine Card Mechanical Details 3

3.1 Form Factor 3

3.2 Connector 3

3.3 Pin Definition 4

3.4 Power Capability and Status 6

3.5 Installation in Chassis 6

4 10GbE Chip 6

4.1 Ports and LEDs 7

4.2 MAC Address Label Requirements 7

5 Management Interface 8

6 Environmental 8

6.1 Environmental Requirements 8

6.2 Shock and Vibration 8

6.3 Regulations 8

2 Overview

This document describes the mezzanine card design for use with Open Compute Project Intel v2.0 motherboards. The mezzanine card is installed on an Intel v2.0 OCP motherboard to provide extended functionality, such as support for 10GbE PCI-E devices.

3 Mezzanine Card Mechanical Details

3.1 Form Factor

illustrates the mezzanine card's form factor. Refer to the 2D DXF and 3D files for dimensions, tolerance, and height restrictions.

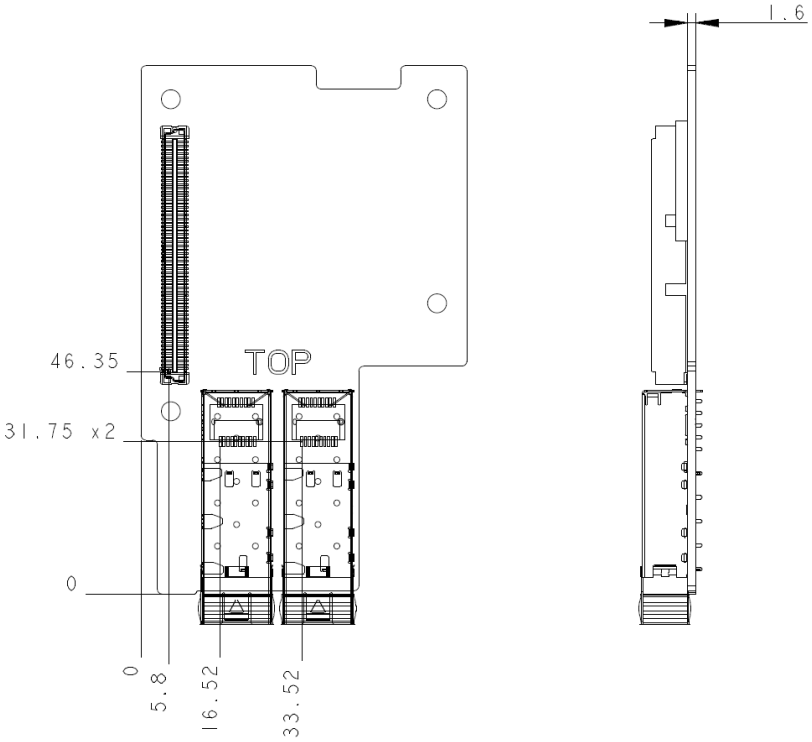

Figure 1 Mezzanine Card Form Factor

3.2 Connector

An FCI 61083-124402LF or equivalent connector is mounted on the mezzanine card, to mate with the FCI 61082-121402LF or equivalent connector that is mounted on the motherboard. PCI-E x8 Gen3 and SATA3/SAS2 signals are provided in the connector.

3.3 Pin Definition

The mezzanine card pin definition is as follows. The directions of the signals are from the perspective of the motherboard.

Signal	Description	Pin	Pin	Signal	Description
P12V/P12V_AUX	Power/Aux Power[1]	61	1	MEZZ_PRSNT1_N	Present pin1, short to Pin120 on Mezz card
P12V/P12V_AUX	Power/Aux Power	62	2	P5V_AUX	Aux Power
P12V/P12V_AUX	Power/Aux Power	63	3	P5V_AUX	Aux Power
GND	Ground	64	4	P5V_AUX	Aux Power
GND	Ground	65	5	GND	Ground
P3V3_AUX	Aux Power	66	6	GND	Ground
GND	Ground	67	7	P3V3_AUX	Aux Power
GND	Ground	68	8	GND	Ground
P3V3	Power	69	9	GND	Ground
P3V3	Power	70	10	P3V3	Power
P3V3	Power	71	11	P3V3	Power
P3V3	Power	72	12	P3V3	Power
GND	Ground	73	13	P3V3	Power
LAN_3V3STB_ALERT_N	SMBus Alert for OOB	74	14	RSVD (MEZZ_CPRSNT1_N)	Reserved (Present pin for hotswap port1)
SMB_LAN_3V3STB_CLK	SMBus Clock for OOB	75	15	RSVD (MEZZ_CPRSNT2_N)	Reserved (Present pin for hotswap port2)
SMB_LAN_3V3STB_DAT	SMBus Data for OOB	76	16	RSVD (SSD_PRSNT_N)	Reserved (Present pin for disk module)
PCIE_WAKE_N	PCIE wake up	77	17	RST_PLT_MEZZ_N	PCIe reset signal
RSVD (DA_DSS)	Reserved (Disk activity input for disk module, pull high to P3V3 on motherboard)	78	18	RSVD (MEZZ_SMCLK)	Reserved (PCIe slot SMBus Clock)
GND	Ground	79	19	RSVD (MEZZ_SMDATA)	Reserved (PCIe slot SMBus Data)
RSVD (SATA_TX+)	Reserved (SATA TX+ for disk module)	80	20	GND	Ground
RSVD (SATA_TX-)	Reserved (SATA TX- for disk module)	81	21	GND	Ground
GND	Ground	82	22	RSVD (SATA_RX+)	Reserved (SATA RX+ for disk module)
GND	Ground	83	23	RSVD (SATA_RX-)	Reserved (SATA RX- for disk module)

[1] Depending on Intel v2.0 motherboard ODM implementation

CLK_100M_MEZZ1_DP	100MHz PCIe clock	84	24	GND	Ground
CLK_100M_MEZZ1_DN	100MHz PCIe clock	85	25	GND	Ground
GND	Ground	86	26	RSVD(CLK_100M_MEZZ2_DP)	Reserved(2nd set of 100MHz PCIe clock)
GND	Ground	87	27	RSVD(CLK_100M_MEZZ2_DN)	Reserved(2nd set of 100MHz PCIe clock)
MEZZ_TX_DP_C<0>	PCIE TX signal	88	28	GND	Ground
MEZZ_TX_DN_C<0>	PCIE TX signal	89	29	GND	Ground
GND	Ground	90	30	MEZZ_RX_DP<0>	PCIE RX signal
GND	Ground	91	31	MEZZ_RX_DN<0>	PCIE RX signal
MEZZ_TX_DP_C<1>	PCIE TX signal	92	32	GND	Ground
MEZZ_TX_DN_C<1>	PCIE TX signal	93	33	GND	Ground
GND	Ground	94	34	MEZZ_RX_DP<1>	PCIE RX signal
GND	Ground	95	35	MEZZ_RX_DN<1>	PCIE RX signal
MEZZ_TX_DP_C<2>	PCIE TX signal	96	36	GND	Ground
MEZZ_TX_DN_C<2>	PCIE TX signal	97	37	GND	Ground
GND	Ground	98	38	MEZZ_RX_DP<2>	PCIE RX signal
GND	Ground	99	39	MEZZ_RX_DN<2>	PCIE RX signal
MEZZ_TX_DP_C<3>	PCIE TX signal	100	40	GND	Ground
MEZZ_TX_DN_C<3>	PCIE TX signal	101	41	GND	Ground
GND	Ground	102	42	MEZZ_RX_DP<3>	PCIE RX signal
GND	Ground	103	43	MEZZ_RX_DN<3>	PCIE RX signal
MEZZ_TX_DP_C<4>	PCIE TX signal	104	44	GND	Ground
MEZZ_TX_DN_C<4>	PCIE TX signal	105	45	GND	Ground
GND	Ground	106	46	MEZZ_RX_DP<4>	PCIE RX signal
GND	Ground	107	47	MEZZ_RX_DN<4>	PCIE RX signal
MEZZ_TX_DP_C<5>	PCIE TX signal	108	48	GND	Ground
MEZZ_TX_DN_C<5>	PCIE TX signal	109	49	GND	Ground
GND	Ground	110	50	MEZZ_RX_DP<5>	PCIE RX signal
GND	Ground	111	51	MEZZ_RX_DN<5>	PCIE RX signal
MEZZ_TX_DP_C<6>	PCIE TX signal	112	52	GND	Ground
MEZZ_TX_DN_C<6>	PCIE TX signal	113	53	GND	Ground
GND	Ground	114	54	MEZZ_RX_DP<6>	PCIE RX signal
GND	Ground	115	55	MEZZ_RX_DN<6>	PCIE RX signal
MEZZ_TX_DP_C<7>	PCIE TX signal	116	56	GND	Ground
MEZZ_TX_DN_C<7>	PCIE TX signal	117	57	GND	Ground
GND	Ground	118	58	MEZZ_RX_DP<7>	PCIE RX signal
GND	Ground	119	59	MEZZ_RX_DN<7>	PCIE RX signal
MEZZ_PRSNT2_N	Present pin2, short to Pin1 on Mezz card	120	60	GND	Ground

3.4 Power Capability and Status

The motherboard supplies power to the power pins on the mezzanine card connector. Four power rails are available. The current capability and power status are indicated in the table below. Normal power is available at on state S0 only. Auxiliary power is available at all power states including hibernate state S4 or off state S5.

Power Rail	Voltage Tolerance	# Pins	Current Capability	Status
P12V/P12V_AUX	±8%(max)	3	2.4A	Normal power or auxiliary power[2]
P5V_AUX	±9%(max)	3	2.4A	Auxiliary power
P3V3_AUX	±9%(max)	2	1.6A	Auxiliary power
P3V3	±9%(max)	8	6.4A	Normal power

3.5 Installation in Chassis

3D View of shows the 3D view of the mezzanine card installed in an Open Compute chassis.

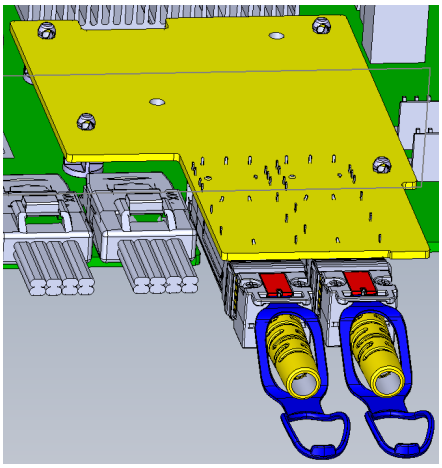

Figure 2 3D View of Mezzanine Card in Chassis

4 10GbE Chip

The mezzanine card has a 10GbE chip to provide two (or, optionally, one) SFP+ 10GbE ports, which are dual or single copper direct-attached cables and dual or single optical modules. Wake on LAN and Reboot over Wakeup features are supported. The ODM should provide a heat sink for the card.

[2] Depending on Intel v2.0 motherboard ODM implementation

4.1 Ports and LEDs

On a card with one port, only port 0 is populated. The mezzanine card has four LEDs to show the status of two ports. shows the location of the two ports and the four LEDs.

- P0-LED0: Port 0, Speed (10G Green/1G Yellow)
- P0-LED1: Port 0, Link/Activity (Green)
- P1-LED0: Port 1, Speed (10G Green/1G Yellow)
- P1-LED1: Port 1, Link/Activity (Green)

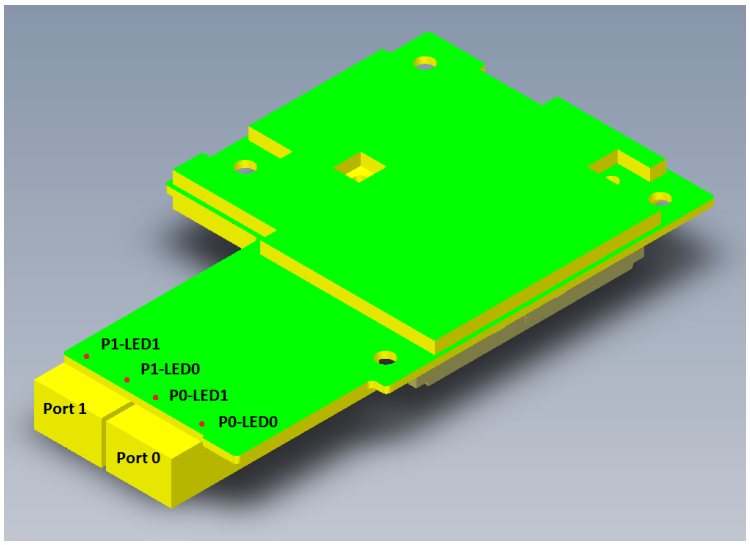

Figure 3 Mezzanine Card Ports and LEDs

4.2 MAC Address Label Requirements

4.2.1 Placement Rules

MAC address label(s) must be scannable when the mezzanine card is installed in the server or rack by the system vendor, rack integrator, or data center technician without interrupting normal operation. Bar code and human readable text for the MAC address must be placed within 18mm of the mezzanine card PCB edge, as shown in .

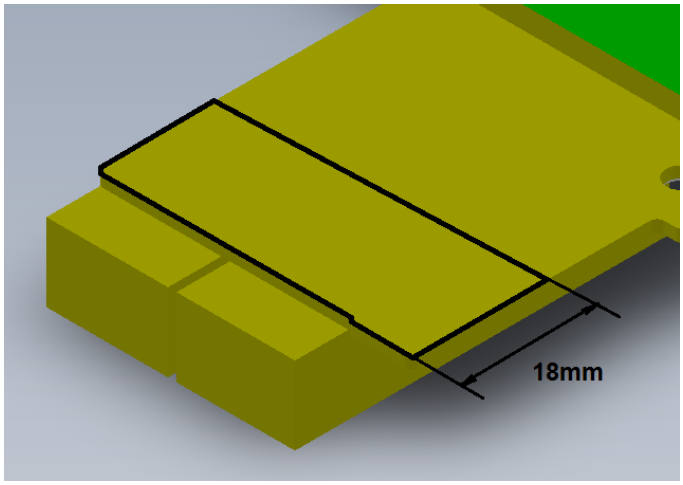

Figure 4 MAC Address Label Placement



4.2.2 Human Readable Text Rules

A header is required for the label. For example: "P0:hh.hh.hh.hh.hh.hh". The font size should be larger than 5 points. If there is more than one MAC address per unit, a human-readable text header is required and must differentiate. For example: "ME:hh.hh.hh.hh.hh.hh" or "P0: hh.hh.hh.hh.hh.hh" or "P1: hh.hh.hh.hh.hh.hh".

4.2.3 Barcode Requirements

The barcode should adhere to Code 128, with a minimum "X dim" >= .003". Barcode data should **not** include the period (".") character. For example: "hh.hh.hh.hh.hh.hh" should scan as "hhhhhhhhhhhh".

4.2.4 Label Permanence and Technology

The MAC address label must adhere for at least 3-5 years in Open Compute usage and thermal environment. Materials can be PCB silkscreen, polyester, and polyamide with acrylic adhesive.

4.2.5 Label Size

Label size is determined by the ODM. It should meet the above requirements.

5 Management Interface

The 10GbE card has a management interface compatible with Intel's Management Engine (ME) through the Patsburg PCH SMLINK0 port and provides Out of Band (OOB) network access. The hardware and firmware design support management capability in both S0 and S5 states.

6 Environmental

6.1 Environmental Requirements

This mezzanine card meets the same environmental requirements specified in the Open Compute Project Intel Motherboard v2.0 design specification. Minimum airflow is 10 LFM at S0 and 0 LFM at S5. Maximum inlet ambient temperature is 35°C.

6.2 Shock and Vibration

This mezzanine card meets the same shock and vibration requirements specified in the Open Compute Project Intel Motherboard v2.0 design specification.

6.3 Regulations

This mezzanine card meets CE and FCC Class A requirements.