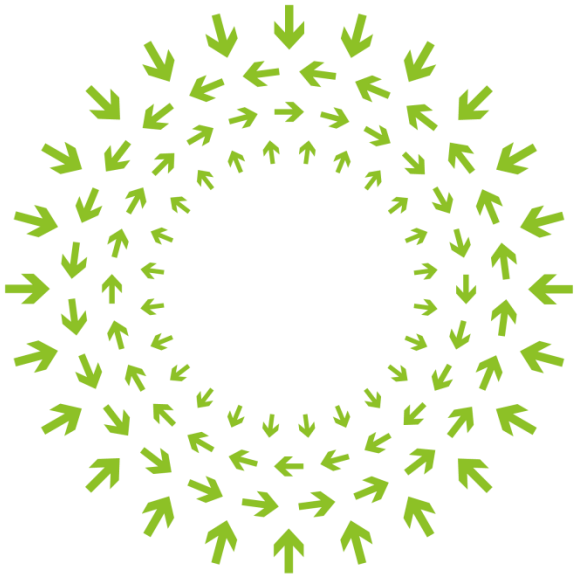

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Compute Project

HPM Common Circuit Type 1 Design Specification under DC-SCM CLA

Revision 1.0, Version 1.00

Revision 1.0, Version 1.00 Authors:

AMD: Ravi Bingi
Aspeed: Dwarka Partani
Dell: Timothy M. Lambert
HPE: David Heinrich, Phillip Leech
IBM: Jerry Fahr, Emile Kowalski
Intel: Kasper Wszolek, Qian Wang
Jabil: Todd Rosedahl
Lenovo: Clifton Kerr, Brian Fuchs
Nuvoton: Lior Albaz, Ohad Falik

Revision History

Revision	Version	Date	Notes
1.0	0.51	10/12/2023	Initial public review
1.0	1.0	8/12/2024	1.0 Release

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Acknowledgement

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback from the authors and supporting companies.

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- OCP NIC 3.0 Design Specification Version 1.0.9
- OCP DC-SCM 2.0 LVDS Tunneling Protocol and Interface (LTPI) Specification 1.0

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1. HPM Common Circuit Type 1 Overview

HPM Common Circuit Type 1 is defined as 1X DC-SCM managing 1X HPM with 1X host domain with 1-4X CPU sockets. Subsequent types may be defined for market driven applications such as Type 2: 2X host domains on 1 HPM or 2X host domains on 2X HPMs with 1X interposer.

1.1 Goals

DC-SCM 2.1 contains a DC-SCI 2.1 superset of interfaces between a DC-SCM and an HPM to cover all possible use cases. DC-SCMs are where platform personality, systems management and security functionality may be anchored and thus are expected to vary in implementation. Possible commercial benefits of a set of HPM common circuits in an OCP Design Specification include:

1. A better chance for hardware interoperability than without
2. Providing a basis for achieving FW, BIOS, and programmable logic interoperability (aligned to the Modular-Plug-n-Play effort within DC-MHS)
3. Maximize CPU vendor validation and design leverage while minimizing OEM customization requirements needed for HPM productization
4. Synergistic systems management connectivity and best practices inclusive of DC-SCM-to-HPM and HPM-to-Peripheral subsystems
5. Maximize miscellaneous component multi-sourcing options
6. Maximize sustainability opportunities, such as HPM and peripheral subsystem re-use

1.2 In Scope

1. CPU type agnostic, specific DC-SCI Version 2.1 single pin usage map (XLS) including functionality, direction, and earliest power state for bias
2. Block Diagrams for single instance connectivity between DC-SCM & HPM directly coupled peripheral subsystems, largely aligned to DC-MHS base specifications
3. Alignment to OCP DC-MHS base specifications for circuit guidance where applicable. e.g., Sideband circuits for M-XIO, PICPWR & 12V_STBY connector

4. Connectivity Rules such as 2-wire fanout controls to aid in software platform enablement

The green area in the follow figure shows that the scope includes circuits local to HPM that excludes HPM Vendor-specific IP, such as CPU particulars. This specification includes guidance for interfacing to one instance of each major type of subsystem coupled to an HPM, attempting to align to DC-MHS where possible. Figure is not to scale.

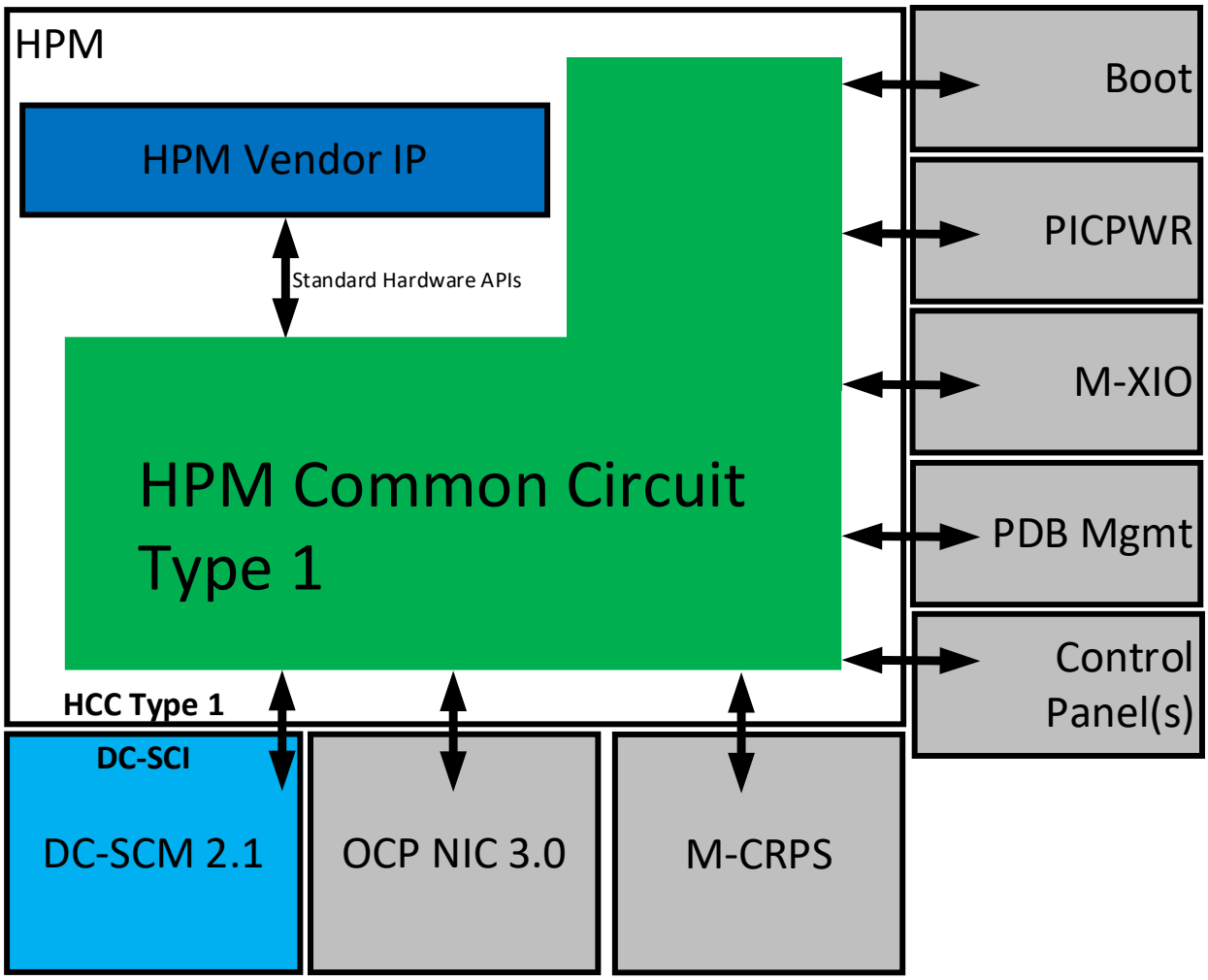


Figure 1. Type 1 Common Circuit Overview

1.3 Out of Scope

1. Specific CPU Vendor/Family/Generation or any NDA collaterals

2. Physical or Operational Behavioral Spec Rules (e.g., silk screen naming of major components/connectors, Time to Boot, etc.)
3. Schematic or layout guidance
4. In-band bus mapping, such as PCIe topologies
5. DC-SCM core logic including a specific BMC or Platform Root of Trust implementation
6. CPLD/FPGA or MCU firmware source code
8. HPM or DC-SCM authentication methods
7. Peripheral subsystem HW/FW guidance beyond what is stipulated in DC-MHS specifications
9. Specific power, reset or clocking topologies beyond those affecting the DC-SCM
10. Endorsement of specific HPM IC vendors or part numbers

2. Glossary & Diagram Notes

DC-MHS: Datacenter-Modular Hardware System
M-HPM: Modular Host Processor Module; host refers to the primary computing domain (versus the system management domain)
DC-SCM: Datacenter-Secure Control Module
DC-SCI: Datacenter-Secure Control module Interfaces between the DC-SCM and HPM
M-PnP: Module Plug-n-Play DC-MHS Design Specification
M-PIC: Modular Platform Infrastructure Connectivity (miscellaneous interconnects)
M-XIO: Modular Extended I/O (connectors, pinouts and HW APIs)
M-CRPS: Modular- Common Redundant Power Supply
M-PESTI: Modular-Peripheral Sideband Tunnelling Interface

Diagram Notes:

1) The drawings within this specification contain solid lines indicate required connections. Dashed / dotted lines indicate optional.

2) All colors in drawings are arbitrary and imply no formal meaning, unless otherwise described in a key.

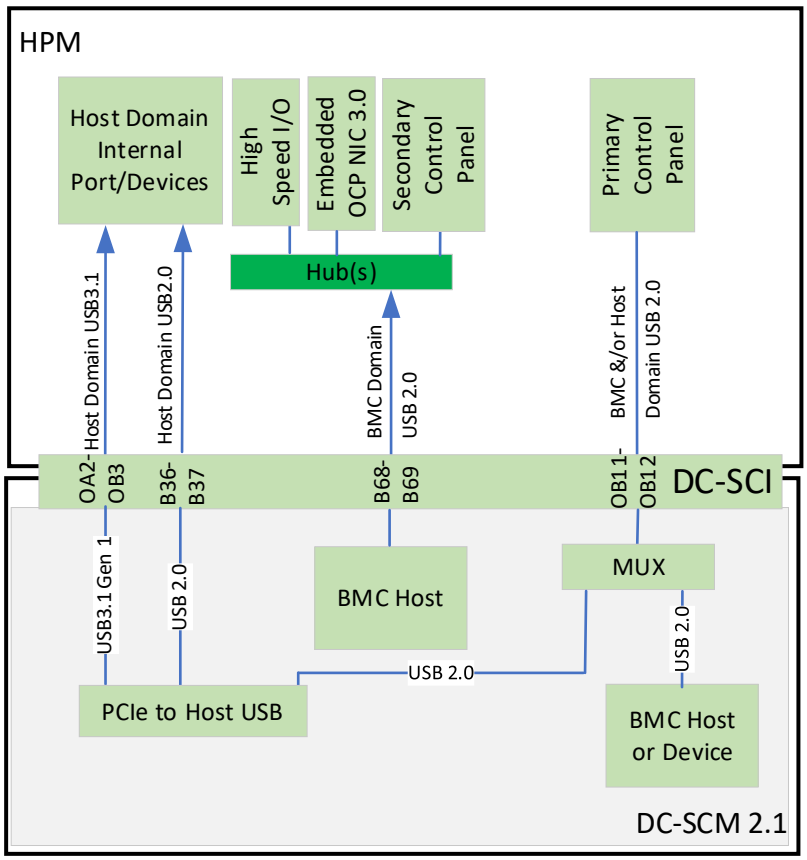
3) Drawings assume voltage level and power domain compatibility with respect to the DC-SCI requirements. Where specific devices may require alternate voltages, such as 1.8V instead of 3.3V or 1.0V instead of 1.8V, isolation is likely omitted from block diagrams.

4) The term ISO is used on some block diagrams to imply that it is likely that cross power domain isolation is necessary

3. Subsystem HW Guidance

This design specification is accompanied by a DC-SCI Type 1 spreadsheet with all the agreed upon single pin usages aligned to the DC-SCI contained within the DC-SCM official 2.1 base specification.

3.1 USB (Host & BMC Managed Domains)



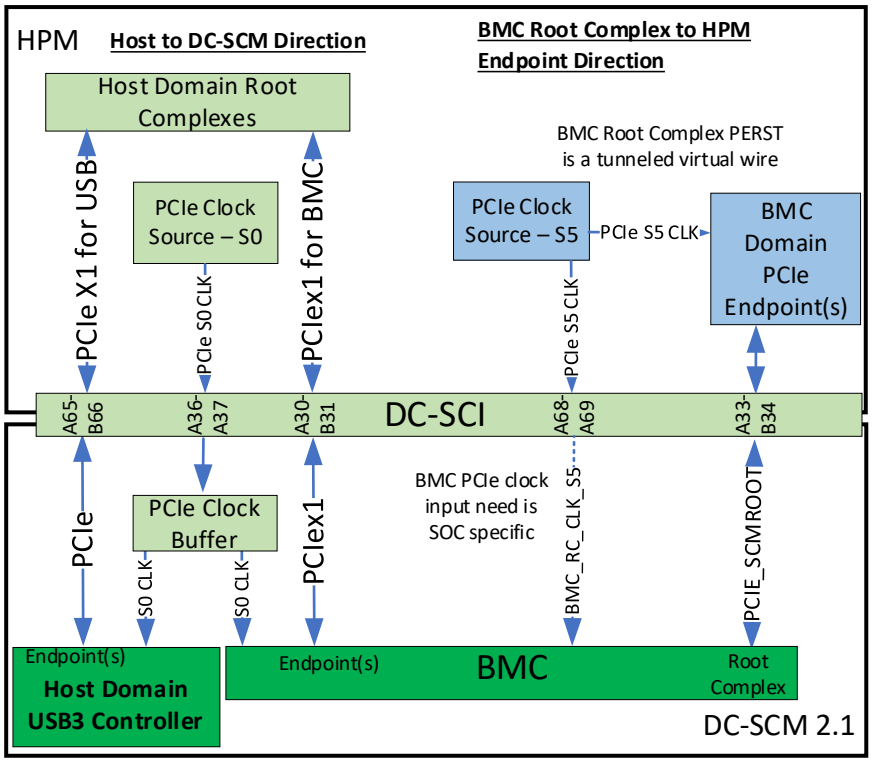
Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 2. USB

Descriptions:

- Assumes Host domain USB ports is generated on the DC-SCM
- OB11-OB12 bus usage is a simple HPM passthrough.
- DC-SCM side diagram shows one example of a method of connectivity to help understand the HPM connectivity rationale.
- BMC virtual devices or DC-SCM local ports are not shown as they do not affect the HPM.
- It is advised to place USB 3.1 0.1uF series capacitors near the transmitter pair on the respective board.

3.2 PCIe (Host and BMC Domains)



Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 3. PCIe

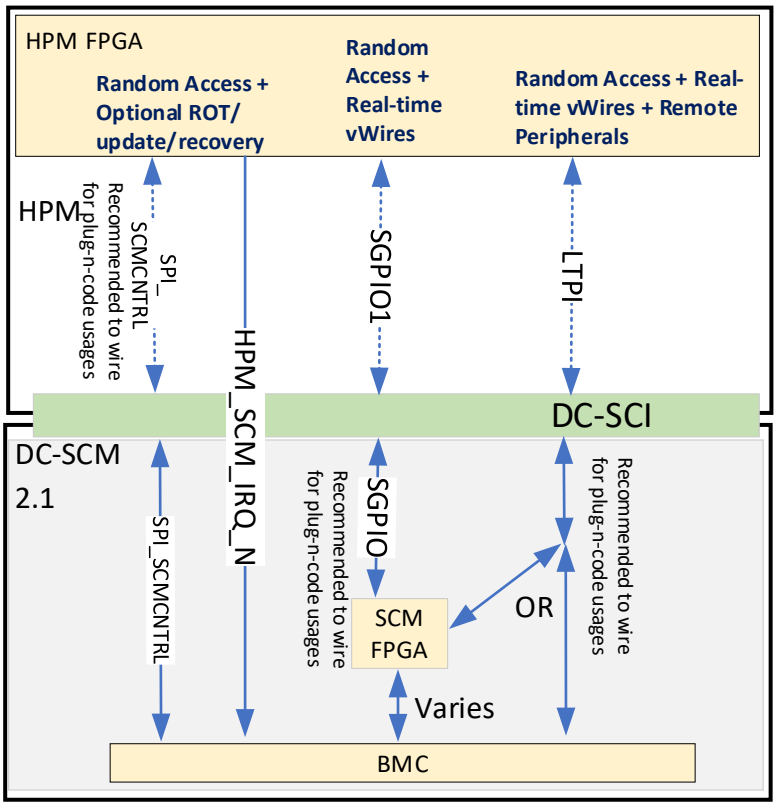
Descriptions:

The DC-SCM diagram shows one example of a method of connectivity to help convey HPM connectivity rationale.

BMC Root Complex to HPM Endpoint Direction:

- If any BMC domain endpoint is supported on the HPM, then the clock must be provided to the end device and DC-SCI.
- If there are no BMC domain PCIe endpoints on the HPM (typical), then REFCLK pins A68-A69 and A33-B34 lanes may be left not connected.
- BMC Domain PCIe endpoints may choose to be in the S0 main power or S5 AUX power domain with clock, PERST# and power state controls left to the implementer. When used, SCM_HPM_PERST# is a tunneled virtual wire and not a discrete signal such as pin B51.
- BMC to host USB-based virtual device connections are not shown.

3.3 SGPIO, LTPI & SPI SCM Control



Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 4. SPI SCM Control, SGPIO, LTPI

Descriptions:

- All HPMs must wire SGPIO OR LTPI between DC-SCI and HPM FPGA. Wiring both busses on the HPM is allowed and is preferred by HPM consumers.
- DC-SCMs are recommended to wire SGPIO AND LTPI to DC-SCI for maximum interoperability.

SPI_SCMCNTRL:

- Potential use cases: Random Access Memory, immutable attestation/update/recovery
- Note that HPM_SCM_IRQ0_N is 1.8V while the rest of the interface is defined as 3.3V. All IRQs may be tunneled over SGPIO1 / LTPI.

SGPIO:

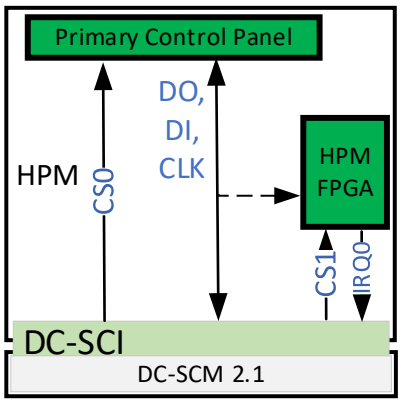
- Potential use cases: small payload, low latency, 100% available, real-time status/control; Random Access Memory
- Preferred to be routed on HPM to ease plug-n-code use.
- DC-SCM is the initiator and the HPM is the target.

- Electrical & timing requirements are in the DC-SCM 2.1 base specification.
- HPMs should target support of >=25MHz, assuming <2.5" of DC-SCM length
- SGPIO payload definition, discovery, compatibility check, and error handling are outside the scope of this hardware design specification.
- If not used on HPM, leave signals no connect.

LTPI:

- Potential use cases: Real-time virtual wires, Random Access memory and select remote peripherals.
- Routed on HPM if the application requires, such as remote peripherals.
- See the DC-SCM 2.1 base and LTPI specifications for electrical, timing and training methods.
- LTPI payload definition, discovery, compatibility check, and error handling are outside the scope of this hardware design specification.
- If not used on HPM, leave signals as no connect.

3.4 SPI SCM Control



Solid lines indicate required connections.
Dashed / dotted lines indicate optional. All diagram colors are arbitrary.

Figure 5. Full SPI SCM Control

Descriptions:

Non-DC-MHS compliant HPMs: Connectivity and usage is undefined.

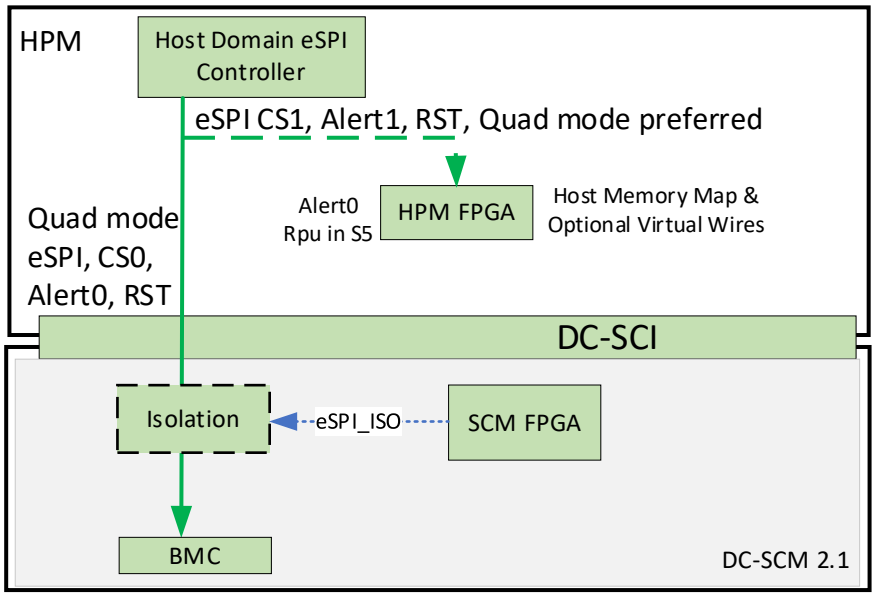
DC-MHS compliant HPMs:

- Controller on DC-SCM
- Required CS0, DO, DI, CLK connection to Primary Control Panel with the shortest routing possible. Target >=12 MHz.

Primary Control Panel (Required) Use Cases: Generic interface for SPI ROM, MCU, bezel, etc. One discrete IRQ and other IRQs tunneled over SGPIO or LTPI.

Connection to HPM FPGA. Target=25 MHz
A stub remover buffer on the Primary Control Panel branch may be needed for optimal signal integrity.

3.5 eSPI



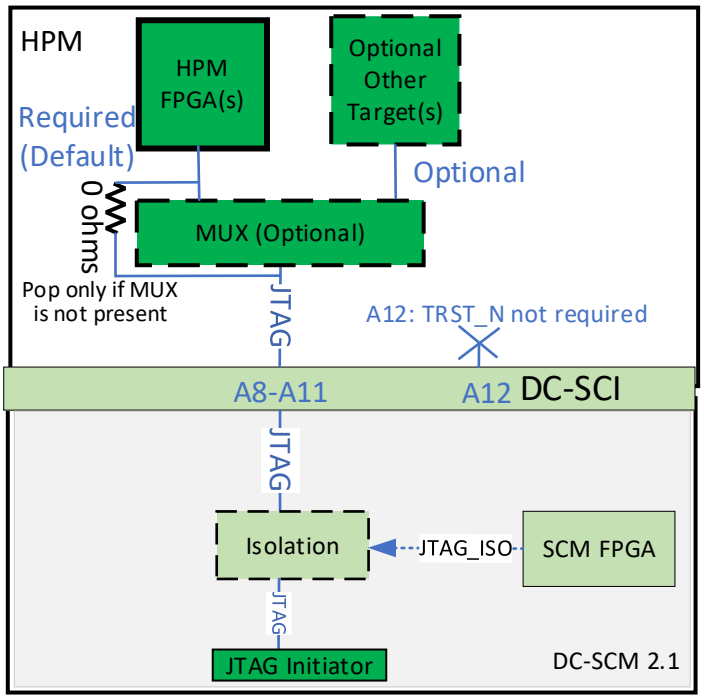
Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 6. eSPI

Descriptions:

- Applies only to CPU hosts that support an eSPI controller.
- Use cases: BIOS/Host memory map & optional virtual wires; Accessible by BIOS via simple I/O read/writes starting in very early POST.
- eSPI CS1 in Quad I/O data mode to HPM FPGA is preferred:
- HPMs without an eSPI host controller must keep eSPI reset asserted into the DC-SCI.
- If BMC SOC eSPI target is electrically well behaved (no pre-S5 voltage bias), then DC-SCM-side isolation logic may be avoided.

3.6 JTAG



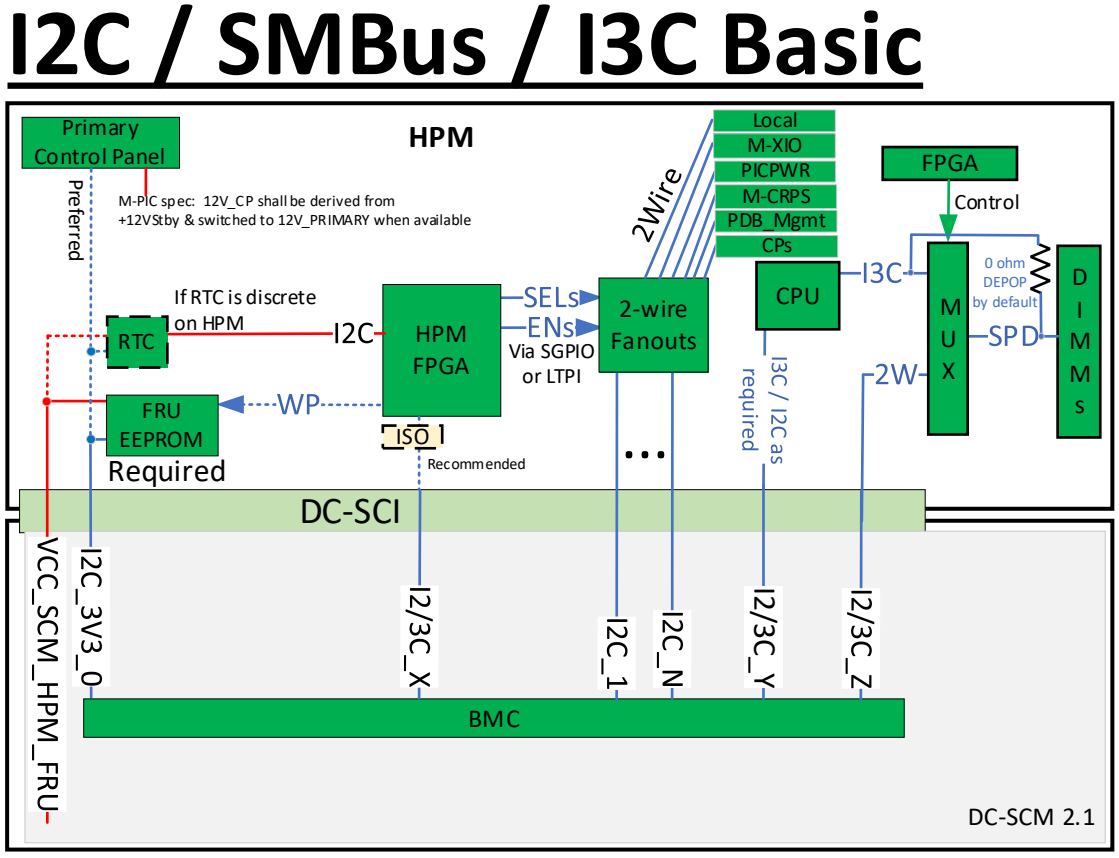
Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 7. JTAG

Descriptions:

- Potential use case: Early HPM Type and FPGA version discovery, DC-SCM-to-HPM FPGA attestation, update, and recovery.
- Required to be connected to HPM FPGA(s).
- Must not connect bus to any optional non-FPGA targets until after the HPM FPGA is operational (SCM_HPM_STBY_RST_N de-asserted).
- Any needed isolation, voltage translation and daisy chaining multiple targets is not shown.
- Pin A12 / TRST_N is not required on a Type 1 HPM. If not used on HPM or DC-SCM, leave as no connect. An alternate GPIO function is not defined for the TRST_N pin.

3.7 I2C, SMBus & I3C Basic



Solid lines indicate required connections. Dashed / dotted lines indicate optional. All diagram colors are arbitrary.

Figure 8. 2-Wire: I2C, SMBus & I3C Basic

Descriptions:

General

- I2C, SMBus, 2Wire terms are used interchangeably.
- All HPM SMBus egresses must be >=100KHz capable, 400KHz preferred.
- All DC-MHS compliant HPM SMBus egresses must default to the 3.3VAUX domain.
- HPM fanout topologies must consider intended traffic patterns to load balance bandwidth across the controllers and minimize nested MUX tiers.
- HPM GPIO-based SMBus MUX EN and SEL controls must utilize SGPIO or LTPI.
- Addressable MUXes are not advised due to cost, security, possible address conflicts and error handling issues.
- Unused DC-SCI traversing 2-wire busses on an HPM may be no connected.
- DC-SCI and HPM egress voltages are defined in the DC-SCI XLS and DC-MHS specifications (including M-PIC, M-XIO, M-CRPS, and OCP NIC 3.0). Ex: M-PIC PDB Management and M-CRPS are 3.3V I2C mode only.

- For any HPM egress that adds I3C support must support defaulting in SMBus 3.3V mode and follow the mode/voltage change flow described in SNIA SFF-TA-1009 and PCI Express Base Specification >= 6.2.
If I3C fanout logic for I/O is used on the HPM, it must assure the HPM capacitance including the egress connector is below 20pf contribution and operate (after downstream negotiation) at 1.8VAUX.

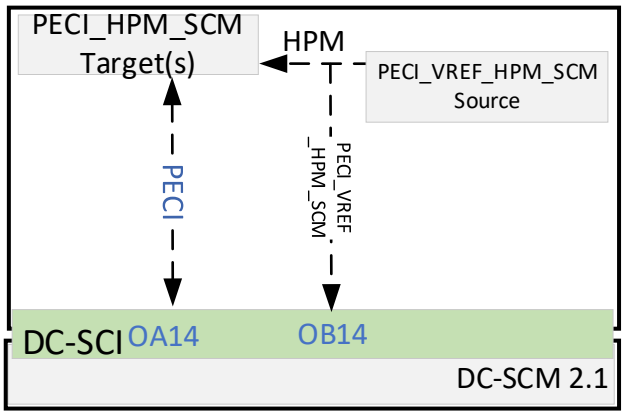
I2C0 Bus:
- All devices must be powered from VCC_SCM_HPM_FRU or have bus isolation.
- HPM FRU EEPROM Write Protect is highly recommended for to be HPM FPGA controlled (default protected).
- If the RTC is located on the HPM, access via I2C0 enables BMC to sync time early. RTC may be inside the BMC in some implementations.
- Extending I2C0 to Primary Control Panel enables relaying user interactions early in the boot sequence.
- No MUX control is enabled on I2C until after the HPM FPGA is operational.

Host Memory:
- Host to DIMMs generally desire I3C mode of operation, often at degraded clock frequency due to high capacitive loading and signal topologies.
- BMC to DIMM connectivity is required via a MUX with 0 ohms between the CPU and DIMMs so a consumer may support only CPU access. If connected, the BMC to DIMM path requires S5 operation and does not require I3C or concurrent / interleaved access support (not a hub). BMC to DIMM use cases include pre-power inventory, PMIC fault isolation, security, optional BMC host runtime ownership.

CPU:
- 2-wire bandwidth per CPU socket must be maximized.
- 1.0V DC-SCI I3C interfaces are recommended for use with CPUs.

I2/3C_X Bus to HPM FPGA:
- Recommended for those wishing to use this path for FPGA attestation, update or random access. Choice of which bus depends on HPM FPGA device capabilities.

3.8 Serial PECI

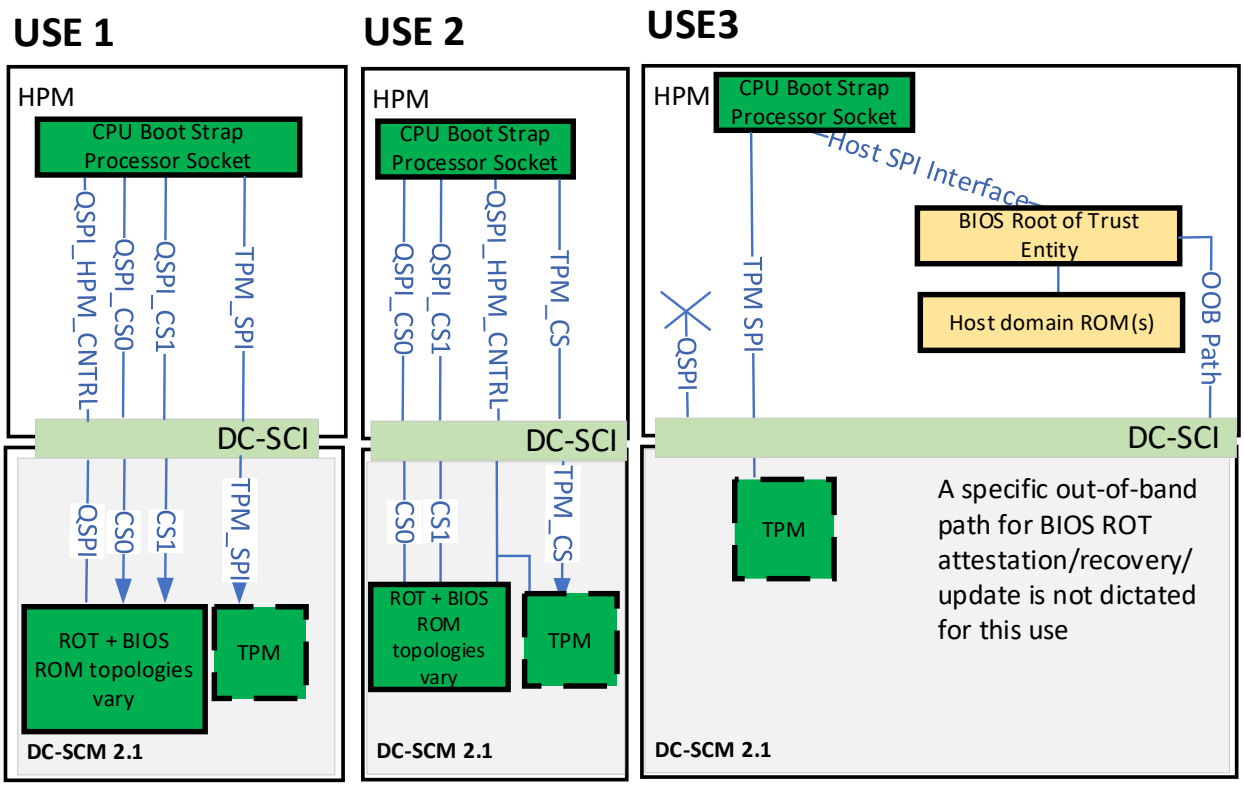


Solid lines indicate required connections. Dashed / dotted lines indicate optional. All diagram colors are arbitrary.

Figure 9. Serial PECI

Descriptions: If Serial PECI is not used, no connect both signals on the HPM.

3.9 QSPI & TPM SPI



Solid lines indicate required connections. Dashed / dotted lines indicate optional. All diagram colors are arbitrary.

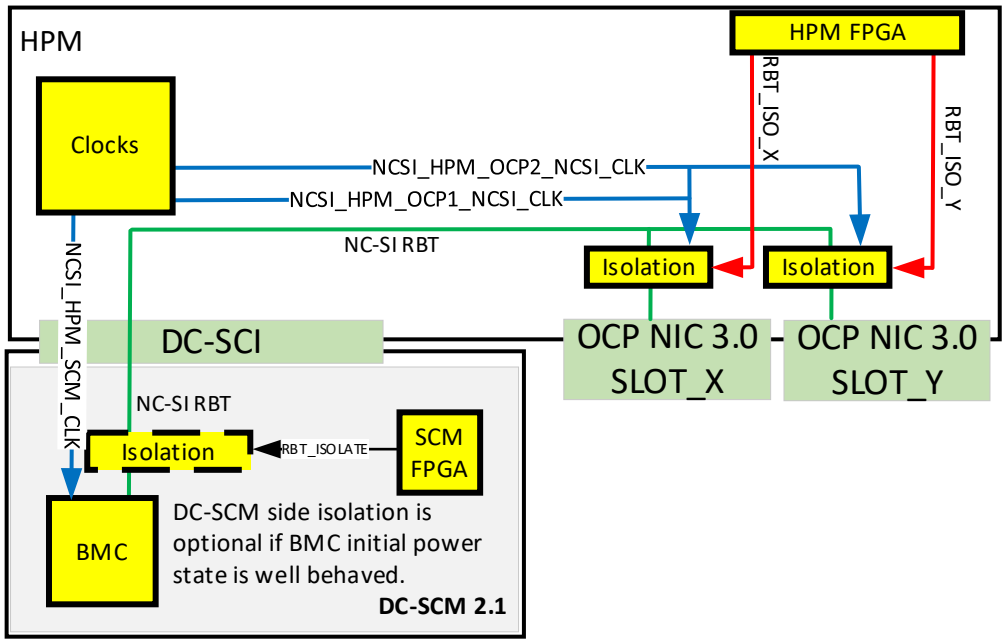
Figure 10. QSPI & TPM SPI

Descriptions:

- Some CPUs support QSPI with 3 CS (2 ROMs & 1 TPM)
- Some CPUs support QSPI with 2 CS (2 ROMs) and a dedicated TPM SPI.
- Any DC-SCM seeking to support both CPU scenarios requires SPI MUX to choose the path for the given HPM Type (not shown).
- TPM IRQ is assumed to be a tunneled virtual wire.

- If an HPM chooses to put the TPM on the HPM (versus rely on the DC-SCM), then it must have an option to be supported via a daughter card due to supply chain logistics with key provisioning. A standard connector, pinout and shape is not standardized currently.

3.10 NC-SI RBT



Solid lines indicate required connections. Dashed / dotted lines indicate optional. All diagram colors are arbitrary.

Figure 11. NC-SI RBT

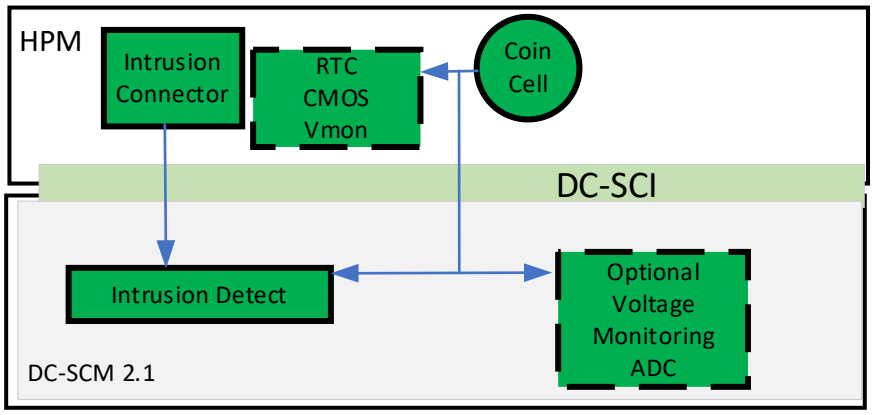
Descriptions:

NC-SI when routed point to point must be <~15". See DC-SCM base specification of routing guidance, length matching, etc.

When routing multi-drop, each slot must utilize a different slot ID strap.

Example is for a platform supporting 2X embedded Small Form Factor OCP NIC 3.0 slots. See respective HPM Base Specification and Design Requirements for slot numbers.

3.11 Intrusion & Coin Cell



Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 12. Intrusion & Coin Cell

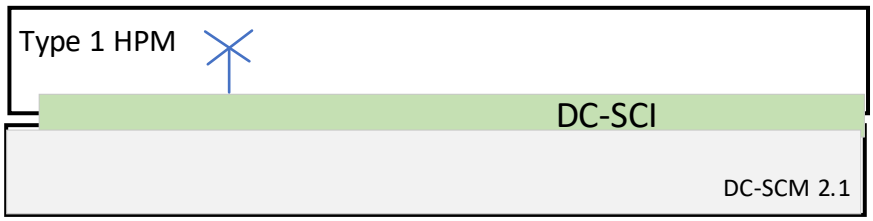
Descriptions:

Coin Cell on HPM. Coin cell battery voltage measurement may be on the HPM or on DC-SCM.

Host RTC and CMOS may be on the HPM or be eSPI or I2C mapped via the DC-SCM BMC.

DC-MHS mandates intrusion connector on HPM with detection logic expected to be on DC-SCM.

3.12 DisplayPort



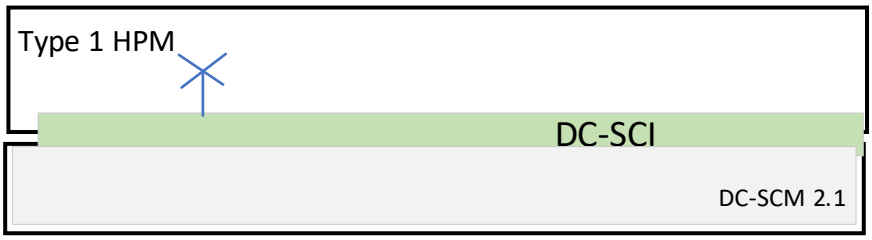
Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 13. DisplayPort

Descriptions:

Not required since DC-MHS M-PIC spec does not define a DisplayPort egress.

3.13 SGMII



Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

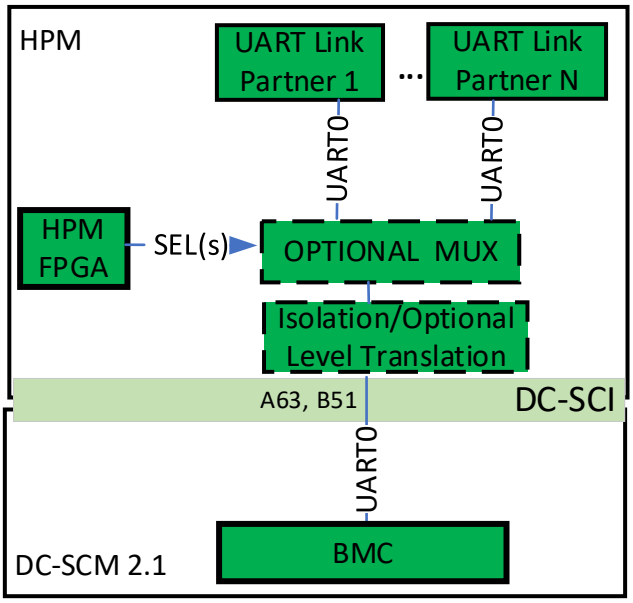
Figure 14. SGMII

Descriptions:

No use case has been identified for Type 1 products.

DC-MHS M-PIC spec does not define an SGMII or Ethernet in/egress.

3.14 UART0



Solid lines indicate required connections. Dashed / dotted lines indicate optional. All diagram colors are arbitrary.

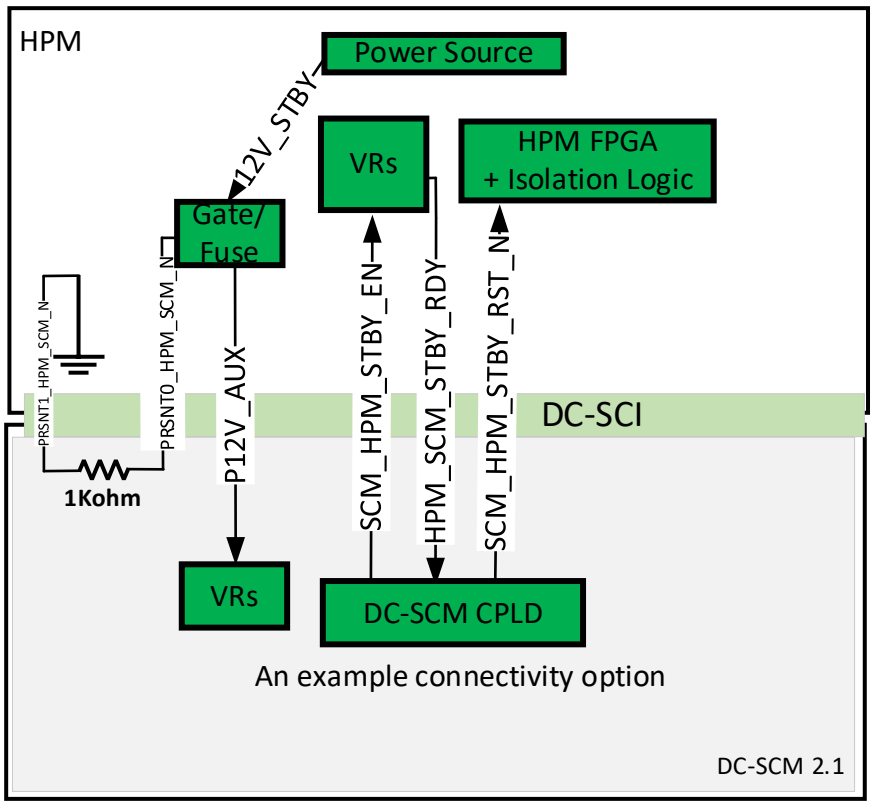
Figure 15. UART0

Descriptions:

- Support: Not required for host COM port usage if eSPI is supported by the host domain unless additional debug consoles/usages are supported. UART1 in the DC-SCI is not supported in this specification.

- When multiple UARTs are needed with mutually exclusive access, a MUX may be used (HPM FPGA controlled). When multiple UARTs need concurrent access, a device such as a USB to multiple UART bridge may be used.
- Isolation: All HPMs most likely need power domain isolation and/or voltage level translation. No isolation is required on the DC-SCI.
- DC-SCM: It is recommended to connect UART0 to the BMC with an RX pullup resistor to avoid a floating input in case of being used with an HPM utilizing UART0. Adherence to the DC-SCI mandated earliest allowed power state of these pins is required.

3.15 Power & Miscellaneous



Solid lines indicate required connections. Dashed / dotted lines indicate optional.
All diagram colors are arbitrary.

Figure 16. Power & Miscellaneous

Descriptions:

- Presence loop ensures card is fully seated before enabling 12VSTBY power. When not seated, P12V_AUX must be removed from the DC-SCM.
- SCM_HPM_STBY_EN: Enables AUX loads on HPM, such as +3.3VAUX.

- HPM_SCM_STBY_RDY: Indication to DC-SCM that HPM AUX rails are within operating ranges. Must not be driven by HPM FPGA logic.

- SCM_HPM_STBY_RST_N: If HPM FPGA is not self-attesting, this signal must be used to allow HPM FPGA to run user logic (e.g., INIT_N).
    - Use case is for DC-SCM to attest the HPM FPGA before use.
    - May be used to enable specific HPM isolation logic.

4. Non-DC-SCI-related HPM Interfaces

4.1 HPM-to-Embedded OCP NIC 3.0 Slot(s)

Must Support:
- ID MODE; AUX Mode; MAIN MODE, NC-SI with RBT-Isolate
- Discrete connections of PRSNTB[3:0]# to HPM FPGA
- NIC_PG connected to HPM FPGA
- Slot ID [1:0] = 00b for left most (external view) slot and 01b if 2nd right side embedded OCP NIC Slot exists.
- Hotplug controllers are required on edge rails with separate enables and PGs connected to HPM FPGA. Provision for 0 ohm wire around and depopulation of HPC logic is permissible.

Recommended Connection: Managed USB
Not supported: Scan Chain

4.2 HPM-to-Embedded M-CRPS Slot(s)

- PS_EN – 6-state mode as of M-CRPS 1.04
- PMBUS – No multi-drop.
- Simple Presence on DSSI pin to HPM FPGA for optional DSSI enablement

4.3 HPM-to-Control Panels

- See DC-MHS, M-PIC specification for required connections.

4.4 HPM-to-M-XIO

- See DC-MHS, M-XIO specification.
- See PCI Express Base Specification 6.2

4.5 HPM-to-PICPWR

- See DC-MHS, M-PIC specification.

4.6 HPM-to-PDB Management

- I2C for M-CRPS and local PDB Management (e.g., CPLD update and memory map)
- SGPIO
- Full Power Cycle support
- VMon (voltage monitor)

4.7 HPM-to-Boot Subsystem

- See DC-MHS, M-PIC specification.