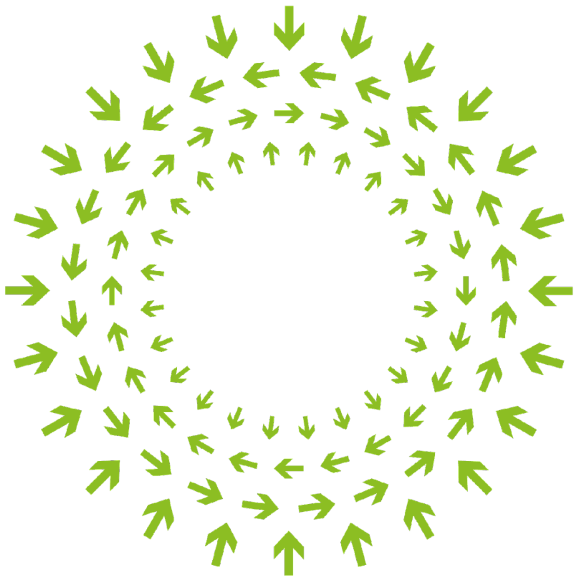


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# Datacenter Secure Control Module Specification (DC-SCM) Rev2.1 Ver 1.1 Errata

1.0.0

Author: Kasper Wszolek, Intel Corporation

## Version History

Note, refer to the OCP Contribution Versions, Revisions and Errata best practices documentation. Generally speaking, Versions and revisions are made to this document and logged here. Errata is a separate document such that the contribution specification document it refers to was not revised. Ex: Version 1, Errata E1

| Date | Version # | Author | Description |
|---|---|---|---|
| October 28, 2024 | 1.0.0 | Kasper Wszolek (Intel Corporation) | Add clarification regarding SFF-TA-1002 Rev1.5 compliance with DC-SCM 2.1 |
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## Current Template Version:

**Specification Errata Template v1.0.0**

Effective January 2024

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# 2. Acknowledgements

N/A

# 3. Scope

The purpose of this Errata document is to provide corrections to the following document:

*Datacenter Secure Control Module (DC-SCM) R2 Specification Rev2.1 Ver 1.1*

# 4. Errata

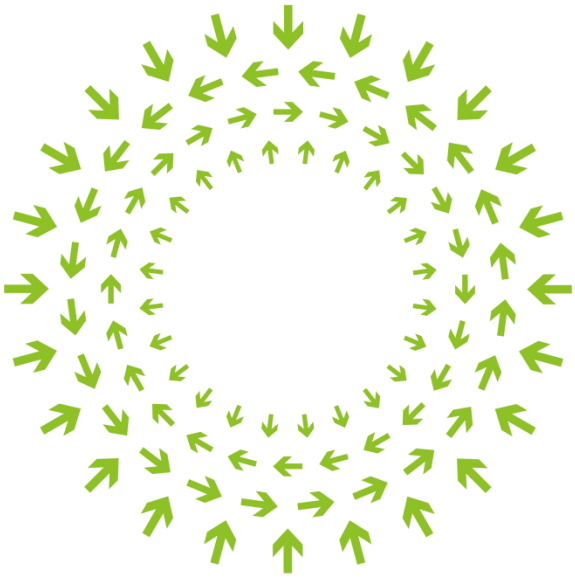
## 4.1. Issue 1

SNIA SFF-TA-1002 Rev 1.5 introduced new definitions of connector Types i.e., Type 1 and Type 2. Only SFF-TA-1002 Type 1 connector is compliant with the DC-SCM R2 specification. Type 2 connector is not compliant with the DC-SCM R2 specification and should not be used with DC-SCM R2 implementations. The DC-SCM R2 Specification shall update all references to SFF-TA-1002 to SFF-TA-1002 Type 1. All the references to SFF-TA-1002 that need to be updated are listed in Table 1.

*Table 1 List of updated to SFF-TA-1002 in the DC-SCM Rev2.1 Ver 1.1*

| Chapter | Current | Updated |
|---|---|---|
| 2.1 General Overview | N/A – new note to be added at the end of the “2.1 General Overview” chapter | Note: *SNIA SFF-TA-1002 Rev 1.5 introduced new definitions of connector Types i.e., Type 1 and Type 2. Only SFF-TA-1002 Type 1 connector is compliant with the DC-SCM R2 specification.* |
| 2.2 Horizontal Form Factor | The connector is defined to be an SFF-TA-1002 compliant 4C+ connector. | The connector is defined to be an SFF-TA-1002 Type 1 compliant 4C+ connector. |
| 3.1 DC-SCI Card Edge Connector Definition | The DC-SCI card edge connector interface is compliant to the SFF-TA-1002 specification with respect to the 4C+ connector size. | The DC-SCI card edge connector interface is compliant to the SFF-TA-1002 Type 1 specification with respect to the 4C+ connector size (Note that DC-SCI is not compliant with SFF-TA-1002 Type 2 connector and it shall not be |

| | | |
|---|---|---|
| | | used with DC-SCM applications). |
| 3.3 HPM Connector Definition | The mating connector on the HPM is mechanically compliant to the 4C+ connector as defined in the SFF-TA-1002 specification for right angle, straddle mount and vertical form factor connectors. | The mating connector on the HPM is mechanically compliant to the 4C+ connector as defined in the SFF-TA-1002 Type 1 specification for right angle, straddle mount and vertical form factor connectors. |



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# Datacenter Secure Control Module Specification (DC-SCM)

**Revision 2.1, Version 1.1**
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# Revision History

| Revision | Version | Date | Notes |
|---|---|---|---|
| **1.0** | 0.8 | Nov 9, 2020 | Initial public review |
| | 0.95 | Dec 2, 2020 | Feedback implemented |
| | 1.0 | March 11, 2021 | Removed ESPI_CS1_N and replaced with RSVD3<br>Figs 3, 4, 5, 6 – updated.<br>Table 3 – updated.<br>Table 22 - SPARE [0:1] desc<br>Figure 22 - updated to initiator/Responder, Table 27: I3C pull-up updated to STBY/MAIN<br>Section 6 - platform interop wording edit<br>Sec 2.2.3 – typo (FFF> HFF) |
| **2.0** | | Dec 31, 2020 | OCP DC-SCM 2.0 initial public review using DC-SCM 0.8 as base |
| | | July 2021 | DC-SCM 2.0 updates using DC-SCM1.0 as base |
| | | Sept 2021 | Updates from working group decisions |
| | 0.5 | Oct 2021 | Implement 0.95 pinout descriptions |
| | 0.51 | Oct 2021 | LTPI details |
| | 0.52 | Nov 9, 2021 | General updates and fixes in the document.<br>Section 2 - Mechanical: HFF dimensions diagram updated with connector shift and notches updated.<br>LTPI: Link Initialization, Training and Configuration details added. Incorporated feedback from v0.51 review |
| | 0.53 | Nov 20, 2021 | Updates based on feedback. Added a note that VFF will be defined in a later version of the spec. |
| | 0.7 | Nov 23, 2021 | 0.7 release |
| | 0.9 | Apr 4, 2022 | Extracted LTPI chapter to standalone specification. Cleanup.<br>Revised to I3C Basic 1.1.1<br>Added detailed mechanical drawings |
| | 0.95 | Apr 25, 2022 | Incorporated 0.9 feedback |
| | 0.96 | May 6, 2022 | Feedback from 0.95, minor clean up |
| | 0.97 | June 3, 2022 | Minor clean up |

| | | | |
|---|---|---|---|
| | | | Clarification around I2C, I3C, FSI<br>Add PRoT in discovery sequence.<br>Add S5 and lower power state recommendation.<br>Add EFF Rail dimensions |
| | 1.0 | July 27, 2022 | 1.0 release |
| **2.1** | 1.0 | Oct 2023 | Figure 2 - add 2 x TPM in dual node diagram.<br>Figure 4 - add chamfer dimensions.<br>Figure 5 - added dims for bottom standoff translational KOZs.<br>Section 2.3 - added Vertical Form Factor information section.<br>Section 3.4 - replaced the DC-SCI Pinout summary table with the pinout diagrams for Single and Dual Node.<br>Section 3.5.3 – update dual node SPI TPM description.<br>Section 3.5.14 - added reference to the IEEE 1149.1 for the JTAG signals direction and naming.<br>Added note on DC-SCI 2.1 change related to JTAG.<br>3.5.15 - relaxing early power state requirement<br>Table 19 - FRU requirement clarifications, removed 32 bytes for OEM, OEM FRU begins at byte 32 if used.<br>Remove Pre-S5 terminology, replaced with STBY to match the DC-SCI spreadsheet.<br>3.5.15.1 – added SGPIO Timing Requirements as specified in M-PIC specification.<br>6.1 – Table 19, add offset 16 HPM Vendor ID<br>add offset 18 HPM Device ID |
| **2.1** | 1.1 | Nov 2023 | Update DC-SCM 2.0 reference to 2.<br>Fix missing page numbers.<br>Fix incorrect Table numbering.<br>2.1 – removed LTPI introduction<br>3.5.7 – removed I3C reference to MIPI spec<br>Table 19 – FRU definition: change all offsets to hex format.<br>Update Record Format Version to 0001 for DC-SCM 2.1<br>LTPI Rev: add Least supported Revision<br>LTPI Ver: add Least supported Version<br>Section 6 first paragraph wording updated.<br>Mechanical section updates with reference to the optional handle dimensions, improved wording for the IFF module definition, and definitions for the chassis opening and I/O region. |
| | | April 2024 | Section 3.5.6 LTPI voltage bias clarification.<br>Figure 59 – changed to an example implementation.<br>Table 4 – added LVDS Rtt recommendations. |
| | | May 2024 | Section 5.1 – remove duplicate information from the OCP NIC specification. Update to reflect DC-SCM only timing requirements.<br>Section 3.5.9.2 – Added notes for USB termination recommendations. |
| | | June 2024 | Table 12 - HPM_STBY_RDY signal clarification, guidance for system using this signal for FPGA readiness. |

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# Acknowledgement

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback of over 150 individuals from 28 different companies.

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- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 4.0, September 2nd, 2019
- SMBus Management Interface Forum. System Management Bus (SMBus) Specification. System Management Interface Forum, Inc, Version 2.0, August 3rd, 2000
- USB Implementers Forum. Universal Serial Bus Specification, Revision 2.0, April 27th, 2000
- DMTF Standard. DSP0222, Network Controller Sideband Interface (NC-SI) Specification. Distributed Management Task Force (DMTF), Rev 1.2.0b, August 4th, 2020.
- MIPI alliance Specification for I3C Basic$^{SM}$ Version 1.1.1. – Released July 2021
- OCP NIC 3.0 Design Specification Version 1.0.9
- OCP DC-SCM 2.1 LVDS Tunneling Protocol and Interface (LTPI) Specification 1.1


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# 1 Overview

This specification provides details for the design features needed to create a Datacenter-ready Secure Control Module (DC-SCM) with a standardized Datacenter-ready Secure Control Interface (DC-SCI). It moves common server management, security, and control features from a typical processor motherboard architecture onto a smaller common form factor module. This module contains all the FW states previously housed on a typical processor motherboard. This provides benefits to both the user and developer.

This document does not prescribe design details that are not essential to the electrical compatibility of the connector interface. Examples are used throughout this document for explaining potential use case, not as requirements of the module or the coupled Host Processor Module design.

From a Data Center perspective, this enables common management and security to be deployed across a higher percentage of platforms. It also enables deployment of management and security upgrades on platforms within a generation without redesigning more complex components.

From a development perspective, this enables a solution provider to remove customer specific solutions from the more complex components (such as motherboards). This enables greater leverage of higher complexity components across platforms.

For the purposes of this specification, to clarify terminology, we introduce the following module definitions:

- HPM – Host Processor Module. This refers to any processing module to be managed by an SCM. In simplest terms, this is the traditional CPU-memory complex but with the BMC and Security moved to the SCM. The HPM is not limited to standard processor architecture and can apply to any architecture utilizing management and security features
- HPM FPGA – Host Processor Module FPGA. This refers to a programmable device on the HPM. Main functions include system power/reset control as well as serializing/de-serializing several IOs between the HPM and BMC
- DC-SCM – The Datacenter - Secure Control Module. The DC-SCM is designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center
- DC-SCI – The Datacenter - Secure Control Interface refers to the connector interface between the DC-SCM and the HPM

A typical DC-SCM design enables the design and deployment of a Host Processing Module (HPM) complex to become a simpler exercise with increased efficiency for time to market deployment. With a standardized DC-SCI pinout and definition, the DC-SCM can be used as a vehicle to drive common boot, monitoring, control, and remote debug for diverse platforms.

The goal of this revision is to allow for future scalability and longevity across a few generations of server platforms. It considers that server platforms will drop support for some of legacy requirements in favor of new use cases such as Multi Node support and new manageability solutions based on high-speed interfaces. This requires the DC-SCM spec to allow more flexibility in interface usage and pinout definition. Thus, we introduced LVDS Tunneling Protocol & Interface (LTPI).

## 1.1 DC-SCM Architecture

For the purposes of this specification, the DC-SCM architecture is assumed to consist of the following primary elements:

- BMC – The Baseboard Management Controller is a specialized service processor that monitors the physical state of server
- BMC Flash – One or more flash devices used to contain the BMC firmware image
- BIOS Flash – One or more flash devices used to contain the BIOS firmware image for each node
- DC-SCM CPLD – A programmable logic device that contains application specific logic and optional LTPI interface
- RoT Security Processor – An optional security processor responsible for attesting the BMC, BIOS and/or other firmware images on the system
- TPM – Trusted Platform Module – An optional dedicated chip or module designed to secure hardware through integrated cryptographic keys

An example block diagram demonstrating an example architectural building blocks of a DC-SCM is shown in
Figure 1. Note that some of these interfaces are mutually exclusive with others.

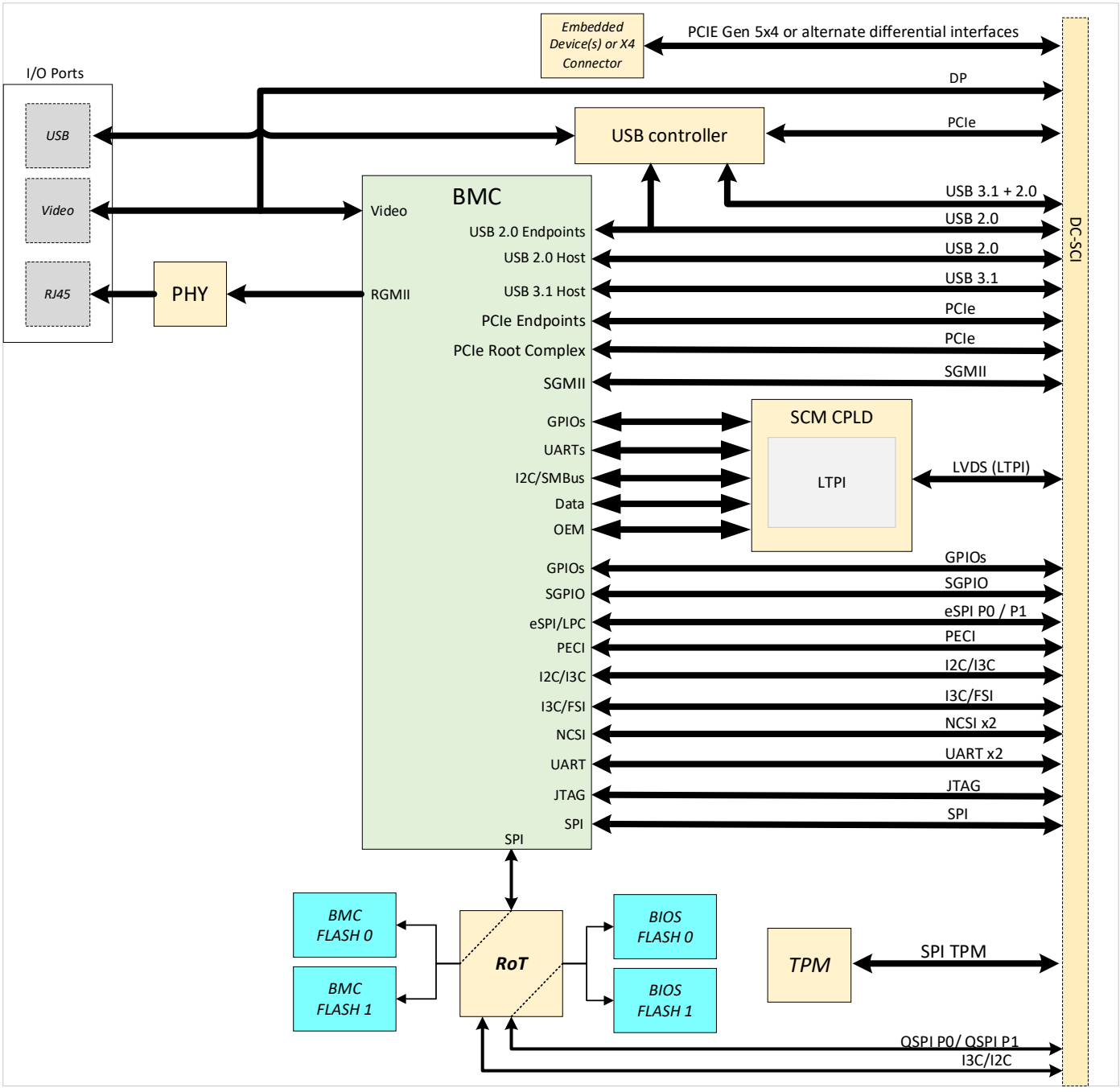



**Figure 1: DC-SCM Example Block Diagram**

## 1.2 Multi-Node Support

The long-term goal is to enable the ability to support more than two independent nodes using a single OCP DC-SCM module. This revision of the specification will focus on the single-node and dual-node pin definitions. In this version of the dual-node pin definition, the signals are arranged to expand as the number of nodes supported by the system. This is achieved by

consolidating various low speed interfaces over the LTPI connection and making pins available for additional interfaces, such as PCIe, ESPI and SPI, which are dedicated to each socket. Note that the following diagram is general connectivity options and not indicative of existing capabilities (such as BMCs with dual eSPI).

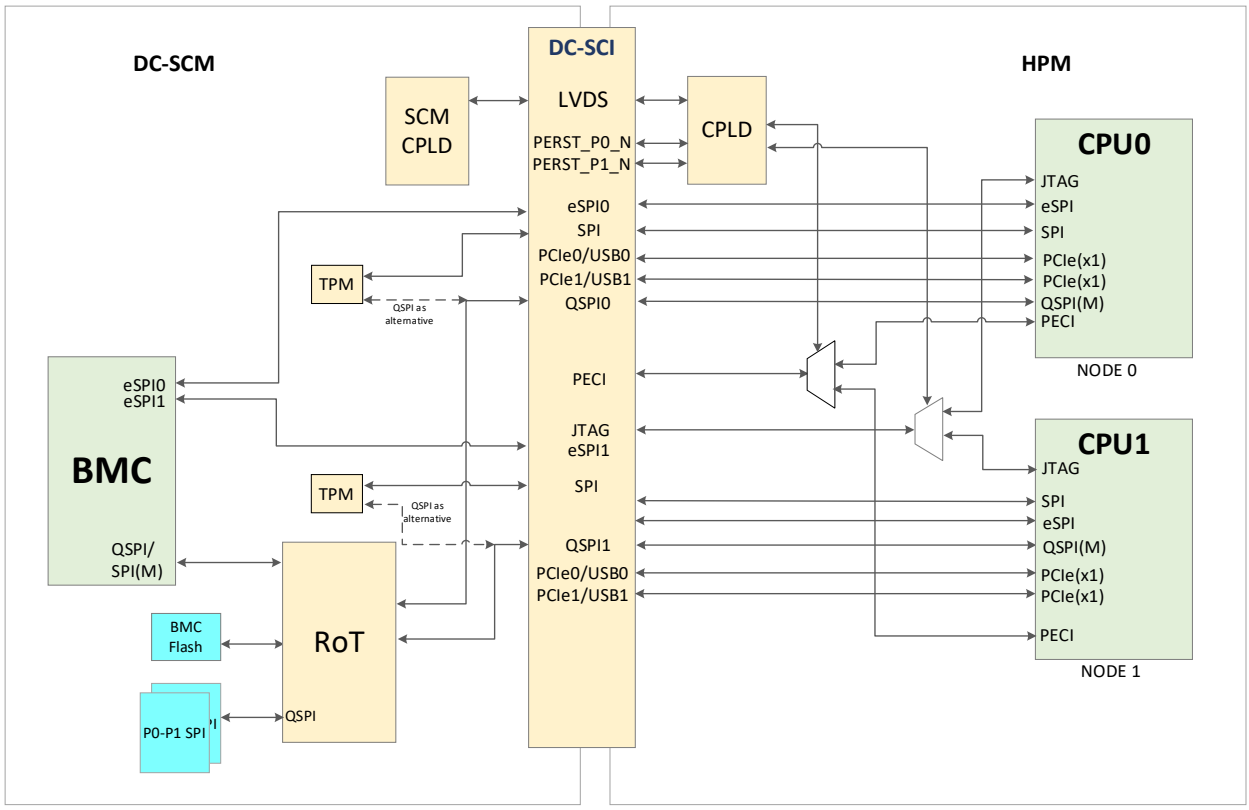



**Figure 2: Dual-Node Example Block Diagram**

# 2 Mechanical Form Factors

## 2.1 General Overview

The OCP DC-SCM 2.1 features horizontal and vertical form factors to provide flexibility to server designers.
The corresponding DC-SCI is intended to support all form factors of OCP DC-SCM; however, many of the block diagrams and descriptions contained in this specification are based on the horizontal external form factor (EFF) and may not demonstrate the cabling requirements of the horizontal internal form factor (IFF).
All mechanical board assemblies shall meet the safety requirements described in Section 7.

## 2.2 Horizontal Form Factor

The OCP DC-SCM 2 horizontal form factor (HFF) is similar to the OCP NIC 3.0 form factor with alterations to the connector interface and to the physical size to accommodate typical DC-SCM circuit requirements and ensure mechanical incompatibility between DC-SCM and OCP NIC. The HFF is physically longer and wider than the OCP NIC 3.0, ensuring that the OCP DC-SCM 2 HFF cannot mate into an OCP NIC 3.0 slot. It also has a **3.25 mm shift** in the card edge key slot geometry to ensure an OCP NIC 3.0 module nor a DC-SCM 1.0 module can mate into an OCP DC-SCM 2 HFF slot and connect electrically. The connector is defined to be an SFF-TA-1002 compliant 4C+ connector. The 4C+ connector is a 4C compliant connector with an additional 28-pin “OCP bay” defined in the OCP NIC 3.0 specification.
To achieve the features outlined in this specification, OCP DC-SCM 2 compliant cards are not backwards compatible with OCP DC-SCM 1.0 cards.
This specification considers two form factors for OCP DC-SCM 2 HFF:

- External Form Factor (EFF) – this form factor is intended for use in servers where the OCP DC-SCM 2 HFF is installed in a coplanar fashion, at the front of the server with direct interface to the front server bezel, or at the rear wall of the server. When installed at the front, standard front panel interfaces are contained on the OCP DC-SCM 2 HFF and may or may not require cables. See Section 2.2.2 for more information.
- Internal Form Factor (IFF) – this form factor is intended for use in servers in which the OCP DC-SCM 2 HFF is embedded internally to the server without direct interface to a server front or rear, or in the case of an externally assembled OCP DC-SCM 2 HFF that employs the use of an internal latching mechanism. In these applications, valid implementations include (A) interconnects located at the faceplate, and (B) cabled interconnects, or a combination of both. In this application, external interfaces such as fan control and front panel require cabled interconnects. The overall dimensions of the form factor are identical to the EFF, although there are some modifications for usage of internal features. See Section 2.2.2 for more information.

### 2.2.1 HFF Board Dimensions and Keep-out Zones

The PCB form factor overall dimensions are shown in Figure 3. It has a thickness of 1.57 mm. There are slots on the sides to enable the IFF version with interfacing rail features to secure the module in place.

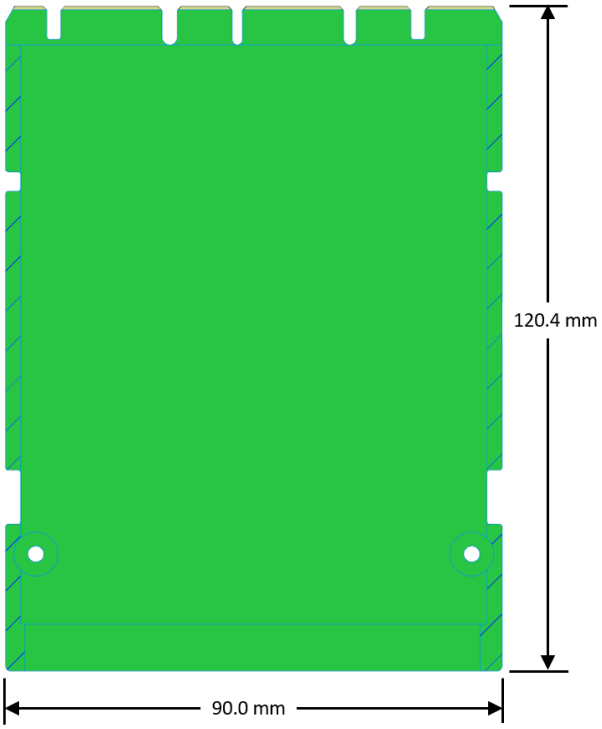



**Figure 3: HFF Form Factor Board Overall Dimensions**

The top-side board dimensions, along with corresponding detail views and Keep-out Zones (KOZs), are shown below in Figure 4. The bottom side dimensions, detail views, and KOZs are illustrated in Figure 5. The side dimensions and KOZs are depicted in Figure 6.

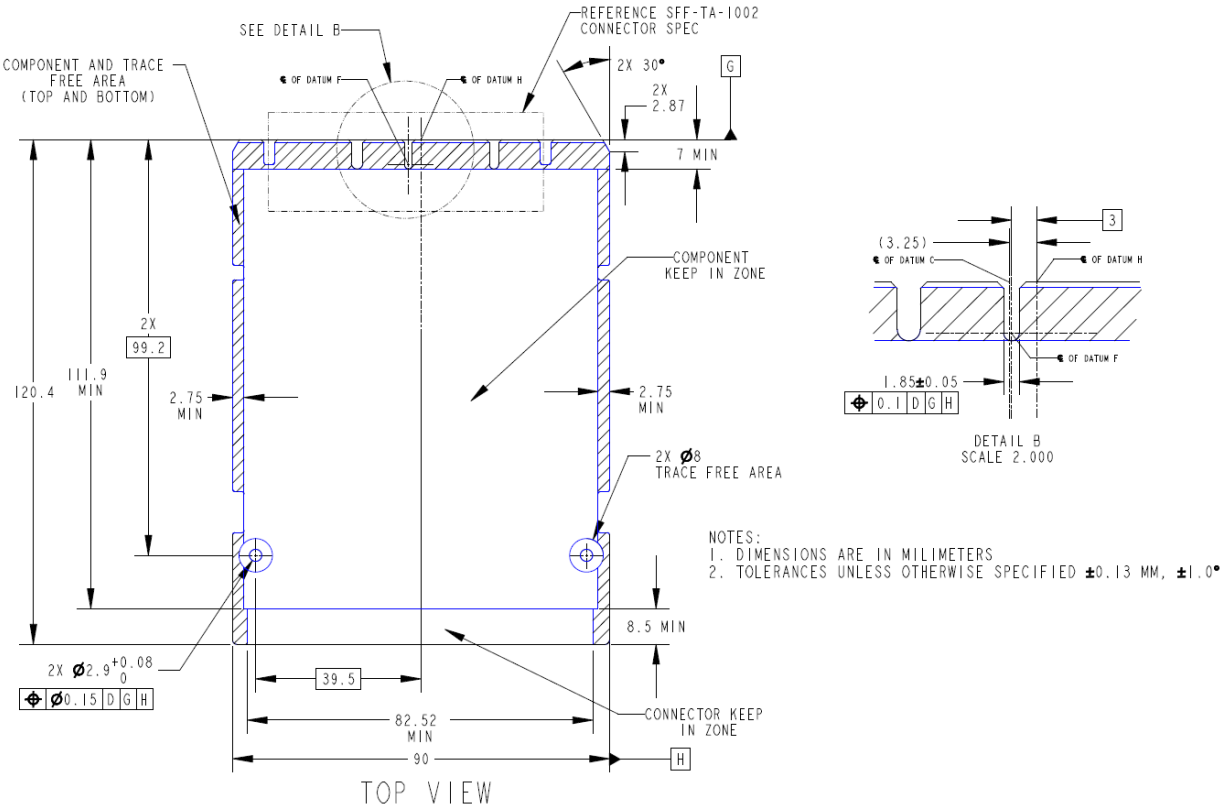



**Figure 4: HFF Board Dimensions and Keep-out Zones – Top View**

The OCP DC-SCM 2 HFF board outline provides features to lock the board into the chassis that are the same as the OCP NIC 3.0 board. This is accomplished with two small notches – one on each board side edge to provide flexible configurations to baseboard vendors. A baseboard may choose to use one or both notches for the internal locking mechanism. If a locking feature is implemented on the baseboard, the OCP DC-SCM 2 board may only be inserted or removed after actuating the internal locking mechanism. The PCB retention notches are compatible with all chassis implementations. Please refer to the board dimensions in Figure 5, Detail D for details.

There are also two additional side notches, wider than the aforementioned internal lock notches, that provide a means to retain the module when the OCP DC-SCM 2 and baseboard are assembled together on a tray prior to assembly into the chassis. These notches are illustrated in Figure 5, Detail C. The guide rails will have hook/slot features that interface in these areas. If these features are utilized, they may also serve as a locking mechanism to prevent module removal externally.

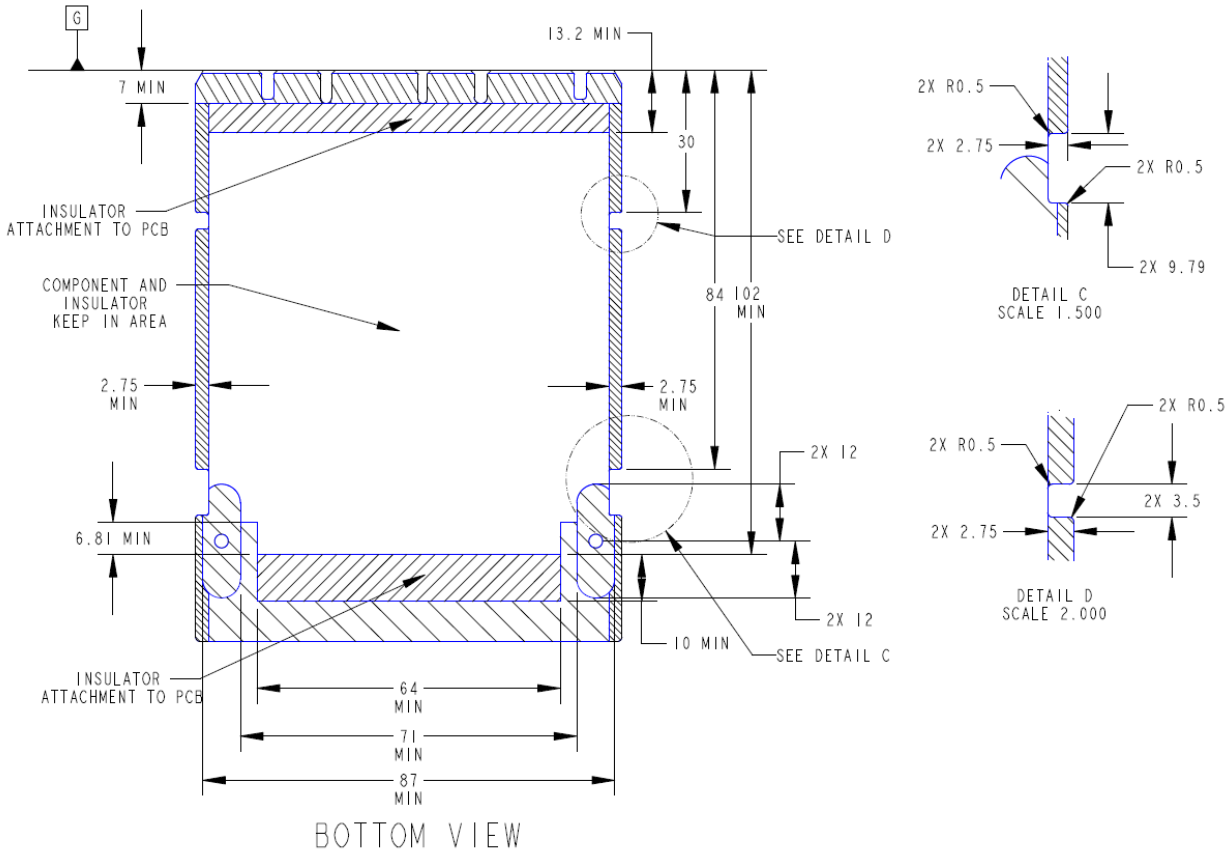



**Figure 5: HFF Board Dimensions and Keep-out Zones – Bottom View**

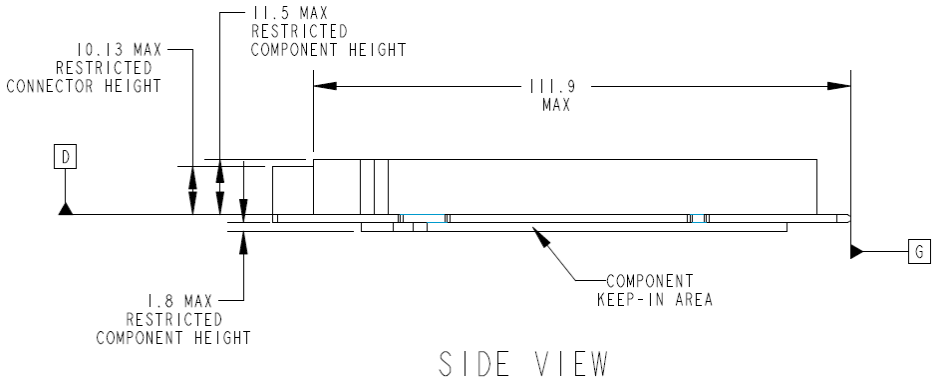



**Figure 6: HFF Board Dimensions and Keep-out Zones – Side View**

For the IFF version of the board, there is an option to include a vertical rear handle to aid with insertion and extraction of the module. Figure 7 shows the dimensions and modified KOZs for the board top and bottom sides. To see the optional handle in an installed state on an IFF module, please see Figure 15.

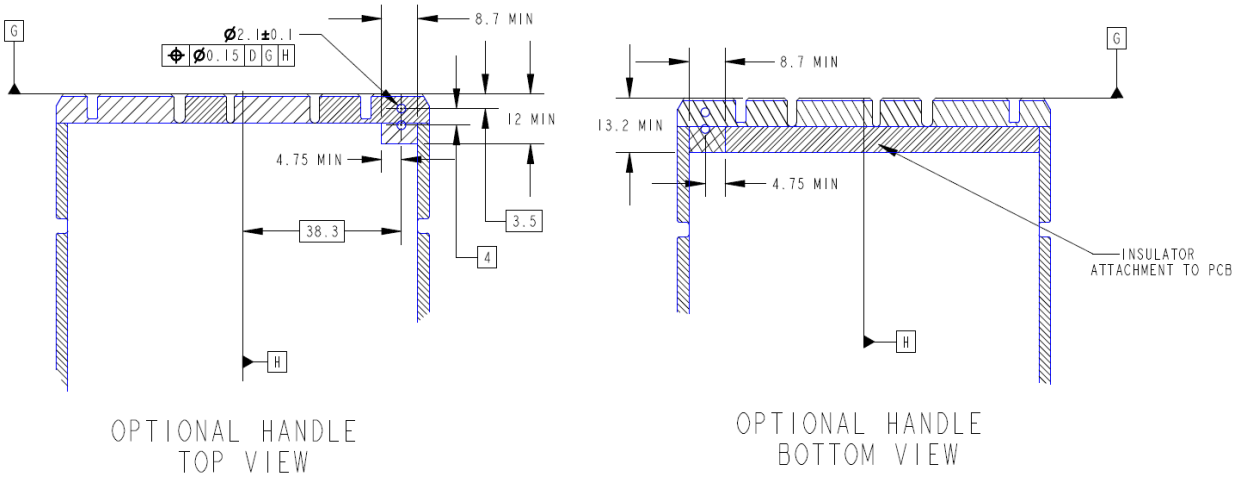



**Figure 7: IFF Dimensions and KOZs for Optional Handle - Top/Bottom Views**

### 2.2.2 HFF External Form Factor

The External Form Factor (EFF) is defined for usage at the front or rear of a chassis and is externally inserted or extracted. Much like the OCP NIC 3.0 module, it has a pull tab and a securing captive fastener on either side of the faceplate bracket for aiding in the chassis assembly.

There are two options for an EMI compliance solution. Option one utilizes metal finger stock that is attached to all sides of the faceplate and interface to the chassis bay opening flanges for contact. Option two takes advantage of Fabric-over-Foam (FoF) components attached to all four sides to make continuous contact with the chassis bay opening flange walls.

Option 1 Option 2

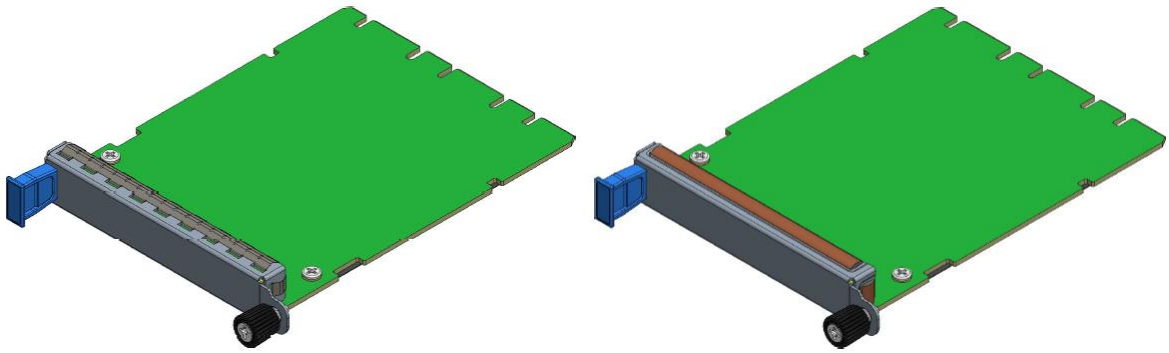


**Figure 8: EFF Module Options - ISO Views**

Exploded views of each corresponding module assembly are shown in Figure 9.

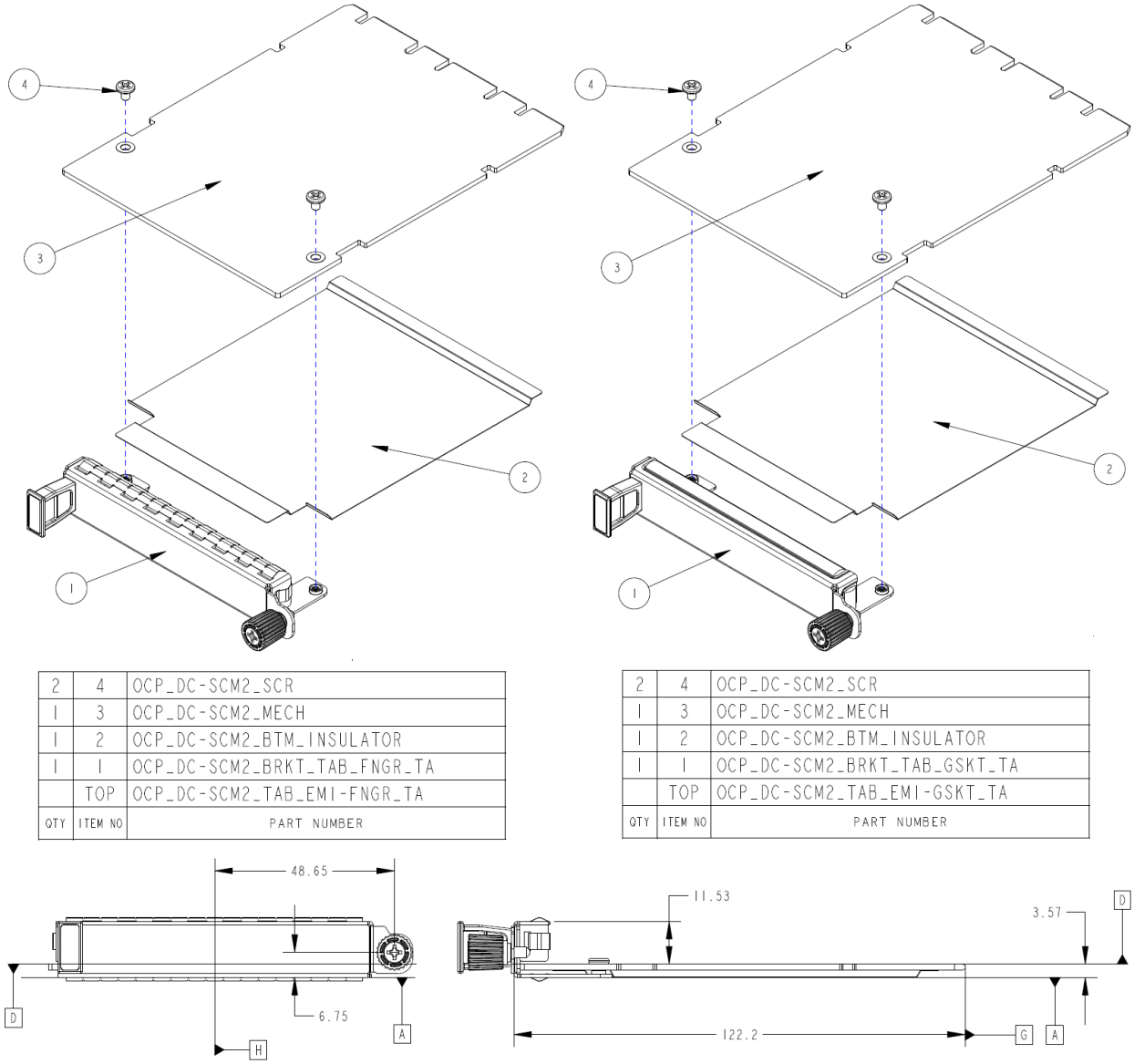


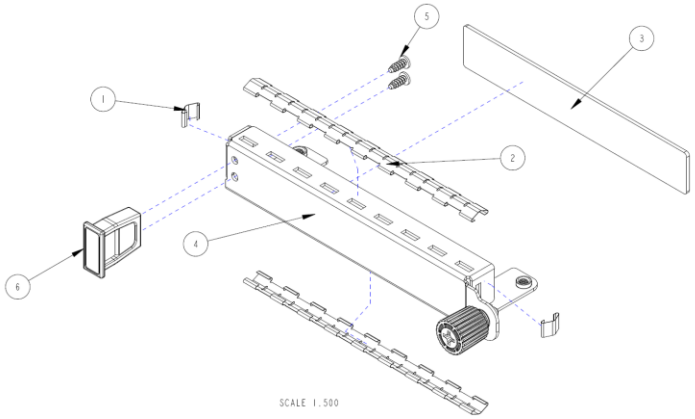

**Figure 9: EFF Module Assemblies – Exploded ISO and Orthographic Views**

### 2.2.2.1 EFF Faceplate Bracket Subassembly

The EFF module supports a front I/O bracket, or faceplate, that enables front I/O access and a securing method of the OCP DC-SCM 2 to the chassis. Each option has the same overall features and dimensions, except for where the EMI solution is attached. Exploded views of the different bracket assemblies are shown below in Figure 10 and Figure 11. The general faceplate dimensions are shown in Figure 12.

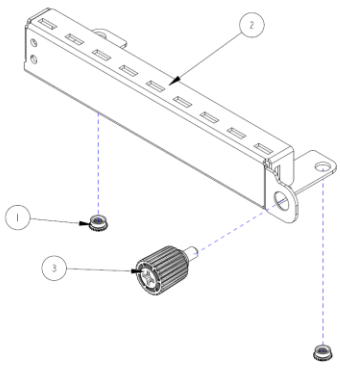
Faceplate connector cut-outs and perforations are excluded from the figures and may be customized per system configuration and system airflow requirements. Where space is permitted on the faceplate, vents sized to a maximum of 3.0 x 3.0 mm, or round vents with a maximum diameter of 3 mm, may be added to help optimize airflow while maintaining the integrity of the

faceplate structure. The OCP DC-SCM 2 card supplier may add port identification markings on the faceplate assembly that meet their manufacturing and customer requirements.
Depending on the OCP DC-SCM 2 card implementation, I/O connectors may be placed anywhere within the allowable connector keep-in regions as defined by the PCB mechanical drawings and faceplate drawings of Section 2.2.1 and Section 2.2.2.1.
Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers.




| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 1 | 6 | SOUTHCO_CN-99-459 | |
| 2 | 5 | OCP_DC-SCM2_EJTR-HNDL_SCR | |
| 1 | 4 | OCP_DC-SCM2_BRKT_TAB_FNGR_ASSY | |
| 1 | 3 | OCP_DC-SCM2_BRKT_GSKT_CONN | |
| 2 | 2 | OCP_DC-SCM2_BRKT_EMI_FNGR_9F | |
| 2 | 1 | OCP_DC-SCM2_BRKT_EMI_FNGR_1F | |
| | TOP | OCP_DC-SCM2_BRKT_TAB_FNGR_TA | |

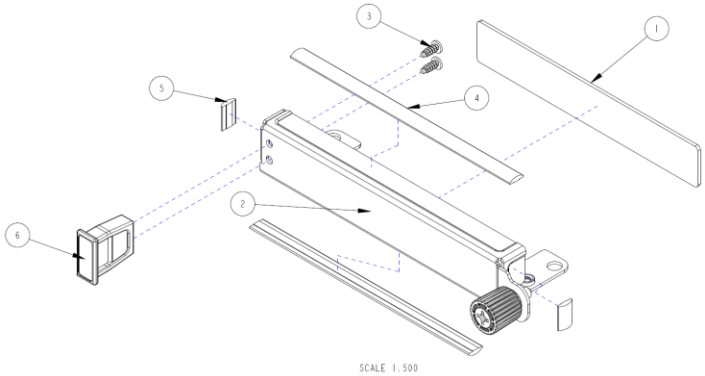
PARTS LIST




| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 1 | 3 | SOUTHCO_4C-99-343-KEEE | |
| 1 | 2 | OCP_DC-SCM2_BRKT_TAB_EMI-FNGR | |
| 2 | 1 | OCP_DC-SCM2_BRKT_STDOFF | |
| | TOP | OCP_DC-SCM2_BRKT_TAB_FNGR_ASSY | |

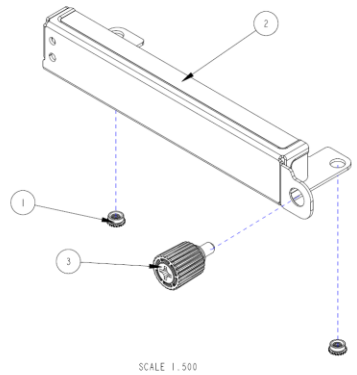
PARTS LIST

**Figure 10: EFF EMI Finger Stock Faceplate Bracket Subassemblies – Exploded ISO Views**




| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 1 | 6 | SOUTHCO_CN-99-459 | |
| 2 | 5 | OCP_DC-SCM2_EMI_FOF_GSKT_7P35 | |
| 2 | 4 | OCP_DC-SCM2_EMI_FOF_GSKT_T8P2 | |
| 2 | 3 | OCP_DC-SCM2_EJTR-HNDL_SCR | |
| 1 | 2 | OCP_DC-SCM2_BRKT_TAB_GSKT_ASSY | |
| 1 | 1 | OCP_DC-SCM2_BRKT_GSKT_CONN | |
| | TOP | OCP_DC-SCM2_BRKT_TAB_GSKT_TA | |

PARTS LIST




| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 1 | 3 | SOUTHCO_4C-99-343-KEEE | |
| 1 | 2 | OCP_DC-SCM2_BRKT_TAB_EMI-GSKT | |
| 2 | 1 | OCP_DC-SCM2_BRKT_STDOFF | |
| | TOP | OCP_DC-SCM2_BRKT_TAB_GSKT_ASSY | |

PARTS LIST

**Figure 11: EFF EMI FoF Gasket Faceplate Bracket Subassemblies – Exploded ISO Views**

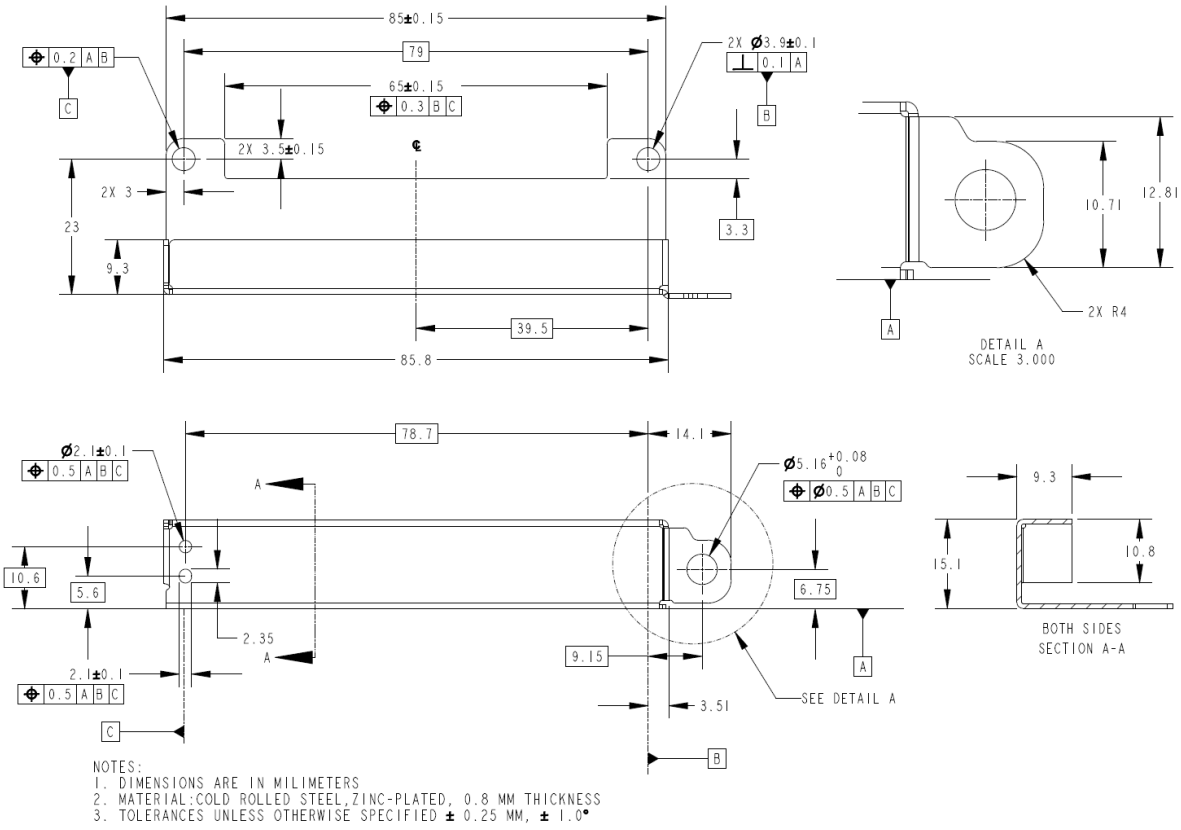



**Figure 12: EFF Generic Faceplate Dimensions**

### 2.2.2.2 EFF EMI Finger Stock Faceplate Bracket

Figure 13 illustrates the specific dimensions for the bracket that are required to use the EMI finger stock components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

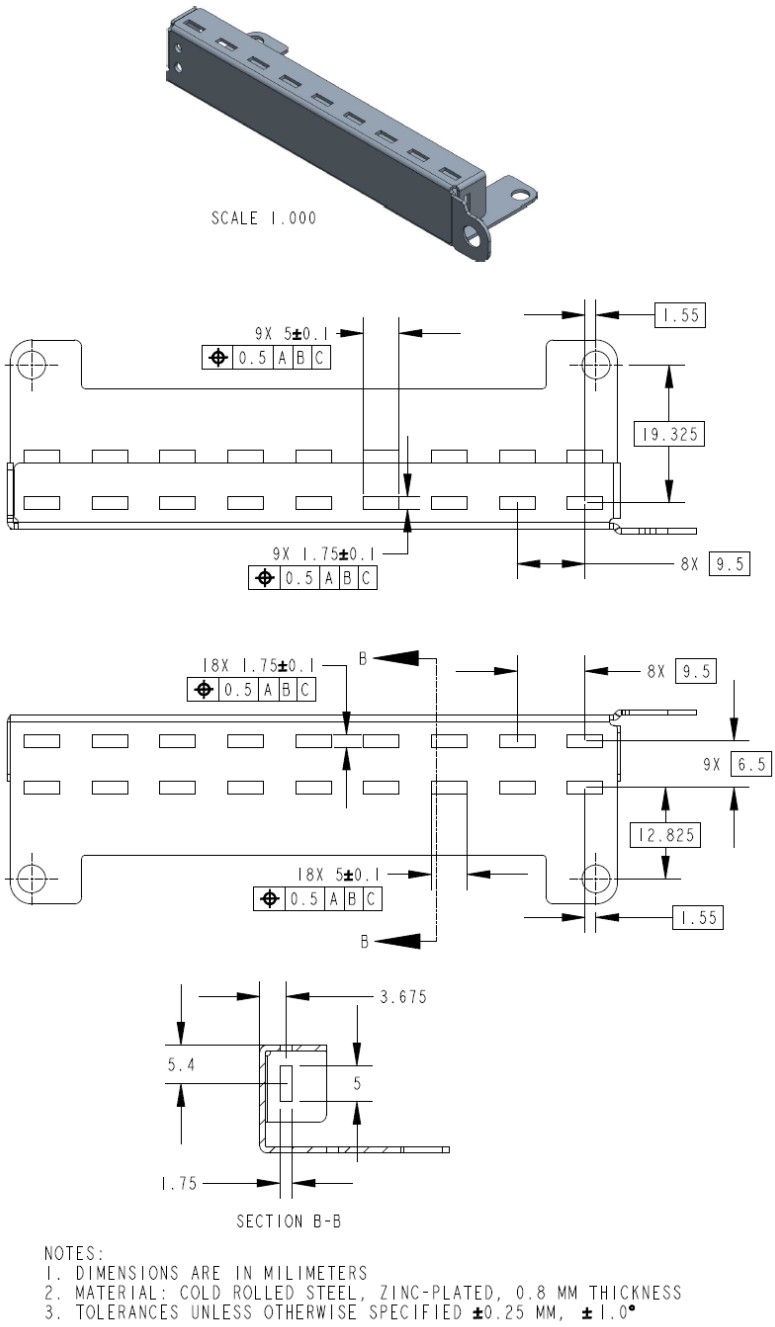



**Figure 13: EFF EMI Finger Stock Faceplate Dimensions**

### 2.2.2.3 EFF EMI FoF Gasket Faceplate Bracket

Figure 14 illustrates the specific dimensions for the bracket that are required to use the EMI FoF gasket components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

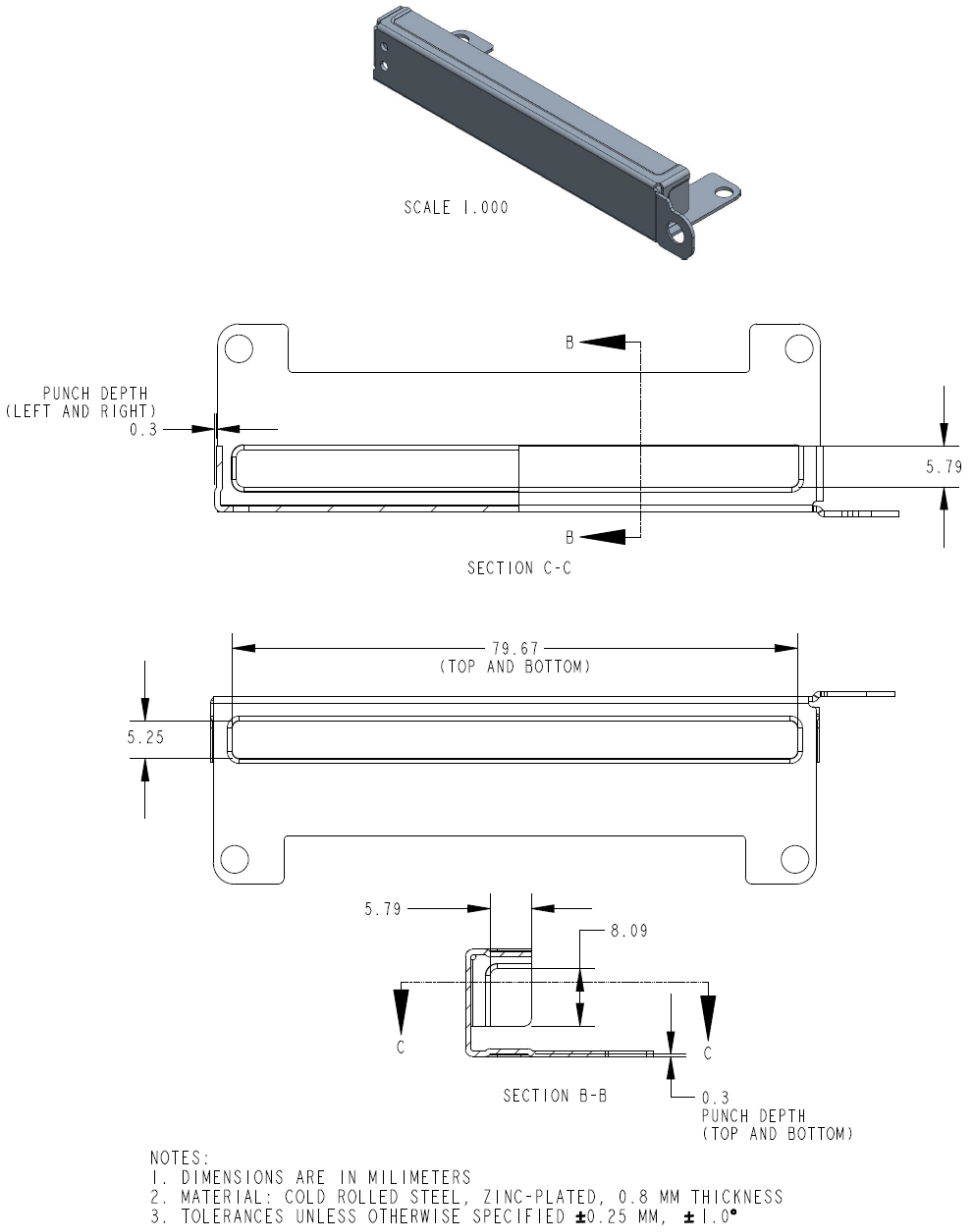



**Figure 14: EFF EMI FoF Gasket Faceplate Dimensions**

### 2.2.3 HFF Internal Form Factor

The Internal Form Factor (IFF) is defined for usage as an internally embedded module to the server without direct insertion/extraction interfaces (i.e., handles, thumbscrews) to a server front or rear wall. It has no defined external securing features for attachment to the chassis. Internal security features provided by the rails prevent insertion or extraction from outside the chassis. The IFF implementation uses the same PCB board outline as the EFF. It does have the option for a vertical handle to aid in the insertion and extraction of the card edge into the connector for an internal locking solution as can be seen in Figure 15. Dimensions and KOZs for the handle are illustrated in Figure 7.

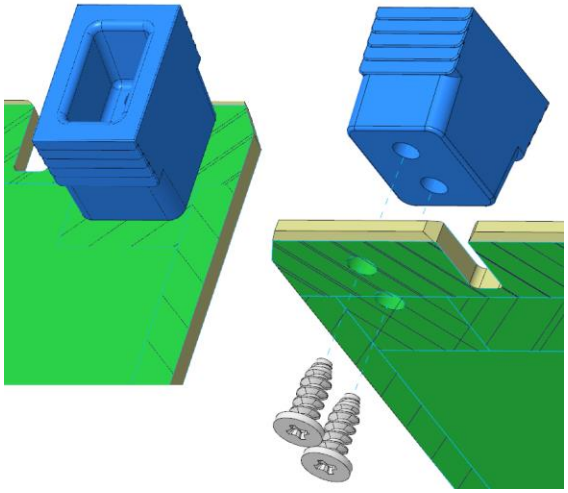


**Figure 15: IFF Optional Handle - ISO Assembled and Exploded Views**

There are two options for an EMI compliance solution shown below in Figure 16. Option one utilizes metal finger stock that is attached to all sides of the faceplate and interface to the chassis bay opening flanges for contact. Option two takes advantage of Fabric-over-Foam (FoF) components attached to all four sides to make continuous contact with the chassis bay opening flange walls.

Option 1 Option 2

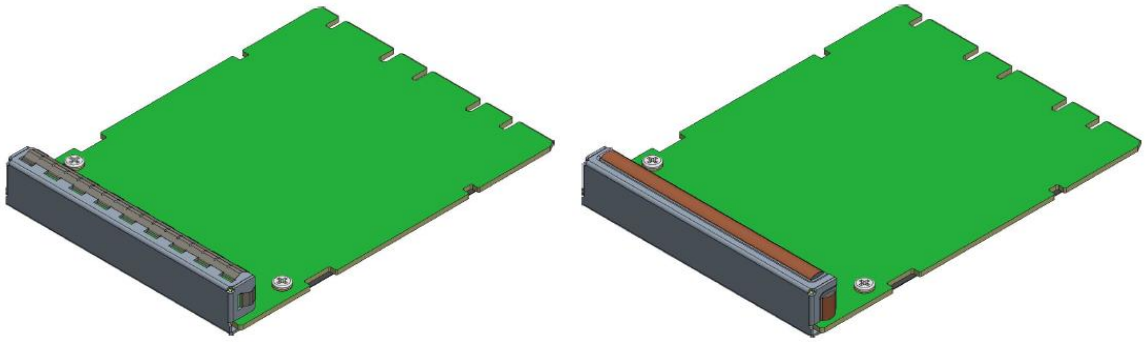
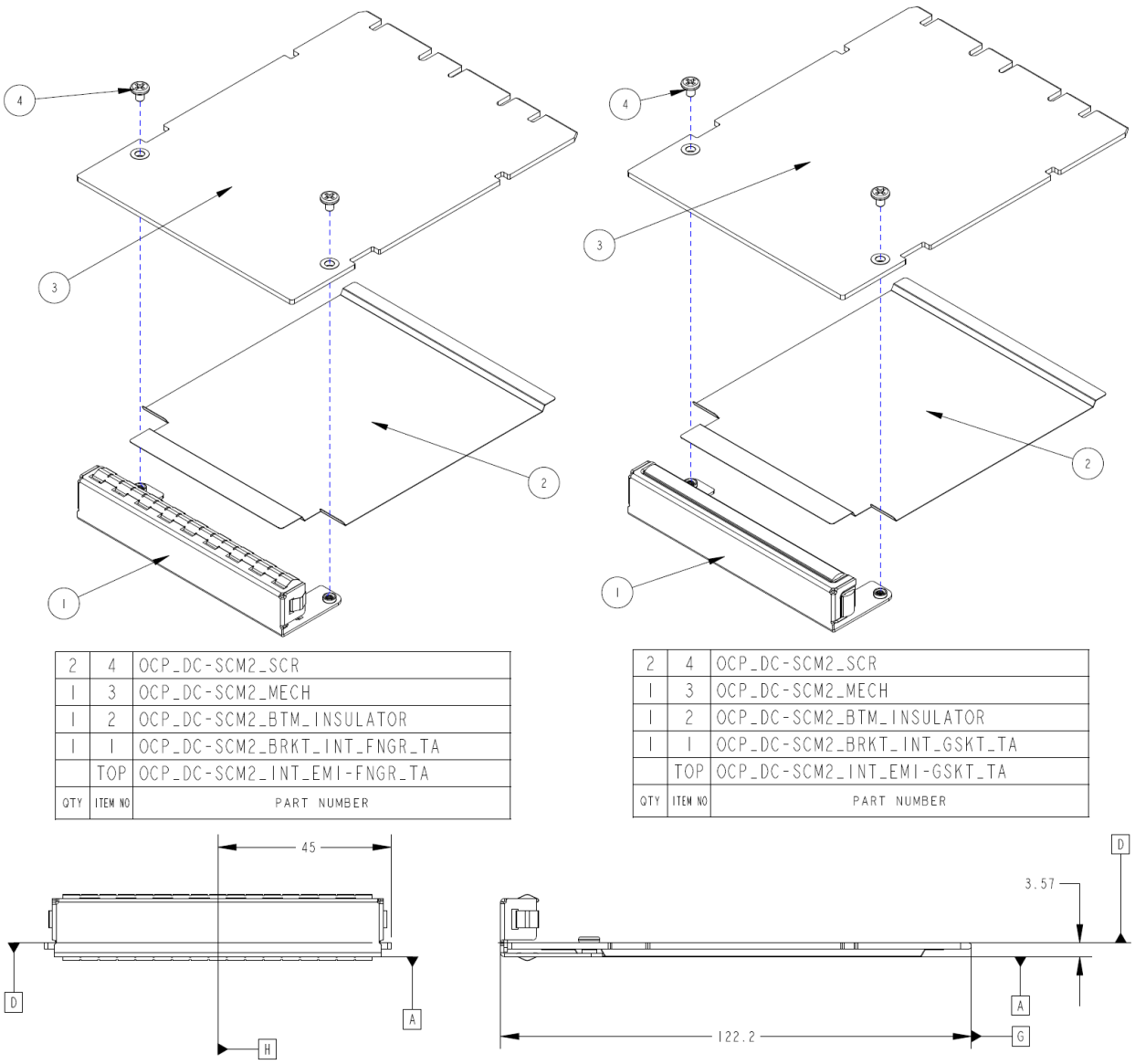


**Figure 16: IFF Module Options - ISO Views**

Exploded views of each corresponding module assembly are shown in Figure 17.




| QTY | ITEM NO | PART NUMBER |
|---|---|---|
| 2 | 4 | OCP_DC-SCM2_SCR |
| 1 | 3 | OCP_DC-SCM2_MECH |
| 1 | 2 | OCP_DC-SCM2_BTM_INSULATOR |
| 1 | 1 | OCP_DC-SCM2_BRKT_INT_FNGR_TA |
| | TOP | OCP_DC-SCM2_INT_EMI-FNGR_TA |

| QTY | ITEM NO | PART NUMBER |
|---|---|---|
| 2 | 4 | OCP_DC-SCM2_SCR |
| 1 | 3 | OCP_DC-SCM2_MECH |
| 1 | 2 | OCP_DC-SCM2_BTM_INSULATOR |
| 1 | 1 | OCP_DC-SCM2_BRKT_INT_GSKT_TA |
| | TOP | OCP_DC-SCM2_INT_EMI-GSKT_TA |

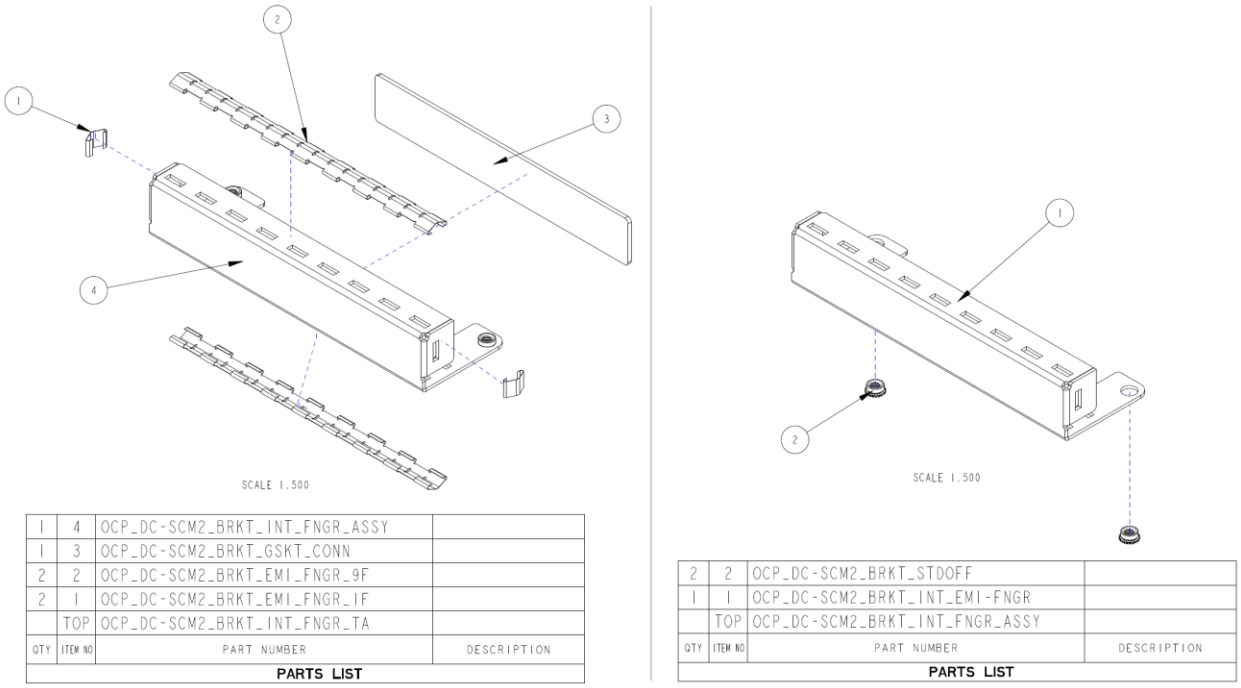
**Figure 17: IFF Module Assemblies – Exploded ISO and Orthographic Views**

#### 2.2.3.1 IFF Faceplate Bracket Subassembly

The IFF module supports a front faceplate that enables front I/O access. It does not include features for external retention to the chassis, and it is expected that these features are present internal to the system. Each faceplate option has the same overall features and dimensions, except for where the EMI solution is attached. Exploded views of the different bracket assemblies are shown below in Figure 18 and Figure 19. The general internal faceplate dimensions are shown in Figure 20.

Faceplate connector cut-outs and perforations are excluded from the figures and may be customized per system configuration and system airflow requirements. Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 x 3.0 mm, or round vents with a maximum diameter of 3 mm, may be added to help optimize airflow while maintaining the integrity of the faceplate structure. The OCP DC-SCM 2 card supplier may add port

identification markings on the faceplate assembly that meet their manufacturing and customer requirements.
Depending on the OCP DC-SCM 2 card implementation, I/O connectors may be placed anywhere within the allowable connector keep-in regions as defined by the PCB mechanical drawings and faceplate drawings of Section 2.2.1 and Section 2.2.3.1.
Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers.



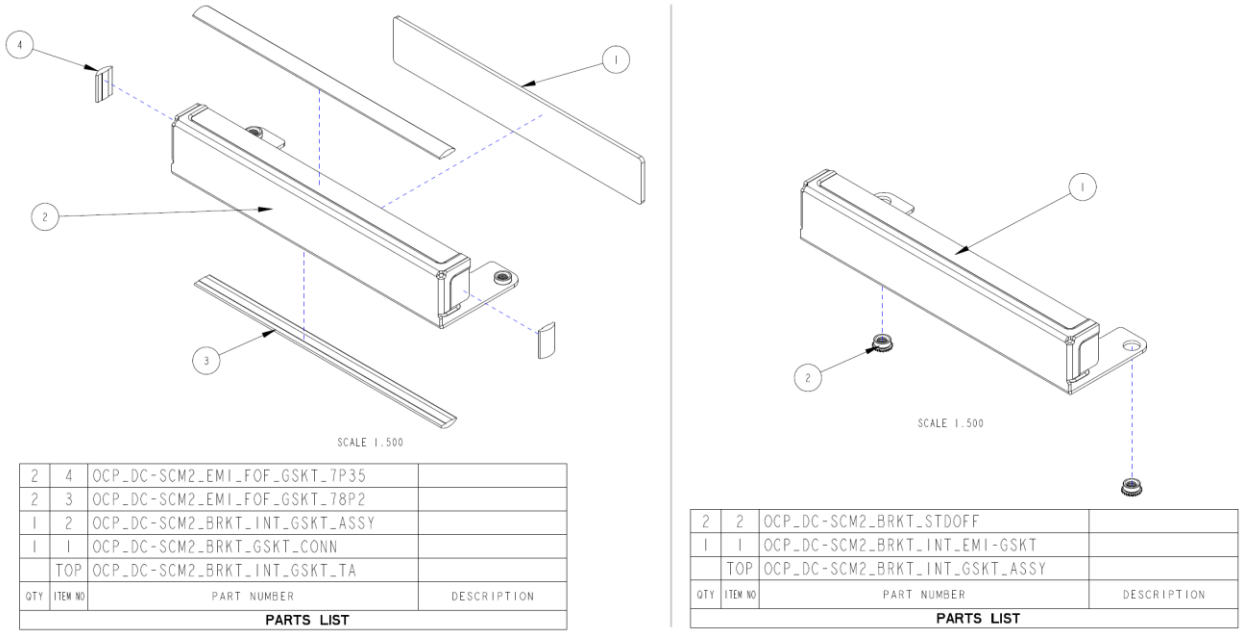

| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 1 | 4 | OCP_DC-SCM2_BRKT_INT_FNGR_ASSY | |
| 1 | 3 | OCP_DC-SCM2_BRKT_GSKT_CONN | |
| 2 | 2 | OCP_DC-SCM2_BRKT_EMI_FNGR_9F | |
| 2 | 1 | OCP_DC-SCM2_BRKT_EMI_FNGR_IF | |
| | TOP | OCP_DC-SCM2_BRKT_INT_FNGR_TA | |

PARTS LIST

| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 2 | 2 | OCP_DC-SCM2_BRKT_STDOFF | |
| 1 | 1 | OCP_DC-SCM2_BRKT_INT_EMI-FNGR | |
| | TOP | OCP_DC-SCM2_BRKT_INT_FNGR_ASSY | |

PARTS LIST

**Figure 18: IFF EMI Finger Stock Faceplate Bracket Subassemblies – Exploded ISO Views**




| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 2 | 4 | OCP_DC-SCM2_EMI_FOF_GSKT_7P35 | |
| 2 | 3 | OCP_DC-SCM2_EMI_FOF_GSKT_78P2 | |
| 1 | 2 | OCP_DC-SCM2_BRKT_INT_GSKT_ASSY | |
| 1 | 1 | OCP_DC-SCM2_BRKT_GSKT_CONN | |
| | TOP | OCP_DC-SCM2_BRKT_INT_GSKT_TA | |

PARTS LIST

| QTY | ITEM NO | PART NUMBER | DESCRIPTION |
|---|---|---|---|
| 2 | 2 | OCP_DC-SCM2_BRKT_STDOFF | |
| 1 | 1 | OCP_DC-SCM2_BRKT_INT_EMI-GSKT | |
| | TOP | OCP_DC-SCM2_BRKT_INT_GSKT_ASSY | |

PARTS LIST

**Figure 19: IFF EMI FoF Gasket Faceplate Bracket Subassemblies – Exploded ISO Views**

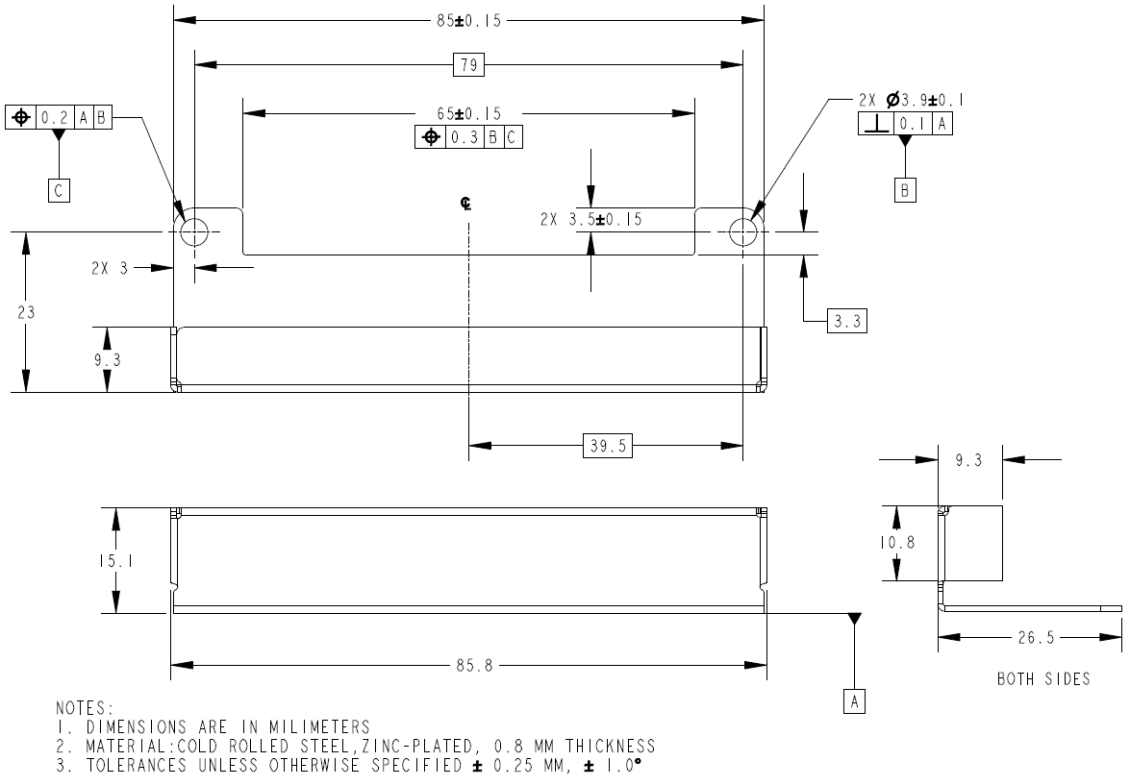



**Figure 20: IFF Generic Faceplate Dimensions**

### 2.2.3.2 IFF EMI Finger Stock Faceplate Bracket

Figure 21 illustrates the specific dimensions for the bracket that are required to use the EMI finger stock components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

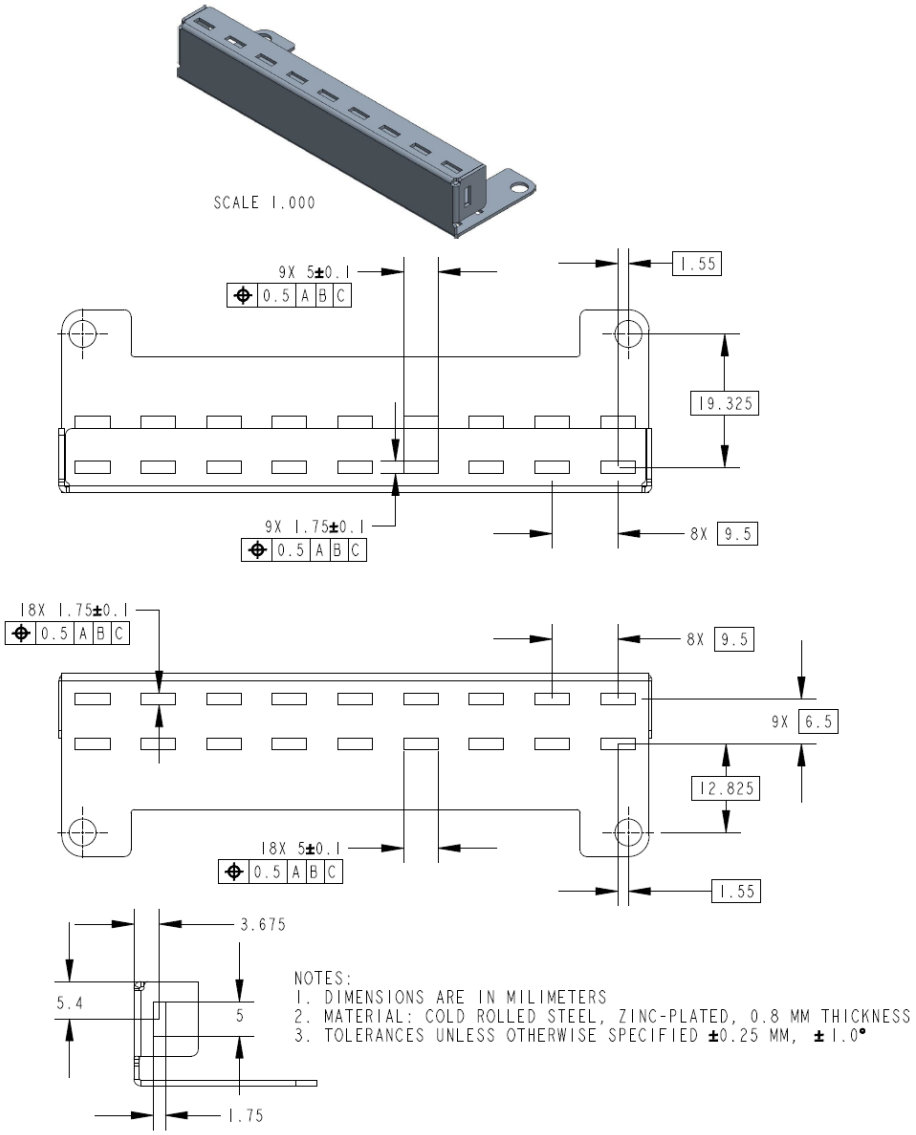



**Figure 21: IFF EMI Finger Stock Faceplate Dimensions**

### 2.2.3.3 IFF EMI FoF Gasket Faceplate Bracket

Figure 22 illustrates the specific dimensions for the bracket that are required to use the EMI FoF gasket components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

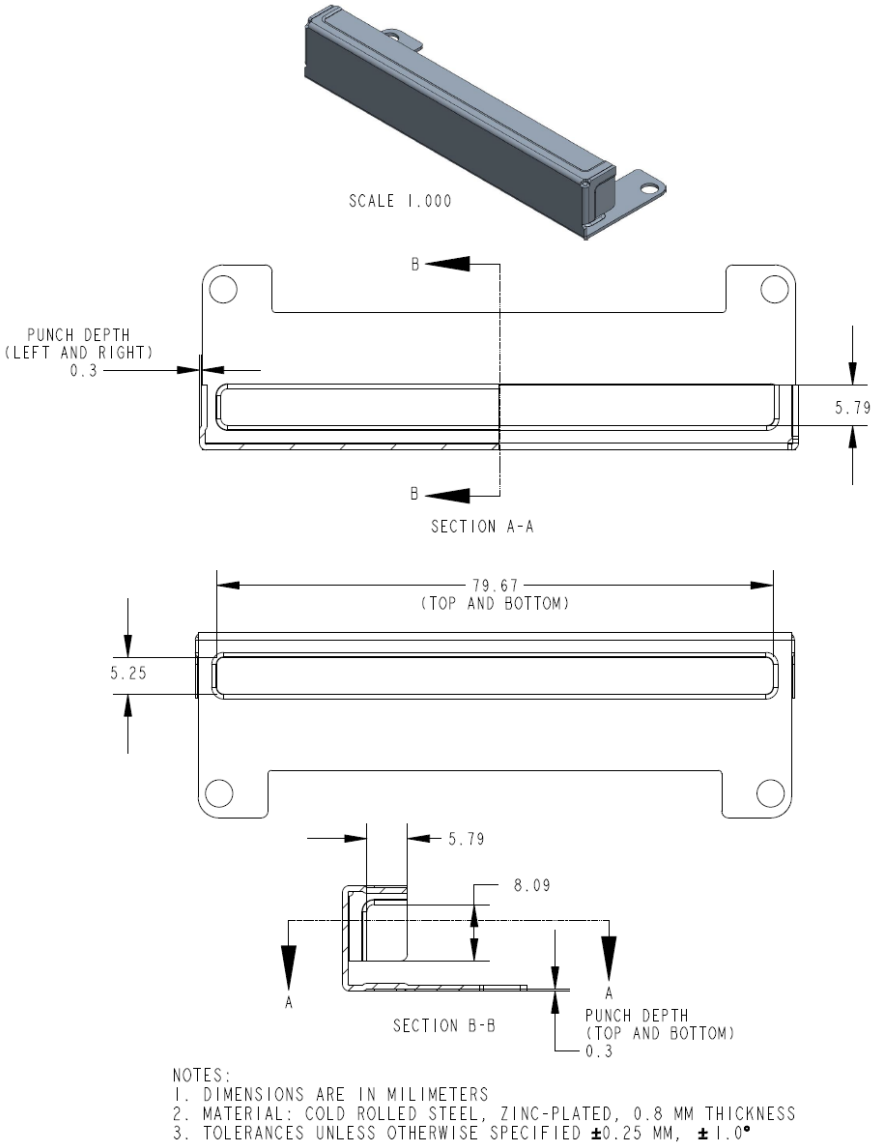



**Figure 22: IFF EMI FoF Gasket Faceplate Dimensions**

### 2.2.4 HFF EMI Compliance Components

In the likely event that emissions must be contained in the system and pass certain regulatory testing for EMC, two EMI solutions are available as detailed in previous sections. Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers.

For Option 1 of both EFF and IFF modules, EMI finger stock is utilized around all four sides of the faceplate bracket. There are two lengths: a nine-finger length and a single-finger length. These can be seen in Figure 23 below.

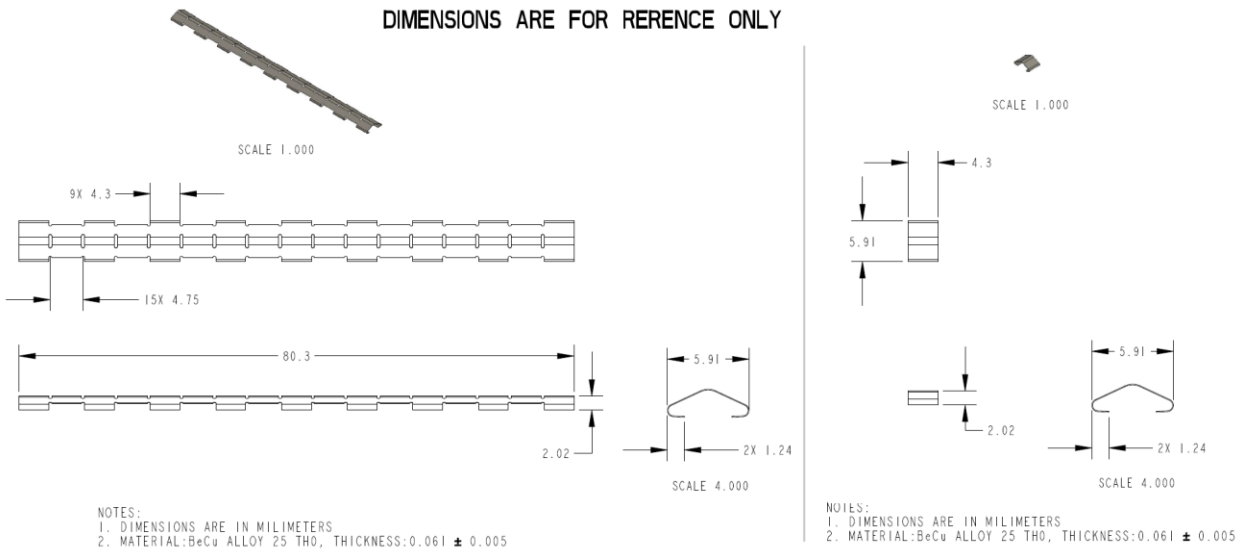



**Figure 23: HFF EMI Finger Stock Reference Dimensions**

For Option 2 of both EFF and IFF modules, FoF gaskets are utilized around all four sides of the faceplate bracket. There are two lengths: a 78.2 mm length and a 7.35 mm length. These can be seen in Figure 24 below.

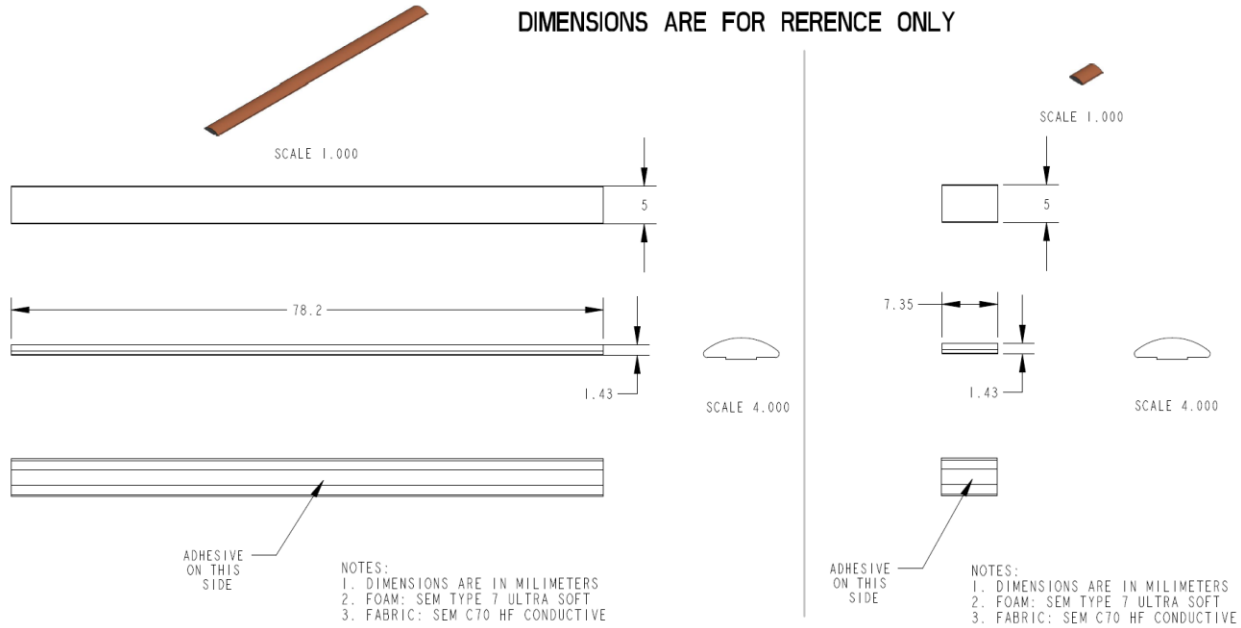



**Figure 24: HFF EMI FoF Gasket Reference Dimensions**

There is a FoF gasket that may be applied to the inside of the front faceplate surface. This gasket has cutouts matching the sheet metal connector cutouts present on the from faceplate wall where the individual connector faces protrude through. It is compressed by the front perimeters of the connector face housings, ensuring good contact for conductive grounding. Gasket connector cut-outs and perforations are excluded from the figures and may be customized per system configuration and system airflow requirements.

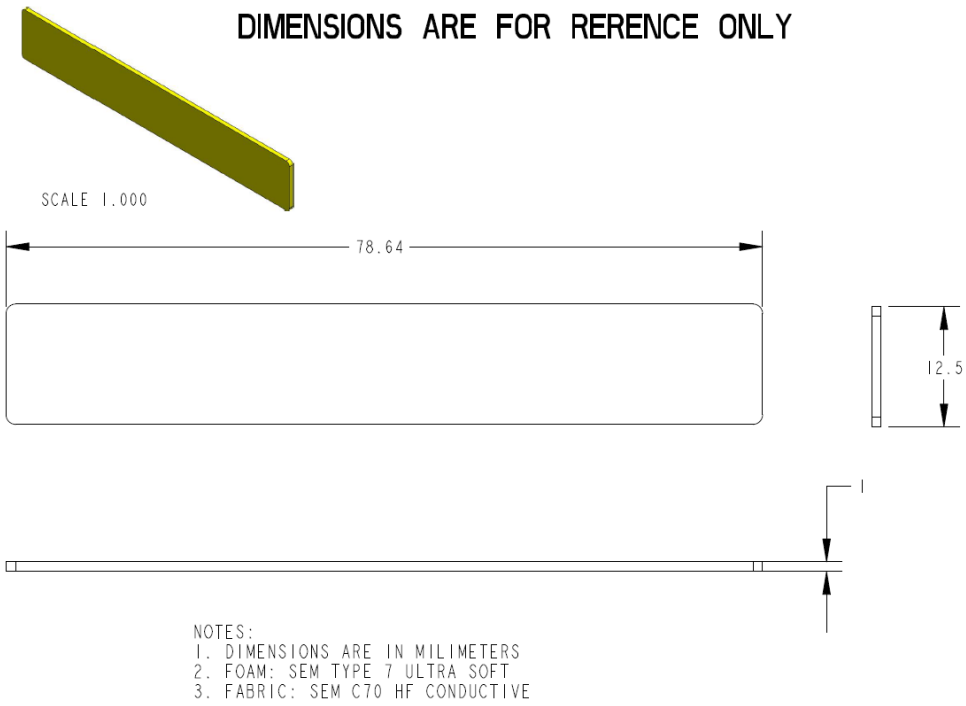



**Figure 25: EMI Front Faceplate FoF Gasket Reference Dimensions**

### 2.2.5 HFF Insulation Requirements

All OCP DC-SCM 2 HFF modules shall implement an insulator to prevent the bottom-side board components from shorting out to the baseboard chassis. The recommended insulator thickness is 0.127 mm (0.005”) and shall reside within the following mechanical envelopes for the EFF and IFF form factors. The total stack up height of the secondary side components, insulator and the labels shall not exceed the 2 mm keep-in dimension as shown in Figure 6 and Figure 26.

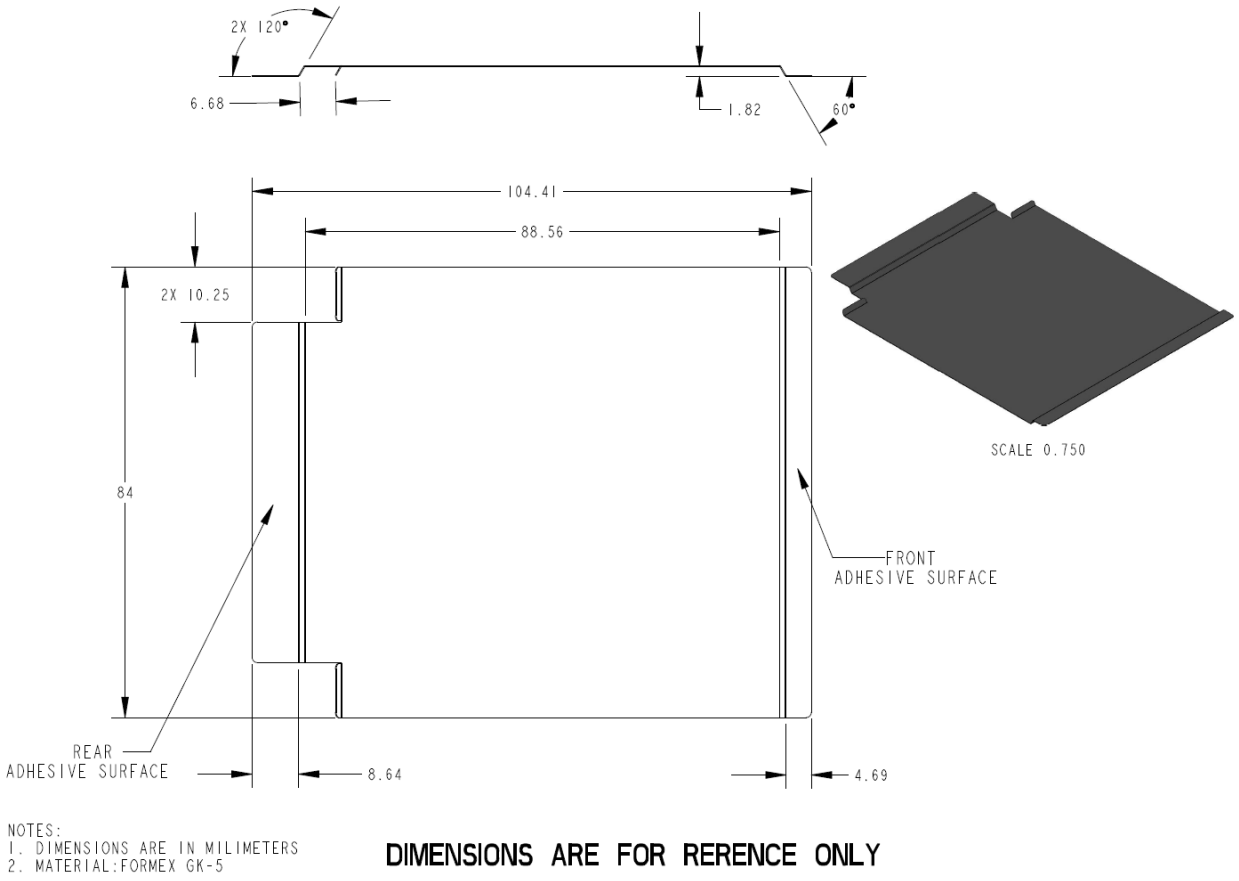



**Figure 26: HFF Insulator Dimensions**

### 2.2.6 HFF Module Guide Rails

The EFF version of the module is designed to leverage most of the geometry of the OCP NIC 3.0 HFF reference rails. There is one major change to the geometry, and that is a set of 23.8 x 0.6 mm cuts at the ends of the rails. This is to enable the inside rail surface to drive the horizontal position of the module, and not the mounting screws that would normally interfere in these areas. Note that the mounting screw locations for OCP DC-SCM 2 HFF are different than the locations in the OCP NIC 3.0 specification. This modified rail design is symmetric and can be rotated 180° to have a left and right-side rail set.

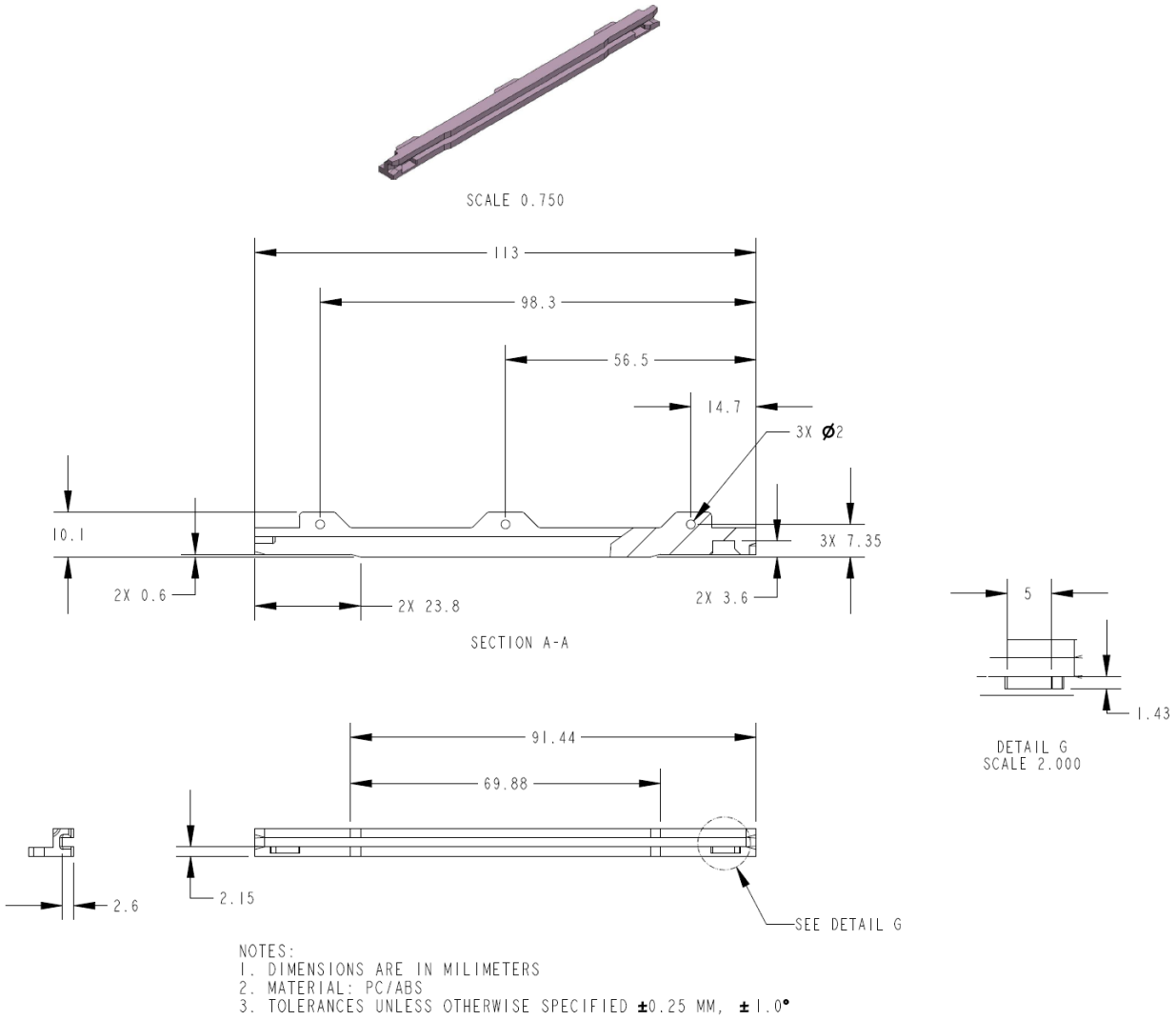



**Figure 27: EFF Module-in-Tray Rail Dimensions**

For the IFF version there are two options: 1) to reuse the modified OCP DC-SCM 2 HFF reference rail design, or 2) use the Module-in-Tray rail reference designs. There is a left and a right rail that make up the set; they are basically mirrored components. They provide a means to retain the module when the OCP DC-SCM 2 HFF and baseboard are assembled on a tray prior to assembly into the chassis. These notches are illustrated in Figure 5, Detail C. The guide rails have hook/slot features that interface in these areas. If the rail features shown in Figure 28, Details E and F are utilized, they may also serve as a locking mechanism to prevent module removal externally.

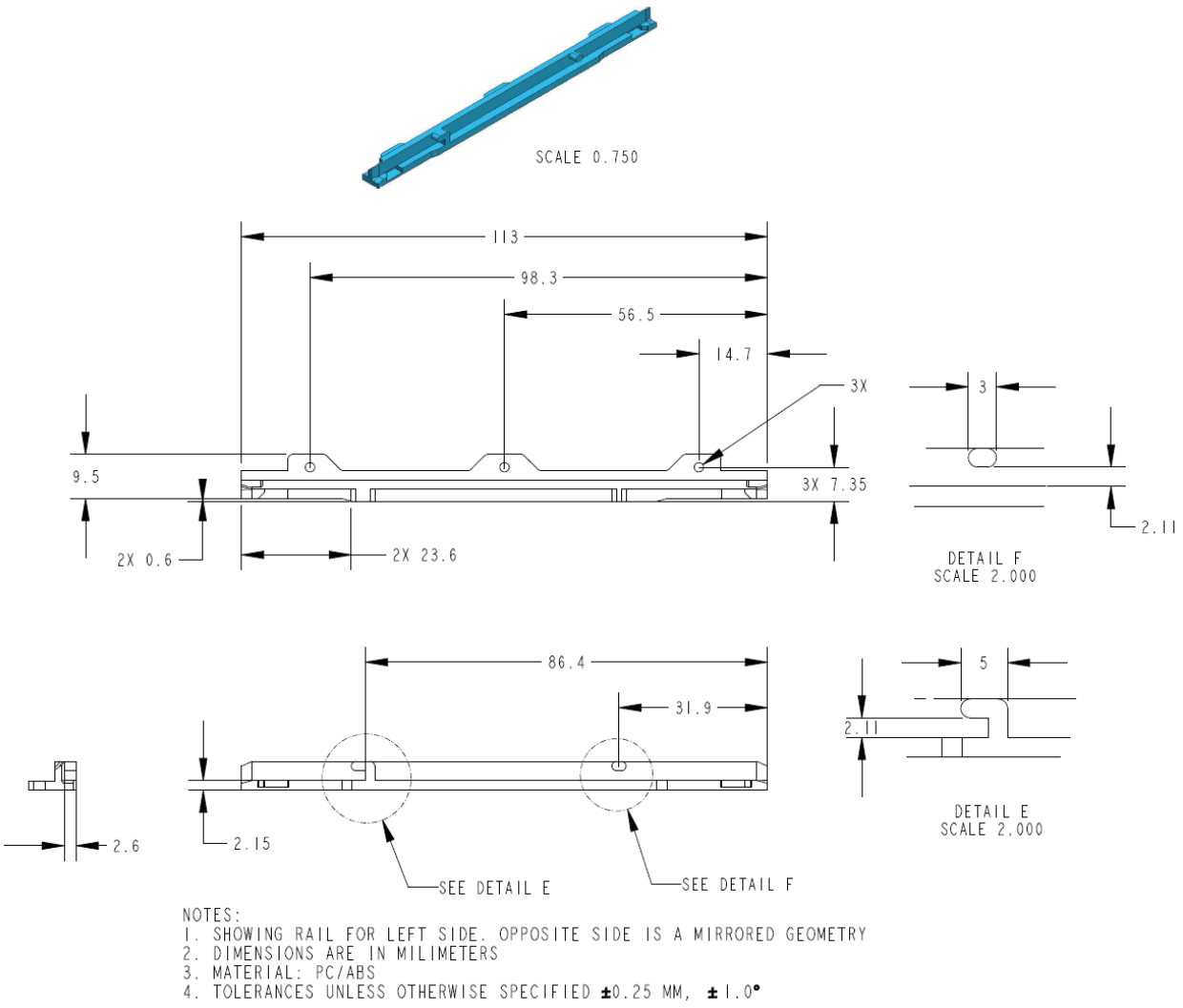



**Figure 28: IFF Module-in-Tray Rail Dimensions**

### 2.2.7 Chassis Bay Opening Requirements

All OCP DC-SCM 2 HFF modules shall fit within the chassis opening defined below in Figure 29. Sheet metal flanges on four sides are bent inwards to provide surfaces for the EMI solutions to make contact with and provide a conductive path to ground. The height of the chassis cutout is dependent on where the module is positioned relative to the card edge connector on the baseboard.

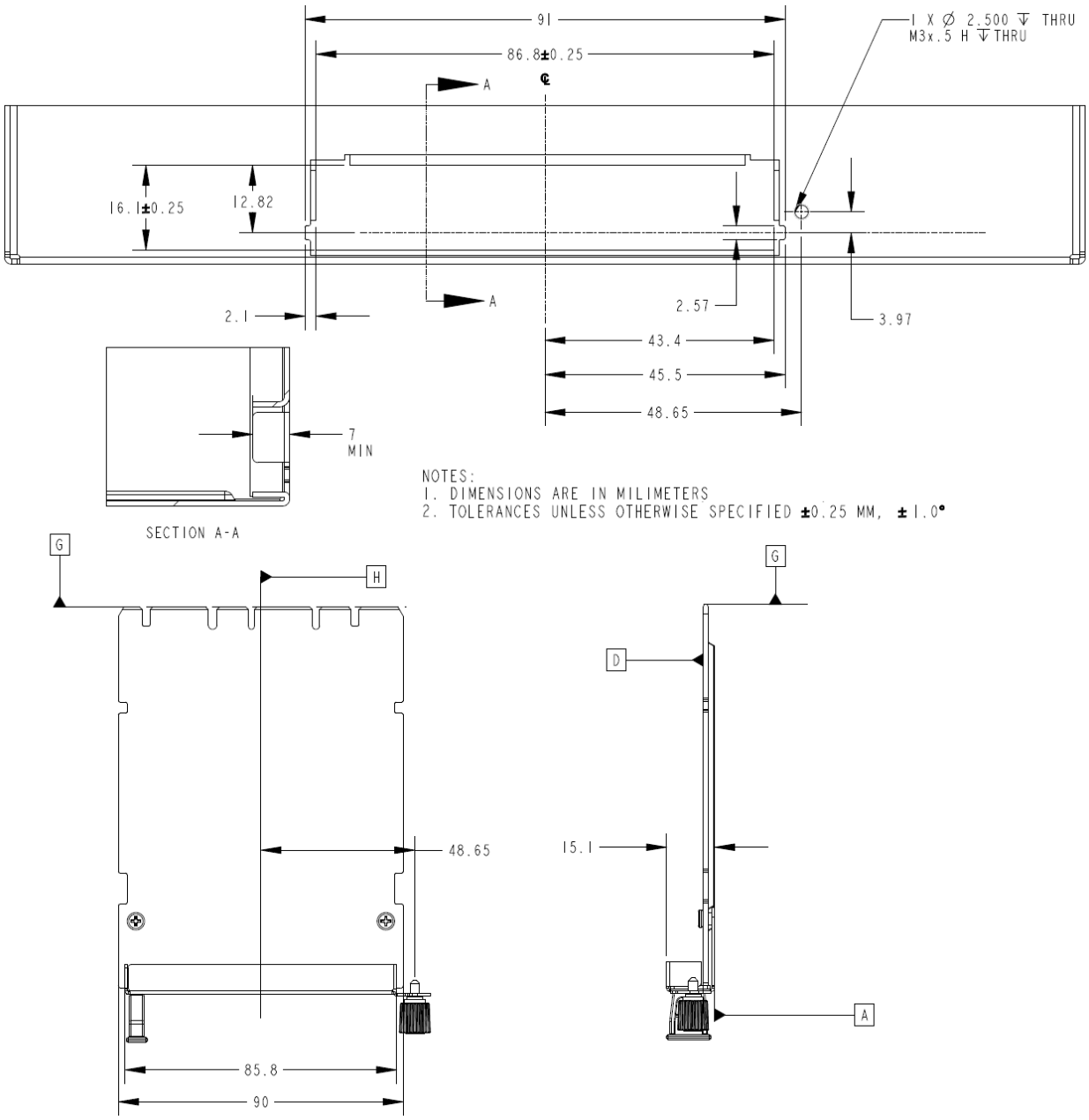



**Figure 29: HFF Chassis Bay Opening Dimensions**

## 2.3 Vertical Form Factor

The Vertical Form Factor (VFF) is intended for use in 2U or taller servers in which the OCP DC-SCM 2 is installed vertically at the chassis front/rear wall (similar to a PCIe AIC card). Standard front panel interfaces are contained on the OCP DC-SCM 2 VFF and accommodates cables as necessary.

### 2.3.1 VFF Board Dimensions and Keep-out Zones

The VFF defines two PCB depths - a Short VFF and a Long VFF. Other than the length of the card, the dimensions between the two are identical. The Short VFF PCB form factor overall dimensions are shown in Figure 39. The Long VFF PCB dimensions are shown in Figure 40. Both PCBs have a thickness of 1.57 mm.

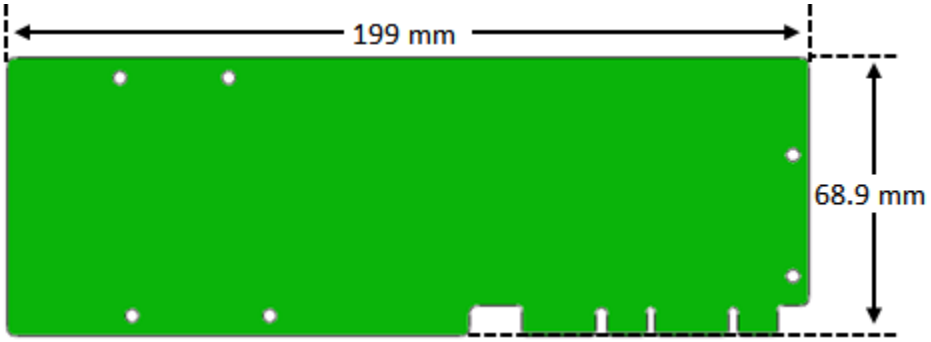



**Figure 30: Short Vertical Form Factor Board Overall Dimensions**

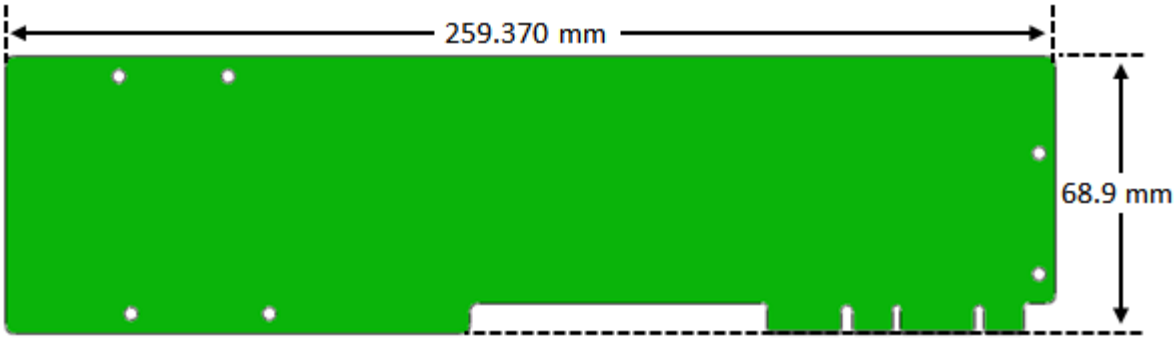



**Figure 31: Long Vertical Form Factor Board Overall Dimensions**

The top-side board dimensions, along with the corresponding detail views and KOZs are shown in Figure 41 and Figure 42. The Bottom side dimensions, detail views, and KOZs are illustrated in Figure 43 and Figure 44.

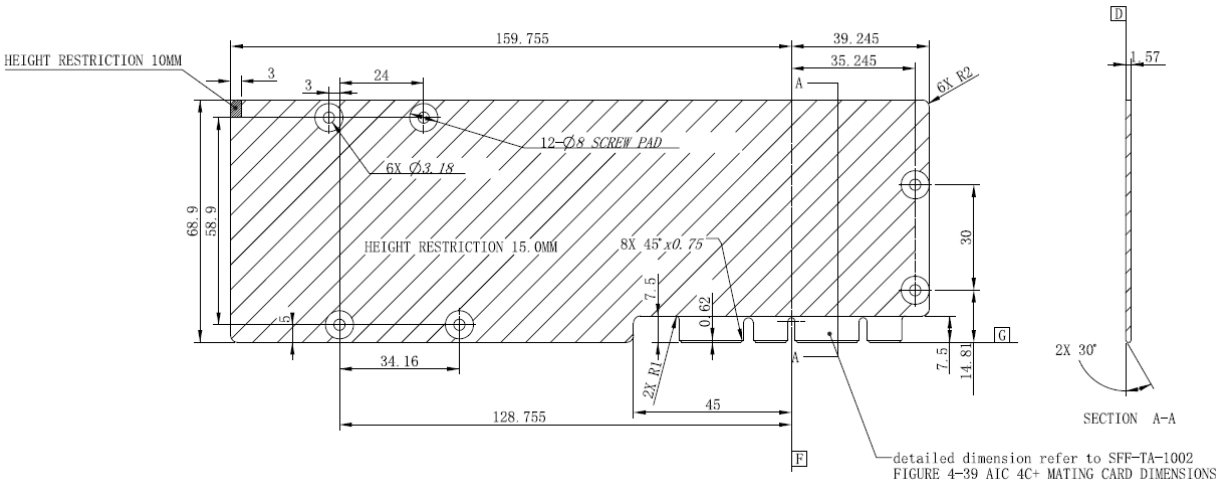



**Figure 32: Short VFF Board Dimensions and Keep-out Zones – Top View**

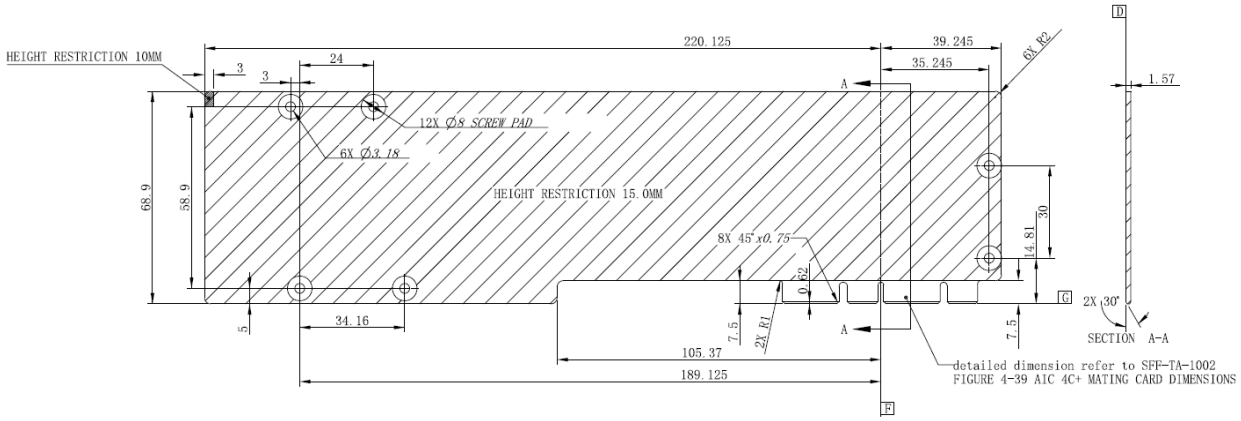



**Figure 33: Long VFF Board Dimensions and Keep-out Zones – Top View**

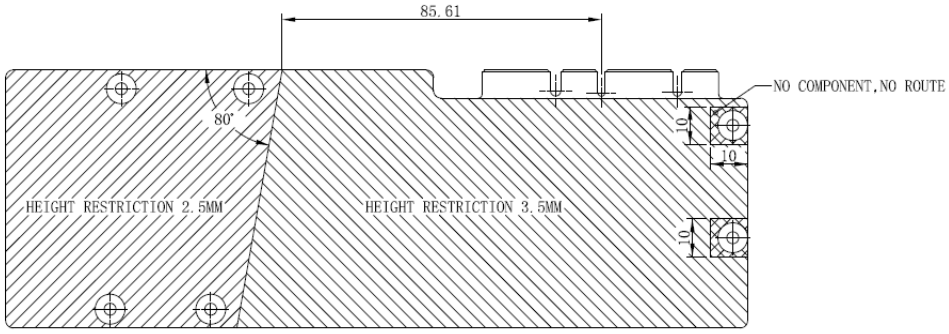



**Figure 34: Short VFF Board Dimensions and Keep-out Zones – Bottom View**

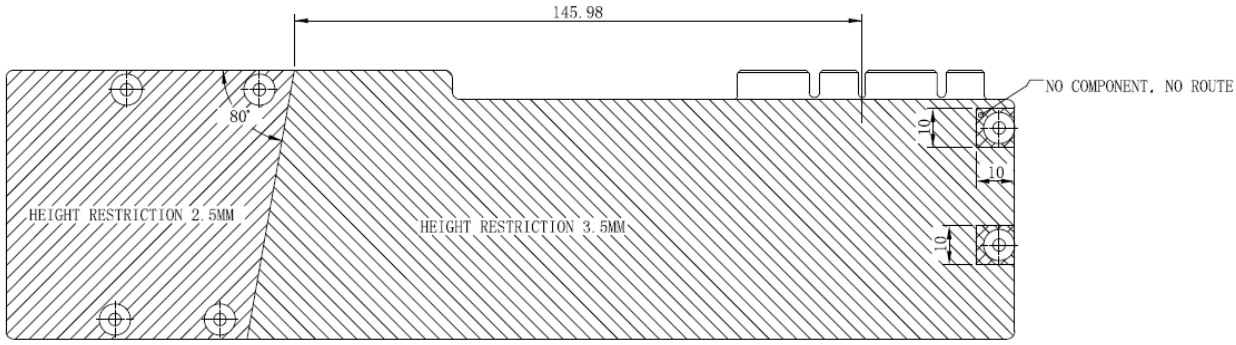



**Figure 35: Long VFF Board Dimensions and Keep-out Zones – Bottom View**

### 2.3.2 VFF Faceplate Brackets

The OCP DC-SCM 2 VFF offers two options for faceplate brackets to give flexibility to chassis designers. The Type 1 faceplate bracket is designed to be mounted flush against the inner surface of front or rear panels of a chassis and is detailed in Figure 34. The Type 2 faceplate bracket is designed with similar dimensions to a low-profile PCIe card and is designed to slot in next to low-profile PCIe cards and utilize PCIe bracket chassis features as detailed in Figure 39. Both Short and Long VFF OCP DC-SCM 2 cards utilize the same faceplate bracket design.

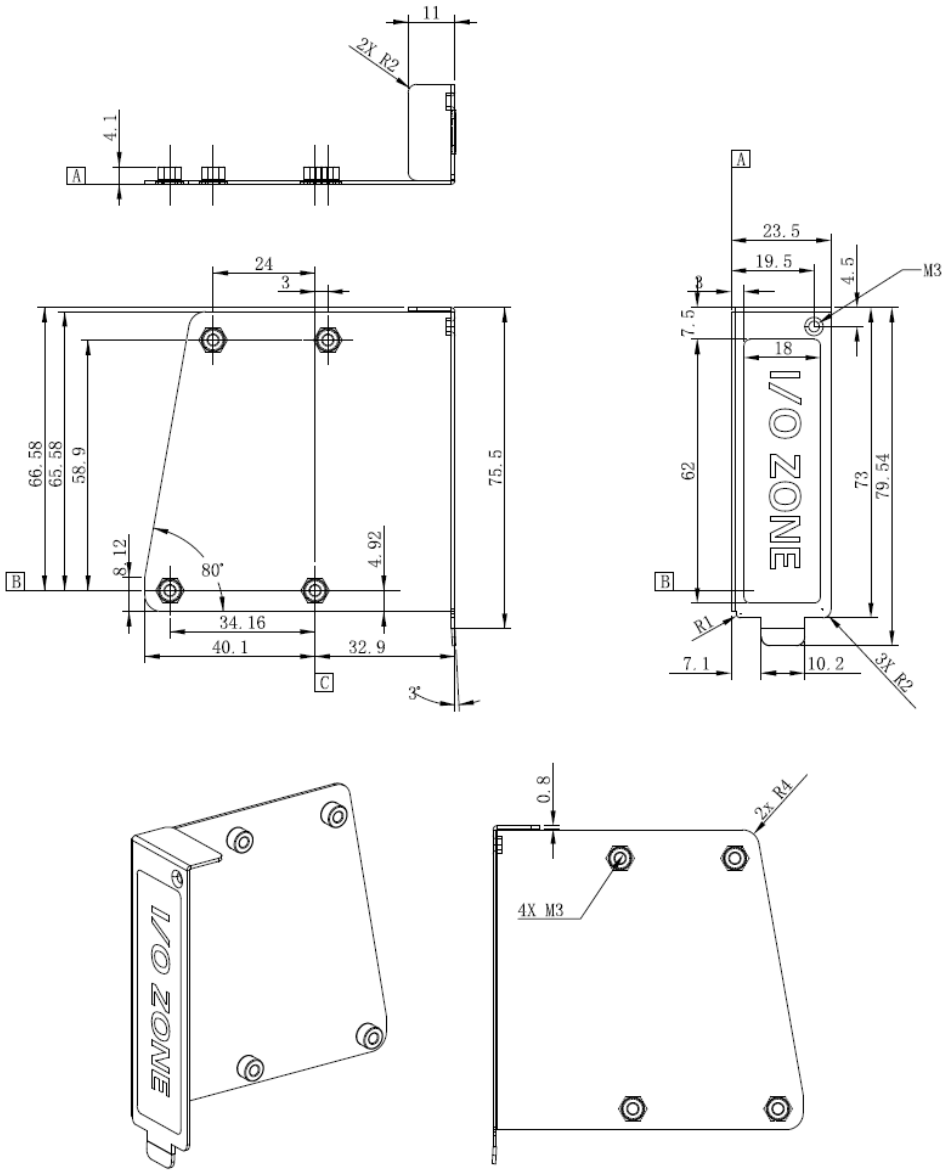



**Figure 34: VFF Type 1 Faceplate Bracket**

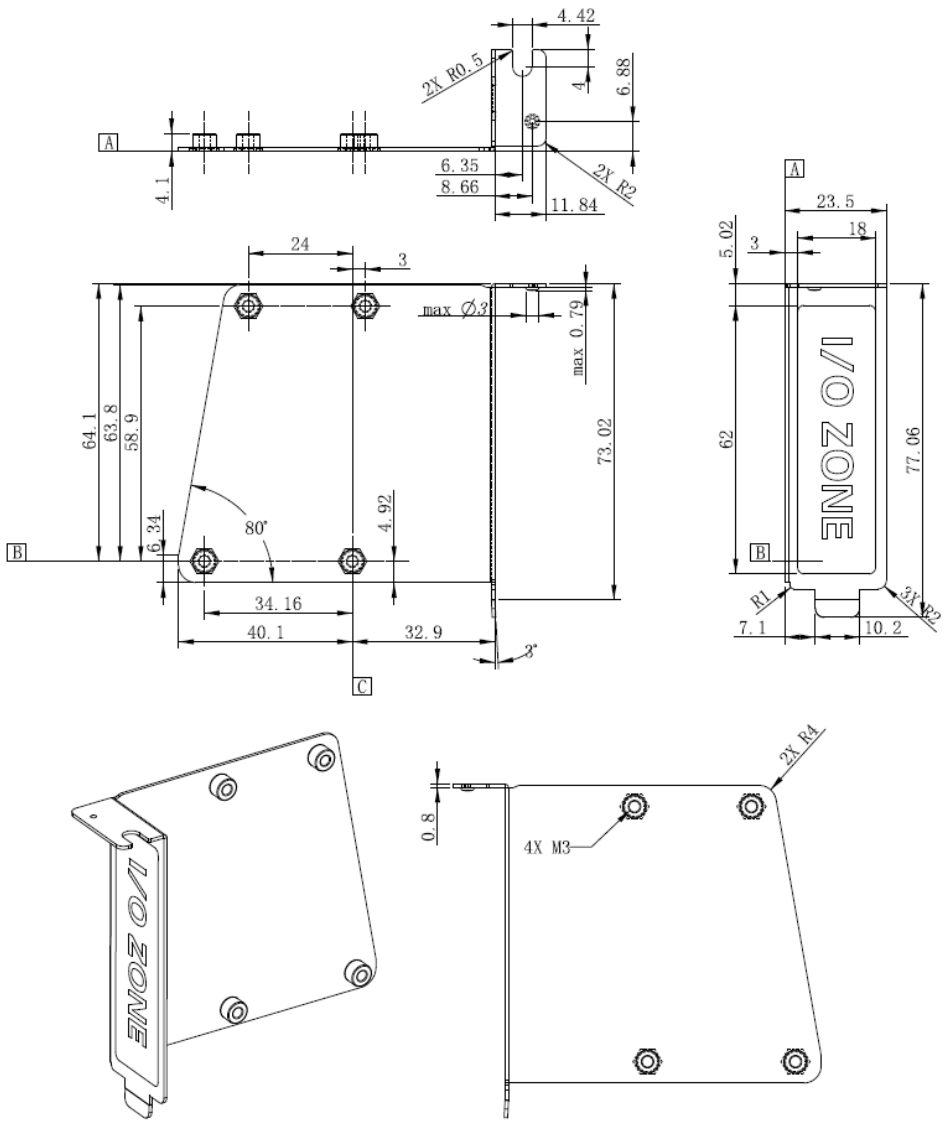



Figure 35: VFF Type 2 Faceplate Bracket

### 2.3.3 VFF Optional Rear Bracket

The OCP DC-SCM 2 VFF defines an optional rear support bracket. The rear bracket attaches to the rear end of the PCB and serves to secure the OCP DC-SCM 2 to the HPM. This is an optional part that can help prevent the card from ejecting from the 4C+ DC-SCI connector during server shipments. It also features a guide pin which can aid in installation of the card, especially in tightly packed server chassis designs which may not allow a service technician a clear view of the connector. The rear bracket is detailed in Figure 36.

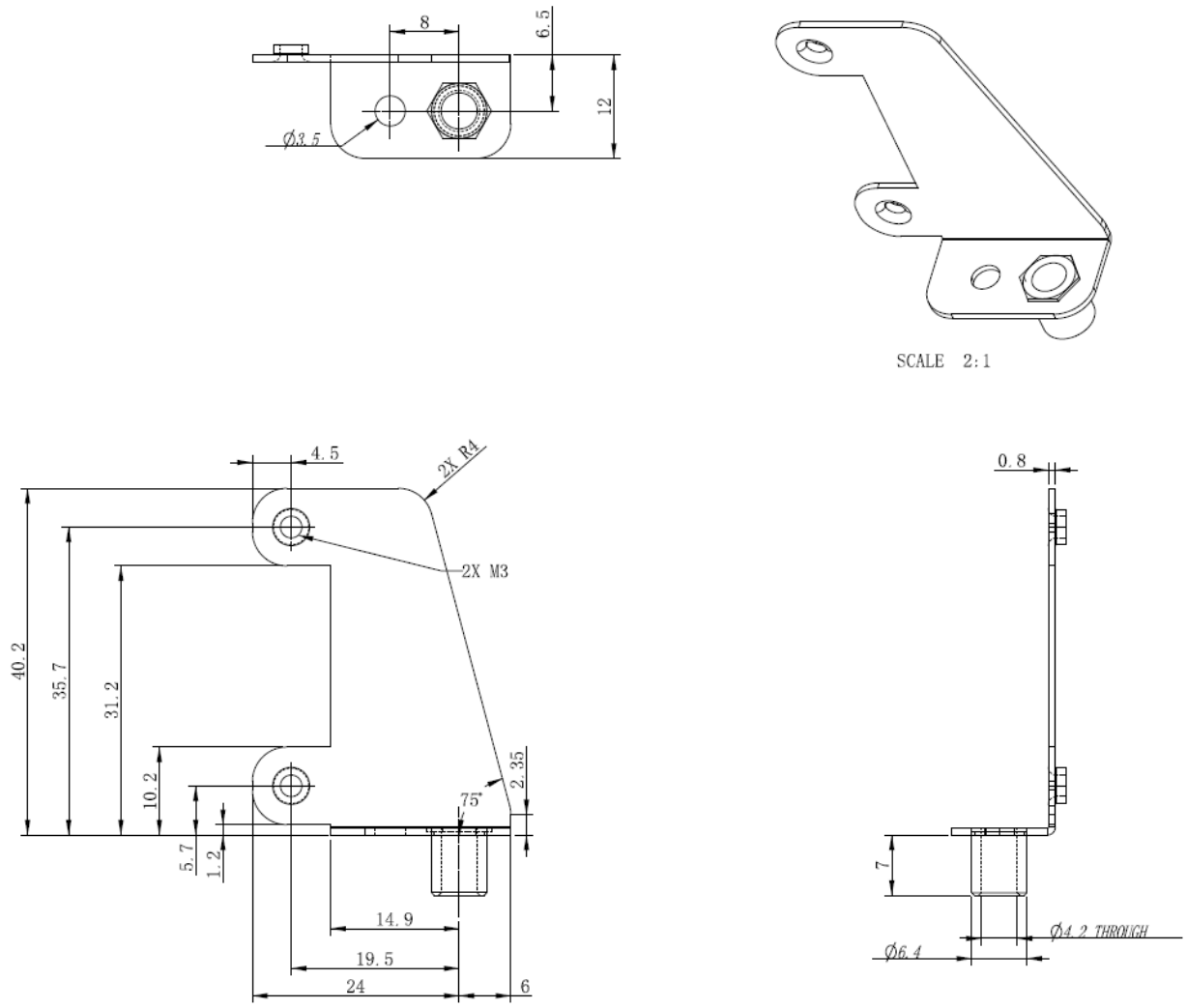



**Figure 36: Optional VFF Rear Bracket**

### 2.3.4 VFF Chassis Opening and Bracket I/O Region

The Type 1 and Type 2 VFF brackets have both a chassis opening, and bracket I/O region defined. The chassis opening is defined as the minimum required aperture, taking into account reference system-level tolerances. Actual dimensions will vary based on system implementation. The size of the chassis opening must include system accommodations, including but not limited to: protruding connectors on the OCP DC-SCM 2 module, and insertion and extraction of the OCP DC-SCM 2 module from the system, etc. The chassis opening is dimensioned in the X and Y directions as shown in Figure 37 and Figure 38. The Z direction, or connector KIV depth, is defined as **18 mm** normal to the faceplate.

I/O connectors mating to the module can have overmolds extending in all directions around this opening, to a **maximum of 2 mm**. This allowance will limit the effective thickness of the chassis near this region. Chassis designers should take note of what connector overmolds may be required for the connectors on the OCP DC-SCM 2 that will assemble into it.

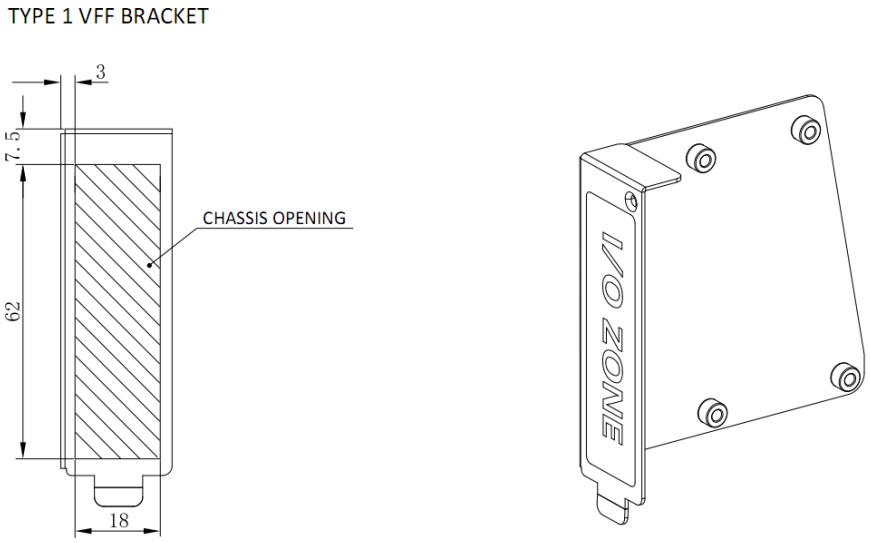



Figure 37: Type 1 VFF Bracket Chassis Bay Opening Dimensions

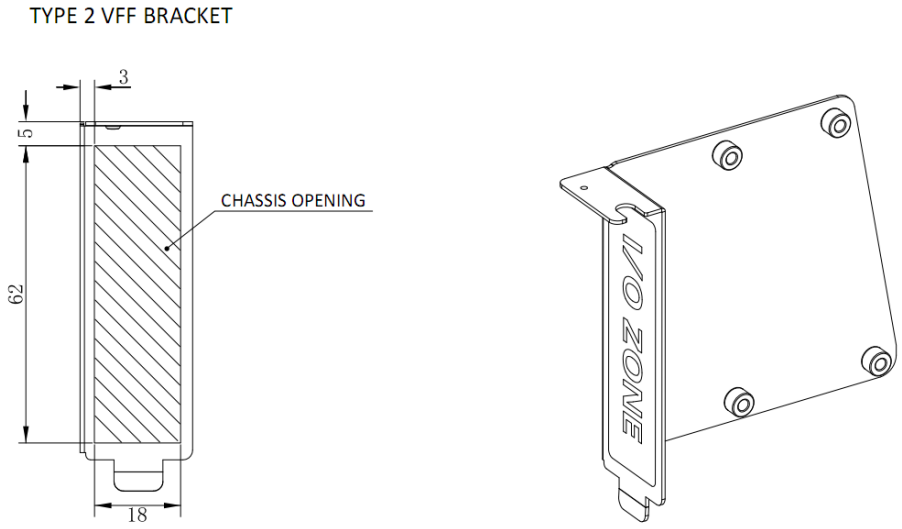



Figure 38: Type 2 VFF Bracket Chassis Bay Opening Dimensions

### 2.3.5 VFF EMI Compliance Components

In the likely event that emissions must be contained in the system and pass certain regulatory testing for EMC, proper chassis-level EMI solutions similar to PCIe AIC bracket implementations should be utilized.

# 3 Interface Definition

## 3.1 DC-SCI Card Edge Connector Definition

The DC-SCI card edge connector interface is compliant to the SFF-TA-1002 specification with respect to the 4C+ connector size. Note that while the interface is mechanically compatible with the 4C+ specification, it does not support the SFF-TA-1009 pinout definition and is therefore not electrically compatible with EDSFF nor OCP NIC 3.0 devices. The pinout is defined in a spreadsheet file separate from this document. Mechanical details of the edge finger requirements are shown in Figure 39, Figure 40, and Figure 41.

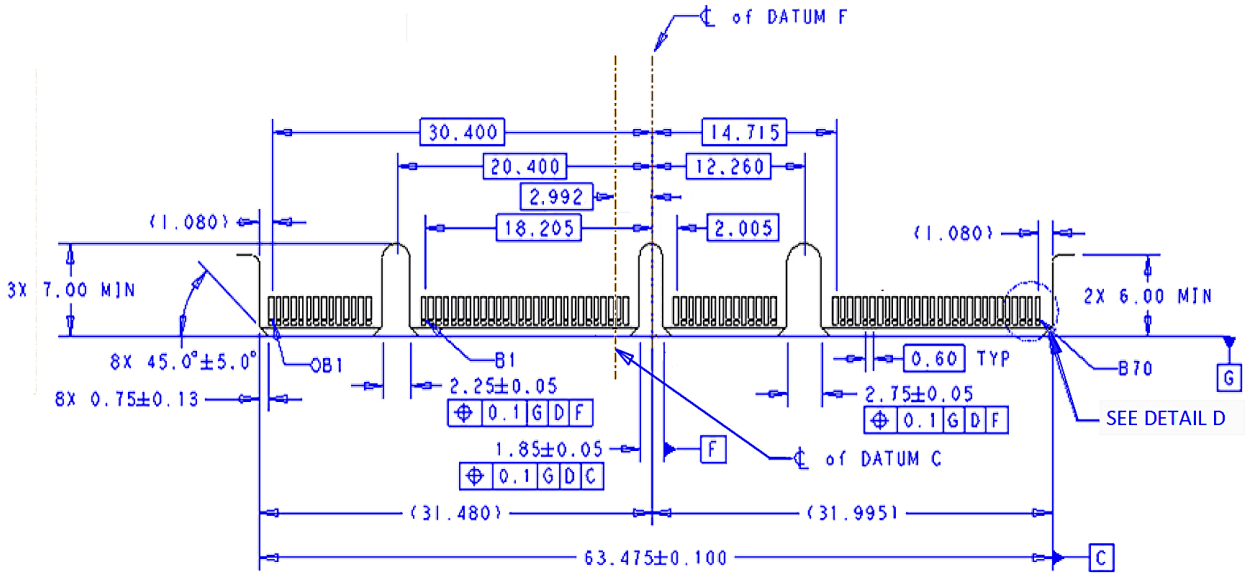



**Figure 39: Card Edge Connector Dimensions – Top Side ("B" Pins)**

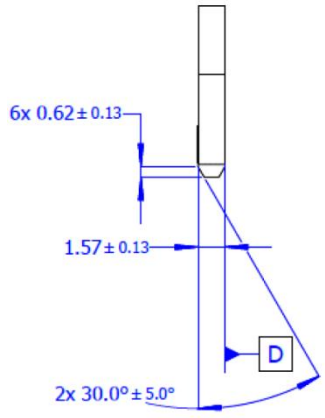



**Figure 40: Card Edge Profile Dimensions**

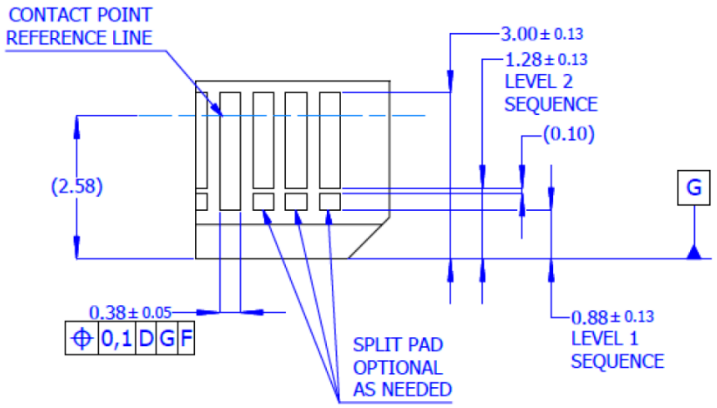



**Figure 41: Card Edge Connector – Detail D**

## 3.2 Gold Finger Plating Requirements

The minimum DC-SCM gold finger plating shall be 30 µinches of gold over 50 µinches of nickel.

## 3.3 HPM Connector Definition

The mating connector on the HPM is mechanically compliant to the 4C+ connector as defined in the SFF-TA-1002 specification for right angle, straddle mount and vertical form factor connectors. All three connector options are supported by this specification. The detailed pin list and pinout are defined in an accompanying spreadsheet document for easier reference and portability into designs.

### 3.3.1 Straddle Mount Connector

Straddle mount connectors are intended for use in designs in which the DC-SCM is installed fully co-planar to the HPM. The dimensions for the connector are shown in Figure 42.

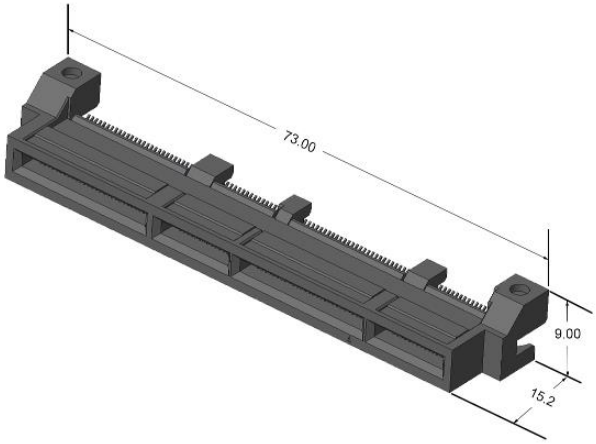



**Figure 42: Straddle Mount Connector Dimensions (in mm)**

The straddle mount connectors support four HPM PCB thicknesses. The available options are shown in Table 1. PCB thickness must be controlled to within ±10%. Note that the DC-SCM PCB thickness is required to be 0.062” (1.57 mm) while the HPM PCB thickness can vary from 0.062” (1.57 mm) to 0.110” (2.79 mm).

**Table 1: Straddle Mount Connector PCB Thicknesses**

| Connector | Mating (SCM) PCB Thickness | Host (HPM) PCB Thickness |
|---|---|---|
| A | 0.062” (1.57 mm) | 0.062” (1.57 mm) |
| B | 0.062” (1.57 mm) | 0.076” (1.93 mm) |
| C | 0.062” (1.57 mm) | 0.093” (2.36 mm) |
| D | 0.062” (1.57 mm) | 0.105” (2.67 mm) |
| E | 0.062” (1.57 mm) | 0.110” (2.79 mm) |

The choice of HPM PCB thickness impacts the offset of the DC-SCM with respect to the HPM PCB. This needs to be accounted for in the system design. Table 2 and the accompanying Figure 43 and Figure 44 details the PCB thickness and offset supports for the connector options.

**Table 2: Straddle Mount Connector PCB Offsets**

| Name | Pins | Style and Baseboard Thickness | Offset (mm) |
|---|---|---|---|
| 4C+ | 168 | 0.062” (1.57 mm) | Coplanar (0 mm) |
| 4C+ | 168 | 0.076” (1.93 mm) | -0.3 mm |
| 4C+ | 168 | 0.093” (2.36 mm) | Coplanar (0 mm) |
| 4C+ | 168 | 0.105” (2.67 mm) | Coplanar (0 mm) |
| 4C+ | 168 | 0.110” (2.79 mm) | Coplanar (0 mm) |

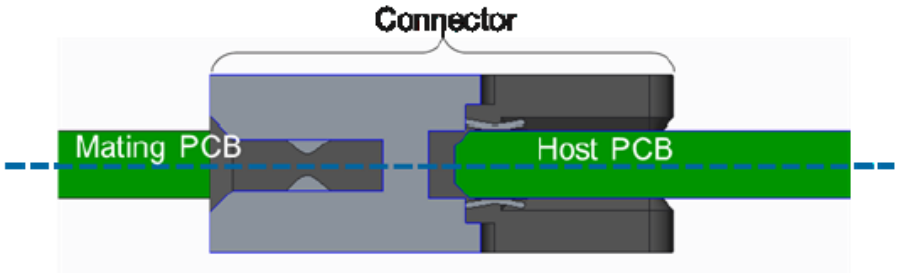



**Figure 43: Straddle Mount Connector 0mm Offset for 0.062”, 0.093”, and 0.105” HPM PCB**

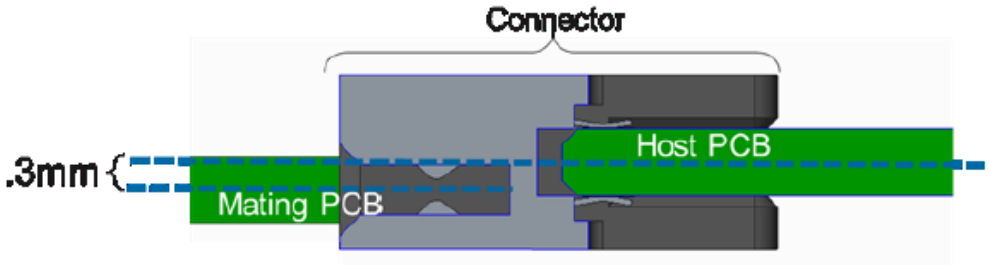



**Figure 44: Straddle Mount Connector -0.3 mm Offset for 0.076” HPM PCB**

### 3.3.2 Right Angle Connector

Right angle connectors are intended for a similar use but enable an increased DC-SCM bottom side keep out. Use of a right-angle connector eliminates any impact of the HPM PCB thickness with relation to the connector offset ensuring a constant 4.05 mm offset for all designs. The dimensions for the connector are shown in Figure 45.

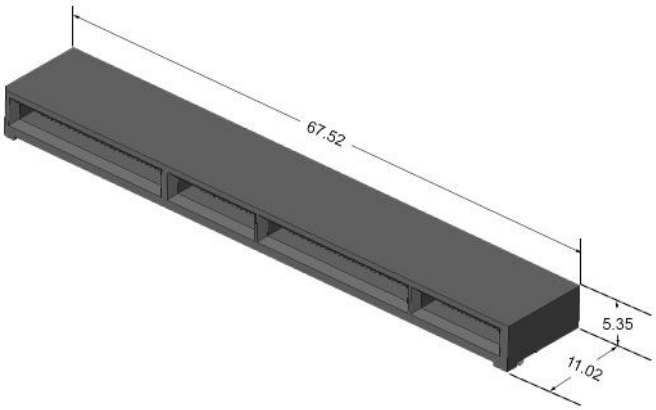



**Figure 45: Right Angle Connector Dimensions (in mm)**

Figure 46 details the PCB thickness and offset supports for this connector option.

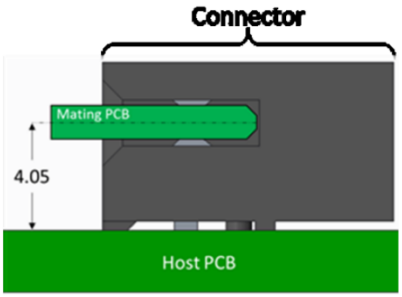



**Figure 46: Right Angle Connector Offset**

### 3.3.3 Vertical Connector

Vertical connectors are intended for use in vertical form factors. The dimensions for the connector are shown in Figure 47.

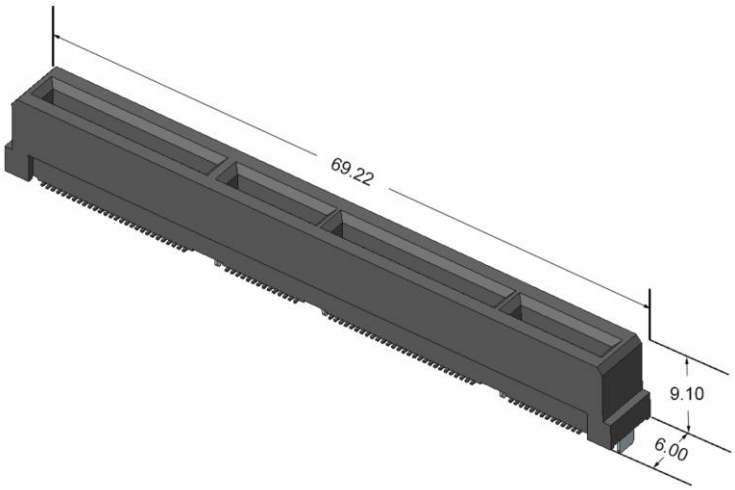



**Figure 47: Vertical Connector Dimensions (in mm)**

## 3.4 DC-SCI Pin Definition

An overview of the alternative interfaces supported by OCP DC-SCM 2 connector pinout is shown in the Figure 48 for the Single Node DC-SCI pinout and in the Figure 49 for the Dual Node DC-SCI Pinout. below.

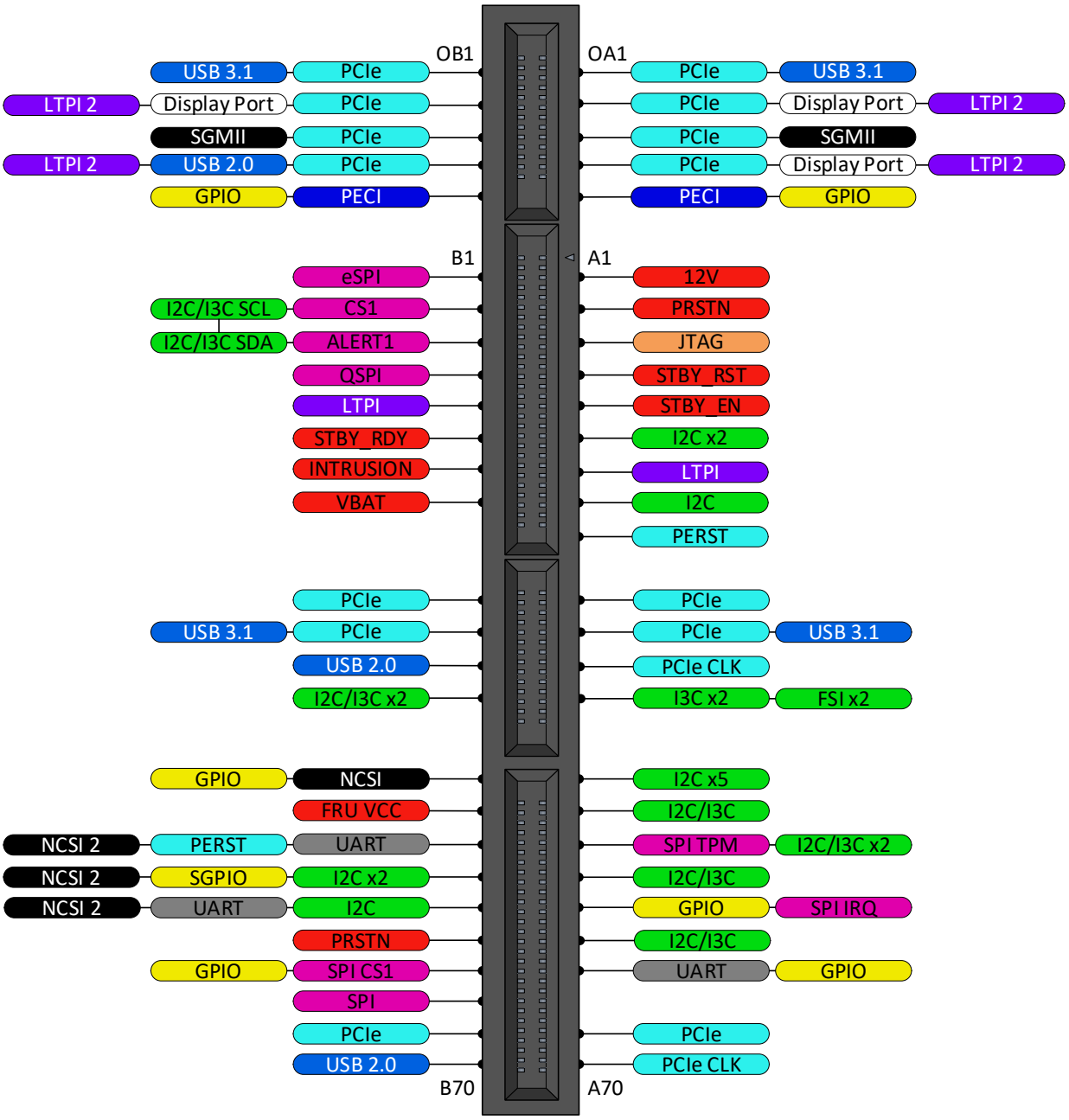



Figure 48: Single Node Pinout Overview

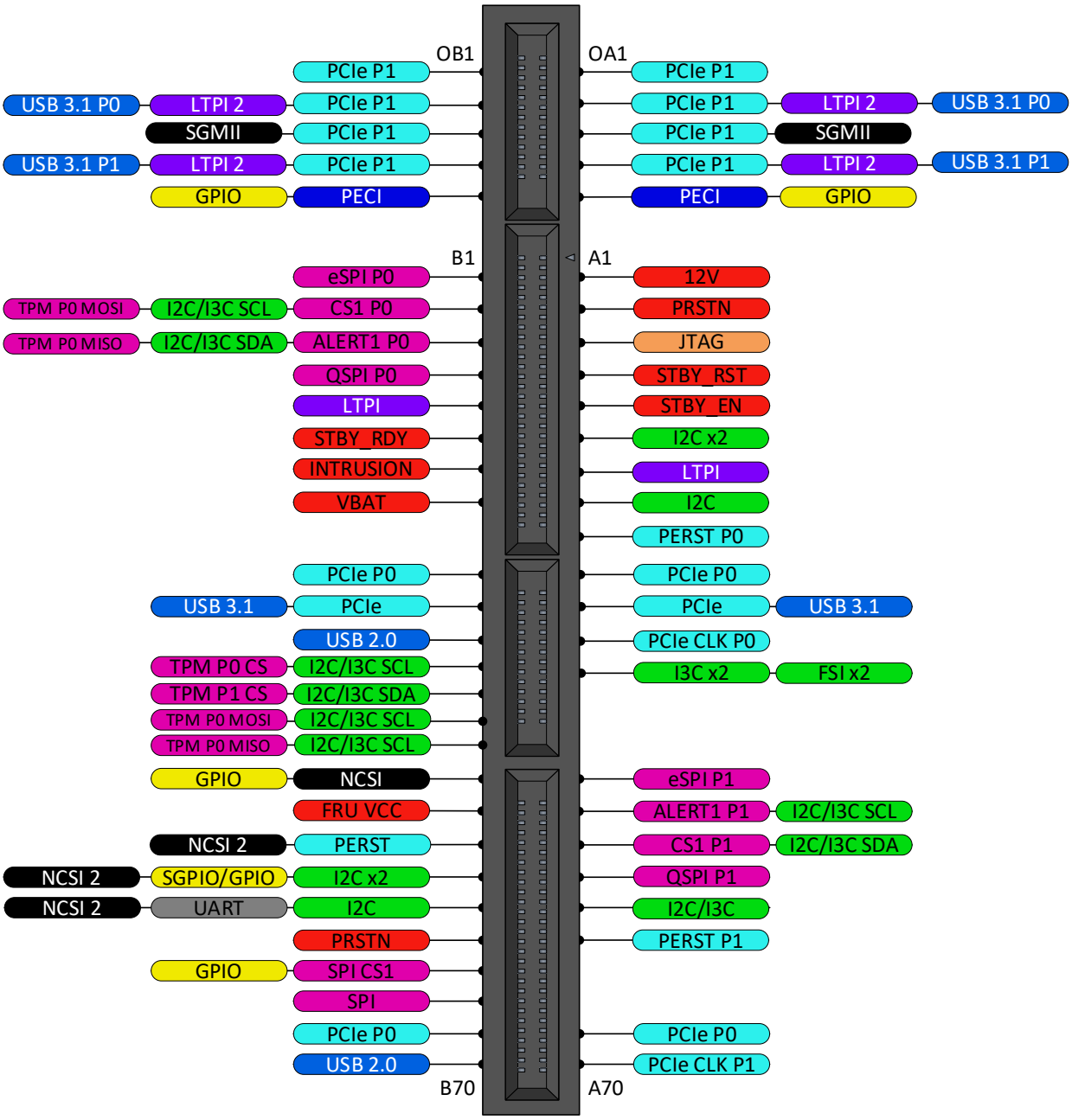



**Figure 49: Dual Node Pinout Overview**

The detailed pin list and pinout are defined in an accompanying spreadsheet document for easier reference and portability into designs. This is defined with the following rules:

- The pin list includes each signal name (preferred HPM and DC-SCM board net names that include functional and directional nomenclature), gold finger lengths, single & dual node usages, voltage, direction, and typical usage details. As much signal ambiguity as possible was removed from signal names as well as duplication of such parameters in individual interface sections within this specification.

- Multi-function DC-SCI pins list the functions starting with the most typical expected usage first.
- When multiple voltages are listed for a signal, they follow the respective alternate pin function order. If a voltage differs between single and dual node, it is described as such.
- The contact sequence for each pin indicates the order in which the pins make contact between the HPM and the DC-SCM. The GND pins are required to be long pins or 1st mate. The PRSNT0_N/ PRSNT1_N pins and P12V_AUX pins are required to be short pins or 2nd mate. However, the remaining pins indicated as 2nd mate can be flexibly assigned as long pins/1st mate if dictated by design or DFM requirements.

## 3.5 DC-SCI Signal Descriptions and Examples

The detailed signal names and descriptions are included in the accompanying spreadsheet, utilizing the notation of: ***function_(bus source)_(signal source)_(signal destination)_Instance#_Node#_Polarity***
Example: PCIE_HPMROOT_HPM_SCM_P1_N
Implementers should reference the relevant bus specifications for frequencies, signal integrity aspects and functional details. There is no attempt to duplicate such information here.
For any mature industry standard interfaces, it is expected that the design of the DC-SCM follows the standard practice regarding signal treatment guidelines and requirements.

### 3.5.1 HPM to SCM PCIe

#### 3.5.1.1 HPM to SCM PCIe Lanes

The DC-SCI supports several PCIe bus options between the HPM and the DC-SCM.

- Typically, PCIe Gen 2.0 but supportable up to PCIe Gen 5.0 x1 Interface (pins A30-B31): This interface is typically connected to a BMC as a PCIe endpoint for usages including enabling host to BMC communication for functions such as video, MCTP over PCIe VDM, memory mapped PCIe device and/or a USB controller.
- Typically, PCIe Gen 2.0, but supportable up to PCIe Gen 5.0 x1 Interface (pins A65-B66): This is typically connected to a USB host controller, due to a trend of less hosts providing such functionality.
- Up to PCIe Gen 5.0 capable x4 Interface (pins OA2-OB12): This interface enables the HPM to communicate with endpoint(s) on or downstream of the DC-SCM. The bus may be link subdivided as 1 x4, 2 x2 lanes, 4 x1 or x2 x1 x1 lanes. Additionally, multi-node HPMs may choose to provide upstream ports split between nodes.

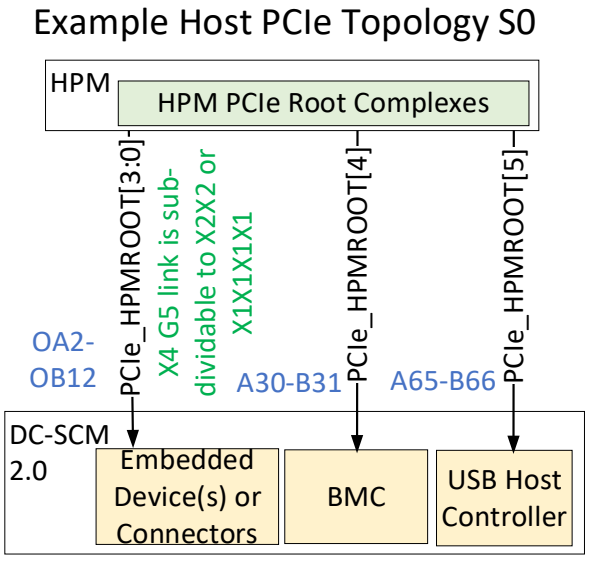



**Figure 50: Host PCIe Mapping Example**

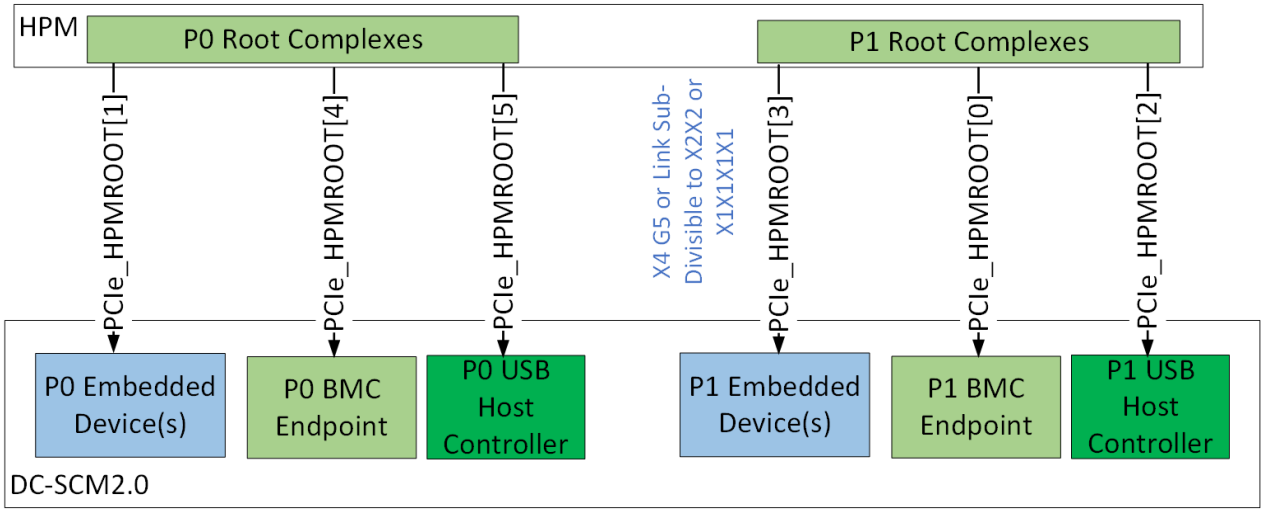



**Figure 51: Dual Node PCIe Example**

### 3.5.1.2 HPM to SCM PCIe Clocks

The DC-SCI supports 2 HPM provided clock interfaces. In a typical scenario, PCIE_HPM_SCM_CLK_100M_0 is expected to feed the X4 endpoint (e.g., Gen5 compatible) and PCIE_HPM_SCM_CLK_100M_1 feeds other slower devices (such as via a clock buffer to fan out to endpoints such as the BMC and USB host controller).
The general expectation is that all DC-SCM host PCIe endpoints are within the same clocking domain as each other, else separate reference clock methods may be necessary.

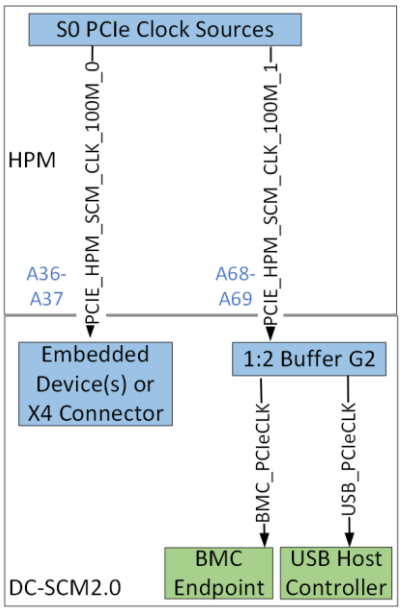



**Figure 52: Typical Host PCIe Clocking Example**

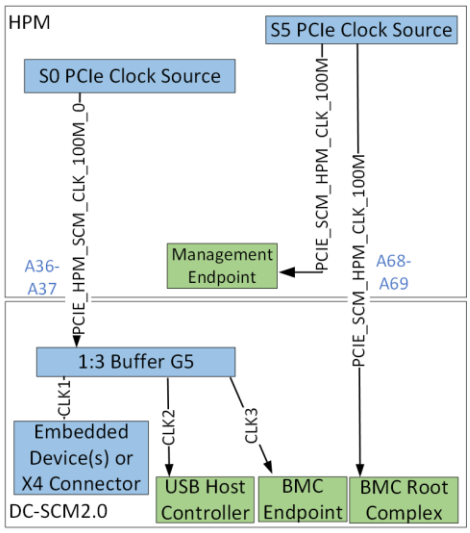



**Figure 53: Alternate PCIe Clocking Example (When BMC Root Needs a Clock)**

#### 3.5.1.3 HPM to SCM PCIe Resets

**Host PCIe Reset:** There is one PCIe Reset signal per node from the HPM to the SCM intended for the PCIe host domain. The host domain control over the PERST signals varies such as being synchronous to platform reset, host firmware or HPM FPGA controlled. Usage and timings are out of scope of this specification. Scenarios where individual endpoint PERST control is required are also out of scope. An example may be when the platform chooses to use the BMC video controller before the host domain is initialized.

**BMC PCIe Reset:** Pin B51 can optionally be used for a BMC PCIe root complex discrete PERST# to endpoints on the HPM. Else, designers may choose to send the BMC PERST# over LTPI as a virtual wire.

### 3.5.2 SCM to HPM PCIe

#### 3.5.2.1 SCM to HPM PCIe Lane

Pins A33-B34 offer three potential mutually exclusive use cases: 1) BMC acting as a PCIe root complex – This section; 2) Host domain passing from a PCIe switch a X1 back into the HPM or 3) USB3.1.

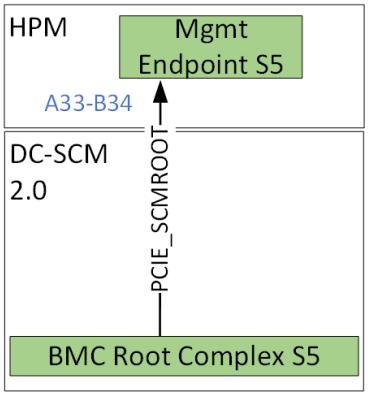



**Figure 54: BMC PCIe Root Complex Example**

Note: pins A68-A69 are the same as in the HPM to SCM PCIe clocking example with a different alternate signal name based on usage.

### 3.5.3 SPI / QSPI / TPM_SPI

For single node mode, the DC-SCI supports three SPI interfaces:

- QSPI_HPMCNTRL: HPM is the initiator. This enables HPM communication with the BIOS flash devices on the DC-SCM. Only one QSPI bus is defined for a single-node design and two for a dual-node design.
- SPI_HPMCTRL_TPM: HPM is the initiator. This enables some hosts to have a dedicated TPM SPI bus. Other hosts utilize a dedicated CS on QSPI. In the latter mode, the other SPI pins are not usable except for alternate functions (e.g., I2C_I3C_1V8*). A more universal DC-SCM may provide the appropriate MUX logic for FW to steer the bus properly during the HPM discovery phase.
- SPI_SCMCNTRL: DC-SCM is the initiator. This enables DC-SCM communication with expansion devices on the HPM such as the HPM FPGA. Note that 1 SPI_HPM_SCM_IRQ0_N discrete signal is provided, like in DC-SCM 1.0. Other shared or non-shared interrupts must be via LTPI.

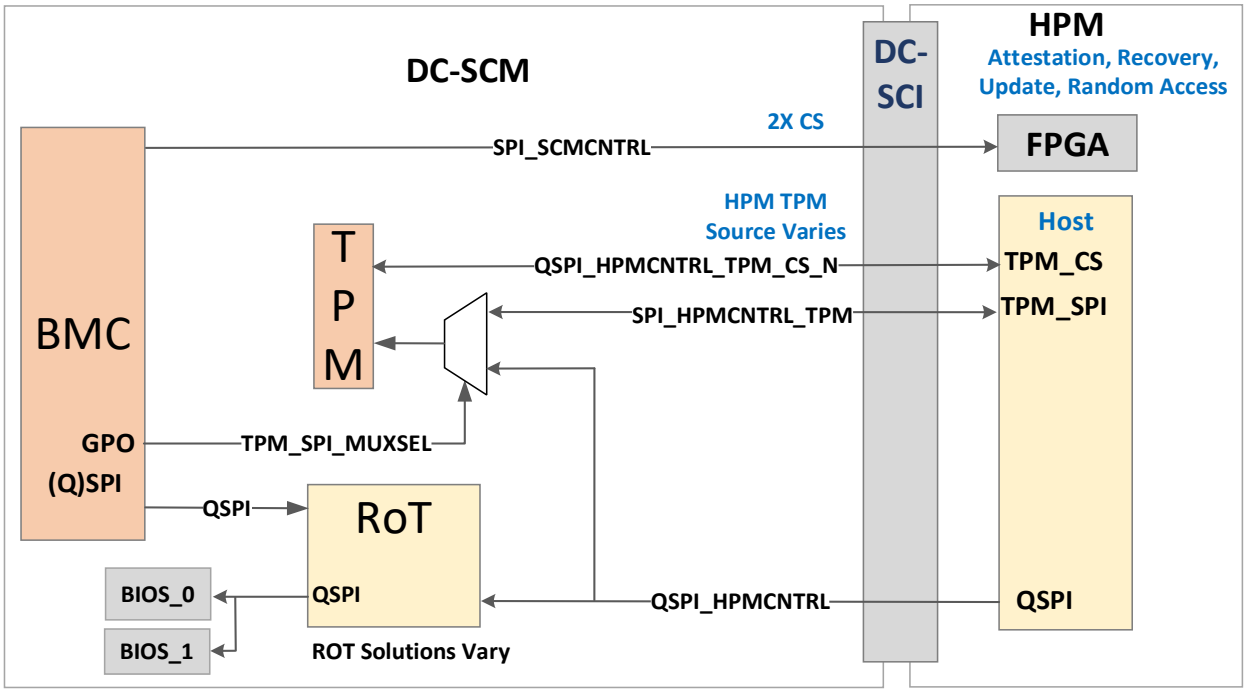



Figure 55: SPI Example Block Diagram

For Dual node, the 2.1 specification added two SPI interfaces as the primary functions for TPMs to be placed on the DC-SCM. Another option to connect the TPMs is to use the QSPIs and a dedicated TPM chip select.

### 3.5.4 NC-SI RBT

The DC-SCI supports up to 2X RMII/NC-SI RMII-based Transport interfaces from the DC-SCM to the HPM. Applications using one NC-SI, should use the 1st interface instance (pins B43-B49). Platforms utilizing two NC-SI interfaces may choose to do so for either redundancy or signal integrity improvements or for use with each of up to two nodes. This interface enables high speed sideband management to NIC(s).
Note: To best account for timing requirements associated with the 50MHz +/-100 ppm NC-SI clock, it is assumed that the clock source is located on the HPM. More timing guidance is provided later in this specification.
RXERR was removed in 2.0 since it is optional and not used in most scenarios and the pin was deemed more valuable for alternate functions.

### 3.5.5 eSPI

In single node configurations 1 HPM to SCM eSPI bus is provided. This includes CS1/ALERT1 in the DC-SCI, although the more typical scenario is to have CS1/ALERT1 terminate with the HPM FPGA, as shown in the picture below. Even though known hosts vary in their need for utilizing eSPI in S5, they are tolerant to S5 bias. Note that it is expected that CS0/ALERT0 are used for the BMC, regardless of if the HPM FPGA or SCM CPLD utilize eSPI (CS1/ALERT1). Multi-node provides a second full eSPI interface. There is no LPC bus support for either mode. Host to BMC interface details when eSPI is unavailable are outside the scope of this specification.

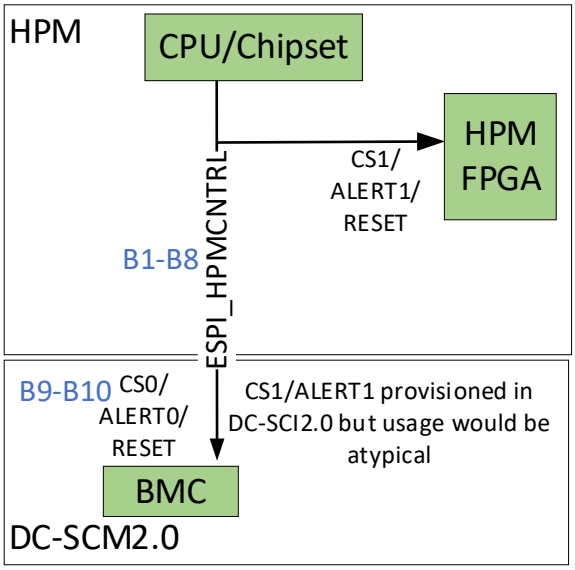



**Figure 56: ESPI Example Block Diagram**

### 3.5.6 LTPI

The DC-SCI defines the LVDS Tunneling Protocol & Interface (LTPI). It uses a total of 8 x CPLD/FPGA LVDS differential I/O pins for connecting the SCM CPLD/FPGA with HPM CPLD/FPGA.

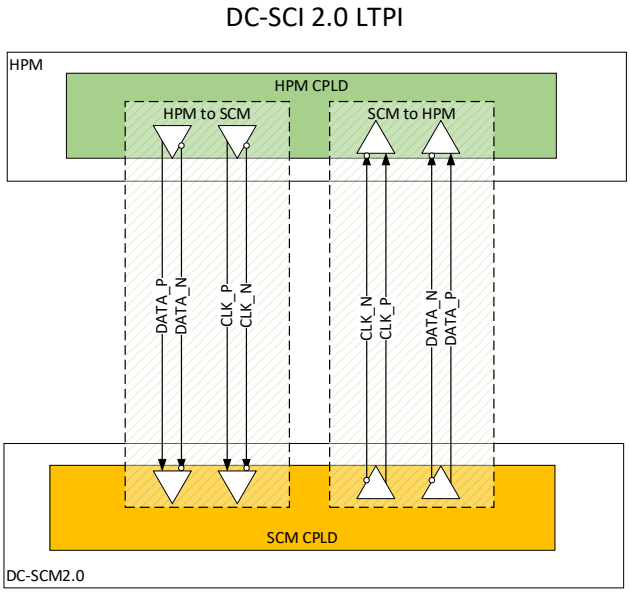



**Figure 57: DC-SCI LVDS differential channels between SCM and HPM**

There is a total of 4x LVDS unidirectional links defined for HPM-to-SCM and SCM-to-HPM communication. The links in each direction are defined by 2 x LVDS-based channels i.e., DATA and CLOCK. The description of the LTPI I/O pins and the direction of LVDS links from SCM CPLD and HPM FPGA is listed in TableTable 3 below.

**Table 3: LVDS Signal Descriptions**

| Function | HPM CPLD LVDS I/O | SCM CPLD LVDS I/O |
|---|---|---|

| | | |
|---|---|---|
| LTPI_HPM_SCM_DATA_DN | TX Data Negative | RX Data Negative |
| LTPI_HPM_SCM_DATA_DP | TX Data Positive | RX Data Positive |
| LTPI_HPM_SCM_CLK_ DN | TX Clock Negative | RX Clock Negative |
| LTPI_HPM_SCM_CLK_ DP | TX Clock Positive | RX Clock Positive |
| LTPI_SCM_HPM_DATA_DN | RX Data Negative | TX Data Negative |
| LTPI_SCM_HPM_DATA_DP | RX Data Positive | TX Data Positive |
| LTPI_SCM_HPM_CLK_DN | RX Clock Negative | TX Clock Negative |
| LTPI_SCM_HPM_CLK_DP | RX Clock Positive | TX Clock Positive |

The LVDS link is defined as AC-coupled to allow interoperability between different CPLD/FPGA Voltage I/O standards existing today. CPLD/FPGA devices in the majority of cases have limited I/O voltage flexibility on LVDS Receiver (RX) Buffer I/O hence a voltage bias circuit is used to match the RX I/O buffer voltage requirements for given CPLD/FPGA. shows an example of AC-coupled LVDS electrical links one in each direction HPM-to-SCM and SCM-to-HPM. The OCP DC-SCM 2 LVDS links have the following characteristics:

- **DC blocking capacitor's placement:** DC-SCM module
- **Voltage bias circuit placement:** Close to LVDS RX I/O buffer

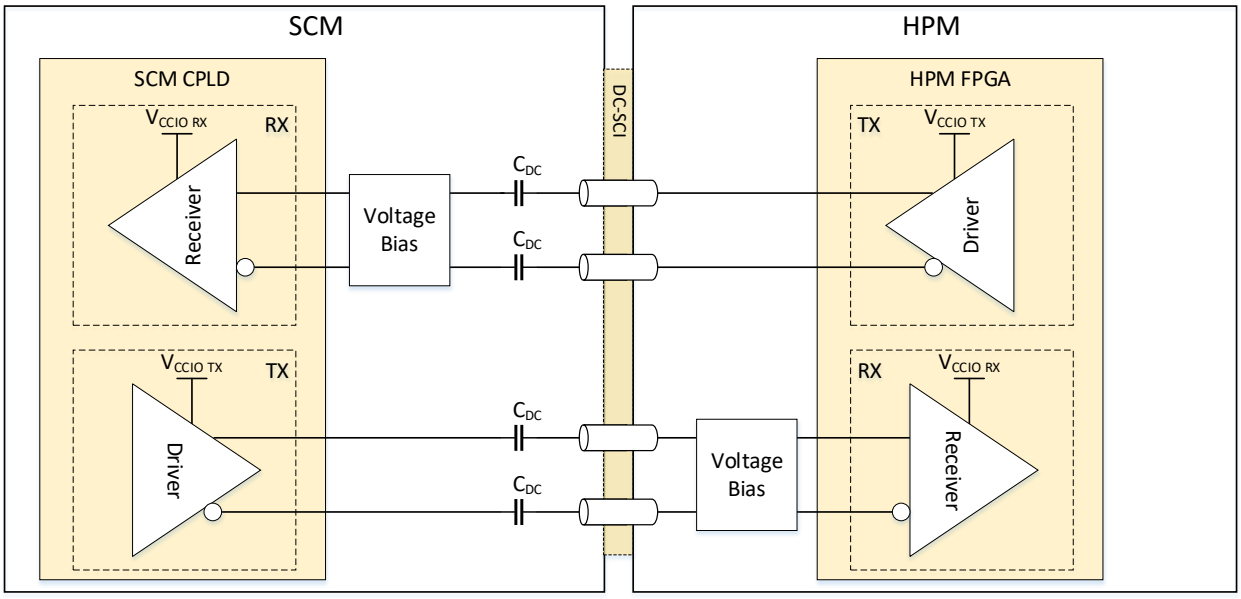



**Figure 58: LVDS Links Electrical I/O**

The example of Voltage Bias circuit for a single LVDS link is shown in Figure 59. All four LVDS links shall have a Voltage Bias circuit; as a result, two circuits shall be located on the SCM side and two on the HPM side. The Voltage Bias circuit is setting the common mode voltage for the RX buffer to meet the device requirements of SCM CPLD and HPM FPGA. The Voltage Bias circuit can also provide termination resistance. Some CPLD/FPGA devices support integrated Termination Resistor which can be used instead of external Termination Resistor presented in Figure 59. The recommended termination resistance is 100 Ohm however

the exact value shall be adjusted to match the device input buffer requirements and LTPI Electrical IO specification listed in Table 4.The DC Blocking capacitor is defined at 0.22 µF which is derived from the LTPI interface Base Frequency and interface training requirements.

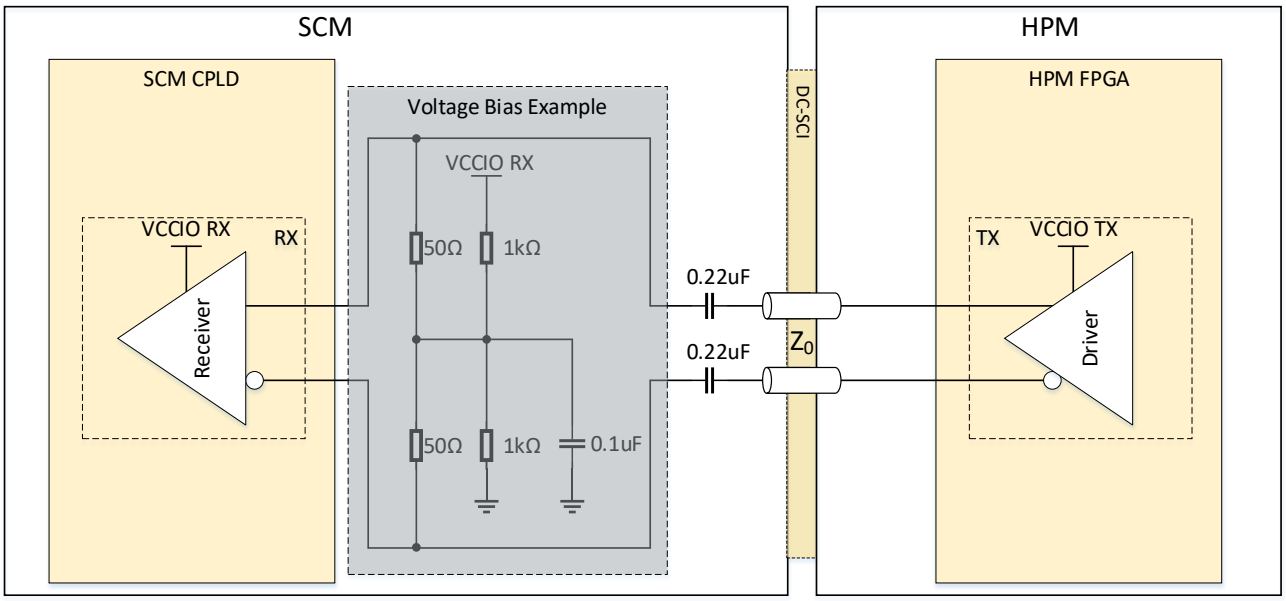



**Figure 59: Example of LVDS Voltage Bias Circuit**

The electrical specification for the OCP DC-SCM 2 LVDS links are defined in Table 4 below.

**Table 4: LVDS Electrical Requirements and Recommendations**

| Parameter | Min. | Max. | Description |
|---|---|---|---|
| $V_{OD}$ | 100 mV | 800 mV | Output Differential Voltage Swing |
| $V_{ID}$ | 100 mV | 800 mV | Input Differential Voltage Swing |
| $V_{CCIO\ RX/TX}$ | N/A | Device Maximum | LVDS VCCIO Voltage (Refer to CPLD/FPGA documentation) |
| | | | |
| $C_{DC}$ | 0.22 uF | N/A | DC blocking capacitor |
| $R_{TT}$ | 100 Ohm - 5% | 100 Ohm + 5% | Reference LVDS Termination Resistor Value (External or Integrated). The exact value shall be adjusted as part of bias circuit design to match the device Rx buffer requirements. |
| $Z_0$ Nominal | 85 Ohm | | Recommended Nominal differential impedance value. |

*Note: The bias circuit defined on Figure 59 is just an example. An HPM/SCM designer shall refer to the CPLD/FPGA device datasheet for details of the Rx input buffer requirements and adjust bias circuit accordingly.*

The details of LTPI interface are covered in the OCP DC-SCM 2 LVDS Tunneling Protocol and Interface (LTPI) Specification 1.0.

### 3.5.7 I2C / I3C

The DC-SCI 2 expands the I2C/I3C bus scenarios. HDR-BT (Bulk Transport) mode of operation is not supported in the DC-SCI. HDR-DDR mode of operation is not precluded for use, but no efforts were spent to ensure proper operation is guaranteed. Designers should carefully refer to this specification in terms of supported modes of operation, use of MUXes or hubs, discovery protocols, etc.
The I2C bus mappings differ between the single-node and the dual node configurations. For a single-node design, the DC-SCI supports a total of 18 possible I2C ports from the DC-SCM to the HPM. These are allocated to two voltages across 10X at 3.3 V and 8X at 1.8 V for either I2C or I3C. The rules are as follows:

1) HPM must provide the appropriate pullup resistors for I2C buses.
2) HPM is responsible for providing cross power domain (AUX to Main) & necessary voltage level translation if targets differ from the DC-SCI voltage.
3) More I2C/I3C controllers are not precluded via controllers/ or bridges on interfaces such as PCIe, USB, LTPI, SPI or I3C to SMBUS hubs.
4) There is no explicit designation of a HPM pure Initiator to DC-SCM Target bus.
5) No discrete I2C/SMBUS alerts are included as any such needs are expected to be virtual GPIOs. I2C Alerts can optionally be supported using SPI_IRQ0, SGPIO or LTPI.
6) Fixed FRUID PROM address: It is required that on the HPM, the FRUID EEPROM be placed directly on channel I2C0 (Not behind a MUX or hub) at address 0xA0 (8-bit address). This provides a fixed location for a BMC to detect an HPM type and load the necessary platform specific parameters to ensure full functionality of the platform.
7) If an optional authentication IC is supported on the HPM, it must also exist on I2C0. The device should be on the same segment and not downstream of a MUX to simplify the discovery method.
8) Multi-initiator is generally desired to be avoided and limited only to standardized use cases like MCTP over SMBus or IPMB.

**Table 5: I2C/I3C Signal Descriptions for Single Node**

| Signal Name | Minimum Power State | Voltage (V) | Description |
|---|---|---|---|
| I2C_3 3_0 | Pre-STBY | 3.3 | HPM FRU must be connected to I2C bus 0 for universal compatibility.<br>If an optional authentication IC is supported on the HPM, it must exist on this bus. |
| I2C_3V3_* | S5 | 3.3 | |
| I2C_I3C_1V8 | S5 | 1.8 | I2C/I3C or various other signals |
| I2C_I3C_1V0 | S5 | 1.0 | I2C/I3C or FSI |

For a dual-node design, there are 6X I2C at 3.3V and 3X I2C at 1.8V. The 1.8 V I2C could be used for I3C. The bus numbers are not continuous to better match the single node naming convention.

**Table 6: I2C/I3C Signal Descriptions for Dual Node**

| Signal Name | Minimum Power State | Voltage (V) | Description |
|---|---|---|---|

| | | | |
|---|---|---|---|
| I2C [0] | Pre-STBY | 3.3 | HPM FRU must be connect to I2C bus 0 for universal compatibility |
| I2C [1:2] | S5 | 3.3 | These are dedicated I2C buses at 3.3 V |
| I2C [7] | S5 | 3.3 | I2C or 2nNCSI signals |
| I2C [8] | S5 | 3.3 | I2C or 2ndNCSI signals |
| I2C [9] | S5 | 3.3 | I2C or 2nd NCSI signals or UART1 |
| I2C/I3C [3:5] | S5 | 1.8 | I2C or I3C |
| I2C_I3C_1V0 | S5 | 1.0 | I2C/I3C or FSI |

### 3.5.8 FSI

OpenPower Flexible Service Interface (FSI) is supported as alternate functions on these interfaces.

**Table 7: FSI Signal Descriptions**

| Signal Name | Minimum Power State | Voltage (V) | Description |
|---|---|---|---|
| I2C_I3C_1V0_##_SCL / FSI_1V2_#_SCL | S5 | 1.0 | Shared with FSI buses, I2C/I3C at 1.0 V only OR FSI at 1.2 V only |

### 3.5.9 USB

#### 3.5.9.1 Host USB

- As there is a trend in some chipsets to not support native USB host controllers, a space and cost-effective way to support host USB is via a PCIe X1 to USB host controller on the DC-SCM. This supports connections to the BMC, local and internal/external ports, and devices.
- In cases where a platform wants to support host domain USB 3.2 Gen1 devices or fanout on the HPM and native chipset USB host controllers are not available nor an additional PCIe to USB host bridge on the HPM is desired, the USBx_SCMHOST busses are available to be part of the HPM host domain. This is different from the BMC USB management domain. It is recommended to take caution with cross power domain connections since the same pins can be used with host and/or devices within the AUX S5 or Main S0 power domains.
- Two optional HPM_SCM USB 2.0 interfaces are available for legacy design where the host chipset retains USB2.0 host controllers/initiators. There are no USB 3.2 Gen1 HPM_SCM interfaces provided in DC-SCI 2.

#### 3.5.9.2 Managed USB

- USB2_SCM_HPM may be used as the BMC managed USB host controller connectivity to the HPM for a high-speed management interface to various subsystems and extended peripherals.

- USB2_BMC_SCMOTG as a BMC managed USB interface may have the BMC serving as the USB host or device with static or dynamically changing roles (On-The-Go). A typical use case includes an external “service port”.
- USB3_SCMROOT_SCM_HPM is available as a managed USB interface for future BMCs or could be supported via the BMC PCIe root complex connected PCIe to USB bridge.

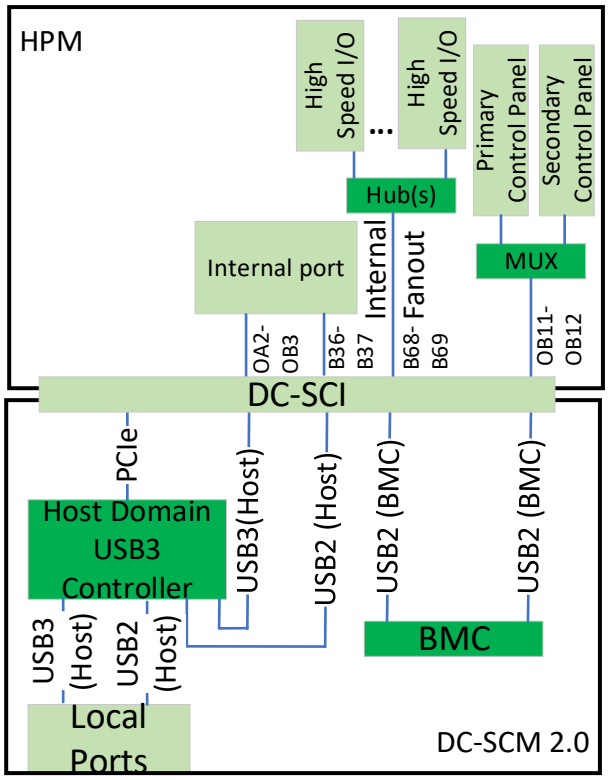



Figure 60: Example USB Block Diagram

Note:
For all DC-SCI traversing USB 3.x TX lanes, where SCM is the source and HPM is the destination, the transmit pair AC capacitors defined by the USB Specification shall be placed on the DC-SCM.
If the bus terminates on the HPM (i.e., USB device or hub), then the AC Capacitor for corresponding USB 3.x TX lane, where HPM is the source and SCM is the destination, shall be placed on the HPM.
If the bus goes directly to an HPM USB Connector, then the AC Capacitor for corresponding USB 3.x TX lane, where HPM USB Connector is the source and SCM is the destination, is expected to be on the device attached to the USB connector.

### 3.5.10 PECI

The DC-SCI supports an optional PECI interface (bus + power) for health monitoring of CPUs. When this interface is un-used by the HPM architecture, it should be appropriately terminated on the HPM, refer to CPU vendor and BMC vendor specifications for detailed PECI electrical IO requirements. Note that the BMC controller PECI interface requires voltage to be supplied by the HPM.

When the PECI interface is not used on both the HPM **AND** DC-SCM the PECI_HPM_SCM signal may be used as a low voltage (0.85 V-1.21 V) GPIO biased only in host MAIN on S0 state. Also, PECI_VREF_HPM_SCM may be used as a unidirectional signal from HPM to SCM in the same voltage range. Direction is limited due to the nature of this being a power signal in PECI operation.

### 3.5.11 UART

The DC-SCI supports two UARTs (3.3 V, TTL logic) with no hardware flow control signals. Typical uses are:

• UART0 - Host Debug Console (typically when not eSPI mapped)

• UART1 – Subsystem consoles (Smart NICs, RAID cards, etc.)

Additional physical UARTs may be supported through alternate interfaces like USB, PCIe, LTPI and SPI.

### 3.5.12 Battery Voltage

The DC-SCI supports one pin for 3.0 V battery power from the HPM.

**Table 8: Battery Voltage**

| Signal Name | I/O | Voltage | Description |
|---|---|---|---|
| P3V0_HPM_SCM_BAT | I | 3.0 V | 3.0 V from coin cell battery located on HPM. Typical uses are RTC, CMOS and chassis intrusion logic Battery backed CPU registers, etc.<br>DC-SCM current consumption from this rail will impact the HPM battery life and HPM shelf storage time. This should be comprehended by OCP DC-SCM 2 and HPM designs. Typical OCP DC-SCM 2 design shall not pull more than 1.2uA.<br>DC-SCM must not source energy into HPM on this signal.<br>When the battery is not in use, drain should only occur during measurement sampling of raw BAT rail. |

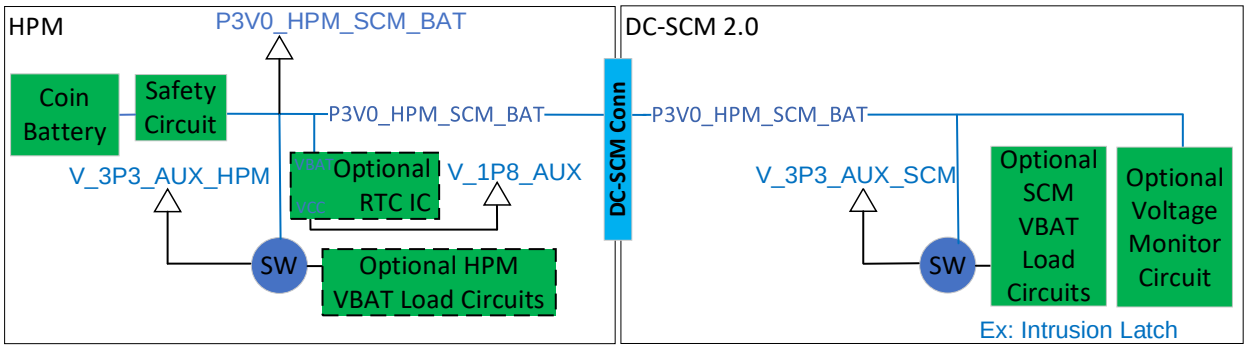



**Figure 61: Battery Circuit**

### 3.5.13 Intrusion

HPM_SCM_INTRUSION_N is the optional 3.3 V DC-SCI 2 input (unidirectional) signal from the HPM. Therefore, the general expectation is that optional chassis intrusion switch connectivity is to the HPM.

Note: active low designation is because the expectation is to use an intrusion button that is open when depressed (not intruded) and closed when released (cover removed).

### 3.5.14 JTAG

The DC-SCI supports a BMC-initiator JTAG interface with possible uses of:

- HPM programmable device update (e.g., FPGA).
- Debug of ASICs or CPUs, often referred to as either at-scale or closed box debug. The design and security-related issues/constraints related to this interface are outside the scope of this specification.

The DC-SCI 2.1 JTAG signal naming and direction follows IEEE 1149.1 definition which is relative to the target device.

Note: The DC-SCI 1.0 and 2.0 release did not follow the IEEE 1149.1 definition of the direction of JTAG TDI and TDO signals. It was fixed in the DC-SCI 2.1 update.

### 3.5.15 SGPIO Requirements

SGPIO timing and voltage requirements for the DC-SCM shall follow DC-MHS latest M-PIC Revision 1.0 specification and errata. The waveform and tables below are from M-PIC version 1.03.

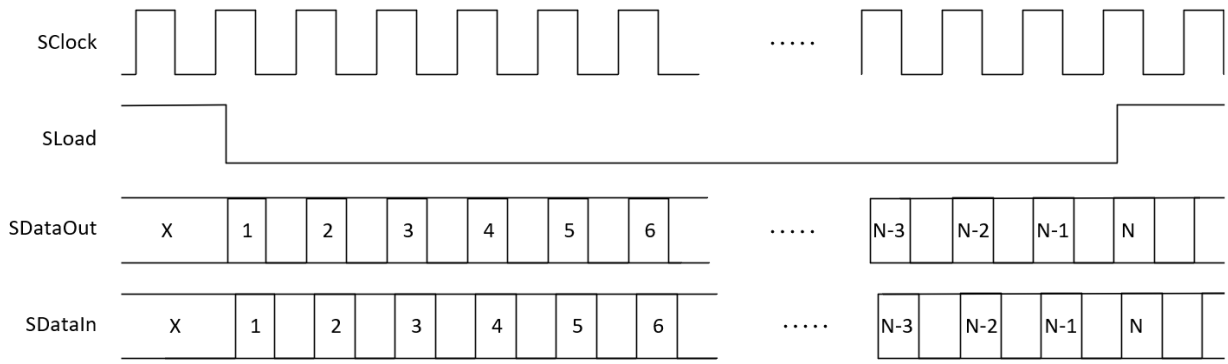



**Figure 62: Example of a SGPIO Transaction Waveform**

#### 3.5.15.1 SGPIO Timing Requirements

The passive DC-SCM interconnect shall be implemented per Table 169.

**Table 9: Passive Interconnect Requirements**

| Parameter | Symbol | Minimum | Maximum | Unit | Notes |
|---|---|---|---|---|---|
| Skew between SClock and SLoad, SDataOut, and SDataIn signal lines on SCM | $T_{SKEW}$ | - | 10 | ps | |

**Table 10: SGPIO Timing Requirements**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| SClock Frequency | $f_{CK}$ | 5 | 25 | MHz | SCM should be designed to support up to $f_{CK\ MAX}$ but the system may operate at lower frequencies because of cable and PDB loading. |
| SClock Duty Cycle | $t_{DUTY}$ | 45 | 55 | % | Measured at the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ of SClock |
| Rise time | $t_R$ | - | 6 | ns | Measured from $V_{IL\ MAX}$ to $V_{IH\ MIN}$. |
| Fall time | $t_F$ | - | 6 | ns | Measured from $V_{IH\ MIN}$ to $V_{IL\ MAX}$. |
| Setup time | $t_{SU}$ | 0 | - | ns | Measured from $V_{IL\ MAX}$ for SLoad, SDataOut, and SDataIn to the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ (on the falling edge) of SClock |
| Hold time | $t_H$ | 2 | - | ns | Measured from the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ (on the falling edge) of SClock to $V_{IL\ MAX}$ for SLoad, SDataOut, and SDataIn |

#### 3.5.15.2 SGPIO Voltage Requirements

The SGPIO signaling levels shall be compatible with 3.3V LVCMOS technology and meet the transmitter and receiver electrical requirements in Table 161.

**Table 11: SGPIO Transmitter and Receiver Electrical Requirements**

| Parameter | Symbol | Mini | Maxi | Unit | Notes |
|---|---|---|---|---|---|
| IO Voltage | $V_{CC\ IO}$ | 3.135 | 3.465 | V | |
| High level input voltage | $V_{IH}$ | 1.7 | 3.465 | V | |
| Low level input voltage | $V_{IL}$ | -0.3 | 0.8 | V | |
| High level output voltage | $V_{OH}$ | $V_{CC\ IO}$ -0.4 | - | V | |
| Low level output voltage | $V_{OL}$ | - | 0.4 | V | |
| IO Capacitance | $C_{I/O}$ | - | 8 | pF | |

## 3.6 Power States & Boot Sequence

The common power state nomenclatures are described below. All signals in the DC-SCI are categorized into each of these states indicating the minimum power state where bias is allowed at the DC-SCI.

The DC-SCM is not specified to support hot insertion or removal. In-rush control for the DC-SCM should be supported on the HPM to protect the circuitry from damage due to damaged connector pins, accidental removal.

Note: stated path or error condition handling aspects of the boot sequence are beyond the scope of this specification. The DC-SCI provides two active low presence pins. The HPM design is recommended to ensure that AUX power to the DC-SCM and HPM circuits are disabled when presence is not detected. A presence enabled eFuse may be used on the HPM but can be excluded provided the DC-SCM is locked with screws or other mechanical solutions.

**Table 12: Power Sequence Signal Descriptions**

| Signal Name | I/O | Voltage (V) | Description |
|---|---|---|---|
| PRSNT0_N | O | 3.3 | Must be connected to PRSNT1_N on the DC-SCM. Must be pulled up on the HPM and used to enable power to the SCM. |
| PRSNT1_N | I | 3.3 | Must be connected to PRSNT0_N on the DC-SCM. Must be connected to GND on the HPM |
| HPM_STBY_EN | O | 3.3 | Active High. Indicates that all DC-SCM STBY power rails are enabled and good. Enables STBY power rails on the HPM |
| HPM_STBY_RDY [1.] | I | 3.3 | Active High. Indicates that the HPM STBY power sequence is complete and all STBY rails are good. |
| HPM_STBY_RST_N | O | 3.3 | Active Low. Holds HPM standby devices in reset. Driven high by the DC-SCM to bring the standby devices on the HPM out of reset |

1. HPM_STBY_RDY: System wishing to use this pin to indicate FPGA readiness would consider the HPM FPGA startup to be part of the standby sequence.

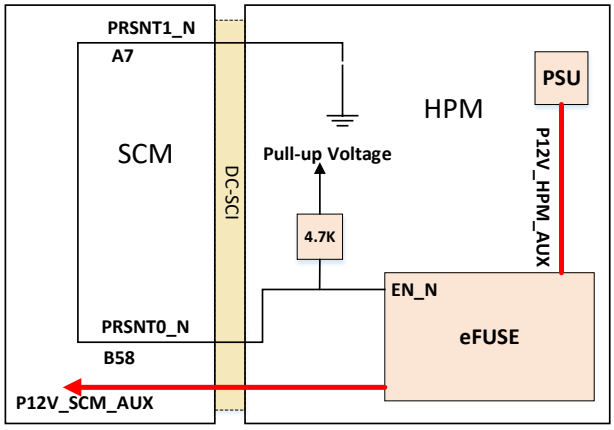



Figure 63: DC-SCM Presence Detection and Power Protection Example

This discovery sequence exists to ensure safety, avoid electrical incompatibility, and stress conditions are avoided. The following sequence is provided as a typical boot flow. It is not advised to bypass steps if interoperability is of concern.

Table 13: Power States and Discovery Sequence

| Power State | Description | Notes |
|---|---|---|
| **G3** | No PSU Input power. The only bias is coin cell. | 1 |
| **Pre-STBY** | 1: PSU input power delivers P12V_HPM_AUX output power<br>2: DC-SCM fully seated enables the HPM eFuse (if present – see example above), providing power to the DC-SCM.<br>3: SCM AUX VRs regulate, including VCC_SCM_HPM_FRU<br>4: SCM BMC boots (preceded by discrete PROT if it exists) to a point to read the I2C HPM FRU (required)<br>& performs HPM crypto authentication (optional)<br>5: Upon compatibility check pass, SCM asserts SCM_HPM_STBY_EN | 2<br>3 |
| **STBY** | 6: HPM asserts HPM_SCM_STBY_RDY when all HPM AUX Rails are within regulation<br>7: SCM de-asserts SCM_HPM_STBY_RST_N. | |

| | | |
|---|---|---|
| **S5** | 8: S5-classified interfaces may engage. HPMs and SCMs may choose to use SCM_HBM_STBY_RST_N as the qualifier for engaging S5 allowed DC-SCI signals.<br>9: The SCM grants the HPM FPGA to enable the host CPU/Chipset (e.g., de-assert RSM_RST_N or assert AUXPWROK) to officially enter S5. Host is OFF. This may be SCM_HBM_STBY_RST_N, virtual bit and/or via AUTH IC secure GPO.<br>10: Host WAKE request sources vary. Host power on request is typically blocked until a BMC grant so that the BMC may perform various boot and security services immediately before power on grant. | 4 |
| **S0** | 11: BMC grants power on, HPM CPLD sequences the host into a full ON / S0 state | |

Note 1: DC-SCI 1.0's Virtual_Reseat was removed from 2 because the same feature can be achieved through multiple alternate methods. The control method and aspects to guarantee AUX rail bleed off are currently beyond the scope of this specification.
Note 2: Although the DC-SCM is not intended to support hot plug or hot removal, an eFUSE is included on the HPM to protect the DC-SCM from any overcurrent events. To ensure that there are no voltage leaks between the HPM and DC-SCM, it is recommended that pullup resistors for all I/O on the DC-SCI be placed on the HPM.
Note 3: If the HPM FRU is deemed incompatible or goes undetected, the DC-SCM must halt the boot sequence, to avoid possible electrical stress conditions. This is called "Plug-N-Detect-Else-Halt".
Note 4: Not included in these states are scenarios such as a system level battery hold up, or orchestration of the system power when a "high AUX" S5 state is required. That would entail a state where the host is OFF, but the system requires more current than PSUs can provide on their AUX power rail. It should be noted that the DC-SCM's maximum supported power level exceeds many PSU's AUX rail capabilities, and the system design would need to handle accordingly.

In addition, if the HPM and SCM type discovery determines specific hardware interface compatibility and complete circuit awareness, then the earliest permitted power state of any given DC-SCI signal may be relaxed.

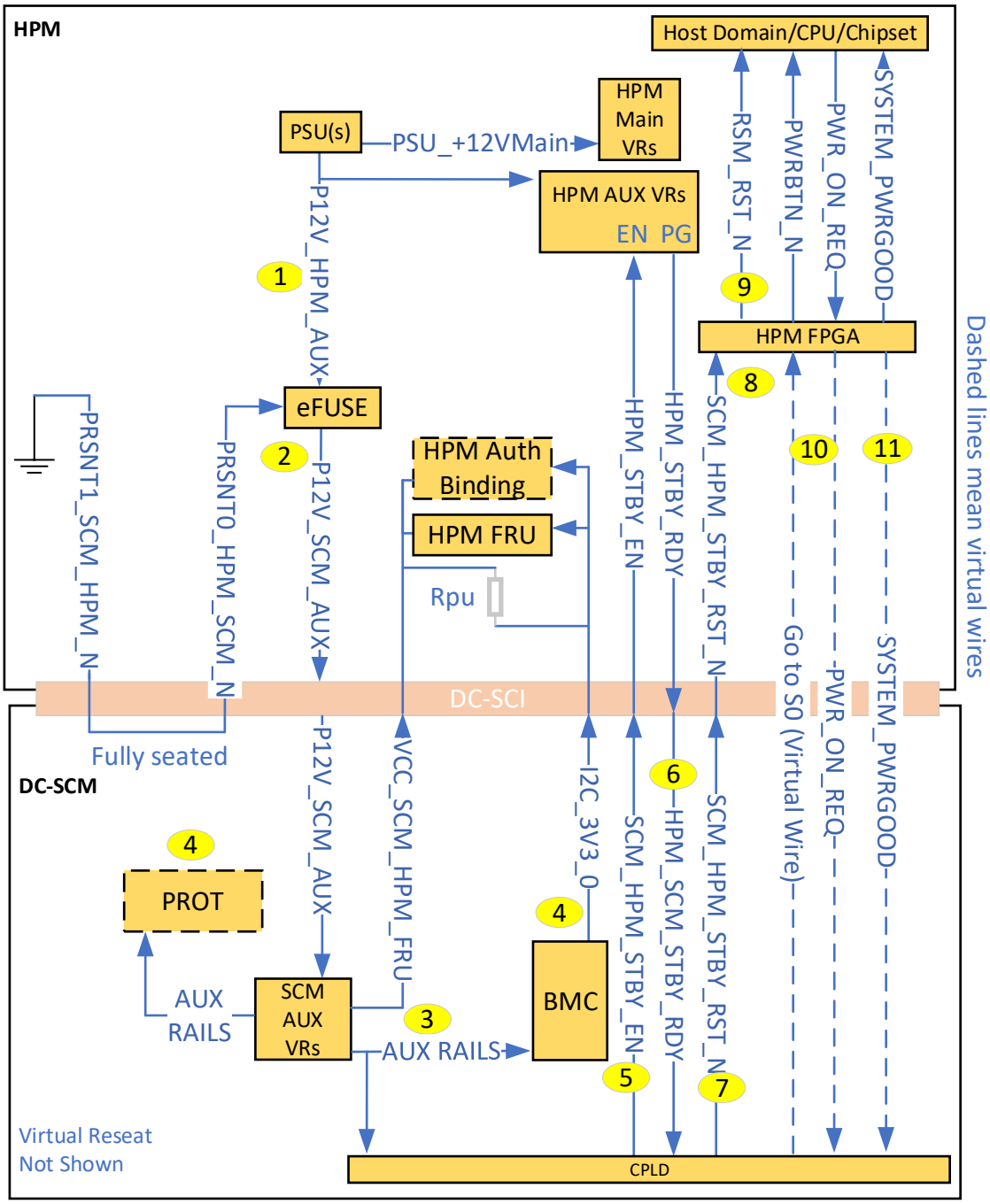



**Figure 64: Discovery Sequence**

# 4 Electrical Specifications

The following sections provide specifications for the DC-SCM input voltage and current.

## 4.1 Input Voltage, Power, and Current

Table 14 lists the nominal, maximum, and minimum values for the DC-SCM input voltage. The maximum and minimum voltages include the effects of connector temperature, age, noise/ripple, and dynamic loading.

**Table 14: Input Power Requirements**

| | Minimum | Nominal | Max |
|---|---|---|---|
| Input voltage | 10.8 V DC | 12.0 V DC | 13.2 V DC |
| Input Power (S5) | n/a | n/a | 47.52 W (10.8 V*1.1 A/pin*4 pins) |
| Inrush Rise Time | 5 ms | n/a | 200 ms |
| *Input Current | n/a | n/a | 4.4 A (1.1 A/pin*4 pins) |
| *Input Power (belowS5) | n/a | n/a | 15 W |

*Input current is based on 1.1 A rating per pin, which is already derated.
*Input Power (STBY): For DC-SCM/HPM compatibility, it is recommended to limit the max power at 15 Watts for all states lower than S5, this includes STBY. This limit is not enforced if the HPM design is known to be capable of supporting the full DC-SCM power limit at these early states.

New to DC-SCI 2 is a power pin for **VCC_SCM_HPM_FRU** sourced from the DC-SCM to the HPM specifically for powering the HPM FRU and optional circuits such as an authentication IC. The current limit is set not due to pin current rating, but instead due to overall budget and reducing burden on the SCM VR while providing enough to aid in the discovery and any potential security functions.

VCC_SCM_HPM_FRU must be +3.3VAUX +- 5% and limited to 200 mA maximum current. Note that this is the limit for overall budget reasons and not by the pin current limit.

**Table 15: VCC_SCM_HPM_FRU Power Requirements**

| | Minimum | Nominal | Max |
|---|---|---|---|
| Input Voltage | 3.135 V DC (-5%) | 3.3 VAUX DC (SCM sourced) | 3.465 V DC (+5%) |
| Input Power | n/a | n/a | 0.627 W (3.135 V*200 mA) |
| Input Current | n/a | n/a | 200 mA |

# 5 Routing Guidelines and Signal Integrity

## 5.1 NC-SI

The following section describes the timing requirements for routing the NC-SI bus. It defines the portion of the overall propagation delay budget allocated from the HPM to the DC-SCM. Please refer to the OCP NIC specification for the segment between the HPM and the OCP NIC. HPM and DC-SCM implementers shall analyze their design to ensure the timing budget is not violated.

The traces shall be implemented as 50 Ohm ±15% impedance-controlled nets. HPM and DC-SCM designers are encouraged to follow the guidelines defined in the RMII and NC-SI specifications for physical routing. Figure 65 outlines the NC-SI clock and the data path timing delays on a typical design with the NC-SI bus routed to the NIC ASIC.

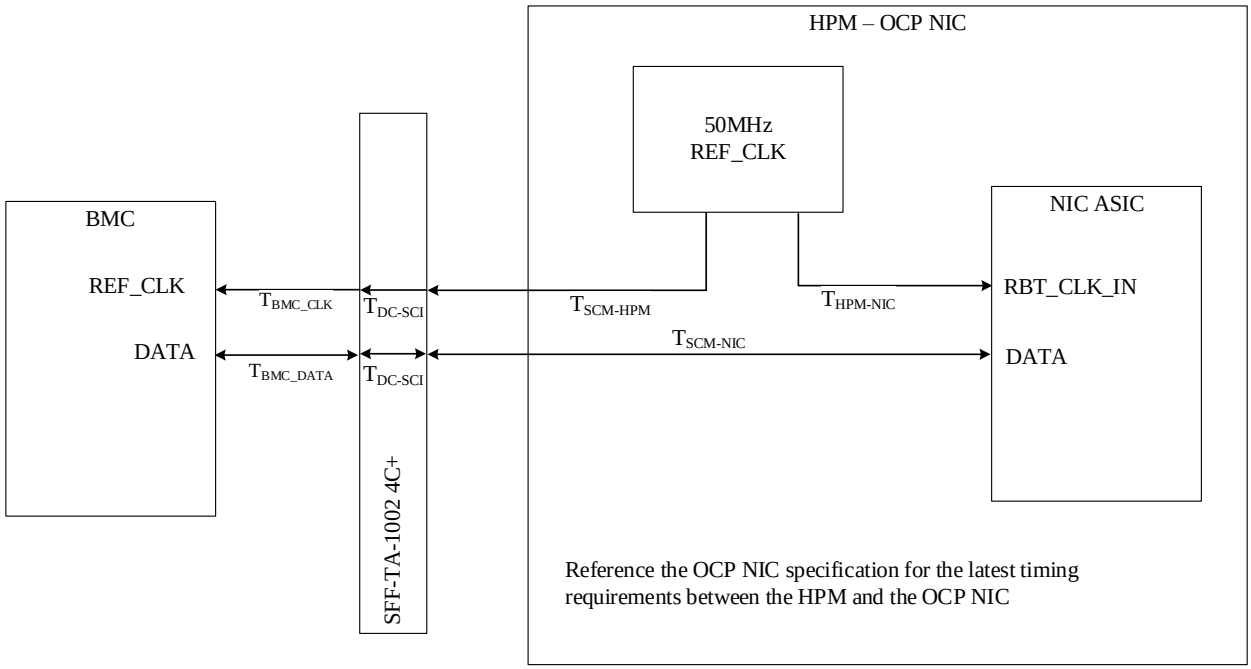



**Figure 65: NC-SI Clock and Data Path Timing Delay Topology**

Table 16 shows the various timing parameters from the BMC to the HPM. Signal details from the HPM to the OCP NIC are described in the OCP NIC 3.0 specification. The propagation delay on the DC-SCM PCB ($T_{BMC}$) is assumed to be 680 ps.

**Table 16: NC-SI Timing Parameters**

| Parameter | Value | Description |
|---|---|---|
| $T_{SKEW[max]}$ | 1.5 ns | Max permissible REF_CLK skew between any two devices in the system |

| | | |
|---|---|---|
| $T_{PD,Budget}$ | 3000 ps | Total propagation delay between BMC and the target ASIC |
| $T_{BMC_DATA}$ | 680 ps | BMC to DC-SCM connectorpropagation delay |
| $T_{DC-SCI}$ | 110 ps | Typical propagation delay over the DC-SCI connector |

### 5.1.1 NC-SI Data Timing

This maximum allowable propagation delay on the data lines from the BMC to each NIC is shared across the DC-SCM ($T_{SCM_DATA}$), DC-SCI connector ($T_{DC-SCI}$), HPM, and the OCP NIC ($T_{HPM-NIC}$) boards as shown Figure 65 . Considering the connector propagation delays, the following requirement shall be met for the total propagation delay:

$$T_{BMC_DATA} + T_{DC-SCI} + T_{SCM-NIC} < T_{PD,Budget}$$

### 5.1.2 NC-SI Clock Timing

The maximum clock skew ($T_{SKEW[max]}$) between the reference clocks, as specified in DSP0222, is noted in the OCP NIC specification Table 16. The critical delays are shown in Figure 65 as $T_{SCM_CLK}$, $T_{DC-SCI}$ , $T_{SCM-HPM,}$ $T_{HPM-NIC}$. The following equation summarizes the skew requirement:

$$|(T_{SCM_CLK} + T_{DC-SCI} + T_{SCM-HPM}) - (T_{HPM-NIC})| \leq T_{SKEW[max]}$$

Note: The end-to-end RBT timing budget may be improved by minimizing $T_{SKEW(actual)}$. The formula above assumes the maximum permissible skew per the DSP0222 specification.

## 5.2 I2C and I3C

For the I2C interfaces, HPM and DC-SCM designers shall follow the System Management Bus (SMBus) Specification, Version 3.0. Refer to this specification for DC characteristics and all AC timings.
For the I3C interfaces, HPM and DC-SCM designers shall not exceed the capabilities of the MIPI I3C Basic v1.1.1 specification. Refer to this specification for DC characteristics and all AC timings. The total capacitance of the I3C bus on the DC-SCM, including the BMC output pin capacitance, DC-SCM trace capacitance and DC-SCI pin capacitance should be less than 25 pF to maximize the possible bus clock rate.

# 6 Platform Interoperability

The DC-SCM specification attempts to support maximum electrical and mechanical interoperability between all DC-SCMs and HPMs, although many options for signal allocation on the DC-SCI are left open to the implementer. As such, full electrical interoperability can be achieved where the DC-SCM and HPM adhere to an additional "design specification" that brings alignment between the DC-SCM and HPM in these open areas. Through adherence to such a design specification, a development model called "Plug-and-Code" can be achieved, making possible multi-vendor HPM/DC-SCM interoperability via changes to BMC firmware, DC-SCM CPLD and HPM FPGA firmware.

In order to ensure that unused buses and signals are properly terminated on the HPM, Table 178 outlines the required and optional interfaces through the DC-SCI and the expected termination on HPM when unused in the system.

**Table 17: Platform Interoperability**

| Interface Name | Required? (Y/N) | HPM Termination If Un-used |
|---|---|---|
| NC-SI | N | No |
| ESPI | N | Yes |
| I2C[0] | Y (HPM FRUID at 0xA0) | 10K |
| I2C_3V3 | N | 10K |
| I2C_I3C_1V8 | N | 10K |
| I3C[0:1] | N | 10K |
| SPI_HPMCNTRL | N | No |
| QSPI; QSPI_P1 | N | No |
| SPI_SCMCNTRL | N | No |
| USBs | N | No |
| PCIe TX/RX | N | No |
| PCIe Clock | N | No |
| PECI_HPM_SCM | N | No |
| PECI_VREF_HPM_SCM | N | Connect to 1.0 V (S0) |
| UART[0:1] | N | No |
| JTAG | N | No |
| P3V0_HPM_SCM_BAT | N | No |
| STBY BOOT SEQUENCE SIGNALS | Y | NA |
| PRSNT[0:1] | Y | NA |
| All other Misc. signals | N | No |

## 6.1 FRU Requirements

The HPM is required to supply an FRU Information Device (typically a discrete EEPROM) placed directly on channel I2C0 and not behind a MUX or hub. The device is required to respond

only to target Address 0xA0 (8-bit address) and must support 2-byte addresses for read or write offsets. FRU Information Device capacity must be an even power of 2 in the range of 256 Bytes (but still support 2-byte offsets) up to 64 KB. Hardware default is to be write protected, but a method such as via the HPM FPGA to override the write protection setting is recommended to cover all conceivable logistical and excursion scenarios. Since only HPM full power cycle resets the FRU Information device, it is the DC-SCM's duty to detect/recover from bus anomalies such as bus busy due to an interrupted transaction, as well as all (re)setting of pointers.

This table defines the requirement for a MultiRecord Area record on the HPM FRU. This record is for the DC-SCM to read to proceed with the appropriate actions, such as the updating the DC-SCM FPGA or BMC firmware.

**Table 18: HPM FRU MultiRecord Definition**

| Offset | Field | Factory Default | Description |
|---|---|---|---|
| 0h | Record Type ID | 0xC1 | |
| 1h | 7:7 – End of list | Implementation Specific | Defined in IPMI FRU spec |
| | 6:4 – Reserved, write as 000b | 000b | |
| | 3:0 – Record Format version | 0000b – DC-SCM2.0<br>0001b – DC-SCM 2.1 | |
| 2h | Record Length | Implementation Specific | Defined in IPMI FRU spec |
| 3h | Record Checksum (zero checksum) | Implementation Specific | Defined in IPMI FRU spec |
| 4h | Header Checksum (zero checksum) | Implementation Specific | Defined in IPMI FRU spec |
| 5h:7h | Manufacture ID | 7fh | OCP INIA assigned ID 0x00A67F, |
| | | A6h | (LSB first) |
| | | 00h | |
| 8h | OCP HPM FRU OEM Record Version | 00h – Reserved | This field indicates the version number of this MultiRecord. This field must be 1h in this version of the specification. |
| | | 01h – OCP DC-SCM 2 card FRU record released with version 1.0 | |
| 9h:Ah | DC-SCI Revision | 02h – For Revision 2.* | DC-SCI Revision to match supported DC-SCI |
| | 15:8 - Major number | | |
| | 7:0 - Minor number | 01h | |
| Bh | DC-SCI Version | 0001b | DC-SCI Version to match supported DC-SCI |
| | 7:4 - Major number | | |
| | 3:0 - Minor number | 0000b | |
| Ch:Dh | LTPI Revision | 01h – Example | Least supported Revision<br>Populate with 00h 00h if not implemented |
| | 15:8 - Major number | | |
| | 7:0 - Minor number | 01h – Example | |
| Eh | LTPI Version | 0001b – Example | Least supported Version<br>Populate with 00h if not implemented |
| | 7:4 - Major number | | |
| | 3:0 - Minor number | 0000b – Example | |

| | | | |
|---|---|---|---|
| Fh | DC-SCM Type | 00h - not any defined type<br>01h - FFh | HPM Common Circuit design Spec Type N (See separate Design Spec) |
| 10h:11h | HPM Vendor ID | Vendor Specific | Use PCI VendorID for the company producing this HPM. Examples:<br>AMD: 1002h<br>Dell: 1028h<br>Foxconn (Hon Hai): 105Bh<br>HPE:1590h<br>IBM:1014h<br>Intel: 8086h<br>Inventec:1170h<br>Jabil: 10D3h<br>Lenovo: 17AAh<br>NVidia: 10DEh<br>Quanta: 152Dh<br>Wistron: 6080h |
| 12h:13h | HPM Device ID | Implementation Specific | It is the HPM Vendor's responsibility to assign a DeviceID that uniquely identifies an HPM product, starting with 0000h and increasing sequentially. For example, the 4th variant of HPM by a specific HPM vendor is: 0003h.<br>This field is not to identify a specific version of an HPM hardware (such as 2nd production revision) or a specific vendor part number. |
| Implementation Specific | OEM | Implementation Specific | Optional |

# 7 Regulatory

## 7.1 Required Compliance

An OCP DC-SCM 2 card shall meet the following Environmental, EMC and safety requirements.

### 7.1.1 Required Environmental Compliance

- **China RoHS Directive**
- **EU RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. The substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates
- **EU REACH Regulation (EC) No 1907/2006** addresses the production and use of chemical substances and their potential impact on human health and the environment.
- **EU Waste Electrical and Electronic Equipment ("WEEE")** Directive (2012/19/EU) – mandates the treatment, recovery and recycling of EEE
- **The Persistent Organic Pollutants Regulation (EC) No. 850/2004** bans production, placing on the market and use of certain persistent organic pollutants
- **The California Safe Drinking Water and Toxic Enforcement Act of 1986 ("Proposition 65")** sets forth a list of regulated chemicals that require warnings in the State of California
- **The Packaging and Packaging Waste Directive 94/62/EC** limits certain hazardous substances in the packaging materials
- **Batteries Directive 2006/66/EC** regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances

### 7.1.2 Required EMC Compliance

Radiated and Conducted Emissions requirements are based on deployed geographical locations. Refer to Table 19: for details.

**Table 19: FCC Class A Radiated & Conducted Emissions Reqs Based on Geo Location**

| Targeted Geography | Applicable Specifications |
|---|---|
| USA | FCC, 47 CFR Part 15, Class A digital device (USA) |
| Canada | ICES-003, class A (CAN) |
| EU | EN 55032: 2015+AC:2016 Class A Radiated and Conducted Emissions requirements for European Union<br>EN 55035: 2017 Immunity requirements for the European Union (EU)<br>EN 55024: 2010+A1:2015 Immunity requirements for European Union (EU) may alternatively be reported.<br>Note: EN55024 is scheduled to be superseded by EN55035. OCP DC-SCM 2 implementors are encouraged to test to EN55035 to avoid recertifying their product when EN55024 is withdrawn |

| | |
|---|---|
| Australia/New Zealand | AS/NZS CISPR 32:2015 Class A<br>CISPR 32:2015 for Radiated and Conducted Emissions requirements |
| Japan | VCCI 32-1 Class A Radiated and Conducted Emissions requirements |
| Korea | KN32 – Radiated and Conducted Emissions<br>KN35- Immunity |
| Taiwan | BSMI CNS13438: 2006 (complete) Class A Radiated and Conducted Emissions requirements |

- **CE** – Equipment must pass the CE specification
- All technical requirements covered under **EMC Directive (2014/30/EU)**

### 7.1.3 Required Product Safety Compliance

- Safety – requirements are listed in Table 20.

**Table 20: Safety Requirements**

| Targeted Category | Applicable Specifications |
|---|---|
| Safety | UL 62368-1 and CAN/CSA C22.2 No. 62368-1-14, 3rd Edition. Audio/video, information, and communication technology equipment Part 1: Safety requirements, dated 2019/12/13 |

### 7.1.4 Required Immunity (ESD) Compliance

The OCP DC-SCM 2 card shall meet or exceed the following ESD immunity requirements listed in Table 21:

**Table 21: Immunity (ESD) Requirements**

| Targeted Category | Applicable Specifications |
|---|---|
| Immunity (ESD) | EN 55035 2017, and IEC 61000-4-2 2008 for ESD.<br>EN 55024 may alternatively be reported. Required ±4 kV contact discharge and ±8 kV air discharge<br>Note: EN55024 is scheduled to be superseded by EN55035. OCP DC-SCM 2 implementors are encouraged to test to EN55035 to avoid recertifying their product when EN55024 is withdrawn |
| NEBS Level 3 (optional) | Optionally test devices to NEBS Level 3 –<br>Required ±8 kV contact discharge and ±15 kV air discharge with interruptions not greater than 2 seconds. The device shall self-recover without operator intervention<br>Note: NEBS compliance is part of the system level testing. The OCP DC-SCM 2 specification is providing a baseline minimum recommendation for ESD immunity |

Note: emissions and immunity tests iare to be completed at the system level. The OCP DC-SCM 2 vendors should work with the system vendors to achieve the applicable requirements listed in this section.

## 7.2 Recommended Compliance

### 7.2.1 Recommended Environmental Compliance

- **Halogen Free**: IEC 61249-2-21 Definition of halogen free: 900 ppm for Bromine or ChIorine, or 1500 ppm combined total halogens
- **Arsenic**: 1000 ppm (or 0.1% by weight)
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act** requires companies using tin, tantalum, tungsten, and gold ("3TG") in their products to verify and disclose the mineral source. While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntarily reporting of this information

### 7.2.2 Recommended EMC Compliance

- FCC, 47 CFR Part 15, Subpart B Class A digital device (USA) with 10 dB margin. Refer to the baseline requirements shown in Section 7.1.2 for details.

# 8 Acronyms

For the purposes of the DC-SCM specification, the following acronyms apply:

| Acronym | Definition |
|---|---|
| ASIC | Application Specific Integrated Circuit |
| BMC | Baseboard Management Controller |
| CBB | Compliance Base Board |
| CFM | Cubic Feet per Minute |
| DC-SCM | Data Center Secure Control Module |
| DC-SCI | Data Center Secure Control Interface |
| DRAM | Dynamic Random Access Memory |
| EDSFF | Enterprise and Datacenter SSD Form Factor |
| EMI | Electro Magnetic Interference |
| ESPI | Enhanced Serial Peripheral Interface |
| FRU | Field Replaceable Unit |
| I/O | Input / Output |
| HFF | Horizontal Form Factor |
| HPM | Host Processor Module |
| I2C | Inter-Integrated Circuit - two wire serial protocol |
| I3C | MIPI Alliance Improved Inter-Integrated Circuit – two wire serial protocol |
| LED | Light Emitting Diode |
| LFF | Large Form Factor |
| LFM | Linear Feet per Minute |
| LPC | Low Pin Count bus |
| LTPI | LVDS Tunneling Protocol and Interface |
| LVDS | Low Voltage Differential Signaling |
| MAC | Media Access Control |
| NC | No Connect |
| NC-SI | Network Controller Sideband Interface |
| NIC | Network Interface Card |
| OCP | Open Compute Project |
| SCM | Secure and Control Module |
| SRIS | Separate Reference Clocks with Independent Spread-Spectrum Clocking |
| SRNS | Separate Reference Clocks with No Spread-Spectrum Clocking |
| VFF | Vertical Form Factor |