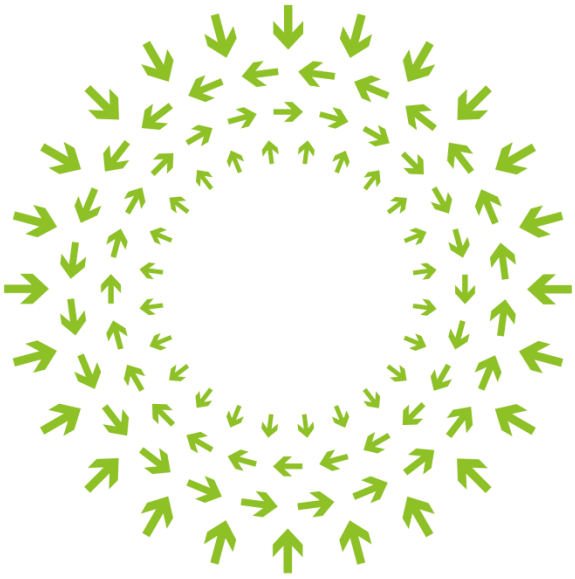

OPEN
Compute Project

Datacenter Secure Control Module Specification (DC-SCM)

Revision 2.0, Version 1.0

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Revision History

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1.0	0.8	Nov 9, 2020	Initial public review.
	0.95	Dec 2, 2020	Feedback Implemented
	1.0	March 11, 2021	Removed ESPI_CS1_N and replaced with RSVD3, Table 22:SPARE[0:1] desc, Fig 22: Updated to initiator/Responder, Table 27: I3C pull-up updated to STBY/MAIN, Sec 6: Platform interop wording edit, Sec 2.2.3- Typo(FFF> HFF), Figs 3, 4, 5, 6 updated, Table 3 updated
2.0		Dec 31, 2020	DC-SCM 2.0 Initial public review using DC-SCM 0.8 as base.
		July, 2021	DC-SCM2.0 updates using DC-SCM1.0 as base
		Sept, 2021	Updates from working group decisions
	0.5	Oct, 2021	Implement 0.95 pinout descriptions
	0.51	Oct, 2021	LTPI Details
	0.52	Nov 9, 2021	General updates and fixes in the document. Mechanical: HFF dimensions diagram updated with connector shift and notches updated. LTPI: Link Initialization, Training and Configuration details added. Incorporated feedback from v0.51 review.
	0.53	Nov 20, 2021	Updates based on feedback. Added a note that VFF will be defined in later version of the spec.
	0.7	Nov 23, 2021	0.7 release
	0.9	Apr 4, 2022	Extracted LTPI Chapter to standalone specification. Cleanup. Revised to I3C Basic 1.1.1 Added detailed mechanical drawings
	0.95	Apr 25, 2022	Incorporated 0.9 feedback
	0.96	May 6, 2022	Feedback from 0.95, minor clean up
	0.97	June 3, 2022	Minor clean up Clarification around I2C, I3C, FSI Add PRoT in discovery sequency Add S5 and lower power state recommendation Add EFF Rail dimensions
	1.0	July 27, 2022	1.0 release

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With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback of over 150 individuals from 28 different companies.

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- DC-SCM 2.0 LVDS Tunneling Protocol and Interface (LTPI) Specification 1.0

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1.1 Overview

This specification provides details for the design features needed to create a Datacenter-ready Secure Control Module (DC-SCM) with a standardized Datacenter-ready Secure Control Interface (DC-SCI). It moves common server management, security, and control features from a typical processor motherboard architecture onto a smaller common form factor module. This module contains all the FW states previously housed on a typical processor motherboard. This provides benefits to both the user and developer.

This document does not prescribe design details that is not essential to the electrical compatibility of the connector interface. Examples are used throughout this document for explaining potential use case, not as requirements of the module or the coupled Host Processor Module design.

From a Data Center perspective, this enables common management and security to be deployed across a higher percentage of platforms. It also enables deployment of management and security upgrades on platforms within a generation without redesign of more complex components.

From a development perspective, this enables a solution provider to remove customer specific solutions from the more complex components (such as motherboards). This enables greater leverage of higher complexity components across platforms.

For the purposes of this specification, to clarify terminology, we introduce the following module definitions:

- HPM – Host Processor Module. This refers to any processing module to be managed by an SCM. In simplest terms, this is the traditional CPU-memory complex but with the BMC and Security moved to the SCM. The HPM is not limited to standard processor architecture and can apply to any architecture utilizing management and security features.
- HPM FPGA – Host Processor Module FPGA. This refers to a programmable device on the HPM. Main functions include system power/reset control as well as serializing/de-serializing several IOs between the HPM and BMC.
- DC-SCM – The Datacenter - Secure Control Module. The DC-SCM is designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
- DC-SCI – The Datacenter - Secure Control Interface refers to the connector interface between the DC-SCM and the HPM.

A typical DC-SCM design enables the design and deployment of a Host Processing Module (HPM) complex to become a simpler exercise with increased efficiency for time to market deployment. With a standardized DC-SCI pinout and definition, the DC-SCM can be used as a vehicle to drive common boot, monitoring, control, and remote debug for diverse platforms.

The goal of this revision is to allow for future scalability and longevity across a few generations of server platforms. It considers that server platforms will drop support for some of legacy requirements in favor

of new use cases such as Multi Node support and new manageability solutions based on high-speed interfaces. This requires the DC-SCM spec to allow more flexibility in interface usage and pinout definition. Thus, we introduce the LTPI (LVDS Tunneling Protocol & Interface).

1.2 DC-SCM Architecture

For the purposes of this specification, the DC-SCM architecture is assumed to consist of the following primary elements:

- BMC – The Baseboard Management Controller is a specialized service processor that monitors the physical state of server.
- BMC Flash – One or more flash devices used to contain the BMC firmware image.
- BIOS Flash – One or more flash devices used to contain the BIOS firmware image for each node.
- DC-SCM CPLD – A programmable logic device that contains application specific logic and optional LTPI interface.
- RoT Security Processor – An optional security processor responsible for attesting the BMC, BIOS and/or other firmware images on the system.
- TPM – Trusted Platform Module – An optional dedicated chip or module designed to secure hardware through integrated cryptographic keys.

An example block diagram demonstrating an example architectural building blocks of a DC-SCM is shown in Figure 1. Note that some of these interfaces are mutually exclusive with others.

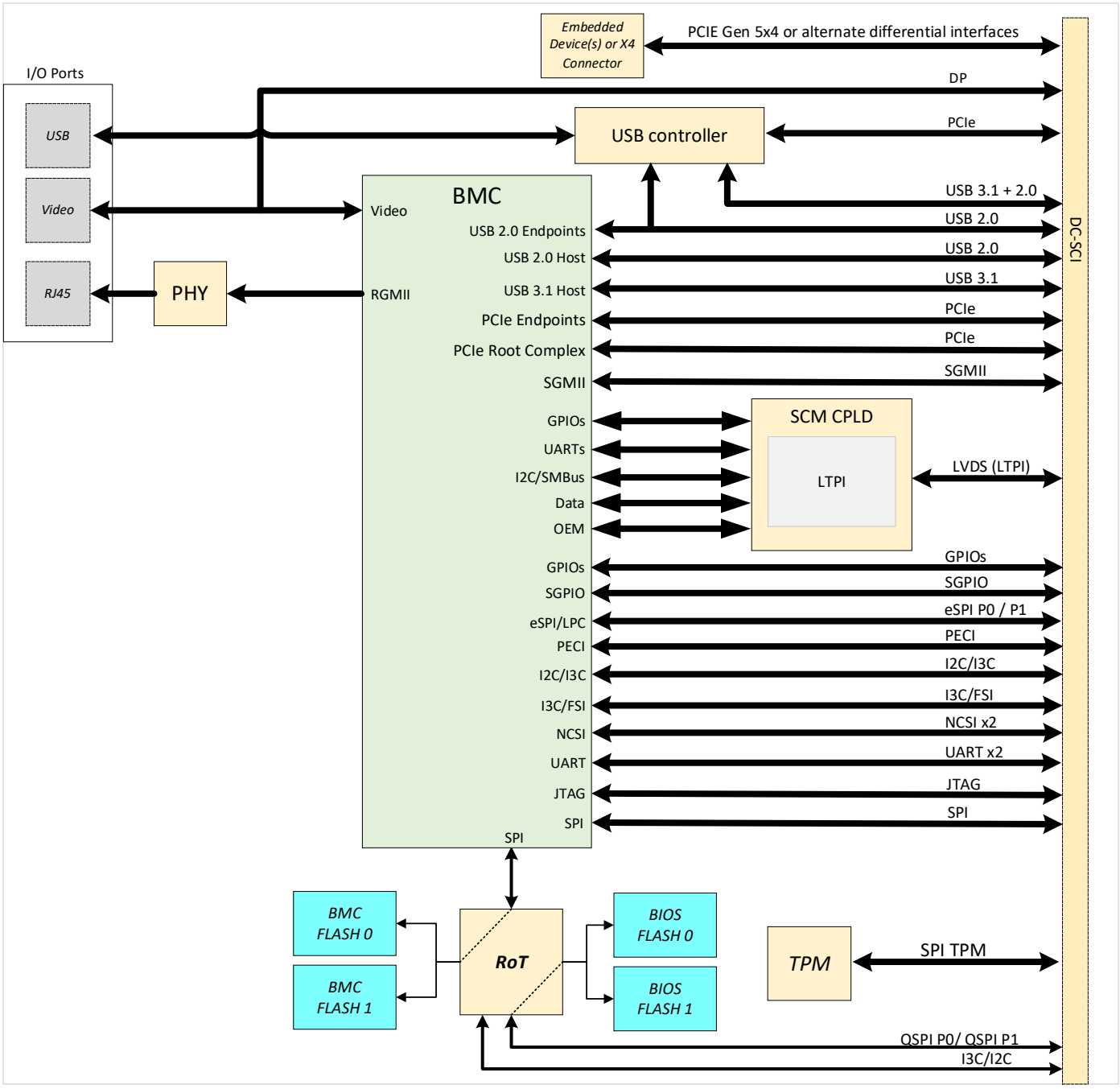


Figure 1: DC-SCM Example Block Diagram

1.3 Multi-Node Support

The long-term goal is to enable the ability to support more than two independent nodes using a single DC-SCM module. The 2.0 revision of the specification will focus on the single-node and dual-node pin

definitions. In this version of the dual-node pin definition, the signals are arranged to expand as the number of nodes supported by the system. This is achieved by consolidating various low speed interfaces over the LTPI connection and make pins available for additional interfaces, such as PCIe, ESPI and SPI, which are dedicated to each socket. Note that the following diagram is general connectivity options and not indicative of existing capabilities (such as BMCs with dual eSPI).

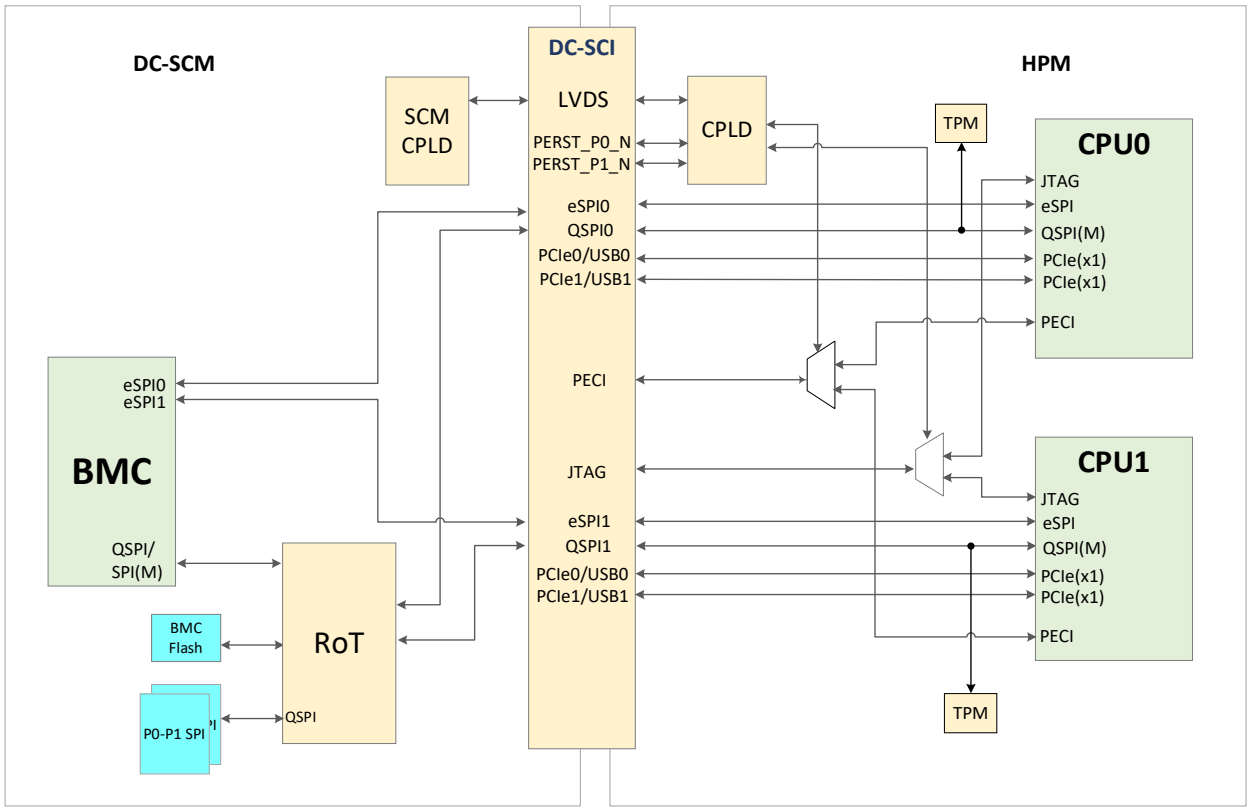


Figure 2: Multi-Node Block Diagram

2 Mechanical Form Factor

2.1 General Overview

The DC-SCM 2.0 form factor is similar to the OCP NIC 3.0 form factor with alterations to the connector interface and to the physical size to accommodate typical DC-SCM circuit requirements and ensure mechanical incompatibility between DC-SCM and OCP NIC. The connector is defined to be an SFF-TA-1002 compliant 4C+ connector. The 4C+ connector is a 4C compliant connector with an additional 28-pin “OCP bay” defined in the OCP NIC 3.0 specification.

The DC-SCM is physically longer and wider ensuring that the DC-SCM 2.0 cannot mate into an OCP NIC v3 slot. It also has a 3.25 mm shift in the card edge key slot geometry to ensure an OCP NIC v3 module

nor a DC-SCM 1.0 module can mate into a DC-SCM 2.0 slot and connect electrically. To achieve the features outlined in this specification, OCP DC-SCM 2.0 compliant cards are not backwards compatible with OCP DC-SCM 1.0 cards.

This specification considers three form factors for DC-SCM:

- External Form Factor (EFF) – This form factor is intended for use in servers where the DC-SCM is installed in a coplanar fashion, at the front of the server with direct interface to the front server bezel, or at the rear wall of the server. When installed at the front, standard front panel interfaces are contained on the DC-SCM and may or may not require cables. See Section 2.3 for more information.
- Internal Form Factor (IFF) – This form factor is intended for use in servers in which the DC-SCM is embedded internally to the server without direct interface to a server front or rear. In this application, external interfaces such as fan control and front panel require cabled interconnects. The overall dimensions of the form factor are identical to the external form factor, although there are some modifications for usage of internal features. See Section 2.3 for more information.
- Vertical Form Factor (VFF) – This form factor is intended for use in 2U or taller servers in which the DC-SCM is installed vertically at the chassis front/rear wall (similar to a PCIe AIC card). Standard front panel interfaces are contained on the DC-SCM and do not require cables. More details may be available in a later version of this specification.

The DC-SCI is intended to support all form factors of DC-SCM; however, many of the block diagrams and descriptions contained in this specification are based on the EFF and may not demonstrate the cabling requirements of the IFF.

All mechanical board assemblies shall meet the safety requirements described in Section 7.

2.2 Board Dimensions and Keep-out Zones

The PCB form factor overall dimensions are shown in Figure 3. It has a thickness of 1.57 mm. There are slots on the sides to enable the IFF version with interfacing rail features to secure the module in place.

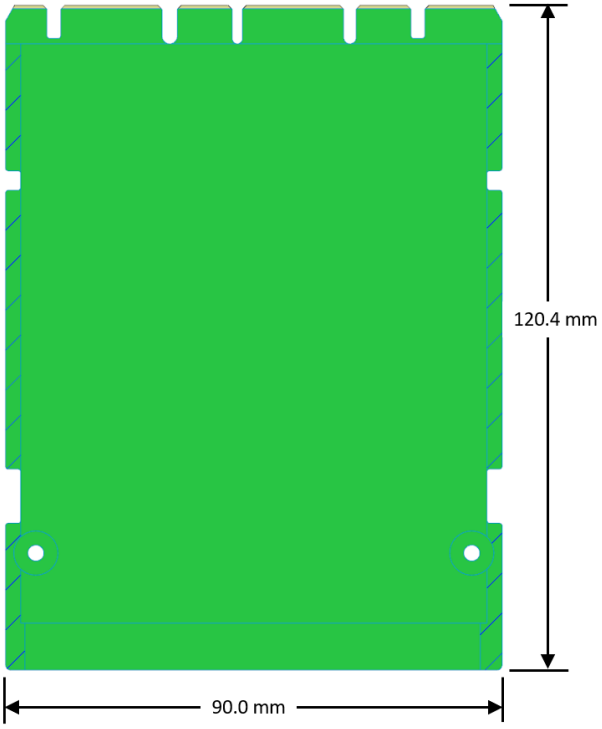


Figure 3: Form Factor Board Overall Dimensions

The top-side board dimensions, along with corresponding detail views and Keep-out Zones (KOZs), are shown below in Figure 4. The bottom side dimensions, detail views, and KOZs are illustrated in Figure 5. The side dimensions and KOZs are depicted in Figure 6.

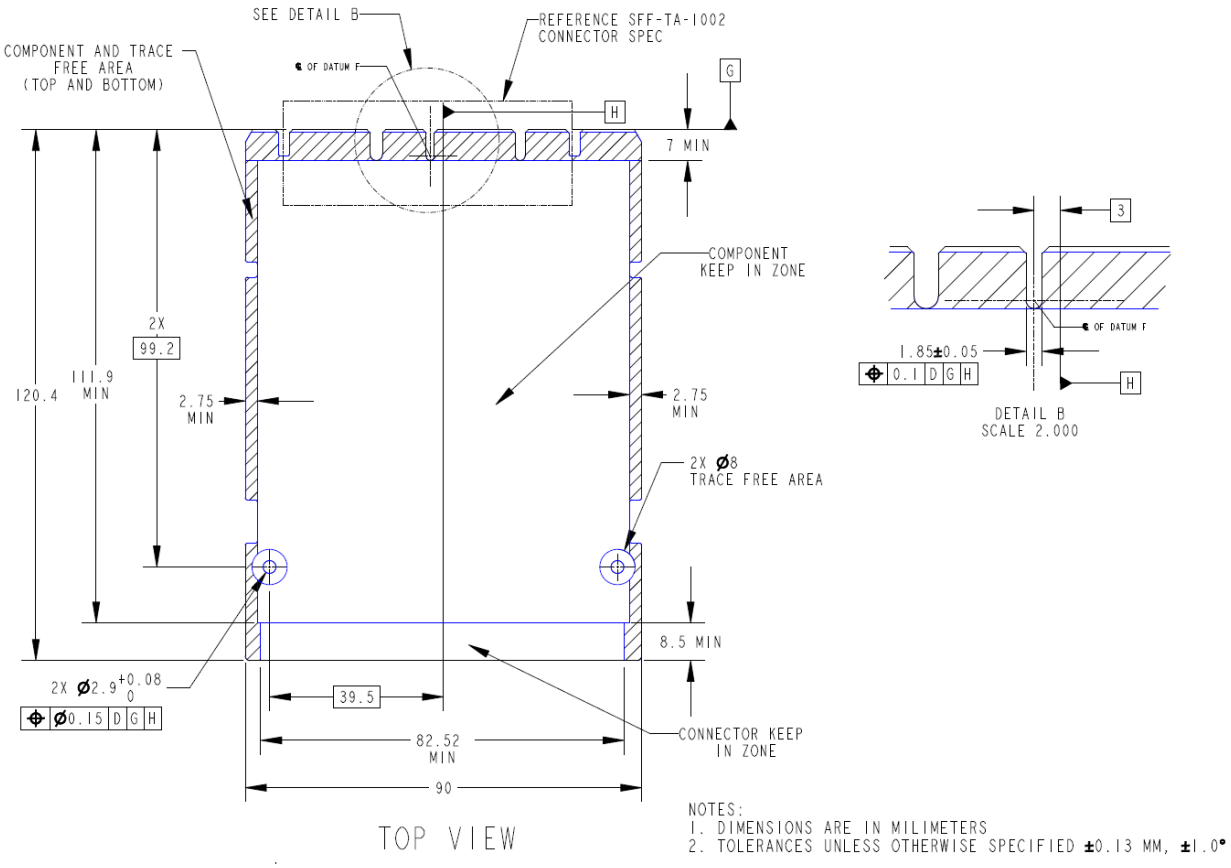


Figure 4: Board Dimensions and Keep-out Zones – Top View

The OCP DC-SCM 2.0 board outline provides features to lock the board into the chassis that are the same as the OCP NIC 3.0 board. This is accomplished with two small notches – one on each board side edge to provide flexible configurations to baseboard vendors. A baseboard may choose to use one or both notches for the internal locking mechanism. If a locking feature is implemented on the baseboard, the OCP DC-SCM 2.0 board may only be inserted or removed after actuating the internal locking mechanism. The PCB retention notches are compatible with all chassis implementations. Please refer to the board dimensions in Figure 5, Detail D for details.

There are also two additional side notches, wider than the aforementioned internal lock notches, that provide a means to retain the module when the DC-SCM and baseboard are assembled together on a tray prior to assembly into the chassis. These notches are illustrated in Figure 5, Detail C. The guide rails will have hook/slot features that interface in these areas. If these features are utilized, they may also serve as a locking mechanism to prevent module removal externally.

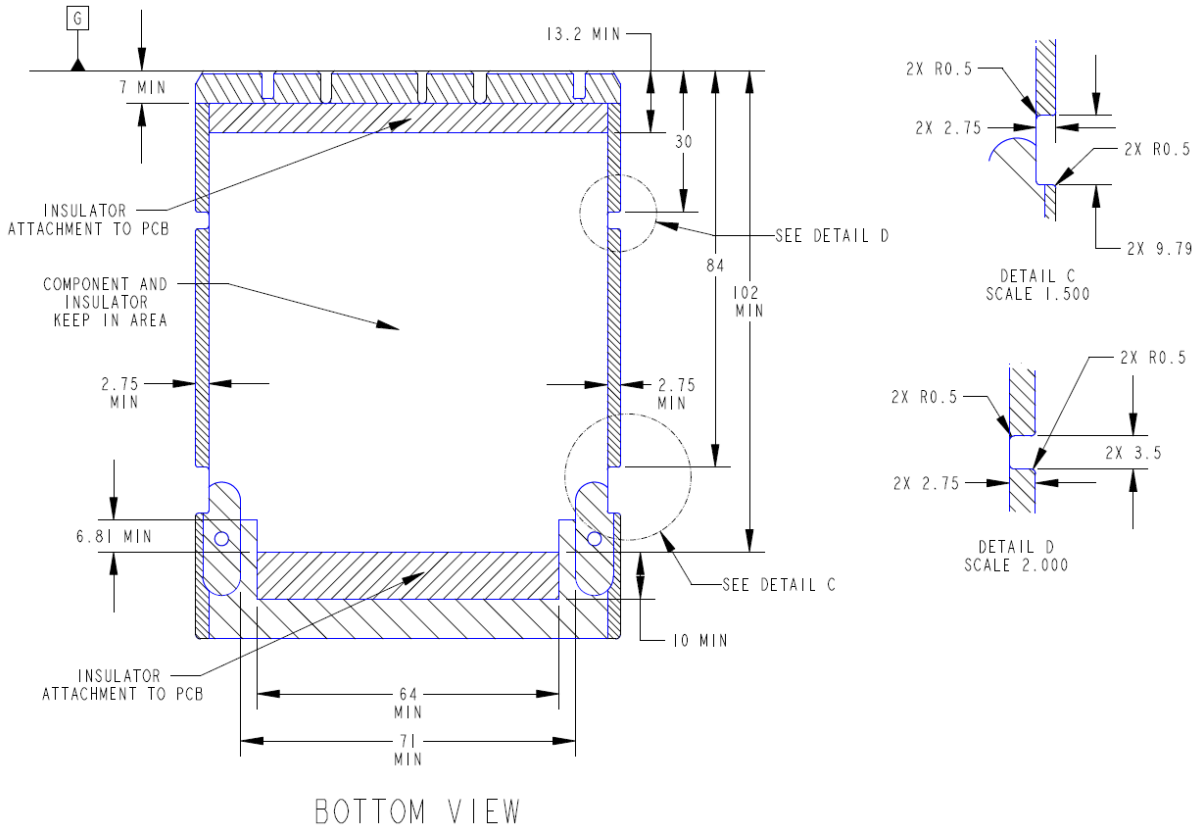


Figure 5: Board Dimensions and Keep-out Zones – Bottom View

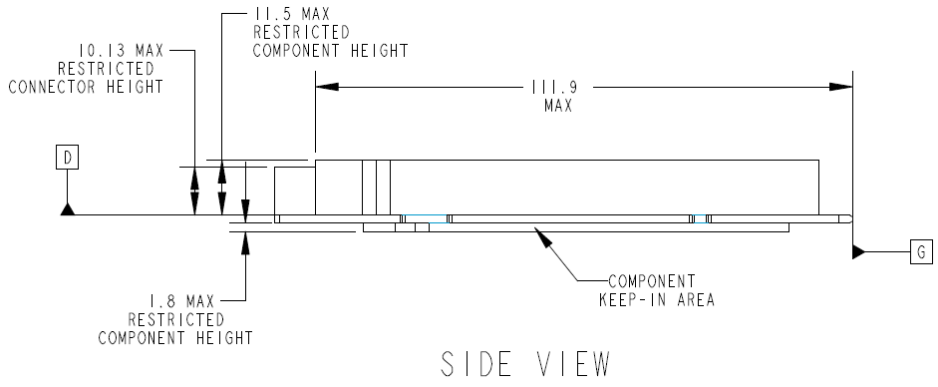


Figure 6: Board Dimensions and Keep-out Zones – Side View

For the IFF version of the board, there is an option to include a vertical rear handle to aid in insertion and extraction of the module. Figure 7 shows the dimensions and modified KOZs for the board top and bottom sides. To see the optional handle in an installed state on an IFF module, please see Figure 15.

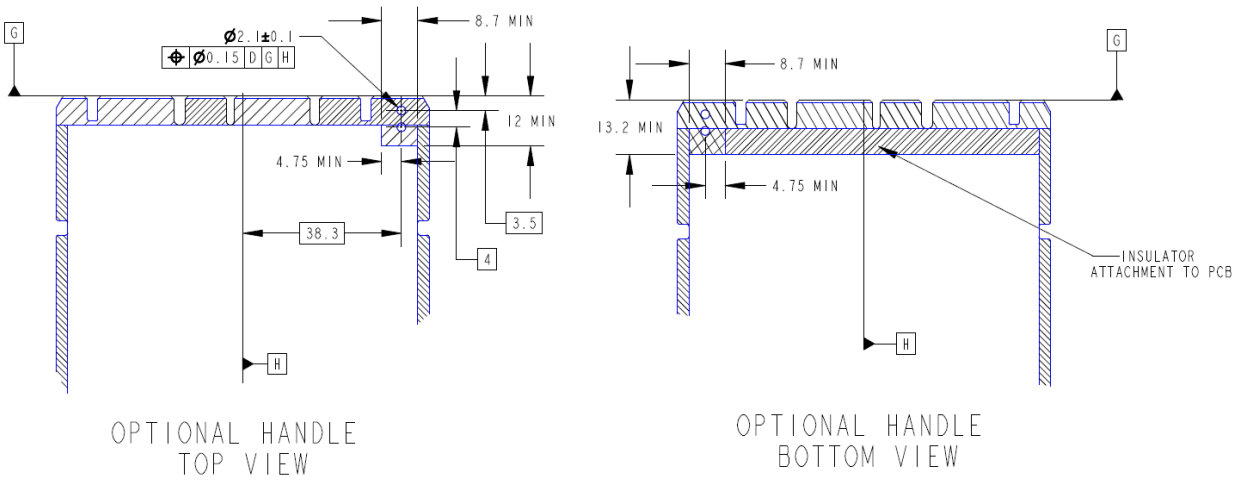


Figure 7: IFF Dimensions and KOZs for Optional Handle - Top/Bottom Views

2.3 External Form Factor

The External Form Factor (EFF) is defined for usage at the front or rear of a chassis and is externally inserted or extracted. Much like the OCP NIC 3.0 module, it has a pull tab and a securing captive fastener on either side of the faceplate bracket for aiding in the chassis assembly.

There are two options for an EMI compliance solution. Option one utilizes metal finger stock that attached to all sides of the faceplate and interface to the chassis bay opening flanges for contact. Option two takes advantage of Fabric-over-Foam (FoF) components attached to all four sides to make continuous contact with the chassis bay opening flange walls.

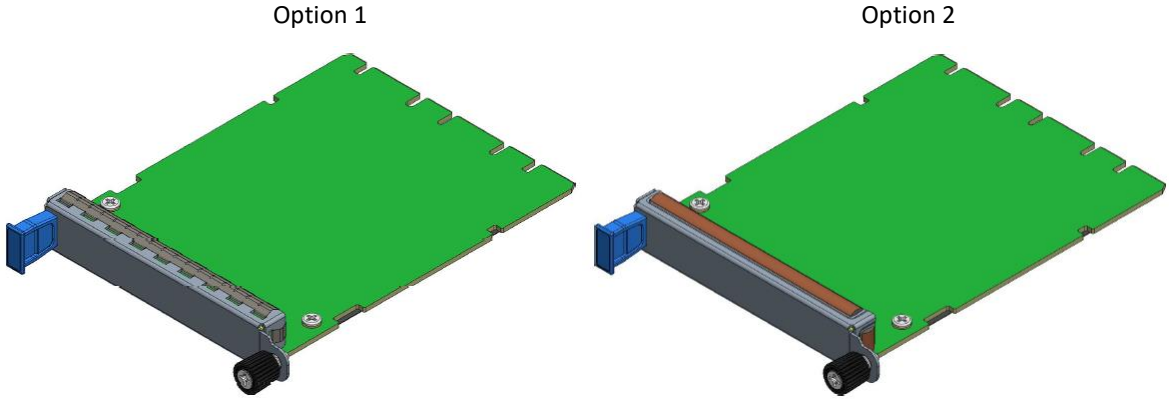


Figure 8: EFF Module Options - ISO Views

Exploded views of each corresponding module assembly are shown in Figure 9.

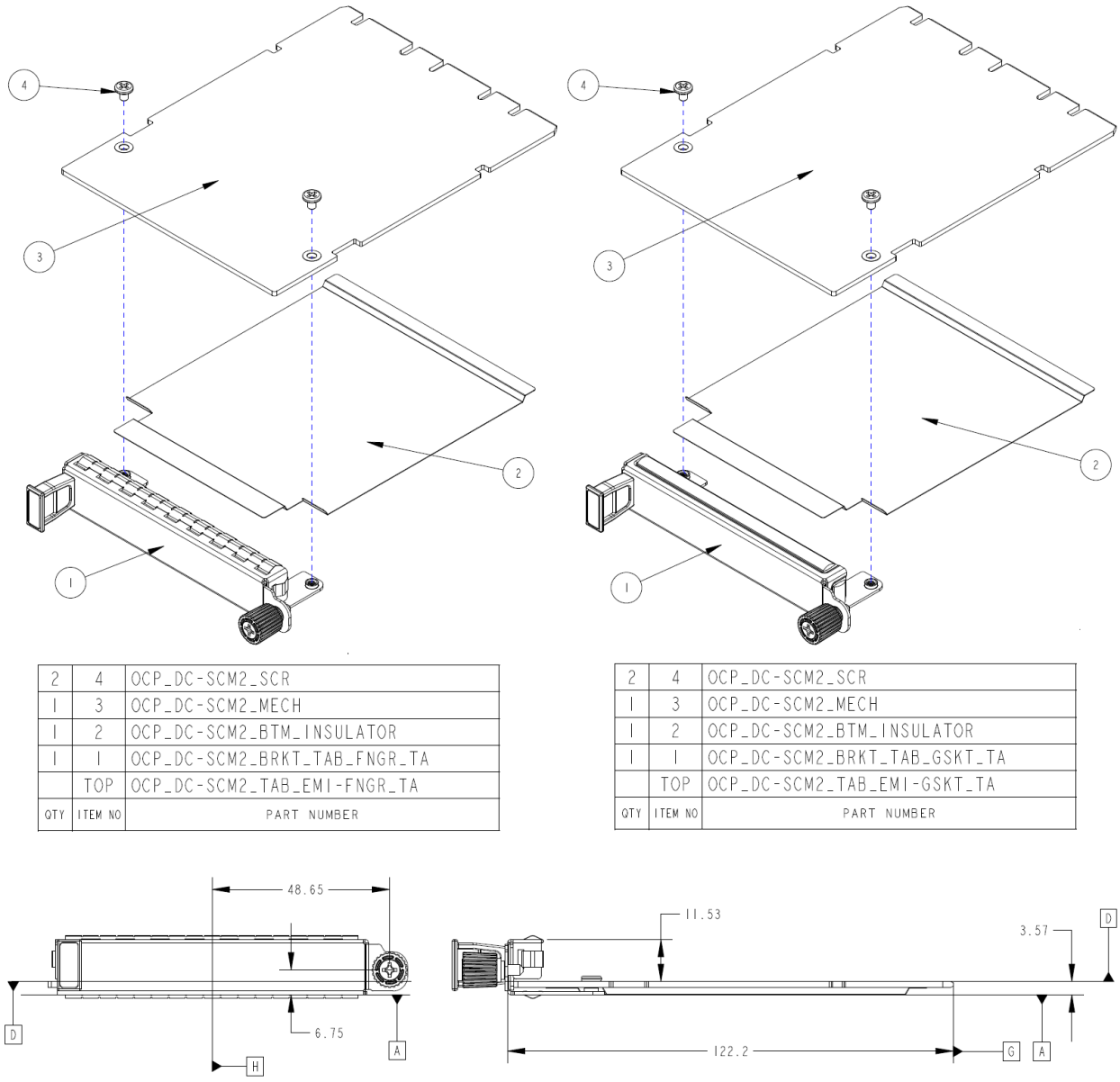


Figure 9: EFF Module Assemblies – Exploded ISO and Orthographic Views

2.3.1.1 EFF Faceplate Bracket Subassembly

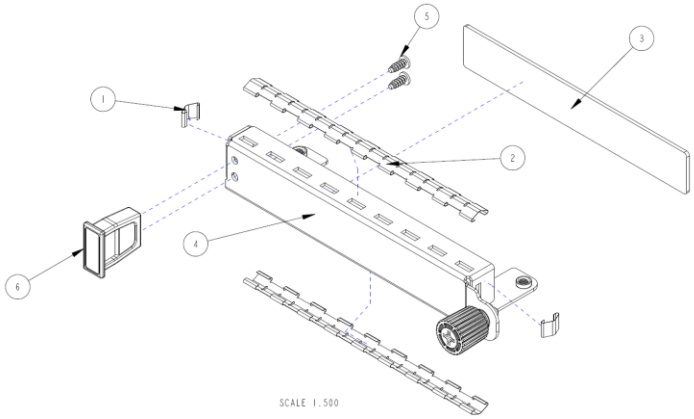
The EFF module supports a front I/O bracket, or faceplate, that enables front I/O access and a securing method of the DC-SCM to the chassis. Each option has the same overall features and dimensions, except for where the EMI solution is attached. Exploded views of the different bracket assemblies are shown below in Figure 10 and Figure 11. The general faceplate dimensions are shown in Figure 5.

Faceplate connector cut-outs and perforations are excluded from the figures and may be customized per system configuration and system airflow requirements. Where space is permitted on the faceplate, vents sized to a maximum of 3.0 mm x 3.0 mm, or round vents with a maximum diameter of 3 mm, may

be added to help optimize airflow while maintaining the integrity of the faceplate structure. The OCP DC-SCM 2.0 card supplier may add port identification markings on the faceplate assembly that meet their manufacturing and customer requirements.

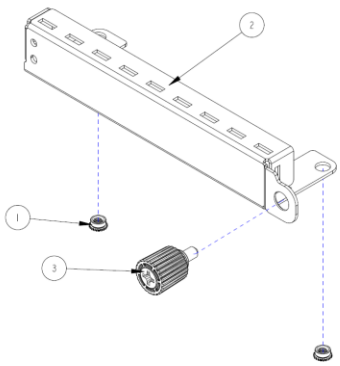
Depending on the OCP DC-SCM 2.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep-in regions as defined by the PCB mechanical drawings and faceplate drawings of Section 2.2 and Section 2.3.1.1.1.

Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers.



QTY	ITEM NO	PART NUMBER	DESCRIPTION
1	6	SOUTHCO_CN-99-459	
2	5	OCP_DC-SCM2_EJTR-HNDL_SCR	
1	4	OCP_DC-SCM2_BRKT_TAB_FNGR_ASSY	
1	3	OCP_DC-SCM2_BRKT_GSKT_CONN	
2	2	OCP_DC-SCM2_BRKT_EMI_FNGR_9F	
2	1	OCP_DC-SCM2_BRKT_EMI_FNGR_1F	
	TOP	OCP_DC-SCM2_BRKT_TAB_FNGR_TA	

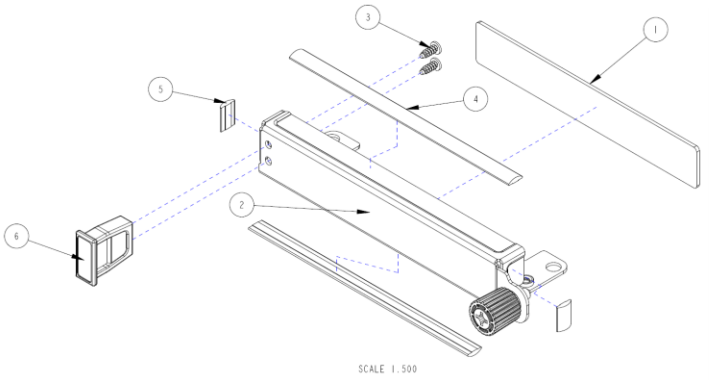
PARTS LIST



QTY	ITEM NO	PART NUMBER	DESCRIPTION
1	3	SOUTHCO_4C-99-343-KEEE	
1	2	OCP_DC-SCM2_BRKT_TAB_EMI-FNGR	
2	1	OCP_DC-SCM2_BRKT_STDOFF	
	TOP	OCP_DC-SCM2_BRKT_TAB_FNGR_ASSY	

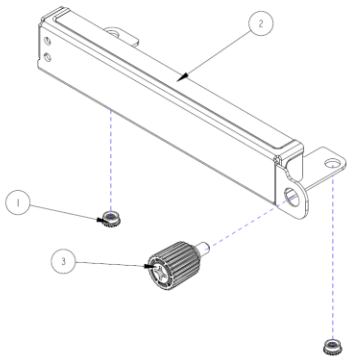
PARTS LIST

Figure 10: EFF EMI Finger Stock Faceplate Bracket Subassemblies – Exploded ISO Views



QTY	ITEM NO	PART NUMBER	DESCRIPTION
1	6	SOUTHCO_CN-99-459	
2	5	OCP_DC-SCM2_EMI_FOF_GSKT_7P35	
2	4	OCP_DC-SCM2_EMI_FOF_GSKT_78P2	
2	3	OCP_DC-SCM2_EJTR-HNDL_SCR	
1	2	OCP_DC-SCM2_BRKT_TAB_GSKT_ASSY	
1	1	OCP_DC-SCM2_BRKT_GSKT_CONN	
	TOP	OCP_DC-SCM2_BRKT_TAB_GSKT_TA	

PARTS LIST



QTY	ITEM NO	PART NUMBER	DESCRIPTION
1	3	SOUTHCO_4C-99-343-KEEE	
1	2	OCP_DC-SCM2_BRKT_TAB_EMI-GSKT	
2	1	OCP_DC-SCM2_BRKT_STDOFF	
	TOP	OCP_DC-SCM2_BRKT_TAB_GSKT_ASSY	

PARTS LIST

Figure 11: EFF EMI FoF Gasket Faceplate Bracket Subassemblies – Exploded ISO Views

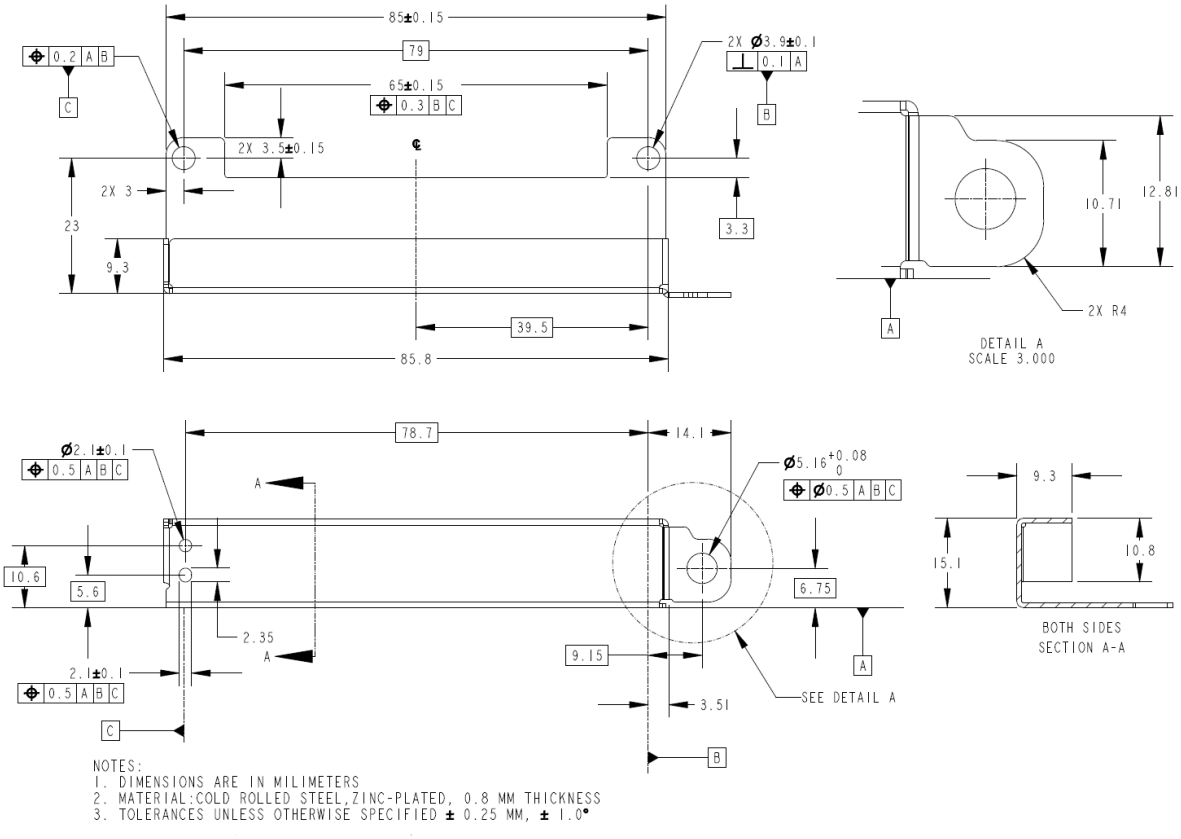


Figure 12: EFF Generic Faceplate Dimensions

2.3.1.2 EFF EMI Finger Stock Faceplate Bracket

Figure 13 illustrates the specific dimensions for the bracket that are required to use the EMI finger stock components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

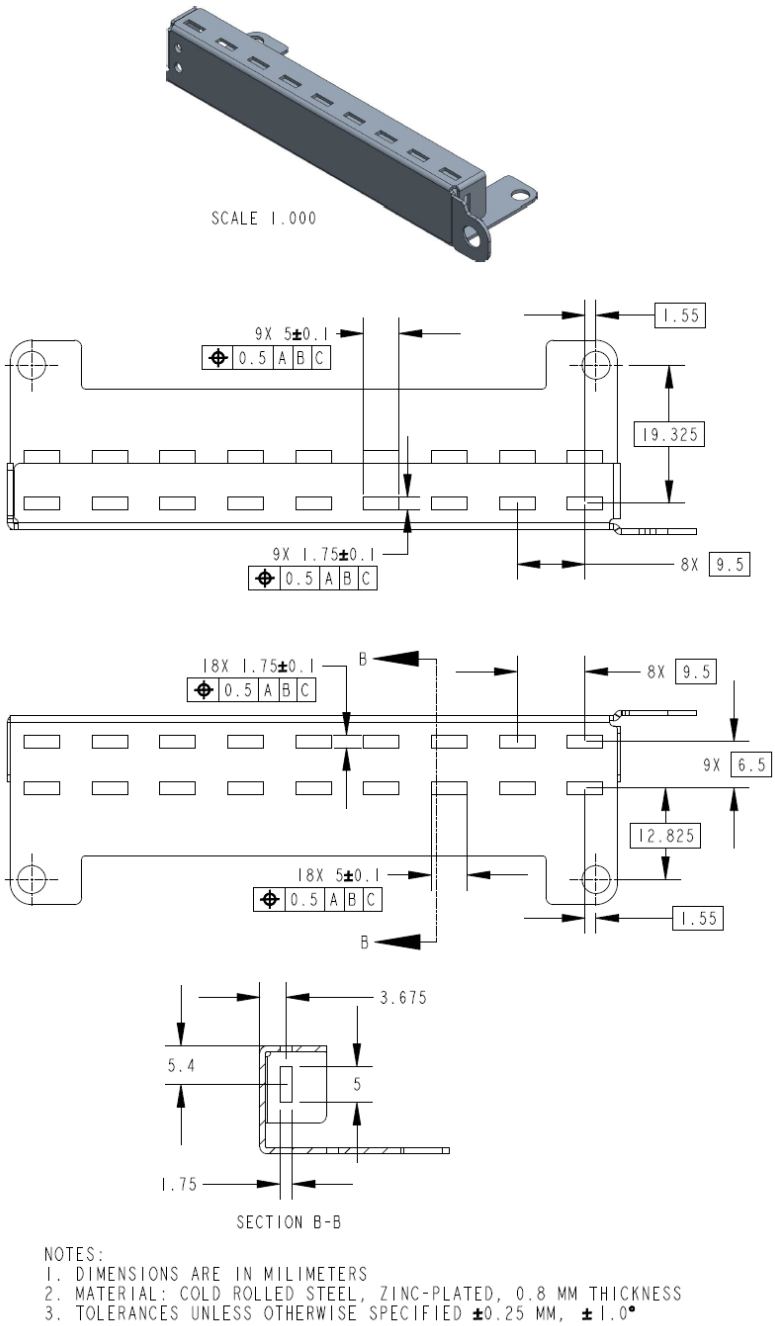


Figure 13: EFF EMI Finger Stock Faceplate Dimensions

2.3.1.3 EFF EMI FoF Gasket Faceplate Bracket

Figure 13 illustrates the specific dimensions for the bracket that are required to use the EMI FoF gasket components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

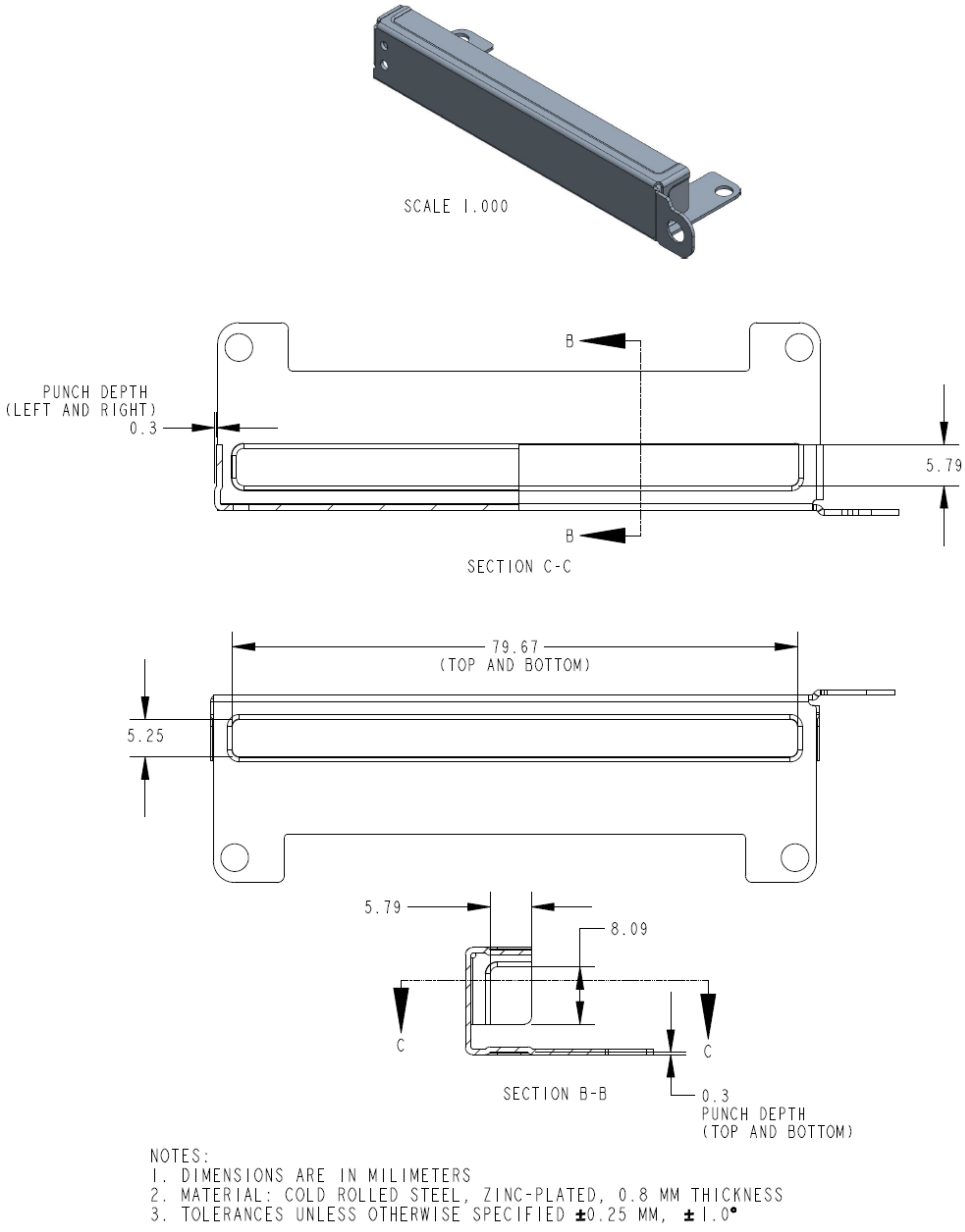


Figure 14: EFF EMI FoF Gasket Faceplate Dimensions

2.4 Internal Form Factor

The Internal Form Factor (IFF) is defined for usage as an internally embedded module to the server without direct interface to a server front or rear. It has no defined external securing features for attachment to the chassis. Internal security features provided by the rails prevent insertion or extraction from outside the chassis.

The IFF implementation uses the same PCB board outline as the EFF. It does have the option for a vertical handle to aid in the insertion and extraction of the card edge into the connector for an internal locking solution as can be seen in Figure 15.

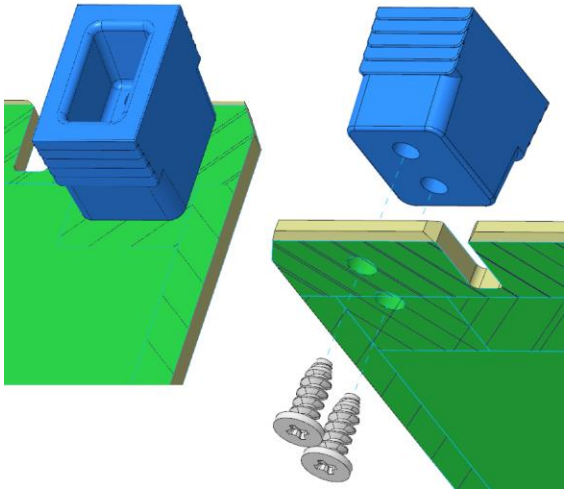


Figure 15: IFF Optional Handle - ISO Assembled and Exploded Views

There are two options for an EMI compliance solution shown below in Figure 16. Option one utilizes metal finger stock that attached to all sides of the faceplate and interface to the chassis bay opening flanges for contact. Option two takes advantage of Fabric-over-Foam (FoF) components attached to all four sides to make continuous contact with the chassis bay opening flange walls.

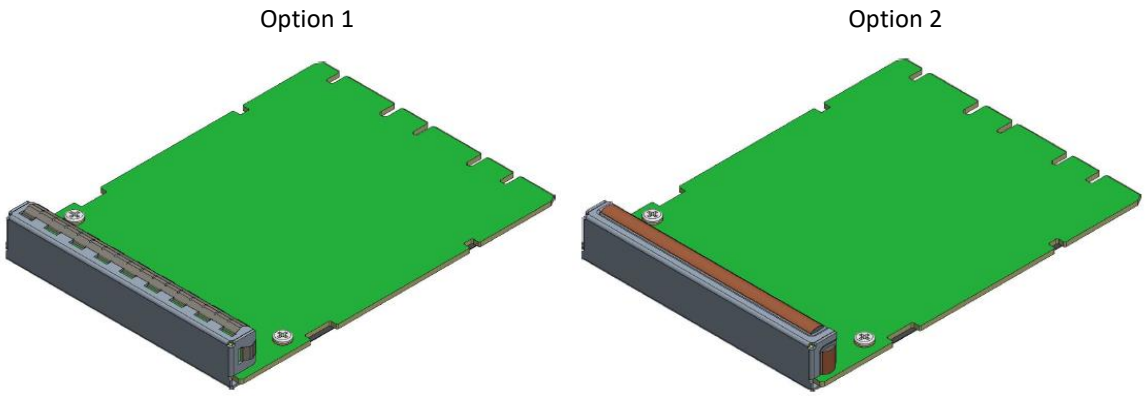
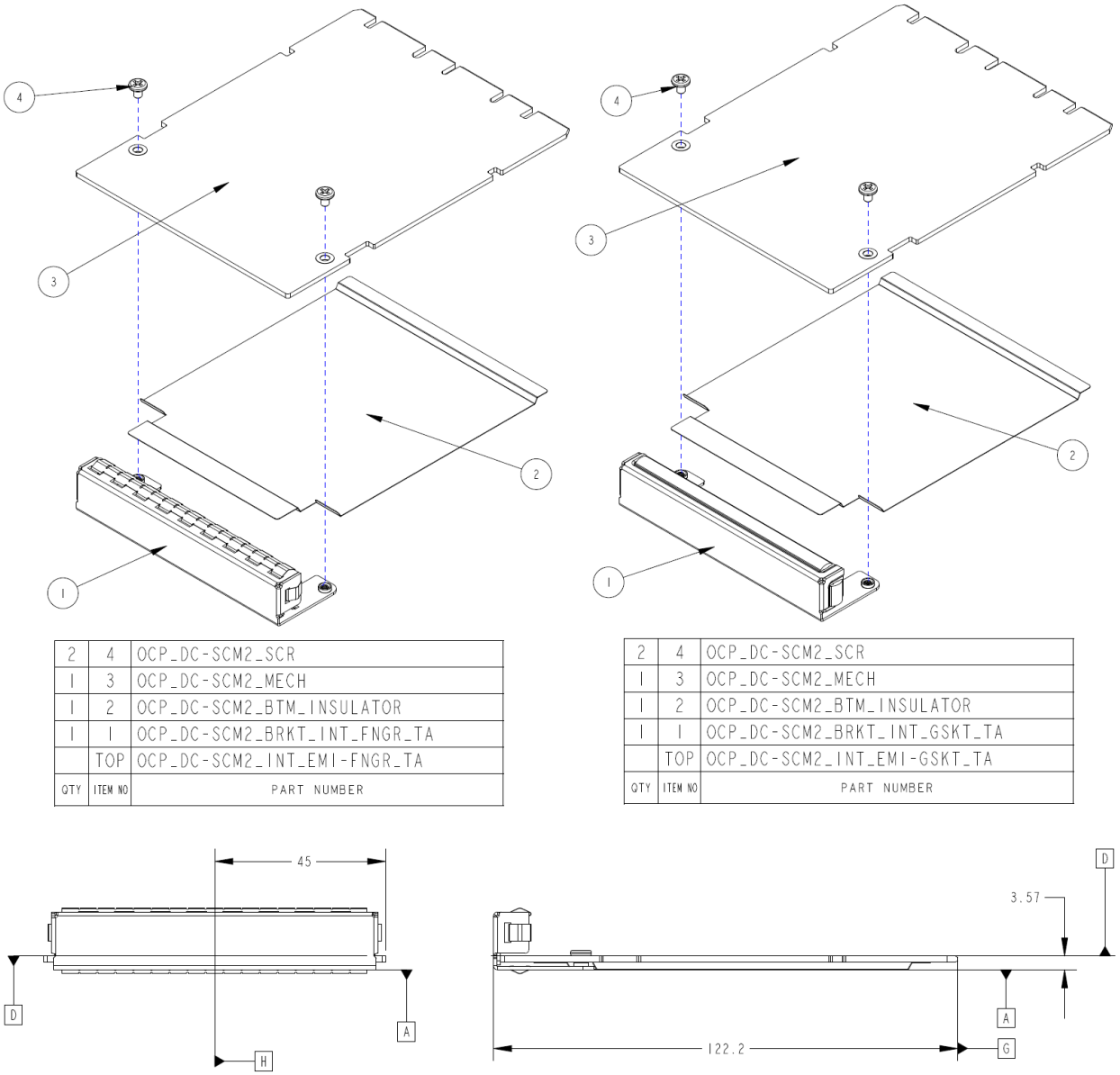


Figure 16: IFF Module Options - ISO Views

Exploded views of each corresponding module assembly are shown in Figure 17.



QTY	ITEM NO	PART NUMBER
2	4	OCP_DC-SCM2_SCR
1	3	OCP_DC-SCM2_MECH
1	2	OCP_DC-SCM2_BTM_INSULATOR
1	1	OCP_DC-SCM2_BRKT_INT_FNGR_TA
	TOP	OCP_DC-SCM2_INT_EMI-FNGR_TA

QTY	ITEM NO	PART NUMBER
2	4	OCP_DC-SCM2_SCR
1	3	OCP_DC-SCM2_MECH
1	2	OCP_DC-SCM2_BTM_INSULATOR
1	1	OCP_DC-SCM2_BRKT_INT_GSKT_TA
	TOP	OCP_DC-SCM2_INT_EMI-GSKT_TA

Figure 17: IFF Module Assemblies – Exploded ISO and Orthographic Views

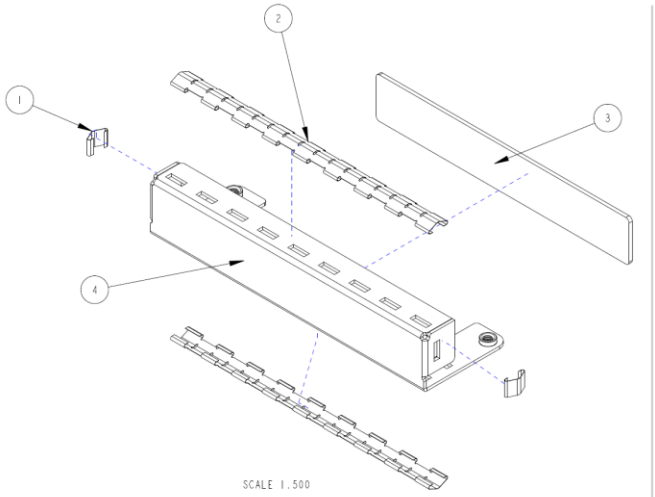
2.4.1 IFF Faceplate Bracket Subassembly

The IFF module supports a front faceplate that enables front I/O access. It does not include features for external retention to the chassis, and it is expected that these features are present internal to the system. Each faceplate option has the same overall features and dimensions, except for where the EMI solution is attached. Exploded views of the different bracket assemblies are shown below in Figure 18 and Figure 19. The general internal faceplate dimensions are shown in Figure 20.

Faceplate connector cut-outs and perforations are excluded from the figures and may be customized per system configuration and system airflow requirements. Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 mm x 3.0 mm, or round vents with a maximum diameter of 3 mm, may be added to help optimize airflow while maintaining the integrity of the faceplate structure. The OCP DC-SCM 2.0 card supplier may add port identification markings on the faceplate assembly that meet their manufacturing and customer requirements.

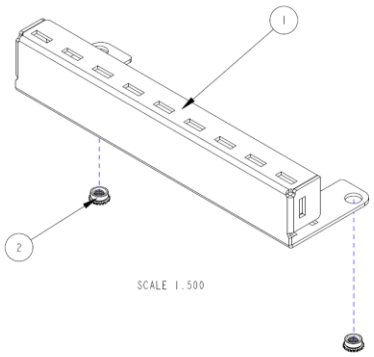
Depending on the OCP DC-SCM 2.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep-in regions as defined by the PCB mechanical drawings and faceplate drawings of Section 2.2 and Section 2.4.1.

Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers.



QTY	ITEM NO	PART NUMBER	DESCRIPTION
1	4	OCP_DC-SCM2_BRKT_INT_FNGR_ASSY	
1	3	OCP_DC-SCM2_BRKT_GSKT_CONN	
2	2	OCP_DC-SCM2_BRKT_EMI_FNGR_9F	
2	1	OCP_DC-SCM2_BRKT_EMI_FNGR_IF	
	TOP	OCP_DC-SCM2_BRKT_INT_FNGR_TA	

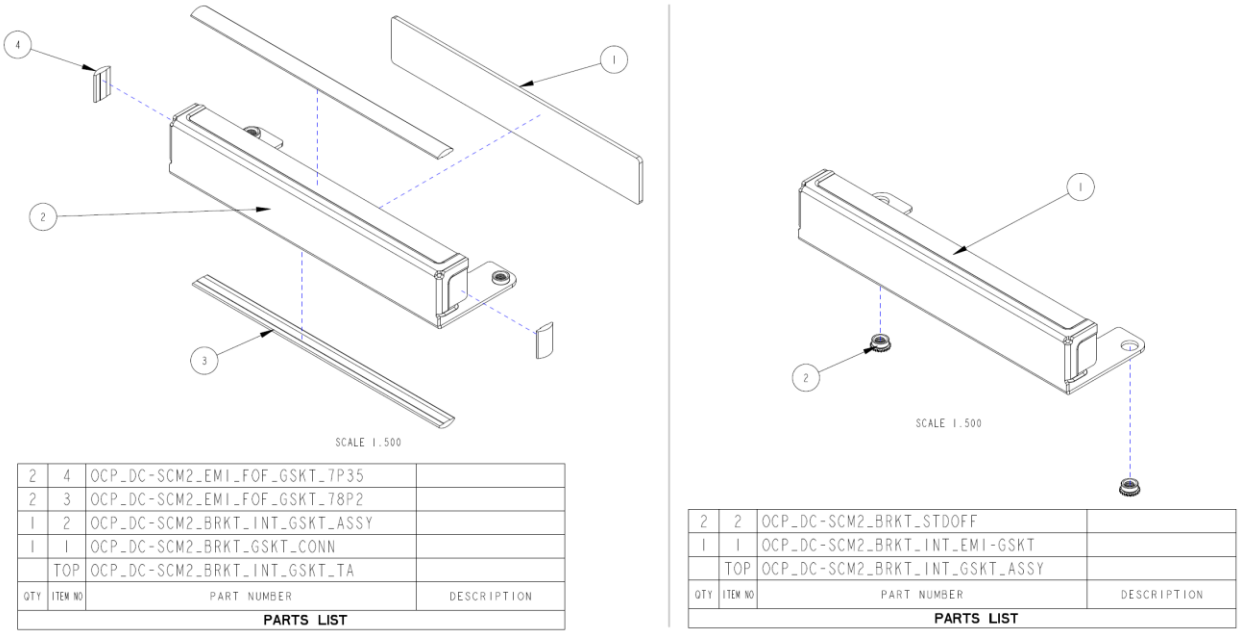
PARTS LIST



QTY	ITEM NO	PART NUMBER	DESCRIPTION
2	2	OCP_DC-SCM2_BRKT_STDOFF	
1	1	OCP_DC-SCM2_BRKT_INT_EMI-FNGR	
	TOP	OCP_DC-SCM2_BRKT_INT_FNGR_ASSY	

PARTS LIST

Figure 18: IFF EMI Finger Stock Faceplate Bracket Subassemblies – Exploded ISO Views



QTY	ITEM NO	PART NUMBER	DESCRIPTION
2	4	OCP_DC-SCM2_EMI_FOF_GSKT_7P35	
2	3	OCP_DC-SCM2_EMI_FOF_GSKT_78P2	
1	2	OCP_DC-SCM2_BRKT_INT_GSKT_ASSY	
1	1	OCP_DC-SCM2_BRKT_GSKT_CONN	
	TOP	OCP_DC-SCM2_BRKT_INT_GSKT_TA	

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
2	2	OCP_DC-SCM2_BRKT_STDOFF	
1	1	OCP_DC-SCM2_BRKT_INT_EMI-GSKT	
	TOP	OCP_DC-SCM2_BRKT_INT_GSKT_ASSY	

PARTS LIST

Figure 19: IFF EMI FoF Gasket Faceplate Bracket Subassemblies – Exploded ISO Views

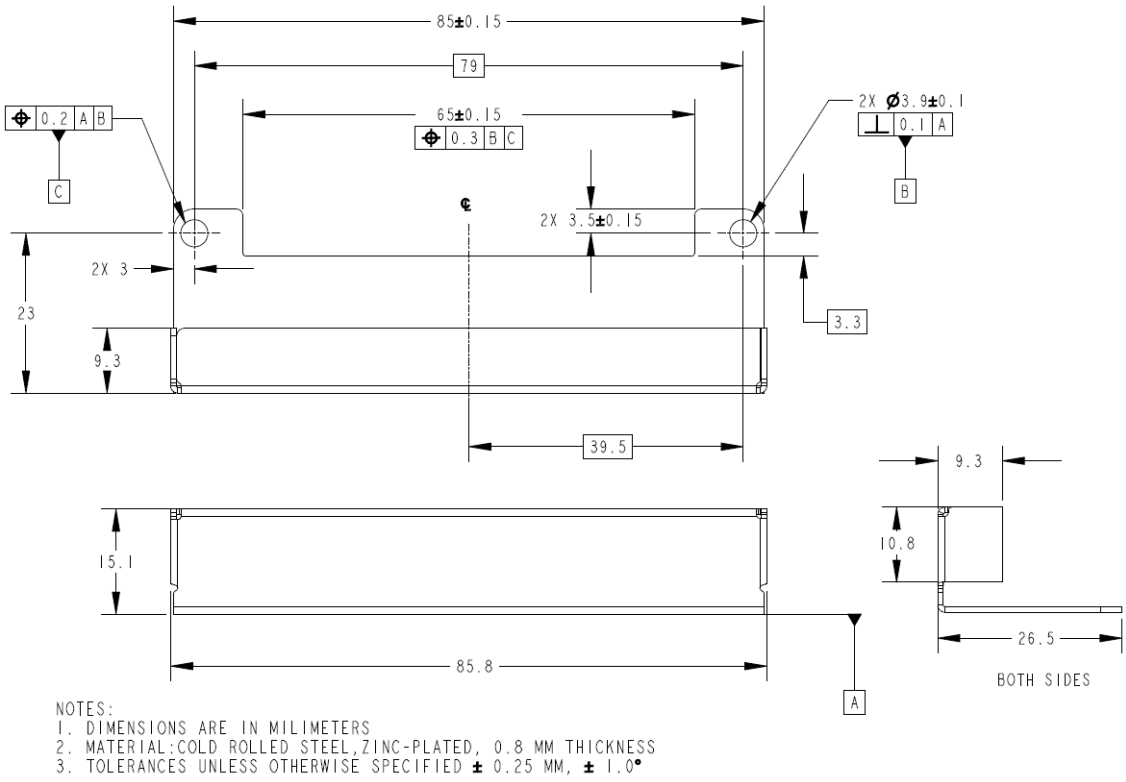


Figure 20: IFF Generic Faceplate Dimensions

2.4.1.1 IFF EMI Finger Stock Faceplate Bracket

Figure 21 illustrates the specific dimensions for the bracket that are required to use the EMI finger stock components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

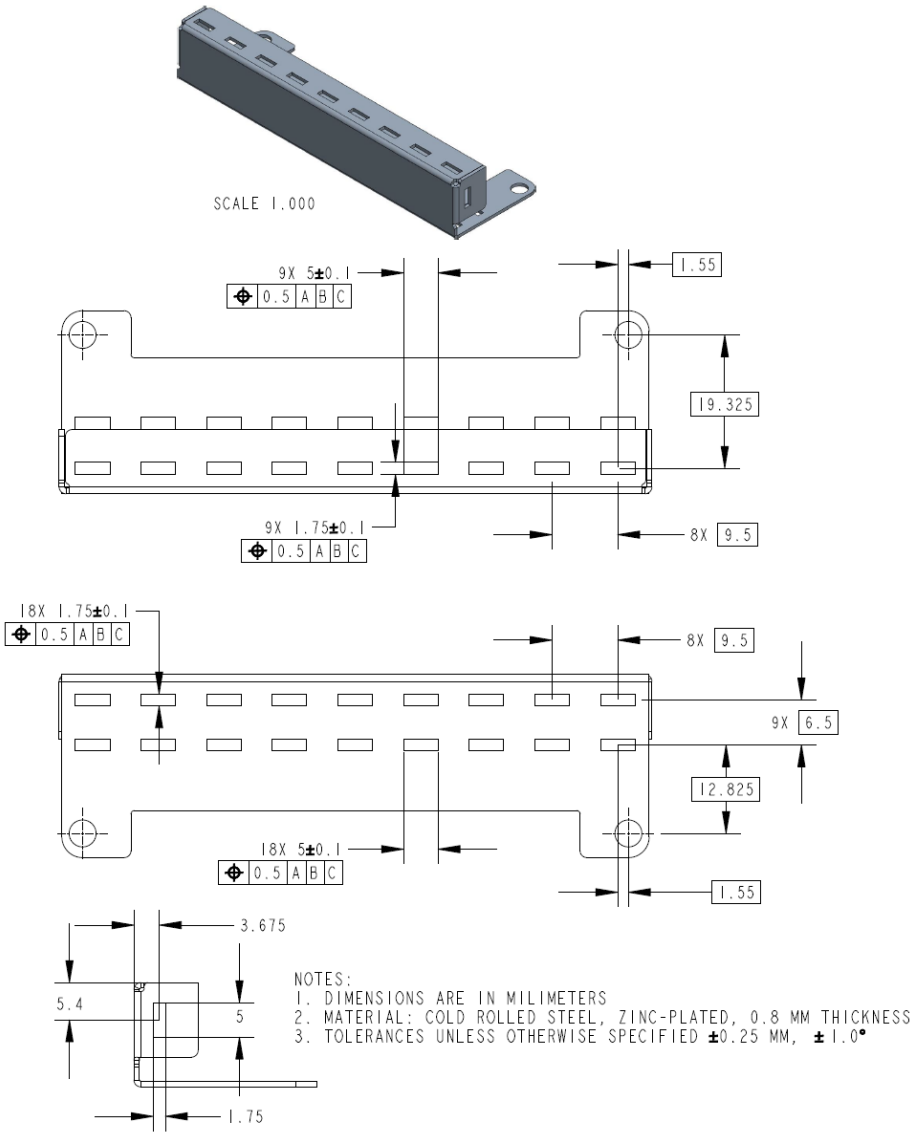


Figure 21: IFF EMI Finger Stock Faceplate Dimensions

2.4.1.2 IFF EMI FoF Gasket Faceplate Bracket

Figure 22 illustrates the specific dimensions for the bracket that are required to use the EMI FoF gasket components. It contains a 3D ISO view of the bracket, 2D projection views, and detail views for clarity. Please note the callouts at the bottom of the figure for part properties.

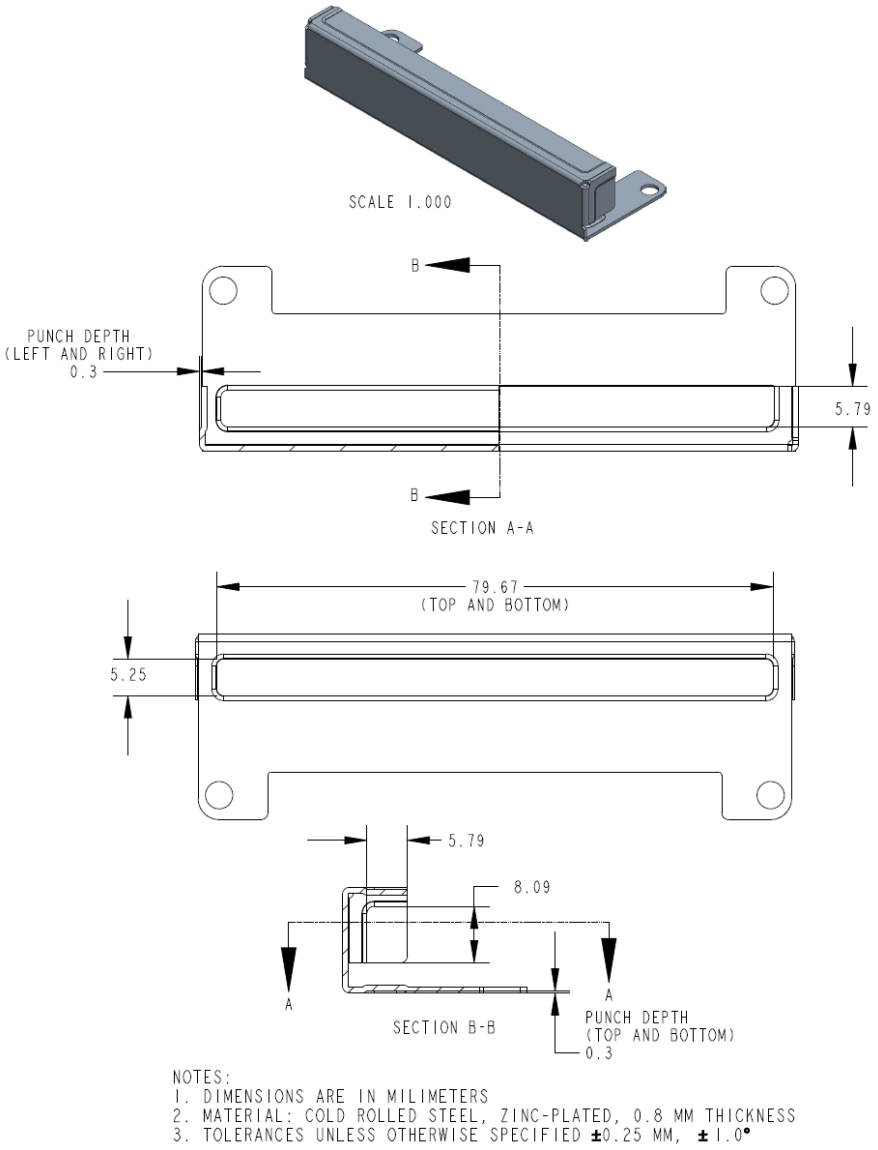


Figure 22: IFF EMI FoF Gasket Faceplate Dimensions

2.5 EMI Compliance Components

In the likely event that emissions must be contained in the system and pass certain regulatory testing for EMC, two EMI solutions are available as detailed in previous sections.

Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers.

For Option 1 of both EFF and IFF modules, EMI finger stock is utilized around all four sides of the faceplate bracket. There are two lengths: a nine-finger length and a single-finger length. These can be seen in Figure 23 below.

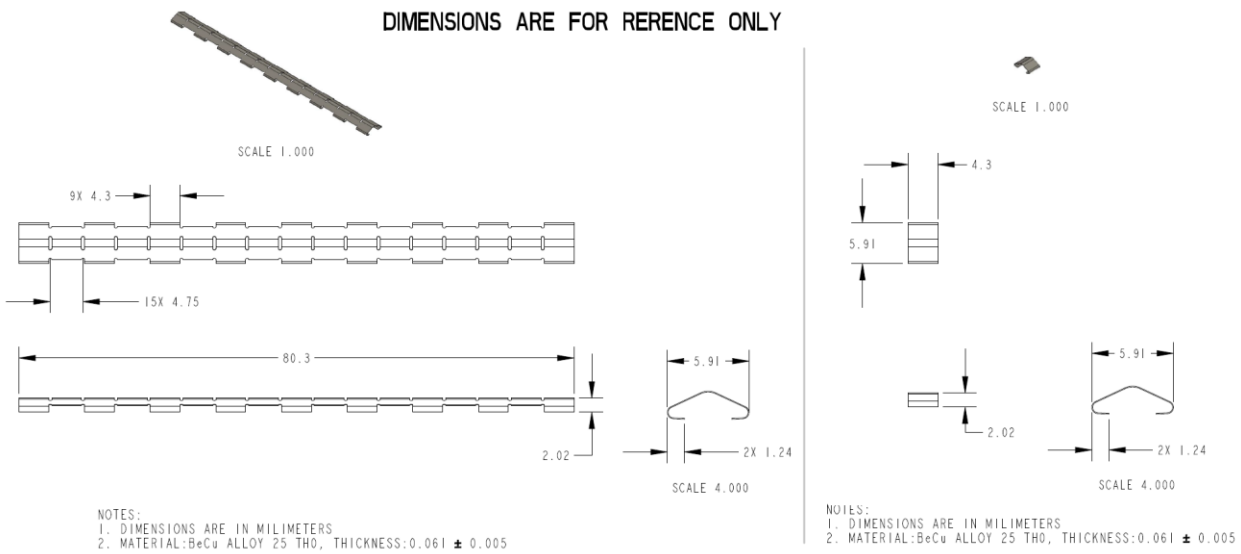


Figure 23: EMI Finger Stock Reference Dimensions

For Option 2 of both EFF and IFF modules, Fabric-over-Foam (FoF) gaskets are utilized around all four sides of the faceplate bracket. There are two lengths: a 78.2 mm length and a 7.35 mm length. These can be seen in Figure 24 below.

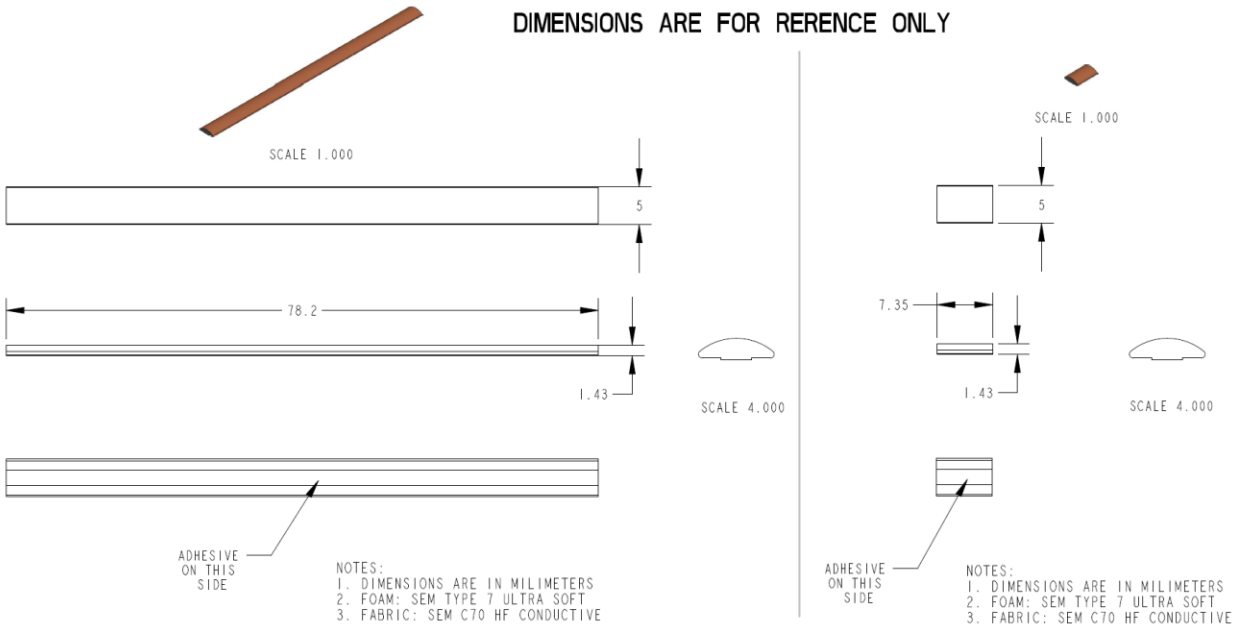


Figure 24: EMI FoF Gasket Reference Dimensions

There is a FoF gasket that may be applied to the inside of the front faceplate surface. This gasket has cutouts matching the sheet metal connector cutouts present on the from faceplate wall where the individual connector faces protrude through. It is compressed by the front perimeters of the connector face housings, ensuring good contact for conductive grounding. Gasket connector cut-outs and perforations are excluded from the figures and may be customized per system configuration and system airflow requirements.

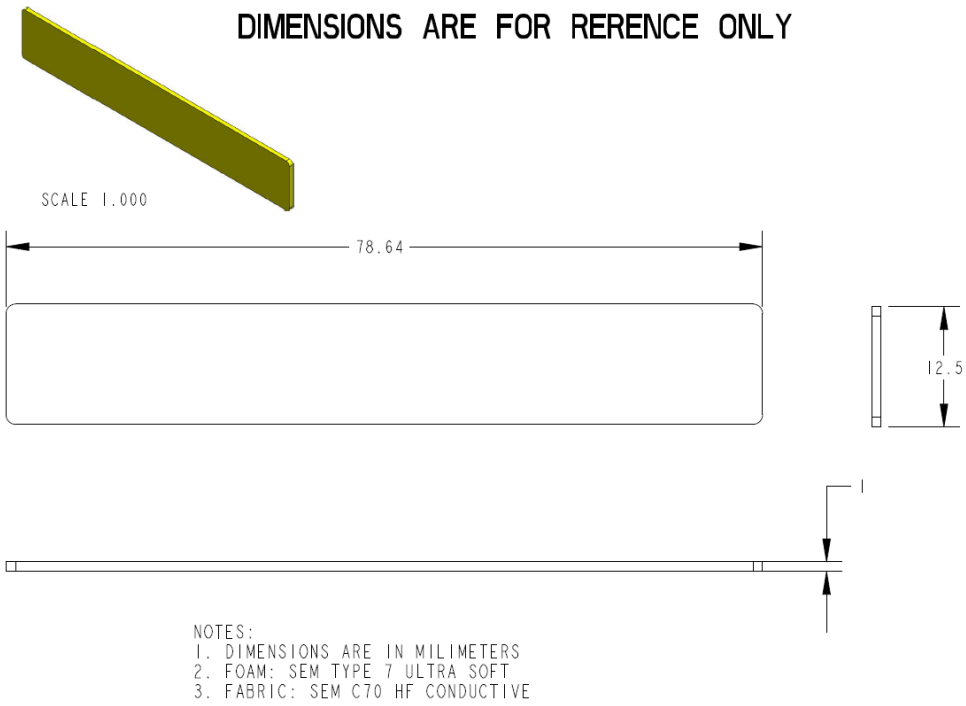


Figure 25: EMI Front Faceplate FoF Gasket Reference Dimensions

2.6 Insulation Requirements

All OCP DC-SCM 2.0 modules shall implement an insulator to prevent the bottom-side board components from shorting out to the baseboard chassis. The recommended insulator thickness is 0.127 mm (0.005”) and shall reside within the following mechanical envelopes for the EFF and IFF form factors. The total stack up height of the secondary side components, insulator and the labels shall not exceed the 2 mm keep-in dimension as shown in Figure 6 and Figure 26.

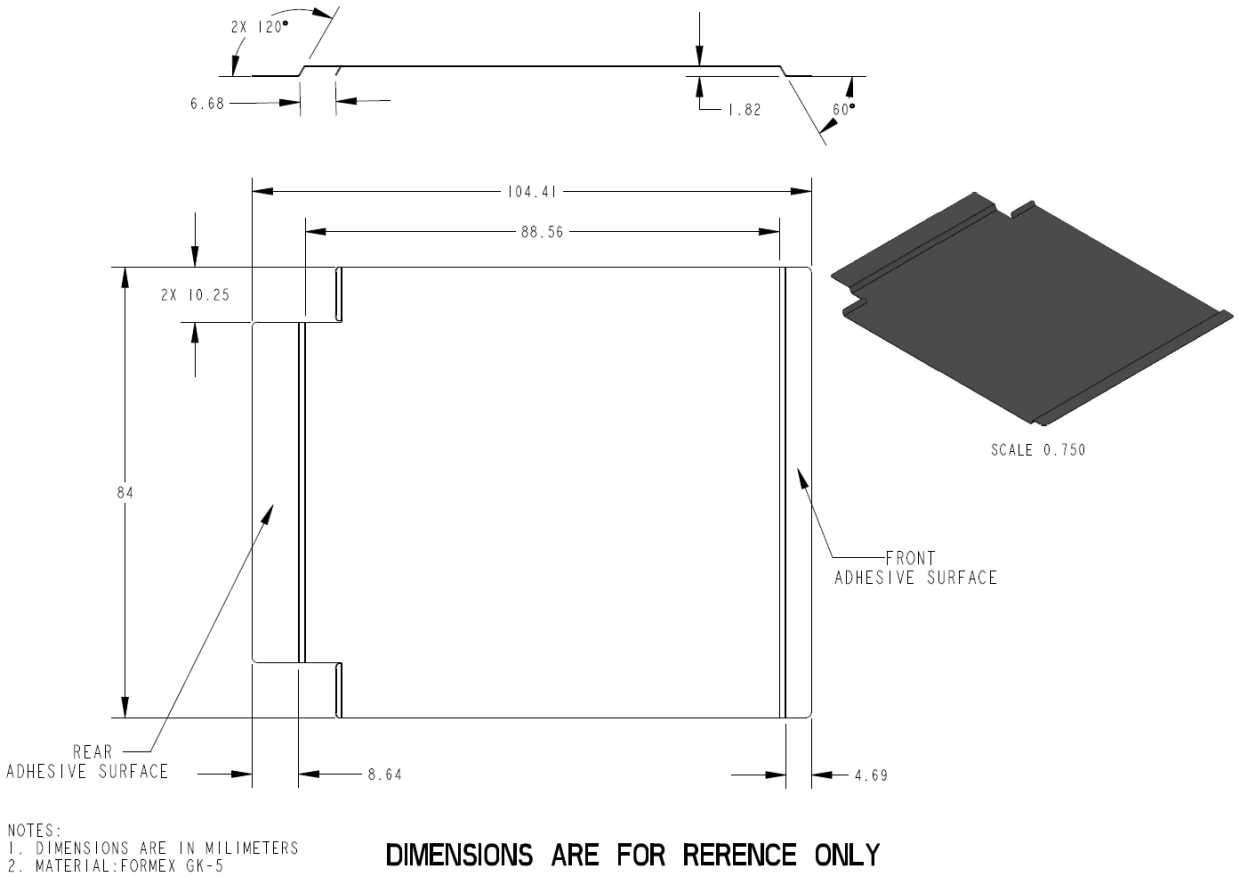


Figure 26: Insulator Dimensions

2.7 Module Guide Rails

The EFF version of the module is designed to leverage most of the geometry of the OCP NIC 3.0 reference rails. There is one major change to the geometry, and that is a set of 23.8 x 0.6 mm cuts at the ends of the rails. This is to enable the inside rail surface to drive the horizontal position of the module, and not the mounting screws that would normally interfere in these areas. Note that the mounting screw locations for DC-SCM 2.0 are different than the locations in the OCP NIC v3 specification. This modified rail design is symmetric and can be rotated 180° to have a left and right-side rail set.

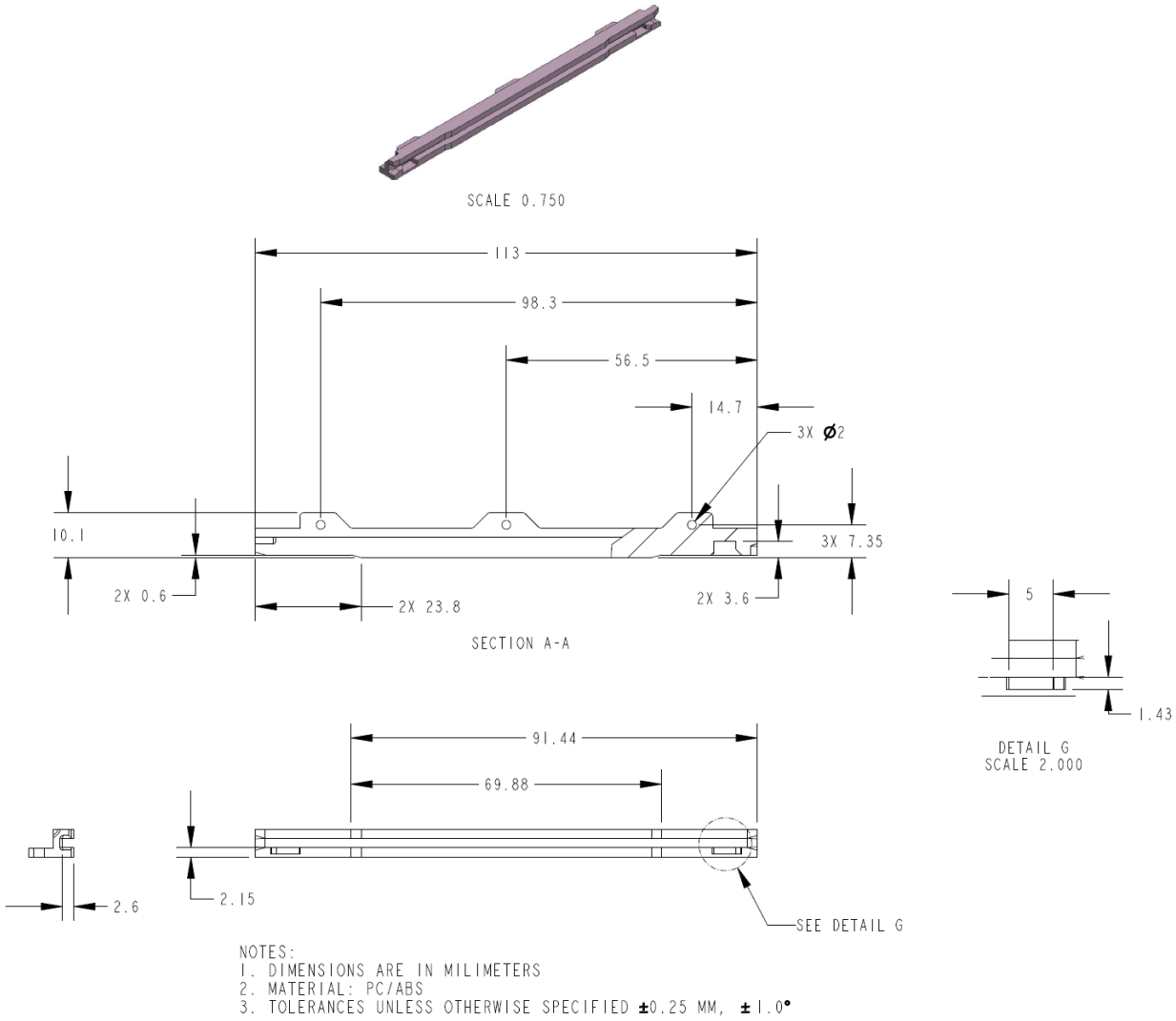


Figure 27: EFF Module-in-Tray Rail Dimensions

For the IFF version there are two options: 1) to reuse the modified DC-SCM 2.0 reference rail design, or 2) use the Module-in-Tray rail reference designs. There is a left and a right rail that make up the set; they are basically mirrored components. They provide a means to retain the module when the DC-SCM and baseboard are assembled together on a tray prior to assembly into the chassis. These notches are illustrated in Figure 5, Detail C. The guide rails have hook/slot features that interface in these areas. If the rail features shown in Figure 28, Details E and F are utilized, they may also serve as a locking mechanism to prevent module removal externally.

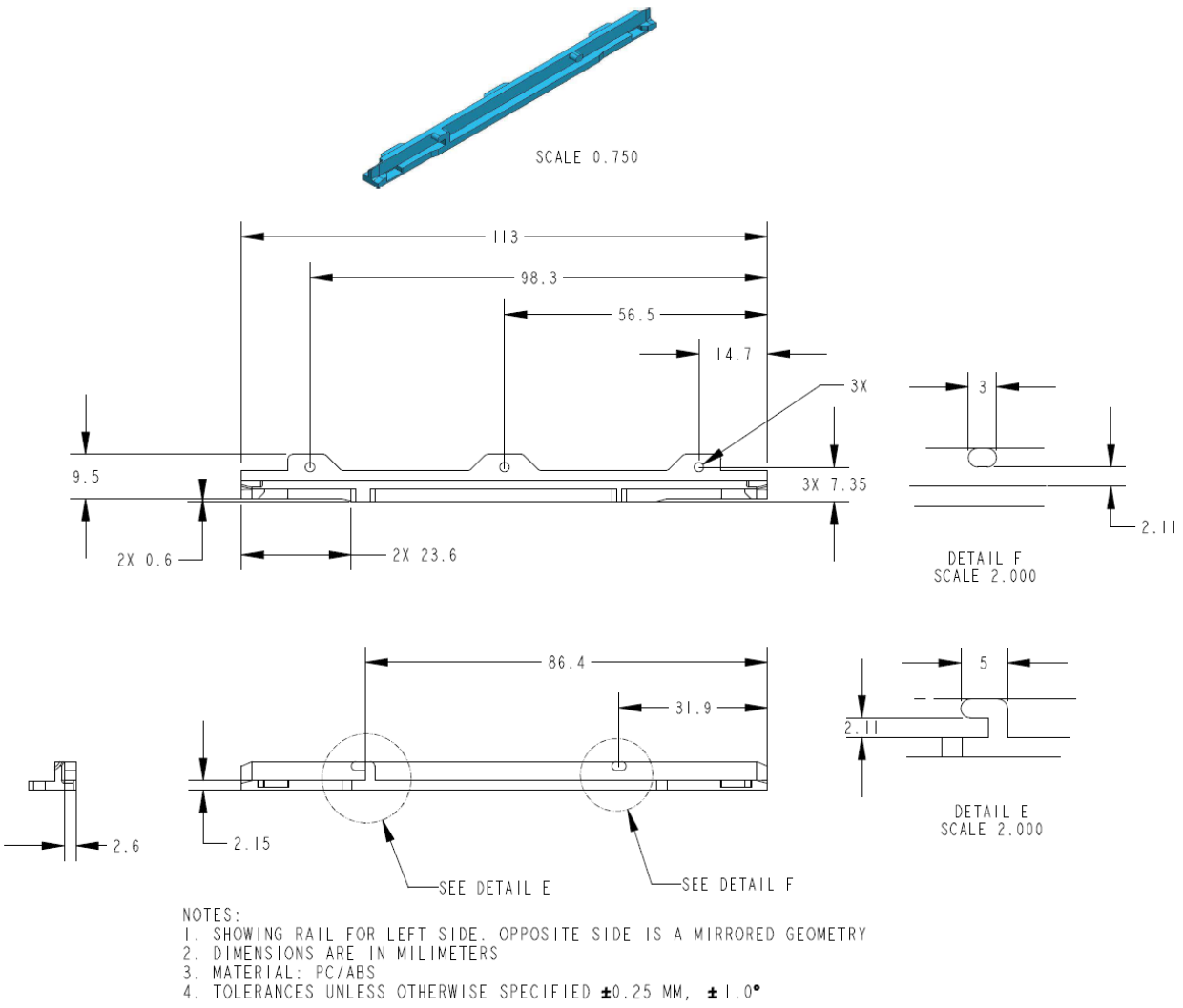


Figure 28: IFF Module-in-Tray Rail Dimensions

2.8 Chassis Bay Opening Requirements

All OCP DC-SCM 2.0 modules shall fit within the chassis opening defined below in Figure 29. Sheet metal flanges on four sides are bent inwards to provide surfaces for the EMI solutions to make contact with and provide a conductive path to ground. The height of the chassis cutout is dependent on where the module is positioned relative to the card edge connector on the baseboard.

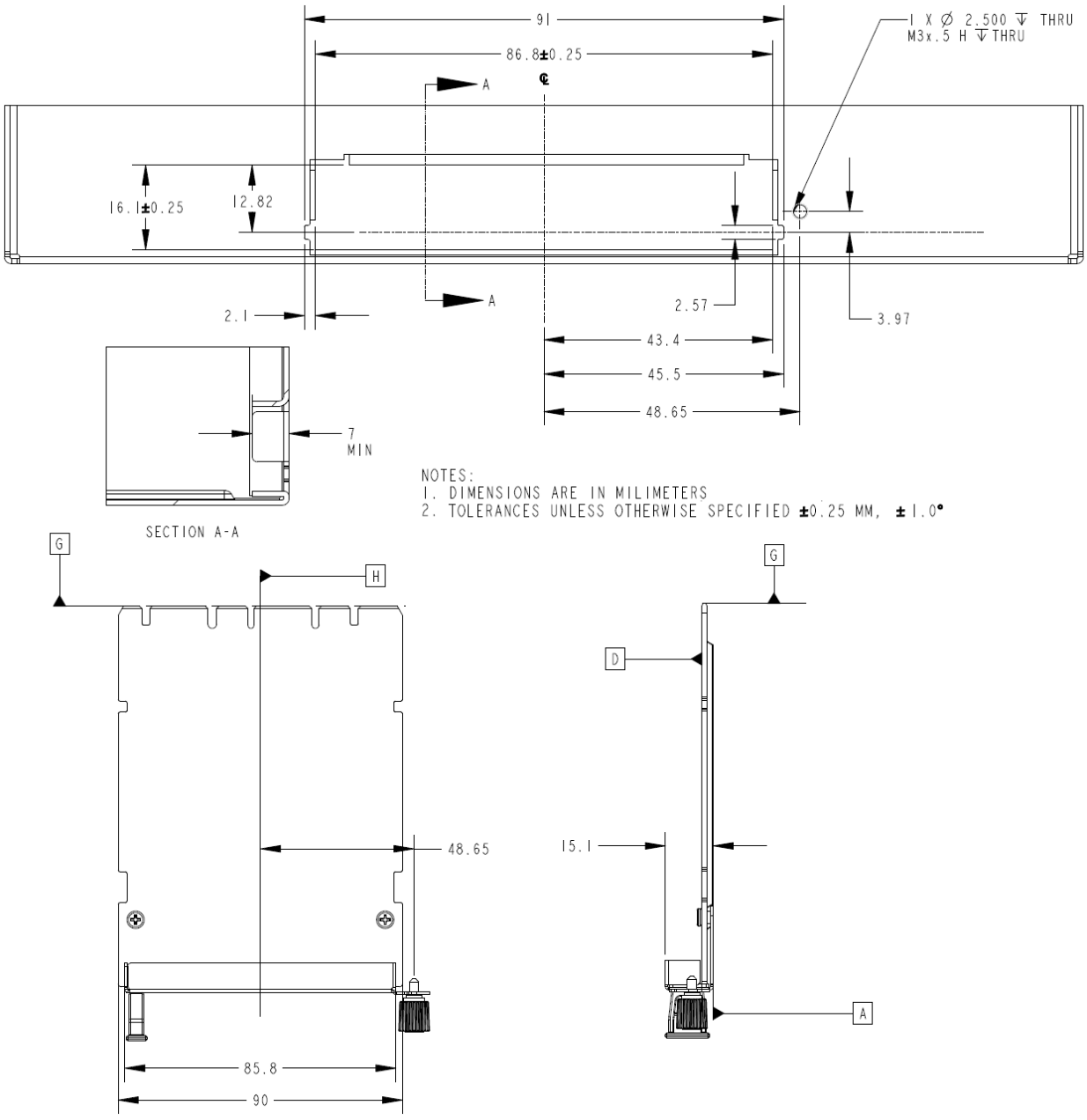


Figure 29: Chassis Bay Opening Dimensions

3 Interface Definition

3.1 DC-SCI Card Edge Connector Definition

The DC-SCI card edge connector interface is compliant to the SFF-TA-1002 specification with respect to the 4C+ connector size. Note that while the interface is mechanically compatible with the 4C+ specification, it does not support the SFF-TA-1009 pinout definition and is therefore not electrically compatible with EDSFF nor OCP NIC 3.0 devices. The pinout is defined in a spreadsheet file separate from this document. Mechanical details of the edge finger requirements are shown in Figure 30, Figure 31, and Figure 32.

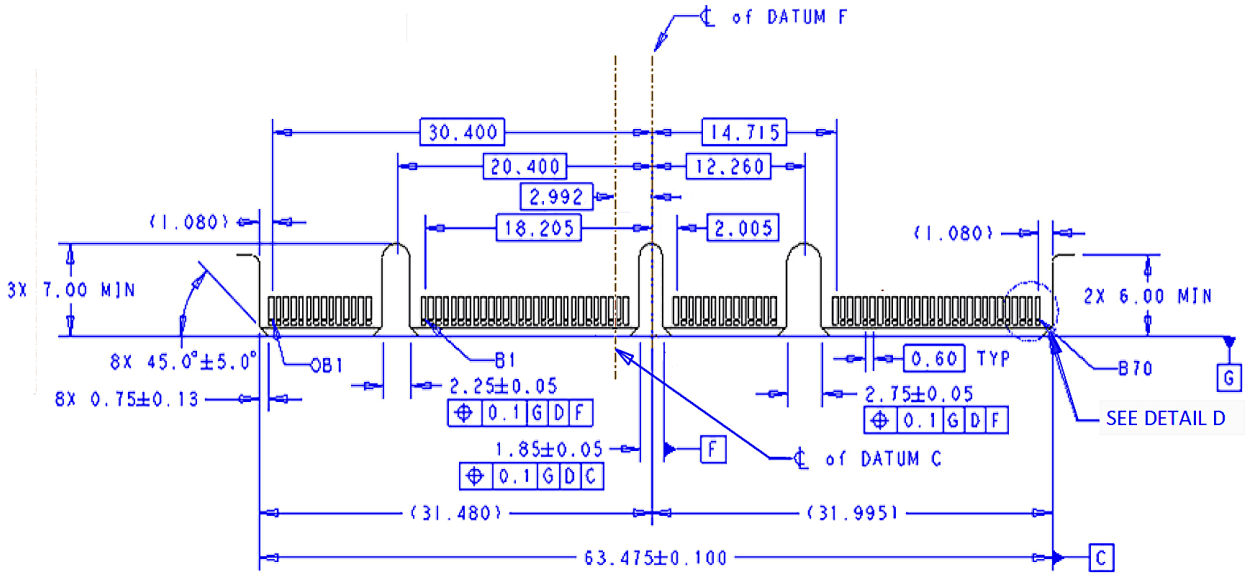


Figure 30: Card Edge Connector Dimensions – Top Side ("B" Pins)

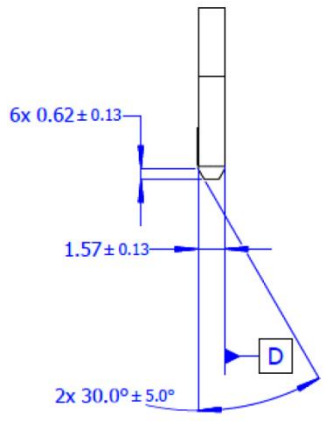


Figure 31: Card Edge Profile Dimensions

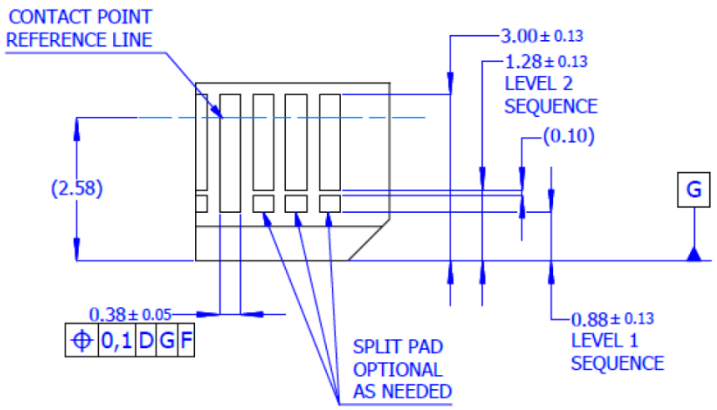


Figure 32: Card Edge Connector – Detail D

3.2 Gold Finger Plating Requirements

The minimum DC-SCM gold finger plating shall be 30 µinches of gold over 50 µinches of nickel.

3.3 HPM Connector Definition

The mating connector on the HPM is mechanically compliant to the 4C+ connector as defined in the SFF-TA-1002 specification for right angle, straddle mount and vertical form factor connectors. All three connector options are supported by this specification. The detailed pin list and pinout are defined in an accompanying spreadsheet document for easier reference and portability into designs.

3.3.1 Straddle Mount Connector

Straddle mount connectors are intended for use in designs in which the DC-SCM is installed fully co-planar to the HPM. The dimensions for the connector are shown in Figure 33.

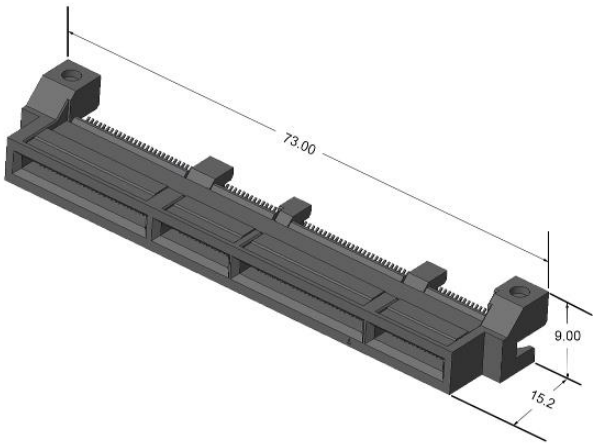


Figure 33: Straddle Mount Connector Dimensions (in mm)

The straddle mount connectors support four HPM PCB thicknesses. The available options are shown in Table 1. PCB thickness must be controlled to within ±10%. Note that the DC-SCM PCB thickness is required to be 0.062” (1.57 mm) while the HPM PCB thickness can vary from 0.062” (1.57 mm) to 0.110” (2.79 mm).

Table 1: Straddle Mount Connector PCB Thicknesses

Connector	Mating (SCM) PCB Thickness	Host (HPM) PCB Thickness
A	0.062” (1.57 mm)	0.062” (1.57 mm)
B	0.062” (1.57 mm)	0.076” (1.93 mm)
C	0.062” (1.57 mm)	0.093” (2.36 mm)
D	0.062” (1.57 mm)	0.105” (2.67 mm)
E	0.062” (1.57 mm)	0.110” (2.79 mm)

The choice of HPM PCB thickness impacts the offset of the DC-SCM with respect to the HPM PCB. This needs to be accounted for in the system design. Table 2 and the accompanying Figure 34 and Figure 35 details the PCB thickness and offset supports for the connector options.

Table 2: Straddle Mount Connector PCB Offsets

Name	**Pins**	**Style and Baseboard Thickness**	**Offset (mm)**
4C+	168	0.062” (1.57 mm)	Coplanar (0 mm)
4C+	168	0.076” (1.93 mm)	-0.3 mm
4C+	168	0.093” (2.36 mm)	Coplanar (0 mm)
4C+	168	0.105” (2.67 mm)	Coplanar (0 mm)
4C+	168	0.110” (2.79 mm)	Coplanar (0 mm)

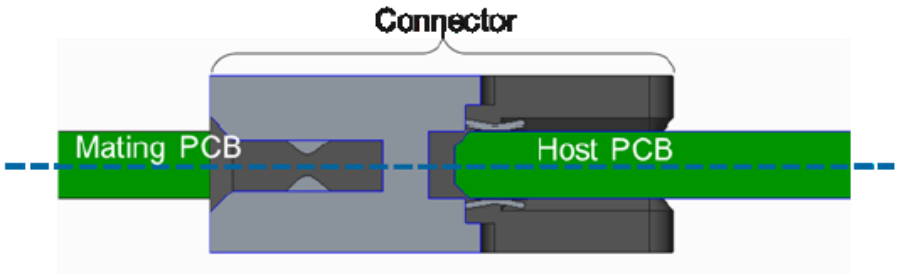


Figure 34: Straddle Mount Connector 0mm Offset for 0.062”, 0.093”, and 0.105” HPM PCB

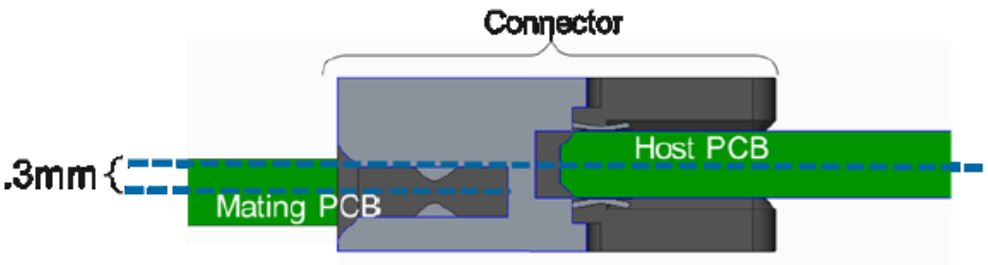


Figure 35: Straddle Mount Connector -0.3 mm Offset for 0.076” HPM PCB

3.3.2 Right Angle Connector

Right angle connectors are intended for a similar use but enable an increased DC-SCM bottom side keep out. Use of a right-angle connector eliminates any impact of the HPM PCB thickness with relation to the connector offset ensuring a constant 4.05 mm offset for all designs. The dimensions for the connector are shown in Figure 36.

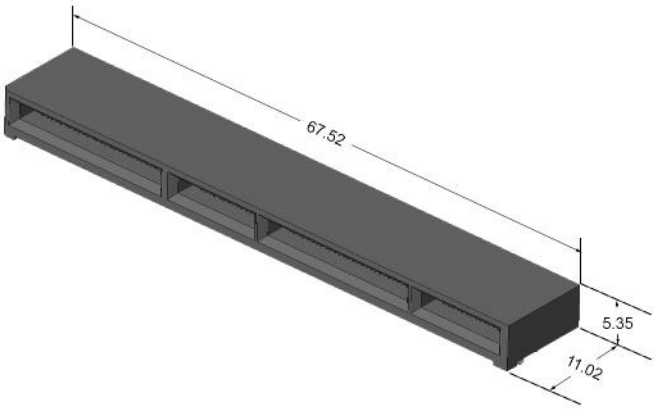


Figure 36: Right Angle Connector Dimensions (in mm)

Figure 37 details the PCB thickness and offset supports for this connector option.

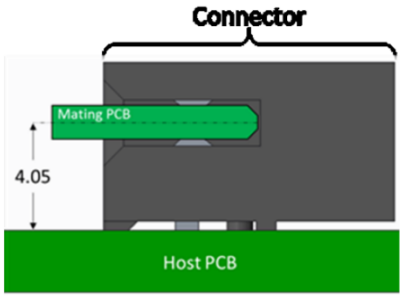


Figure 37: Right Angle Connector Offset

3.3.3 Vertical Connector

Vertical connectors are intended for use in vertical form factors. The dimensions for the connector are shown in Figure 38.

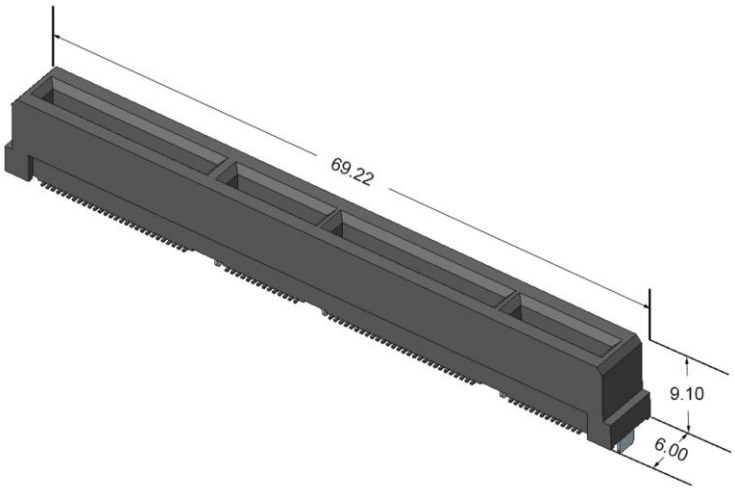


Figure 38: Vertical Connector Dimensions (in mm)

3.4 DC-SCI Pin Definition

An overview of the interfaces supported by DC-SCM 2.0 connector pinout is defined in the Table 3 below.

Table 3: DC-SCM 2.0 Pinout Overview

Primary Function	Alternative Functions	Dedicated Dual Node Functions
12 V Aux Power	-	-
Power Sequencing & Present Detection	-	-
JTAG	-	-
LTPI (LVDS)	-	-
BMC PCIe x1 Endpoint	-	-
SCM PCIe x1 Endpoint	-	-
eSPI (Single Node/CPU P0)	-	-
PECI	GPIO	-
SPI	1 x GPIO	-
QSPI (Single Node/CPU P0)	1 x GPI on CS1	-
BMC PCIe Root Complex	BMC USB 3.1 Host	-
BMC USB 2.0 Host	HPM (CPU) USB 2.0 Host	-
SCM USB 2.0 Controller Port to HPM Wraparound	HPM (CPU) USB 2.0 Host	-
NCSI	7 x GPIO	-
2 x I3C 1.0 V	2 x FSI 1.2 V	-
1 x I2C/I3C 1.8 V	eSPI (CPU P0) CS1/ALERT1	-
5 x I2C/I3C 1.8 V	-	QSPI (CPU P1), eSPI (CPU P1) CS1/ALERT1

10 x I2C 3.3 V	UART1, SGPIO, NCSI2	eSPI (CPU P1) 1.8 V, SGPIO, 4xGPIO, NCSI2
1 x GPI	SPI IRQ	QSPI (CPU P1) CS1
SPI TPM	2 x I2C/I3C 1.8 V, QSPI TPM CS	QSPI (CPU P1)
UART0	1 x GPIO, PCIe Reset (BMC RC), NCSI2 (TX_EN)	PCIe Reset (CPU P1), PCIe Reset (BMC RC), NCSI2 (TX_EN)
SCM PCIe x4 Endpoint	Bifurcation options (2x2, 4x1), USB 3.1 Host (HPM CPU or BMC), LTPI2, DisplayPort, SGMII, SCM USB 2.0 Host	BMC PCIe Endpoint x1 (CPU P1), SCM PCIe Endpoint x1 (CPU P1), LTPI2, HPM (CPU P0) USB 3.1 Port Wraparound, HPM (CPU P1) USB 3.1 Port Wraparound

The detailed pin list and pinout are defined in an accompanying spreadsheet document for easier reference and portability into designs. This is defined with the following rules:

- The pin list includes each signal name (preferred HPM and DC-SCM board net names that include functional and directional nomenclature), gold finger lengths, single & dual node usages, voltage, direction, and typical usage details. As much signal ambiguity as possible was removed from signal names as well as duplication of such parameters in individual interface sections within this specification.
- Multi-function DC-SCI pins list the functions starting with the most typical expected usage first.
- When multiple voltages are listed for a signal, they follow the respective alternate pin function order. If a voltage differs between single and dual node, it is described as such.
- The contact sequence for each pin indicates the order in which the pins make contact between the HPM and the DC-SCM. The GND pins are required to be long pins or 1st mate. The PRSNT0_N/ PRSNT1_N pins and P12V_AUX pins are required to be short pins or 2nd mate. However, the remaining pins indicated as 2nd mate can be flexibly assigned as long pins/1st mate if dictated by design or DFM requirements.

3.5 DC-SCI Signal Descriptions and Examples

The detailed signal names and descriptions are included in the accompanying spreadsheet, utilizing the notation of: ***function_(bus source)_(signal source)_(signal destination)_Instance#_Node#_Polarity***

Example: PCIE_HPMROOT_HPM_SCM_P1_N

Implementers should reference the relevant bus specifications for frequencies, signal integrity aspects and functional details. There is no attempt to duplicate such information here.

For any mature industry standard interfaces, it is expected that the design of the DC-SCM follows the standard practice regarding signal treatment guidelines and requirements.

3.5.1 HPM to SCM PCIe

3.5.1.1 HPM to SCM PCIe Lanes

The DC-SCI supports several PCIe bus options between the HPM and the DC-SCM.

- Typically, PCIe Gen 2.0 but supportable up to PCIe Gen 5.0 x1 Interface (pins A30-B31): This interface is typically connected to a BMC as a PCIe endpoint for usages including enabling host to BMC communication for functions such as video, MCTP over PCIe VDM, memory mapped PCIe device and/or a USB controller.
- Typically, PCIe Gen 2.0, but supportable up to PCIe Gen 5.0 x1 Interface (pins A65-B66): This is typically connected to a USB host controller, due to a trend of less hosts providing such functionality.
- Up to PCIe Gen 5.0 capable x4 Interface (pins OA2-OB12): This interface enables the HPM to communicate with endpoint(s) on or downstream of the DC-SCM. The bus may be link subdivided as 1 x4, 2 x2 lanes, 4 x1 or x2 x1 x1 lanes. Additionally, multi-node HPMs may choose to provide upstream ports split between nodes.

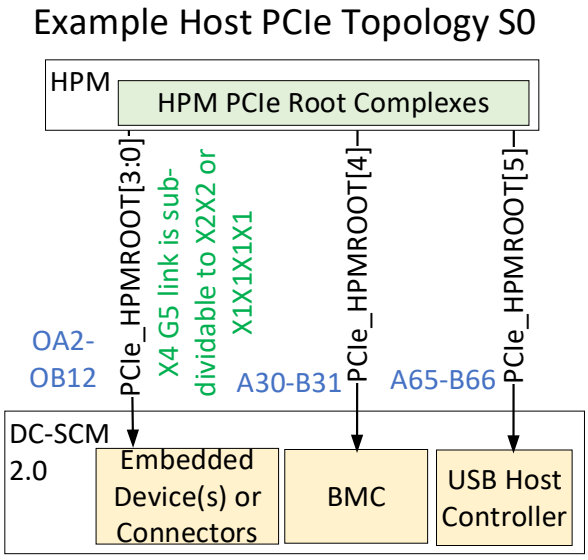


Figure 39: Host PCIe Mapping Example

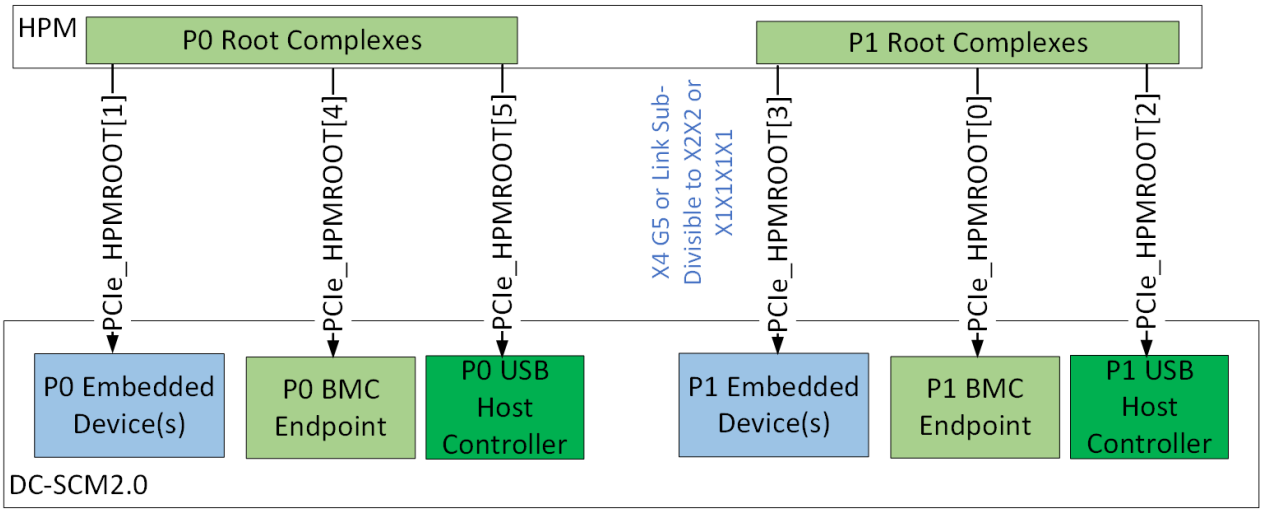


Figure 40: Dual Node PCIe Example

3.5.1.2 HPM to SCM PCIe Clocks

The DC-SCI supports 2 HPM provided clock interfaces. In a typical scenario, PCIE_HPM_SCM_CLK_100M_0 is expected to feed the X4 endpoint (e.g., Gen5 compatible) and PCIE_HPM_SCM_CLK_100M_1 feeds other slower devices (such as via a clock buffer to fan out to endpoints such as the BMC and USB host controller).

The general expectation is that all DC-SCM host PCIe endpoints are within the same clocking domain as each other, else separate reference clock methods may be necessary.

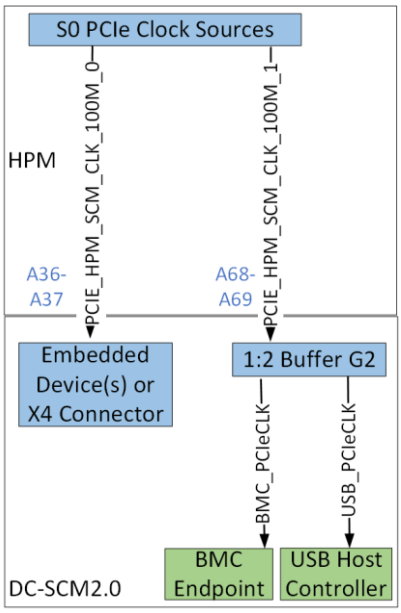


Figure 41: Typical host PCIe Clocking Example

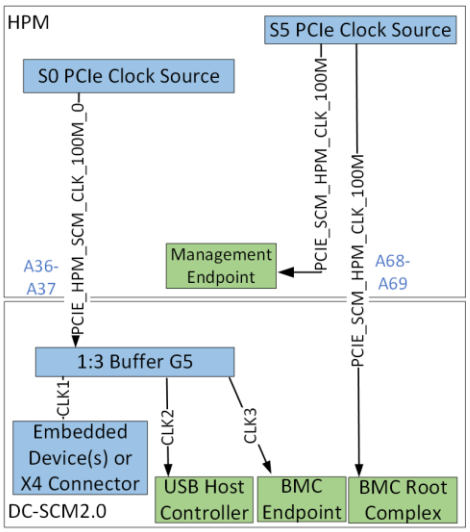


Figure 42: Alternate PCIe Clocking Example (When BMC Root Needs a Clock)

3.5.1.3 HPM to SCM PCIe Resets

Host PCIe Reset: There is one PCIe Reset signal per node from the HPM to the SCM intended for the PCIe host domain. The host domain control over the PERST signals varies such as being synchronous to platform reset, host firmware or HPM FPGA controlled. Usage and timings are out of scope of this specification. Scenarios where individual endpoint PERST control is required are also out of scope. An example may be when the platform chooses to use the BMC video controller before the host domain is initialized.

BMC PCIe Reset: Pin B51 can optionally be used for a BMC PCIe root complex discrete PERST# to endpoints on the HPM. Else, designers may choose to send the BMC PERST# over LTPI as a virtual wire.

3.5.2 SCM to HPM PCIe

3.5.2.1 SCM to HPM PCIe Lane

Pins A33-B34 offer three potential mutually exclusive use cases: 1) BMC acting as a PCIe root complex – This section; 2) Host domain passing from a PCIe switch a X1 back into the HPM or 3) USB3.1

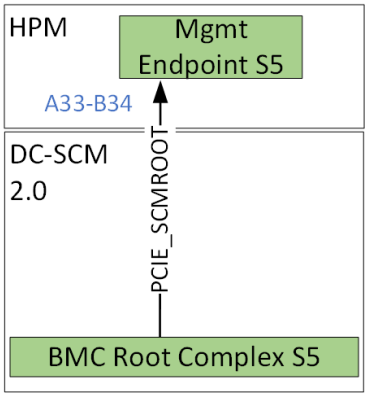


Figure 43: BMC PCIe Root Complex Example

Note that Pins A68-A69 are the same as in the HPM to SCM PCIe clocking example with a different alternate signal name based on usage.

3.5.3 SPI / QSPI / TPM_SPI

For single node mode, the DC-SCI supports three SPI interfaces:

- QSPI_HPMCNTRL: HPM is the initiator. This enables HPM communication with the BIOS flash devices on the DC-SCM. Only one QSPI bus is defined for a single-node design and two for a dual-node design.
- SPI_HPMCTRL_TPM: HPM is the initiator. This enables some hosts to have a dedicated TPM SPI bus. Other hosts utilize a dedicated CS on QSPI. In the latter mode, the other SPI pins are not usable except for alternate functions (e.g., I2C_I3C_1V8*). A more universal DC-SCM may provide the appropriate MUX logic for FW to steer the bus properly during the HPM discovery phase.
- SPI_SCMCNTRL: DC-SCM is the initiator. This enables DC-SCM communication with expansion devices on the HPM such as the HPM FPGA. Note that 1 SPI_HPM_SCM_IRQ0_N discrete signal is provided, like in DC-SCM 1.0. Other shared or non-shared interrupts must be via LTPI.

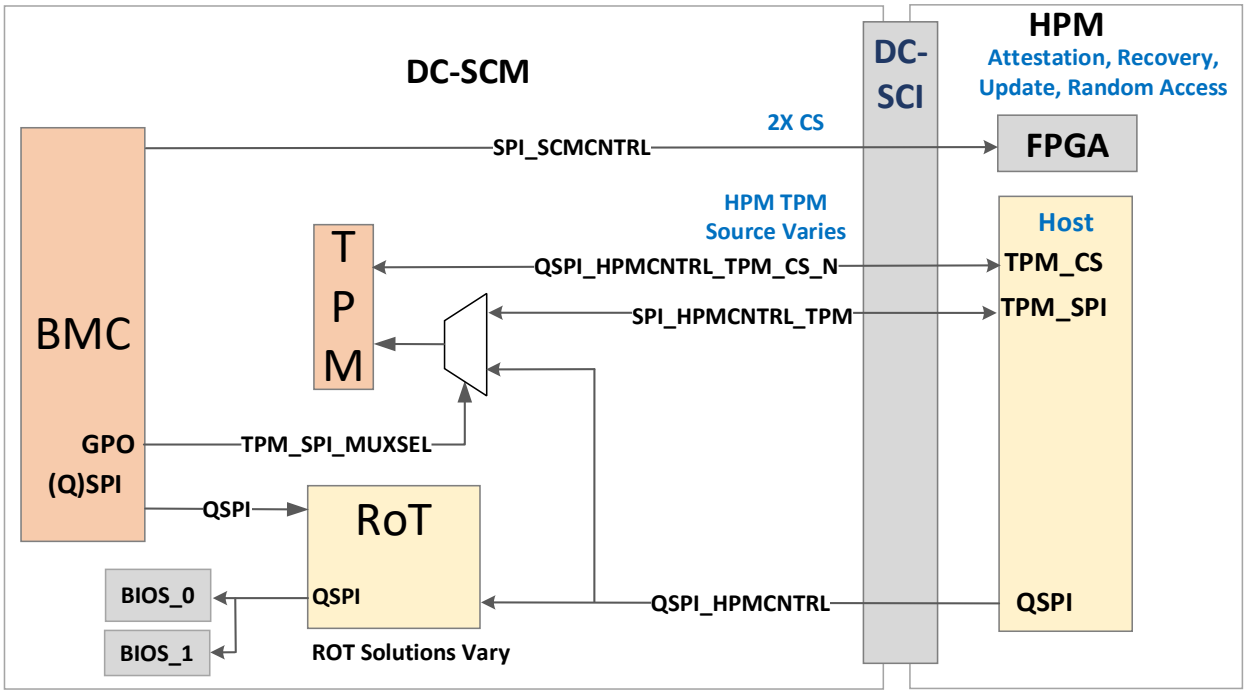


Figure 44: SPI Example Block Diagram

It is recognized that in dual node situations, that due to lack of pins for a 2nd dedicated SPI_HPMCNTRL_TPM bus and physical space on the DC-SCM that at least 1 optional TPM would need to be located on the HPM.

3.5.4 NC-SI RBT

The DC-SCI supports up to 2X RMII/NC-SI RMII-based Transport interfaces from the DC-SCM to the HPM. Applications using one NC-SI, should use the 1st interface instance (pins B43-B49). Platforms utilizing two NC-SI interfaces may choose to do so for either redundancy or signal integrity improvements or for use with each of up to two nodes. This interface enables high speed sideband management to NIC(s). Note: To best account for timing requirements associated with the 50MHz +-100ppm NCSI clock, it is assumed that the clock source is located on the HPM. More timing guidance is provided later in this specification.

RXERR was removed in 2.0 since it is optional and not used in most scenarios and the pin was deemed more valuable for alternate functions.

3.5.5 eSPI

In single node configurations 1 HPM to SCM eSPI bus is provided. This includes CS1/ALERT1 in the DC-SCI, although the more typical scenario is to have CS1/ALERT1 terminate with the HPM FPGA, as shown in the picture below. Even though known hosts vary in their need for utilizing eSPI in S5, they are tolerant to S5 bias. Note that it is expected that CS0/ALERT0 are used for the BMC, regardless of if the HPM FPGA or SCM CPLD utilize eSPI (CS1/ALERT1).

Multi-node provides a second full eSPI interface. There is no LPC bus support for either mode.

Host to BMC interface details when eSPI is unavailable are outside the scope of this specification.

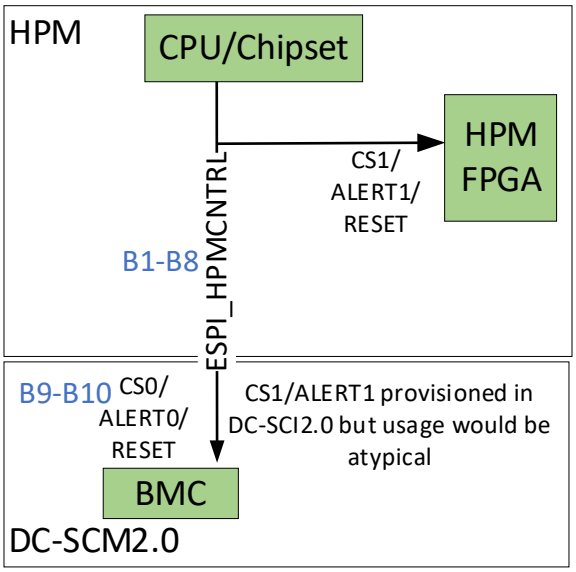


Figure 45: ESPI Example Block Diagram

3.5.6 LTPI

The DC-SCI defines the LVDS Tunneling Protocol & Interface (LTPI). It uses total of 8 x CPLD/FPGA LVDS differential I/O pins for connecting the SCM CPLD/FPGA with HPM CPLD/FPGA.

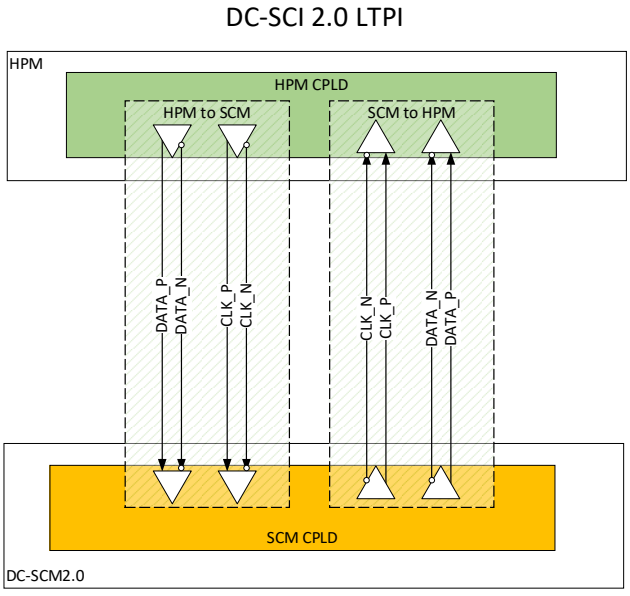


Figure 46: DC-SCI LVDS differential channels between SCM and HPM

There is a total of 4x LVDS unidirectional links defined for HPM-to-SCM and SCM-to-HPM communication. The links in each direction are defined by 2 x LVDS-based channels i.e., DATA and

CLOCK. The description of the LTPI I/O pins and the direction of LVDS links from SCM CPLD and HPM FPGA is listed in the Table 4 below.

Table 4: LVDS Signal Descriptions

Function	HPM CPLD LVDS I/O	SCM CPLD LVDS I/O
LTPI_HPM_SCM_DATA_DN	TX Data Negative	RX Data Negative
LTPI_HPM_SCM_DATA_DP	TX Data Positive	RX Data Positive
LTPI_HPM_SCM_CLK_ DN	TX Clock Negative	RX Clock Negative
LTPI_HPM_SCM_CLK_ DP	TX Clock Positive	RX Clock Positive
LTPI_SCM_HPM_DATA_DN	RX Data Negative	TX Data Negative
LTPI_SCM_HPM_DATA_DP	RX Data Positive	TX Data Positive
LTPI_SCM_HPM_CLK_DN	RX Clock Negative	TX Clock Negative
LTPI_SCM_HPM_CLK_DP	RX Clock Positive	TX Clock Positive

The LVDS link is defined as AC-coupled to allow interoperability between different CPLD/FPGA Voltage I/O standards existing today. CPLD/FPGA devices in majority of cases have limited I/O voltage flexibility on LVDS Receiver (RX) Buffer I/O hence a voltage bias circuit is used to match the RX I/O buffer voltage requirements for given CPLD/FPGA. shows an example of AC-coupled LVDS electrical links one in each direction HPM-to-SCM and SCM-to-HPM. The DC-SCM 2.0 LVDS links have the following characteristics:

- **DC blocking capacitor's placement:** DC-SCM module
- **Voltage bias circuit placement:** Close to LVDS RX I/O buffer

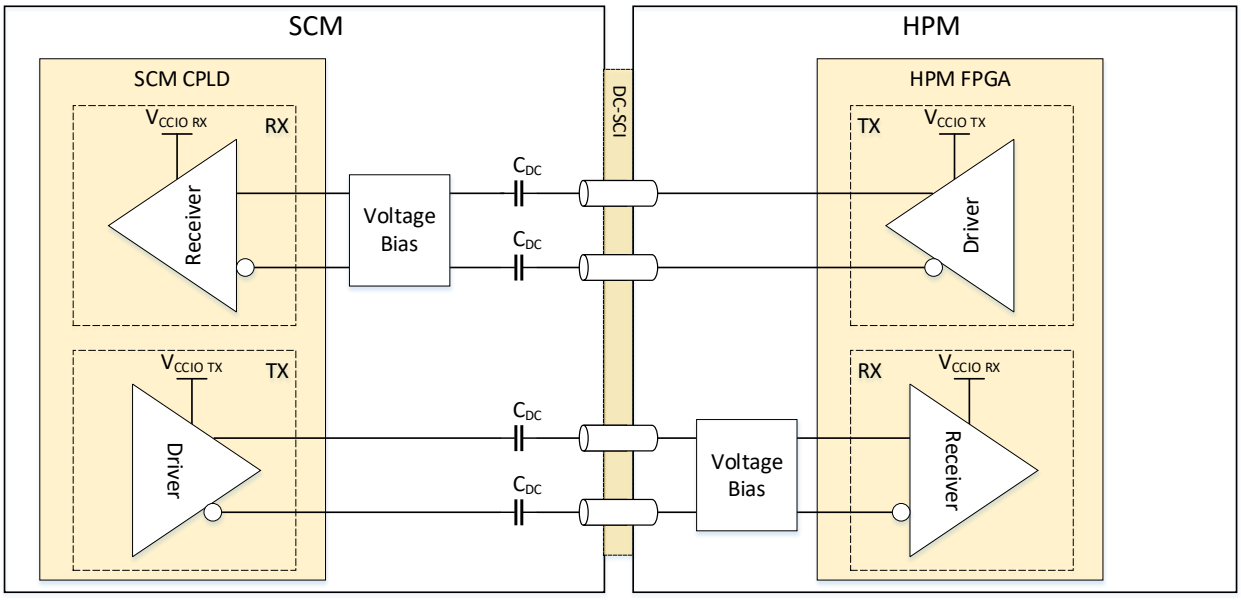


Figure 47: LVDS Links Electrical I/O

The Voltage Bias circuit for a single LVDS link is shown in Figure 48. All four LVDS links shall follow the same design of Voltage Bias circuits; as a result, two circuits shall be located on the SCM side and two on the HPM side. The Voltage Bias circuit is setting the common mode voltage at ½ of VCCIO for input RX Buffer and providing 100 Ohm termination resistance. The DC Blocking capacitor is defined at 0.22 µF which is derived from the LTPI interface Base Frequency and interface training requirements.

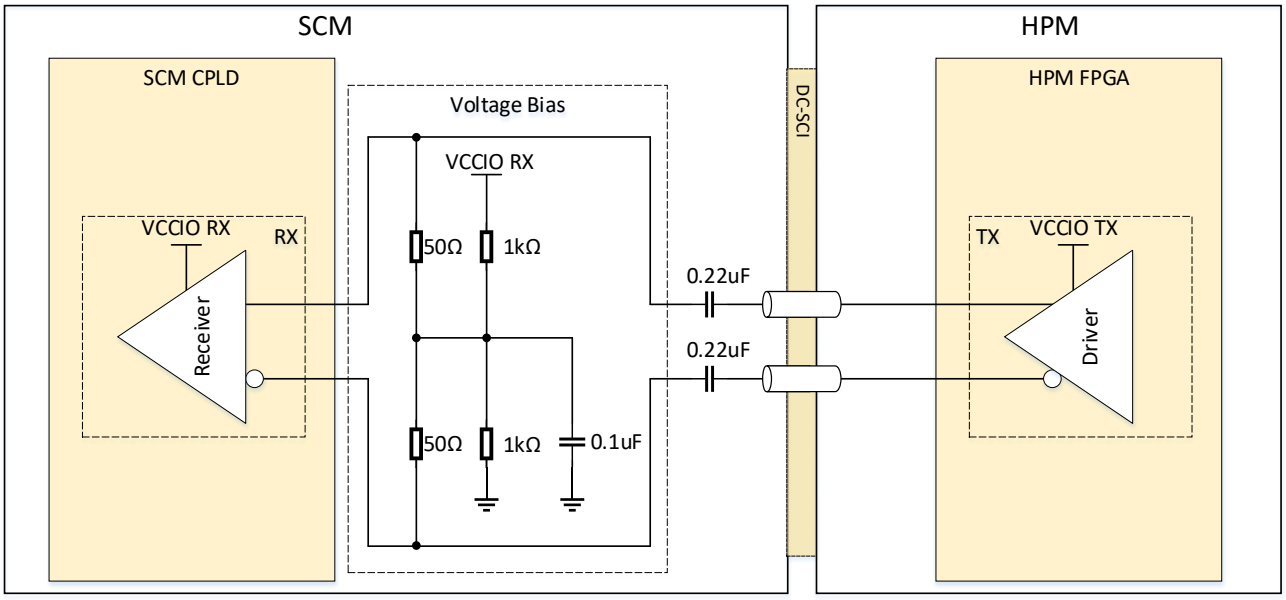


Figure 48: LVDS Voltage Bias Circuit

The electrical specification for the DC-SCM 2.0 LVDS links are defined in Table 5 below.

Table 5: LVDS Electrical Requirements

Parameter	Min.	Max.	Description
V_{OD}	100 mV	800 mV	Output Differential Voltage Swing
V_{ID}	100 mV	800 mV	Input Differential Voltage Swing
$V_{CCIO\ RX/TX}$	N/A	3.3V	LVDS VCCIO Voltage (Refer to CPLD/FPGA documentation)
V_{ICM}	N/A	($V_{CCIO\ RX}$ / 2) + 20%	Input common mode voltage on LVDS I/O pins
C_{DC}	0.22 uF	N/A	DC blocking capacitor
R_{TT}	100 Ohm - 5%	100 Ohm + 5%	LVDS Termination Resistor

The details of LTPI interface are covered in the DC-SCM 2.0 LVDS Tunneling Protocol and Interface (LTPI) Specification 1.0.

3.5.7 I2C / I3C

The DC-SCI 2.0 expands the I2C/I3C bus scenarios. At this time, no I3C functionality beyond the MIPI I3C Basic 1.1.1 specification is expected to be supported. HDR-BT (Bulk Transport) mode of operation is not

supported in the DC-SCI. HDR-DDR mode of operation is not precluded for use, but no efforts were spent to ensure proper operation is guaranteed. Designers should carefully refer to this specification in terms of supported modes of operation, use of MUXes or hubs, discovery protocols, etc.

The I2C bus mappings differ between the single-node and the dual node configurations. For a single-node design, the DC-SCI supports a total of 18 possible I2C ports from the DC-SCM to the HPM. These are allocated to two voltages across 10X at 3.3 V and 8X at 1.8 V for either I2C or I3C. The rules are as follows:

1) HPM must provide the appropriate pullup resistors for I2C busses.
2) HPM is responsible to provide cross power domain (AUX to Main) & necessary voltage level translation if targets differ from the DC-SCI voltage.
3) More I2C/I3C controllers are not precluded via controllers/ or bridges on interfaces such as PCIe, USB, LTPI, SPI or I3C to SMBUS hubs.
4) There is no explicit designation of a HPM pure Initiator to DC-SCM Target bus.
5) No discrete I2C/SMBUS alerts are included as any such needs are expected to be virtual GPIOs. I2C Alerts can optionally be supported using SPI_IRQ0, SGPIO or LTPI.
6) Fixed FRUID PROM address: It is required that on the HPM, the FRUID EEPROM be placed directly on channel I2C0 (Not behind a MUX or hub) at address 0xA0 (8-bit address). Note too that the device must support 10-bit addressing. This provides a fixed location for a BMC to detect an HPM type and load the necessary platform specific parameters to ensure full functionality of the platform. The data format is covered elsewhere.
7) If an optional authentication IC is supported on the HPM, it must also exist on I2C0. The device should be on the same segment and not downstream of a MUX to simplify the discovery method.
8) Multi-initiator is generally desired to be avoided and limited only to standardized use cases like MCTP over SMBus or IPMB.

Table 6: I2C/I3C Signal Descriptions for Single Node

Signal Name	Minimum Power State	Voltage (V)	Description
I2C_3 3_0	Pre-STBY	3.3	HPM FRU must be connect to I2C bus 0 for universal compatibility. If an optional authentication IC is supported on the HPM, it must exist on this bus.
I2C_3V3_*	S5	3.3	
I2C_I3C_1V8	S5	1.8	I2C/I3C or various other signals
I2C_I3C_1V0	S5	1.0	I2C/I3C or FSI

For a dual-node design, there are 6X I2C at 3.3V and 3X I2C at 1.8V. The 1.8 V I2C could be used for I3C. The bus numbers are not continuous to better match the single node naming convention.

Table 7: I2C/I3C Signal Descriptions for Dual Node

Signal Name	Minimum Power State	Voltage (V)	Description
I2C [0]	Pre-STBY	3.3	HPM FRU must be connect to I2C bus 0 for universal compatibility

I2C [1:2]	S5	3.3	These are dedicated I2C buses at 3.3 V
I2C [7]	S5	3.3	I2C or 2nd NCSI signals
I2C [8]	S5	3.3	I2C or 2nd NCSI signals
I2C [9]	S5	3.3	I2C or 2nd NCSI signals or UART1
I2C/I3C [3:5]	S5	1.8	I2C or I3C
I2C_I3C_1V0	S5	1.0	I2C/I3C or FSI

3.5.8 FSI

OpenPower Flexible Service Interface (FSI) is supported as alternate functions on these interfaces.

Table 8: FSI Signal Descriptions

Signal Name	Minimum Power State	Voltage (V)	Description
I2C_I3C_1V0_##_SCL / FSI_1V2_#_SCL	S5	1.0	Shared with FSI buses, I2C/I3C at 1.0 V only OR FSI at 1.2 V only

3.5.9 USB

3.5.9.1 Host USB

- As there is a trend in some chipsets to not support native USB host controllers, a space and cost-effective way to support host USB is via a PCIe X1 to USB host controller on the DC-SCM. This supports connections to the BMC, local and internal/external ports, and devices.
- In cases where a platform wants to support host domain USB 3.2 Gen1 devices or fanout on the HPM and native chipset USB host controllers are not available nor an additional PCIe to USB host bridge on the HPM is desired, the USBx_SCMHOST busses are available to be part of the HPM host domain. This is different from the BMC USB management domain. It is recommended to take caution with cross power domain connections since the same pins can be used with host and/or devices within the AUX S5 or Main S0 power domains.
- Two optional HPM_SCM USB 2.0 interfaces are available for legacy design where the host chipset retains USB2.0 host controllers/initiators. There are no USB 3.2 Gen1 HPM_SCM interfaces provided in DC-SCI 2.0.

3.5.9.2 Managed USB

- USB2_SCM_HPM may be used as the BMC managed USB host controller connectivity to the HPM for a high-speed management interface to various subsystems and extended peripherals.

- USB2_BMC_SCMOTG as a BMC managed USB interface may have the BMC serving as the USB host or device with static or dynamically changing roles (On-The-Go). A typical use case includes an external “service port”.
- USB3_SCMROOT_SCM_HPM is available as a managed USB interface for future BMCs or could be supported via the BMC PCIe root complex connected PCIe to USB bridge.

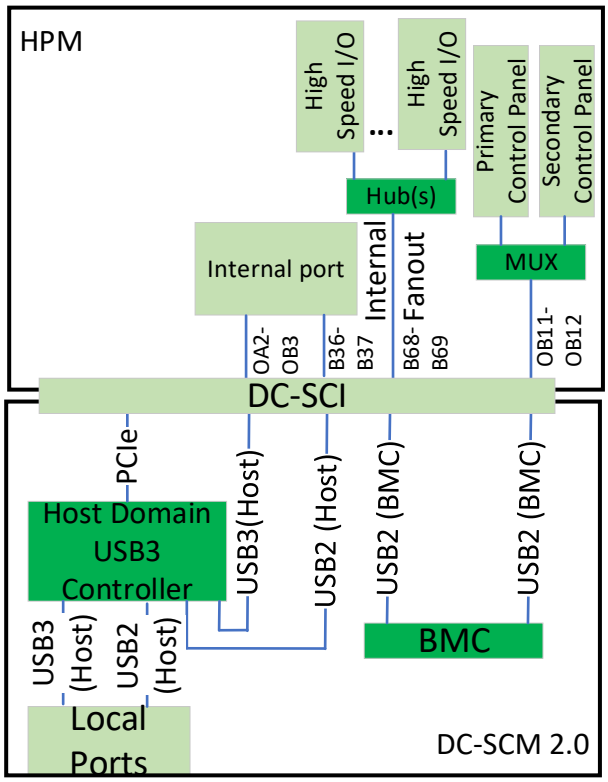


Figure 49: Example USB Block Diagram

3.5.10 PECI

The DC-SCI supports an optional PECI interface (bus + power) for health monitoring of CPUs. When this interface is un-used by the HPM architecture, it should be appropriately terminated on the HPM, refer to CPU vendor and BMC vendor specifications for detailed PECI electrical IO requirements. Note that the BMC controller PECI interface requires voltage to be supplied by the HPM.

When the PECI interface is not used on both the HPM **AND** DC-SCM the PECI_HPM_SCM signal may be used as a low voltage (0.85 V-1.21 V) GPIO biased only in host MAIN on S0 state. Also, PECI_VREF_HPM_SCM may be used as a unidirectional signal from HPM to SCM in the same voltage range. Direction is limited due to the nature of this being a power signal in PECI operation.

3.5.11 JTAG

The DC-SCI supports a BMC-initiator JTAG interface with possible uses of:

- HPM programmable device update (e.g., FPGA).
- Debug of ASICs or CPUs, often referred to as either at-scale or closed box debug. The design and security-related issues/constraints related to this interface are outside the scope of this specification.

3.5.12 UART

The DC-SCI supports two UARTs (3.3 V, TTL logic) with no hardware flow control signals. Typical uses are:

• UART0 - Host Debug Console (typically when not eSPI mapped)

• UART1 – Subsystem consoles (Smart NICs, RAID cards, etc.)

Additional physical UARTs may be supported through alternate interfaces like USB, PCIe, LTPI and SPI.

3.5.13 Battery Voltage

The DC-SCI supports one pin for 3.0 V battery power from the HPM.

Table 9: Battery Voltage

Signal Name	I/O	Voltage	Description
P3V0_HPM_SCM_BAT	I	3.0 V	3.0 V from coin cell battery located on HPM. Typical uses are RTC, CMOS and chassis intrusion logic Battery backed CPU registers, etc. DC-SCM current consumption from this rail will impact the HPM battery life and HPM shelf storage time. This should be comprehended by DC-SCM 2.0 and HPM designs. Typical DC-SCM 2.0 design shall not pull more than 1.2uA. DC-SCM must not source energy into HPM on this signal. When the battery is not in use, drain should only occur during measurement sampling of raw BAT rail.

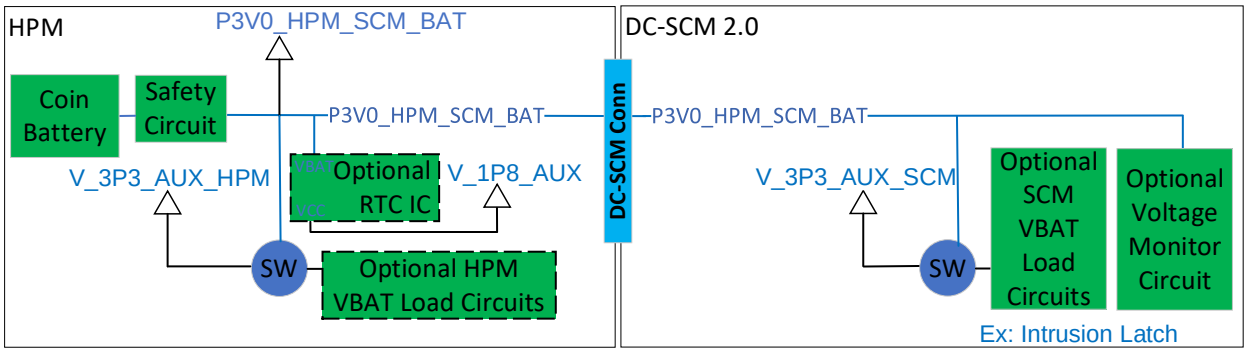


Figure 50: Battery Circuit

3.5.14 Intrusion

HPM_SCM_INTRUSION_N is the optional 3.3 V DC-SCI 2.0 input (unidirectional) signal from the HPM. Therefore, the general expectation is that optional chassis intrusion switch connectivity is to the HPM.

Note that active low designation is because the expectation is to use an intrusion button that is open when depressed (not intruded) and closed when released (cover removed).

3.5.15 Power States & Boot Sequence

The common power state nomenclatures are described below. All signals in the DC-SCI are categorized into each of these states indicating the minimum power state where bias is allowed at the DC-SCI.
The DC-SCM is not specified to support hot insertion or removal. In-rush control for the DC-SCM should be supported on the HPM to protect the circuitry from damage due to damaged connector pins, accidental removal.

Note that sad path or error condition handling aspects of the boot sequence are beyond the scope of this specification. The DC-SCI provides two active low presence pins. The HPM design is recommended to ensure that AUX power to the DC-SCM and HPM circuits are disabled when presence is not detected. A presence enabled eFuse may be used on the HPM but can be excluded provided the DC-SCM is locked with screws or other mechanical solutions.

Table 10: Power Sequence Signal Descriptions

Signal Name	I/O	Voltage (V)	Description
PRSNT0_N	O	3.3	Must be connected to PRSNT1_N on the DC-SCM. Must be pulled up on the HPM and used to enable power to the SCM.
PRSNT1_N	I	3.3	Must be connected to PRSNT0_N on the DC-SCM. Must be connected to GND on the HPM
HPM_STBY_EN	O	3.3	Active High. Indicates that all DC-SCM STBY power rails are enabled and good. Enables STBY power rails on the HPM
HPM_STBY_RDY	I	3.3	Active High. Indicates that all HPM STBY power rails are good. Can optionally be used to indicate that the HPM FPGA is configured.
HPM_STBY_RST_N	O	3.3	Active Low. Holds HPM standby devices in reset. Driven high by the DC-SCM to bring the standby devices on the HPM out of reset

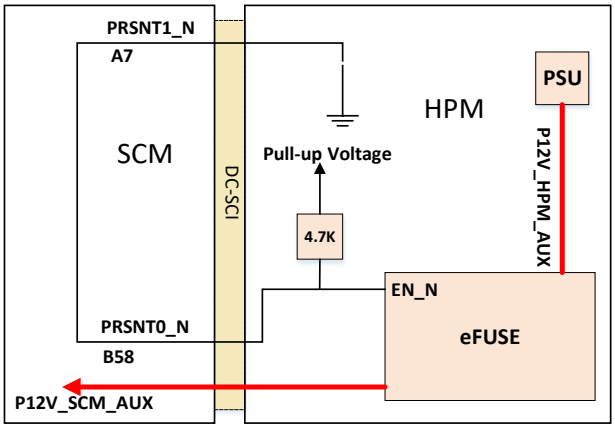


Figure 51: DC-SCM Presence Detection and Power Protection Example

This discovery sequence exists to ensure safety, avoid electrical incompatibility, and stress conditions are avoided. The following sequence is provided as a typical boot flow. It is not advised to bypass steps if interoperability is of concern.

Table 11: Power States and Discovery Sequence

Power State	Description	Notes
G3	No PSU Input power. Only bias is coin cell.	1
Pre-STBY	1: PSU input power delivers P12V_HPM_AUX output power 2: DC-SCM fully seated enables the HPM eFuse (if present – see example above), providing power to the DC-SCM. 3: SCM AUX VRs regulate, including VCC_SCM_HPM_FRU 4: SCM BMC boots (preceded by discrete PROT if it exists) to a point to read the I2C HPM FRU (required) & performs HPM crypto authentication (optional) 5: Upon compatibility check pass, SCM asserts SCM_HPM_STBY_EN	2 3
Pre-S5	6: HPM asserts HPM_SCM_STBY_RDY when all HPM AUX Rails are within regulation 7: SCM de-asserts SCM_HPM_STBY_RST_N.	
S5	8: S5-classified interfaces may engage. HPMs and SCMs may choose to use SCM_HBM_STBY_RST_N as the qualifier for engaging S5 allowed DC-SCI signals. 9: The SCM grants the HPM FPGA to enable the host CPU/Chipset (e.g., de-assert RSM_RST_N or assert AUXPWROK) to official enter S5. Host is OFF. This may be SCM_HBM_STBY_RST_N, virtual bit and/or via AUTH IC secure GPO. 10: Host WAKE request sources vary. Host power on request is typically blocked until a BMC grant so that the BMC may perform various boot and security services immediately before power on grant.	4
S0	11: BMC grants power on, HPM CPLD sequences the host into a full ON / S0 state	

Note 1: DC-SCI 1.0's Virtual_Reseat was removed from 2.0 because the same feature can be achieved through multiple alternate methods. The control method and aspects to guarantee AUX rail bleed off are currently beyond the scope of this specification.

Note 2: Although the DC-SCM is not intended to support hot plug or hot removal, an eFUSE is included on the HPM to protect the DC-SCM from any overcurrent events. To ensure that there are no voltage leaks between the HPM and DC-SCM, it is recommended that pullup resistors for all I/O on the DC-SCI be placed on the HPM.

Note 3: If the HPM FRU is deemed incompatible or goes undetected, the DC-SCM must halt the boot sequence, to avoid possible electrical stress conditions. This is called "Plug-N-Detect-Else-Halt".

Note 4: Not included in these states are scenarios such as a system level battery hold up, or orchestration of the system power when a "high AUX" S5 state is required. That would entail a state where the host is OFF, but the system requires more current than PSUs can provide on their AUX power

rail. It should be noted that the DC-SCM's maximum supported power level exceeds many PSU's AUX rail capabilities, and the system design would need to handle accordingly.

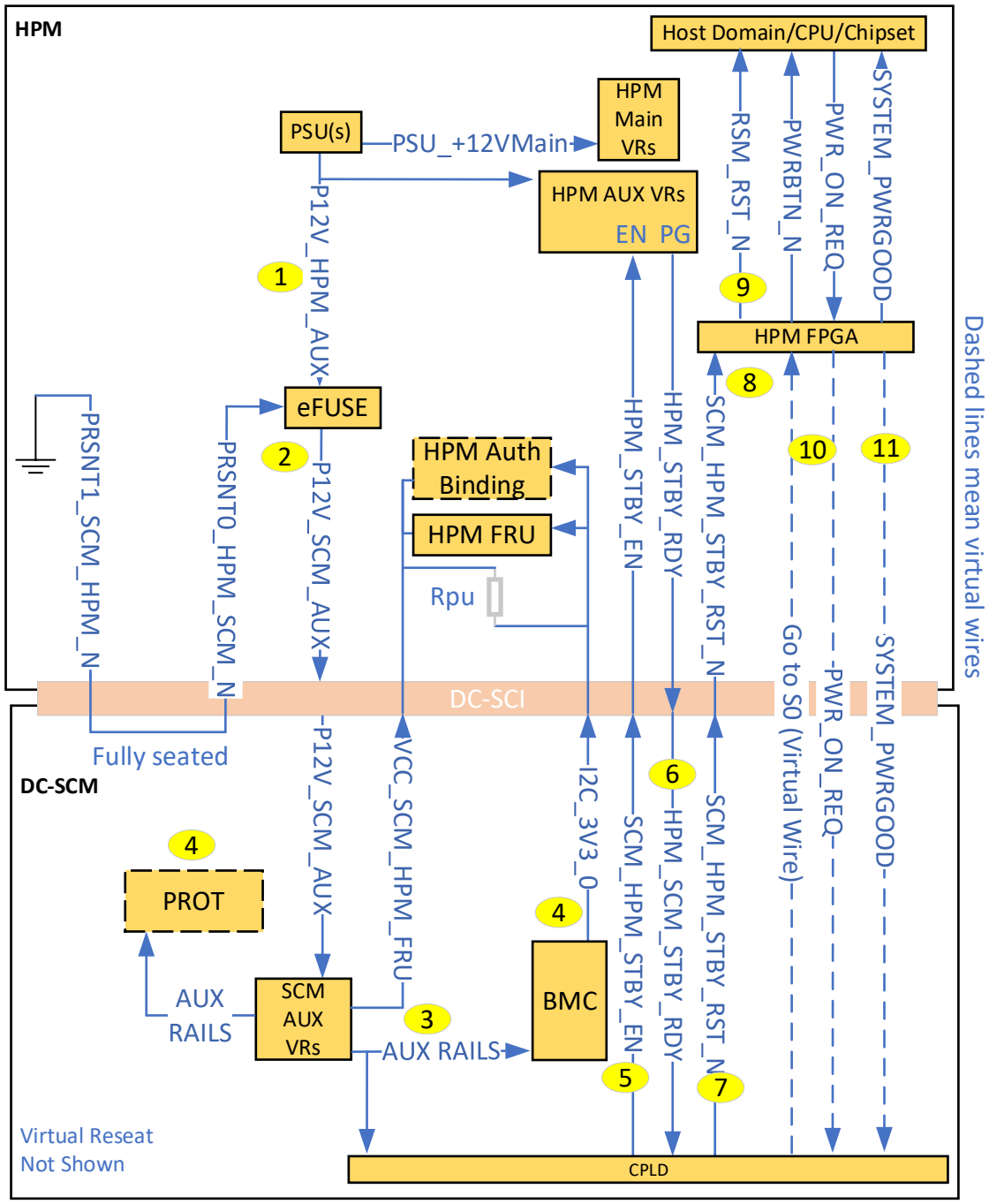


Figure 52: Discovery Sequence

4 Electrical specifications

The following sections provide specifications for the DC-SCM input voltage and current.

4.1 Input Voltage, Power, and Current

Table 12 lists the nominal, maximum, and minimum values for the DC-SCM input voltage. The maximum and minimum voltages include the effects of connector temperature, age, noise/ripple, and dynamic loading.

Table 12: Input Power Requirements

	Minimum	Nominal	Max
Input voltage	10.8 V DC	12.0 V DC	13.2 V DC
Input Power (S5)	n/a	n/a	47.52 W (10.8 V*1.1 A/pin*4 pins)
Inrush Rise Time	5 ms	n/a	200 ms
*Input Current	n/a	n/a	4.4 A (1.1 A/pin*4 pins)
*Input Power (belowS5)	n/a	n/a	15 W

*Input current is based on 1.1 A rating per pin, which is already derated.

*Input Power (STBY, Pre-S5): For DC-SCM/HPM compatibility, it is recommended to limit the max power at 15 Watts for all states lower than S5, this includes STBY and Pre-S5. This limit is not enforced if the HPM design is known to be capable of supporting the full DC-SCM power limit at these early states.

New to DC-SCI 2.0 is a power pin for **VCC_SCM_HPM_FRU** sourced from the DC-SCM to the HPM specifically for powering the HPM FRU and optional circuits such as an authentication IC. The current limit is set not due to pin current rating, but instead due to overall budget and reducing burden on the SCM VR while providing enough to aid in the discovery and any potential security functions.

VCC_SCM_HPM_FRU must be +3.3VAUX +- 5% and limited to 200 mA maximum current. Note that this is limited for overall budget reasons and not by the pin current limit.

Table 13: VCC_SCM_HPM_FRU Power Requirements

	Minimum	Nominal	Max
Input voltage	3.135 V DC (-5%)	3.3 VAUX DC (SCM sourced)	3.465 V DC (+5%)
Input Power	n/a	n/a	0.627 W (3.135 V*200 mA)
Input Current	n/a	n/a	200 mA

5 Routing Guidelines and Signal Integrity

5.1 NC-SI

The following section describes the timing requirements that need to be met while routing the NC-SI bus. It defines the portion of the overall propagation delay budget allocated to the HPM and to the DC-SCM, as well as additional requirements for each. HPM and DC-SCM implementers shall analyze their design to ensure the timing budget is not violated.

The traces shall be implemented as 50 Ohm ±15% impedance-controlled nets. HPM and DC-SCM designers are encouraged to follow the guidelines defined in the RMII and NC-SI specifications for physical routing. Figure 53 outlines the NC-SI clock and the data path timing delays on a typical design with the NC-SI bus routed to an OCP NIC 3.0.

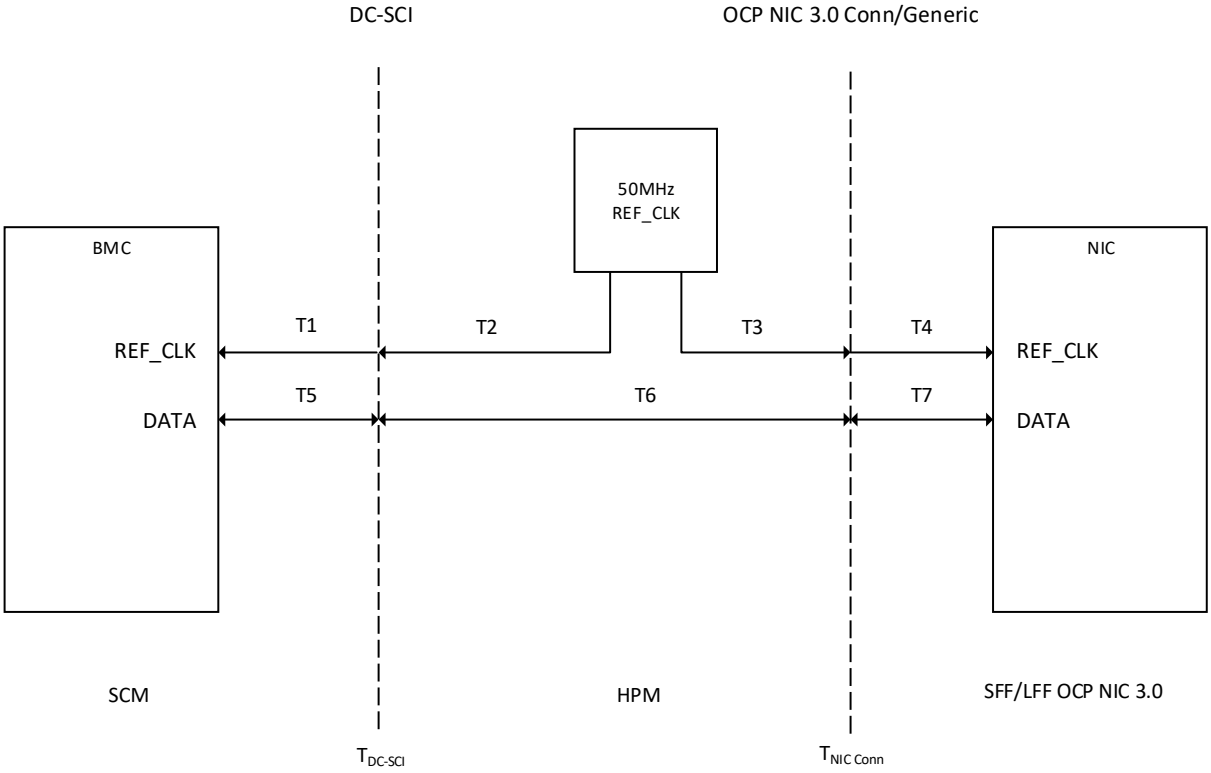


Figure 53: NC-SI Clock and Data Path Timing Delay Topology

Table 14 shows the various timing parameters derived from the NC-SI interface specification (DSP0222) and the OCP NIC 3.0 specification. The propagation delay on the DC-SCM PCB (T5) is assumed to be 680ps.

Table 14: NC-SI Timing Parameters

Parameter	Value	Description
T_{CLK}	20 ns	Period of 50MHz REF_CLK
$T_{CO[max]}$	12.5 ns	Max permissible clock-to-out value per DSP0222
$T_{SU[min]}$	3 ns	Min permissible single ended data setup to REF_CLK rising edge
$T_{SKEW[max]}$	1.5 ns	Max permissible REF_CLK skew between any two devices in the system
$T_{PD,Budget}$	3000 ps	Total propagation delay between BMC and the target ASIC
$T_{NIC,SFF}$(T7)	900 ps	Max permissible propagation delay for an SFF OCP NIC 3.0 card
$T_{NIC,LFF}$(T7)	1350 ps	Max permissible propagation delay for an LFF OCP NIC 3.0 card
T_{SCM} (T5)	680 ps	SCM propagation delay
$T_{DC\ SCI}$	110 ps	Typical propagation delay over the DC-SCI connector
$T_{NIC\ Conn\ Straddle}$	110 ps	Typical propagation delay over an OCP NIC 3.0 Straddle Connector
$T_{NIC\ Conn\ RA}$	130 ps	Typical propagation delay over an OCP NIC 3.0 Right Angle Connector

5.1.1 NC-SI Data Timing

Based on the values in Table 14 , the data timing budget from the BMC to the NIC ASIC is 3 ns as shown in the formula below. Note that the hold time is guaranteed by the RMII spec.

$$Timing\ Budget = T_{CLK} - T_{CO[max]} - T_{SU[min]} - T_{SKEW[max]}$$
$$= 20\ ns - 12.5\ ns - 3\ ns - 1.5\ ns = 3\ ns$$

This maximum allowable propagation delay on the data lines from the BMC to each NIC is shared across the DC-SCM (T5), HPM (T6), and the OCP NIC (T7) boards as shown Figure 53 . Considering the connector propagation delays, the following requirement shall be met for the total propagation delay:

$$T5 + T_{DC\ SCI} + T6 + T_{NIC\ Conn} + T7 < 3000\ ps$$

The Table 15 below calculates the typical data signal timing budget on an HPM (T6) using LFF and SFF OCP NIC 3.0 cards, based on values in Table 14.

Table 15: NC-SI Board Timing Budget

	Max SCM Delay (T5)	Max NIC Card Delay (T7)	Max HPM Delay ($T_{DC\text{-}SCI}$ + T6 + $T_{NIC\ Conn}$)
NIC-LFF	680 ps	1350 ps	970 ps
NIC-SFF	680 ps	900 ps	1420 ps

5.1.2 NC-SI Clock Timing

The maximum clock skew ($T_{SKEW[max]}$) between the reference clocks, as specified in DSP0222, is noted in Table 14. The critical delays are shown in Figure 53 as T1, T2, T3, and T4. The following equation summarizes the skew requirement.

$$|(T1 + T_{DC\ SCI} + T2) - (T3 + T_{NIC\ Conn} + T4)| \leq T_{SKEW[max]}$$

$$|(T1 + T_{DC\ SCI} + T2) - (T3 + T_{NIC\ Conn} + T4)| \leq 1500\ ps$$

5.2 I2C and I3C

For the I2C interfaces, HPM and DC-SCM designers shall follow the System Management Bus (SMBus) Specification, Version 3.0. Refer to this specification for DC characteristics and all AC timings.

For the I3C interfaces, HPM and DC-SCM designers shall not exceed the capabilities of the MIPI I3C Basic v1.1.1 specification. Refer to this specification for DC characteristics and all AC timings. The total capacitance of the I3C bus on the DC-SCM, including the BMC output pin capacitance, DC-SCM trace capacitance and DC-SCI pin capacitance should be less than 25pF to maximize the possible bus clock rate.

6 Platform Interoperability

The DC-SCM specification attempts to support maximum electrical and mechanical interoperability between all DC-SCMs and HPMs. However, it is expected and within the scope of this specification to not have this inter-operability “out-of-the-box” and to require different firmware sets (BMC firmware, DC-SCM CPLD and HPM FPGA firmware) to be loaded in the system to account for differences. The DC-SCM spec enables and requires these differences to be accounted for by firmware changes only. This referred to as the “Plug-and-Code Model” when the hardware layer interoperability exists.

In order to ensure that unused buses and signals are properly terminated on the HPM, Table 16 outlines the required and optional interfaces through the DC-SCI and the expected termination on HPM when unused in the system.

Table 16: Platform Interoperability

Interface Name	Required? (Y/N)	HPM termination if un-used
NC-SI	N	No
ESPI	N	Yes
I2C[0]	Y (HPM FRUID at 0xA0)	10K
I2C_3V3	N	10K
I2C_I3C_1V8	N	10K
I3C[0:1]	N	10K
SPI_HPMCNTRL	N	No
QSPI; QSPI_P1	N	No
SPI_SCMCNTRL	N	No
USBs	N	No
PCIe TX/RX	N	No
PCIe Clock	N	No
PECI_HPM_SCM	N	No
PECI_VREF_HPM_SCM	N	Connect to 1.0 V (S0)
UART[0:1]	N	No
JTAG	N	No
P3V0_HPM_SCM_BAT	N	No
STBY BOOT SEQUENCE SIGNALS	Y	NA
PRSNT[0:1]	Y	NA
All other Misc. signals	N	No

6.1 FRU Requirements

This table defines the requirement for a MultiRecord Area record on the HPM FRU. This record is for the DC-SCM to read to proceed with the appropriate actions, such as the updating the DC-SCM FPGA or BMC firmware.

Table 17: HPM FRU MultiRecord Definition

Offset	field length	field	Value	
0	1	Record Type ID	0xC1	
1	1	7:7 – End of list 6:4 – Reserved, write as 000b 3:0 – Record Format version		
2	1	Record Length		
3	1	Record Checksum (zero checksum)		
4	1	Header Checksum (zero checksum)		
5	3	Manufacture ID	0x7f	OCP INIA assigned ID 0x00A67F, (LSB first)
			0xA6	
			0x00	

8	1	OCP DC-SCM 2.0 FRU OEM Record Version	0x00 – Reserved 0x01 – OCP DC-SCM 2.0 card FRU record released with version 1.0	
9	2	DC-SCM Revision 15:8 - Major number 7:0 - Minor number	0x02 0x00	Revision 2.0
11	1	DC-SCM Version 7:4 - Major number 3:0 - Minor number	0x1 0x0	Version 1.0
12	2	LTPI Revision 15:8 - Major number 7:0 - Minor number	0x01 0x00	Revision 1.0
14	1	LTPI Version 7:4 - Major number 3:0 - Minor number	0x1 0x0	Version 1.0
15	1	DC-SCM Type	0x00 - not any defined type 0x01 - 0xFF Reserved	
16	16	Reserved	Reserved set to 0xFF	
31	32	OEM		Board ID, type, etc

7 Regulatory

7.1 Required Compliance

An OCP DC-SCM 2.0 card shall meet the following Environmental, EMC and safety requirements.

Note: Emissions and immunity tests in Section 7.1.4 are to be completed at the system level. The OCP DC-SCM 2.0 vendors should work with the system vendors to achieve the applicable requirements listed in this section.

7.1.1 Required Environmental Compliance

- **China RoHS Directive**
- **EU RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. The substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates
- **EU REACH Regulation (EC) No 1907/2006** addresses the production and use of chemical substances and their potential impact on human health and the environment.

- **EU Waste Electrical and Electronic Equipment ("WEEE")** Directive (2012/19/EU) – mandates the treatment, recovery and recycling of EEE
- **The Persistent Organic Pollutants Regulation (EC) No. 850/2004** bans production, placing on the market and use of certain persistent organic pollutants
- **The California Safe Drinking Water and Toxic Enforcement Act of 1986 ("Proposition 65")** sets forth a list of regulated chemicals that require warnings in the State of California
- **The Packaging and Packaging Waste Directive 94/62/EC** limits certain hazardous substances in the packaging materials
- **Batteries Directive 2006/66/EC** regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances

7.1.2 Required EMC Compliance

Radiated and Conducted Emissions requirements are based on deployed geographical locations. Refer to Table 18: for details.

Table 18: FCC Class A Radiated & Conducted Emissions Requirements Based on Geographical Location

Targeted Geography	Applicable Specifications
USA	FCC, 47 CFR Part 15, Class A digital device (USA)
Canada	ICES-003, class A (CAN)
EU	EN 55032: 2015+AC:2016 Class A Radiated and Conducted Emissions requirements for European Union EN 55035: 2017 Immunity requirements for the European Union (EU) EN 55024: 2010+A1:2015 Immunity requirements for European Union (EU) may alternatively be reported. Note: EN55024 is scheduled to be superseded by EN55035. OCP DC-SCM 2.0 implementors are encouraged to test to EN55035 to avoid recertifying their product when EN55024 is withdrawn
Australia/New Zealand	AS/NZS CISPR 32:2015 Class A CISPR 32:2015 for Radiated and Conducted Emissions requirements
Japan	VCCI 32-1 Class A Radiated and Conducted Emissions requirements
Korea	KN32 – Radiated and Conducted Emissions KN35- Immunity
Taiwan	BSMI CNS13438: 2006 (complete) Class A Radiated and Conducted Emissions requirements

- **CE** – Equipment must pass the CE specification
- All technical requirements covered under **EMC Directive (2014/30/EU)**

7.1.3 Required Product Safety Compliance

- Safety – requirements are listed in Table 19.

Table 19: Safety Requirements

Targeted Category	Applicable Specifications
Safety	UL 62368-1 and CAN/CSA C22.2 No. 62368-1-14, 3rd Edition. Audio/video, information, and communication technology equipment Part 1: Safety requirements, dated 2019/12/13

7.1.4 Required Immunity (ESD) Compliance

The OCP DC-SCM 2.0 card shall meet or exceed the following ESD immunity requirements listed in Table 20:

Table 20: Immunity (ESD) Requirements

Targeted Category	Applicable Specifications
Immunity (ESD)	EN 55035 2017, and IEC 61000-4-2 2008 for ESD. EN 55024 may alternatively be reported. Required ±4 kV contact discharge and ±8 kV air discharge Note: EN55024 is scheduled to be superseded by EN55035. OCP DC-SCM 2.0 implementors are encouraged to test to EN55035 to avoid recertifying their product when EN55024 is withdrawn
NEBS Level 3 (optional)	Optionally test devices to NEBS Level 3 – Required ±8 kV contact discharge and ±15 kV air discharge with interruptions not greater than 2 seconds. The device shall self-recover without operator intervention Note: NEBS compliance is part of the system level testing. The OCP DC-SCM 2.0 specification is providing a baseline minimum recommendation for ESD immunity

7.2 Recommended Compliance

All OCP DC-SCM 2.0 cards are required to meet the requirements specified in Section 7.1. Card vendors should also consider meeting the requirements below:

7.2.1 Recommended Environmental Compliance

- **Halogen Free**: IEC 61249-2-21 Definition of halogen free: 900 ppm for Bromine or Chlorine, or 1500 ppm combined total halogens
- **Arsenic**: 1000 ppm (or 0.1% by weight)
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act** requires companies using tin, tantalum, tungsten, and gold (“3TG”) in their products to verify and disclose the mineral source. While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntarily reporting of this information

7.2.2 Recommended EMC Compliance

- FCC, 47 CFR Part 15, Subpart B Class A digital device (USA) with 10 dB margin. Refer to the baseline requirements shown in Section 7.1.2 for details.

8 Acronyms

For the purposes of the DC-SCM specification, the following acronyms apply:

Acronym	Definition
ASIC	Application Specific Integrated Circuit
BMC	Baseboard Management Controller
CBB	Compliance Base Board
CFM	Cubic Feet per Minute
DC-SCM	Data Center Secure Control Module
DC-SCI	Data Center Secure Control Interface
DRAM	Dynamic Random Access Memory
EDSFF	Enterprise and Datacenter SSD Form Factor
EMI	Electro Magnetic Interference
ESPI	Enhanced Serial Peripheral Interface
FRU	Field Replaceable Unit
I/O	Input / Output
HFF	Horizontal Form Factor
HPM	Host Processor Module
I2C	Inter-Integrated Circuit - two wire serial protocol
I3C	MIPI Alliance Improved Inter-Integrated Circuit – two wire serial protocol
LED	Light Emitting Diode
LFF	Large Form Factor
LFM	Linear Feet per Minute
LPC	Low Pin Count bus
LTPI	LVDS Tunneling Protocol and Interface
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
NC	No Connect
NC-SI	Network Controller Sideband Interface
NIC	Network Interface Card
OCP	Open Compute Project
SCM	Secure and Control Module
SRIS	Separate Reference Clocks with Independent Spread-Spectrum Clocking
SRNS	Separate Reference Clocks with No Spread-Spectrum Clocking
VFF	Vertical Form Factor