



OPEN

Compute Project

NEBIUS 20U Server, AMD EPYC™ 4th Gen server processors
Model name NB-D-SR-O2ASP5

Base Specification
version 1.0.1
December 2024

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1. License

1.1. OPTION B: Open Web Foundation (OWF) CLA

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Usage of this Specification is governed by the terms and conditions set forth in **Modified OWFa1.0 Final Specification Agreement (FSA) (As of August 16, 2021) (“Specification License”)**.

- 1) The above license does not apply to the Appendix or Appendices. The information in the Appendix or Appendices is for reference only and non-normative in nature.

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2. Compliance with OCP Tenets

This contribution shares openly key design selections and technical characteristics of the Nebius 2OU Scalable Server AMD EPYC™ 4th Gen server processors. This way it enables other users to benefit from design effort used for this server design.

2.1. Openness

Nebius 2OU Scalable Server specification describes a design which can be used to support many configuration types. It can be leveraged by other OCP partners as a standalone server, or as a ORV2/ORV3 solutions.

2.2. Efficiency

The Nebius 2OU Scalable Server is designed to achieve high power and thermal efficiency, as well as flexibility in server configuration for various purposes. It enables optimal Total Cost of Ownership (TCO) outcomes for modern data centers.

2.3. Impact

The Nebius 2OU Scalable Server sets a new standard for data center design within OCP principals. Its contributions will drive the evolution of designs tailored to meet the requirements of new adopters, enabling a cycle of innovation and further contributions.

2.4. Scale

Nebius 2OU Scalable Server is designed for data center deployment and operations. The system is designed with different optional modules, ease of serviceability, and reliability as a focus. The front side tool-less serviceability design provides fast production assembly and easy maintenance in operation.

2.5. Sustainability

Nebius 2OU Scalable server power and thermal design lead to reduced overall energy consumption.

3. Change Log

Date	Version #	Author	Description
December, 5 2024	1.0.0	Igor Znamenskiy	Initial release
December, 10 2024	1.0.1	Igor Znamenskiy	Document formation

4. Scope

Nebius 2OU Scalable Server featured with 4th generation AMD EPYC™ scalable CPU. This document highlights the main technical specifications of this server.

Nebius 2OU Scalable server includes the following functional modules, which can be installed in various configurations.

- 4x U.2/U.3 NVMe® x4 PCIe Gen5
- 4x 2.5"/3.5" SATA-3
- 2x FLFH x16 PCIe Gen5
- 1x HHHL x16 PCIe Gen5
- 1x OCP3 x16 PCIe Gen5
- 2x M.2 (80-110 mm) x4 PCIe Gen5

5. Overview

The Nebius 2OU Scalable server is the multifunctional server for the modern data centers. The server is designed with main OCP ideas, principals and specifications.

In addition, Nebius 2OU Scalable server introduces a flexible SKU design to meet various data center demand, functional modules design provides additional options for easy storage expansion or add on FLFH GPU cards for ML/AI computing demand.

The new CPU and several other improvements bring significant benefits in running various real time applications. Designed system cooling in this 2OU server enables simultaneous use of higher TDP CPUs and other accelerator cards. Information is listed below.

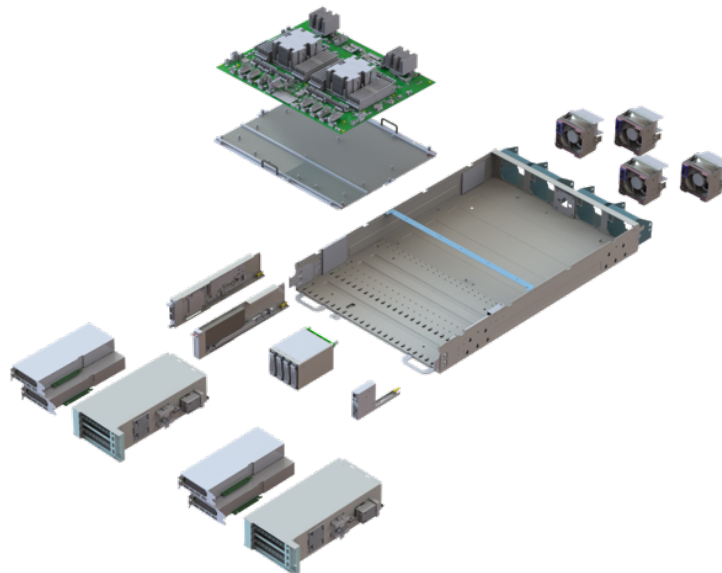


Figure 1. Nebius 2OU Scalable Server, main components overview

Server configurations listed below show the examples function modules combinations. Front side of the server has 24 unified mounting holes for the tool-less function modules installation.

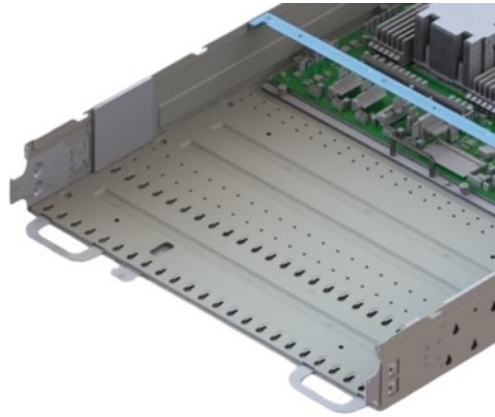


Figure 2. Mounting holes for modules installation

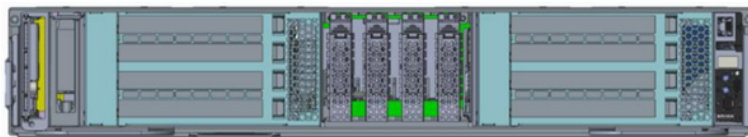


Figure 3. 4x FLFH PCIe cards, 4x 2.5" NVMe, OCP3 NIC, HHHL PCIe card

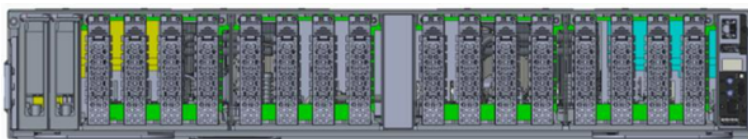


Figure 4. 16x 2.5" NVMe, 2x HHHL PCIe cards

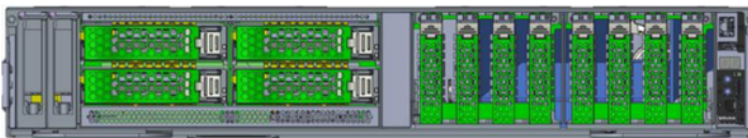


Figure 5. 4x 3.5" SATA, 8x 2.5" NVMe, 2x HHHL PCIe cards

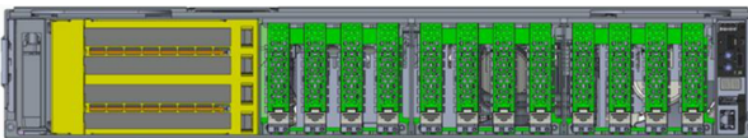


Figure 5. 2x FLFH PCIe cards, 12x 2.5" NVMe, OCP3 NIC

6. Specification

The Nebius 20U Scalable Server features the below server main board. It supports AMD EPYC™ 4th Gen server processors and provides 9x unified MCIO x16 PCIe gen5 connectors for various configurations of the function modules.

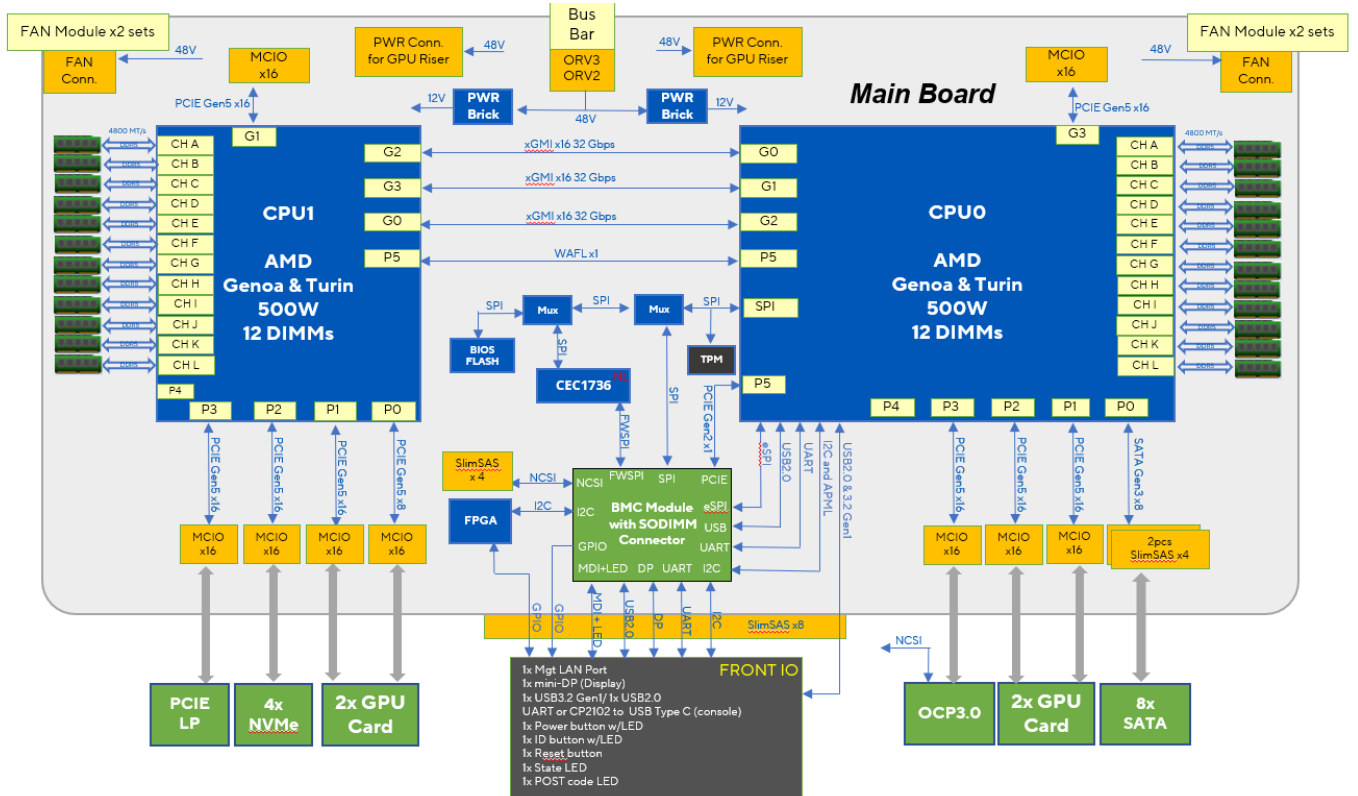


Figure 6. Main board function block diagram

Model Name		Nebius 20U Scalable Server
Motherboard		NB-E-MB-ASP5C5
Processor Support		2 x Socket SP5 AMD EPYC™
Chipset		System on Chip (SoC)
Memory	Total Slots	24
	Capacity	Maximum up to 3072GB
	Memory Type	DDR5 4800/4400
	Memory Size	128GB, 96GB, 64GB, 32GB, 16GB RDIMM
Expansion Slots	Total PCI/PCI-X/ PCI-E/PIKE Slots	9x MCIO PCIe Gen5 slots
	Slot Type	OCP Riser module, x16 Gen5 HHHL Riser module, x16 Gen5 FHFL Riser module, 2x x16 Gen5
	M.2	2x M.2 x4 PCIe Gen5 kit
	Micro SD Card Slot	-
	Proprietary Slot 1	-
	Proprietary Slot 2	-
Disk Controller	SATA Controller	AMD SoC controller, up to 8x SATA drives
	SAS Controller	Optional RAID/HBA card
Storage Bays	Storage Bay	up to 8x 3.5" SATA drives up to 4 x 3.5" Hot-Swap Bays per SATA module up to 16x 2.5" U.2/U.3 NVMe drives up to 4 x 3.5" Hot-Swap Bays per NVMe module
	Onboard storage	-
Networking		1 x Management Port Optional NIC Adapters on function modules (OCP3, HHHL, FHFL) Up to 400Gb/s Ethernet / InfiniBand per adapter
Display		Aspeed AST2600
Graphic		Up to 4x FHFL GPU
Front I/O Ports		1 x USB 3.2 Gen1 port 1 x USB 2.0 port 1 x UART port 1 x MiniDP 1 x RJ-45 MGMT LAN port
Rear I/O Ports		-
Switch/LED		Front Switch/LED: 1 x Power Switch (w/ LED) 1 x Reset Switch 1 x UID Switch (w/ LED) 1 x Post Indicator 1 x Status LED 1 x BMC Heartbeat LED

Security Options	Optional TPM-SPI
OS Support	Windows Server RedHat® Enterprise Linux Ubuntu
Dimension	885.4mm x 537mm x 94.7mm (2OU) 34.86" x 21.15" x 3.73"
Net Weight kg	33.01kg (CPU, DRAM & HDD included)
Gross Weight kg	43.65kg (CPU, DRAM, HDD and packing included)
Power Supply (following different configuration by region)	ORV2/ORV3 compatible
Environment	Operating temperature: 5° ~ 40° Non operating temperature: -40° ~ 60° Non operating humidity: 20% ~ 90% (Non condensing)

7. Mechanical specification

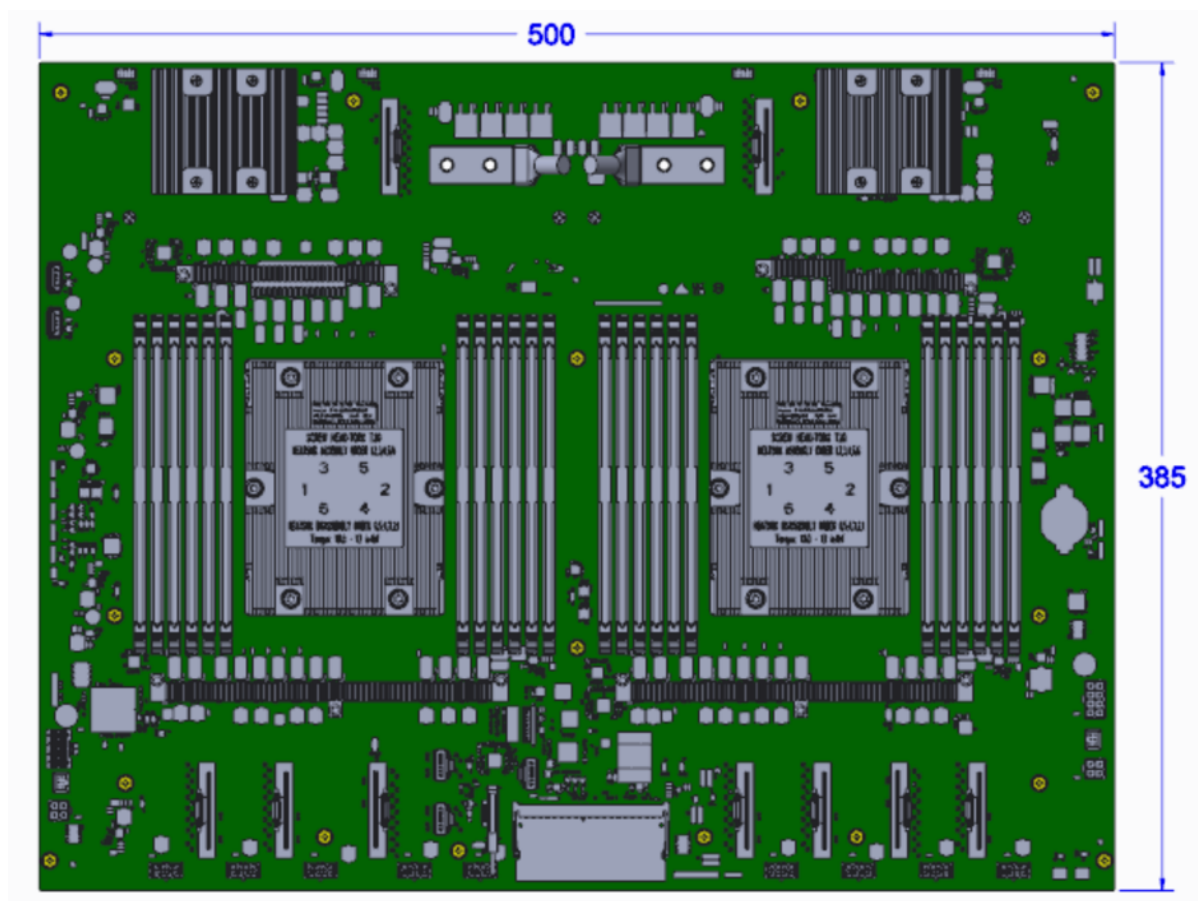


Figure 7. Main board

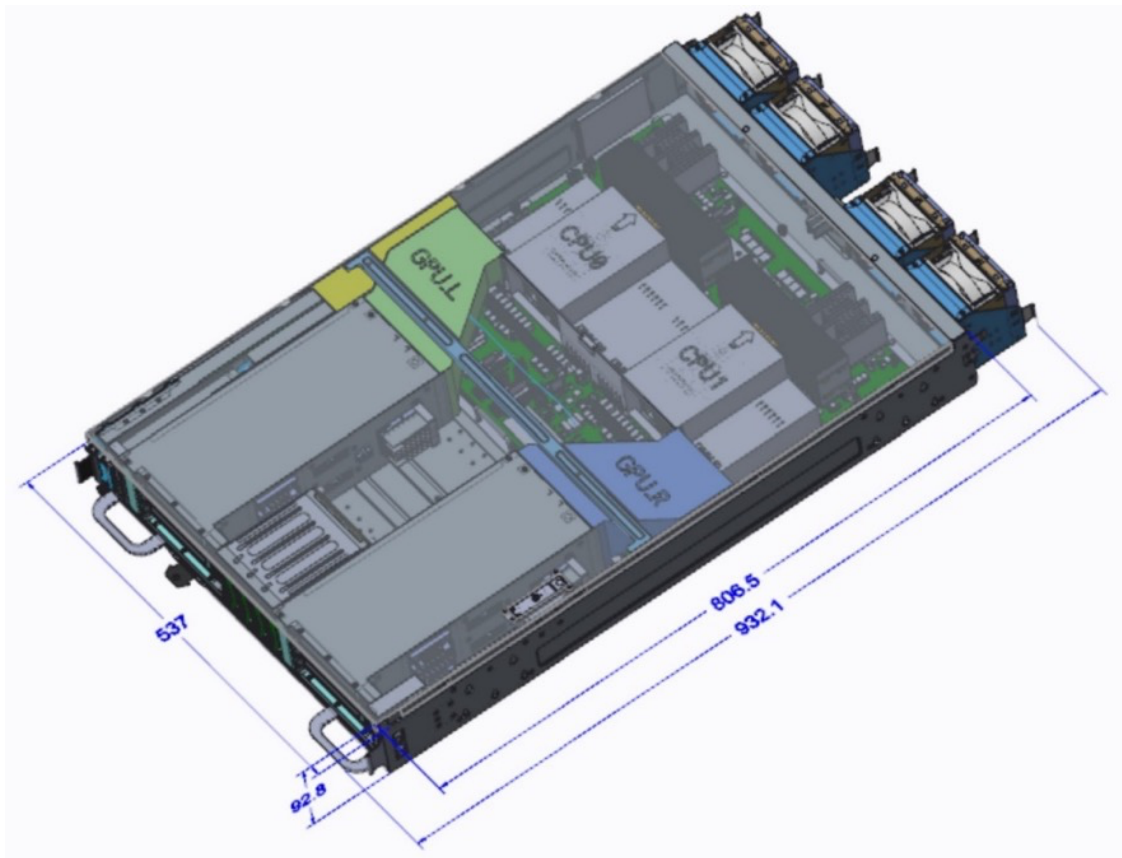
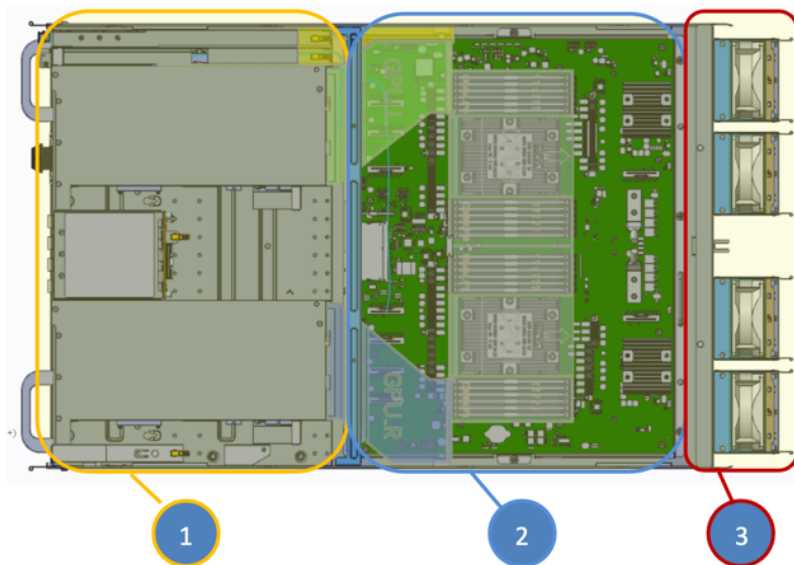


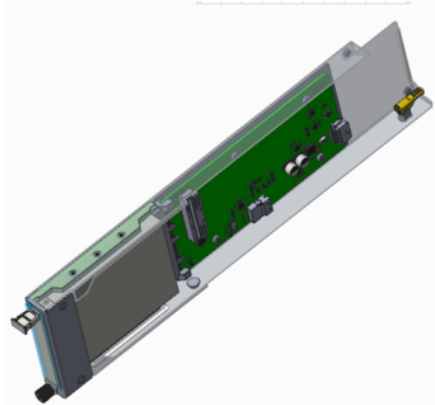
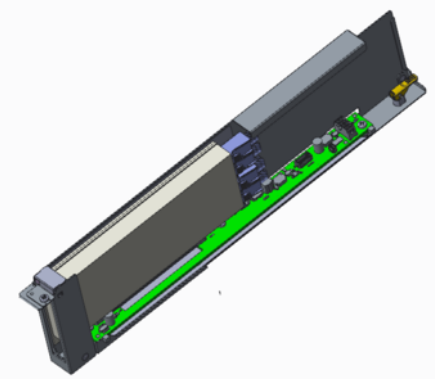
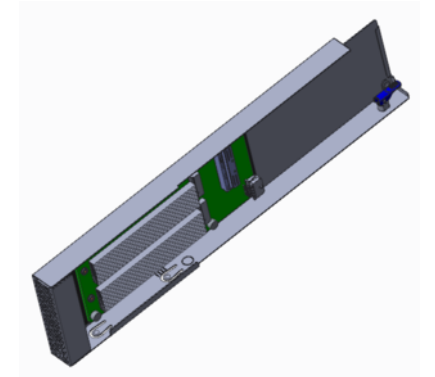
Figure 8. 20U chassis

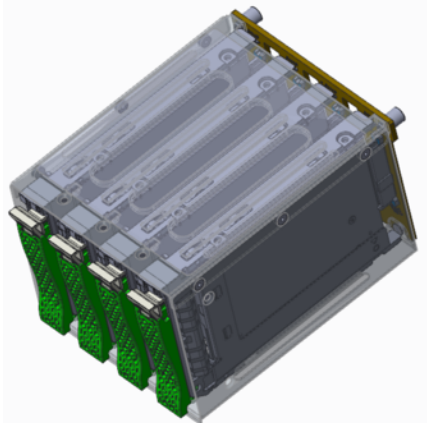
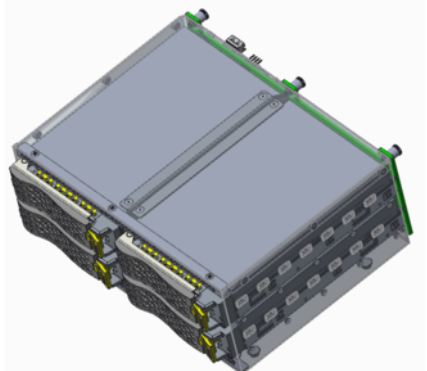
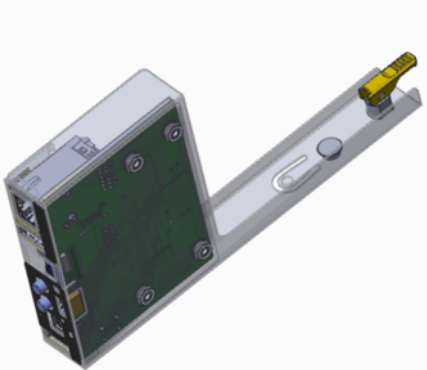


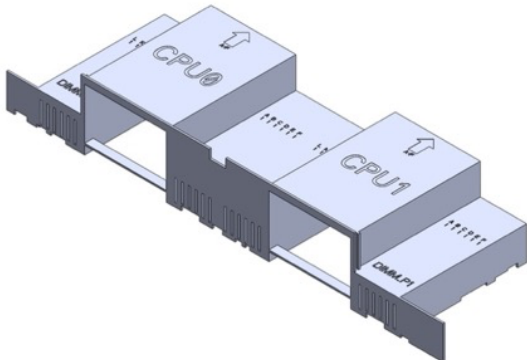
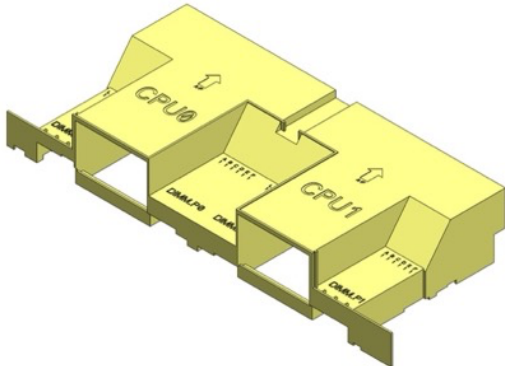
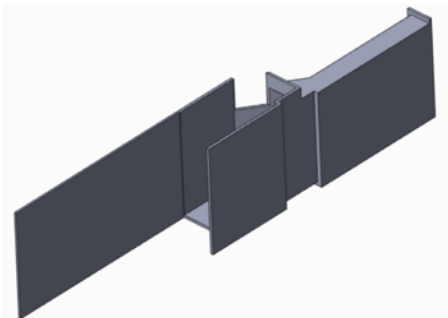
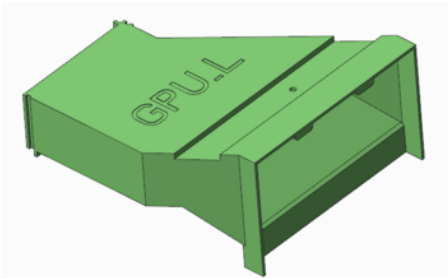
Item	Description
1	Function modules Area
2	Main Board Area
3	Fan module Area

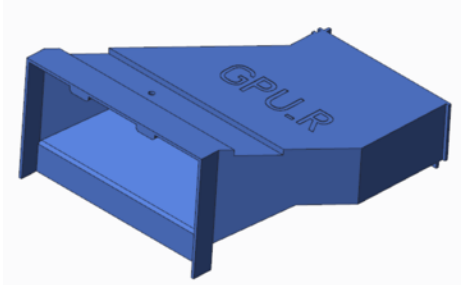
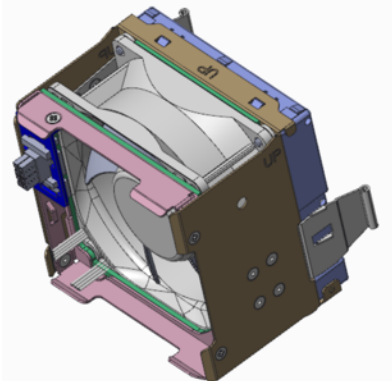
Figure 9. Server zones

Function modules and server parts

	OCP3 riser module x16 MCIO connection SFF with Pull Tab
	HHL riser module x16 MCIO connection
	M.2 module x16 MCIO connection

	FHFL module 2x x16 MCIO connection 2x DC-DC convertors 48-12V ¼ power brick
	NVMe module x16 MCIO connection 4x U.2/U.3 x4 slots
	SATA module Slimline x4 connection 4x 2.5"/3.5" SATA-3 slots
	Front IO module

	350W TDP CPU air duct
	500W TPD CPU air duct (for EVAC HS)
	HHHL and OCP3 riser air duct
	FLFH module air duct (Left)

	FLFH module air duct (Right)
	9238 H/S Fan module

8. Electrical Requirements

This system supports ORV2/ORV3 bus bar from +48V to +54V and baseboard has connector of three types, nine 3 mm pitch 2x4P connectors, two 4.2 mm pitch 2x4P connectors and two 3.4 mm pitch 2x2P connectors, to supply power for function modules. These connectors and their supply voltage are shown below.

The pin definition of 3 mm pitch connector is shown below. It supplies power for all finction modules, except FHFL module. There are two colors on the board. The black connector supplies 12V payload power. The white connector supplies 12V auxiliary power for OCP accessed under S5 mode.

Pin number	Description	Pin number	Description
1	3.3V auxiliary power	5	12V payload power
2	Ground	6	12V payload power
3	Ground	7	12V payload power
4	Ground	8	12V payload power

The pin definition of 4.2 mm pitch connector is shown below. It mainly supplies power for FHFL module. This 54V is from bus bar via hot swap controller LM5066.

Pin number	Description	Pin number	Description
1	3.3V auxiliary power	5	54V
2	Ground	6	54V
3	Ground	7	54V
4	Ground	8	54V

The 2x2P connectors of 3 mm pitch is reserved for future use, and its pin definition is shown below.

Pin number	Description	Pin number	Description
1	Ground	3	3.3V payload power
2	Ground	4	3.3V payload power

9. Thermal Design specification

The air consumption of the Nebius 20U Scalable Server depends on the configuration and is shown in the table below. The server's thermal design allows it to operate at an inlet temperature of up to +40 °C.

Configuration	25 °C inlet temperature	40 °C inlet temperature
4x 400W GPU	314 m3/h (185 CFM)	535 m3/h (315 CFM)
4x 20W NVMe U.2	4x FANS at 808 RPM	4x FANS at 11200 RPM
2x 350W CPU	54% PWM	85% PWM
16x 20W NVMe U.2	300 m3/h (175 CFM)	345 m3/h (203 CFM)
2x 350W CPU	4x FANS at 7080 RPM	4x FANS at 9200 RPM
	PWM 46%	PWM 63%

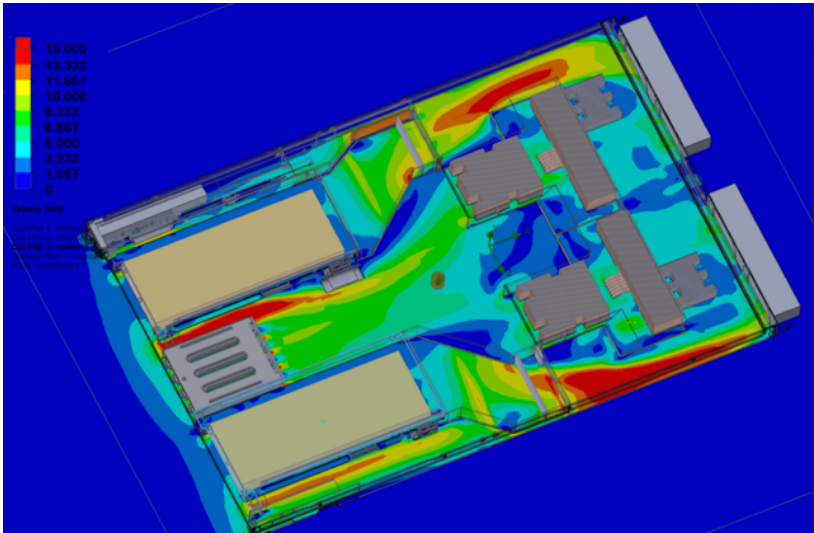
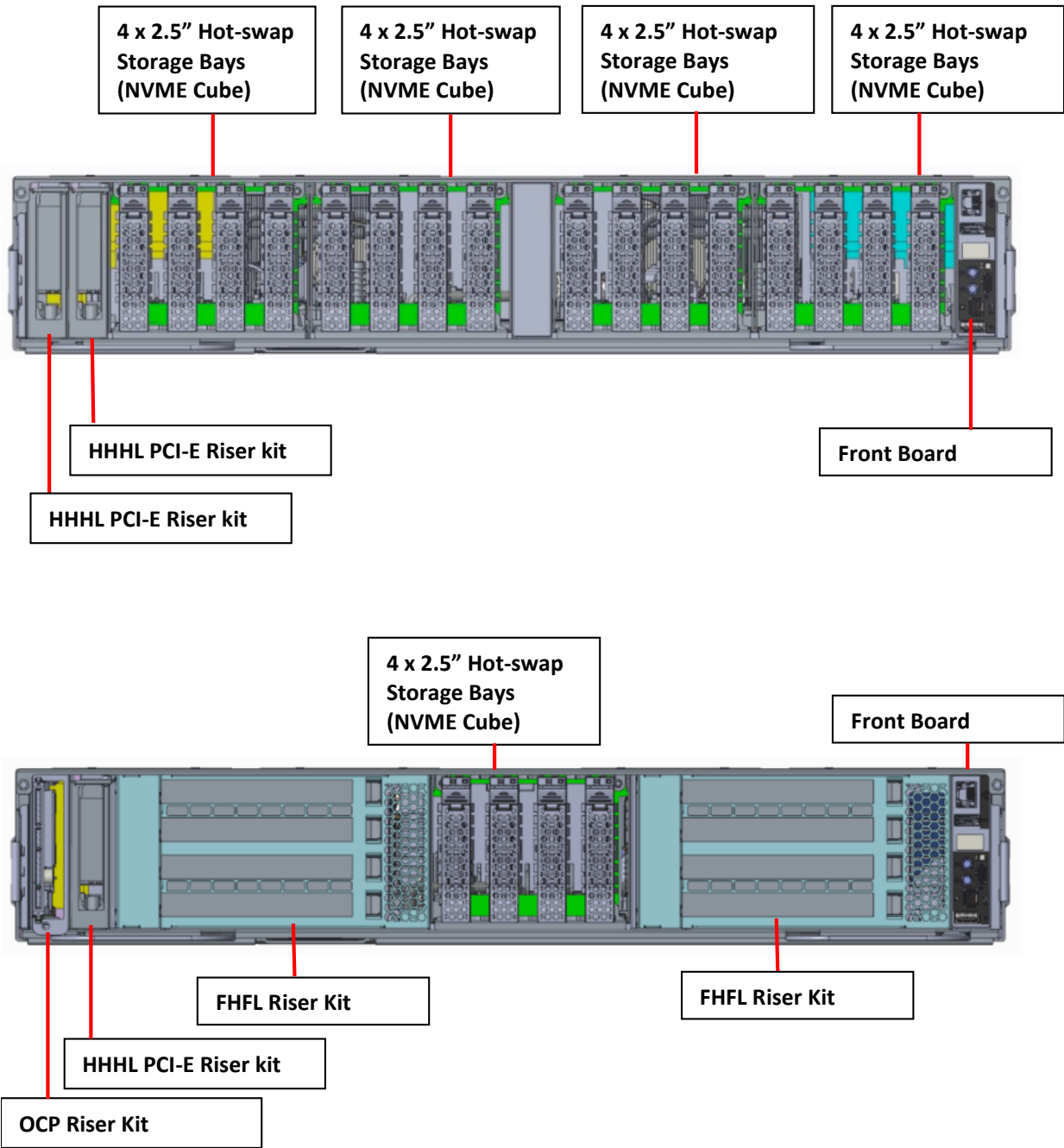


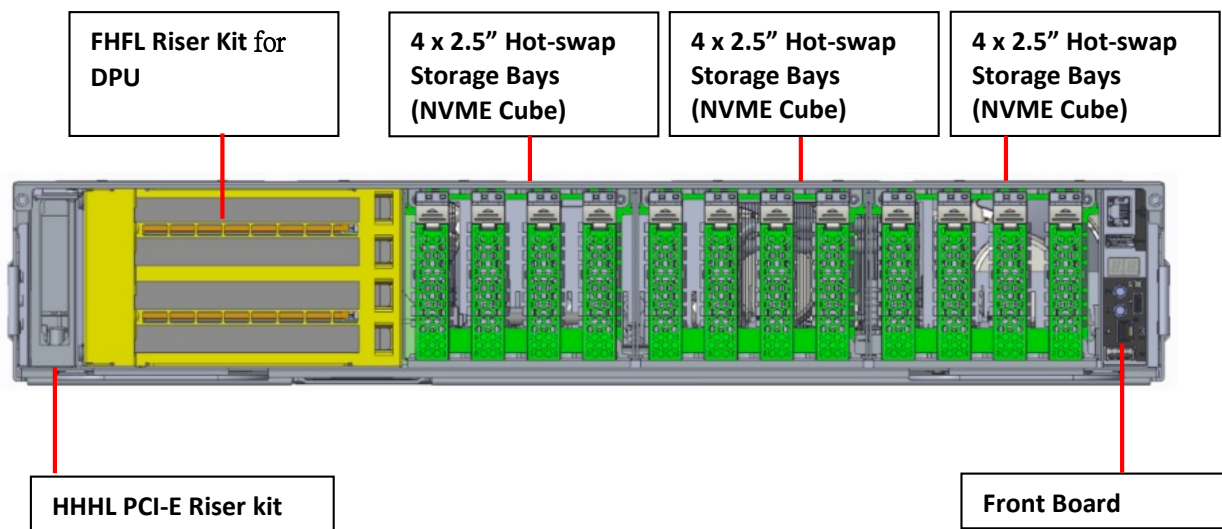
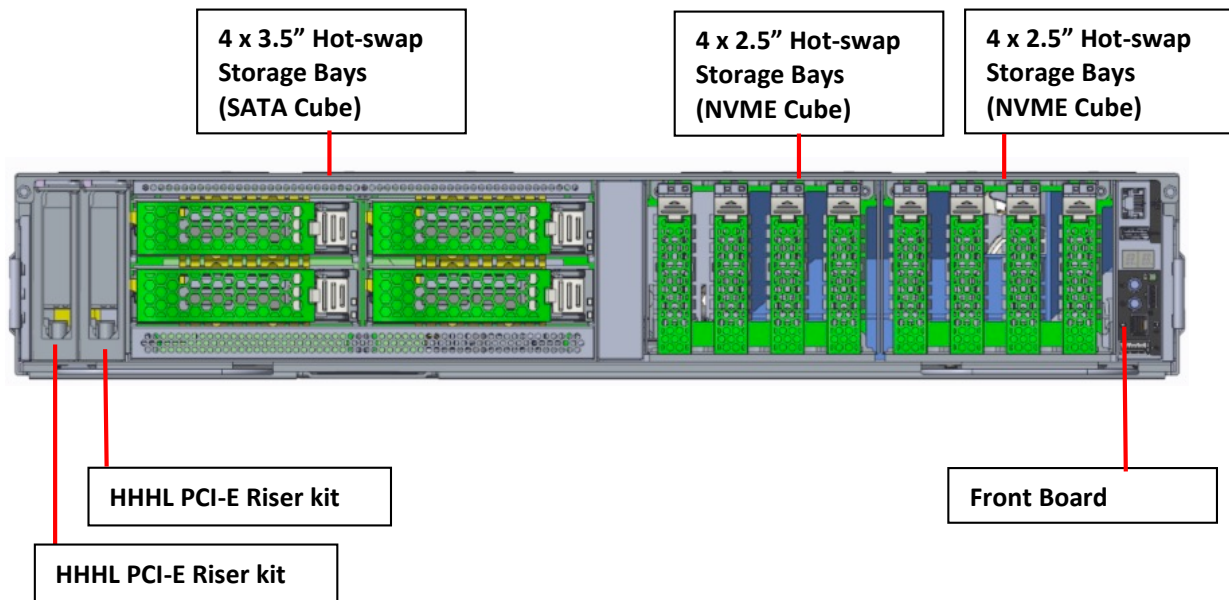
Figure 10. Server CFD

Item	Description
System FAN	• (4pcs) 9238, MAX 15400/149000 RPM fan • Support N+1 redundancy
CPU Heat-sink	• Standard Heatsink for 350 W TDP CPU • EVAC Heatsink for 500 W TDP CPU
Airduct	• GPU airduct • CPU airducts for 350W and 500W TDP CPU • Riser airduct for HHHL and OCP

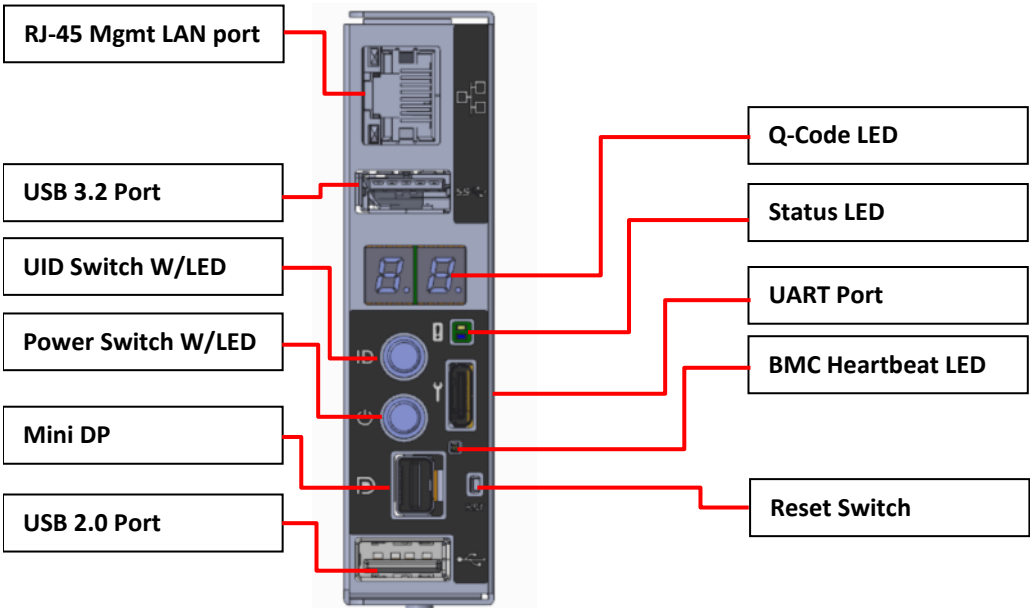
10. Interfaces

The main input-output ports and the front line function modules description are shown below on the main server configurations.

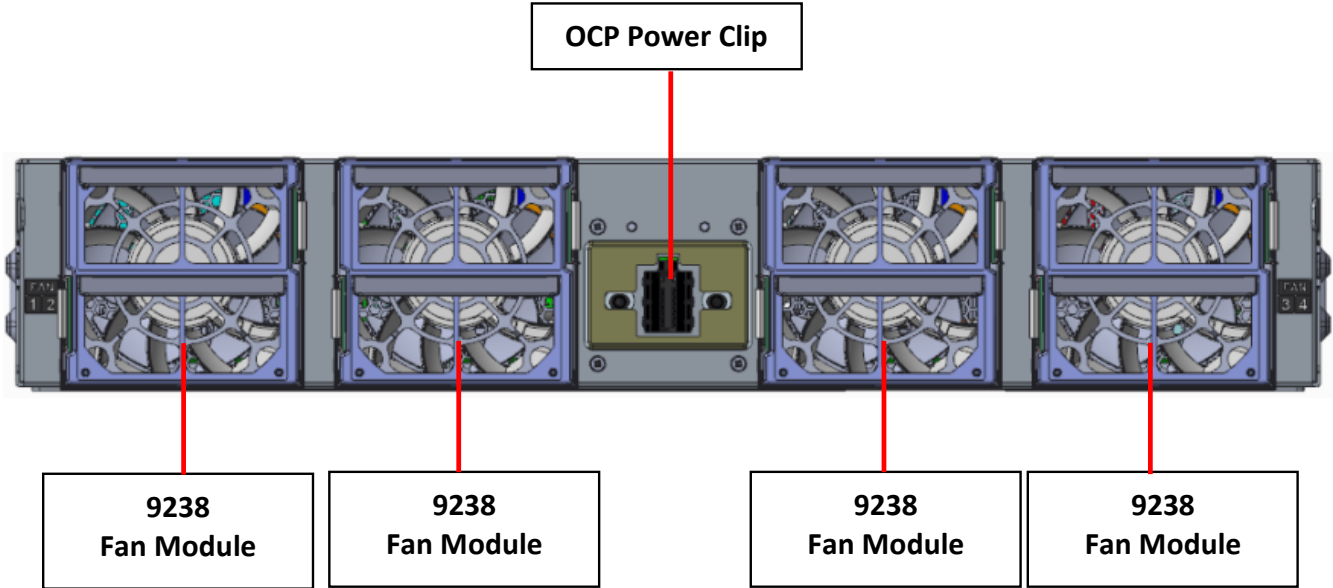




Front Board Features



System Rear View



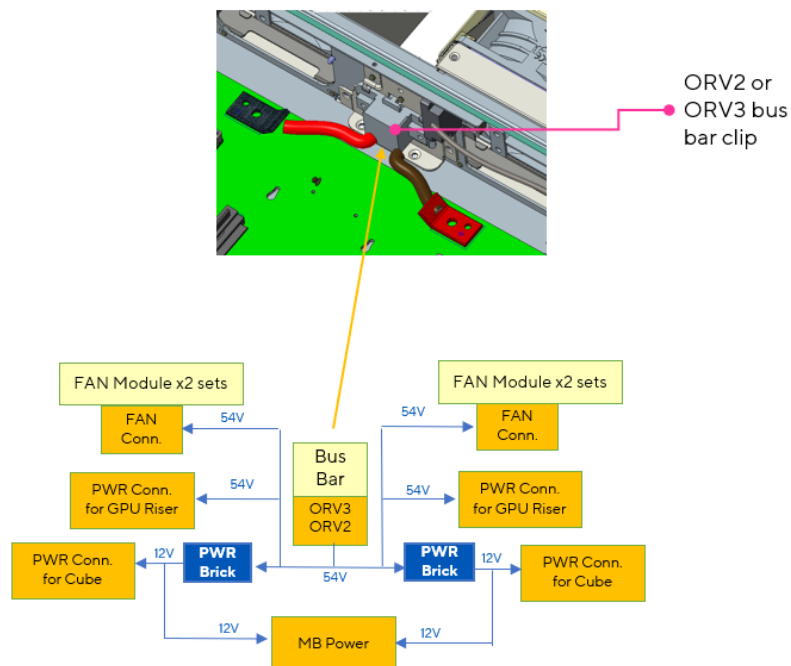
Signal List

The system support below high-speed signal interface.

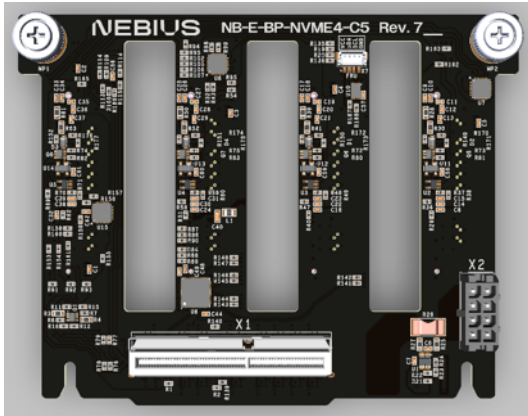
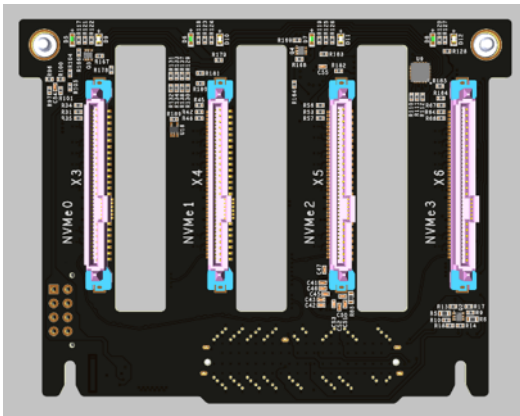
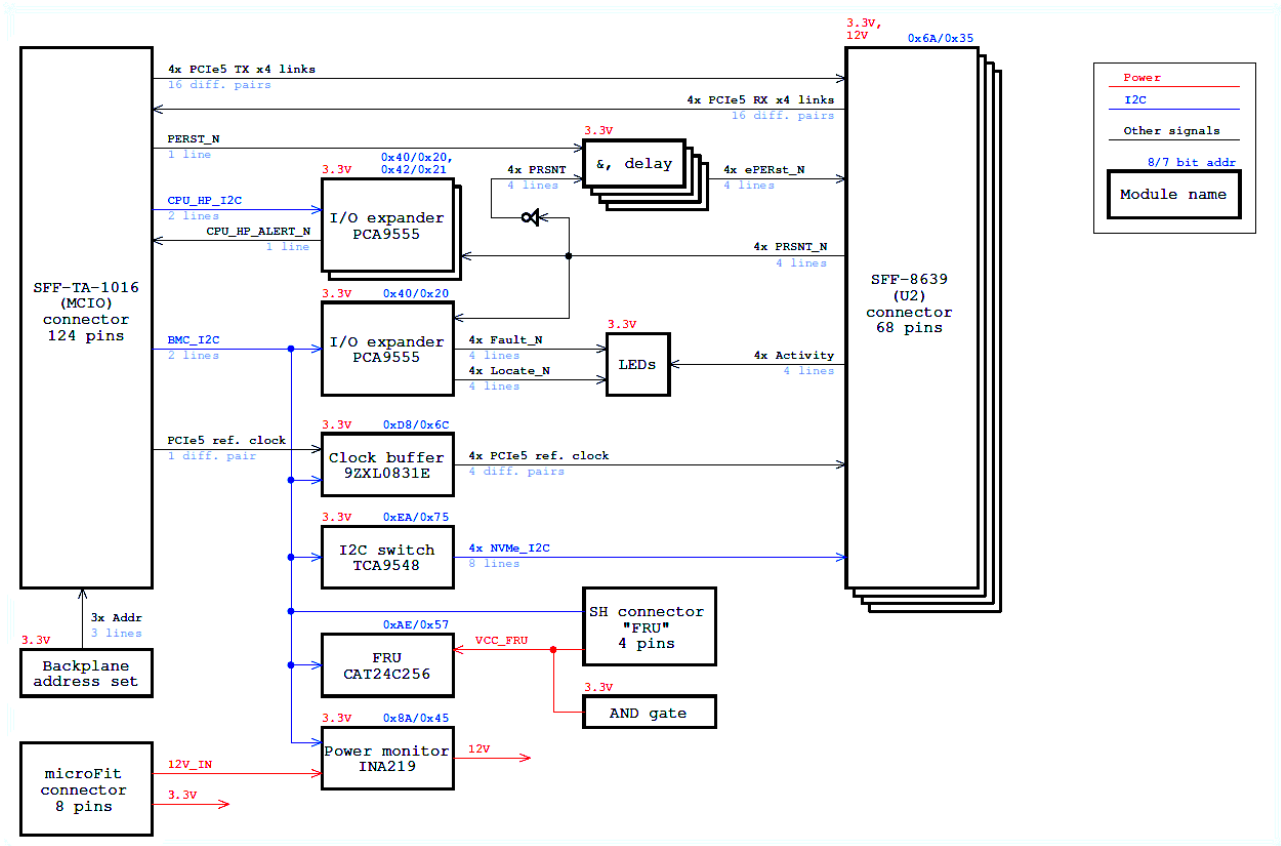
1. Memory: 24 DIMM slots for DDR5 with ECC. DDR5 speed can reach up to 4800 MT/s, and the total DDR5 capacity is up to total 3 TB.
2. PCIE slot: Support 9 MCIO x16 connectors of PCIE for module using in MB
HHHL module supports one PCIE Gen5 x16, PCIE HHHL slot
OCP3 module supports one PCIE Gen5 x16, OCP3 slot
FHFL module supports two PCIE Gen5 x16, PCIE FHFL slots
NVMe module supports four PCIE Gen5 x4, NVMe U.2 slots
3. Storage: Support 2 Slimline x4 connectors of SATA for module using in MB
SATA module supports four SATA Gen3, 3.5" HDD
4. LAN: One 1000BASE-T RJ45 in server front panel.
5. Display: One mini display port 1.1a output
6. USB: One USB3.2 Gen1 Type-A port and one USB2.0 Type-A port.
7. UART: One USB Type-C console port

Rear Side Power, I/O, Expansion Board and Midplane Subsystems

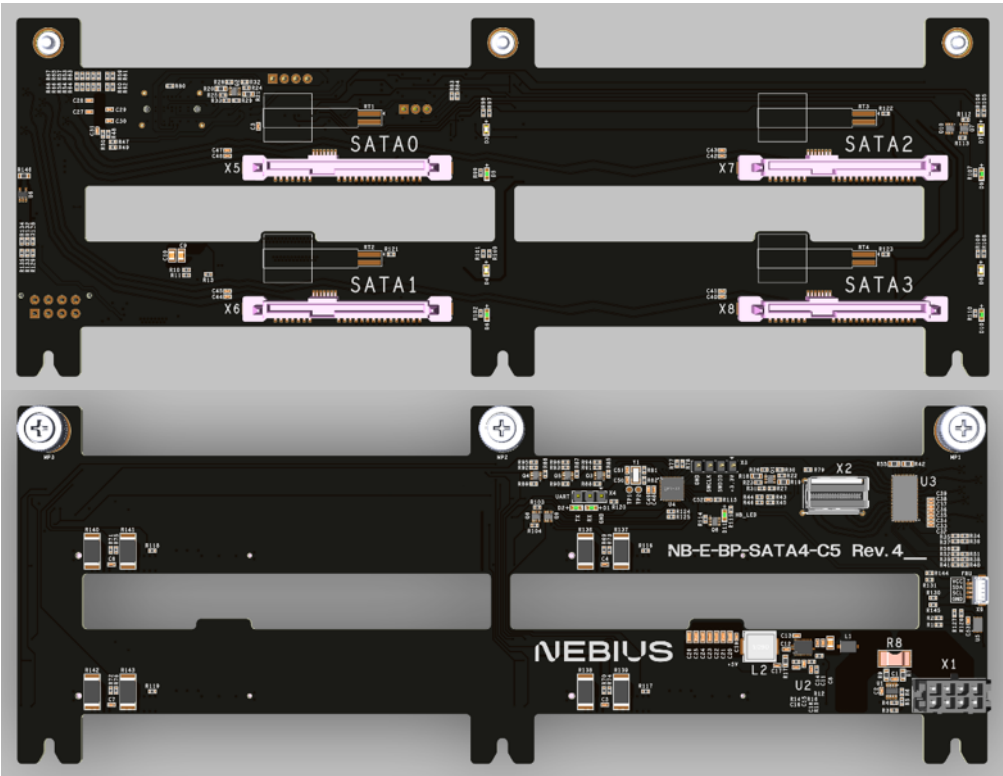
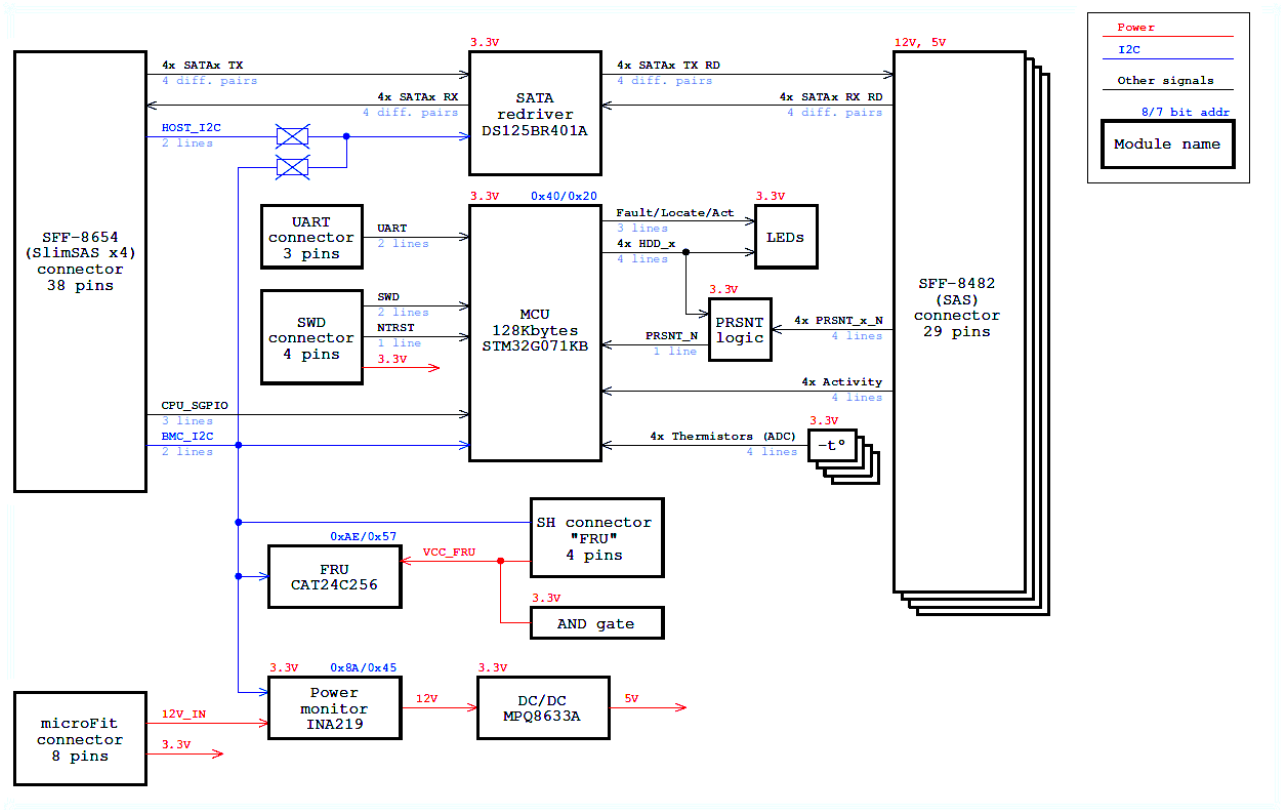
Rear Side Power, I/O, Expansion Board and Midplane Subsystems



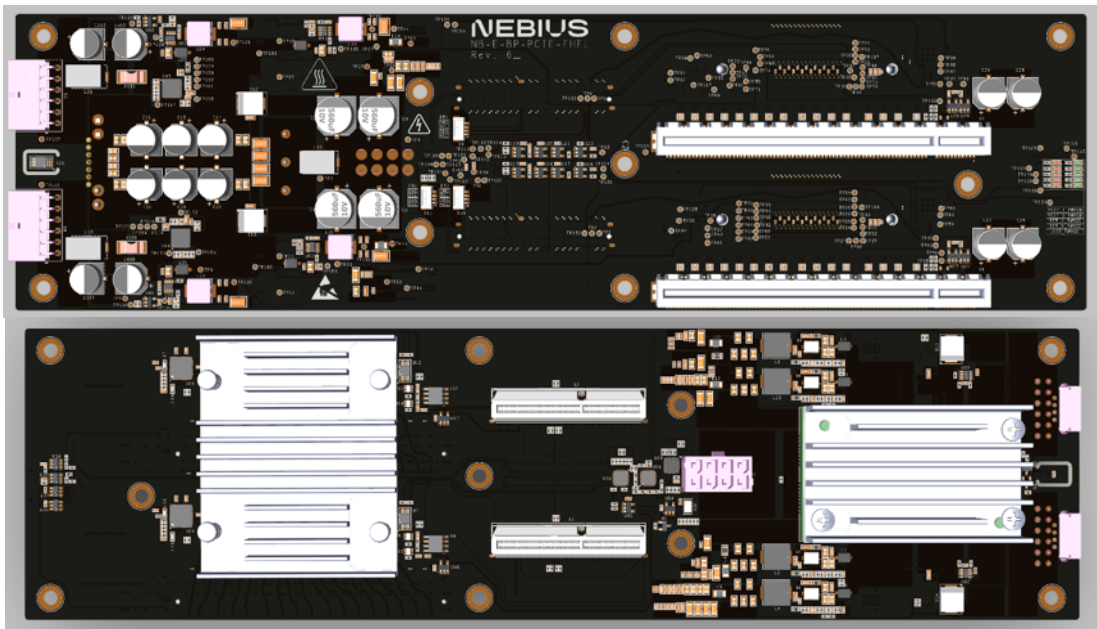
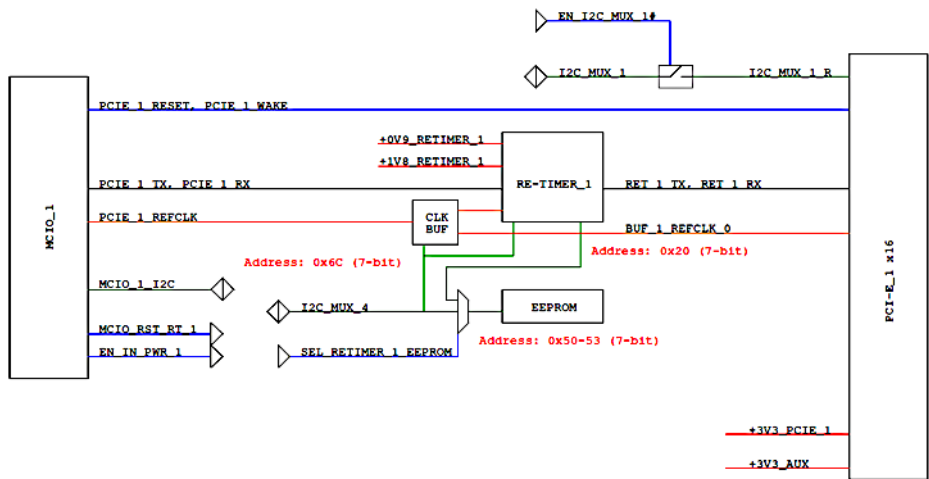
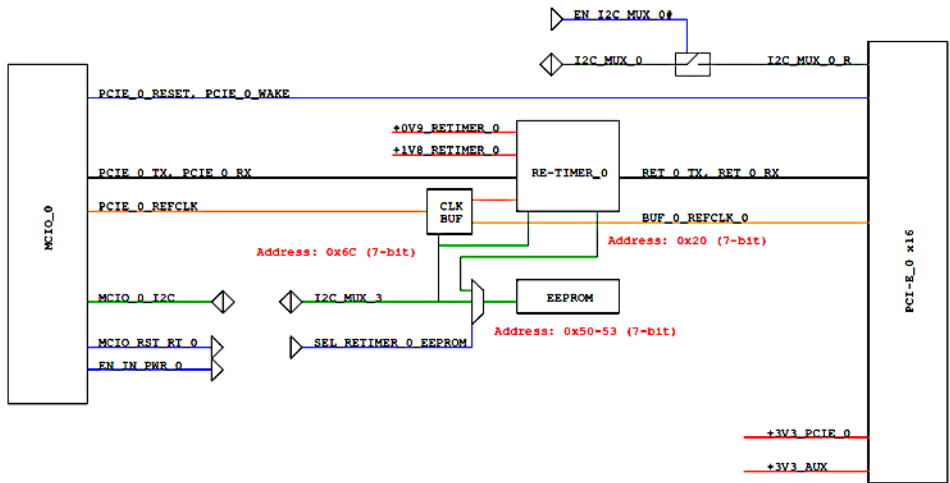
NVMe Backplane



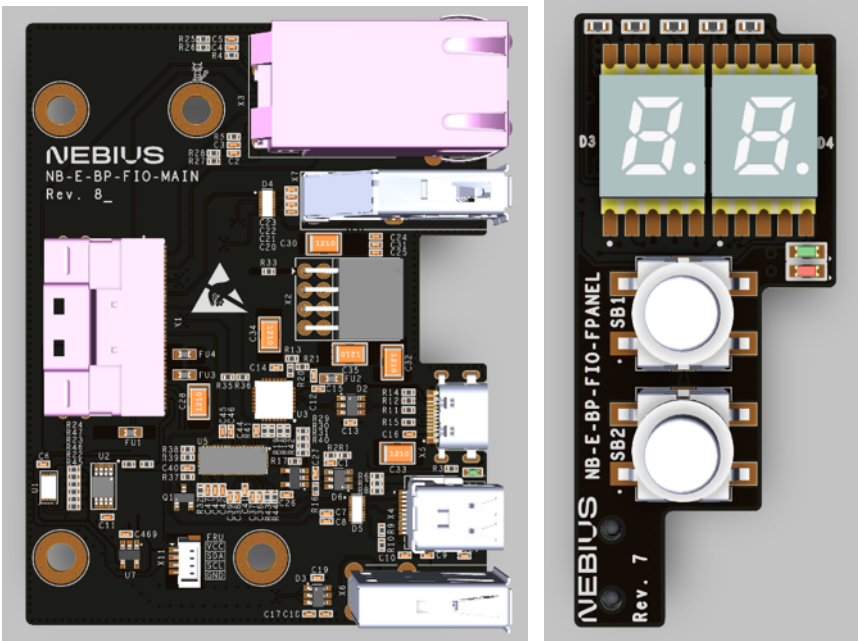
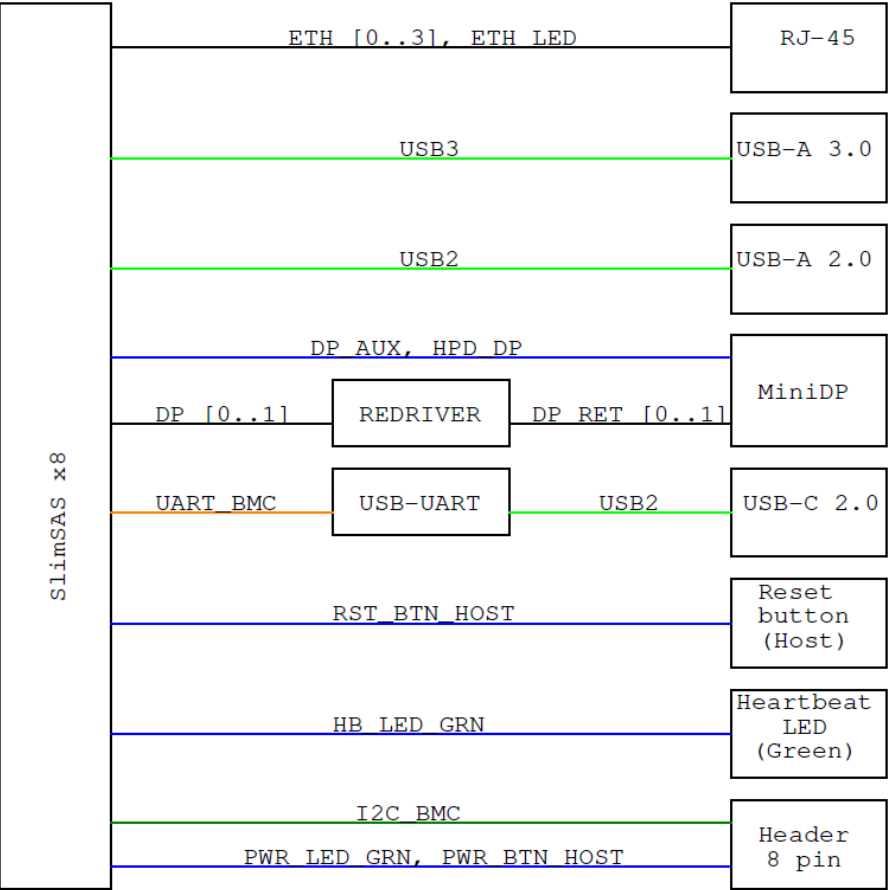
SATA Backplane



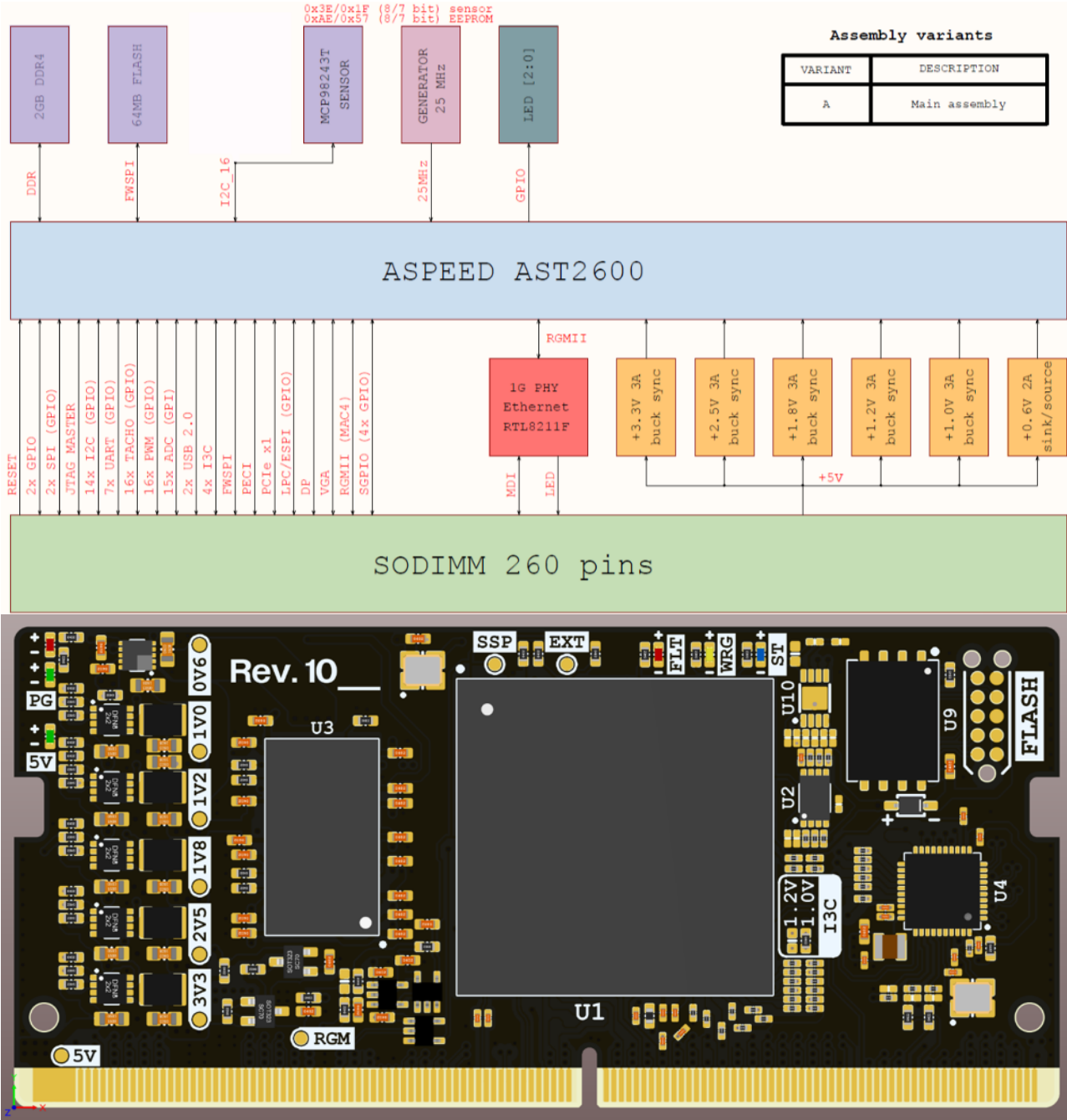
FHFL Riser Card



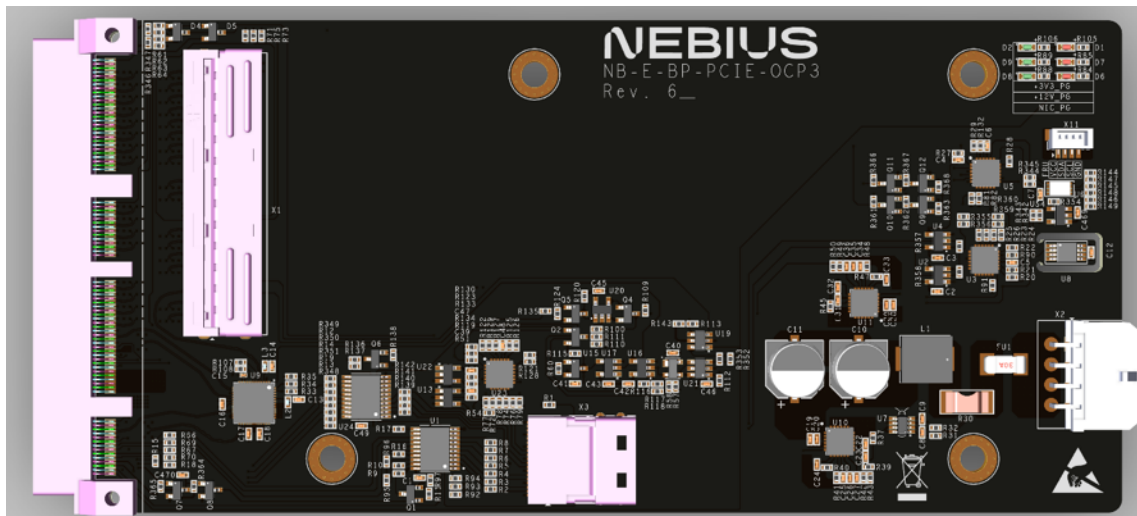
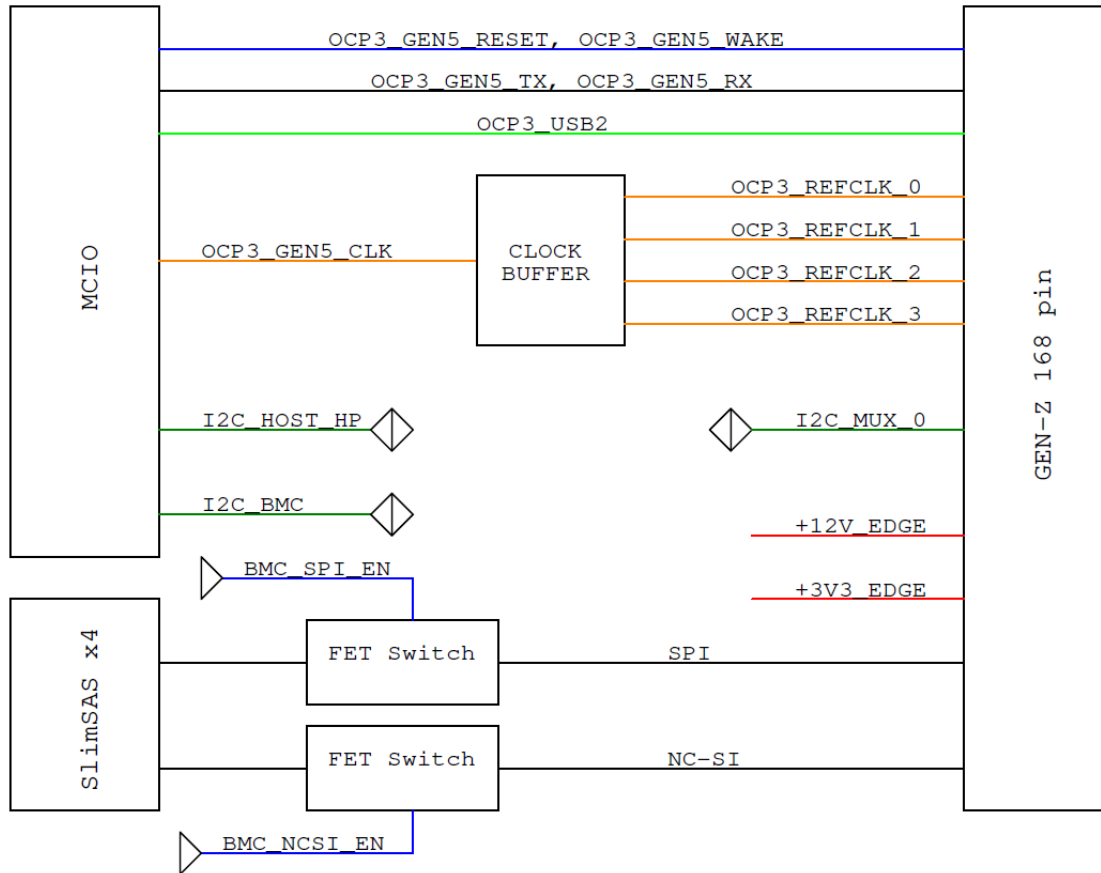
FIO Module



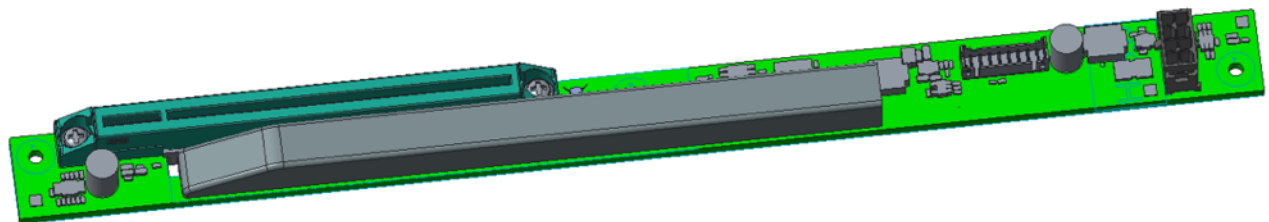
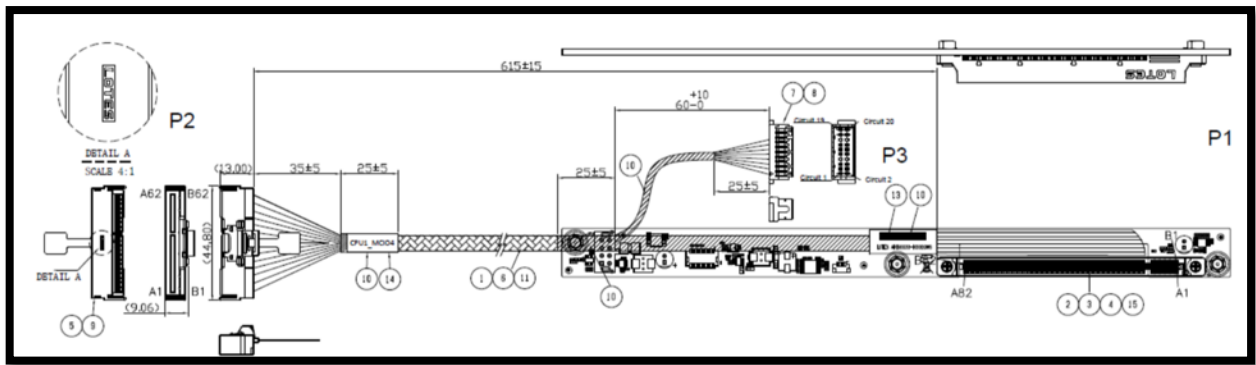
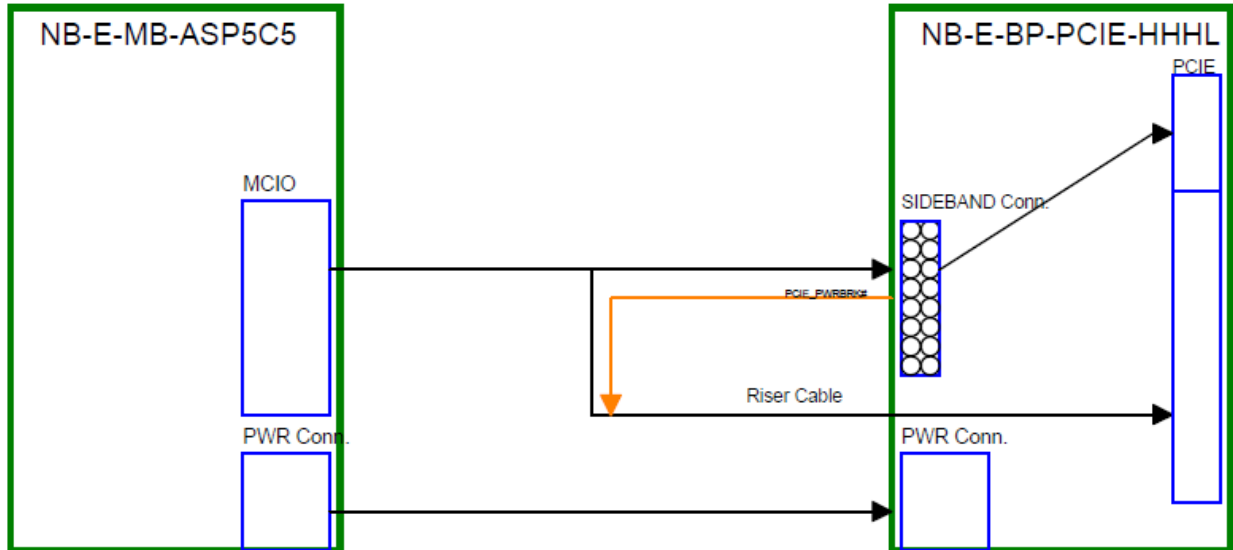
BMC Module



OCP3.0 Adapter Card



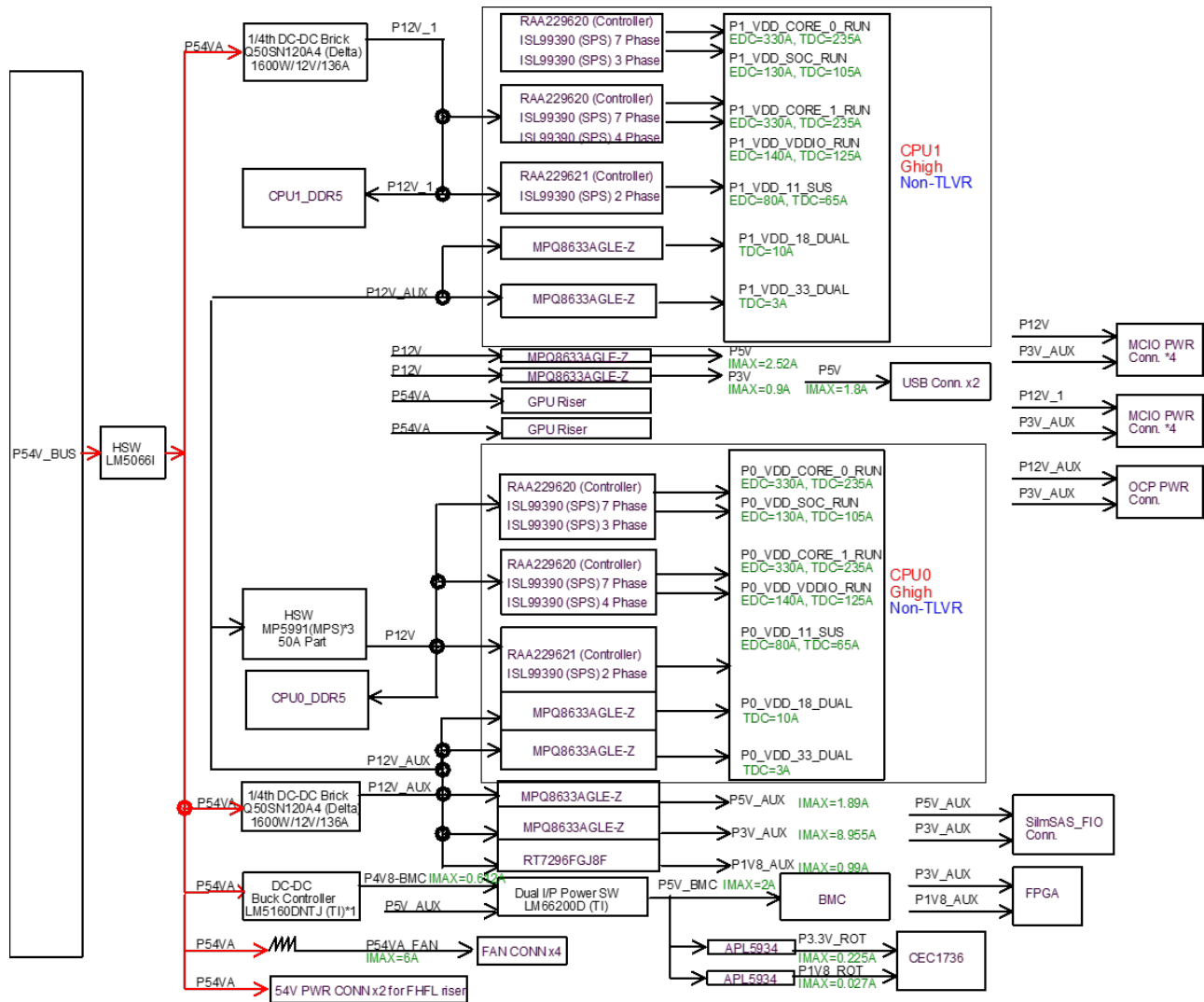
HHHL Riser Card



11. Onboard Power System

The Nebius 20U Scalable server includes a hot swap controller that manages the over current protect feature's limit at 72A for 20U system, refer to below Power tree:

Power Tree



12. Prescribed Materials

Nebius 2OU Scalable server designs with max CPU TDP of 500W.

13. System Firmware

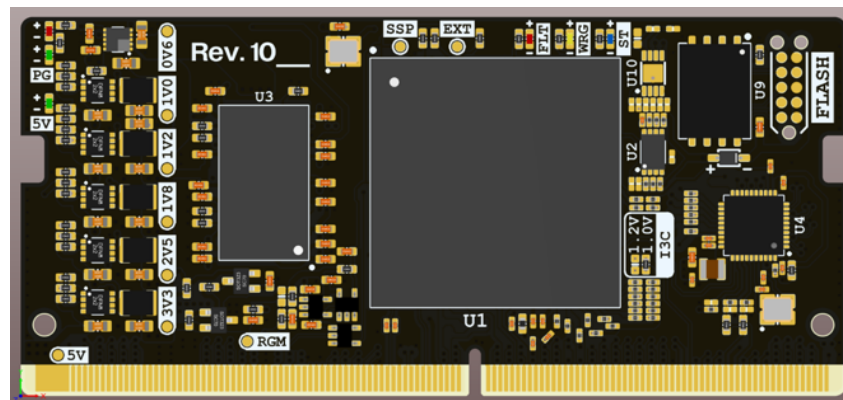
Nebius 2OU Scalable server is an OCP V2 48-54V and OCP V3 48-54V rack server powered by 4th Generation AMD EPYC™ processors. AMD Zen4 architecture is the most energy-efficient solution for data center and cloud node. It provides more scalability to handle all possible purpose. The system firmware BIOS is AML code base and follow below standards to design.

- Unified Extensible Firmware Interface Specification Version 2.8
- UEFI Platform Initialization Specification Version 1.7
- Intelligent Platform Management Interface Specification
- Advanced Configuration and Power Interface Specification Version 6.5
- PCI Express® 5.0 Specification
- TCG Storage Security Subsystem Class: Opal Specification Version 2.01
- NVMe Express® Base Specification 2.0
- System Management BIOS Reference Specification Version 3.5.0
- TPM Main Specification Level 2 Version 1.2 Rev 116
- TCG EFI Protocol and Platform Specification Version 1.22

BIOS update is also available via remote operation in BMC web.

14. Hardware Management

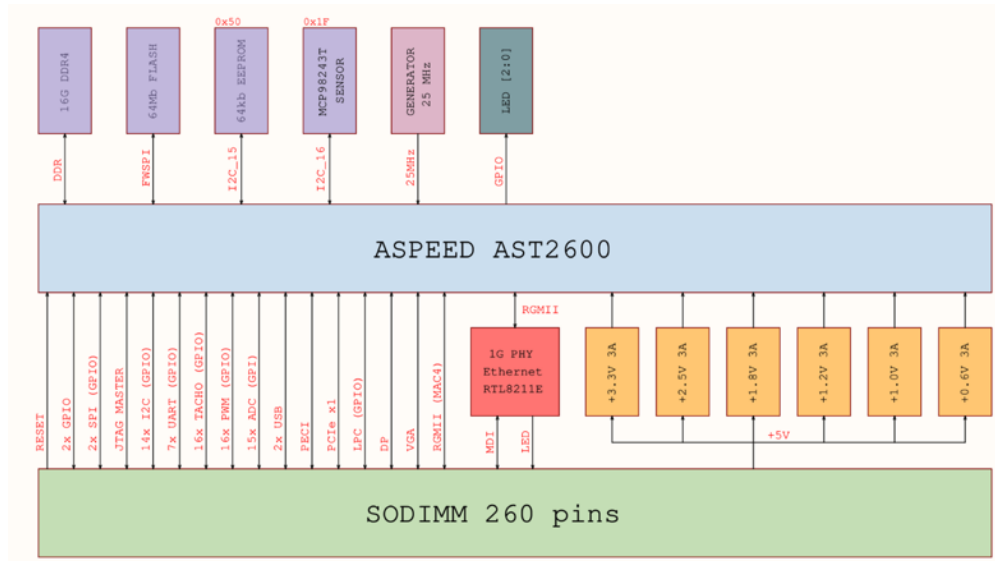
The Baseboard Management Controller BMC is implemented as a separated daughter board (SOM – System on module) with ASPEED AST2600 SoC, DDR4 memory, BMC SPI flash with BMC software and data, EEPROM for FRU data storage, ethernet PHY chip and power circuitry that provides all necessary voltages for the SOM components and service LEDs indicating SOM power rails state and BMC heartbeat indicator.



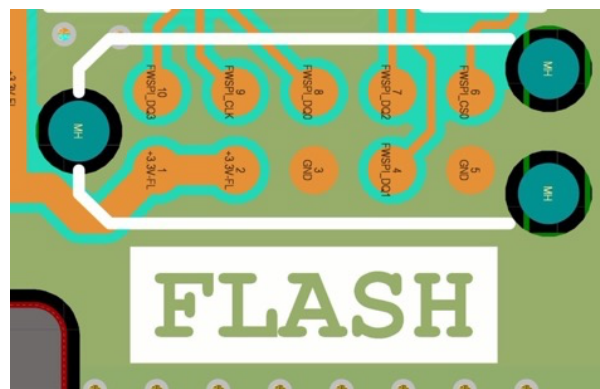
SOM is implemented with inspiration from RunBMC v1.0 standard as a SODIMM module with 260 pins edge connector. Those pins provide both power and communication signals to and from the BMC (GPIO, I2C buses, debug UART console, network, PCIe bus towards host, etc.).

For the initial BMC programming there are pads to SPI bus. The footprint of those pads corresponds to the TAG-connect(tm) connector to the SPI programmer device.

SOM is installed into the motherboard in the corresponding connector horizontally.



BMC firmware is stored in the SPI flash chip soldered on the SOM itself, secondary SPI boot chip function is not used. For initial SPI flash programming, the set of test points is implemented on the board.



External SPI programmer like SF100 or similar is used together with TAG-Connect spring connector (P/N: TC2050).

Power and reset signals

To BMC	
PWROK	Power good signal from the host power distribution system
POST_COMPLETE	Signal indicating the end of POST (Power-on self-test) stage
POWER_BUTTON	Signal from power button on FIO board
RESET_BUTTON	Signal from reset button on FIO board
NMI_BUTTON	Signal from diagnostic button on FIO board
ID_BUTTON	Signal from button ID on FIO board
PWRGD_CPU	Signal from CPU VRs
PWRGD_AUX	Auxiliary power status signal
BMC_PWR_RESTART	BMC cold reset signal
From BMC	
PCH_PWR_RESTART	PCH power cycle signal
POWER_OUT	Power on signal to host
RESET_OUT	Reset signal to host
NMI_OUT	NMI (non-maskable interrupt, diagnostic interrupt) signal to host

Communication

To BMC	
FAN_TACH	Tachometer signals from fan
BIOS_READY	Signal complete stage BIOS
From BMC	
ID_LED	Signal to ID LED on FIO board
LED_STATUS	Signal to status LED on FIO board
BMC_READY	Signal to PCH/CPU/FPGA that BMC is ready to work
CLR_CMOS	Signal to clear CMOS from BMC

RAS

To BMC	
CPU_ERR	Signals errors from CPU
CPU_MISMATCH	Signals install not compatible CPU
CPU_FIVR_FAULT	Signals error fully integrated voltage regulators
CPU_THERM_TRIP	Signals overheating CPU
CPU_VRHOT	Signals from CPU overheating VR power CPU
CPU_MEM_VRHOT	Signals from CPU overheating VR power memory
CPU_MEM_THERMEVENT	Signals overheating memory
CU_CATERR	Signals catastrophic errors from CPU

SPI connections

There are 2 SPI busses going from BMC:

1. FWSPI that goes to SPI flash with BMC firmware;
2. SPI that goes to host's flash with BIOS firmware.

The first one is also connected to the SOM pins for external Root-of-trust IC be able to verify BMC firmware.

The second bus to BIOS flash has a multiplexer between BMC and host to avoid access conflict. The multiplexer is controlled using BMC GPIO signal.

Network

There are 2 dedicated MACs for board management, MAC3 and MAC4. MAC3 is connected to PHY chip on SOM itself, MAC4 is connected to SOM pins. The interface used is RGMII + MDIO. MAC4 is also used for NC-SI using host's OCP3 NIC.

SODIMM pinout

+5V	1	2	GND
+5V	3	4	GND
+5V	5	6	GND
+5V	7	8	GND
+5V	9	10	GND
+5V	11	12	USB2_P
I2C_SCL1	13	14	USB2_N
I2C_SDA1	15	16	USB1_P
I2C_SCL5	17	18	USB1_N
I2C_SDA5	19	20	UART5_RX
I2C_SDA9	21	22	UART5_TX
I2C_SCL9	23	24	I2C_SDA10
UART1_TX	25	26	I2C_SCL10
UART1_RX	27	28	I2C_SCL6
I2C_SCL7	29	30	I2C_SDA7
I2C_SDA8	31	32	I2C_SDA3
I2C_SDA6	33	34	I2C_SCL3
I2C_SCL8	35	36	GND
GND	37	38	GND
GND	39	40	GND
GND	41	42	GND
GND	43	44	GND
GND	45	46	GND
GND	47	48	GND
GND	49	50	GND
GND	51	52	GND
GND	53	54	GND
GND	55	56	GND
FWSPI_DQ1	57	58	GND
FWSPI_CS0	59	60	I3C1_SCL
FWSPI_DQ0	61	62	I3C2_SCL
FWSPI_DQ2	63	64	I3C4_SCL
FWSPI_CLK	65	66	I3C3_SDA
FWSPI_DQ3	67	68	I3C1_SDA
GND	69	70	I3C3_SCL
GND	71	72	I3C2_SDA
GND	73	74	I3C4_SDA
GND	75	76	GND
GND	77	78	GND
GND	79	80	UART3_TX
	81	82	UART3_RX
DP_HPD	83	84	I2C_SCL14
	85	86	I2C_SDA14
	87	88	I2C_SDA2
	89	90	I2C_SCL2
	91	92	GND
	93	94	BMC_RESET
	95	96	GND
LPC_AD0	97	98	DPTX1_N
LPC_AD1	99	100	DPTX1_P
LPC_AD3	101	102	GND
LPC_AD2	103	104	GND
LPC_SIRQ	105	106	DPTX0_N
LPC_CLK	107	108	DPTX0_P
LPC_RESET	109	110	GND
LPC_FRAME	111	112	DP_AUX_N
GND	113	114	DP_AUX_P
GND	115	116	GND
GND	117	118	JTAG_MASTER_TDI
PCIe_EP_TX_P	119	120	JTAG_MASTER_TDO
PCIe_EP_TX_N	121	122	JTAG_MASTER_Nrst
GND	123	124	JTAG_MASTER_TMS
PCIe_EP_CLK_P	125	126	JTAG_MASTER_TCK
PCIe_EP_CLK_N	127	128	I2C_SCL13
GND	129	130	I2C_SDA13

PCIe_EP_RX_P	131	132	I2C_SDA4
PCIe_EP_RX_N	133	134	I2C_SCL4
GND	135	136	SPI2_MISO
SPI2_CS0	137	138	PCIe_EP_PERST
SPI2_CLK	139	140	SPI2_CS1
SPI2_DQ2	141	142	SPI2_DQ3
SPI2_MOSI	143	144	GND
GND	145	146	SPI1_DQ3
SPI1_DQ0	147	148	SPI1_CS1
SPI1_WP	149	150	SPI1_CLK
SPI1_DQ1	151	152	SPI1_DQ2
SPI1_CS0	153	154	PECI
GPIOV3	155	156	PECI_VDD
GPIOV0	157	158	ADC_CH8
ADC_CH14	159	160	ADC_CH13
ADC_CH12	161	162	ADC_CH9
ADC_CH15	163	164	ADC_CH11
ADC_CH10	165	166	ADC_CH2
ADC_CH7	167	168	ADC_CH6
ADC_CH5	169	170	ADC_CH0
ADC_CH3	171	172	GND
ADC_CH4	173	174	VGA_B
VGA_R	175	176	FAN_PWM8
VGA_G	177	178	DDC_DAT
	179	180	FAN_PWM1
DDC_CLK	181	182	FAN_PWM2
VGA_HS	183	184	FAN_PWM5
VGA_VS	185	186	FAN_PWM3
FAN_PWM13	187	188	FAN_PWM7
FAN_PWM4	189	190	FAN_PWM14
FAN_PWM0	191	192	FAN_PWM6
FAN_PWM10	193	194	FAN_TACH12
FAN_TACH10	195	196	FAN_TACH9
FAN_TACH8	197	198	FAN_TACH1
FAN_TACH14	199	200	FAN_TACH15
FAN_TACH2	201	202	FAN_TACH3
FAN_TACH5	203	204	FAN_TACH6
FAN_TACH0	205	206	GND
GND	207	208	GND
FAN_TACH7	209	210	ETH_TXRX0_N
FAN_PWM11	211	212	ETH_TXRX0_P
FAN_TACH4	213	214	GND
FAN_PWM15	215	216	ETH_TXRX1_N
FAN_PWM9	217	218	ETH_TXRX1_P
FAN_PWM12	219	220	GND
FAN_TACH13	221	222	GND
FAN_TACH11	223	224	GND
ETH3_LED1	225	226	ETH_TXRX2_N
GND	227	228	ETH_TXRX2_P
ETH3_LED0	229	230	GND
UART11_TX	231	232	ETH_TXRX3_N
UART11_RX	233	234	ETH_TXRX3_P
UART10_RX	235	236	GND
UART10_TX	237	238	GND
GND	239	240	ETH_MDIO4
ETH_MAC4_TXD0	241	242	ETH_MDC4
ETH_MAC4_CLKO	243	244	ETH_MAC4_TXD1
ETH_MAC4_TXD2	245	246	ETH_MAC4_TXD3
ETH_MAC4_TXEN	247	248	UART2_RX
ETH_MAC4_RXD1	249	250	UART2_TX
ETH_MAC4_RXCTL	251	252	ETH_MAC4_RXD2
	253	254	ETH_MAC4_RXD0
ETH_MAC4_CLKI	255	256	UART4_RX
GND	257	258	UART4_TX
ETH_MAC4_CLKI	259	260	GND

	Power
	Ground
	UART
	I2C
	USB
	I3C
	SPI
	PWM
	Tacho
	Ethernet
	JTAG
	VGA
	Analog Input
	Display Port
	PCIe
	LPC

BMC major features

Primary BMC features include:

- BMC (ASPEED AST2600);
- 1Gb or 2Gb DDR4 BMC memory;
- 2 x BMC dedicated 1GbE LAN for network connectivity;
- Low pin count (LPC), eSPI, I2C and UART connections to the chipset to support in-band management;
- FRUID EEPROM for storage of manufacturing data;
- Power monitoring of all crucial power rails by either direct read of voltage regulators (VRs) or by requests to host supervisor unit (Management Engine, Power Management Processor, etc.);
- Cooling control by monitoring essential server temperatures and controlling fans
- Collecting sensor information for further transfer to monitoring and management system;
- Keyboard, video, and mouse transfer over the network (KVM feature);
- Host serial port transfer over the network (SOL function);
- Passing virtual media images into host by means of simulated USB mass-storage device (Virtual Media function);
- Collecting and storing system event list (SEL) and providing it via network;
- Collecting and storing all RAS events;
- Providing IPMI and RedFish network interfaces for interaction;
- Providing access control on BMC's network interfaces using logins, password, and encryption keys;
- Set of boot options of host by means of standard IPMI and RedFish commands;
- Collection of all sensors and configuration information of the server and providing it as JSON on unauthorized request via HTTPS.

IPMI support

IPMI v2.0 is implemented in BMC. Despite the IPMI stack is still in active development, most mandatory IPMI commands are supported. The fallback to IPMI v1.5 or IPMI v1.0 is not supported due to security concerns.

RedFish support

RedFish is implemented in accordance with 2022.3 DMTF specification.

Serial over LAN

BMC FW supports text console redirection (Serial over LAN, SOL) to remotely access BIOS setup or text consoles available on the serial console of host system. FW includes support for IPMI based SOL where the standard IPMI client like IPMITOOL is used to establish a SOL session. SOL default baud rate is set by BMC to 115200.

OEM commands support

Except for standard IPMI commands, BMC provides the OEM commands that implement specific requirements from the consumers.

Event logging support

Standard Server Error Log (SEL) as described in IPMI v2.0 specification and RedFish log are implemented.

Power control

The power control in the BMC is implemented by dedicated service. It provides all necessary timing and a state machine for different models of servers. The host power can be controlled using buttons on the front input-output board (FIO), using standard IPMI commands or using RedFish API. Button power on/power off should work with failed BMC.

POST codes

The BIOS outputs a set of Power-On Self-Test (POST) codes identifying the current initialization step and any errors encountered during the initialization. The POST codes sequence can be fetched either through OEM IPMI command or by calling RedFish service. Double seven-segment indicator on FIO board for displaying the current POST code.

BMC Heartbeat LED

BMC heartbeat LED blinks with 1Hz frequency during normal operations and with 5Hz frequency during upgrade.

ID LED (Color: Blue)

There is an ID LED located on the front panel of the server. It is used to identify the location of the server in the rack. It can be turned on and off either by physical button located on the same FIO, or by OEM IPMI command, or by RedFish service.

State LED (Color: Red / Green)

The host state LED on the FIO is used to indicate the host status and has the following states: Green – all OK, Red – uncleared error or warning is present in the system.

External devices LED control

It is necessary to control the indication LEDs on the external devices, e.g., JBOD. For this purpose, a set of IPMI OEM commands is implemented.

Firmware upgrade

BMC firmware upgrade is possible using RedFish service or via BMC web interface. Server model and firmware files cryptographic signatures are used to prevent malicious software to be flashed.

BMC time synchronization

BMC time is synchronized using NTP protocol (unicast, broadcast, multicast) and stored in the external real-time clock (RTC) with battery backup. It is also possible to set BMC time from host using IPMI, but this command is disabled if BMC is in sync with NTP server.

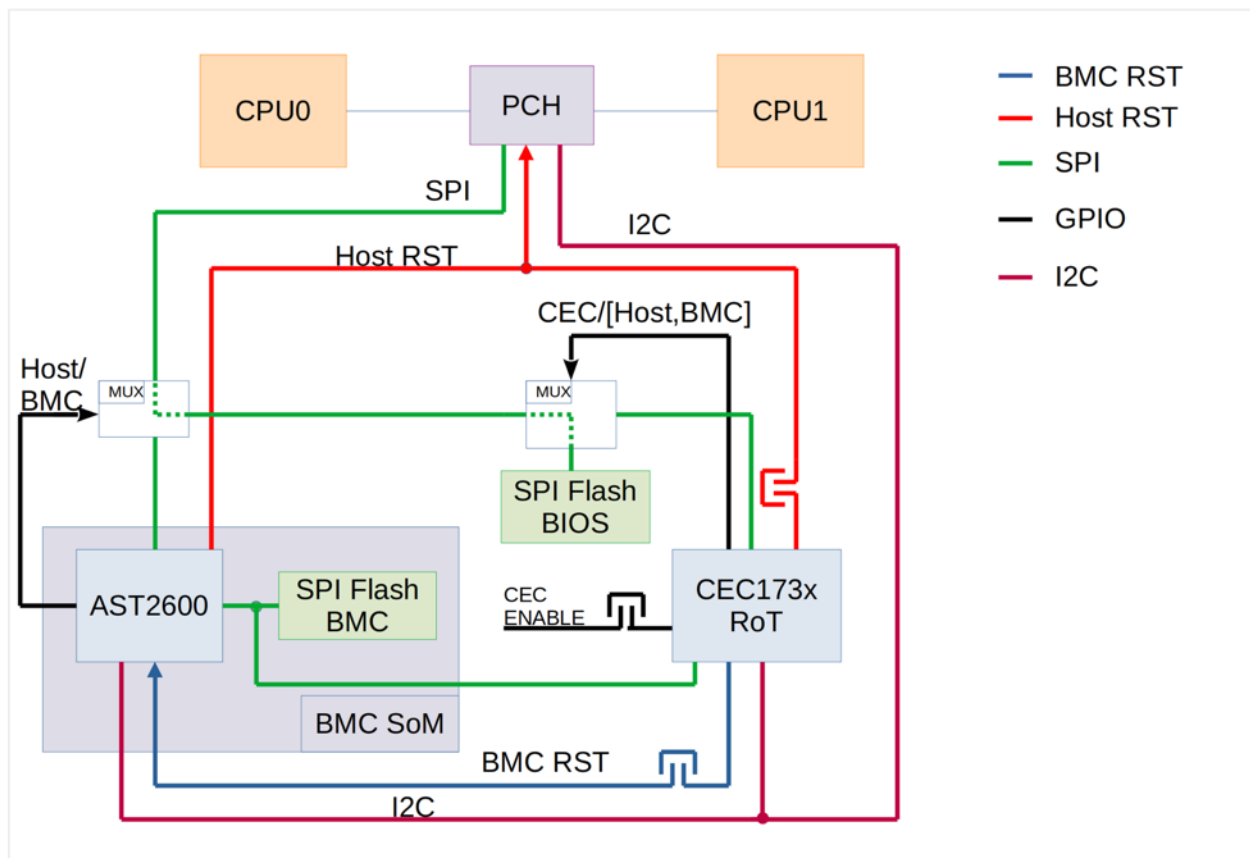
Virtual Media

Virtual Media function is a pass of USB or CD/DVD image provided as a binary image into host system. It is done using virtual USB device (either USB or CD/DVD) and USB 2.0 connection between BMC and host.

15. Security

The security requirements are related to Root of trust and secure boot mechanisms.

The target block diagram is shown below as an example for Intel platform. To introduce an extended flexibility, both Microchip CEC1736 (CEC on the diagram) and AST2600 embedded RoT can verify the firmware and release reset signals to application processors, thus upon the final user, one or another approach can be used.



Appendix A - Checklist for IC approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

Item	Status	Link to detailed explanation
Has this contribution been presented to an OCP Project group during a project call or engineering workshop?	Yes	If “No”, please state the reason.
Approval by Project Leads	No	Waiting for the presentation to the steering committee
Is this contribution entered into the OCP Contribution Portal?	No	Waiting for the presentation to the steering committee
Was it approved in the OCP Contribution Portal?	No	Waiting for the presentation to the steering committee