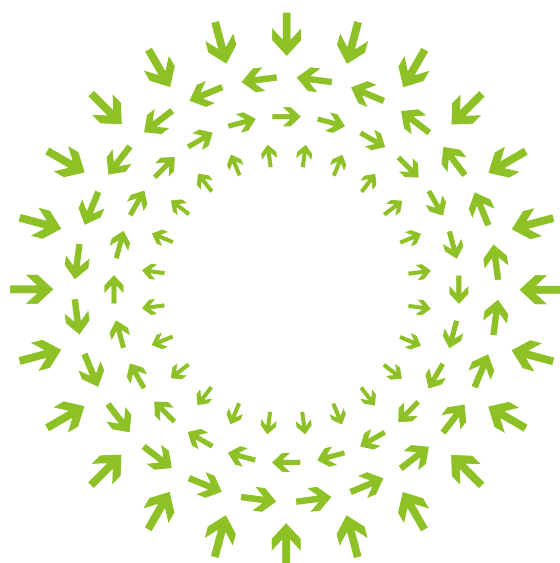




OPEN

Compute Project

MiTAC Capri V2 1S Server

Rev 1.2

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James Chiang, MiTAC Computing Technology Corp.**

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2. Compliance with OCP Tenets

2.1 Openness

- The Capri2 OCP server sled compatible with either ORV2 or ORV3 Rack cabinet.
- One OCP 3.0 mezzanine slot.

2.2 Efficiency

- Supporting AMD EPYC 9004 processor.
- Increasing DDR5 memory and PCIE Gen5 speed and performance
- Design with new generation of BMC chip controller; Aspeed AST2600 optimizes the performance and computing power.

2.3 Impact

- The server form factor is same as Capri, so it supports Cubby shelf for ORV2 cabinet
- Modify Cubby for supporting ORV3 cabinet

2.4 Scale

- Define 2 SKUs for Compute and AI inference.

2.5 Sustainability

- Continuing to develop a SKU of Capri2 that implements immersion cooling technology. It can reduced datacenter PUE, and save operating expense.

3. Change Log

Revision History

Date	Name	Description
Sep 5 th ,2023	Michael Yeh	Initial version
Oct 3 rd , 2023	Michael Yeh	Add OCP Tenets
Oct 11 th ,2023	Michael Yeh	Add Sustainability

Scope & Overview

Scope:

This document defines the technical specifications for the MiTAC CP2S11 used in Open Compute Project Capri V2 1S Server.

Overview:

MiTAC CP2S11 1S Server (Capri V2) is a highly optimized OCP system. This product follows the same form factor as Facebook Tioga Pass product and based on AMD EPYC™ 9004 Serial (Genoa) product family CPU architecture. It supports up to 8 DIMMs.

MiTAC CP2S11 1S Server (Capri V2) has two models for customers to choose depending on the drive type, **Standard sku** support 2 NVMe SSD; while **Ultra sku** supports 4 E1.S.

4. Rack Compatibility

MiTAC CP2S11 1S Server (Capri V2) system is designed to work with Open Rack V2 (Orv2) and Open Rack V3 (Orv3) structure.

5. Physical Specifications

5.1 Block Diagram

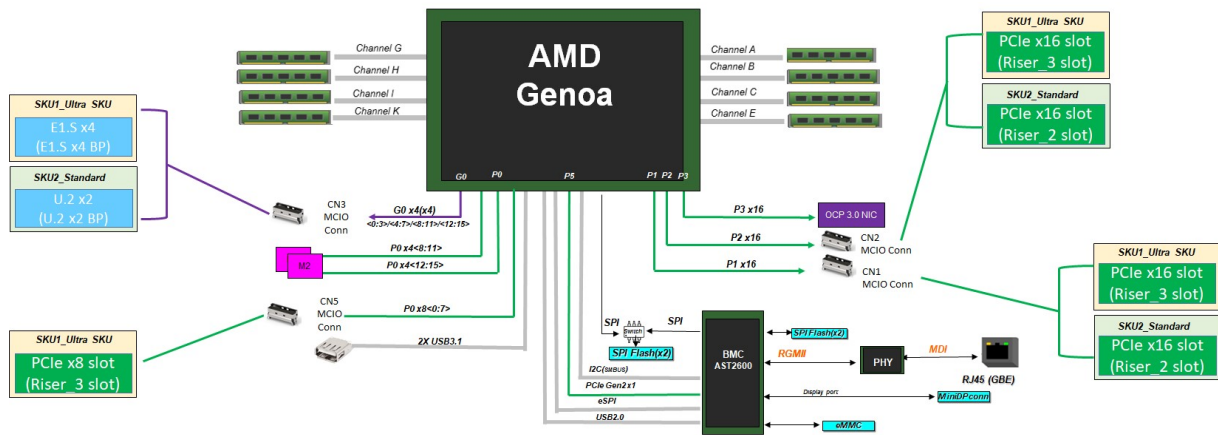


Figure 1 MiTAC CP2S11 1S Server (Capri V2) Block Diagram

5.2 Placement and Form Factor

MiTAC CP2S11 1S Server (Capri V2) dimension is 28.46" x 6.87" x 3.5" (724 x 175 x 89mm); this is compatible with Cubby (2OU 3NODES) chassis. For easy understanding, MiTAC CP2S11 1S Server (Capri V2) is having the same form factor as Tioga Pass and Capri.

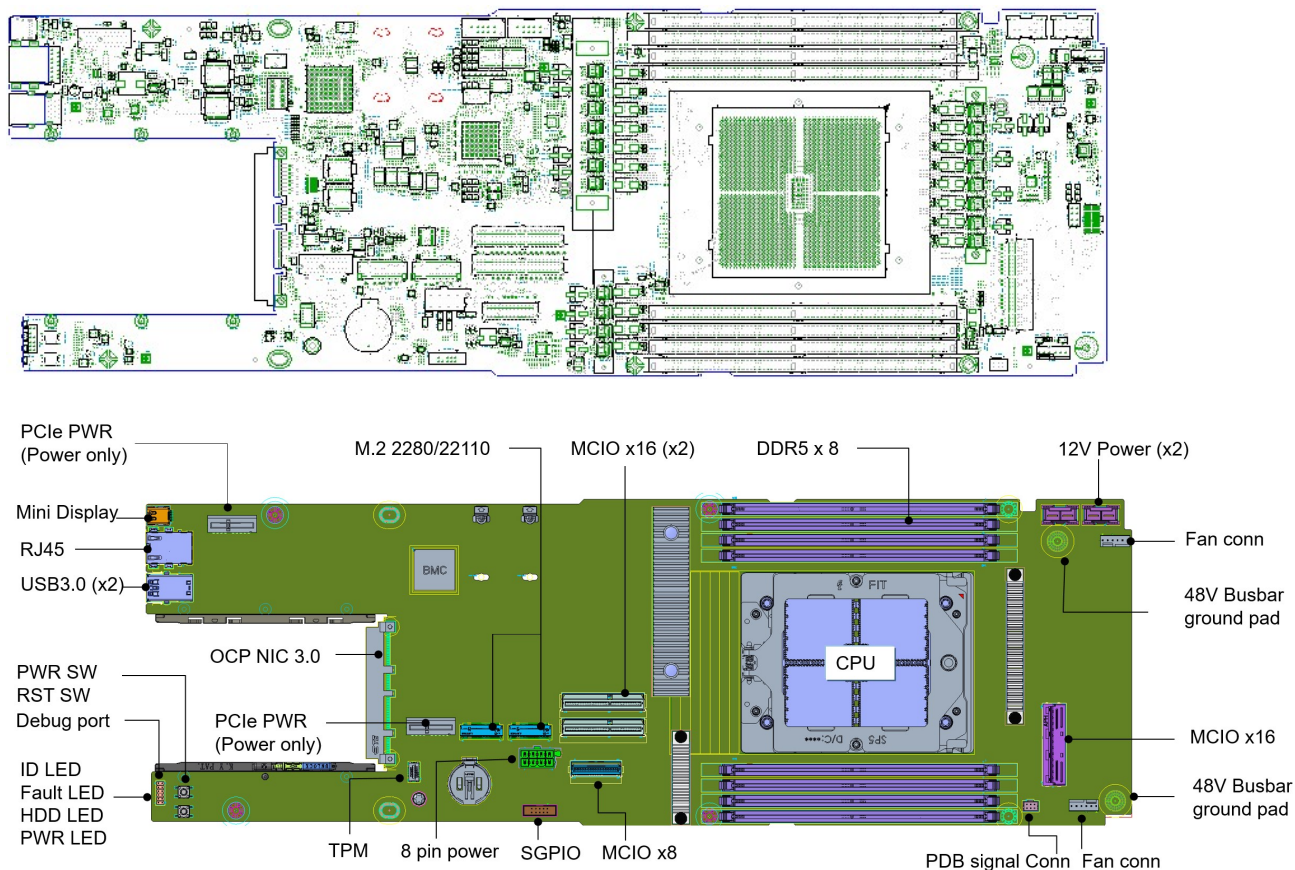


Figure 2 MiTAC Capri V2 1S Server placement

5.3 CPU and Memory

As mentioned in Scope and Overview (Page 9), MiTAC CP2S11 1S Server (Capri V2) has two different sku and below is the table for CPU and Memory support.

	Advanced	Ultra
Processor	● AMD EPYC™ 9004, Genoa (TDP: ≤ 400W)	
Memory	Up to 4TB RDIMM(DDR5, 4800, pending ecosystem enablement) 8 DIMM slots/ 8 channels (1DPC)	

5.4 PCB Stack-Up

MiTAC CP2S11 1S Server (Capri V2) has mainboard, riser board (2_slots/3_slots for Ultra/Standard SKU), E1.S x4 backplane board, U.2 x2 backplane board and PDB(only applied on 48V SKU). Below is the stack-up info. for reference.

此設計需要 單面背板, 單面銅箔(Bottom), VPPPO, Low Etching, LDI																							
請按圖(件)品名與規格 Loss Spec + Spec or Loss Spec Table 而訂								RUBY 2DPC 公模 board file ONYX 1DPC 公模 board file DDR (只有 Top 50 ohm) 50 ohm Single-Ended, Default				BGA Differential-Pair, pitch=37mil, pad=16mil, Drill=8mil 內層 3.75/3.5/3.75 需要採用 LDI 作業				RUBY 2DPC 公模 board file DDR 75 ohm Differential-Pair DDR DQS							
MTAC SI 指定 Loss Spec (下拉式選單):				Ultra Low				ONYX 1DPC 公模 board file DDR 45 ohm Single-Ended															
Thickness Spec (mil or mm +/- 10% or 其他選單值):				1.93 mm																			
Golden-finger (Yes or No), (下拉式選單):				No																			
MITAC Proposal				MITAC Design				Simulated				MITAC Design				Simulated							
No. of Layer	Type	Cu weight(oz)	THK (mil)	Target Zo (Ω)	LW (mil)	Target Zo ± 1 (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	Target Zo ± 1 (Ω)	LW (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo ± 1 (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo ± 1 (Ω)	LW/LS (mil)				
L1	TOP	6.5oz + Plating	2	45±10%	4.72	44.89	4.72	50±10%	3.9	49.07	3.9	阻抗不控制	3.5/4	86.14	3.5/4	75±10%	5.91/5.12	74.9	5.51/5.52				
pp			2.3																				
L2	GND1	1oz	1.2																				
core			3																				
L3	IN1	1oz	1.2	45±10%	4.53	45.94	4.73	50±10%	3.9	50.36	3.9	阻抗不控制	3.75/3.5	86.23	3.75/3.5	75±10%	5.32/5.12	75.74	5.72/4.72				
pp			6																				
L4	GND2	1oz	1.2																				
core			3																				
L5	IN2	1oz	1.2	45±10%	4.53	45.94	4.73	50±10%	3.9	50.36	3.9	阻抗不控制	3.75/3.5	86.23	3.75/3.5	75±10%	5.32/5.12	75.74	5.72/4.72				
pp			6																				
L6	GND3	1oz	1.2																				
core			3																				
L7	VCC1	2oz	2.4																				
pp			2.4																				
L8	VCC2	2oz	2.4																				
core			3																				
L9	GND4	1oz	1.2																				
pp			6																				
L10	IN3	1oz	1.2	45±10%	4.53	45.94	4.73	50±10%	3.9	50.36	3.9	阻抗不控制	3.75/3.5	86.23	3.75/3.5	75±10%	5.32/5.12	75.74	5.72/4.72				
core			3																				
L11	GND5	1oz	1.2																				
pp			6																				
L12	IN4	1oz	1.2	45±10%	4.53	45.94	4.73	50±10%	3.9	50.36	3.9	阻抗不控制	3.75/3.5	86.23	3.75/3.5	75±10%	5.32/5.12	75.74	5.72/4.72				
core			3																				
L13	GND6	1oz	1.2																				
pp			2.3																				
L14	BOTTOM	6.5oz + Plating	2	45±10%	4.72	44.89	4.72	50±10%	3.9	49.07	3.9	阻抗不控制	3.5/4	86.14	3.5/4	75±10%	5.91/5.12	74.9	5.51/5.52				
SM			0.7																				
Total Thickness (mil)			75.9																				
Total Thickness (mm)			1.92786																				

Figure 3 MiTAC CP2S11 1S Server MB 14-layer PCB Stack-Up

PWB Thickness		1.57mm +/-0% (合金手插)		Capri2		2 slot Riser		50 ohm Single-Ended		85 ohm Differential-Pair		實際成品 Loss spec (dB/in)								
PWB Material		ultra low loss (EM-890K + HVLP2 +flow etching)																		
MITAC Proposal				Vendor proposal				MITAC Design		_Simulated_		MITAC Design		_Simulated_		4G	8G	16G		
No. of Layer	Type	Cu weight	Cu Type	THK (mil)	Structure	Cu Type	THK (mil)	RC%	DK(1G)	DF (1G)	Ref layers	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	
L1	TOP	0.5+Plating	STD	0.5		HTE	1.9		3.8			50±10%	5	50	4.7	85±10%	5.5/5.5	84.77	5.15/5.85	
pp				2.5	1035*1		2.4	75%	2.57	0.002								0.55	0.9	
L2	GND	1	HVLP2	1.2			2.4												1.5	
Core				3.5	1078*1		3.5			0.002										
L3	IN1	1	HVLP2	1.2		HVLP2	1.2					50±10%	4.5	50.13	4.35	85±10%	5.5/5	84.82	5.3/5.2	
pp				4.5	1035*2		4.30	75%	2.57	0.002								0.33	0.8	
L4	GND	1	HVLP2	1.2		HVLP2	1.2													
Core				3	1078*1		3		2.81	0.002										
L5	IN2	1	HVLP2	1.2		HVLP2	1.2					50±10%	5	50.1	4.65	85±10%	5.5/5.5	85.23	5.45/5.55	
pp				9	3313*2		7.90	61%	2.73	0.002								0.32	0.48	
L6	PWR/GND	1	RG311	1.2		HVLP2	1.2												0.77	
Core				3.5	1078*1		3.5		2.75	0.002										
L7	PWR/GND	1	RG311	1.2		HVLP2	1.2													
pp				9	3313*2		7.90	61%	2.73	0.002										
L8	IN3	1	HVLP2	1.2		HVLP2	1.2					50±10%	5	50.1	4.65	85±10%	5.5/5.5	85.23	5.45/5.55	
Core				3	1078*1		3		2.81	0.002								0.32	0.48	
L9	GND	1	HVLP2	1.2		HVLP2	1.2												0.77	
pp				4.5	1035*2		4.30	75%	2.57	0.002										
L10	IN4	1	HVLP2	1.2		HVLP2	1.2					50±10%	4.5	50.13	4.35	85±10%	5.5/5	84.82	5.3/5.2	
Core				3.5	1078*1		3.5		2.75	0.002								0.33	0.8	
L11	GND	1	HVLP2	1.2		HVLP2	1.2												0.79	
pp				2.5	1035*1		2.4	75%	2.57	0.002										
L12	BOT	0.5+Plating	STD	1.9		HTE	1.9					50±10%	5	50	4.7	85±10%	5.5/5.5	84.77	5.15/5.85	
	SM			0.5			0.6		3.8									0.55	0.9	
Total Thickness (mil)				65.3		61.50												4G	8G	16G
Total Thickness (mm)				1.658623		1.562103												0.55	0.99	1.78
																		0.31	0.48	0.77
																		Ultra low-loss 2	Microstrip	Stripline

Figure 4 MiTAC CP2S11 1S Server Riser Board(2 slots) Stack-Up

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PWB Thickness	1.37mm +/- .016" (合金手板)	Capri2		3 Slot Riser		50 ohm Single-Ended				85 ohm Differential-Pair				實際成品 Loss spec (dB/in)									
PWB Material	ultra low loss (EM-8802 + HVLP2 +slow etching)																						
MITAC Proposal						Vendor proposal						MITAC Design		Simulated		MITAC Design		Simulated		4G	8G	16G	
No. of Layer	Type	Cu weight	Cu Type	THK (mil)	Structure	Cu Type	THK (mil)	RC%	DN(1G)	DF(1G)	Ref layers	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)				
L1	TOP	0.5+Plating	STD	1.9		HTE	1.9					50±10%	5	50	4.7	85±10%	5.5/5.5	84.77	5.15/5.85	0.55	0.9	1.5	
pp				2.5	1035*1		2.4	75%	2.57	0.002													
L2	GND	1	HVLP2	1.2		HVLP2	1.2																
Core				3.5	1078*1		3.5		2.75	0.002													
L3	IN1	1	HVLP2	1.2		HVLP2	1.2					50±10%	4.5	50.13	4.35	85±10%	5.5/5	84.82	5.3/5.2	0.33	0.8	0.79	
pp				4.5	1035*2		4.30	75%	2.57	0.002													
L4	GND	1	HVLP2	1.2		HVLP2	1.2																
Core				3	1078*1		3		2.81	0.002													
L5	IN2	1	HVLP2	1.2		HVLP2	1.2					50±10%	5	50.1	4.65	85±10%	5.5/5.5	85.23	5.45/5.55	0.32	0.48	0.77	
pp				9	3313*2		7.00	61%	2.73	0.002													
L6	PWR/GND	1	RG311	1.2		HVLP2	1.2																
Core				3.5	1078*1		3.5		2.75	0.002													
L7	PWR/GND	1	RG311	1.2		HVLP2	1.2																
pp				9	3313*2		7.00	61%	2.73	0.002													
L8	IN3	1	HVLP2	1.2		HVLP2	1.2					50±10%	5	50.1	4.65	85±10%	5.5/5.5	85.23	5.45/5.55	0.32	0.48	0.77	
Core				3	1078*1		3		2.81	0.002													
L9	GND	1	HVLP2	1.2		HVLP2	1.2																
pp				4.5	1035*2		4.30	75%	2.57	0.002													
L10	IN4	1	HVLP2	1.2		HVLP2	1.2					50±10%	4.5	50.13	4.35	85±10%	5.5/5	84.82	5.3/5.2	0.33	0.8	0.79	
Core				3.5	1078*1		3.5		2.75	0.002													
L11	GND	1	HVLP2	1.2		HVLP2	1.2																
pp				2.5	1035*1		2.4	75%	2.57	0.002													
L12	BOT	0.5+Plating	STD	1.9		HTE	1.9					50±10%	5	50	4.7	85±10%	5.5/5.5	84.77	5.15/5.85	0.55	0.9	1.5	
	SM			0.5			0.6		3.8												4G	8G	16G
Total Thickness (mil)					65.3			61.90													0.55	0.99	1.78
Total Thickness (mm)					1.658623317			1.562103													0.31	0.48	0.77
																					Ultra low-loss 2 Microstrip Stripline		

Figure 5 MiTAC CP2S11 1S Server Riser Board(3 slots) Stack-Up

PWB Thickness	2mm +/- .10%			50 ohm Single-Ended				85 ohm Differential-Pair				100 ohm Differential-Pair					
PWB Material	EM526+RG311																
MITAC Proposal				MITAC Design				Simulated		MITAC Design		Simulated		MITAC Design		Simulated	
No. of Layer	Type	Cu weight	Cu Type	THK (mil)	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	
	SM			0.5													
L1	TOP	0.5+Plating	STD	1.9	50±10%	4.5	49.78	4.5	85±10%	5/7	85.88	5.0/7	100±10%	4/11	99.6	4.0/11	
pp				2.7													
L2	GND	1	RG311	1.2													
Core				4													
L3	IN1	1	RG311	1.2	50±10%	4	49.99	4.1	85±10%	5/7	85.03	5.15/6.85	100±10%	4/11	99.47	4.0/11	
pp				5													
L4	GND	1	RG311	1.2													
Core				4													
L5	IN2	1	RG311	1.2	50±10%	5	49.94	5.3	85±10%	5.5/6.5	85.21	5.8/6.2	100±10%	4.5/10.5	100.2	4.7/10.3	
pp				12													
L6	PWR/GND	1	RG311	1.2													
Core				6													
L7	PWR/GND	1	RG311	1.2													
pp				12													
L8	IN3	1	RG311	1.2	50±10%	5	49.94	5.3	85±10%	5.5/6.5	85.21	5.8/6.2	100±10%	4.5/10.5	100.2	4.7/10.3	
Core				4													
L9	GND	1	RG311	1.2													
pp				5													
L10	IN4	1	RG311	1.2	50±10%	4	49.99	4.1	85±10%	5/7	85.03	5.15/6.85	100±10%	4/11	99.47	4.0/11	
Core				4													
L11	GND	1	RG311	1.2													
pp				2.7													
L12	BOT	0.5+Plating	STD	1.9	50±10%	4.5	49.78	4.5	85±10%	5/7	85.88	5.0/7	100±10%	4/11	99.6	4.0/11	
	SM			0.5													
Total Thickness (mil)				78.2													
Total Thickness (mm)				1.986283973													

Figure 6 MiTAC CP2S11 1S Server U.2 x2 backplane board

Open Compute Project • <MiTAC Capri V2 1S Server>

PWB Thickness	1.57mm +/-8%	Capri2			E1.S BP						50 ohm Single-Ended				85 ohm Differential-Pair				實際成品 Loss spec (dB/in)				
PWB Material	ultra low loss (EM-890K + HVLP2 -New etching)																						
MITAC Proposal		Vendor proposal										MITAC Design		Simulated		MITAC Design		Simulated		4G	8G	16G	
No. of Layer	Type	Cu weight	Cu Type	THK (mil)	Structure	Cu Type	THK (mil)	RC%	Dk(1G)	Df(1G)	Ref layers	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)				
L1	TOP	0.5+Plating	STD	1.9		HTE	1.9					50±10%	5	50	4.7	85±10%	5.5/5.5	84.77	5.15/5.85	0.55	0.9	1.5	
pp				2.5	1035*1		2.4	75%	2.57	0.002													
L2	GND	1	HVLP2	1.2		HVLP2	1.2																
Core				3.5	1078*1		3.5		2.75	0.002													
L3	IN1	1	HVLP2	1.2		HVLP2	1.2					50±10%	4.5	50.13	4.35	85±10%	5.5/5	84.82	5.3/5.2	0.33	0.8	0.79	
pp				4.5	1035*2		4.30	75%	2.57	0.002													
L4	GND	1	HVLP2	1.2		HVLP2	1.2																
Core				3	1078*1		3		2.81	0.002													
L5	IN2	1	HVLP2	1.2		HVLP2	1.2					50±10%	5	50.1	4.65	85±10%	5.5/5.5	85.23	5.45/5.55	0.32	0.48	0.77	
pp				9	3313*2		7.90	61%	2.73	0.002													
L6	PWR/GND	1	RG311	1.2		HVLP2	1.2																
Core				3.5	1078*1		3.5		2.75	0.002													
L7	PWR/GND	1	RG311	1.2		HVLP2	1.2																
pp				9	3313*2		7.90	61%	2.73	0.002													
L8	IN3	1	HVLP2	1.2		HVLP2	1.2					50±10%	5	50.1	4.65	85±10%	5.5/5.5	85.23	5.45/5.55	0.32	0.48	0.77	
Core				3	1078*1		3		2.81	0.002													
L9	GND	1	HVLP2	1.2		HVLP2	1.2																
pp				4.5	1035*2		4.30	75%	2.57	0.002													
L10	IN4	1	HVLP2	1.2		HVLP2	1.2					50±10%	4.5	50.13	4.35	85±10%	5.5/5	84.82	5.3/5.2	0.33	0.8	0.79	
Core				3.5	1078*1		3.5		2.75	0.002													
L11	GND	1	HVLP2	1.2		HVLP2	1.2																
pp				2.5	1035*1		2.4	75%	2.57	0.002													
L12	BOT	0.5+Plating	STD	1.9		HTE	1.9					50±10%	5	50	4.7	85±10%	5.5/5.5	84.77	5.15/5.85	0.55	0.9	1.5	
SM				0.5			0.6		3.8												4G	8G	16G
Total Thickness (mil)				65.3			61.90														0.55	0.99	1.78
Total Thickness (mm)				1.658623			1.562103														0.31	0.48	0.77
																		Ultra low-loss 2	Microstrip Stripline				

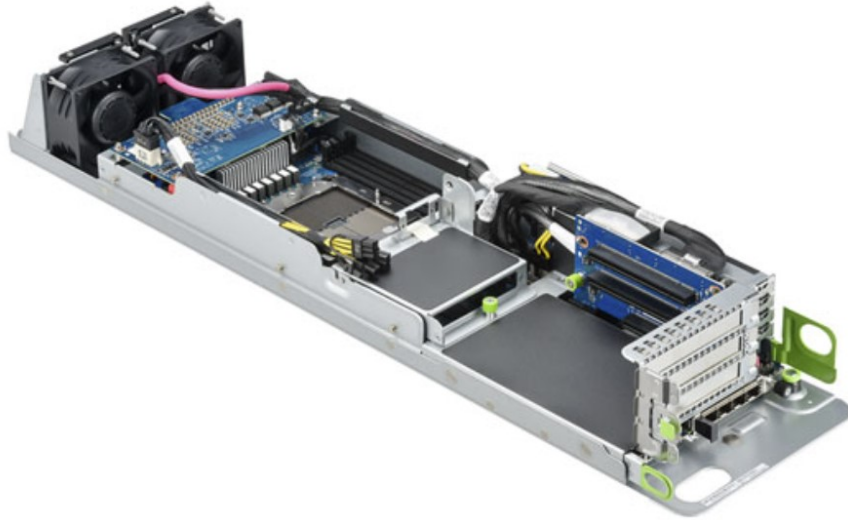
Figure 7 MiTAC CP2S11 1S Server E1.S x4 backplane board

PWB Thickness	2.3mm+/-10%	Capri2_PDB										50 ohm Single-Ended			
PWB Material	TU-862 HF														
MITAC Proposal					Vendor proposal						MITAC Design		Simulated		
No. of Layer	Type	Cu weight	Cu Type	THK (mil)	Structure	Cu Type	THK (mil)	RC%	Dk(1G)	Ref layers	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	
	SM			1	SM		1		3.6						
L1	TOP	1+Plating	HTE	2.4	Cu+Plating	HTE	2.4			L2	50±10%	6.2	50.6	6.2	
pp				4	1067(71%)*2		4.08	71%	3.67						
L2	GND	3	RTF	3.6	3	RTF	3.6								
Core				12	12mil_1506*2		12		4.39						
L3	IN1	3	RTF	3.6	3	RTF	3.6			L2,L4	50±10%	9	50.34	9	
pp				14	2116HR(60%)*3		13.78	60%	3.97						
L4	PWR/GND	3	RTF	3.6	3	RTF	3.6								
Core				4	4mil_1067*2		4		3.81						
L5	PWR/GND	3	RTF	3.6	3	RTF	3.6								
pp				14	2116HR(60%)*3		13.78	60%	3.97						
L6	IN2	3	RTF	3.6	3	RTF	3.6			L5,L7	50±10%	9	50.34	9	
Core				12	12mil_1506*2		12		4.39						
L7	GND	3	RTF	3.6	3	RTF	3.6								
pp				4	1067(71%)*2		4.08	71%	3.67						
L8	BOT	1+Plating	HTE	2.4	Cu+Plating	HTE	2.4			L7	50±10%	6.2	50.6	6.2	
	SM			1	SM		1		3.6						
Total Thickness (mil)				92.4	Total		92.12								
Total Thickness (mm)				2.346964694			2.33985								

Figure 8 MiTAC CP2S11 1S Server PDB backplane board

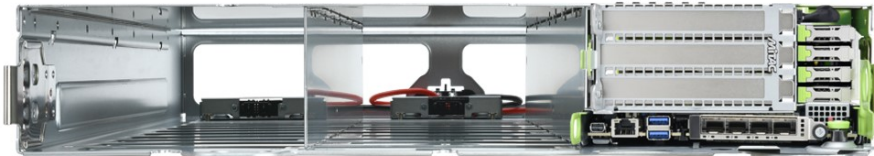
5.5 Figures & Illustrations

Figure 6 MiTAC Capri V2 1S



Server

Figure 7 MiTAC Capri V2 1S Server in Cubby



6. BIOS

6.1 BIOS Chip

MiTAC CAPRI V2 1S Server follows OCP (Open Computing Project) v4_0v16 specification to design the board and it adopts AMD GENOA processor. The ROM size of Capri V2 BIOS is 32MB.

6.2 BIOS Source Code

The BIOS source code is from AMI.

6.3 BIOS Source Code

The BIOS source code is from AMI.

6.4 BIOS Feature Requirements

6.4.1 Boot Logo

While BIOS booting, if there is a graphic display supported in the system, user can see the defined logo screen when enabling boot logo present feature. BIOS shall provide a selection option in SETUP for user to choose boot logo presented or not at the boot time. If this feature is enabled, it could be scale to full screen with sufficient image resolution and keep a while of seconds on screen.

If user set boot logo presented option to be disabled, BIOS shall switch to IBV native defined mode on display. The message must include platform information which is defined in section “4.3.2 Information Displayed during POST Time” to let user can properly to know system summary information.

Need to take care of logo resolution when it's in full screen scale. The MiTAC logo file and the minimum format requirement are defined as,

- BMP format
- 8bits color depths
- 800x600 pixels dimension

6.4.2 Information Displayed during POST Time

During BIOS POST, the text message will be showed on the host display or redirected to remote console connection for user to examine the summary information about the whole system without entering BIOS setup. The screen contents shall hold and keep around 1 second so as to view the information easily. The contents would cover below information,

- BIOS Version
- BIOS Build Date
- BMC Version
- IPMI IP Address
- Total Installed Memory Size

6.4.3 BIOS Hotkeys

Support to use specified single key or combination keys to enter BIOS Setup Menu, the default setting is or <F2> during boot time when prompt information is displayed on screen or remote console. The following instructional message would be displayed on the screen.

- Press <F11> to prompt boot popup menu.
- Press <F12> to PXE Boot.
- ¹Press or <F2> to enter setup.

¹ Number Lock function shall set **Disabled** as default.

Furthermore, the prompt presented time on the screen would be a selection in BIOS setup menu. User can define a specified value with seconds scale to wait for input actions.

The default setup prompt timeout is **1** seconds.

6.4.4 Remote Combination Hotkeys

BIOS provides serial redirection feature in various remote management console. Here is the combination key supported list for different kind of terminal setting.

Key or Function	Sequence
Right	<ESC> [, C
Left	<ESC> [, D
Up	<ESC> [, A
Down	<ESC> [, B
Home	<ESC> [, H
End	<ESC> [, K
F1	<ESC> O , P
F2	<ESC> O , Q
F3	<ESC> O , R
F4	<ESC> O , S
System Reset	<ESC>R<ESC>r<ESC>R

Figure 8 Standard ANSI Sequences

Key or Function	Sequence
F1	<ESC> O , P
F2	<ESC> O , Q
F3	<ESC> O , R
F4	<ESC> O , S
F5	<ESC> O , T
F6	<ESC> O , U
F7	<ESC> O , V
F8	<ESC> O , W
F9	<ESC> O , X
F10	<ESC> O , Y
F11	<ESC> O , Z
F12	<ESC> O , [
Home	<ESC> [, 1, ~
Ins	<ESC> [, 2, ~
Del	<ESC> [, 3, ~
End	<ESC> [, 4, ~
Page Up	<ESC> [, 5, ~
Page Dn	<ESC> [, 6, ~

Figure 9 Putty VT100 Keypad

6.4.5 BIOS POST Code

The POST codes are composed of two or four HEX codes according to Intel or AMD platform. During the period of POST time, BIOS shall output these HEX codes to specified interfaces or media to let user realize the system POST status. *E.g. BMC SoL.*

6.4.5.1 POST Code for OPROM Entry and Exit

It's a special pair of BIOS post codes to indicate the entry and exit of option ROM. Two consecutive bytes are assigned for the entry and exit to avoid the same sequence used on another BIOS POST code. The definition is,

- Use [AA][C0] to indicate entering Option ROM.
- Use [BB][C1] to indicate exiting Option ROM.

6.4.6 BMC FRB2 Watch Dog Timer

The default setting of watch dog function is DISABLED and only be enabled in MP stage. The default timeout setting is 15 minutes and then RESET the system when the timer expired. The watchdog timer is always disabled after POST.

6.4.7 Protected Processor Inventory Number

BIOS shall support PPIN and set default to **[Unlock and Enable]**. There are two ways for user to access PPIN,

- BIOS shall map PPIN of CPU to SMBIOS OEM Strings (Type 11) String 5 . User can view PPIN value from Linux's "dmidecode" command.
- BIOS shall implement Send_PPIN OEM Command to communicate to BMC, per BMC's request.

BIOS shall perform 2 actions to synchronize PPIN value to BMC,

- Serves SMI# signal from BMC and use Send_PPIN OEM command to communicate PPIN to BMC.
- Use Send_PPIN OEM command to communicate PPIN to BMC when BIOS POST COMPLETE.

6.4.8 Start of POST and End of POST Information

BIOS shall assert specified GPIO pin status to inform BMC about BIOS **start of POST** and **end of POST** events.

6.4.9 Manufacture Mode

BMC will provide an IPMI command to enter manufacture mode. It is a special BIOS mode designed to decrease the time which systems spend on the assembly line. This is done by skipping non-essential boot functions/tests and by prioritizing pre-defined boot devices ordering. These changes decrease the boot time significantly which allows more systems to complete the factory processes in less time.

BIOS shall replace AMI boot logo with a manufacture mode picture like below and set Quiet Mode to **disabled** to show up on the screen during BIOS POST Time to indicate user that the system is booting on manufacture status.

Booting in MFG mode

6.4.9.1 Prerequisites

For example, BIOS could implement below listed items,

- Set “Onboard LAN” to be the first bootable device, if it presents.
- System console redirection would be always enabled.
- Do not launch onboard storage and add-on card, if it appears in system.
- Launch onboard storage and add-on card, if it doesn’t appear in system.

6.4.10 WHEA ID

Beginning with Windows Server 2008 and Windows Vista SP1, when a hardware error occurs, the operating system creates an error record that describes the error condition and sends an event tracing for Windows (ETW) event that contains the error record to user mode. The format of the error record is based on the Common Platform Error Record as described in Appendix N of version 2.2 of the Unified Extensible Firmware Interface (UEFI) Specification.

The following table describes each of the WHEA error-specific hardware error events that are defined for Windows Server 2008, Windows Vista SP1, and later versions of Windows.

Event	Event ID
WHEALOGR_DEFAULT_ERROR	1
WHEALOGR_DEFAULT_WARNING	2
WHEALOGR_DEFAULT_INFO	3
WHEALOGR_PCIE_ERROR	16
WHEALOGR_PCIE_WARNING	17
WHEALOGR_XPF_MCA_ERROR	18
WHEALOGR_XPF_MCA_WARNING	19
WHEALOGR_XPF_AMD64NB_MCA_ERROR	20
WHEALOGR_XPF_AMD64NB_MCA_WARNING	21
WHEALOGR_PLATFORM_MEMORY_ERROR	22
WHEALOGR_PLATFORM_MEMORY_WARNING	23
WHEALOGR_PCIBUS_ERROR	24
WHEALOGR_PCIBUS_WARNING	25
WHEALOGR_PCIXDEVICE_ERROR	26
WHEALOGR_PCIXDEVICE_WARNING	27
WHEALOGR_IPF_MCA_ERROR	38
WHEALOGR_IPF_MCA_WARNING	39
WHEALOGR_PCIE_NODEVICEID_ERROR	40
WHEALOGR_PCIE_NODEVICEID_WARNING	41
WHEALOGR_PCIBUS_NODEVICEID_ERROR	42
WHEALOGR_PCIBUS_NODEVICEID_WARNING	43
WHEALOGR_PCIXDEVICE_NODEVICEID_ERROR	44

WHEALOGR_PCIXDEVICE_NODEVICEID_WARNING	45
WHEALOGR_PLATFORM_MEMORY_NOTYPE_ERROR	46
WHEALOGR_PLATFORM_MEMORY_NOTYPE_WARNING	47

6.4.11 Endless Boot Support

If this feature was enabled, BIOS shall start to traverse all bootable devices constantly which are attached to the system. Particularly, it shall avoid entering in **EFI shell** or **BIOS SETUP** when BIOS tried to boot but failed for every device. However, during the period of endless loop, BIOS shall keep listening the hot key such as F2 or DEL to break the loop.

When this feature was disabled, it will show ***“Reboot and Select proper Boot device Or Insert Boot Media in selected Boot device and press a key”*** on the screen.

Be awarded that the LAN port which was dedicated to use by BMC was not included in Endless boot retry loop.

7. BMC

7.1 BMC overview in MiTAC CP2S11 1S Server (Capri V2)

The BMC firmware implements IPMI 2.0 based on AST2600 service processor. It performs all the BMC management tasks defined by IPMI 2.0 and, as a Service Processor, allows for remote monitoring using Serial Over LAN.

7.2 BMC Hardware Component in MiTAC CP2S11 1S Server (Capri V2)

Component	Size	Usage
Aspeed AST2600	NA	It's a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms.
DDR5 SDRAM	512MB	BMC memory
SPI flash	64MB	BMC Flash part includes BMC FW, user configuration, SEL and SDR.
EEPROM	8KB	FRU information
PHY NIC	10M/100M/1G	Dedicated for BMC

7.3 BMC Main Features

7.3.1 IPMI 2.0 Standard Features BMC Main Features

Feature	Description
System Interface support	• KCS • LAN(RMCP/RMCP+)
Text Console Redirection: SOL	• Support in IPMI stack for SOL to remotely access BIOS and text console before OS booting.
IPMI 2.0 based Management	• BMC stack with a full IPMI 2.0 implementation • Optional commands supported(refer to section 4.1.1) • OEM commands supported(refer to section 4.1.2 and section 5)
System Management	• System health monitoring. • System Power management • Fan speed monitor and control
Event Log and Alerting	• Read Log events • Sensor readings

	• SNMP traps
Remote Server Power Control	• Server's power status report • Support for remotely power-cycle, power-down, power-up, reset the server
Watchdog Timer Support	• Watchdog function that can generate interrupt or reset after zero count down
Sophisticated User Management	• IPMI based user management • Multiple user permission level • Extended security algorithms and cipher suites support

7.3.2 OEM features

Feature	Description
Management Network Interface	• BMC should have Shared-NIC uses RMII/NCSI interface for Out-of-Band access.
Port 80 POST	• BMC to support port 80 POST code display to drive 8 bit HEX GPIO and SOL • BMC should have access to POST code and record up to 256 POST codes.
FSC in BMC	• BMC should support FSC in both PID and step mode. BMC should support both In-Band and Out-of-Band FSC configuration update; updates should take effect immediately without reboot required. BMC should support FAN boost during fan failure. • Default fan PWM setting is 60% when power on by HW.
BIOS recovery	
UART port switch control	
Remote change BIOS boot mode/boot order	
Board ID	
FAB Revision ID	
Control Power and System Identification LED	
Auto BIOS Recovery	
Manual BIOS Copy	
Manual remote update BIOS	
Enable/Disable Auto BIOS recovery	
Get Dual BIOS feature status	
Get BIOS Version	
YAFU BMC/BIOS/CPLD remote update	
BMC web GUI	

7.4 Messaging interfaces

The BMC messaging interfaces comply with the IPMI 2.0 specification. The following interfaces are supported.

- Keyboard Controller Style (KCS) Host Interface – Chapter 9 of the IPMI 2.0 specification.
- LAN Interface – Chapter 13 of the IPMI 2.0 specification.
- IPMI Serial/Modem Interface – Chapter 14 of the IPMI 2.0 specification.

Channel	Interface
0h	IPMB
1h	LAN
3h	KCS
Fh	Host/SMS

6.4.1. KCS Interface

Capri V2 BMC provides one KCS interface for communication with host. The programmed address for KCS interface, data port is at CA2h and status port is at CA3h.

6.4.2. LAN Interface

Capri V2 BMC uses the NCSI side-band or dedicated network interface to provide support for IPMI messaging over LAN.

6.4.3. FRU ID Number

FRU Name	ID Number	I2C Bus	Slave Address	Support Command
Main Board FRU	0	7	A0h	1. Read/Write FRU Data 2. Master Write-Read

6.4.4. Ciphers and Keys Security implementation

All ciphers are supported by IPMI V.2.0 and disabled by default. There are only 2 ciphers (Cipher ID# 3, 8) at enabled status and all other ciphers will be at disable status by default. The detail ciphers table are listed below.

Cipher ID	Authentication Algorithm	Integrity Algorithm	Confidentiality Algorithm	Default Status
0	RAKP-none	None	None	Disable
1	RAKP-HMAC-SHA1	None	None	Disable
2	RAKP-HMAC-SHA1	HMAC-SHA1-96	None	Disable
3	RAKP-HMAC-SHA1	HMAC-SHA1-96	AES-CBC-128	Enable
6	RAKP-HMAC-MD5	None	None	Disable
7	RAKP-HMAC-MD5	HMAC-MD5-128	None	Disable

8	RAKP-HMAC-MD5	HMAC-MD5-128	AES-CBC-128	Enable
11	RAKP-HMAC-MD5	MD5-128	None	Disable
12	RAKP-HMAC-MD5	MD5-128	AES-CBC-128	Disable

7.5 BMC user account

Default user account as below table:

User ID	User Name	Password	Status	Default Privilege
1	[NULL]	[NULL]	Disable	Administrator
2	admin	admin	Enable	Administrator
3~10	Undefined	Undefined	Disable	Undefined

NOTE: Users need to modify the user password at first log-in.

7.6 Text console redirection – SOL (Serial over LAN)

Capri V2 BMC FW provides the support for text console redirection (SOL) to remotely access BIOS setup or text consoles that are available on the serial console of host system.

The firmware includes support for IPMI based SOL where the standard IPMI client like IPMITOOL can be used to establish a SOL session with the service processor.

The SOL default baud rate is setup by BMC flash part as 57600. BMC and uEFI will synch at the system booting POST stage.

7.7 Commands Support

Capri V2 BMC FW provides a fully-compliant IPMI 2.0 based management of the service processor.

All the mandatory requirements and commands in IPMI 2.0 are supported.

6.7.1. IPMI Global Commands

In addition to the mandatory criteria in IPMI 2.0 specification, Capri V2 BMC FW also supports many optional commands.

The following is a list of commands that currently support to the Capri V2 BMC firmware.

6.7.1.1. IPMI Global Commands

IPM Global Commands
Get Device ID
Cold Reset
Warm Reset
Get Self Test Results
Set ACPI Power State
Get ACPI Power State
Get Device GUID
Get NetFn Support
Get Command Support
Get Command Sub-function Support
Get Configurable
Get Configurable Command Sub-functions

6.7.1.2. BMC Watchdog Timer Commands

BMC Watchdog Timer Commands
Reset Watchdog Timer
Set Watchdog Timer
Get Watchdog Timer

6.7.1.3. IPMI Messaging Support Commands

IPMI Messaging Support Commands
Set BMC Global Enables
Get BMC Global Enables
Clear Message Flags
Get Message Flags
Enable Message Channel Receive
Get Message
Send Message
Read Event Message Buffer
Get System GUID
Get Channel Authentication Capabilities
Get Session Challenge
Activate Session
Set Session Privilege Level
Close Session
Get Session Info

Get AuthCode
Set Channel Access
Get Channel Access
Get Channel Info
Set Channel Security Keys
Set User Access
Get User Access
Set User Name
Get User Name
Set User Password
Master Write-Read
Get Channel Cipher Suites
Get System Interface Capabilities
Set System Info Parameters
Get System Info Parameters

6.7.1.4. RMCP+ Support and Payload Commands

RMCP+ Support and Payload Commands
Activate Payload
Deactivate Payload
Get Payload Activation Status
Get Payload Instance Info
Set User Payload Access
Get User Payload Access
Get Channel Payload Support
Get Channel Payload Version
Get Channel OEM Payload Info
Suspend/Resume Payload Encryption

6.7.1.5. Chassis Device Commands

Chassis Device Commands
Get Chassis Capabilities
Get Chassis Status
Chassis Control
Chassis Identify
Set Chassis Capabilities
Set Power Restore Policy – disable by default
Get System Restart Cause

Set System Boot Options
Get System Boot Options
Get POH Counter

6.7.1.6. Event Commands

Event Commands
Set Event Receiver
Get Event Receiver
Platform Event

6.7.1.7. PEF and Alerting Commands

PEF and Alerting Commands
Get PEF Capabilities
Arm PEF Postpone Timer
Set PEF Configuration Parameters
Get PEF Configuration Parameters
Set Last Processed Event ID
Get Last Processed Event ID
Alert Immediate
PET Acknowledge

6.7.1.8. Sensor Device Commands

Sensor Device Commands
Get Device SDR Info
Get Sensor Reading Factors
Set Sensor Hysteresis
Get Sensor Hysteresis
Set Sensor Threshold
Get Sensor Threshold
Set Sensor Event Enable
Get Sensor Event Enable
Re-arm Sensor Events
Get Sensor Event Status
Get Sensor Reading
Set Sensor Reading And Event Status
Set Sensor Type

6.7.1.9. FRU Inventory Area Info

FRU Device Commands
Get FRU Inventory Area Info
Read FRU Data
Write FRU Data

6.7.1.10. SDR Repository Device Commands

SDR Repository Device Commands
Get SDR Repository Info
Get SDR Repository Allocation Info
Reserve SDR Repository
Get SDR
Add SDR
Partial Add SDR
Delete SDR
Clear SDR Repository
Get SDR Repository Time
Enter SDR Repository Update Mode
Exit SDR Repository Update Mode
Run Initialization Agent

6.7.1.11. SEL Device Commands

SEL Device Commands
Get SEL Info
Get SEL Allocation Info
Reserve SEL
Get SEL Entry
Add SEL Entry
Partial Add SEL Entry
Clear SEL
Get SEL Time
Set SEL Time
Get SEL Time UTC Offset
Set SEL Time UTC Offset

6.7.1.12. IPMI LAN Commands

IPMI LAN Commands
Set LAN Configuration Parameters
Get LAN Configuration Parameters
Suspend BMC ARPs

6.7.1.13. SOL Commands

SOL Commands
Set Serial/Modem Configuration
Get Serial/Modem Configuration
SOL Activating
Set SOL Configuration Parameters
Get SOL Configuration Parameters

6.7.2. OEM command support

Except the Standard and optional commands, provide the system specific OEM commands that dedicated for Capri V2 system, below are all the OEM commands that available for Capri V2.

The following is a list of OEM commands that planning to support on the Capri V2 BMC firmware.

Command Set	Sub command	NetFn	CMD Code
FSC Command Set	Enter FSC Update Mode Command	30h	61h
	Exit FSC Update Mode Command	30h	62h
	Read FSC Profile Header Command	30h	63h
	Write FSC Profile Header Command	30h	64h
	Read FSC Profile Command	30h	65h
	Write FSC Profile Command	30h	66h
	Read Zone Control Setting Command	30h	67h
	Write Zone Control Setting Command	30h	68h
	Get PWM value Command	30h	69h
	Set PWM value Command	30h	70h
	Get the total number of PWM IDs Command	30h	71h
	Restore FSC Command	30h	72h
Auto BIOS Recovering command Set	Set Dual BIOS Mux Command	30h	43h
	Set Dual BIOS Recovery Command	30h	44h
	Get Dual BIOS Status Command	30h	45h
	Set Dual BIOS Version Obtain Command	30h	54h
	Get Dual BIOS Version Command	30h	50h
	Perform BIOS Recovery Command	30h	41h
	Perform BIOS Backup Command	30h	42h
	Get BIOS Flash Info	30h	55h
	Get BIOS Version Command	30h	83h
	Disable ARB Timer Command	3Ch	30h
Other OEM Command Set	Restore Factory Default Command	32h	66h

	Get 80 Port Record Command	30h	49h
	Set DIMM Information Command	30h	1Ch
	Get DIMM Information Command	30h	1Dh
	Set VR Monitor Enable Command	30h	D2h
	Get VR Monitor Enable Command	30h	D4h
	Get CPLD Information Command	3Ch	88h
	Set Network Sequence Command	30h	80h
	Get Network Sequence Command	30h	81h
	Replay SOL Buffer Command	30h	48h
	Set PPIN Command	30h	77h
	Get PPIN Command	30h	78h
	Set Preserve Configuration Command	32h	83h
	Get Preserve Configuration Command	32h	84h
	Set First Time BIOS Boot Flag Command	30h	40h
	Set PHY Reset Status Command	30h	30h
	Get PHY Reset Status Command	30h	31h
	Set GPIO Command	30h	E0h
	Get GPIO Command	30h	E1h
	Getting Multiple IPv6 IP Addresses command	32h	99h
	Get PIN	30h	DFh
	Get Board ID Command	3Ch	89h
	Get FAB Revision Command	3Ch	8Ah

6.7.2.1. Auto BIOS Recovering command Set

6.7.2.1.1. Set Dual BIOS Mux Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
43h	Set Dual BIOS Mux	Request: Byte 1 – 00h = Set SPI flash bus to Host CPU. 01h = Set SPI flash bus to BMC. Byte 2 – 01h = Select primary BIOS flash. 02h = Select backup BIOS flash. Response: Byte 1 – Completion code. 00h = Command Completed Normally. D5h = Command could not be executed, BIOS in post/setup mode. C0h = Node Busy. The previous operation	This command could not execution during BIOS post 、 BIOS setup menu and system reboot.

		not finished yet.	
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6.7.2.1.2. Set Dual BIOS Recovery Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
44h	Set Dual BIOS Recovery	Request: Byte 1 –Setting of Dual BIOS recovery 00h = Disable 01h = Enable. Response: Byte 1 – Completion code. 00h = Command Completed Normally.	Setting of enable/disable Auto BIOS Recovery after 1st time boot after a BIOS update

6.7.2.1.3. Get Dual BIOS Status Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
45h	Get Dual BIOS Status	Request: N/A Response: Byte 1 – Completion code. Byte 2 – Setting of Dual BIOS recovery 00h = Disabled 01h = Enabled. Byte 3 – 00h = SPI flash bus has been selected to CPU Host. 01h = SPI flash bus has been selected to BMC. Byte 4 – 01h = The primary flash has been selected. 02h = The backup flash has been selected.	The default Byte 2 = 0. The default Byte 3 = 0. The default Byte 4 = 1.

		Byte 5 – Recover/Backup status 00h = Nothing to happen 01h = Performing BIOS Recovery 02h = Performing BIOS Backup	
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6.7.2.1.4. Set Dual BIOS Version Obtain Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
54h	Set Dual BIOS Version Obtain	Request: N/A Response: Byte 1 – Completion code. D5h = Command could not be executed, BIOS in post/setup mode. C0h = Node Busy. The previous operation not finished yet.	Request BMC to read BIOS version from physical primary and backup SPI flash device, and save in BMC DRAM. Get dual BIOS version reads the same variable in BMC DRAM. <i>This command could not execution during BIOS post 、 BIOS setup menu and system reboot.</i> <i>If completion code is C0h, please wait for 15 seconds and try this command again.</i>

6.7.2.1.5. Get Dual BIOS Version Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
50h	Get Dual BIOS Version	Request: Byte 1– 01h = Get primary BIOS FW version. 02h = Get backup BIOS FW version. Response:	Read BIOS version of primary and backup image from BMC DRAM.

		Byte 1 – Completion code. 00h = Command Completed Normally. CBh = Requested Sensor, data, or record not present. CCh = Invalid data field in Request. 82h = Dual BIOS version not ready Byte 2:N – BIOS FW version(ASCII code) (LSB first)	
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6.7.2.1.6. Perform BIOS Recovery Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
41h	Perform BIOS Recovery	Request: Byte 1 – 72h ('r') Byte 2 – 65h ('e') Byte 3 – 63h ('c') Byte 4 – 6Fh ('o') Byte 5 – 76h ('v') Byte 6 – 65h ('e') Byte 7 – 72h ('r') Response: Byte 1 – Completion code. 00h = Command Completed Normally. C0h = Node Busy. The previous operation not finished yet. D5h = Command could not be executed, BIOS in post/setup mode.	Copy backup BIOS image to primary BIOS image. This command could not execution during BIOS post 、 BIOS setup menu and system reboot. Please send the below command to execute Global Reset after the recovery is done 'ipmitool power cycle'

6.7.2.1.7. Perform BIOS Backup Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
42h	Perform BIOS Backup	Request: Byte 1 – 62h ('b') Byte 2 – 61h ('a') Byte 3 – 63h ('c') Byte 4 – 6Bh ('k') Byte 5 – 75h ('u') Byte 6 – 70h ('p') Response: Byte 1 – Completion code. 00h = Command Completed Normally. C0h = Node Busy. The previous operation not finished yet. D5h = Command could not be executed, BIOS in post/setup mode	Copy primary BIOS image to backup BIOS image. This command could not execution during BIOS post 、 BIOS setup menu and system reboot. Please send the below command to execute Global Reset after the backup is done 'ipmitool power cycle'

6.7.2.1.8. Get BIOS Flash Info

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
55h	Get BIOS Flash Info	Request: Byte 1 – 00h = Primary BIOS SPI flash 01h = Backup BIOS SPI flash Response: Byte 1 – Completion code. 00h = Command Completed Normally. C0h = Node Busy. The previous operation not	Read BIOS SPI Flash JEDEC ID and status register

		finished yet. 82h = BIOS SPI flash info not ready. D5h = Command could not be executed, BIOS in post/setup mode. The below data can be respond while the BIOS flash info is ready in the BMC DRAM, Byte 2 – Manufactory ID Byte 3 – Memory type Byte 4 – Memory density/capacity Byte 5 – Status register	
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6.7.2.1.9. Get BIOS Version Command

Net Function = 30h (OEM)			
Code	Command	Request/Response Data	Description
83h	Get BIOS Version	Request: N/A Response: Byte 1 – Completion code. 00h = Command Completed Normally. CBh = Requested Sensor, data, or record not present. Byte 2:N – BIOS FW version (ASCII code)	Read BIOS version from BMC DRAM that BIOS passed to BMC during BIOS POST.

6.7.2.1.10. Disable ARB Timer Command

Net Function = 0x3C			
Code	Command	Request/Response Data	Description
0x30	Disable ARB Timer	Request: N/A Response: Byte[1] : Completion	This command only for BIOS. This command let BIOS to notify BMC to disable ARB timer. The disable conditions are as below:

		code	BIOS runs normally and BIOS will send a “disable ARB timer” command to BMC before boot to OS
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6.7.3. BIOS Boot option Command Set

6.7.3.1. Get BIOS Boot Option Status Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request/Response Data	Description
0x10	Get BIOS Boot Option Status.	Request: N/A Response: Byte 1 – Completion code. Byte 2 – Boot Option Changed Status. 00h = Boot sequence no change. 01h = Boot sequence has been changed.	This command only for BIOS.

6.7.3.2. Get BIOS Boot Option Counter Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x11	Get BIOS Boot Option Counter.	Request: N/A Response: Byte 1 – Completion code. Byte 2 – Counter Number.	Byte 2 – 0: BIOS Boot Option Data is empty in BMC. This OEM command only for software tool and BIOS.

6.7.3.3. Get BIOS Boot Order Command

Net Function = Net Function = 30h (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x53	Get BIOS Boot Order	Request: Byte 1 – Set reading status. 0: first data reading. 1: To be continued. Response: Byte 1 – Completion code. Byte 2 – Data readable status. 0: Last batch. 1: Remaining. Byte 3 – Index Number.	This OEM command only for software tool and BIOS.

Net Function = Net Function = 30h (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
		Byte 4: 5 – Option Number (LSB first). Byte 6: 9 – Attribute (LSB first). Byte 10 – Device Type. Byte 11:74 – Option Name String (64Byte).	

6.7.3.4. Set BIOS Boot Order Command

Net Function = Net Function = 30h (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x52	Set BIOS Boot Order	Request: Byte 1 – Set writing status. 0: first data writing. 1: To be continued. Byte 2 – Index Number. Byte 3: 4 – Option Number (LSB first). Byte 5: 8 – Attribute (LSB first). Byte 9 – Device Type. Byte 10:73 – Option Name String.(64Byte) Response: Byte 1 – Completion code.	This OEM command only for software tool and BIOS.

6.7.3.5. Set BIOS Boot Option Status Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x14	Set BIOS Boot Option Status.	Request: Byte 1 – Boot Option Changed Status. 00h = Boot sequence no change. 01h = Boot sequence has been changed. Response: Byte 1 – Completion code.	This command only for software tool.

6.7.3.6. Set BIOS Boot Mode Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x15	Set BIOS Boot Mode	Request: Byte 1 – 0x00 = UEFI mode. 0x01 = Legacy mode. Byte 2 – 0x00 = Setting by uEFI.	This OEM command only for software tool and BIOS.

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
		– 0x01 = Setting by tool. Response: Byte 1 – Completion code.	

6.7.3.7. Get BIOS Boot Mode Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x16	Get BIOS Boot Mode	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 0x00 = UEFI mode. 0x01 = Legacy mode.	

6.7.3.8. Get BIOS Boot Mode Status Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x17	Get BIOS Boot Mode Status.	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 0x00 = No change. 0x01 = The boot mode has been changed by software tool.	

6.7.3.9. Clean BIOS Boot Mode Status Command

Net Function = 0x3C (OEM)			
Code	Command	Request, Response Data	Description
0x18	Clean BIOS Boot Mode Status.	Request: N/A Response: Byte 1 – Completion code.	<i>This OEM command only for BIOS.</i>

6.7.4. Other OEM Command Set

6.7.4.1. Restore Factory Default Command

Net Function = 32h (OEM)			
Code	Command	Request, Response Data	Description
66h	Restore Factory Default	Request: NA	When send this command to BMC, the LAN Configuration Parameters will be changed current setting value to default value

Net Function = 32h (OEM)			
Code	Command	Request, Response Data	Description
		Responses: Byte 1 – Completion code.	as following: IP Address Source = 0x00(DHCP) The Network sequence priority default is dedicated LAN for PVT/MP. The MEZZ protocol priority default is NCSI for PVT/MP. User IDs (User/Password/Privilege/Channels). Debug Console Serial Parameters. Product Information - Product ID. - Manufacturer ID Remove all the special settings such as different priority, but SEL will not remove. (Note: The BMC will reset itself after restore to default.)

6.7.4.1.1. Set Over Current Detect Command

Net Function = 3Ch (OEM)			
Code	Command	Request, Response Data	Description
6Ah	Set Over Current Detect Command	Request: Byte 1 – 00h = Disable Over Current Detect. 01h = Enable Over Current Detect Response: Byte 1 – Completion code.	Change setting of current based FM_OC_DETECT_EN_N. This OEM command only for BIOS.

6.7.4.1.2. Get Over Current Detect Command

Net Function = 3Ch (OEM)			
Code	Command	Request, Response Data	Description
6Bh	Get Over Current Detect Command	Request: N/A Response: Byte 1 – Completion code.	Read setting of current based FM_OC_DETECT_EN_N. The Over Current Detect default is disable (FM_OC_DETECT_EN_N = high).

Net Function = 3Ch (OEM)			
Code	Command	Request, Response Data	Description
		Byte 2 – 00h = Disable Over Current Detect. 01h = Enable Over Current Detect.	

6.7.4.1.3. Get 80 Port Record Command

Net Function = 30h (OEM)			
Code	Command	Request, Response Data	Description
49h	Get 80 Port Record	Request: N/A Response: Byte 1 – Completion code. Byte 2:N – POST code.	Replay the last port 80 POST codes (up to 256x POST records). N: maximum number = 256

6.7.4.1.4. Set DIMM Information Command

Net Function = 0x30 (OEM)			
Code	Command	Request, Response Data	Description
0x1C	Set DIMM Information	Request: Byte 1:N – All DIMM information. Response: Byte 1 – Completion code.	Write DIMM type to BMC by BIOS. <i>This OEM command only for BIOS.</i>

6.7.4.1.5. Get DIMM Information Command

Net Function = 30h (OEM)			
Code	Command	Request, Response Data	Description
1Dh	Get DIMM Information	Request: N/A Response: Byte 1 – Completion code. Byte 2:N – All DIMM information.	Read DIMM Type from BMC.

6.7.4.1.6. Get VR FW Version

Net Function = 30h (OEM)			
Code	Command	Request, Response Data	Description
51h	Get VR FW Version	Request: Byte 1 – The VR controller desired 00: CPU0 VR 01: CPU1 VR 02: CPU0 DIMM0 VR 03: CPU0 DIMM1 VR 04: CPU1 DIMM0 VR 05: CPU1 DIMM1 VR Response: Byte 1 – Completion code. Byte 2:5 – VR checksum (LSB first)	BMC can provide the NVM Checksum stored in the BMC DRAM for the specific VR controller.

6.7.4.1.7. Store VR version To BMC

Net Function = 30h (OEM)			
Code	Command	Request, Response Data	Description
D3h	Store VR version To BMC	Request: N/A Response: Byte 1 – Completion code.	While the command is executed, BMC can send MFR_SERIAL (9EH) PMBUS command to obtain NVM checksums for all the VR controllers and store them into the BMC DRAM.

6.7.4.1.8. Set VR Monitor Enable Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
D2h	Set VR Monitor Enable	Request: Byte 1 – 00h = Disable BMC to get VRD related sensor information 01h = Enable BMC to get VRD related sensor information.(Default) Response:	Change setting of enable/disable CPU Vcore and memory VDDQ VR sensor polling. This OEM command only for update VRD tool

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
		Byte 1 – Completion code.	

6.7.4.1.9. Get VR Monitor Enable Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
D4h	Get VR Monitor Enable	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 0 = Disable BMC to get VRD related sensor information 1 = Enable BMC to get VRD related sensor information.(Default)	Read setting of enable/disable CPU Vcore and memory VDDQ VR sensor polling. The VR monitor default setting is enabling.

6.7.4.1.10. Set First Time BIOS Boot Flag Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
40h	Set First Time BIOS Boot Flag	Request: Byte 1 – 01h = Set First Time BIOS Boot Flag Response: Byte 1 – Completion code.	For inband BIOS update utility to set flag for first time boot after an inband BIOS update action.

6.7.4.1.11. Set Preserve Configuration Command

Net Function = 32h (OEM)			
Code	Command	Request/ Response Data	Description
83h	Set Preserve Configuration	Request: Byte 1 – Selector Byte 2 – 0 = Disable 1 = Enable Response: Byte 1 – Completion code.	Set BMC configuration to be preserved or not after BMC FW update. This command is for YAFU flash update tool.

6.7.4.1.12. Get Preserve Configuration Command

Net Function = 32h (OEM)			
Code	Command	Request/ Response Data	Description
84h	Get Preserve Configuration	Request: Byte 1 – Selector Response: Byte 1 – Completion code. Byte 2 – 00h = Disable 01h = Enable	

6.7.4.1.13. Get CPLD Information Command

Net Function = 3Ch (OEM)			
Code	Command	Request/ Response Data	Description
88h	Get CPLD Information	Request: N/A Response: Byte 1 – Completion code. Byte 2 – CPLD version number. Byte 3:6 – Device ID(LSB first). Byte 7:10 – Checksum(LSB first).	Get CPLD version via CPLD SGPIO by BMC. Get CPLD Device ID via JTAG interface by BMC.

6.7.4.1.14. Set Network Sequence Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
80h	Set Network Sequence	Request: Byte 1 – 00h = Dedicated LAN is priority 1. OCP card is priority 2. 01h = OCP card is priority 1. Dedicated LAN is priority 2. Response: Byte 1 – Completion code.	Change setting of OOB interface priority between dedicated LAN and OCP card. BMC will apply the new priority at next AC reset or cold reset The default setting as following: Dedicated LAN is priority 1 OCP card is priority 2.

6.7.4.1.15. Get Network Sequence Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
81h	Get Network Sequence	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 00h = Dedicated LAN is priority 1. OCP card is priority 2. 01h = OCP card is priority 1. Dedicated LAN is priority 2.	Read setting of OOB interface priority. The Network sequence priority default is dedicated LAN (Byte 2 = 0).

6.7.4.1.16. Replay SOL Buffer Command

Net Function = 30h			
Code	Command	Request/ Response Data	Description
48h	Replay SOL Buffer	Request: N/A Response: Byte 1 – Completion code.	Replay last 16KB of SOL screen in SOL console. Use this command can display 5x last frames buffer when SOL session is connecting.

6.7.4.1.17. Set PPIN Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
77h	Set PPIN	Request: Byte 1 – CPU number (CPU#0: 00h, CPU#1: 01h) Byte 2-9 –VALUE-The 64 bit (bit 63:0) inventory number (MS-byte first). Response: Byte 1 – Completion code.	BMC would pull the SMI signal to low after BMC reset; BIOS shall serve the request by using This command to write PPIN of CPU0 and CPU1 to BMC. BIOS also Set_PPIN when BIOS POST COMPLETE. This OEM command only for BIOS.

6.7.4.1.18. Get PPIN Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
78h	Get PPIN	Request: Byte 1 – CPU number (CPU#0: 00h, CPU#1: 01h) Response: Byte 1 – Completion code. Byte 2:9 – VALUE-The 64 bit (bit 63:0) inventory number (MS-byte first).	Read PPIN from BMC. BMC default provides 0xFFFFFFFFFFFFFFF for CPU 0/1.

6.7.4.1.19. Set PHY Reset Status Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
30h	Set PHY Reset Status	Request: Byte 1 – 00h = Disable PHY reset. 01h = Enable PHY reset. Response: Byte 1 – Completion code.	Change setting to enable/disable shared NIC PHY reset of all shared NICs during system warm reboot and DC cycle. This default setting is 0.

6.7.4.1.20. Get PHY Reset Status Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
31h	Get PHY Reset Status	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 00h = Disable PHY reset. 01h = Enable PHY reset.	Read setting of keep NIC PHY link up feature of all shared NICs. This default setting is 0.

6.7.4.1.21. Set GPIO Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
E0h	Set GPIO	Request: Byte 1 – GPIO number(GPIOA0=0, GPIOA1=1, GPIOA2=2,...GPIOA7=7, GPIOB0=8.....GPIOZ7=0xCF,GPIOAA0=0xD0..GPIOAB7=0xDF) Byte 2 – 00h = Config to GPO. 01h = Config to GPI. Byte 3 – output value for GPO Response: Byte 1 – Completion code	Set GPIO status

6.7.4.1.22. Get GPIO Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
E1h	Get GPIO	Request: Byte 1 – GPIO number(GPIOA0=0, GPIOA1=1, GPIOA2=2,...GPIOA7=7, GPIOB0=8.....GPIOZ7=0xCF,GPIOAA0=0xD0..GPIOAB7=0xDF) Response: Byte 1 – Completion code. Byte 2 – 00h = Config to GPO. 01h = Config to GPI. Byte 3 – GPIO value.	Read GPIO status.

6.7.4.1.23. Get PIN Command

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
DFh	Get PIN	Request: Byte 1:2 –Duration time (LSB first), resolution of 0.1s. Response:	Read average PIN in any duration between 0.1 to 60 seconds

Net Function = 30h (OEM)			
Code	Command	Request/ Response Data	Description
		Byte 1 – Completion code.	
		Byte 2:3 –Average power (LSB first), resolution of 0.1W.	

6.7.4.1.24. Get Board ID Command

Net Function = 3Ch (OEM)			
Code	Command	Request/ Response Data	Description
89h	Get Board ID	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 09h = SKU1 0ah = SKU2 0bh = SKU3 0ch = SKU4	Read Board SKU ID pin status

6.7.4.1.25. Get FAB Revision ID Command

Net Function = 3Ch (OEM)			
Code	Command	Request/ Response Data	Description
8Ah	Get FAB Revision ID	Request: N/A Response: Byte 1 – Completion code. Byte 2 – 00h = R0A 01h = R0B 02h = R0C 04h = R0D 05h = R0E	Read Board REV ID pin status

Net Function = 3Ch (OEM)			
Code	Command	Request/ Response Data	Description
		06h = R0F 07h = R0G	

6.7.5. Standard IPMI Option Command Support

6.7.5.1.1. Chassis Identify command

This command causes the chassis to physically identify itself by a mechanism chosen by the system implementation. Unless the optional “Force Identify On” capability is supported and used, the *Chassis Identify* command automatically times out.

Request/ Response Data
Request: Byte 1: [7:0] - Identify Interval in seconds. 1-based. Timing accuracy = -0/+20%. This field is optional. If this byte is not provided the default timeout shall be 15 seconds -0/+20%. Note that this byte can be overridden by optional byte 2. 00h = Turn off Identify Byte 2: Force Identify On. This optional field enables software to command the Identify to be On indefinitely. The BMC implementation should return an error completion code if this byte is not supported. [7:1] - reserved [0] - 1b = Turn on Identify indefinitely. This overrides the values in byte 1. 0b = Identify state driven according to byte 1.
Response: Byte[1] : Completion code

7.8 Monitoring

6.8.1. Sensors

The Table below shows the IPMI sensors monitored on the Capri V2 by the AST2600 BMC. Details of these sensor connections are described in the following sections. The following thresholds are defined by the IPMI2.0 specification

6.8.1.1. Sensor List

Sensor Name	Sensor Number ^[1]	Sensor Type ^[2]	Sensor Reading Type ^[3]	Sensor Record Type ^[3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event ^[6]
Threshold Sensors								
CPU_TEMP	01h	01H	01H	01H	20H	03H	00H	UC
HSC_TEMP	0Fh	01H	01H	01H	20H	07H	00H	UC
PDB_HSC_TEMP	4Fh	01H	01H	01H	20H	07H	00H	UC
DIMM_A_TEMP	10h	01H	01H	01H	20H	08H	00H	UC
DIMM_B_TEMP	11h	01H	01H	01H	20H	08H	00H	UC
DIMM_C_TEMP	12h	01H	01H	01H	20H	08H	00H	UC
DIMM_E_TEMP	14h	01H	01H	01H	20H	08H	00H	UC
DIMM_G_TEMP	16h	01H	01H	01H	20H	08H	00H	UC
DIMM_H_TEMP	17h	01H	01H	01H	20H	08H	00H	UC
DIMM_I_TEMP	18h	01H	01H	01H	20H	08H	00H	UC
DIMM_K_TEMP	1ah	01H	01H	01H	20H	08H	00H	UC
SYS_FAN0	63h	04H	01H	01H	20H	1DH	01H	LC
SYS_FAN1	64h	04H	01H	01H	20H	1DH	01H	LC
HSC_PIN	90h	08H	01H	01H	20H	07H	00H	UC
HSC_VIN	91h	02H	01H	01H	20H	07H	00H	LC,UC
HSC_IOUT	92h	03H	01H	01H	20H	07H	00H	UC
PDB_RT1_TEMP	41h	01H	01H	01H	20H	07H	00H	UC
PDB_HSC_PIN	98h	08H	01H	01H	20H	07H	00H	UC
PDB_HSC_VIN	96h	02H	01H	01H	20H	07H	00H	LC,UC
PDB_HSC_IOUT	97h	03H	01H	01H	20H	07H	00H	UC
SOC_VIN	94h	02H	01H	01H	20H	07H	00H	LC,UC
SOC_VOUT	95h	02H	01H	01H	20H	07H	00H	LC,UC
SYS_Air_Inlet	30h	01H	01H	01H	20H	07H	00H	UC
SYS_Air_Outlet	32h	01H	01H	01H	20H	07H	00H	UC
M2_Inlet	31h	01H	01H	01H	20H	07H	00H	UC
OCP_NIC_TEMP	38h	01H	01H	01H	20H	07H	00H	UC
E1S_BP_TEMP1	4dh	01H	01H	01H	20H	07H	00H	UC
E1S_BP_TEMP2	4eh	01H	01H	01H	20H	07H	00H	UC
RISER_3_TEMP	49h	01H	01H	01H	20H	07H	00H	UC
E1S_SSD_TEMP1	34h	01H	01H	01H	20H	07H	00H	UC
E1S_SSD_TEMP2	35h	01H	01H	01H	20H	07H	00H	UC
E1S_SSD_TEMP3	36h	01H	01H	01H	20H	07H	00H	UC

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
E1S_SSD_TEMP4	37h	01H	01H	01H	20H	07H	00H	UC
VR_VDDR_SOC	48h	01H	01H	01H	20H	07H	00H	UC
VR_VDD_11_SUS	33h	01H	01H	01H	20H	07H	00H	UC
VR_VDDCR_0	45h	01H	01H	01H	20H	07H	00H	UC
VR_VDDCR_1	46h	01H	01H	01H	20H	07H	00H	UC
VDDIO	47h	01H	01H	01H	20H	07H	00H	UC
M2_SSD_TEMP1	3Ah	01H	01H	01H	20H	07H	00H	UC
M2_SSD_TEMP2	3Bh	01H	01H	01H	20H	07H	00H	UC
GPU_PCIE1_TEMP	4Ah	01H	01H	01H	20H	07H	00H	UC
GPU_PCIE2_TEMP	4Bh	01H	01H	01H	20H	07H	00H	UC
GPU_PCIE3_TEMP	4Ch	01H	01H	01H	20H	07H	00H	UC
CPU_CORE0	50h	02H	01H	01H	20H	07H	00H	LC,UC
CPU_VDDIO	51h	02H	01H	01H	20H	07H	00H	LC,UC
CPU_SOC	52h	02H	01H	01H	20H	07H	00H	LC,UC
CPU_11_SUS	53h	02H	01H	01H	20H	07H	00H	LC,UC
CPU_CORE1	54h	02H	01H	01H	20H	07H	00H	LC,UC
CPU_33_DUAL	55h	02H	01H	01H	20H	07H	00H	LC,UC
VBAT	57h	02H	01H	01H	20H	07H	00H	LC,UC
P12V_STBY	59h	02H	01H	01H	20H	07H	00H	LC,UC
VDD_5_RUN	5Ah	02H	01H	01H	20H	07H	00H	LC,UC
VDD_33_RUN	5Bh	02H	01H	01H	20H	07H	00H	LC,UC
VDD_33_DUAL	5Ch	02H	01H	01H	20H	07H	00H	LC,UC
CPU_18_DUAL	5Dh	02H	01H	01H	20H	07H	00H	LC,UC
Discrete Sensors								
POST Error	2BH	0FH	6FH	03H	01H	22H	00H	Event Data1: [7:6] 10b or 11b [5:4] 10b [3:0] Offset 0x00 (System Firmware Error) Event Data2: ED1[7:6]= 10b, LSB of POST Error Code. ED1[7:6]= 11b, Per IPMI Spec. Event Data3: MSB of POST Error Code

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
HSC_Status_Low	C1h	0BH	6FH	02H	20H	14H	00H	[0]=1b, NONEABOVE_STATUS [1]=1b, CML_FAULT [2]=1b, TEMP_FAULT [3]=1b, VIN UV FAULT [4]=1b, IOUT OC FAULT [5]=1b, VOUT OV FAULT [6]=1b, HOTSWAP_OFF [7]=1b, BUSY
HSC_Status_High	C2h	0BH	6FH	02H	20H	14H	01H	[0]=1b, Unknown [1]=1b, Other [2]=1b, Fans [3]=1b, Power Good [4]=1b, MFR Specific [5]=1b, Input [6]=1b, Iout/Pout [7]=1b, Vout
PDB_HSC_Status_L	C3h	Other Units-based Sensor 0BH	6FH	02H	20H	14H	00H	[0]=1b, NONEABOVE_STATUS [1]=1b, CML_FAULT [2]=1b, TEMP_FAULT [3]=1b, VIN UV FAULT [4]=1b, IOUT OC FAULT [5]=1b, VOUT OV FAULT [6]=1b, HOTSWAP_OFF [7]=1b, BUSY
PDB_HSC_Status_H	C4h	0BH	6FH	02H	20H	14H	01H	[0]=1b, Unknown [1]=1b, Other [2]=1b, Fans [3]=1b, Power Good [4]=1b, MFR Specific [5]=1b, Input [6]=1b, Iout/Pout [7]=1b, Vout
DCMI Watchdog	60H	23H	6FH	02H	20H	D0H	01H	[0]=1b, Timer expired [1]=1b, Hard Reset [2]=1b, Power Down [3]=1b, Power Cycle [8]=1b, Timer interrupt
SEL Status	61H	10H	6FH	02H	20H	D0H	00H	02h, SEL Clear
Power Unit State	70H	09H	6Fh	03H	20H	0AH	00H	04h - AC lost.
System Event	80H	12H	6Fh	03H	20H	07H	00H	Event Data1: E5h = Timestamp Clock sync: if ED1 = 01h: BIOS POST complete Event Data2: if ED1 = E5h: 0x00: event is first of pair 0x80: event is second of if ED1 = 01h: FFh

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Sys restart	82H	1DH	6FH	03H	20H	07H	00H	07h - System Restart. Event Data 2 and Event Data 3 must follow IPMI specification with the following Get System Restart Cause offsets
Button	AAh	14H	6FH	03H	20H	07H	00H	Event Data1: [7:4] 0h [3:0] 0h: Power button pressed 2h: Reset button pressed Event Data2: FFh - Not Used Event Data3: FFh - Not Used
ACPI_Power_State	ABH	22H	6Fh	03H	20H	07H	00H	Event Data1: [7:4]=0000b [3:0]= 0h - S0/G0 "working" 5h - S5/G2 "soft-off"

Note:

Refer to IPMI 2.0 Table 43-1 byte 8

Refer to IPMI 2.0 Table 43-1 byte 13

Refer to IPMI 2.0 Table 43-1 byte 14

Refer to IPMI 2.0 Table 43-1 byte 9

Refer to IPMI 2.0 Table 43-1 byte 9

Refer to IPMI 2.0 Table 43-1 byte 15~20

Enabled condition: 0. Always Enable

1. Power on
2. BIOS sets SPD MUX to BMC
3. CPU is present
4. DIMM# is present

Capri V2 sensor for Event-Only Sensors

Sensor Name	Sensor Number	Generator ID	Assertion Event
POST Error	0x2B	0x0001	Event Data1: [7:6] 10b or 11b [5:4] 10b [3:0] Offset 0x00 (System Firmware Error) Event Data2: ED1[7:6]= 10b, LSB of POST Error Code. ED1[7:6]= 11b, Per IPMI Spec. Event Data3: MSB of POST Error Code
Machine Chk Err	0x40	0x0001	Event Data1: [7:6]=10b [5:4]=10b [3:0]=0Bh, Uncorrectable Or 0Ch, Correctable Event Data2: Machine Check bank Number (Any one of 0 to 21) Event Data3: [7:5] CPU Number [4:0] Core Number

PCIe Error	0x41	0x0001	Event Data1: [7:6]=10b [5:4]=10b [3:0]= 04h = PCI PERR 05h = PCI SERR 07h, correctable 08h, uncorrectable 0Ah, Bus Fatal Event Data2: [7:3] Device Number [2:0] Func Number Event Data3: [7:0] Bus No
Other IIO Err	0x43	0x0001	Event Data1: [7:6] 10b [5:4] 10b [3:0] Offset 0x00 (Other IIO) Event Data2: [7:0] Error ID [Refer to Haswell EDS Vol1 Sec 11.1.7 IIO module error codes] Event Data3: [7:5] CPU Number [4:3] Reserved [2:0] Source 000b = IRP0 001b = IRP1 010b = IIO-Core 011b = VT-d 100b = Intel Quick data 101b = Misc Others = Reserved

Power Error	0x56	0x0020	Event Data1: [7:6]=00b [5:4]=00b [3:0]=Event offset: 01h, SYS_PWROK Failure Event Data2: FFh - Not Used Event Data3: FFh - Not Used
Memory Error	0x00	0x0021	Event Data1: [7:6] 10b – OEM Code in Byte2 [5:4] 10b – OEM Code in Byte3 [3:0] Sensor-Specific offset 00h – Correctable ECC 01h – Uncorrectable ECC 04h – Memory device disabled Event Data2: If ED1 = A0h or A1h ED2 [7:0] 00h: Memory type is ECC 10h: Memory type is parity 20h: Memory type is CRC If ED1= A4h ED2 [7:0] Reserved. Event Data3: [7:4] DIMM Channel (*1, see below) [3:0] Reserved.
Software NMI	0x90	0x0001	Event Data1: [7:6] 00b – Unspecified byte2 [5:4] 00b – Unspecified byte3 [3:0] 03h – Software NMI Event Data2: FFh - Not Used Event Data3: FFh - Not Used
CMOS Clear	0xC7	0x0001	Event Data1: [7:0] 01b – Assert Event Data2: FFh - Not Used Event Data3: FFh - Not Used
Button	0xAA	0x0020	Event Data1: [7:4] 0h [3:0] 0h: Power button pressed 2h: Reset button pressed Event Data2: FFh - Not Used Event Data3: FFh - Not Used

Power State	0xAB	0x0020	Event Data1: [7:4] 0h [3:0] 0h: Transition to running 2h: Transition to power off Event Data2: FFh - Not Used Event Data3: FFh - Not Used
Power Policy	0xAC	0x0020	Event Data1: [7:6]=00b [5:4]=00b [3:0]=Event offset: 05h: Soft-power control failure Event Data2: FFh - Not Used Event Data3: FFh - Not Used
Network Status	0xB1	0x0020	Event Data1: [7:6]=00b [5:4]=00b [3:0]=Event offset: 00h, After BMC has IP assigned, and Both IPv4 and IPv6 network cannot ping gateway. BMC in disconnection state 01h, Either IPv4 or IPv6 can ping gateway after disconnection state Event Data2: FFh - Not Used Event Data3: FFh - Not Used

System Event	0xE9	0x0020	Event Data1: [7:0]=E5h, Timestamp Clock synch. [7:0]=C4h, PEF Action. Event Data2: if ED1 = E5h: 0x00: event is first of pair 0x80: event is second of pair if ED1 = C4h: 0x1: PEF Action Event Data3: if ED1 = E5h: Cause of time changed: 00h: NTP 01h: Host RTC 02h: Set SEL time command 03h: Set SEL time UTC offset Command FFh: Unknown if ED1 = C4h: FFh
Critical IRQ	0xEA	0x0020	Event Data1: 00h, Front Panel NMI / Diagnostic Interrupt Event Data2: FFh - Not Used Event Data3: FFh - Not Used

Dual BIOS Up Sts	0xEF	0x0020	Event Data1: 01h: Auto Recovery 02h: Manual Recovery 03h: OOB Directly Event Data2: if ED1 = 01h 01h: ARB Timer timeout 02h: BIOS Good de-assert (GPIOAA5) if ED1 = 02h 03h: Recovery from Gold to primary 04h: Recovery from Primary to Gold if ED1 = 03h 05h: Primary directly 06h: Gold directly Event Data3: if ED2 = 01h or 02h 01h: Start the progress for recovery 02h: End the progress for recovery
			Event Data1: 00h Primary flash booting fail.
ABR ERR	0x89	0x0020	

*1: Instance to Mainboard DIMM channel Mapping

Instance ID	DIMM Channel / Event Data 3
00h (UMC0)	DIMM A / 00h
10h (UMC1)	DIMM B / 10h
20h (UMC2)	DIMM D / 30h
30h (UMC3)	DIMM C / 20h
40h (UMC4)	DIMM H / 70h
50h (UMC5)	DIMM G / 60h
60h (UMC6)	DIMM E / 40h
70h (UMC7)	DIMM F / 50h

OEM event log #1 definition for BIOS post code for ABR sensor (0x89) log when ABR ERR trigger

Byte	Field	Description
1	Record ID	ID used for SEL Record access.
2		
3	Record Type	0xE0
4	Generator	0x20
5		
6	Sensor Number	0x89
7	Latest BIOS Post code#1	xx
8	Latest BIOS Post code#2	xx
9	Latest BIOS Post code#3	xx
10	Latest BIOS Post code#4	xx
11	Latest BIOS Post code#5	xx
12	Latest BIOS Post code#6	xx
13	Latest BIOS Post code#7	xx
14	Latest BIOS Post code#8	xx
15	Latest BIOS Post code#9	xx
16	Latest BIOS Post code#10	Xx

Byte	Field	Description
1	Record ID	ID used for SEL Record access.
2		
3	Record Type	0xE0
4	Generator	0x20
5		
6	Sensor Number	0x89
7	Latest BIOS Post code#11	xx
8	Latest BIOS Post code#12	xx
9	Latest BIOS Post code#13	xx
10	Latest BIOS Post code#14	xx
11	Latest BIOS Post code#15	xx
12	Latest BIOS Post code#16	xx
13	Latest BIOS Post code#17	xx

14	Latest BIOS Post code#18	xx
15	Latest BIOS Post code#19	xx
16	Latest BIOS Post code#20	xx

The definition of Event Data 2/3 for Dual BIOS Up Sts (EFh) SEL

Event Data 2	Event Data 3
if ED1 = 01h	if ED2 = 01h or 02h
01h: FRB2 WDT timeout	01h: Start the progress for recovery
02h: BIOS Good de-assert (GPION2)	02h: End the progress for recovery
07h: Watchdog not enable	03h: Checksum compare failed
	04h: Primary BIOS is not present
if ED1 = 02h	05h: Gold BIOS is not present
03h: Recovery from Gold to Primary	
04h: Recovery from Primary to Gold	
if ED1 = 03h	
05h: Primary directly	
06h: Gold directly	
if ED1 = 04h	
08h: BMC Self test failed	
09h: Unexpected power off	
0Ah: BMC ready pin deassert (GPIOQ4)	

If ED1 = 05h	
03h: Recovery from Gold to Primary	

6.8.1.2. Threshold Table for analog Sensors (Raw Reading)

BMC has access to all analog sensors on Capri V2 directly or through PCH Management Engine. All analog sensors need to be displayed in sensor data record (SDR) repository. Currently, some values are setup as the min/max values and will be provided later when it is available.

IPMI 2.0 Thresholds Specification

Term	Full Name	Description
LNR	Lower non-recoverable	Anything below causes power down
LC	Lower critical	Below this point , the shelf will take action
LNC	Lower non-critical	Above this point is the normal operating point
UNC	Upper non-critical	below this point is the normal operating point
UC	Upper critical	above this point the shelf will take action
UNR	Upper non-recoverable	anything above causes power down

Threshold Table for analog Sensors

Sensor Description	Sensor No.	LNR	LC (raw data)	LC (real value)	LNC	UNC	UC (raw data)	UC (real value)	UNR	Formula[1]
CPU_TEMP	01h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
HSC_TEMP	0Fh	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
DIMM_A_TEMP	10h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_B_TEMP	11h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_C_TEMP	12h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_E_TEMP	14h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_G_TEMP	16h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_H_TEMP	17h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_I_TEMP	18h	NA	NA	NA	NA	NA	0x55	85	NA	y=x
DIMM_K_TEMP	1Ah	NA	NA	NA	NA	NA	0x55	85	NA	y=x
SYS_Air_Inlet	30h	NA	NA	NA	NA	NA	0x32	50	NA	y=x
M2_Inlet	31h	NA	NA	NA	NA	NA	0x32	50	NA	y=x
SYS_Air_Outlet	32h	NA	NA	NA	NA	NA	0x32	50	NA	y=x
VR_VDD_11_SUS	33h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
E1S_SSD_TEMP1	34h	NA	NA	NA	NA	NA	0x4d	77	NA	y=x

Sensor Description	Sensor No.	LNR	LC (raw data)	LC (real value)	LNC	UNC	UC (raw data)	UC (real value)	UNR	Formula[1]
E1S_SSD_TEMP2	35h	NA	NA	NA	NA	NA	0x4d	77	NA	y=x
E1S_SSD_TEMP3	36h	NA	NA	NA	NA	NA	0x4d	77	NA	y=x
E1S_SSD_TEMP4	37h	NA	NA	NA	NA	NA	0x4d	77	NA	y=x
OCP_NIC_TEMP	38h	NA	NA	NA	NA	NA	0x5a	90	NA	y=x
M2_SSD_TEMP1	3Ah	NA	NA	NA	NA	NA	0x4c	76	NA	y=x
M2_SSD_TEMP2	3Bh	NA	NA	NA	NA	NA	0x4c	76	NA	y=x
PDB_RT1_TEMP	41h	NA	NA	NA	NA	NA	0x5a	90	NA	y=x
VR_VDDCR_0	45h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
VR_VDDCR_1	46h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
VDDIO	47h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
VR_VDDR_SOC	48h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
RISER_3_TEMP	49h	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
GPU_PCIE1_TEMP	4Ah	NA	NA	NA	NA	NA	0x55	85	NA	y=x
GPU_PCIE2_TEMP	4Bh	NA	NA	NA	NA	NA	0x55	85	NA	y=x
GPU_PCIE3_TEMP	4Ch	NA	NA	NA	NA	NA	0x55	85	NA	y=x
E1S_BP_TEMP1	4Dh	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
E1S_BP_TEMP2	4Eh	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
PDB_HSC_TEMP	4Fh	NA	NA	NA	NA	NA	0x5f	95	NA	y=x
CPU_CORE0	50h	NA	0x28	0.448	NA	NA	0xe0	2.509	NA	y=0.0112x
CPU_VDDIO	51h	NA	0x55	0.833	NA	NA	0x87	1.323	NA	y=0.0098x
CPU_SOC	52h	NA	0x3e	0.608	NA	NA	0x9a	1.509	NA	y=0.0098x
CPU_11_SUS	53h	NA	0x59	0.872	NA	NA	0x8c	1.372	NA	y=0.0098x
CPU_CORE1	54h	NA	0x28	0.448	NA	NA	0xe0	2.509	NA	y=0.0112x
CPU_33_DUAL	55h	NA	0x8f	2.788	NA	NA	0xba	3.627	NA	y=0.0195x
VBAT	57h	NA	0x89	2.671	NA	NA	0xf0	4.68	NA	y=0.0195x
P12V_STBY	59h	NA	0x69	10.5	NA	NA	0x82	13	NA	y=0.1x
VDD_5_RUN	5Ah	NA	0x2d	4.5	NA	NA	0x37	5.5	NA	y=0.1x
VDD_33_RUN	58h	NA	0x8f	2.788	NA	NA	0xba	3.627	NA	y=0.0195x
VDD_33_DUAL	5Ch	NA	0x8f	2.788	NA	NA	0xba	3.627	NA	y=0.0195x
CPU_18_DUAL	5Dh	NA	0x9c	1.529	NA	NA	0xc9	1.97	NA	y=0.0098x
SYS_FAN0	63h	NA	0x15	2625	NA	NA	NA	NA	NA	y=125x
SYS_FAN1	64h	NA	0x15	2625	NA	NA	NA	NA	NA	y=125x

Sensor Description	Sensor No.	LNR	LC (raw data)	LC (real value)	LNC	UNC	UC (raw data)	UC (real value)	UNR	Formula[1]
HSC_PIN	90h	NA	NA	NA	NA	NA	0XA8	840	NA	$y=5x$
HSC_VIN	91h	NA	0x67	9.27	NA	NA	0XA3	14.67	NA	$y=0.09x$
HSC_IOUT	92h	NA	NA	NA	NA	NA	0xb3	53.7	NA	$y=0.3x$
SOC_VIN	94h	NA	0xad	10.38	NA	NA	0xd3	12.66	NA	$y=0.06x$
SOC_VOUT	95h	NA	0xa	0.6	NA	NA	0x1a	1.56	NA	$y=0.06x$
PDB_HSC_VIN	96h	NA	0x9c	39	NA	NA	0Xec	59	NA	$y=0.25x$
PDB_HSC_IOUT	97h	NA	NA	NA	NA	NA	0x64	40	NA	$y=0.4x$
PDB_HSC_PIN	98h	NA	NA	NA	NA	NA	0x39	1140	NA	$y=20x$

Note:

1. Refer to IPMI 2.0 Section 36.3, where: y : Converted reading x : Raw reading.
Table 10 below provides the converted reading for maintenance.
2. 2's complement for negative value.

7.9 Event logging and Alerting

All of the system events are logged to an internal 64K bytes flash. However, Capri V2 BMC does not support any alert mechanism based on manufacturer per-configured Alert Policy.

7.10 Chassis and Power Control

This section describes the chassis control mechanism of Capri V2 platform. The related chassis commands are specified in IPMI v2.0 chapter 28.

6.10.1. Chassis Capabilities

Provides Monitoring Interrupt (NMI)

Chassis provides intrusion sensor

6.10.2. Chassis Control

The BMC must have ability to perform system power on/off and reset functions. These functions will be controlled externally through the IPMI chassis commands that described in the IPMIv2.0 specification. Including Get chassis

capabilities, Get chassis status, and chassis control, these kind of commands are mandatory IPMI commands and must be implemented.

Power down

Power up

Power cycle

Hard Reset

6.10.3. Chassis Control

The BMC have ability to generate unique events in SEL for the below button response.

Host System State	Button Action
Powered on	Any button press Short press (<=5 sec)
Powered off	Long press (1min> time >5 sec) Button stuck (>1min)

7.11 LAN Configuration

For SNMP Traps related LAN configuration setting, please refer to IPMI v2.0 spec Chapter 23.2 Get LAN Configuration Parameters Command “Table 23-4 LAN Configuration Parameters”, because Capri V2 BMC is following IPMI v2.0 spec definition to implement related function. Therefore Capri V2 BMC can’t allow user to enter host name to set LAN configuration.

Parameter	#	Parameter Data (non-volatile unless otherwise noted) ^[1]
Destination Addresses	19	Sets/Gets the list of IP addresses that a LAN alert can be sent to. This parameter is not present if the Number of Destinations parameter is 0. data 1 - Set Selector = Destination Selector. [7:4] - reserved [3:0] - Destination selector. Destination 0 is always present as a volatile destination that is used with the <i>Alert Immediate</i> command. data 2 - Address Format [7:4] - Address Format. 0h = IPv4 IP Address followed by DIX Ethernet/802.3 MAC Address [3:0] - reserved For Address Format = 0h: data 3 - Gateway selector [7:1] - reserved [0] - 0b = use default gateway 1b = use backup gateway data 4:7 - Alerting IP Address (MS-byte first) data 8:13 - Alerting MAC Address (MS-byte first) <i>Following parameters are introduced with IPMI v2.0 / RMCP+ VLAN configuration can be used with IPMI v1.5 and IPMI v2.0 sessions. Parameters labeled “RMCP+” are specific to IPMI v2.0 implementations that implement IPMI v2.0 / RMCP+ sessions.</i>
802.1q VLAN ID (12-bit)	20	data 1

6.11.1. Get / Set LAN Configuration Parameters

In order to reflect the capabilities provided by the BMC for some of the network settings, the values for some of the parameter data is defined as shown below.

6.11.1.1. DHCP

In addition to the usual methods of obtaining an IP address, the BMC provides a mode where it attempts to obtain an IP address from a DHCP server for a given period of time and if unsuccessful fails over to using a static IP address.

Parameter	#	Parameter Data
IP Address Source	4	<u>data 1</u> [7:4] – reserved [3:0] – address source 0h = unspecified 1h = static address (manually configured) 2h = address obtained by BMC running DHCP 3h = address obtained by BIOS or system software 4h = address obtained by BMC running other address assignment protocol. The BMC will use the value 4h to indicate the address mode of DHCP with failover to static.

7.12 Port 80 POST

Capri V2 BMC support port 80 POST code display to drive 8 bit HEX GPIO to debug header described. The BMC post function would ready before system BIOS starts to send 1st POST code to port 80.

BMC would access to POST code and record up to 256x POST codes. OOB raw command can be used to retrieve last 20x POST code from BMC.

7.13 LED Control by BMC

6.13.1. BMC Heartbeat LED

The BMC heartbeat LED will be blinking while BMC is alive, otherwise it must be deactivated while BMC's firmware is out of working.

6.13.2. UART Channel LED

BMC would control UART channel switch signal, and then this signal would direct to LED signal.

UART Channel LED

UART Channel	UART_LED1	UART_LED0
Host console	OFF	OFF
BMC debug console	OFF	ON
BMC UART2/IE UART	ON	OFF

6.13.3. Power and System Identification LED

The motherboard combines Power LED and System Identification LED to a single blue LED at front side.

Power LED on is defined by the readiness of major run time power rails (P12V, P5V, and P3V3) but NOT the readiness of all run time power rails; for example, CPU core power rail being ready is not required for Power LED on indication.

Power LED blinking is used as system identification. The on time is different during power on and power off.

There are 4 states of Power/system identification LED depending on system power state, and chassis identify status.

Power off, Chassis identify off: LED consistently off

Power off, Chassis identify on: LED on for 0.1sec, off for 0.9sec, and loop

Power on, Chassis identify off: LED consistently on

Power on, Chassis identify on: LED on for 0.9sec, off for 0.1sec, and loop

7.14 UART channel selection

When press UART switch, BMC shall be received the pulses, and control UART MUX to change Host UART console(Default)->BMC debug UART console->BMC UART2/IE UART console.

UART channel and connection

Channel	UART Connection
---------	-----------------

01	Host console
02	BMC debug console
03	BMC UART2/IE UART

7.15 BIOS Load default

Capri V2 BMC is following IPMI standard *Boot Option Parameters* #5 data 2 bit 7 to enable BIOS load default (set CMOS clear) for “Set System Boot Options Command” in IPMI 2.0 spec Table 28-14, *Boot Option Parameters*.

7.16 BMC Firmware Update

Capri V2 BMC supports in-band and out-of-band flashing of the BMC firmware via related tools.

6.16.1. BMC Firmware Update tools

User is able to update BMC by the following manners.

These utilities should be workable for FW update.

Yafuflash (7.01.0039 or above) via local USB or remote host via network for below OS:

Linux (CentOS 6.8/7.3 64-bit).

6.16.2. CPLD Code Update

Capri V2 BMC can access motherboard CPLD through JTAG and perform CPLD code upload from remote control server to BMC, update code from BMC to CPLD through CPLD JTAG interface. All the steps above shall be done from an update utility that supports CentOS 6.4 64-bit with updated Kernel specified by customer. BMC support OEM command to read CPLD code device ID, and version number.

7.17 Software Scheme

Auto BIOS recovery from backup flash to primary flash:

When 1st boot up after BIOS FW update fails and BMC watch dog timer (WDT) times out, BMC determine BIOS needs recovery, takes over control of flash access and duplicate backup flash content to primary flash.

Manual BIOS recovery from backup flash to primary flash :

User to use IPMI OEM command to trigger BMC taking over control of flash access and duplicate backup flash content to primary flash.

Manual BIOS save from primary flash to backup flash:

User to use IPMI OEM command to trigger BMC taking over control of flash access and duplicate primary flash to backup flash.

Manual Mux control:

User to use IPMI OEM command to trigger BMC to change of the state of two multiplexers.

Manual BIOS recovery from network to flash

User to use IPMI OEM command to trigger a BIOS SPI flash binary to be transferred to BMC and written to primary or secondary flash, depending on the state of multiplexer.

Enable/Disable Auto BIOS recovery

User to use IPMI OEM command to Enable and Disable feature of Auto BIOS recovery from backup flash to primary flash:

Get dual BIOS feature status:

User to use IPMI OEM command to get current state of two multiplexers, and Auto recovery

Enable/Disable status.

Get dual BIOS version:

User to use IPMI OEM command to access and return BIOS version of both primary and secondary flash.

6.17.1. Auto Recovering BIOS

Capri V2 is a dual bios system and BMC provides a BIOS auto recovering feature that it will automatically switch to the second bios if there is a crash/unexpected interruption occurred while updating bios. This chapter specifies what kinds of functions are required and explains how the auto recovering bios process performs.

7.18 BMC Network Status

BMC add one sensor #0xB1 with ED1=00/01 for LAN detection, expected behavior of this feature as following:

After BMC FW get IP address from DHCP server, BMC FW ping default GW IP.

If ping keep failed over 10x10 seconds , there will be ED1=00h SEL assertion event.

(Note: If ping successfully within 100 seconds, should not generate SEL log.)

Until ping successfully, then BMC generate ED=01h SEL event for de-assertion.

7.19 BMC Time Sync

In the Capri V2 platform, BIOS should send 'Set SEL Time' command to set the BMC time during POST.

7.20 Average Power Reporting

After BMC FW ready, BMC keeps sampling READ_EIN_EXT readings in one second interval until 60 readings in buffer.

Then go on sampling reading and over-write old data to keep 60 readings in buffer.

Run Get_PIN OEM command, BMC will output average value of 60 readings in buffer by ASCII format. (example: "1234.5" W)

There is a limitation that before BMC got 60 readings for average, there will be error response for command execution.

So after AC on, user needs to wait BMC ready plus around 60 seconds for sampling then this OEM command could work normally.

7.21 BMC Secure boot

There are 2 BMC flash images for BMC flash redundancy, and two stages for BMC secure boot mechanism:

Stage 1. RoT secure image to verify SPL

Stage 2. Signature FW image to verify kernel and root

BMC FW boots for verifying signature of the uboot image.

If the uboot SPL is verified passed with signature, then booting processes switch to Stage 2 and go on normal booting.

If the any parts is verified failed with signature, then secure FW stop booting process and proceed to boot into the 2nd flash image and continue FW booting process from stage 1 to stage 2.

8. Thermal Design Requirements

To meet thermal reliability requirements, the thermal and cooling solution should dissipate heat from the components when the system operating at its maximum thermal power. The thermal solution should be found by setting a high power target for initial design in order to avoid redesign of cooling solution; however, the final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. The thermal solution should not allow any overheating issues for any components in the system. CPU or memory should not throttle due to any thermal issue under the following environment:

- Inlet temperature lower than or equal to 35°C, and 0 inch H₂O datacenter pressure with all FANs in each thermal zone running properly

8.1 Data Center Environmental Conditions

The thermal design for Capri V2 needs to satisfy the data center operational conditions as described below.

7.1.1. Location of Data Center/Altitude

Data centers may be located 3050 meters above sea level or higher. Any variation of air properties or environmental difference due to the high altitude needs to be considered when creating the thermal design.

7.1.2. Cold-Aisle Temperature

Data centers will generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard deviation. The cold aisle temperature in a data center may fluctuate minutely depending to the outside air temperature of the data center. Every component in the system must be cooled and maintained below its maximum specified temperature in any cold aisle temperature in a data center.

7.1.3. Cold-Aisle Pressurization

Data centers will maintain the cold aisle pressure to be between 0" H₂O and 0.005" H₂O. The thermal solution of the system accommodates the worst-case operational pressurization in the data centers, which is 0" H₂O with no fan failures.

7.1.4. R.H

Most data centers will maintain the relative humidity to be between 20% and 90%. The thermal solution must sustain uninterrupted operation of the system across the aforementioned RH range. Server operational condition

8.2 Server operational condition

7.2.1. System Loading

The power consumption of individual components on the system motherboard will vary by application or by motherboard SKU. The total system power consumption may vary with use or with the number of existence of PCIe cards on the system:

- System Loading: idle to 100%
- Number of PCIe full height or half height cards that can be installed: 0 to 2
- Number of PCIe Mezz cards that can be installed: 0 to 1
- Number of 2.5" HDD: 0 to 2

Plan of record worst case configuration for thermal and power delivery design is 1 x 225W TDP CPU with 8 x 128GB DDR5 DIMM, or 8x 64GB DDR5 DIMM.

A unified thermal solution that can cover 100% of system loading is preferred. However, an ODM can propose non-unified thermal solution if there is alternative way to provide cost benefits. At least the air-duct design should be unified for all SKU.

7.2.2. DDR DIMM DRAM Operation

Thermal design should meet DIMM maximum operating temperature as 85°C with single refresh rate. Thermal test should be done based on a DIMM module's AVL (Approved Vendor List). The vendor should implement BIOS and memory subsystem to have optimized refresh rate and utilize optional DIMM Auto-Self-Refresh (ASR) based on DIMM temperature. The implementation should follow updated DDR5 memory controller and DIMM vendor's specification.

7.2.3. Inlet Temperature

The inlet air temperature will vary. The cooling system should cover inlet temperatures at 20°C, 25°C, 30°C, and 35°C. Cooling above 30°C is beyond operating specification, but used during validation to demonstrate design margin. CPU throttling is not allowed to activate over the validation range 0°C – 35°C.

7.2.4. Pressurization

Except for the condition of a single rotor in a server fan failing, the thermal solution should not be found with considering extra airflow from a data center cooling system. If and only if one rotor in server fan fails, the negative or positive DC pressurization can be considered in the thermal solution in the hot aisle or in cold aisle respectively.

7.2.5. System Airflow or Volumetric Flow

The unit of airflow (or volumetric flow) used for this spec is CFM (cubic feet per minute). The maximum allowable airflow per watt in the system must be 0.107. The desired airflow per watt is 0.1 or lower in the system at the mean temperature (plus or minus standard deviation). See section 7.1.2 for the temperature definitions.

7.2.6. Delta T

The delta T is the air temperature difference across the system or the temperature difference between outlet air temperature of system and inlet air temperature of system. The desired rack-level delta T must be greater than 13.9°C (25°F). The desired server-level delta T is 17°C (31°F) when the inlet air temperature to the system is equal to or lower than 30°C.

7.2.7. Thermal Margin

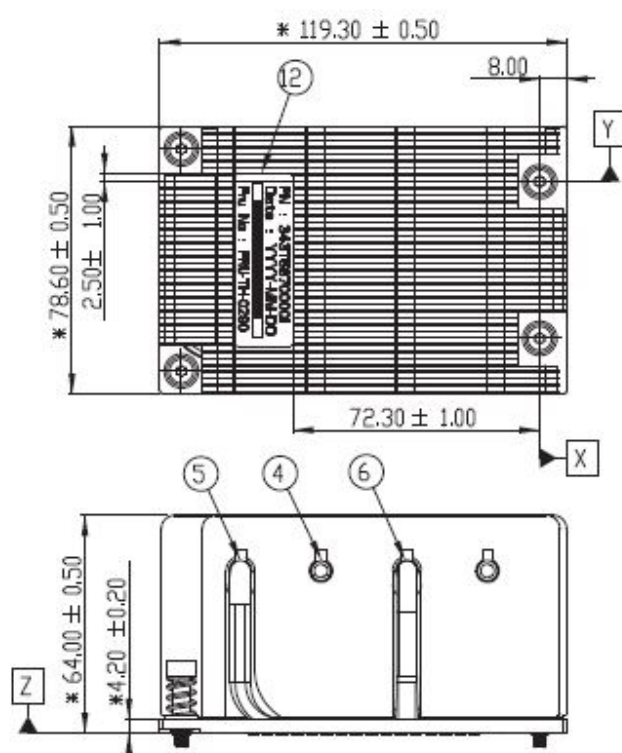
The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component in the system. Otherwise, the thermal margin for every component in the system is at least 7% for temperatures up to 30°C.

8.3 Thermal Kit Requirements

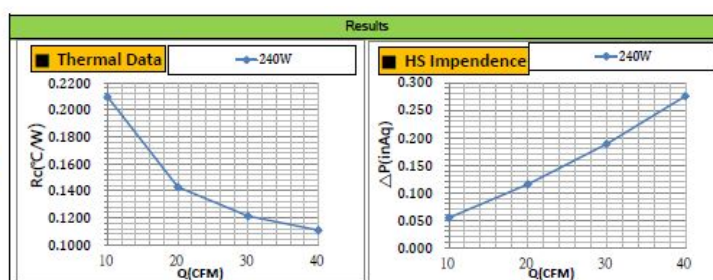
Thermal testing must be performed at up to 35°C (95°F) inlet temperature to guarantee high temperature reliability.

7.3.1. Heat Sink

The heat sink design should choose to be most optimized design with lowest cost. The heat sink design should be reliable and the most energy efficient design that satisfies all the conditions described above. The number of heat pipes in the heat sink should not be more than three. The ODM can always propose for different heat sink type if there is alternative way to provide cost benefits. The heat sink should be without complex installation guidance, such as air-flow direction.



Thermal performance Test (Taisol)							
item	condition						
1. Test System	Wind Tunnel						
2. Grease	TC5026 t=0.15 mm						
3. Heat source	TTV						
4. Power	240 watt						
5. Air Flow	10 - 20 - 30 - 40 CFM						
Results							
240W							
CFM	Tc(°C)	Ta	ΔT _{oa}	W	R _{oa} (°C/W)	ΔP(inAq)	
10	72.70	22.4	50.3	240	0.2096	0.0546	
20	56.50	22.2	34.3	240	0.1429	0.1154	
30	51.40	22.3	29.1	240	0.1213	0.1886	
40	48.60	22.0	26.6	240	0.1108	0.2758	

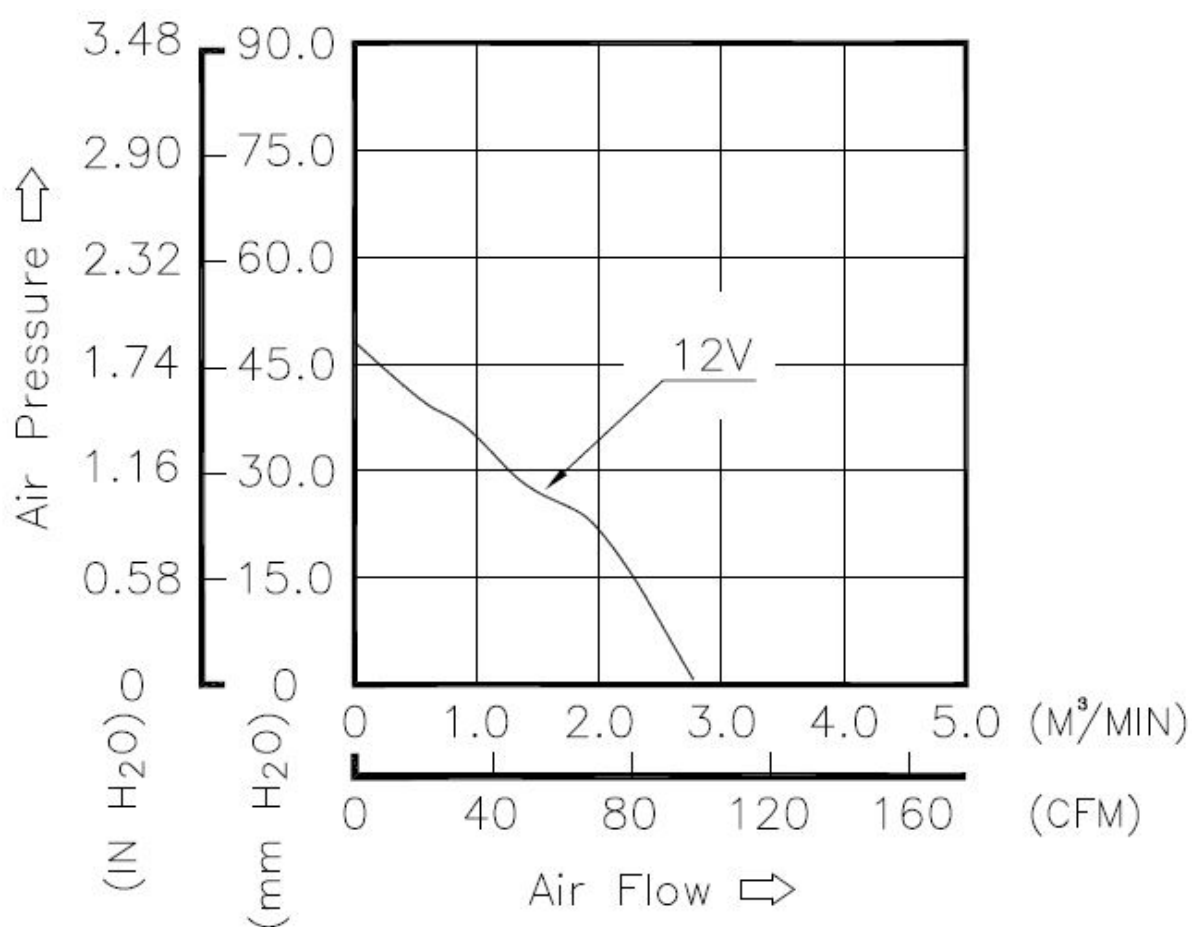
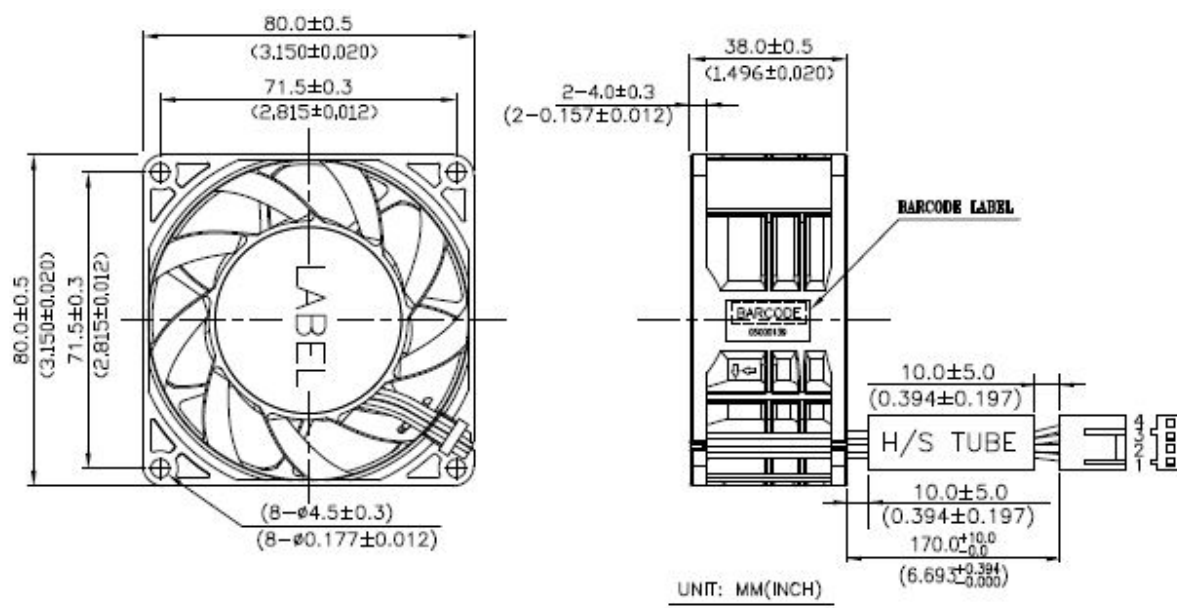


7.3.2. System Fan

The system fan must be highly power-efficient. The propagation of vibration cause by fan rotation should be minimized and limited. The minimum frame size of fan is 60x60mm and the maximum frame size is 80x80mm. ODM can propose larger frame size of fan than 80x80mm if and only if there is alternative way to provide cost benefits. The maximum thickness of fan should not be greater than 38mm. Each rotor in the fan should have a

maximum of five wires. Except for the condition when one fan (or one rotor) fails, the fan power consumption in system should not be exceeding 5% of total system power excluding the fan power. System fan should not have back rush current in all condition. System fan should have an inrush current of less than 1A on 12V per fan. When there is a step change on fan PWM signal from low PWM to high PWM, there should be less than 10% of overshoot or no overshoot for fan input current. System should stay within its power envelope (300W for Open Rack V1 configure) in all condition of fan operation.

ITEM	DESCRIPTION
RATED VOLTAGE	12 VDC
OPERATION VOLTAGE	11.25 - 13.75 VDC
INPUT CURRENT	1.60 (1.92 MAX.) A (SAFETY CURRENT 2.54A)
INPUT POWER	19.20 (23.04 MAX.) W
SPEED	10000±10% R.P.M.
MAX. AIR FLOW (AT ZERO STATIC PRESSURE)	2.76 (MIN. 2.48) M ³ /MIN 97.780(MIN. 88.00) CFM
MAX.AIR PRESSURE (AT ZERO AIR FLOW)	47.72 (MIN. 38.65) mmH ₂ O 1.878 (MIN. 1.521) inH ₂ O
ACOUSTICAL NOISE (AVG.)	66.0 (MAX 70.0) dB-A
INSULATION TYPE	UL: CLASS A



7.3.1. Air-Duct

The air duct needs to be part of the motherboard tray cover, and must be most energy efficient design. The air-duct design should be simple and easily serviceable. The air-duct design should be unified for all SKUs. Using highly green material or reusable material for the air duct is preferred.

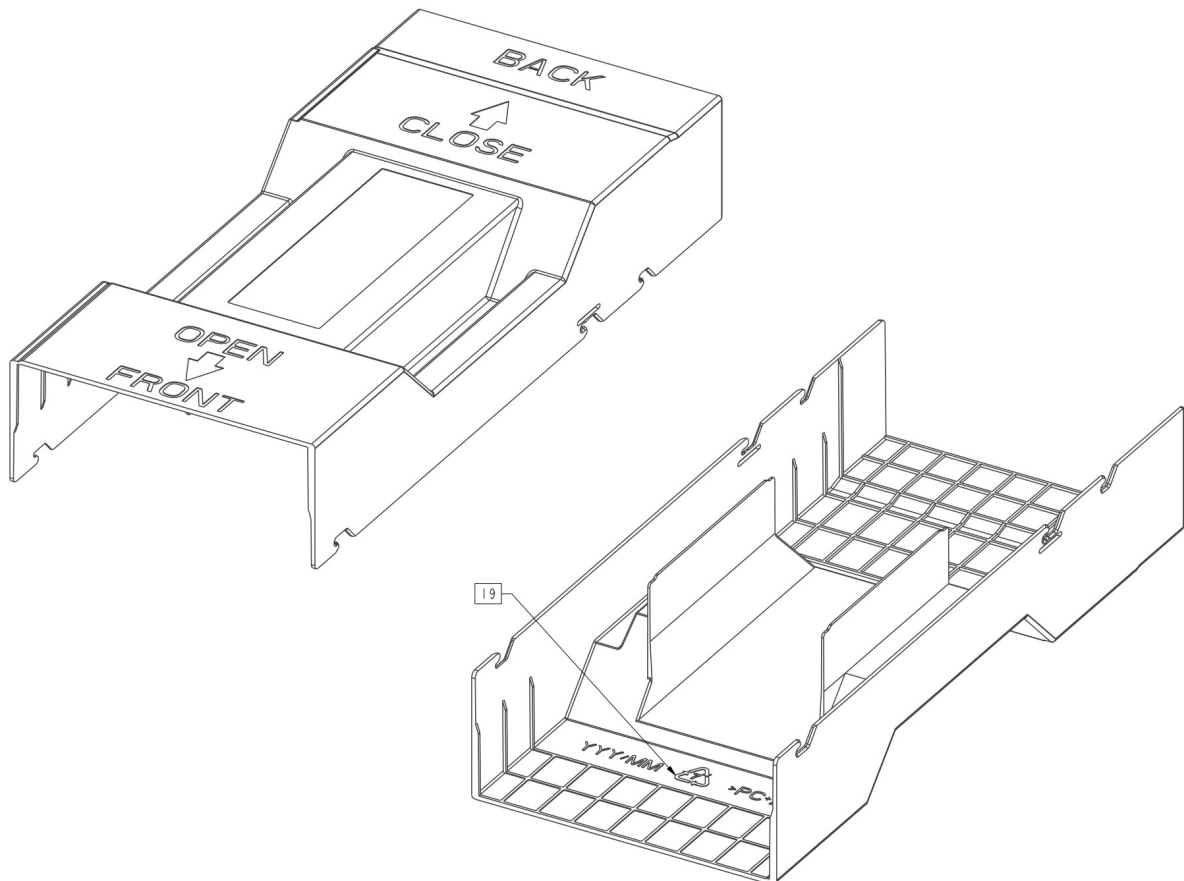


Figure 10 MiTAC CAPRI V2 Capri V2 Air-Duct Figure

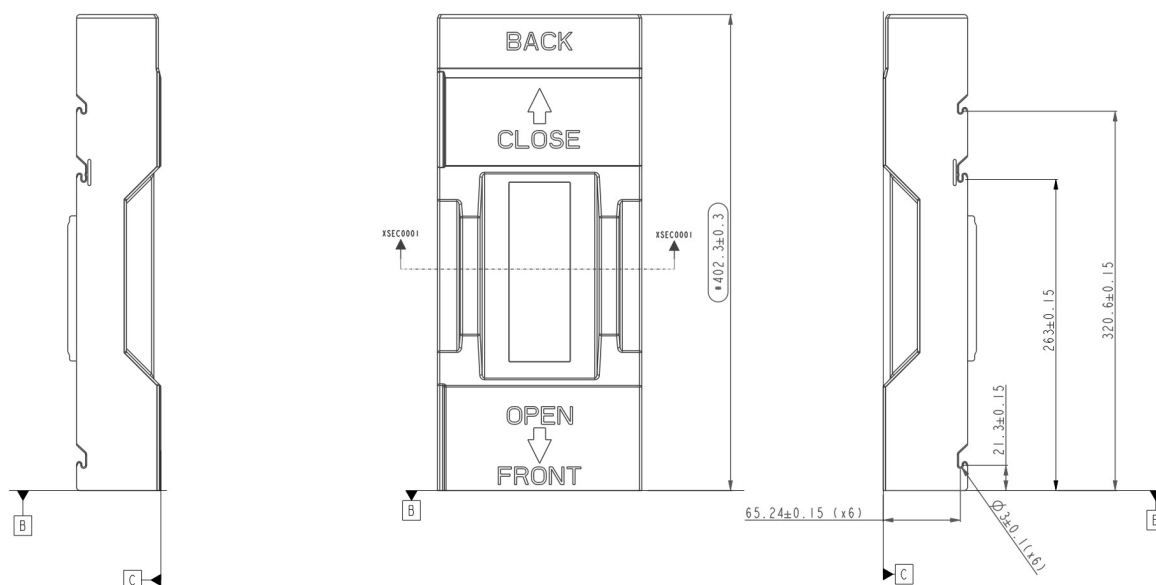


Figure 11 MiTAC CAPRI V2 Capri V2 Top View And Side View

7.3.2. Thermal sensor

The maximum allowable tolerance of thermal sensors in the motherboard is $\pm 3^{\circ}\text{C}$.

9. I/O System

9.1 Riser Card

9.1.1 Riser(2 and 3 slots) interface between riser card and motherboard

Two riser cards are used in this motherboard :

(1) 3_slots Riser is used for Ultra SKU(Support 2 PCIe16 slots and 1 PCIe8 slot)

(2) 2_slots Riser is used for Standard SKU(Support 2 PCIe16 slots)

All PCIe lanes is from CPU via MB MCIO connector(CN1, CN2 and CN5), and power delivery via MB PCIe x1 connector(J1_4 for 3_slots Riser, J1_3 for 2_slots Riser)

CN1(MCIO, PCIe x16 connector)			
A1	GND	B1	GND
A2	PCI_E_P1_TX_C_DP<0>	B2	PCI_E_P1_RX_L<0>
A3	PCI_E_P1_TX_C_DN<0>	B3	PCI_E_P1_RX_H<0>
A4	GND	B4	GND

A5	PCIE_P1_TX_C_DP<1>	B5	PCIE_P1_RX_L<1>
A6	PCIE_P1_TX_C_DN<1>	B6	PCIE_P1_RX_H<1>
A7	GND	B7	GND
A8	P_CONN_PCIE_RST_L<0>	B8	P1_CONN_UBM_I2C_ALERT_R_L
A9	NVME5_PRSNT_L	B9	NC
A10	NVME6_PRSNT_L	B10	NC
A11	NVME7_PRSNT_L	B11	NC
A12	NVME8_PRSNT_L	B12	NC
A13	GND	B13	GND
A14	PCIE_P1_TX_C_DP<2>	B14	PCIE_P1_RX_L<2>
A15	PCIE_P1_TX_C_DN<2>	B15	PCIE_P1_RX_H<2>
A16	GND	B16	GND
A17	PCIE_P1_TX_C_DP<3>	B17	PCIE_P1_RX_L<3>
A18	PCIE_P1_TX_C_DN<3>	B18	PCIE_P1_RX_H<3>
A19	GND	B19	GND
A20	PCIE_P1_TX_C_DP<4>	B20	PCIE_P1_RX_L<4>
A21	PCIE_P1_TX_C_DN<4>	B21	PCIE_P1_RX_H<4>
A22	GND	B22	GND
A23	PCIE_P1_TX_C_DP<5>	B23	PCIE_P1_RX_L<5>
A24	PCIE_P1_TX_C_DN<5>	B24	PCIE_P1_RX_H<5>
A25	GND	B25	GND
A26	NC	B26	CPU_P1_CONN_R_I2C_SCL
A27	NC	B27	CPU_P1_CONN_R_I2C_SDA
A28	GND	B28	GND
A29	CLK_100M_PCIE_SLOT1_DH	B29	NC
A30	CLK_100M_PCIE_SLOT1_DL	B30	NC
A31	GND	B31	GND
A32	PCIE_P1_TX_C_DP<6>	B32	PCIE_P1_RX_L<6>
A33	PCIE_P1_TX_C_DN<6>	B33	PCIE_P1_RX_H<6>
A34	GND	B34	GND
A35	PCIE_P1_TX_C_DP<7>	B35	PCIE_P1_RX_L<7>
A36	PCIE_P1_TX_C_DN<7>	B36	PCIE_P1_RX_H<7>
A37	GND	B37	GND
A38	GND	B38	GND
A39	PCIE_P1_TX_C_DP<8>	B39	PCIE_P1_RX_L<8>
A40	PCIE_P1_TX_C_DN<8>	B40	PCIE_P1_RX_H<8>
A41	GND	B41	GND
A42	PCIE_P1_TX_C_DP<9>	B42	PCIE_P1_RX_L<9>
A43	PCIE_P1_TX_C_DN<9>	B43	PCIE_P1_RX_H<9>
A44	GND	B44	GND
A45	PCIE_P1_TX_C_DP<10>	B45	PCIE_P1_RX_L<10>
A46	PCIE_P1_TX_C_DN<10>	B46	PCIE_P1_RX_H<10>
A47	GND	B47	GND
A48	PCIE_P1_TX_C_DP<11>	B48	PCIE_P1_RX_L<11>
A49	PCIE_P1_TX_C_DN<11>	B49	PCIE_P1_RX_H<11>
A50	GND	B50	GND
A51	PCIE_P1_TX_C_DP<12>	B51	PCIE_P1_RX_L<12>
A52	PCIE_P1_TX_C_DN<12>	B52	PCIE_P1_RX_H<12>
A53	GND	B53	GND
A54	PCIE_P1_TX_C_DP<13>	B54	PCIE_P1_RX_L<13>
A55	PCIE_P1_TX_C_DN<13>	B55	PCIE_P1_RX_H<13>
A56	GND	B56	GND
A57	PCIE_P1_TX_C_DP<14>	B57	PCIE_P1_RX_L<14>
A58	PCIE_P1_TX_C_DN<14>	B58	PCIE_P1_RX_H<14>
A59	GND	B59	GND

A60	PCIE_P1_TX_C_DP<15>	B60	PCIE_P1_RX_L<15>
A61	PCIE_P1_TX_C_DN<15>	B61	PCIE_P1_RX_H<15>
A62	GND	B62	GND

CN2(MCIO, PCIe x16 connector)			
A1	GND	B1	GND
A2	PCIE_P2_TX_C_DN<15>	B2	PCIE_P2_RX_H<15>
A3	PCIE_P2_TX_C_DP<15>	B3	PCIE_P2_RX_L<15>
A4	GND	B4	GND
A5	PCIE_P2_TX_C_DN<14>	B5	PCIE_P2_RX_H<14>
A6	PCIE_P2_TX_C_DP<14>	B6	PCIE_P2_RX_L<14>
A7	GND	B7	GND
A8	P_CONN_PCIE_RST_L<1>	B8	P2_CONN_UBM_I2C_ALERT_R_L
A9	NVME10_PRSENT_L	B9	NC
A10	NVME11_PRSENT_L	B10	NC
A11	NVME12_PRSENT_L	B11	NC
A12	NVME13_PRSENT_L	B12	NC
A13	GND	B13	GND
A14	PCIE_P2_TX_C_DN<13>	B14	PCIE_P2_RX_H<13>
A15	PCIE_P2_TX_C_DP<13>	B15	PCIE_P2_RX_L<13>
A16	GND	B16	GND
A17	PCIE_P2_TX_C_DN<12>	B17	PCIE_P2_RX_H<12>
A18	PCIE_P2_TX_C_DP<12>	B18	PCIE_P2_RX_L<12>
A19	GND	B19	GND
A20	PCIE_P2_TX_C_DN<11>	B20	PCIE_P2_RX_H<11>
A21	PCIE_P2_TX_C_DP<11>	B21	PCIE_P2_RX_L<11>
A22	GND	B22	GND
A23	PCIE_P2_TX_C_DN<10>	B23	PCIE_P2_RX_H<10>
A24	PCIE_P2_TX_C_DP<10>	B24	PCIE_P2_RX_L<10>
A25	GND	B25	GND
A26	NC	B26	CPU_P2_CONN_R_I2C_SCL
A27	NC	B27	CPU_P2_CONN_R_I2C_SDA
A28	GND	B28	GND
A29	CLK_100M_PCIE_SLOT2_DH	B29	NC
A30	CLK_100M_PCIE_SLOT2_DL	B30	NC
A31	GND	B31	GND
A32	PCIE_P2_TX_C_DN<9>	B32	PCIE_P2_RX_H<9>
A33	PCIE_P2_TX_C_DP<9>	B33	PCIE_P2_RX_L<9>
A34	GND	B34	GND
A35	PCIE_P2_TX_C_DN<8>	B35	PCIE_P2_RX_H<8>
A36	PCIE_P2_TX_C_DP<8>	B36	PCIE_P2_RX_L<8>
A37	GND	B37	GND
A38	GND	B38	GND
A39	PCIE_P2_TX_C_DN<7>	B39	PCIE_P2_RX_H<7>
A40	PCIE_P2_TX_C_DP<7>	B40	PCIE_P2_RX_L<7>
A41	GND	B41	GND
A42	PCIE_P2_TX_C_DN<6>	B42	PCIE_P2_RX_H<6>
A43	PCIE_P2_TX_C_DP<6>	B43	PCIE_P2_RX_L<6>
A44	GND	B44	GND
A45	PCIE_P2_TX_C_DN<5>	B45	PCIE_P2_RX_H<5>
A46	PCIE_P2_TX_C_DP<5>	B46	PCIE_P2_RX_L<5>
A47	GND	B47	GND

A48	PCIE_P2_TX_C_DN<4>	B48	PCIE_P2_RX_H<4>
A49	PCIE_P2_TX_C_DP<4>	B49	PCIE_P2_RX_L<4>
A50	GND	B50	GND
A51	PCIE_P2_TX_C_DN<3>	B51	PCIE_P2_RX_H<3>
A52	PCIE_P2_TX_C_DP<3>	B52	PCIE_P2_RX_L<3>
A53	GND	B53	GND
A54	PCIE_P2_TX_C_DN<2>	B54	PCIE_P2_RX_H<2>
A55	PCIE_P2_TX_C_DP<2>	B55	PCIE_P2_RX_L<2>
A56	GND	B56	GND
A57	PCIE_P2_TX_C_DN<1>	B57	PCIE_P2_RX_H<1>
A58	PCIE_P2_TX_C_DP<1>	B58	PCIE_P2_RX_L<1>
A59	GND	B59	GND
A60	PCIE_P2_TX_C_DN<0>	B60	PCIE_P2_RX_H<0>
A61	PCIE_P2_TX_C_DP<0>	B61	PCIE_P2_RX_L<0>
A62	GND	B62	GND

CN5(MCIO, PCIe x8 connector)			
A1	GND	B1	GND
A2	PCIE_P0_RX_H<7>	B2	PCIE_P0_TX_C_L<7>
A3	PCIE_P0_RX_L<7>	B3	PCIE_P0_TX_C_H<7>
A4	GND	B4	GND
A5	PCIE_P0_RX_H<6>	B5	PCIE_P0_TX_C_L<6>
A6	PCIE_P0_RX_L<6>	B6	PCIE_P0_TX_C_H<6>
A7	GND	B7	GND
A8	SLIMSAS_BP_TYPE9	B8	NC
A9	PCIE_CN5_WAKE_L	B9	NC
A10	GND	B10	GND
A11	CLK_100M_NVME5_DH	B11	NVME_PERST5
A12	CLK_100M_NVME5_DL	B12	NVME9_PRSTNT_L
A13	GND	B13	GND
A14	PCIE_P0_RX_H<5>	B14	PCIE_P0_TX_C_L<5>
A15	PCIE_P0_RX_L<5>	B15	PCIE_P0_TX_C_H<5>
A16	GND	B16	GND
A17	PCIE_P0_RX_H<4>	B17	PCIE_P0_TX_C_L<4>
A18	PCIE_P0_RX_L<4>	B18	PCIE_P0_TX_C_H<4>
A19	GND	B19	GND
A20	PCIE_P0_RX_C_H<3>	B20	PCIE_P0_TX_C_L<3>
A21	PCIE_P0_RX_C_L<3>	B21	PCIE_P0_TX_C_H<3>
A22	GND	B22	GND
A23	PCIE_P0_RX_C_H<2>	B23	PCIE_P0_TX_C_L<2>
A24	PCIE_P0_RX_C_L<2>	B24	PCIE_P0_TX_C_H<2>
A25	GND	B25	GND
A26	NC	B26	NVME_SMB_SCL6
A27	P0_CONN_CN5_I2C_ALERT_L	B27	NVME_SMB_SDA6
A28	GND	B28	GND
A29	NC	B29	NC
A30	NC	B30	NC
A31	GND	B31	GND
A32	PCIE_P0_RX_C_H<1>	B32	PCIE_P0_TX_C_L<1>
A33	PCIE_P0_RX_C_L<1>	B33	PCIE_P0_TX_C_H<1>
A34	GND	B34	GND
A35	PCIE_P0_RX_C_H<0>	B35	PCIE_P0_TX_C_L<0>

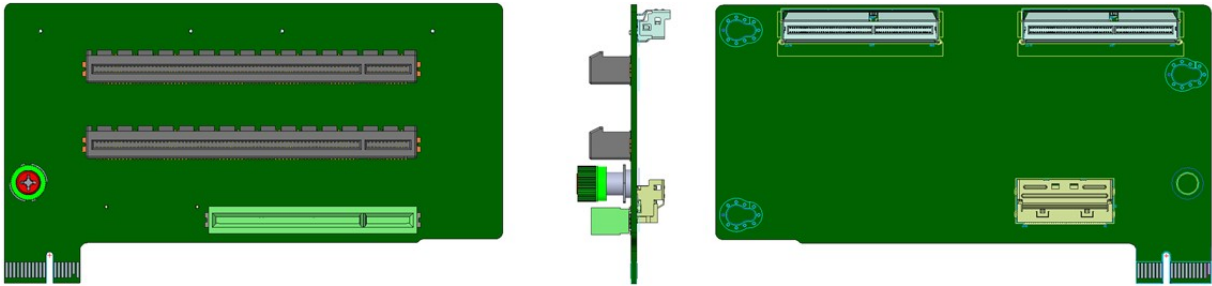
A36	PCIE_P0_RX_C_L<0>	B36	PCIE_P0_TX_C_H<0>
A37	GND	B37	GND

J1_4(PClex1 connector for 3 slots Riser power)			
A1	P12V_1	B1	P12V_1
A2	P12V_1	B2	P12V_1
A3	P12V_1	B3	P12V_1
A4	P12V_1	B4	P12V_1
A5	P12V_1	B5	P12V_1
A6	P12V_1	B6	P12V_1
A7	P12V_1	B7	P12V_1
A8	P12V_1	B8	P12V_1
A9	P12V_1	B9	P12V_1
A10	GND	B10	GND
A11	GND	B11	GND
A12	GND	B12	GND
A13	GND	B13	GND
A14	GND	B14	GND
A15	GND	B15	GND
A16	GND	B16	GND
A17	GND	B17	GND
A18	3SLOT_RISER_PRNT_R_N	B18	GND

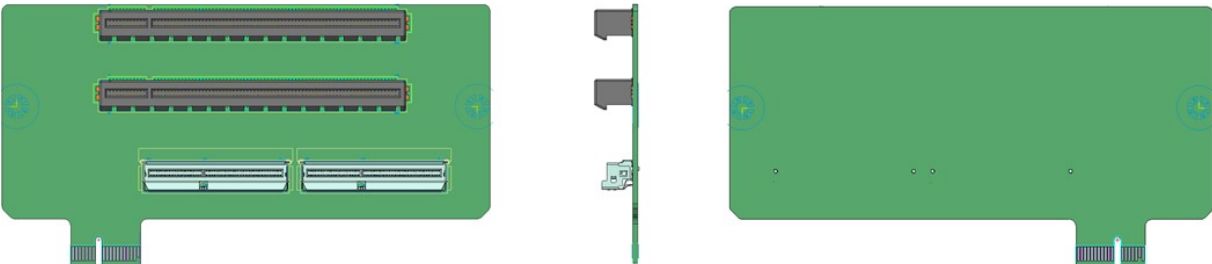
J1_3(PClex1 connector for 2 slots Riser power)			
A1	P12V_0	B1	P12V_0
A2	P12V_0	B2	P12V_0
A3	P12V_0	B3	P12V_0
A4	P12V_0	B4	P12V_0
A5	P12V_0	B5	P12V_0
A6	P12V_0	B6	P12V_0
A7	P12V_0	B7	P12V_0
A8	P12V_0	B8	P12V_0
A9	P12V_0	B9	P12V_0
A10	GND	B10	GND
A11	GND	B11	GND
A12	GND	B12	GND
A13	GND	B13	GND
A14	GND	B14	GND
A15	GND	B15	GND
A16	GND	B16	GND
A17	GND	B17	GND
A18	2SLOT_RISER_PRNT_R_N	B18	GND

9.1.2 Riser card types

Riser_3 slots



Riser_2 slots



9.2 E1.S(x4) BP and U.2 BP

9.2.1 E1.S(x4)/U.2 BP interface between E1.S(x4)/U.2 BP and motherboard

All PCIE lanes PCIE is from CPU via MB MCIO connector(CN3), and power delivery via MB power connector(PWR2)

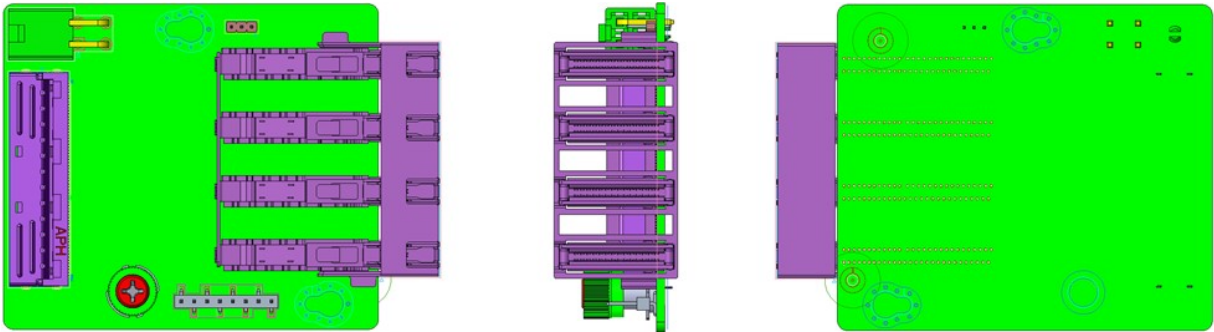
CN3(MCIO, PCIe x16 connector)			
A1	GND	B1	GND
A2	XGMI_G0_RX_H<15>	B2	XGMI_G0_TX_C_L<15>
A3	XGMI_G0_RX_L<15>	B3	XGMI_G0_TX_C_H<15>
A4	GND	B4	GND
A5	XGMI_G0_RX_H<14>	B5	XGMI_G0_TX_C_L<14>
A6	XGMI_G0_RX_L<14>	B6	XGMI_G0_TX_C_H<14>
A7	GND	B7	GND
A8	CLK_100M_NVME1_DH	B8	VDD_33_DUAL
A9	CLK_100M_NVME1_DL	B9	VDD_33_DUAL
A10	GND	B10	VDD_33_DUAL
A11	NVME2_PRSENT_L	B11	VDD_33_DUAL
A12	NVME3_PRSENT_L	B12	NC
A13	GND	B13	GND

A14	XGMI_G0_RX_H<13>	B14	XGMI_G0_TX_C_L<13>
A15	XGMI_G0_RX_L<13>	B15	XGMI_G0_TX_C_H<13>
A16	GND	B16	GND
A17	XGMI_G0_RX_H<12>	B17	XGMI_G0_TX_C_L<12>
A18	XGMI_G0_RX_L<12>	B18	XGMI_G0_TX_C_H<12>
A19	GND	B19	GND
A20	XGMI_G0_RX_H<11>	B20	XGMI_G0_TX_C_L<11>
A21	XGMI_G0_RX_L<11>	B21	XGMI_G0_TX_C_H<11>
A22	GND	B22	GND
A23	XGMI_G0_RX_H<10>	B23	XGMI_G0_TX_C_L<10>
A24	XGMI_G0_RX_L<10>	B24	XGMI_G0_TX_C_H<10>
A25	GND	B25	GND
A26	NVME4_PRSTNT_L	B26	NVME_SMB_SCL1
A27	NVME_PERST1	B27	NVME_SMB_SDA1
A28	NVME_PERST2	B28	NVME_SMB_SCL2
A29	NVME_PERST3	B29	NVME_SMB_SDA2
A30	NVME_PERST4	B30	NVME1_PRSTNT_L
A31	GND	B31	GND
A32	XGMI_G0_RX_H<9>	B32	XGMI_G0_TX_C_L<9>
A33	XGMI_G0_RX_L<9>	B33	XGMI_G0_TX_C_H<9>
A34	GND	B34	GND
A35	XGMI_G0_RX_H<8>	B35	XGMI_G0_TX_C_L<8>
A36	XGMI_G0_RX_L<8>	B36	XGMI_G0_TX_C_H<8>
A37	GND	B37	GND
A38	GND	B38	GND
A39	XGMI_G0_RX_H<7>	B39	XGMI_G0_TX_C_L<7>
A40	XGMI_G0_RX_L<7>	B40	XGMI_G0_TX_C_H<7>
A41	GND	B41	GND
A42	XGMI_G0_RX_H<6>	B42	XGMI_G0_TX_C_L<6>
A43	XGMI_G0_RX_L<6>	B43	XGMI_G0_TX_C_H<6>
A44	GND	B44	GND
A45	XGMI_G0_RX_H<5>	B45	XGMI_G0_TX_C_L<5>
A46	XGMI_G0_RX_L<5>	B46	XGMI_G0_TX_C_H<5>
A47	GND	B47	GND
A48	XGMI_G0_RX_H<4>	B48	XGMI_G0_TX_C_L<4>
A49	XGMI_G0_RX_L<4>	B49	XGMI_G0_TX_C_H<4>
A50	GND	B50	GND
A51	XGMI_G0_RX_H<3>	B51	XGMI_G0_TX_C_L<3>

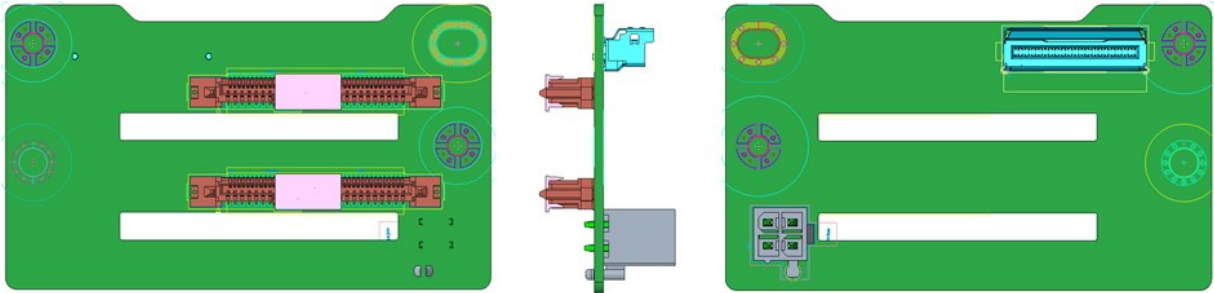
A52	XGMI_G0_RX_L<3>	B52	XGMI_G0_TX_C_H<3>
A53	GND	B53	GND
A54	XGMI_G0_RX_H<2>	B54	XGMI_G0_TX_C_L<2>
A55	XGMI_G0_RX_L<2>	B55	XGMI_G0_TX_C_H<2>
A56	GND	B56	GND
A57	XGMI_G0_RX_H<1>	B57	XGMI_G0_TX_C_L<1>
A58	XGMI_G0_RX_L<1>	B58	XGMI_G0_TX_C_H<1>
A59	GND	B59	GND
A60	XGMI_G0_RX_H<0>	B60	XGMI_G0_TX_C_L<0>
A61	XGMI_G0_RX_L<0>	B61	XGMI_G0_TX_C_H<0>
A62	GND	B62	GND

PWR2(Power for E1.Sx4 BP and U.2 BP)			
1	GND	5	VDD_5_RUN
2	GND	6	P12V_1
3	GND	7	VDD_5_RUN
4	GND	8	P12V_1

E1.Sx4 BP



U.2 BP



9.3 DIMM Sockets

The motherboard requires 15u" gold contact for DDR5 SMT DIMM socket. Socket uses Black housing and latch for far end DIMM in a DDR channel. Vendor shall announce if the color selection will increase the cost of the DIMM Socket.

9.4 Mezzanine Card

Capri v2 is compatible with Mezzanine Card for OCP Mezzanine Card 3.0 design specifications.

The motherboard has connector OCP3_1 as OCP Mezz 3.0 specification to provide up to X 16 PCIe connection to Mezzanine card.

9.4.1 OCP3_1

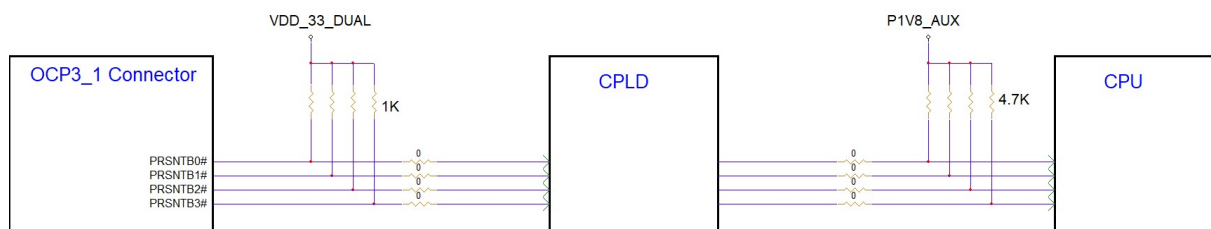
Below table shows connector OCP3_1 pin definition:

OCP3_1			
OA1	OCP3_RST2_DELAY_N	OB1	NIC_PWR_GOOD
OA2	OCP3_RST3_DELAY_N	OB2	OCP3_MAIN_PWR_EN_R
OA3	OCP3_WAKE_N	OB3	OCP3_LOAD
OA4	RBT_ARB_IN	OB4	OCP3_DATAIN
OA5	RBT_ARB_OUT	OB5	OCP3_DATAOUT
OA6	OCP_SLOT_ID1	OB6	OCP3_12M_CLK
OA7	OCP_NCSI_TXEN	OB7	OCP_SLOT_ID0
OA8	OCP_NCSI_TXD1	OB8	OCP_NCSI_RXD1
OA9	OCP_NCSI_TXD0	OB9	OCP_NCSI_RXD0
OA10	GND	OB10	GND
OA11	MEZZ_PREFERCLK_B_DL	OB11	MEZZ_PREFERCLK_A_DL
OA12	MEZZ_PREFERCLK_B_DH	OB12	MEZZ_PREFERCLK_A_DH
OA13	GND	OB13	GND
OA14	OCP_NCSI_50M	OB14	OCP_NCSI_CRSDV
A1	GND	B1	P12V_AUX_OCPV3
A2	GND	B2	P12V_AUX_OCPV3
A3	GND	B3	P12V_AUX_OCPV3
A4	GND	B4	P12V_AUX_OCPV3
A5	GND	B5	P12V_AUX_OCPV3
A6	GND	B6	P12V_AUX_OCPV3
A7	LAN_OCP_SMB_CLK	B7	OCP_BIF0
A8	LAN_OCP_SMB_DAT	B8	OCP_BIF1
A9	PU_OCP_SMRST_N	B9	OCP_BIF2
A10	GND	B10	OCP_PERST0_L
A11	OCP_PERST1_L	B11	P3V3_PCIE
A12	OCP_PRSTB2#	B12	OCP3_AUX_PWR_EN
A13	GND	B13	GND
A14	MEZZ_PREFERCLK_A1_DL	B14	MEZZ_PREFERCLK_B1_DL
A15	MEZZ_PREFERCLK_A1_DH	B15	MEZZ_PREFERCLK_B1_DH
A16	GND	B16	GND

A17	PCIE_P3_RX_L<0>	B17	PCIE_P3_TX_C_DP<0>
A18	PCIE_P3_RX_H<0>	B18	PCIE_P3_TX_C_DN<0>
A19	GND	B19	GND
A20	PCIE_P3_RX_L<1>	B20	PCIE_P3_TX_C_DP<1>
A21	PCIE_P3_RX_H<1>	B21	PCIE_P3_TX_C_DN<1>
A22	GND	B22	GND
A23	PCIE_P3_RX_L<2>	B23	PCIE_P3_TX_C_DP<2>
A24	PCIE_P3_RX_H<2>	B24	PCIE_P3_TX_C_DN<2>
A25	GND	B25	GND
A26	PCIE_P3_RX_L<3>	B26	PCIE_P3_TX_C_DP<3>
A27	PCIE_P3_RX_H<3>	B27	PCIE_P3_TX_C_DN<3>
A28	GND	B28	GND
A29	GND	B29	GND
A30	PCIE_P3_RX_L<4>	B30	PCIE_P3_TX_C_DP<4>
A31	PCIE_P3_RX_H<4>	B31	PCIE_P3_TX_C_DN<4>
A32	GND	B32	GND
A33	PCIE_P3_RX_L<5>	B33	PCIE_P3_TX_C_DP<5>
A34	PCIE_P3_RX_H<5>	B34	PCIE_P3_TX_C_DN<5>
A35	GND	B35	GND
A36	PCIE_P3_RX_L<6>	B36	PCIE_P3_TX_C_DP<6>
A37	PCIE_P3_RX_H<6>	B37	PCIE_P3_TX_C_DN<6>
A38	GND	B38	GND
A39	PCIE_P3_RX_L<7>	B39	PCIE_P3_TX_C_DP<7>
A40	PCIE_P3_RX_H<7>	B40	PCIE_P3_TX_C_DN<7>
A41	GND	B41	GND
A42	OCP_PRSENTB1#	B42	OCP_PRSENTB0#
A43	GND	B43	GND
A44	PCIE_P3_RX_L<8>	B44	PCIE_P3_TX_C_DP<8>
A45	PCIE_P3_RX_H<8>	B45	PCIE_P3_TX_C_DN<8>
A46	GND	B46	GND
A47	PCIE_P3_RX_L<9>	B47	PCIE_P3_TX_C_DP<9>
A48	PCIE_P3_RX_H<9>	B48	PCIE_P3_TX_C_DN<9>
A49	GND	B49	GND
A50	PCIE_P3_RX_L<10>	B50	PCIE_P3_TX_C_DP<10>
A51	PCIE_P3_RX_H<10>	B51	PCIE_P3_TX_C_DN<10>
A52	GND	B52	GND
A53	PCIE_P3_RX_L<11>	B53	PCIE_P3_TX_C_DP<11>
A54	PCIE_P3_RX_H<11>	B54	PCIE_P3_TX_C_DN<11>
A55	GND	B55	GND
A56	PCIE_P3_RX_L<12>	B56	PCIE_P3_TX_C_DP<12>
A57	PCIE_P3_RX_H<12>	B57	PCIE_P3_TX_C_DN<12>
A58	GND	B58	GND
A59	PCIE_P3_RX_L<13>	B59	PCIE_P3_TX_C_DP<13>
A60	PCIE_P3_RX_H<13>	B60	PCIE_P3_TX_C_DN<13>
A61	GND	B61	GND
A62	PCIE_P3_RX_L<14>	B62	PCIE_P3_TX_C_DP<14>
A63	PCIE_P3_RX_H<14>	B63	PCIE_P3_TX_C_DN<14>
A64	GND	B64	GND
A65	PCIE_P3_RX_L<15>	B65	PCIE_P3_TX_C_DP<15>
A66	PCIE_P3_RX_H<15>	B66	PCIE_P3_TX_C_DN<15>
A67	GND	B67	GND
A68	USB2_N7_OCP3.0_R	B68	NC
A69	USB2_P7_OCP3.0_R	B69	NC
A70	PE_PWRBRK_N_R	B70	OCP_PRSENTB3#

9.4.2 Mezzanine present pin

Capri V2 Mezzanine present pins' connection to CPLD (CPLD pass to CPU) as below:



9.5 Network

9.5.1 Data network

The motherboard uses OCP mezzanine 3.0 card as its primary data network interface at I/O side.

9.5.2 Management Network

The motherboard has management network interface for BMC's connection. Management network shares data network's physical interface. Management connection should be independent from traffic, and OS/driver condition.

Shared-NIC from Mezzanine 3.0 NIC, driven by BMC through RMII/NC-SI or I2C.

9.5.3 IPv4/IPv6 support

The system needs to have the capacity to be deployed in both IPv4 and IPv6 network environment. All data network and management network should have this capability. This includes, but not limited to: DHCP and static IP setting, PXE booting capability, NIC and BMC firmware support, OS driver, and utility in both IPv4 and IPv6.

9.6 USB

The motherboard has two external type A right angle USB 2.0/3.0 port located in front of the motherboard. BIOS should support following devices on motherboard:

- USB keyboard and mouse.
- USB flash drive (bootable)
- USB hard drive (bootable)
- USB optical drive (bootable)

9.7 M.2

The motherboard has 2x M.2 connector. M.2 connector has connection of PCIe4 from CPU. On board M.2 connector supports 2280, 22110 card form factor with both single side and double side.

9.8 Debug header

The motherboard has 1 debug headers to work with 15 pin debug card.

15 pin debug card header

Debug header pin definition:

J62	
VDD_33_DUAL	1
DBG_ESPI_CS1_N	2
LAD0_ESPI_DBG_IO0	3
LAD1_ESPI_DBG_IO1	5
DBG_ESPI_RESET_N	6
LAD2_ESPI_DBG_IO2	7
GND	8
LAD3_ESPI_DBG_IO3	9
CLK_DBG_ESPI	10
DBG_ESPI_ALERT1_N	11
GND	12
DB_UART_TX	13
DB_UART_RX_R	14
DB_UART_SWITCH_N	15
N.C.	16

9.9 LEDs

The table below indicates the color and function of each LED on MB.

■ Power On LED

status	LED COLOR	Behavior	LED Location
System power on	ON	MB is in the power on status	LED1

■ HDD LED

status	LED COLOR	Behavior	LED Location
Hard drive activity	ON	ON when M.2 install	LED2

■ BMC HEARTBEAT LED

status	LED	Behavior	LED
--------	-----	----------	-----

	COLOR		Location
BMC ready	Blinking 1Hz	When BMC FW initialize	D1_2

■ ID LED

status	LED COLOR	Behavior	LED Location
Chassis identify	Blinking	-LED on for 0.1sec, off for 0.9sec and loop when system power off.-LED on for 0.9sec, off for 0.1sec and loop when system power on.	D77

■ CPU PWR OK LED

status	LED COLOR	Behavior	LED Location
CPU Power OK	ON	When CPU power OK	D52

■ CPU PWR GOOD LED

status	LED COLOR	Behavior	LED Location
CPU Power GOOD	ON	When CPU power GOOD	D57

■ CPU RESET LED

status	LED COLOR	Behavior	LED Location
CPU RESET	ON	When CPU Reset	D58

■ UART SW LED

status	LED COLOR	Behavior	LED Location
UART activity	Blinking	MSB	D18
UART activity	Blinking	LSB	D19

9.10 FAN connector

The motherboard has two system FAN connectors.

FAN connector Pin Definition

6Pin x1 (FAN1)

Net Name	Pin #
GND	1
P12V_FAN	2
FAN_TACH0_CPU0_D1	3
FAN_PWM_OUT_SYS0_R	4
GND	5
P12V_FAN	6

6Pin x1 (FAN2)

Net Name	Pin #
GND	1
P12V_FAN	2
FAN_TACH1_CPU0_D1	3
FAN_PWM_OUT_SYS1_R	4
GND	5
P12V_FAN	6

10. Rear Side Power, I/O and Midplane

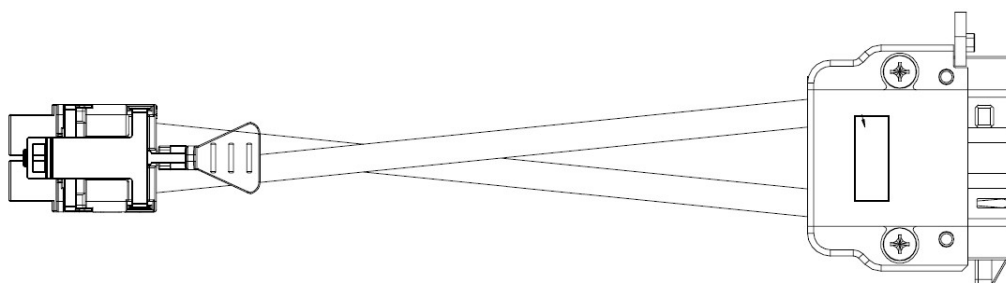
10.1 Overview of Footprint and Population Options

For 12V SKU, there is 2x footprint at rear side of the motherboard to provide power to motherboard. The population of the footprints is flexible to fit the need of different use cases.

For 48V SKU, there is 1x footprint at the PDB to provide power to motherboard. The population of the footprints is flexible to fit the need of different use cases.

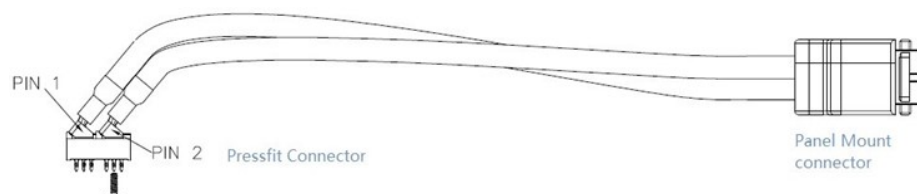
10.2 Midplane

A power cable is enabled for the use case of 12V SKU. A side view is shown below



One side of the 12V power cable is installed on motherboard connector. The other side of the cable is a panel mount connector. It is installed on a sheet metal panel with tool-less install and remove.

A pressfit cable on PDB is enabled for 48V SKU. A side view is shown below.



One side of the Pressfit cable is a pressfit power connector. The pressfit power connector is installed on PDB with pressfit process, and secured by a screw for added strength. Pressfit power connector shares the same footprint and pin define as FCI/10124648-001LF.

The other side of the pressfit cable is a panel mount connector. It is installed on a sheet metal panel with tool-less install and remove.

11. ORv2 Implementation

MiTAC Capri V2 is compatible and can be complied with Orv2. This is because the form factor of Capri V2 follows Tioga Pass (20U 3Nodes) therefore it is compatible with Open Rack v2.

12. Mechanical

12.1 Single Side Sled mechanical

Capri V2 single sled mechanical design and tooling follows Tioga Pass in ORv2 sled. For the detail mechanical design, please refer to Tioga Pass document in OCP.

12.2 PCB Thickness

To ensure proper alignment of the motherboard and mid-plane interface within its mechanical enclosure, the motherboard should follow PCB stack up to have 75.0mil (1.93mm) PCB thickness. And thickness of PDB PCB should also be 92.4mil (2.3mm). Thickness of riser card PCB should also be 61.5mil (1.57mm).

12.3 Heat Sinks and ILM

The motherboard shall support heat sinks that are mounted according to the AMD thermal mechanical specification and design guide. The vendor shall comply with all keep out zones defined by AMD in the reference specification.

12.4 Silk Screen

The silk screen shall be white in color and include printings for the components listed below. Additional items required on the silk screen are listed in the section of Regulations.

- DIMM slot numbering.
- LEDs.
- Switches as PWR and RST.

12.5 PCB Color

Different PCB colors shall be used to help identify the motherboards revision. Table below indicates the PCB color to be used for each development revision.

Revision	PCB color
EVT	Red
DVT	Blue
PVT	Green
MP	Green

13. Motherboard Power System

13.1 Input Voltage

13.1.1 12V Input Voltage Level

The nominal input voltage provided by the power supply under light load is 12.5V DC, with a range between 11V and 13V. The motherboard should operate normally within an input voltage tolerance range of 10.8V to 13.2V, when all under voltage related throttling features are disabled in section 12.2.

Motherboard's under-voltage protection level should be less than 10.1V.

13.1.2 48V Input Voltage Level

When using a 48V system, it's necessary to install a PDB to enable the system to withstand a 48V input voltage.

The nominal input voltage provided by the power supply under light load is 50V DC, with a range between 47.5V and 51V.

13.1.3 Capacitive Load

Previous server generations required a maximum capacitive load of 4,000 uF. This requirement does not apply to CapriV2 design. The motherboard design requires greater than 4,500 uF capacitive loading on P12V_AUX for supplying surge current from CPU VR, and reduce the slew rate of P12V_AUX decaying for NVDIMM feature at surprising power fail. Hot Swap Controller design should limit the inrush current to node during soft-start to less or equal to 10A.

13.1.4 P12V as AUX rail

There is only one 12V rail delivered to the mother board as auxiliary power rail. Caution need to be taken to provide proper isolation to PCIe device, HDD, FAN, and all other devices in system, to meet voltage and timing requirement during running time and power on/off. The isolation circuit should have a soft start to avoid inrush current to P12V AUX rail, and prevent SOA damage of isolation MOSFET.

13.2 Hot-Swap Controller (HSC) Circuit

13.2.1 12V Hot-Swap Controller Circuit

In order to have a better control of 12.5V DC power input to each motherboard, one HSC (ADI/ADM1278) is used on the mother board. HSC circuit provides the following functions:

- Inrush current control when motherboard is inserted and powered up.
- Current limiting protection for over current and short circuit. Over current trip point should be able to set to 53.9A and 41.4A with Iset jumper setting for single side mother board; default is 53.9A.
- HSC UVP shall be set to 9V~10.1V and OVP shall be set to 14.3V~15V.
- SOA protection during MOSFET turning on and off.
- HSC fault protection is set to latch off (default) with retry as stuff option.
- PMBUS interface to enable BMC following actions:
 - Report server input power and log event if it triggers upper critical threshold.
 - Report input voltage (up to 1 decimal point) and log event if it triggers either lower or upper critical threshold.
 - Log status event based on hot swap controller status register.
- Use HSC or external circuit to provide fast (<20us) over current sense alert to trigger system throttling and CPU fast PROCHOT#; over current based fast PROCHOT# shall be controller by HSC Iset jumper. Fast PROCHOT# threshold shall be slightly lower than HSC DC OCP set point to be useful. Feature can be disabled by BMC GPIO directly. BIOS has a setting to control Enable/Disable/ [no change]. No change is the default. This means follow the BMC initial setting. BMC sets it to disable as the default. Before BMC is ready, the hardware POR state is enable.
- Use HSC or external circuit to provide fast (<20us) under-voltage alert to trigger system throttling and CPU fast PROCHOT#. This feature is enable by default with resistor option to disable. The threshold is set to 11.5V by default and with option to set it 11V. A jumper for UV_HIGH_SET is implemented together with BMC to control under voltage FPH trip point. When the jumper is at pin 1 and pin 2, trip point is 11.5V or follow BMC; when jumper is at pin 2 and 3, trip point is 11V.
- Use HSC or external circuit to provide fast (<20us) under-voltage alert to trigger system FAN throttling. This feature is disable by default with resistor option to enable.
- Use HSC or external circuit to provide HSC timer alert to trigger system throttling before HSC OCP happens.
- The voltage drop on HSC current sense resistor should be less or equal to 25mV at full loading. Hot swap controllers should have SMBUS address set to 0x11 (7bit format) with 0.25m ohm Rsense on.

13.2.2 48V Hot-Swap Controller Circuit

In order to have a better control of 50V DC power input to each motherboard, one HSC (ADI/ADM1272) is used on the mother board. HSC circuit provides the following functions:

- Inrush current control when motherboard is inserted and powered up.
- Current limiting protection for over current and short circuit. Over current protection shall be set to 40A.
- HSC UVP shall be set to 38V~39V and OVP shall be set to 59V~60V.
- SOA protection during MOSFET turning on and off.
- HSC fault protection is set to latch off (default) with retry as stuff option.
- PMBUS interface to enable BMC following actions:
 - Report server input power and log event if it triggers upper critical threshold.
 - Report input voltage (up to 1 decimal point) and log event if it triggers either lower or upper critical threshold.
 - Log status event based on hot swap controller status register.

- The voltage drop on HSC current sense resistor should be less or equal to 30mV at full loading. Hot swap controllers should have SMBUS address set to 0x10 (7bit format) with 0.5m ohm Rsense on.

13.3 CPU VR

13.3.1 CPU maximum power

The motherboard shall be design to handle a processor with a maximum TDP of 400W. As a result the vendor shall optimize the CPU VR accordingly.

13.3.2 CPU VR Optimizations

CPU VR optimizations shall be implemented to remove cost and increase the efficiency of the power conversion system. Vendors shall only use the minimum number of total phases to support the CPU maximum power defined in 11.3.1. CPU VR should have auto phase dropping feature, and run at optimized phase count among 1, 2, 3, ... , and the maximum phase count. CPU VR should support all Power States to allow the VRM to operate at its peak efficiency at light loading.

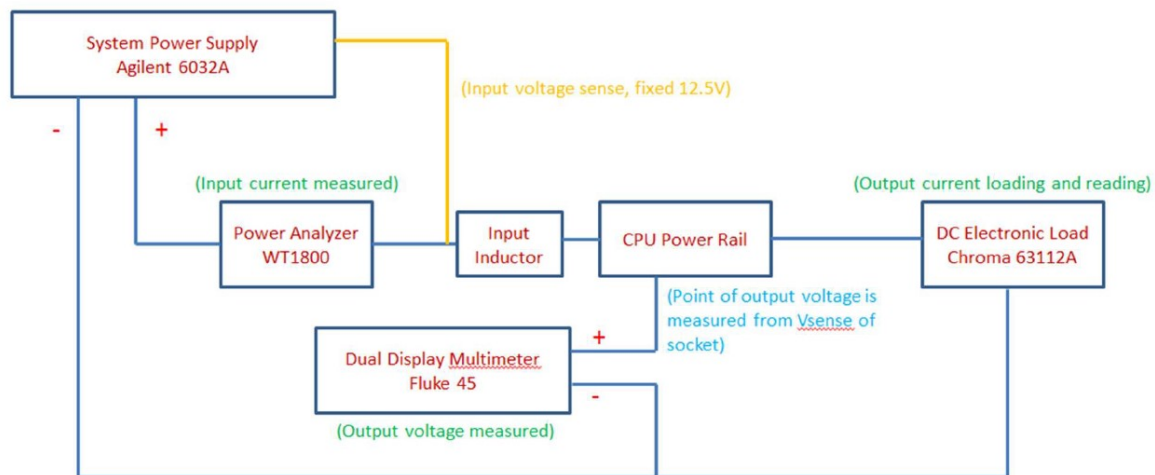
CPU VR should be compliant to latest AMD specification and validation method and pass test with margin.

13.3.3 CPU VRM Efficiency

For CPU efficiency measurement:

- VID is set to 0.9V
- Vin is set to 12V
- Efficiency is measured from input inductor to socket
- Driver and controller loss should be included
- Output voltage is gathered from Vsense of socket
- No additional air flow shall be supplied to the VR area other than the air flow caused by measure tool FAN.
- Test is done in room temperature(20C~25C)
- Voltage measurement shall be done by tool and method with 0.05% accuracy or better.
- Current measurement shall be done by tool and method with 0.05% accuracy or better.
- Efficiency should be over 86% at 35A~ 175A load.

Below is the efficiency test set up process for reference:



13.3.4 CPU VR configuration

Vendor should use CPU core VR solution with all configurations stored in NVRAM without any external resistor strapping. Vendor should provide utility under CentOS to perform VR configuration change. Configuration change should take effort without AC cycling node. The guaranteed rewrite count of NVRAM should be greater or equal to 15.

13.4 VRM design guideline

For VRM, vendor should list current budget for each power rail based on worst case loading case in all possible operation conditions. General requirements for VR component selection and VR design should meet 120% of this budget, and OCP should set to 120%~200% of this budget. Vendors should do design check, inform purchasers about the actual OCP setting chosen for VRM and explain the reason if it cannot meet this general requirement above.

For VRM which requires firmware or power code or configuration file, vendors should maintain version control to track all the releases and changes between each version, and provide a method to retrieve version through application software during system run time. This software method should run under CentOS 7.x 64 bit with updated Kernel specified by customer.

- Different BOM options and VR firmware are allowed to accommodate AVL with exceptions. Vendor's manufacture process shall be able to handle different BOM, matching AVL of power stage.
- Different BOM options do not apply to all other components
 - input/output inductor/capacitor shall not have BOM dependency to power stage AVL.
- If different VR firmware is required to support different power stages, VR firmware shall have unique ID in user specific area matching each power stage.

13.5 Hard Drive Power

The motherboard shall supply power to all possible hard drives connected. This means to support 2A continuous per HDD on 12V power rail. Inrush current required to spin up the drive must also be considered in power delivery design. 12V disk output power rails shall protect against shorts and overload conditions.

13.5.1 Spin-up delay

When hard drive spins up after power on, it draws excessive current on 12V. The peak current may reach 1.5A ~ 2A range in 12V. System may have all hard drives installed, so there is need to spin up hard drive in sequence. BIOS should implement 5 seconds delay between each hard drive spinning up.

13.6 System VRM efficiency

Vendors shall supply high efficiency VRMS for all other voltage regulators over 20W not defined in this specification. All other voltage regulation modules shall be 85% efficiency over the 30% to 90% load range. Vendors are encouraged to deliver systems with higher efficiencies. If higher efficiencies are available at additional cost vendors shall present those options.

13.7 Power On

Motherboard should be set to restore last power state during AC on/off. This means that, when AC does on/off cycle, motherboard should power on automatically without requiring power button. Only when motherboard is powered off on purpose, then motherboard should be kept power off through AC on/off.

14. Environmental and Regulations

The motherboard shall meet the following environmental requirements:

- Ambient operating temperature range: +5C to +40C
- Operating and Storage relative humidity: 20% to 90%
- Storage temperature range: -40C to +70C
- Transportation temperature range: -40C to +70C

The full system shall meet the following environmental requirements:

- Ambient operating temperature range: +5C to +40C
- Operating and Storage relative humidity: 20% to 90%
- Storage temperature range: -40C to +70C
- Transportation temperature range: -40C to +70C

15. Environmental Requirements

15.1 Vibration & Shock

- OP Vibration: 0.3Grms, 5 to 500 Hz(5-20Hz; 6dB/Oct , 20-200Hz; 0.0003G²/Hz , 200-500Hz; -6dB/Oct , 20 mins each of the three axes
- OP Shock: 5G, half-sine 11mS, 5 shocks per each of the 3 axes, Operational face (bottom) only
- Non-OP Vibration: 1G acceleration, sine wave, 5-500 Hz , 10 sweeps at 1 oct / min , per each of the 3 axes
- Non-OP Shock: 5G, half-sine 11mS, 10 shocks per each of the 3 axes, Operational face (bottom) only

15.2 Regulations

The components used on motherboard need to have rack level CE, and the sled should be compliant with RoHS and WEEE. The Capri V2 mother board should have UL 94 V-0 certificate. The vendor should design an EMI panel kit and pass FCC Class A.

16. Prescribed Materials

16.1 Disallowed Components

The disallowed components in Capri V2 follows the European Union's Restriction of Hazardous Substances Directive (RoHS).