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Compute Project

Meta Minipack2 128x 200G Data Center Switch Generic System Specification

Rev 1.0

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Note: The ideals behind open sourcing stipulate that everyone benefits when we share and work together. Any open source project is designed to promote sharing of design elements with peers and to help them understand and adopt those contributions. There is no purpose in sharing if all parties aren't aligned with that philosophy. The IC will look beyond the contribution for evidence that the contributor is aligned with this philosophy. The contributor actions, past and present, are evidence of alignment and conviction to all the tenets.

2.1 Openness

The measure of openness is the ability of a third party to build, modify, or personalize the device or platform from the contribution. OCP strives to achieve completely open platforms, inclusive of all programmable devices, firmware, software, and all mechanical and electrical design elements. Any software utilities necessary to modify or use design contributions should also be open sourced. Barriers to achieving this goal should be constantly addressed and actions taken to remove anything that prevents an open platform. Openness can also be demonstrated through collaboration and willingness to share, seek feedback, and accept changes to design and specification contributions under consideration.

Minipack2: The electrical design and mechanical design of Minipack2 is fully open, and all the PCB and chassis design files have been included in the design package.

2.2 Efficiency

Continuous improvement has been a fundamental value of the industry. New contributions (and updates to existing contributions) shall be more efficient than existing or prior generation contributions. Efficiency can be measured in many ways - OpEx and CapEx reduction, performance, capacity, power or water consumption, raw materials, utilization, size or floorspace are some examples. The goal is to express efficiency with clear metrics, valued by end-users, when the contribution is proposed.

Minipack2: The system comes in a 4RU form factor, similar to Minipack, its 128x 100G predecessor, while doubling the switching throughput both in terms of bandwidth and packets per second. The switch main board is FRU-able in Minipack2, which increases the efficiency in fleet maintenance.

2.3 Impact

OCP contributions should have a transformative impact on the industry. This impact can come from introducing new technology, time-to-market advantage of technology, and/or enabling technology through supply chains that deliver to many customers in many regions of the world. New technologies are impactful when such technology is enabled through a global

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supply channel. One example is the NIC 3.0 specification which achieved global impact by having over 12 companies author, adopt, and supply products that conformed to the specification. Another example is emerging and open security features that establish and verify trust of a product.

Minipack2 leverages the latest generation of switch ASIC, utilizes the 50G PAM4 SerDes technology at scale, and achieves efficiency gains outlined above.

2.4 Scale

OCP contributions must have sufficient enabling, distribution and sales support (pre and post) to scale to Fortune 100 as well as large hyperscale customers. Demonstration of this tenet can be accomplished by providing sales data or by providing go-to-market plans that involve either platform/component providers or systems integrator/VAR (direct and/or channel). Platform/component providers or systems integrators/VARs that can use this contribution to obtain product recognition (OCP Accepted™ or OCP Inspired™) and create Integrated Solutions which would also demonstrate scale. Software projects can also demonstrate this tenet when software is adopted across business segments or geographies, when software is a key factor in accelerating new technology, or when software provides scale of new hardware which meets OCP tenets.

Minipack2: It is designed with FRU-able line card (PIM), switch control module (micro-server), switch main board, fan, and PSU for easy field maintenance. There are multiple hardware sensors built-in, and OpenBMC has necessary utilities for hardware monitoring. It has been and will continue to be deployed in Meta's F16 data center fabric networks in large quantities.

3 Revision History

Date	Revision	Changed by	Description
09/16/2021	1.0	Xu Wang	Initial OCP release
		Ivy Wu	
		Jiu Xu	

4 Scope

This document outlines the generic technical specifications of the Meta 128x 200G open switch platform. It applies to Meta Minipack2 compact modular switch, however Minipack2 is not the only embodiment. Instead, the intention is to have a common specification for the 128x 200G switches that have equivalent form, fit and functions of Meta Minipack2.

5 System Architecture

Minipack2 is Meta's next generation 128x 200G compact datacenter modular switching platform. The following are the key system features and requirements.

- Chassis
 - **4RU**
 - ***Designed to mount in an EIA 19" rack***
 - *Can be mounted to Open Rack with a purpose-built rack mount kit*
 - Orthogonal-direct architecture: SMB is horizontal, and PIM is vertical in the system.
- Switch Main Board (SMB)
 - Broadcom Tomahawk4 (TH4) switch ASIC, 25.6Tbps with 512x 50G PAM4 SerDes lanes
 - The system architecture doesn't limit the switch ASIC to be Broadcom TH4. It could be an equivalent switch ASIC with 512x 50G PAM4 SerDes that satisfies the similar hardware interface, thermal, and application software requirements.
 - FRU-able
- Port Interface Module (PIM)
 - PIM-16Q
 - 16x QSFP56 200G ports
 - Backward compatibility: Each QSFP56 port can support a 100G QSFP28 module.
 - Forward compatibility: Two QSFP56 ports can be "combined" to support a 400G QSFP-DD module.
 - More options can be developed, such as a PIM for 8x QSFP-DD 400G ports with MACSec encryption / decryption.
 - FRU-able
- Control plane – Switch Control Module (SCM)
 - Intel Broadwell-DE CPU D1527
 - The system architecture doesn't limit the CPU selection to Intel Broadwell-DE. An alternative CPU is possible as long as it satisfies the hardware interface, thermal, and application software requirements.
 - Minimum 32GB DDR4 DRAM w/ ECC
 - Minimum 256GB M.2 NVMe SSD
 - Front panel RJ-45 RS232 console
 - Front panel RJ-45 OOB (management) Ethernet, 1000BASE-T
 - Front panel USB 2.0 Type-A port

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- FRU-able
- Management plane
 - The Baseboard Management Controller is hosted by a RunBMC module.
 - Aspeed AST2620 Baseboard Management Controller (Dual ARM core)
 - Minimum 2GB DDR4 DRAM
 - Minimum 8GB eMMC
 - An out-of-band / management GbE switch connecting the front panel GbE RJ-45 port, the BMC, and the CPU
- Power plane
 - Redundant AC/DC PSU (Nominal AC input: 208V, 230V, 277V)
 - 12V output
 - Typical power consumption should be less than 1,750W.
 - Ambient temperature: 30°C
 - With 128 200G-FR4 QSFP56 optics installed on 8 PIM-16Q
 - Optics power consumption included
 - AC/DC power conversion loss included
- Thermal
 - Air cooling
 - Front to back airflow
 - Can support 6.5W 200G-FR4 QSFP56 optics with 65°C case temperature limit on PIM-16Q at 35°C maximum ambient temperature
 - The airflow needed for system cooling should not exceed 0.145CFM/W at sea level, where the wattage is the total system power consumption.

The following table lists the key parameters of Minipack2.

Attributes	Quantity	Notes
Chassis Form Factor	4RU Less than 30" deep	
Port Interface Module	Minimum 8	8 PIM in a Minipack2 chassis <i>The chassis can also reserve more PIM slots for alternative switch architectures. However, 8 PIMs are required for Meta's applications.</i>
Total number of QSFP56 ports	128	128 QSFP56 200G ports. Each PIM-16Q has 16 QSFP56 ports.
Total number of QSFP28 ports	128	All the QSFP56 ports are backward compatible to be QSFP28 100G ports.
Total number of QSFP-DD ports	64	64 QSFP-DD 400G ports. Each PIM-16Q supports 8 QSFP-DD ports.
Total number of Switch ASIC SerDes Lanes	512	512 x 53.125Gbps PAM4

Total number of Switch ASIC PCIe Lanes	4	PCIe Gen-3 x4 for switch ASIC
Switch Control Module	1	Control plane CPU DRAM NVMe SSD Front panel RJ-45 for management Ethernet Front panel RJ-45 for serial console Front panel USB 2.0 Type A port
BMC	1	Hardware management and monitor functions
Management GbE Switch	1	Connecting the management Ethernet ports of the CPU and the BMC, and the front panel RJ-45 port
Typical power consumption	1750W	Full line rate snake test with 128 200G-FR4 QSFP56 optics installed on 8 PIM-16Q
System airflow	0.145CFM/W	At sea level

Table 1: Minipack2 System Parameters



Note: Alternative chassis architectures may reserve more than 8 PIM slots.

Figure 5-1: Minipack2 Chassis Front View

6 Functional Descriptions

Minipack2 system has the following FRUs:

- Switch Main Board (SMB)
- System Controller Module (SCM)
- Port Interface Module (PIM)
 - 16x QSFP56 Port Interface Module (PIM-16Q)
- Redundant AC/DC Power Supply Units (PSU)
- Redundant Fan Trays

The PIM and SCM plug into the front side of the chassis, while the SMB, PSU, and the Fan Trays plug into the rear side of the chassis.

FRU Type	Name	Quantity required in Meta's applications
Switch Main Board	SMB	1
Port Interface Module	PIM	8
System Control Module	SCM	1
PSU	PSU	Redundant
Fan Tray	FAN	Redundant

Table 2: FRU List

6.1 System Hardware Architecture

Minipack2 is a modular switch with a single-chip 25.6T switch ASIC, 8 Port Interface Modules (PIM), and 1 System Control Module (SCM). The following is the functional block diagram of Minipack2.

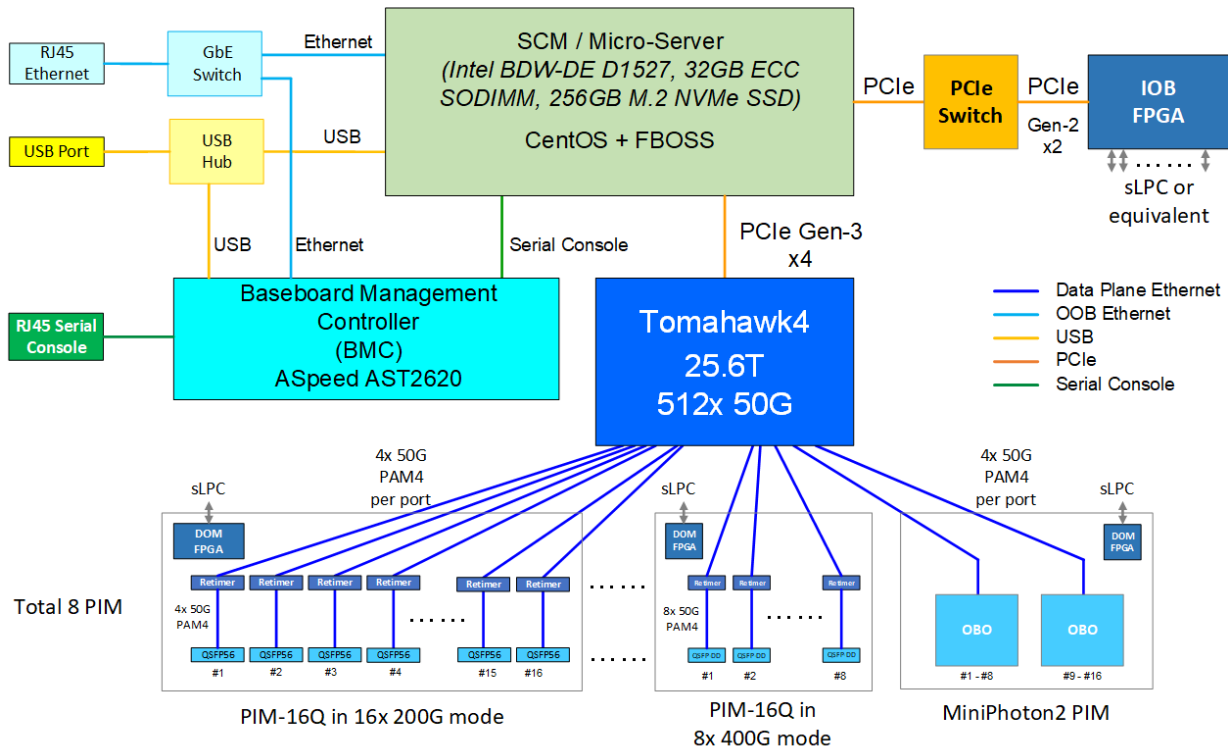


Figure 6-1: System Architecture of Minipack2

The retimers on PIM-16Q and the PCIe switch in the above diagram are specific to the Minipack2 implementation by Meta and its Original Design Manufacturer (ODM) partner. These may not be present in alternative implementations of the generic Minipack2 architecture.

Switch Main Board (SMB) hosts the Broadcom Tomahawk4 (TH4) switch ASIC and its supporting circuit. It has 512 53.125G PAM4 SerDes interfaces (1024 differential pairs) for the Ethernet ports, and the PAM4 signals are routed to the PIMs through high-speed orthogonal-direct connectors.

The TH4 is controlled through its PCIe Gen-3 x4 interface by the Broadwell-DE CPU on the SCM. The 10GBase-KR ports of TH4 usually reserved for management purposes are not used in Minipack2.

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The CPU also has a PCIe link to the IOB (IO Bus) FPGA, and the IOB FPGA connects to the DOM (Digital Optics Monitoring) FPGA on PIM-16Q to control and monitor the pluggable optics. The interface between the IOB FPGA and the DOM FPGAs is a proprietary bus defined by the switch vendor.

The Minipack2 system architecture doesn't limit the CPU selection to Intel Broadwell-DE. An alternative CPU is possible as long as it satisfies the hardware interface, thermal, and application software requirements.

The system also has a Baseboard Management Controller (BMC) Aspeed AST2620 for hardware housekeeping functions, such as firmware upgrade, voltage and temperature sensor monitoring, and fan speed control.

6.2 PIM-16Q: 16x 200G Port Interface Module

PIM-16Q hosts the 16 QSFP56 ports for the pluggable optics modules. There are both backward compatibility and forward compatibility requirements for the QSFP ports.

- Normal mode: Each QSFP56 port supports a 200G interface with 4x 53.125Gbps PAM4 host interface lanes, e.g., a 200G-FR4 optics module.
- Backward compatibility: Each QSFP56 port supports a 100G interface with 4x 25.78125Gbps NRZ host interface lanes, e.g., a 100G-CWDM4 optics module.
- Forward compatibility: Two QSFP56 ports can be "combined" to support a 400G interface with 8x 53.125Gbps PAM4 host interface lanes, e.g., a 400G-FR4 QSFP-DD optics module.

6.3 Orthogonal Direct Architecture

Minipack2 uses orthogonal-direct architecture for the chassis design. It does not have a midplane or backplane, and the PIM high-speed connector directly mates to the high-speed connectors of SMB, providing more space for airflow inside the chassis. Orthogonal-direct architecture also minimizes the high speed PCB trace lengths to provide lower insertion loss than traditional backplane architectures.

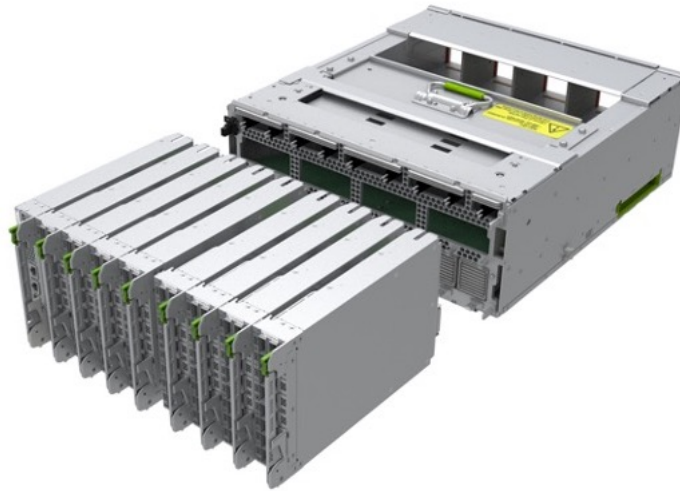


Figure 6-2: Front ISO View of Minipack2 Orthogonal-Direct Architecture



Figure 6-3: Rear ISO View of Minipack2 Orthogonal-Direct Architecture

6.3.1 Switch ASIC Port Mapping

In a Minipack2 system, eight PIMs and SMB are connected orthogonally. Each PIM connects to eight 8x53.125Gbps PAM4 SerDes macros of the TH4 switch ASIC. As TH4 incorporates multiple packet processing pipelines, the front panel port assignment between the PIMs and SMB should balance the load of multiple packet processing pipelines of TH4.

7 Thermal Design Requirements

The thermal design of Minipack2 is optimized to support a 25.6T-generation switch ASIC, 200G-FR4 optics (up to 6.5 W) with 65°C case max temperature limit and 400G-FR4 optics (up to 12 W) with 70°C case max temperature limit. The worst-case ambient temperature is 35°C. The worst-case altitude condition is 6000 ft.

The airflow is from front to rear of the chassis, driven by multiple fans, with at least N+1 redundancy. The BMC monitors the thermal condition of the system based on readings from key temperature sensors, including system inlet ambient temperature, switch ASIC on-die temperature and front panel optics temperatures. The fan speed is controlled by a combined algorithm of linear lookup table and PID controller. The system fan speed control should also support indefinite time for service of one fan tray or service of one PSU.

The system airflow should not exceed 0.145 CFM/W at sea level, and 0.181 CFM/W at 6000 ft altitude level, when the system is fully populated (and at maximum traffic). Here the CFM refers to the total air flow going through the system and the wattage is the total system power consumption. The goal is to consume only the airflow necessary to keep the components at proper temperatures and reduce fan power consumption.

8 System I/O

8.1 Optics Transceivers Supported by PIM-16Q

8.1.1 100G optics

- QSFP28 100G-CWDM4 (MSA) or 100G-CWDM4-Lite transceiver

8.1.2 200G optics

- QSFP56 200G-FR4 transceiver

8.1.3 400G optics

- QSFP-DD 400G-FR4 transceiver
- QSFP-DD 400G-LR4 transceiver

8.2 Management interfaces

There are 3 management interfaces on the SCM front panel:

- One console RJ-45 port, 9600Baud RS232
- One 1000BASE-T Ethernet RJ-45 port
- One USB 2.0 Type-A port to the micro-server

9 Host CPU and BMC Functional Features

9.1 Micro-server CPU BIOS Feature List

The BIOS requirements are outlined below. However, new requirements may arise in the full product life cycle.

- **Intel TXT support, and supporting Intel Dynamic Boot (DRTM – Dynamic Root of Trust for Measurements)**
- UEFI compatible
- Configuration and features
 - Disable unused devices including video interfaces and GPU if supported by hardware
 - BIOS setup menu
 - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- Linux-based BIOS settings tool
- Default boot device priority
 - Network / PXE -> NVMe
- PXE boot
 - Supports IPv4 and IPv6 UEFI PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (eth0).
 - PXE timeout timer set to 10 seconds
 - Supports UEFI mode
 - Supports both PXE boot over IPv4 and IPv6, and be able to boot from a PXE server on a different IPv4 or IPv6 subnet
- Other boot options
 - Provides the capability to select boot options
- Remote BIOS update
 - Scenario 1: Sample / audit BIOS settings
 - Scenario 2: Update BIOS with pre-configured set of BIOS settings
 - Scenario 3: BIOS / firmware update with a new revision
 - Update from the CentOS operating system over the LAN
 - Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
 - No user interaction (e.g., prompts)

- BIOS updates and option changes do not take longer than five (5) minutes to complete.
 - Can be scripted and propagated to multiple machines
- Event log
 - Implement SMBIOS Type 15 System Event Log per SMBIOS specification Rev 2.6
 - Hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB)
 - Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID.
 - A system access interface and application software to retrieve and clear the event log from the BIOS
- Logged errors
 - Single-bit ECC error
 - Multi-bit ECC error
 - PCIe error
 - SATA error
 - POST error
 - NMI error
 - System reboot events
 - Sensor values exceeding warning or critical thresholds
- Error thresholds
 - Setting must be enabled for both correctable and uncorrectable errors.
 - Threshold for Memory Correctable ECC is 1.
 - PCIe error threshold is 1.
- Console redirection to the serial ports
 - Console redirection shall be enabled whenever the CPU starts booting and kept enabled after the OS starts running.
- POST codes
 - To be provided on the serial console
 - To be provided on the LPC bus
- DMI
 - Model
 - Serial Number
 - Additional information if requested by Meta
- ATA Security State 2
 - The BIOS shall not send out ATA FREEZE command to the SSDs attached to the SATA ports.

- Support AMI RuntimeMemoryHole eModule, so that we can avoid using the kernel module of SCELNX and AFULNX.
- **ONIE support is required.**

9.2 BMC Feature Support

The BMC needs to support the following features:

- All SEL commands
- All sensor commands
- All SDR commands
- TPM 2.0 support
- Power on/off/cycle / hardware reset / soft reset commands
- I2C access to power sequencers, hot swap controllers, and DC-DC convertors
- Inventory EEPROM access
- Fan-tray present status check, fan PWM control and speed tachometer read
- Dual SPI boot
- On-board PHY MDIO interface access
- CPLD and FPGA in-system firmware upgrade

10 Regulatory Compliance, Environmental, and Reliability Requirements

10.1 Regulatory Compliance Requirements

Compliance reports must be from labs accredited to a current version of IEC 17025. The reports and certificates must name the ODM as the applicant.

- **CE Declaration to the following Regulatory Directives by ODM / OEM:**
 - EMC Directive 2014/30/EU
 - Low Voltage (LVD) Directive 2014/35/EU
- **Safety certification**
 - CB certificate/report to IEC 62368-1 including all national deviations
 - CB certificate/report to IEC/EN 60950-1 including all national deviations
 - UL/CSA/IEC/EN 60950-1 with all latest amendments
 - UL/IEC 62368-1 with all latest amendments
 - CNS14336 Taiwan BSMI safety regulation
 - EN 60825-1 Safety of Laser products – part 1
 - UL 94-Vo Flammability rating
- **EMC certification**
 - FCC Part 15 (Class A)
 - ICES-003 (Canada) Class A
 - EN55032 (Europe) Class A
 - CISPR32 (International) Class A
 - AS/NZS CISPR32 (Australia and New Zealand) Class A
 - VCCI CISPR 32 (Japan) Class A
 - CNS 13438 (Taiwan) Class A
 - EN61000-3-2
 - EN61000-3-3
 - EN55024
 - EN 61000-4-2 ESD
 - EN 61000-4-3 Radiated Immunity
 - EN 61000-4-4 EFT
 - EN 61000-4-5 Surge
 - EN 61000-4-6 Low Frequency Conducted Immunity
 - EN 61000-4-11 Voltage Variations and Dips

▪ Immunity levels

Network Equipment						
Immunity Standard	Description	Standard Criteria (Required)	FB Criteria (Goal)	Standard Level (Required)	FB Level (Goal)	Remarks
IEC 61000-4-2	Electrostatic Discharge (ESD)	B	A	4 kV Cont. / 8 kV Air	8 kV Cont. / 15 kV Air	Criteria A (FB Goal) is highly desirable for any level
IEC 61000-4-3	Radiated Immunity	A	A	3 V/m	10 V/m	For communication cables >3 meters
IEC 61000-4-4	EFT	B	B	0.5 kV		Ports: Signal & Telecom (>3 meters), DC power input
		B	B	1 kV		Ports: AC power input & AC/DC Converter
IEC 61000-4-5	Surges	C	A	1 kV		Ports: Signal and Telecom connected to outdoor cables
		B	A	0.5 kV		Ports: DC power input
				1 kV L-L / 2 kV L-GND		Ports: AC power input & AC/DC Converter
IEC 61000-4-6	Conducted Immunity	A	A	3 V	10 V	Ports: Signal & Telecom (>3 meters), AC and DC power input
IEC 61000-4-8	Magnetic Field	A	A	1 A/m		Only EUT containing devices susceptible to magnetic fields
	Voltage Dips	B	B	>95% Reduction		Ports: AC power input & AC/DC

IEC 61000-4-11						Converter (0.5 Period)
		C	C	30% Reduction		Ports: AC power input & AC/DC Converter (25 Periods)
	Voltage Interruptions	C	C	>95% Reduction		Ports: AC power input & AC/DC Converter (250 Periods)

The ODM must strive to design to the FB Goal at the start and during the project. Meta will decide if levels below the goal are acceptable. Off the shelf power supplies must meet the required level at a minimum.

- **Sound levels**

Network Equipment				
	OHSA (Required)	Directive 2003/10/EC (Goal)	FB Design Goal	Remarks
Sound Limit (dBA)	85	80	78	Under normal operation at 25 °C, the system must not produce a A-weighted sound power level above the required limit. The FB design goal should be targeted during development of the product. The Directive goal represents the limit that requires hearing protection to be provided to our Data Center Staff in Europe. The ODM must provide the result of the formal testing.

The ODM must strive to design to the FB Goal at the start and during the project. Meta will decide if levels above the goal are acceptable. The sound power level limits apply to the normal operating conditions where the system is configured and equipped in its deployed state with the worst case configuration to produce the loudest noise. Maintenance conditions, open covers, are not considered normal conditions and do not need to be measured. Sound from

alarms does not need to be measured. Maximum fan speed expected under normal operation should be measured.

10.2 Materials of Concern Requirements

Regulatory

- RoHS Directive (2011/65/EU), including provisions of RoHS 3 Directive (2015/863) upon coming into effect.
- REACH Regulation (EC) No 1907/2006
- Waste Electrical and Electronic Equipment (“WEEE”) Directive (2012/19/EU)
- The Persistent Organic Pollutants Regulation (EC) No. 850/2004
- The California Safe Drinking Water and Toxic Enforcement Act of 1986 (“Prop 65”)
- The Packaging and Packaging Waste Directive 94/62/EC
- Batteries Directive 2006/66/EC

Corporate Sustainability Requirements

- **RoHS Exemptions position:** Compliance to the latest version of RoHS Directive is mandatory, and FB requires the use of no exemption where practical. If not practically possible, using the following exemption is allowed based on EU directive (2011/65/EU, 2015/863/EU) or future decision by European commission. As of the last revision date of this standard, relevant exemptions include 5a, 5b, 6a, 6b, 6c, 7a, 7c-I, 7c-II, 7c-IV, 8b, 9, 9b, 13(a), 13(b), 15, 21
- **Halogens (Bromine & Chlorine and their compounds)***
- **Phthalates (DEHP, DBP, DiBP, BBP)***
- **Arsenic and its compounds***
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act;** requires companies using tin, tantalum, tungsten, and gold (“3TG”) in in-scope products to verify and disclose the mineral source.

See the table (below) for scope, concentration limits, exemptions, and compliance deadlines for requirements marked with an asterisk (*).

HAZARDOUS SUBSTANCE	CAS NUMBER	SCOPE	CONCENTRATION LIMIT OF INTEREST (FOR ALL HOMOGENEOUS MATERIALS)	EXEMPTIONS	COMPLIANCE DEADLINE
Halogens (incl. PVC, BFRs/CFRs)	Br: 7726-95-6 Cl: 7782-50-5	All Parts	900 ppm for Br or Cl, or 1500 ppm combined	N/A	Dec 31, 2019
Phthalates (DEHP, DBP, DiBP, BBP)	DEHP: 117-81-7 DBP: 84-74-2 DiBP: 84-69-5 BBP: 85-68-7	All Parts	1000 ppm (or 0.1% by weight)	N/A	Jul 22, 2019 (RoHS 3.0)
Arsenic	Includes but is not limited to: 7440-38-2	Glass and non-metals	50 ppm (or 0.005% by weight)	Semiconductors, optical elements	Dec 31, 2020
		Metals and alloys	1000 ppm (or 0.1% by weight)	Copper foil for printed circuit boards	

Table 3: Corporate sustainability scope, concentration limits, exemptions, and compliance deadlines

10.3 Environmental Requirements

The Minipack system should meet the following environmental requirements:

- Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Operating and storage relative humidity: 10% to 85% (non-condensing)
- Operating temperature range (with 100G CWDM4 MSA optics): 0°C to +45°C
- Operating temperature range (with 100G CWDM4-Lite optics): +15°C to +35°C
- Storage temperature range: -40°C to +70°C (long-term storage)
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-rating: up to 6,000 feet
- Shock and Vibration: IEC 68-2-36, IEC 68-2-6

10.4 Operational Life and Annual Failure Rate (AFR) Requirements

The operational life of Minipack2 is expected to be at least 5 years, and the annual failure rate (AFR) of any of the FRUs and the chassis assembly itself shall be under 1%.

11 Labels and Markings

11.1 PCBA Labels and Markings

Minipack PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

Table 4: PCBA Label Requirements

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Meta P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

11.2 Chassis Labels and Markings

The pull-out tag at the front panel of the chassis includes system model number and serial number. Meta asset tag should also be included in the chassis front markings.

12 Appendix A - Requirements for IC Approval

List all the requirements in one summary table with links from the sections.

Requirements	Details	Link to which Section in Spec
Contribution License Agreement	Which one?	1 License
Tenets	Which ones? Openness Efficiency Impact Scale	2 OCP Tenets Compliance
Supplier Requirements:		
Supplier must be an OCP Member.		
Supplier must become an OCP Solution Provider.		
Supplier must provide product based on this spec within 120 days		
Supplier must make product available to the PUBLIC		
Name of Supplier(s)		

13 Appendix B - OCP Supplier Information (to be provided by the Supplier of Product within 120 days)

Your product must apply for OCP Product Recognition within 120 days.

Company:

Contact Info:

Product Name:

Product SKU#:

Description:

OCP Product Recognition:

Please have your supplier complete the following [2021 Supplier Requirements](#) before seeking OCP Product Recognition. Insert the completed spreadsheet link in the table below.

- Supplier Details
- Security (Bronze for OCP Inspired™ or Silver/Gold for OCP Accepted™)
- BMC if applicable

List all the requirements in one summary table with links from the sections.

Requirements	Details	Links
Which Product recognition?	OCP Accepted™ or OCP Inspired™	
If OCP Accepted™, who provided the Design Package?		Link
2021 Supplier Requirements for your product(s)		Link