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Compute Project

Facebook Minipack 128x 100G Switch System Generic Specification

Rev 2.0

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Table of Content

Table of Content.....	2
Table of Figures	4
Table of Tables.....	5
1 License	6
2 OCP Tenets Compliance	8
2.1 Openness.....	8
2.2 Efficiency.....	8
2.3 Impact	8
2.4 Scale.....	9
3 Revision History	10
4 Scope.....	11
5 Overview	12
6 Functional Descriptions.....	15
6.1 System Hardware Architecture	16
6.2 PIM-16Q: 16x 100G Port Interface Module	17
6.3 Orthogonal Direct Architecture	18
6.3.1 Port Mapping between SMB and PIM	20
7 Thermal Design Requirements.....	21
8 System I/O	22
8.1 Optics Transceivers Supported by PIM-16Q QSFP Ports	22
8.1.1 100G optics.....	22
8.1.2 200G optics.....	22
8.1.3 400G optics.....	22
8.1.4 40G optics	22
8.2 Management interfaces.....	22
9 Host CPU and BMC Functional Features	23
9.1 Micro-server CPU BIOS Feature List	23
9.2 BMC Feature Support.....	25
10 Regulatory Compliance, Environmental, and Reliability Requirements	26

10.1	Regulatory Compliance Requirements.....	26
10.2	Materials of Concern Requirements	29
10.3	Environmental Requirements	30
10.4	Mean Time Between Failures (MTBF) Requirements	30
11	Labels and Markings	31
11.1	PCBA Labels and Markings.....	31
11.2	Chassis Labels and Markings.....	31
12	Appendix A - Requirements for IC Approval.....	32

Table of Figures

<i>Figure 5-1: Minipack Chassis Front View</i>	<i>14</i>
<i>Figure 6-1: System Architecture of Minipack</i>	<i>16</i>
<i>Figure 6-2: Minipack Data Path</i>	<i>17</i>
<i>Figure 6-3: PIM-16Q Front Panel</i>	<i>18</i>
<i>Figure 6-4: Front ISO View of Minipack Orthogonal-Direct Architecture</i>	<i>19</i>
<i>Figure 6-5: Rear ISO View of Minipack Orthogonal-Direct Architecture</i>	<i>19</i>

Table of Tables

<i>Table 1: Minipack System Parameters</i>	<i>13</i>
<i>Table 2: FRU List</i>	<i>15</i>
<i>Table 3: Corporate sustainability scope, concentration limits, exemptions, and compliance deadlines</i>	<i>30</i>
<i>Table 4: PCBA Label Requirements</i>	<i>31</i>

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2.1 Openness

The measure of openness is the ability of a third party to build, modify, or personalize the device or platform from the contribution. OCP strives to achieve completely open platforms, inclusive of all programmable devices, firmware, software, and all mechanical and electrical design elements. Any software utilities necessary to modify or use design contributions should also be open sourced. Barriers to achieving this goal should be constantly addressed and actions taken to remove anything that prevents an open platform. Openness can also be demonstrated through collaboration and willingness to share, seek feedback, and accept changes to design and specification contributions under consideration.

Minipack: The electrical design and mechanical design of Minipack is fully open, and all the PCB and chassis design files have been included in the design package.

2.2 Efficiency

Continuous improvement has been a fundamental value of the industry. New contributions (and updates to existing contributions) shall be more efficient than existing or prior generation contributions. Efficiency can be measured in many ways - OpEx and CapEx reduction, performance, capacity, power or water consumption, raw materials, utilization, size or floorspace are some examples. The goal is to express efficiency with clear metrics, valued by end-users, when the contribution is proposed.

Minipack: There is significant power and space saving in Minipack, compared to Backpack, the previous generation of Facebook's 128x 100G switch. It consumes about 50% of the power of Backpack, and occupies half the rack space, while providing the same switching throughput.

2.3 Impact

OCP contributions should have a transformative impact on the industry. This impact can come from introducing new technology, time-to-market advantage of technology, and/or enabling technology through supply chains that deliver to many customers in many regions of the world. New technologies are impactful when such technology is enabled through a global supply channel. One example is the NIC 3.0 specification which achieved global impact by

Minipack 128x 100G Switch System Generic Specification

having over 12 companies author, adopt, and supply products that conformed to the specification. Another example is emerging and open security features that establish and verify trust of a product.

Minipack leverages the latest generation of switch ASIC, utilizes the latest 50G PAM4 SerDes technology at scale, and achieves efficiency gains outlined above.

2.4 Scale

OCP contributions must have sufficient enabling, distribution and sales support (pre and post) to scale to Fortune 100 as well as large hyperscale customers. Demonstration of this tenet can be accomplished by providing sales data or by providing go-to-market plans that involve either platform/component providers or systems integrator/VAR (direct and/or channel). Platform/component providers or systems integrators/VARs that can use this contribution to obtain product recognition (OCP Accepted™ or OCP Inspired™) and create Integrated Solutions which would also demonstrate scale. Software projects can also demonstrate this tenet when software is adopted across business segments or geographies, when software is a key factor in accelerating new technology, or when software provides scale of new hardware which meets OCP tenets.

Minipack: It is designed with FRU-able line card (PIM), switch control module (micro-server), fan, and PSU for easy field maintenance. There are multiple hardware sensors built-in, and OpenBMC has necessary utilities for hardware monitoring. It has been deployed in Facebook's F16 data center fabric networks in large quantities.

3 Revision History

Date	Revision	Changed by	Description
02/10/2019	1.0	Xu Wang Jimmy Leung Rongchun Zhou Lingjun Wu	Initial OCP release
03/01/2021	2.0	Xu Wang	Updated the specification to only include the requirements for Facebook data center applications, while eliminate some implementation details that are equipment manufacturer specific.

4 Scope

This document outlines the generic technical specifications of the Facebook 128x 100G open switch platform. It applies to Facebook Minipack compact modular switch, but Minipack is not the only embodiment. Instead, the intention is to have a common specification for the 128x 100G switches that have equivalent form factor and functions of Facebook Minipack.

5 Overview

Minipack is Facebook's next generation compact datacenter modular switching platform. The following are the key system features and requirements.

- Chassis
 - **4RU**
 - ***Designed to mount in EIA 19" rack***
 - *Can be mounted to Open Rack with a purpose-designed rack mount kit*
 - Orthogonal-direct architecture: SMB is horizontal, and PIM is vertical in the system.
- Switch Main Board (SMB)
 - Tomahawk3 (TH3) switch ASIC, 12.8Tbps
- Port Interface Module (PIM)
 - PIM-16Q: 16x QSFP28 100G port interface module
 - PIM-4DD: 4x QSFP-DD 400G port interface module
 - More options can be developed, such as with MACsec PHY, etc.
 - FRU-able
- Control plane – Switch Control Module (SCM)
 - Intel Broadwell-DE CPU D1527
 - The Minipack system architecture doesn't limit the CPU selection to Intel Broadwell-DE. An alternative CPU is possible as long as it satisfies the hardware interface, thermal, and application software requirements.
 - Minimum 32GB DDR4 DRAM w/ ECC
 - Minimum 256GB M.2 SATA SSD
 - Front panel RS232 console
 - Front panel RJ-45 OOB (management) Ethernet
 - FRU-able
- Management plane
 - Aspeed AST2520 Baseboard Management Controller (ARM core)
- Power plane
 - Redundant AC/DC PSU (Nominal AC input: 208V, 230V)
 - 12V output
 - Typical power consumption should be less than 1,400W.
 - Ambient temperature: 30°C
 - 128 100G-CWDM4 Lite QSFP28 optics installed on 8 PIM-16Q
- Thermal
 - Air cooling
 - Front to back air flow

Minipack 128x 100G Switch System Generic Specification

- Able to support 100G-CWDM4 Lite QSFP28 with 55°C case temperature limit on PIM-16Q at 35°C maximum ambient temperature

The following table lists the key attributes of Minipack system.

Attributes	Quantity	Notes
Port Interface Module	Minimum 8	8 PIM in a Minipack chassis <i>The chassis can also reserve more PIM slots for alternative switch architectures. However, 8 PIMs are required for Facebook's applications.</i>
TH3 SerDes Links	256	256 x 53.125Gbps PAM4
QSFP28 SerDes Links	512	128 x 4 x 25.78125Gbps NRZ
Total number of PCIe Lanes for Tomahawk3	4	PCIe x4 for Tomahawk3 ASIC
Total number of QSFP28 ports	128	128 QSFP28 100G ports. Each PIM-16Q has 16 QSFP28 100G ports.
Total number of QSFP56 ports	64	64 QSFP56 200G ports. Each PIM-16Q has 8 QSFP56 200G ports.
Total number of QSFP-DD ports	32	32 QSFP-DD 400G ports. Each PIM-4DD has 4 QSFP-DD 400G ports.

Table 1: Minipack System Parameters



Note: Alternative chassis architectures may reserve more than 8 PIM slots.

Figure 5-1: Minipack Chassis Front View

6 Functional Descriptions

Minipack system has the following components:

- Switch Main Board (SMB)
- System Controller Module (SCM)
- Port Interface Module (PIM)
 - 16 x QSFP28 Port Interface Module (PIM-16Q)
 - 4 x QSFP-DD Port Interface Module (PIM-4DD)
- Redundant AC/DC Power Supply Units (PSU)
- Power Distribution Boards
- Redundant Fan Trays

The Port Interface Module (PIM) and System Controller Module(SCM) plug into the front side of the chassis. The Power Supply Unit (PSU) and Fan Tray plug into the rear side of the chassis.

FRU Type	Name	Quantity required in Facebook's applications
Port Interface Module	PIM	8
System Control Module	SCM	1
PSU	PSU	Redundant
Fan Tray	FAN	Redundant

Table 2: FRU List

6.1 System Hardware Architecture

Minipack is a modular switch with only one 12.8T Tomahawk3 switch ASIC, 8 Port Interface Modules (PIM), and 1 System Control Module (SCM). The following is the functional block diagram of Minipack:

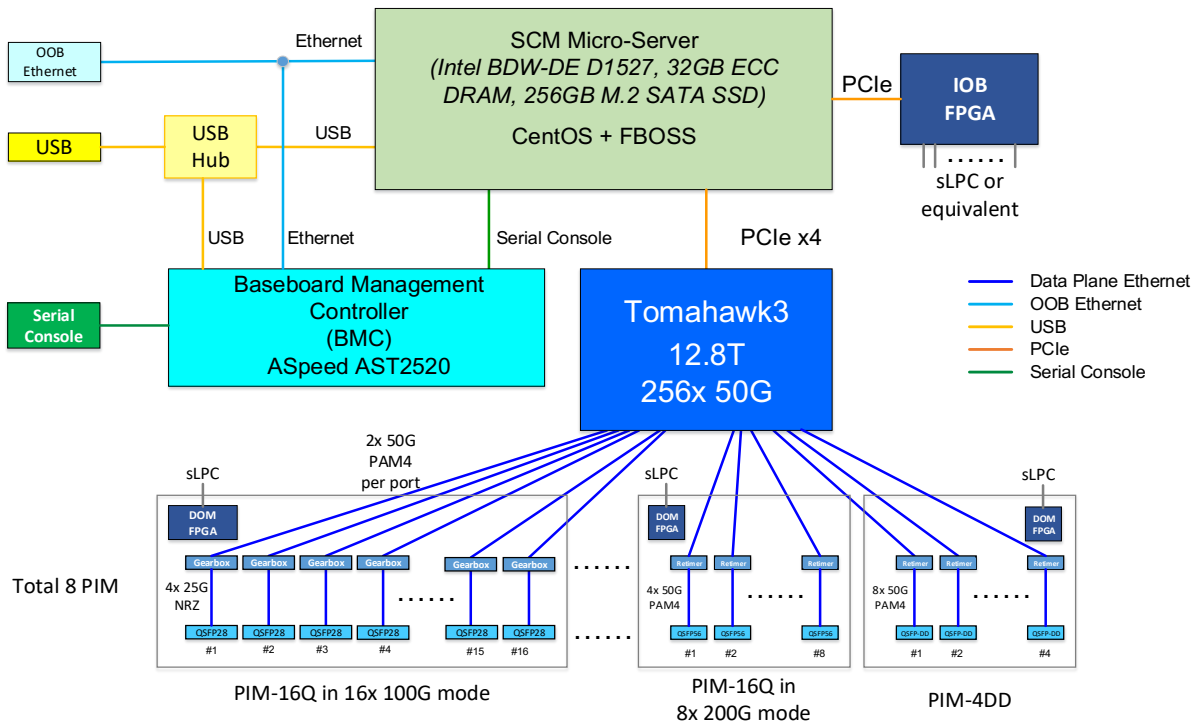


Figure 6-1: System Architecture of Minipack

Switch Main Board (SMB) hosts the Tomahawk3 (TH3) switch ASIC and its supporting circuit. It has 53.125G PAM4 SerDes interfaces for the Ethernet ports, and the PAM4 signals are routed to the PIMs through the orthogonal-direct connectors. There are reverse gearboxes on the PIM-16Qs to convert 53.125G PAM4 signals to 25.78125G NRZ signals for the 100G-CWDM4 optics in the QSFP28 ports.

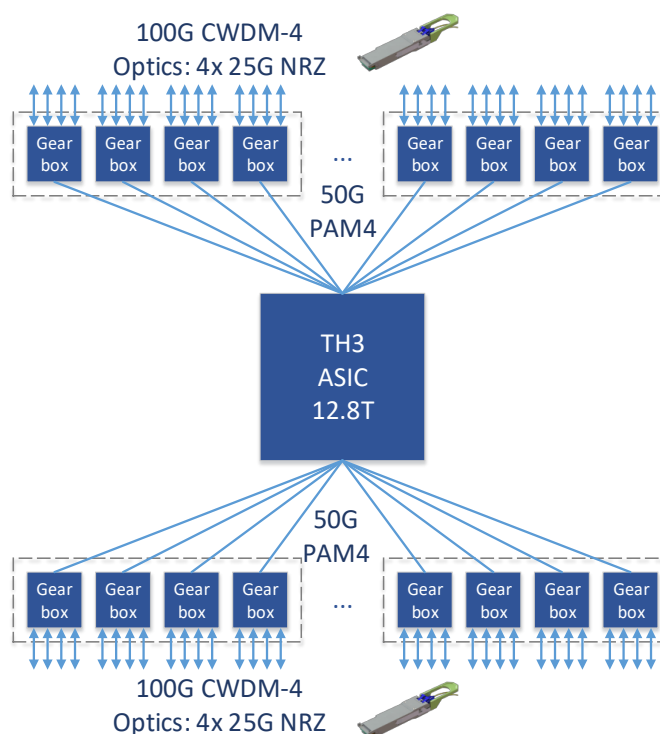


Figure 6-2: Minipack Data Path

The TH3 is controlled through its PCIe interface by the Broadwell-DE CPU on the SCM. The CPU also has a PCIe link to the IOB (IO Bus) FPGA, and the IOB FPGA connects to the DOM (Digital Optics Monitoring) FPGA on PIM-16Q to control and monitor the pluggable optics. The interface between the IOB FPGA and the DOM FPGAs is a proprietary bus defined by the switch vendor.

The Minipack system architecture doesn't limit the CPU selection to Intel Broadwell-DE. An alternative CPU is possible as long as it satisfies the hardware interface, thermal, and application software requirements.

The system also has a Baseboard Management Controller (BMC) Aspeed AST2520 for hardware housekeeping functions, such as firmware upgrade, voltage and temperature sensor monitoring, and fan speed control.

6.2 PIM-16Q: 16x 100G Port Interface Module

PIM-16Q hosts the reverse gearbox devices and the QSFP28 connectors. There are primarily two operating modes of the reverse gearbox:

- 2x 50G PAM4 to 4x 25G NRZ reverse gearbox. It terminates and regenerates the FEC (Forward Error Correction) between the system side (TH3) and the line side (QSFP28), as the 2x 50G PAM4 100G port uses RS(544, 514) FEC and the 4x 25G NRZ 100G port uses RS(544, 528) FEC as specified by the relevant industry standards.

- 4x 50G PAM4 to 4x 50G PAM4 retimer. No FEC termination and regeneration is needed. A 200G port is formed by 4x 50G PAM4 lanes.

Consequently, a PIM-16Q can support either 16 QSFP28 100G ports or 8 QSFP56 200G ports. It is required the configuration of port modes can be done on each pair of QSFP28 ports, one on the left and one on the right. For example, the modes of ports P1 and P2 (shown below) can be configured independently from P3 and P4.

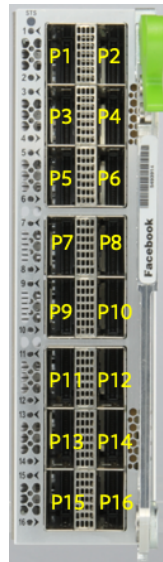


Figure 6-3: PIM-16Q Front Panel

6.3 Orthogonal Direct Architecture

Minipack uses orthogonal-direct architecture for chassis design. It does not have a midplane or backplane, and the PIM high-speed connector directly mates to the high-speed connector of SMB, providing more space for air flow inside the chassis. Orthogonal-direct architecture also minimizes the high speed PCB trace lengths to provide lower insertion loss than traditional backplane architectures.

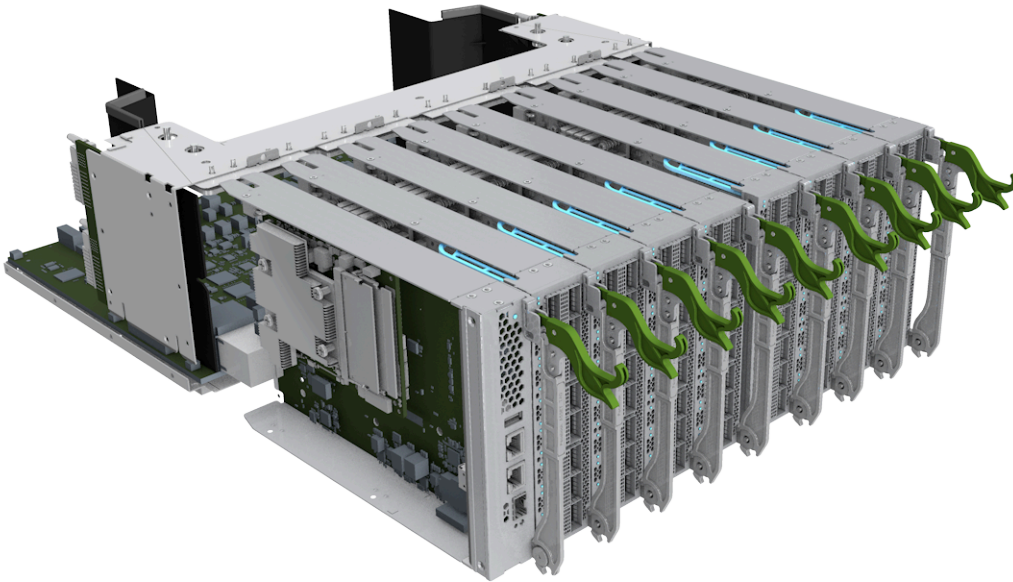


Figure 6-4: Front ISO View of Minipack Orthogonal-Direct Architecture

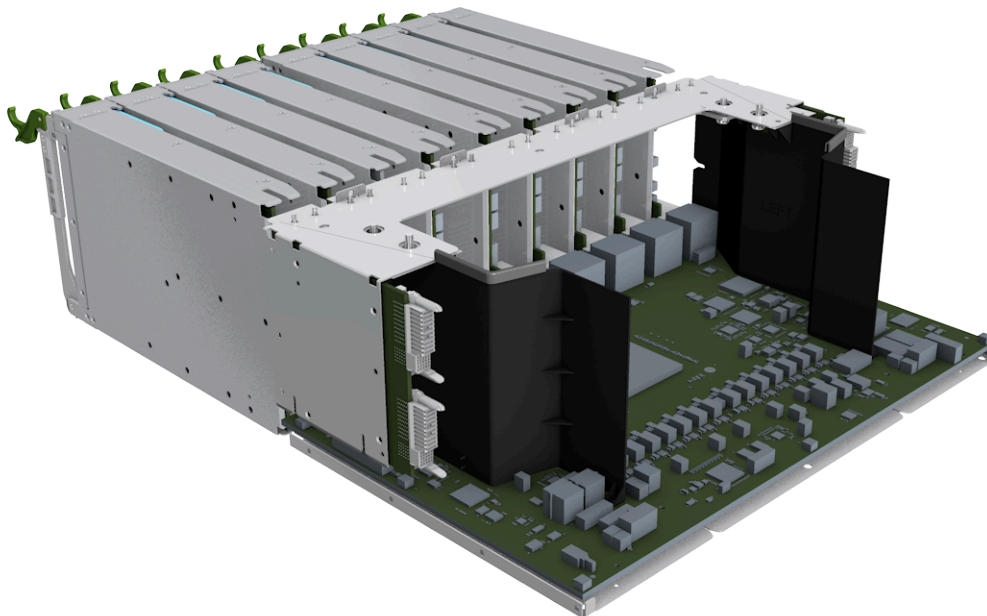


Figure 6-5: Rear ISO View of Minipack Orthogonal-Direct Architecture

6.3.1 Port Mapping between SMB and PIM

In a Minipack system, eight PIM and SMB are connected orthogonally. Each PIM connects to four Blackhawk SerDes macros of Tomahawk3. As Tomahawk3 divides its packet buffer into 2 banks shared by 8 packet processing pipelines, the port assignment between PIM and SMB should balance the usage of packet buffers as well as the load of packet processing pipelines of Tomahawk3.

7 Thermal Design Requirements

The thermal design of Minipack is optimized to support 100G-CWDM4 Lite optics with 55°C case temperature limit and future 200G and 400G optics. The air flow is from front to rear, and the worst case ambient temperature is 35°C when the 100G-CWDM4 Lite QSFP28 optics are installed on PIM-16Q.

The BMC monitors the thermal condition of the system based on readings from key temperature sensors, and controls the fan speed accordingly. The goal is to consume only the airflow necessary to keep the components at proper temperatures and reduce fan power consumption.

8 System I/O

8.1 Optics Transceivers Supported by PIM-16Q QSFP Ports

8.1.1 100G optics

- QSFP28 CWDM4-OCF 100G transceiver
- QSFP28 CWDM4 100G transceiver (MSA)
- QSFP28 LR4/LR4-lite 100G transceiver (IEEE)
- QSFP28 SR4 100G transceiver (IEEE)

8.1.2 200G optics

- QSFP56 FR4 200G transceiver
- QSFP56 DR4 200G transceiver

8.1.3 400G optics

- QSFP56-DD FR4 400G transceiver
- QSFP56-DD DR4 400G transceiver

8.1.4 40G optics

- QSFP+ LR4 40G transceiver
- QSFP+ SR4 40G transceiver

8.2 Management interfaces

There are 3 management interfaces on the SCM front panel:

- One console RJ-45 port, 9600Baud RS232
- One 1000BASE-T Ethernet RJ-45 port
- One device USB 2.0 port to the micro-server

9 Host CPU and BMC Functional Features

9.1 Micro-server CPU BIOS Feature List

The BIOS requirements are outlined below. However, new requirements may arise in the full product life cycle.

- **Intel TXT support, and supporting Intel Dynamic Boot (DRTM – Dynamic Root of Trust for Measurements)**
- UEFI compatible
- Configuration and features
 - Disable unused devices including video interfaces and GPU if supported by hardware
 - BIOS setup menu
 - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- Linux-based BIOS settings tool
- Default boot device priority
 - Network / PXE -> 1st SATA
- PXE boot
 - Supports IPv4 and IPv6 UEFI PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (eth0).
 - PXE timeout timer set to 10 seconds
 - Supports UEFI mode
 - Supports both PXE boot over IPv4 and IPv6, and be able to boot from a PXE server on a different IPv4 or IPv6 subnet
- Other boot options
 - Also supports booting from SATA interfaces
 - Provides the capability to select boot options
- Remote BIOS update
 - Scenario 1: Sample / audit BIOS settings
 - Scenario 2: Update BIOS with pre-configured set of BIOS settings
 - Scenario 3: BIOS / firmware update with a new revision
 - Update from the CentOS operating system over the LAN
 - Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)

- No user interaction (e.g., prompts)
 - BIOS updates and option changes do not take longer than five minutes to complete.
 - Can be scripted and propagated to multiple machines
- Event log
 - Implement SMBIOS Type 15 System Event Log per SMBIOS specification Rev 2.6
 - Hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB)
 - Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID.
 - A system access interface and application software to retrieve and clear the event log from the BIOS
- Logged errors
 - Single-bit ECC error
 - Multi-bit ECC error
 - PCIe error
 - SATA error
 - POST error
 - NMI error
 - System reboot events
 - Sensor values exceeding warning or critical thresholds
- Error thresholds
 - Setting must be enabled for both correctable and uncorrectable errors.
 - Threshold for Memory Correctable ECC is 1.
 - PCIe error threshold is 1.
- Console redirection to the serial ports
 - Console redirection shall be enabled whenever the CPU starts booting and kept enabled after the OS starts running.
- POST codes
 - To be provided on the serial console
 - To be provided on the LPC bus
- DMI
 - Model
 - Serial Number
 - Additional information if requested by Facebook
- ATA Security State 2

- The BIOS shall not send out ATA FREEZE command to the SSDs attached to the SATA ports.
- Support AMI RuntimeMemoryHole eModule, so that we can avoid using the kernel module of SCELNx and AFULNx.
- **ONIE support is required.**

9.2 BMC Feature Support

The BMC needs to support the following features:

- All SEL commands
- All sensor commands
- All SDR commands
- TPM 2.0 support
- Power on/off/cycle / hardware reset / soft reset commands
- I2C access to power sequencers, hot swap controllers, and DC-DC convertors
- Inventory EEPROM access
- Fan-tray present status check, fan PWM control and speed tachometer read
- Dual SPI boot
- On-board PHY MDIO interface access
- CPLD and FPGA online upgrade

10 Regulatory Compliance, Environmental, and Reliability Requirements

10.1 Regulatory Compliance Requirements

Compliance reports must be from labs accredited to a current version of IEC 17025. The reports and certificates must name the ODM as the applicant.

- **CE Declaration to the following Regulatory Directives by ODM / OEM:**
 - EMC Directive 2014/30/EU
 - Low Voltage (LVD) Directive 2014/35/EU
- **Safety certification**
 - CB certificate/report to IEC 62368-1 including all national deviations
 - CB certificate/report to IEC/EN 60950-1 including all national deviations
 - UL/CSA/IEC/EN 60950-1 with all latest amendments
 - UL/IEC 62368-1 with all latest amendments
 - CNS14336 Taiwan BSMI safety regulation
 - EN 60825-1 Safety of Laser products – part 1
 - UL 94-Vo Flammability rating
- **EMC certification**
 - FCC Part 15 (Class A)
 - ICES-003 (Canada) Class A
 - EN55032 (Europe) Class A
 - CISPR32 (International) Class A
 - AS/NZS CISPR32 (Australia and New Zealand) Class A
 - VCCI CISPR 32 (Japan) Class A
 - CNS 13438 (Taiwan) Class A
 - EN61000-3-2
 - EN61000-3-3
 - EN55024
 - EN 61000-4-2 ESD
 - EN 61000-4-3 Radiated Immunity
 - EN 61000-4-4 EFT
 - EN 61000-4-5 Surge
 - EN 61000-4-6 Low Frequency Conducted Immunity
 - EN 61000-4-11 Voltage Variations and Dips

▪ Immunity levels

Network Equipment						
Immunity Standard	Description	Standard Criteria (Required)	FB Criteria (Goal)	Standard Level (Required)	FB Level (Goal)	Remarks
IEC 61000-4-2	Electrostatic Discharge (ESD)	B	A	4 kV Cont. / 8 kV Air	8 kV Cont. / 15 kV Air	Criteria A (FB Goal) is highly desirable for any level
IEC 61000-4-3	Radiated Immunity	A	A	3 V/m	10 V/m	For communication cables >3 meters
IEC 61000-4-4	EFT	B	B	0.5 kV		Ports: Signal & Telecom (>3 meters), DC power input
		B	B	1 kV		Ports: AC power input & AC/DC Converter
IEC 61000-4-5	Surges	C	A	1 kV		Ports: Signal and Telecom connected to outdoor cables
		B	A	0.5 kV		Ports: DC power input
				1 kV L-L / 2 kV L-GND		Ports: AC power input & AC/DC Converter
IEC 61000-4-6	Conducted Immunity	A	A	3 V	10 V	Ports: Signal & Telecom (>3 meters), AC and DC power input
IEC 61000-4-8	Magnetic Field	A	A	1 A/m		Only EUT containing devices susceptible to magnetic fields
	Voltage Dips	B	B	>95% Reduction		Ports: AC power input & AC/DC

IEC 61000-4-11						Converter (0.5 Period)
		C	C	30% Reduction		Ports: AC power input & AC/DC Converter (25 Periods)
	Voltage Interruptions	C	C	>95% Reduction		Ports: AC power input & AC/DC Converter (250 Periods)

The ODM must strive to design to the FB Goal at the start and during the project. Facebook will decide if levels below the goal are acceptable. Off the shelf power supplies must meet the required level at a minimum.

- **Sound levels**

Network Equipment				
	OHSA (Required)	Directive 2003/10/EC (Goal)	FB Design Goal	Remarks
Sound Limit (dBA)	85	80	78	Under normal operation at 25 °C, the system must not produce a A-weighted sound power level above the required limit. The FB design goal should be targeted during development of the product. The Directive goal represents the limit that requires hearing protection to be provided to our Data Center Staff in Europe. The ODM must provide the result of the formal testing.

The ODM must strive to design to the FB Goal at the start and during the project. Facebook will decide if levels above the goal are acceptable. The sound power level limits apply to the normal operating conditions where the system is configured and equipped in its deployed state with the worst case configuration to produce the loudest noise. Maintenance conditions, open covers, are not considered normal conditions and do not need to be measured. Sound from

alarms does not need to be measured. Maximum fan speed expected under normal operation should be measured.

10.2 Materials of Concern Requirements

Regulatory

- RoHS Directive (2011/65/EU), including provisions of RoHS 3 Directive (2015/863) upon coming into effect.
- REACH Regulation (EC) No 1907/2006
- Waste Electrical and Electronic Equipment (“WEEE”) Directive (2012/19/EU)
- The Persistent Organic Pollutants Regulation (EC) No. 850/2004
- The California Safe Drinking Water and Toxic Enforcement Act of 1986 (“Prop 65”)
- The Packaging and Packaging Waste Directive 94/62/EC
- Batteries Directive 2006/66/EC

Corporate Sustainability Requirements

- **RoHS Exemptions position:** Compliance to the latest version of RoHS Directive is mandatory, and FB requires the use of no exemption where practical. If not practically possible, using the following exemption is allowed based on EU directive (2011/65/EU, 2015/863/EU) or future decision by European commission. As of the last revision date of this standard, relevant exemptions include 5a, 5b, 6a, 6b, 6c, 7a, 7c-I, 7c-II, 7c-IV, 8b, 9, 9b, 13(a), 13(b), 15, 21
- **Halogens (Bromine & Chlorine and their compounds)***
- **Phthalates (DEHP, DBP, DiBP, BBP)***
- **Arsenic and its compounds***
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act;** requires companies using tin, tantalum, tungsten, and gold (“3TG”) in in-scope products to verify and disclose the mineral source.

See the table (below) for scope, concentration limits, exemptions, and compliance deadlines for requirements marked with an asterisk (*).

HAZARDOUS SUBSTANCE	CAS NUMBER	SCOPE	CONCENTRATION LIMIT OF INTEREST (FOR ALL HOMOGENOUS MATERIALS)	EXEMPTIONS	COMPLIANCE DEADLINE
Halogens (incl. PVC, BFRs/CFRs)	Br: 7726-95-6 Cl: 7782-50-5	All Parts	900 ppm for Br or Cl, or 1500 ppm combined	N/A	Dec 31, 2019
Phthalates (DEHP, DBP, DiBP, BBP)	DEHP: 117-81-7 DBP: 84-74-2 DiBP: 84-69-5 BBP: 85-68-7	All Parts	1000 ppm (or 0.1% by weight)	N/A	Jul 22, 2019 (RoHS 3.0)
Arsenic	Includes but is not limited to: 7440-38-2	Glass and non-metals	50 ppm (or 0.005% by weight)	Semiconductors, optical elements	Dec 31, 2020
		Metals and alloys	1000 ppm (or 0.1% by weight)	Copper foil for printed circuit boards	

Table 3: Corporate sustainability scope, concentration limits, exemptions, and compliance deadlines

10.3 Environmental Requirements

The Minipack system should meet the following environmental requirements:

- Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Operating and storage relative humidity: 10% to 85% (non-condensing)
- Operating temperature range (with 100G CWDM4 MSA optics): 0°C to +45°C
- Operating temperature range (with 100G CWDM4-Lite optics): +15°C to +35°C
- Storage temperature range: -40°C to +70°C (long-term storage)
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-rating: up to 6,000 feet
- Shock and Vibration: IEC 68-2-36, IEC 68-2-6

10.4 Mean Time Between Failures (MTBF) Requirements

The MTBF of Minipack is required to be at least 5 years or 43,800 hours.

11 Labels and Markings

11.1 PCBA Labels and Markings

Minipack PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

Table 4: PCBA Label Requirements

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Facebook P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

11.2 Chassis Labels and Markings

The pull-out tag at the front panel of the chassis includes system model number, serial number, and Facebook asset tag.

12 Appendix A - Requirements for IC Approval

List all the requirements in one summary table with links from the sections.

Requirements	Details	Link to which Section in Spec
Contribution License Agreement	Which one?	1 License
Tenets	Which ones? Openness Efficiency Impact Scale	2 OCP Tenets Compliance
Supplier available within 120 days	List Supplier Name(s)	Edgecore Networks (Accton Technology Corporation) Arista Networks Inc.
Will they apply for OCP product recognition?		Yes