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Compute Project

Project Olympus

Intel® Xeon® Scalable Processor

Motherboard Specification

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Open Compute Project • Project Olympus Intel® Scalable Processor Motherboard Specification

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1 Project Olympus Specifications List

Table 1 lists the Project Olympus system specifications.

Table 1. List of Specifications

Specification title	Description
Project Olympus Server Rack Specification	Describes the mechanical rack hardware used in the system.
Project Olympus Server Mechanical Specification	Describes the mechanical structure for the server used in the system.
Project Olympus Universal Motherboard Specification	Describes the server motherboard general requirements.
Project Olympus PSU Specification	Describes the Power Supply Unit (PSU) used in the server.
Project Olympus Power Management Distribution Unit Specification	Describes the Power Management Distribution Unit (PMDU).
Project Olympus Rack Manager Specification	Describes the Rack Manager PCBA used in the PMDU.

This document is intended for designers and engineers who will be building servers for Project Olympus systems.

2 Overview

This specification describes the Project Olympus Intel® Server Motherboard. This is an implementation specific specification under the Project Olympus Universal Motherboard Specification.

Refer to respective specifications for other elements of the Project Olympus system such as Power Supply Unit (PSU), Rack Manager (RM), Power and Management Distribution Unit (PMDU), and Server Rack.

This specification covers block diagram, management sub-system, power management, FPGA Card support, IO connectors, and physical specifications of the Server Motherboard.

3 Background

The server motherboard is the computational element of the server. The motherboard includes a full server management solution and supports interfaces to integrated or rear-access 12V Power Supply Units (PSUs).

The Server optionally interfaces to a rack-level Power and Management Distribution Unit (PMDU).

The PMDU provides power to the Server and interfaces to the Rack Manager (RM).

The motherboard design provides optimum front-cable access (cold aisle) for external IO such as networking and storage as well as standard PCIe cards. This enables flexibility to support many configurations.

4 Block Diagram

Figure 1 shows the baseline block diagram describing general requirements for the server motherboard.

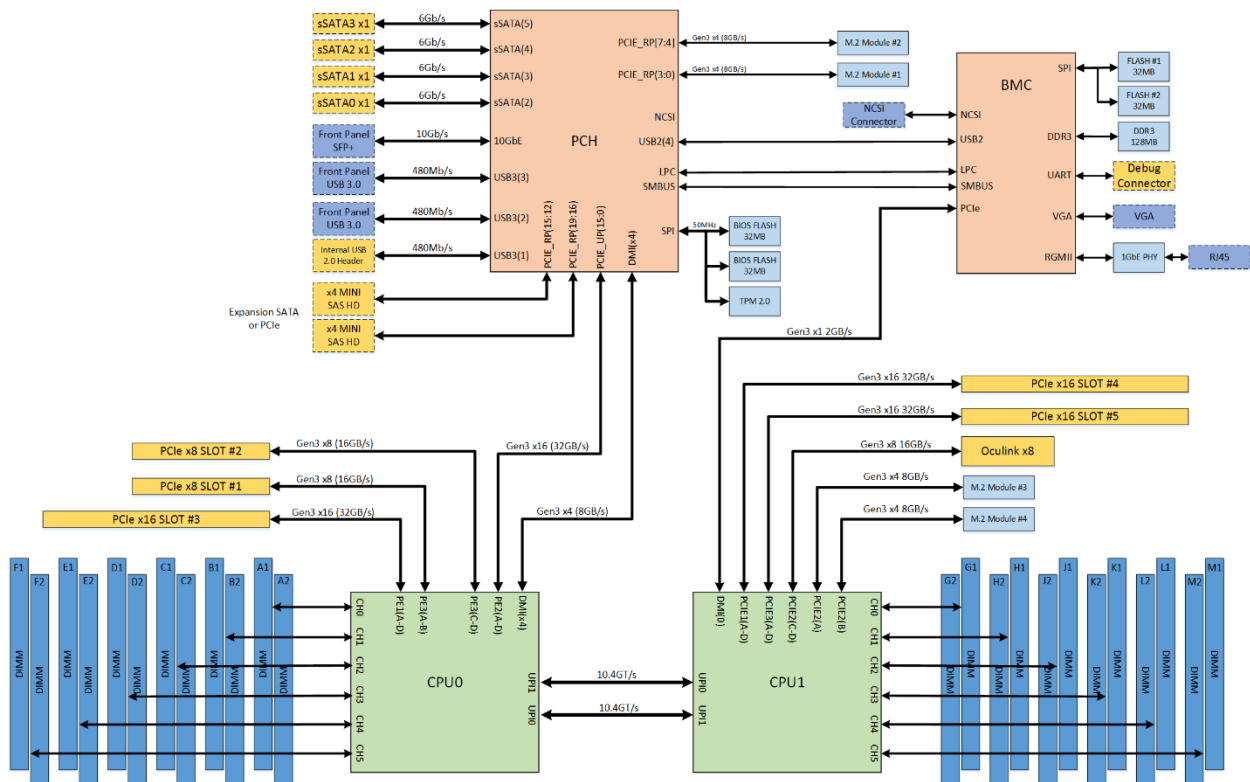


Figure 1. Top Level Block Diagram

5 Features

The motherboard includes support for the following features:

Processor	
Platform	Intel® Xeon® Scalable Platform
CPU	Intel® Xeon® Scalable processors
Sockets	Dual socket operation
TDP Wattage	Up to 205W (Support for all server class SKUs)
Memory	
DIMM Slots	24 DIMM slots 12 DIMMs per CPU 2 DIMMs per channel
DIMM Type	Double data rate fourth generation (DDR4) Registered DIMM (RDIMM) with Error-Correcting Code (ECC)
DIMM Speed	DDR4-2400 (2DPC), DDR4-2666 (2DPC)
DIMM Size	16GB, 32GB, 64GB
Capacities Supported	128GB, 192GB, 256GB, 512GB, 768GB, 1536GB
On-Board Devices	
Chipset	Intel® C620 series chipset (PCH)
SATA	4 local ports @ 6.0 Gb/s (SATA x1) 8 Flex I/O expansion ports @ 6.0Gb/s (MiniSAS HD)
Server Management	
Chipset	BMC Aspeed AST1250/AST2400
Interface	Representational State Transfer (REST) API Windows Management Instrumentation (WMI) Open Management Interface (OMI) Command-Line Interface (CLI)

System Firmware	
Version, Vendor	Unified Extensible Firmware Interface (UEFI) 2.3.1, AMI (TBD)
Security	Trusted Platform Module (TPM 2.0) Secure Boot
PCI-Express Expansion	
2 PCIe x8 Slots	Supports PCIe M.2 Riser Cards
3 PCIe x16 Slots	Supports standard PCIe x16 cards.
4 M.2 Slots	Supports 60mm, 80mm, and 110mm M.2 Cards
1 PCIe x8 Expansion	OCuLink PCIe x8
2 PCIe x4 Expansion	2 MiniSAS HD PCIe x4 connected to PCH Root Port
1 PCIe x16 Expansion	Support Intel® QuickAssist Technology (QAT)
1 PCIe x8 Expansion	2 MiniSAS HD PCIe x4 connected to PCH Flex I/O
Networking	
LOM	1x 10GbE from PCH on SFP+ Connector
MGMT	1x 1GbE from BMC to RJ45 Connector

5.1 CPUs

The motherboard supports two Intel® Xeon® Scalable processors for all server class SKUs. The maximum TDP supported is 205W.

5.2 PCH

The motherboard supports all SKUs of the Intel® C620 series chipset (PCH).

5.3 Flexible I/O Mapping

Table 2 describes the mapping of the PCH Flexible I/O to the motherboard interfaces.

Table 2. PCH Flex I/O Mapping

Flexible I/O Port	Motherboard Mapping	Description
1	USB3(1)	USB 2.0 port to internal header
2	USB3(2)	USB 3.0 port to front panel
3	USB3(3)	USB 3.0 port to front panel
4	Not Used	USB 3.0 (Not used)
5	Not Used	USB 3.0 (Not used)
6	Not Used	USB 3.0 (Not used)
7	PCIE_RP(0)	PCIe root port to M.2 #1
8	PCIE_RP(1)	PCIe root port to M.2 #1
9	PCIE_RP(2)	PCIe root port to M.2 #1
10	PCIE_RP(3)	PCIe root port to M.2 #1
11	PCIE_RP(4)	PCIe root port to M.2 #2
12	PCIE_RP(5)	PCIe root port to M.2 #2
13	PCIE_RP(6)	PCIe root port to M.2 #2
14	PCIE_RP(7)	PCIe root port to M.2 #2
15	sSATA(2)	sSATA to SATA connector SATA0
16	sSATA(3)	sSATA to SATA connector SATA1
17	sSATA(4)	sSATA to SATA connector SATA2
18	sSATA(5)	sSATA to SATA connector SATA3
19	PCIE_RP(12)	PCIe root port or SATA4
20	PCIE_RP(13)	PCIe root port or SATA5
21	PCIE_RP(14)	PCIe root port or SATA6
22	PCIE_RP(15)	PCIe root port or SATA7
23	PCIE_RP(16)	PCIe root port or SATA8
24	PCIE_RP(17)	PCIe root port or SATA9
25	PCIE_RP(18)	PCIe root port or SATA10
26	PCIE_RP(19)	PCIe root port or SATA11

5.4 DIMMs

The motherboard supports 24 DDR4 RDIMMs with 12 RDIMMS per CPU socket. It supports all available configurations for single, dual, and quad rank RDIMMs supported by the Intel® Xeon® Scalable Platform. The DIMM pitch is 370mils.

The motherboard is designed to support the following technologies but use of these technologies has not been validated.

- LRDIMM
- 3DS RDIMM
- DDR4 NVDIMM with 12V support through the DIMM connector

5.5 PCIe Support

5.5.1 CPU PCIe Mapping

Table 5 describes the PCIe port mapping between the CPUs and the PCIe endpoints.

Table 3. CPU PCIe Port Mapping

CPU	PCIe Bus	Destination
0	DMI	PCH
0	PE1(A-D)	PCIe Slot #3
0	PE2(A-D)	PCH PCIe Uplink (QAT)
0	PE3(A-B)	PCIe Slot #1
0	PE3(C-D)	PCIe Slot #2
1	DMI[0]	BMC
1	PE1(A-D)	PCIe Slot #4
1	PE2(A)	M.2 Module #3
1	PE2(B)	M.2 Module #4
1	PE2(C-D)	OCuLink x8
1	PE3(A-D)	PCIe Slot #5

5.5.2 PCIe x8 Slots

The motherboard supports PCIe x8 connections to slots 1 and 2 as shown in Figure 2. Each slot supports 1x8 and 2x4 bifurcation. 2x4 bifurcation is supported at the connector with the addition of a 2nd PCIe clock to the standard PCIe pinout. The primary purpose of the slots is to support M.2 Modules with each slot capable of supporting two modules. Use of the modules requires a PCIe riser edge card to connect the modules to the PCIe bus. The riser is capable of supporting 60mm, 80mm, and 110mm M.2 Modules.

5.5.3 PCIe x16 Slots

The motherboard supports PCIe x16 connections to slots 3, 4, and 5 as shown in Figure 2. Each slot supports a standard PCIe form factor card using a riser card to interface to the PCIe connector. The size of the card supported is dependent on the height of the tray assembly. 1U trays can support FHHL PCIe cards. 2U trays can support FHFL cards. Note that Slot #4 is targeted for use by FPGA cards requiring two PCIe x8 channels and this is the default configuration. In this case, additional PCIe can be cabled from the OcuLink x8 connector.

All slots support bifurcation below 1x16 but utilize the standard PCIe connector pinout and do not contain additional clocks. Additional clocks required for bifurcation below 1x16 must be handled with buffer circuitry on the PCIe card.

5.5.4 PCIe Cables

The motherboard supports a single OcuLink x8 connector for the primary purpose of expanding PCIe support to Slot 4 to 24 lanes. PCIe clock and control signals are not supported by the implementation. Physical cabling must avoid any FHHL PCIe card located in Slot 5.

5.5.5 M.2 Modules

The motherboard supports M.2 modules through any of the following methods:

- Standard M.2 connector mounted directly on the motherboard. The motherboard supports up to four on-board M.2 modules.
- M2 Riser Cards in Slots 1 and 2: PCIe Riser card supporting up to two M.2. modules in each slot. Two of the modules are connected to a PCIe endpoint on the PCH. The other two modules are connected to a PCIe endpoint on CPU1.
- Quad M.2 Carrier Card (OCP AVA): FHHL PCIe Card in standard PCIe format supporting up to four M.2 modules.

For both motherboard and PCIe Card applications, the supported M.2 modules are 60mm, 80mm, and 110mm dual sided form factors (Type 2260, 2280, and 22110).

5.5.6 Intel® QuickAssist Technology Support

The motherboard supports PCIe x16 support from CPU0 to the Intel® QuickAssist Technology (QAT) engines in the PCH.

5.6 PCIe/SATA Expansion

The motherboard supports two MiniSAS-HD x4 connectors for optional PCIe or SATA expansion from root ports on the PCH. The connectors are connected to Flex I/O PCIe_RP(19:16) and PCIe_RP(15:12) on the PCH. The functionality of the ports (PCIe vs SATA) are controlled by two GPIO outputs of the BMC enabling each nibble to be configured independently.

5.7 SATA Storage

The motherboard support cabling for up to 12 SATA storage drives. This is accomplished with four x1 SATA connectors connected to PCH sSATA ports and two MiniSAS-HD x4 connectors connected to PCH Flex I/O ports described in section 5.6.

5.8 TPM Module

The motherboard includes a connector to support a TPM 2.0 module connected to the PCH SPI bus.

5.9 Management Subsystem

The Baseboard Management Controller (BMC) circuitry for the motherboard uses an ASPEED AST2400 family processor. This section describes the requirements for management of the motherboard. Primary features include.

- BMC - ASPEED AST1250/AST2400
- BMC dedicated 1GbE LAN for server management

- Low pin count (LPC) connection to the chipset to support in-band management
- Out of band environmental controls for power and thermal management
- FRUID EEPROM for storage of manufacturing data and events (I²C)
- Thermal sensors for inlet and exhaust temperature monitoring (I²C)
- Power monitoring through the 12V Hot Swap Controller circuitry (I²C)
- Service LEDs

Figure 2 shows the management block diagram.

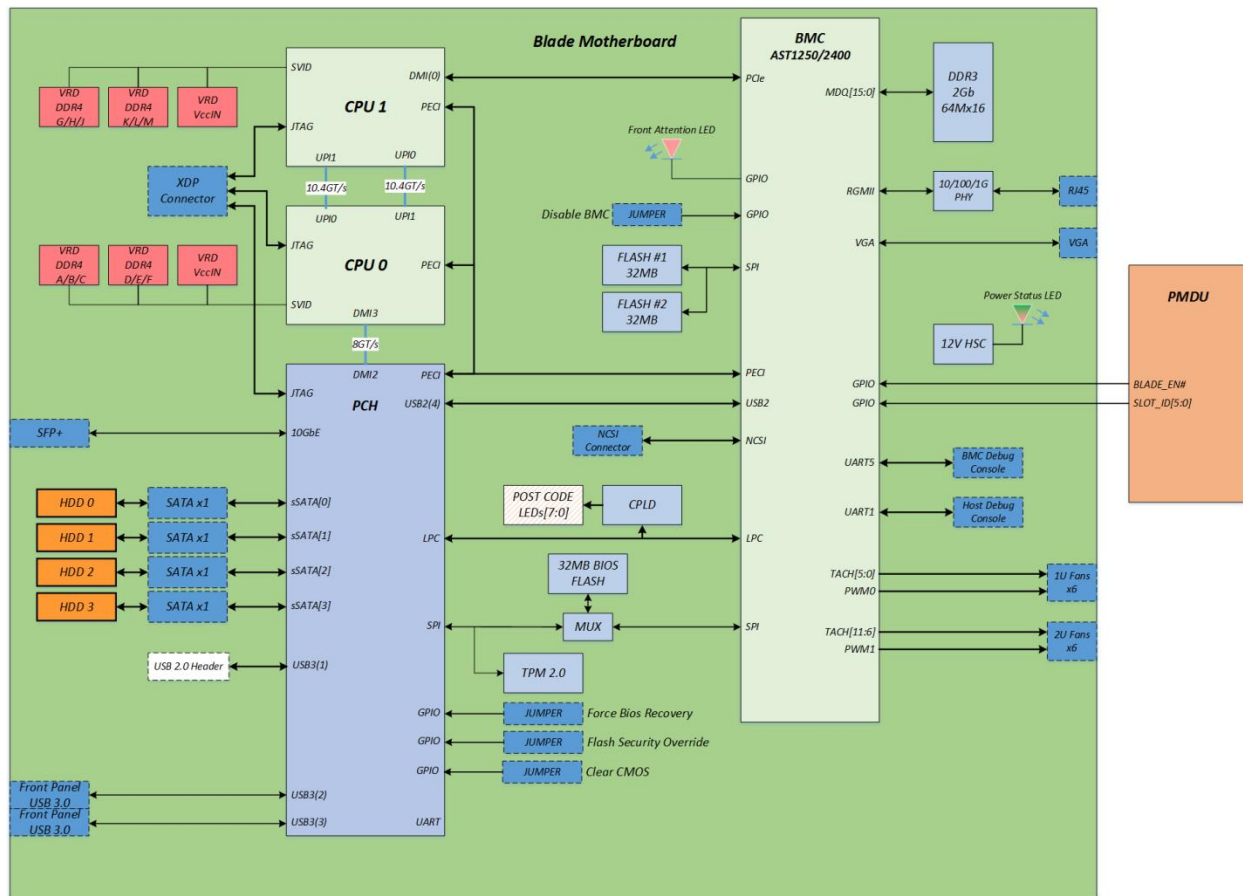


Figure 2. Management Block Diagram

5.9.1 BMC

The design for the BMC is based on the Aspeed 2400 family and supports either the AST1250 or the AST2400 processor. Primary features include:

- Embedded ARM Processor

- Minimum 256MiB of DDR3 memory
- Redundant NOR/NAND/SPI flash memory
- I²C /SMBus
- UART
- LPC Bus Interface
- Over 200 GPIO pins
- VGA (AST2400 only)

5.9.2 DRAM

The BMC supports a minimum of 256MB of DDR3 memory.

5.9.3 BMC Boot Flash

The BMC boots from a flash memory device located on the SPI bus. The device size is 256Mb (32MB) minimum and can be used to store FPGA and CPLD recovery images. The device is Winbond W25Q256 or equivalent. A secondary device is supported to provide BMC recovery.

5.9.4 BIOS Flash

The BIOS utilizes one 256Mb (32MB) Flash BIOS device located on the chipset SPI bus. The device is Winbond MPN W25Q256 or equivalent. The BIOS is recoverable from the BMC in the event the chipset is inaccessible.

5.9.5 1GbE PHY

The server is managed through a 1GbE PHY connected to the BMC. An RJ45 connector located at the front of the server provides 1GbE connectivity to an external management switch. The device is Broadcom BCM54612E.

5.9.6 UARTS

The motherboard supports 2 debug UARTS connected to the BMC as follows:

- UART5 BMC Debug Console
- UART1 Host Debug Console

Figure 3 shows a block diagram of the UART support.

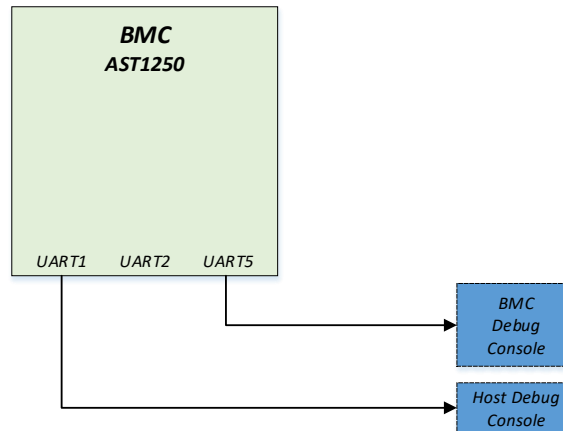


Figure 3. UART Block Diagram

5.9.7 PECI

The motherboard uses the PECI Host Controller inside the PCH to support integrated thermal monitoring of the two CPU sockets. PECI is connected from the CPU to the BMC by default. The motherboard contains BOM load options to connect PECI to the PCH.

5.9.8 VGA

The motherboard includes optional support for VGA assuming the AST2400 processor. To support VGA, PCIe is provided from the DMI[0] PCIe port of CPU1.

5.9.9 I2C

The motherboard supports I2C devices available to the BMC and PCH. A block diagram of the I2C tree is shown in Figure 4. A brief description of the entities is included below. Note that addresses shown are 8-bit address with the R/W bit as the LSB set to 0 (0xA8=1010100x).

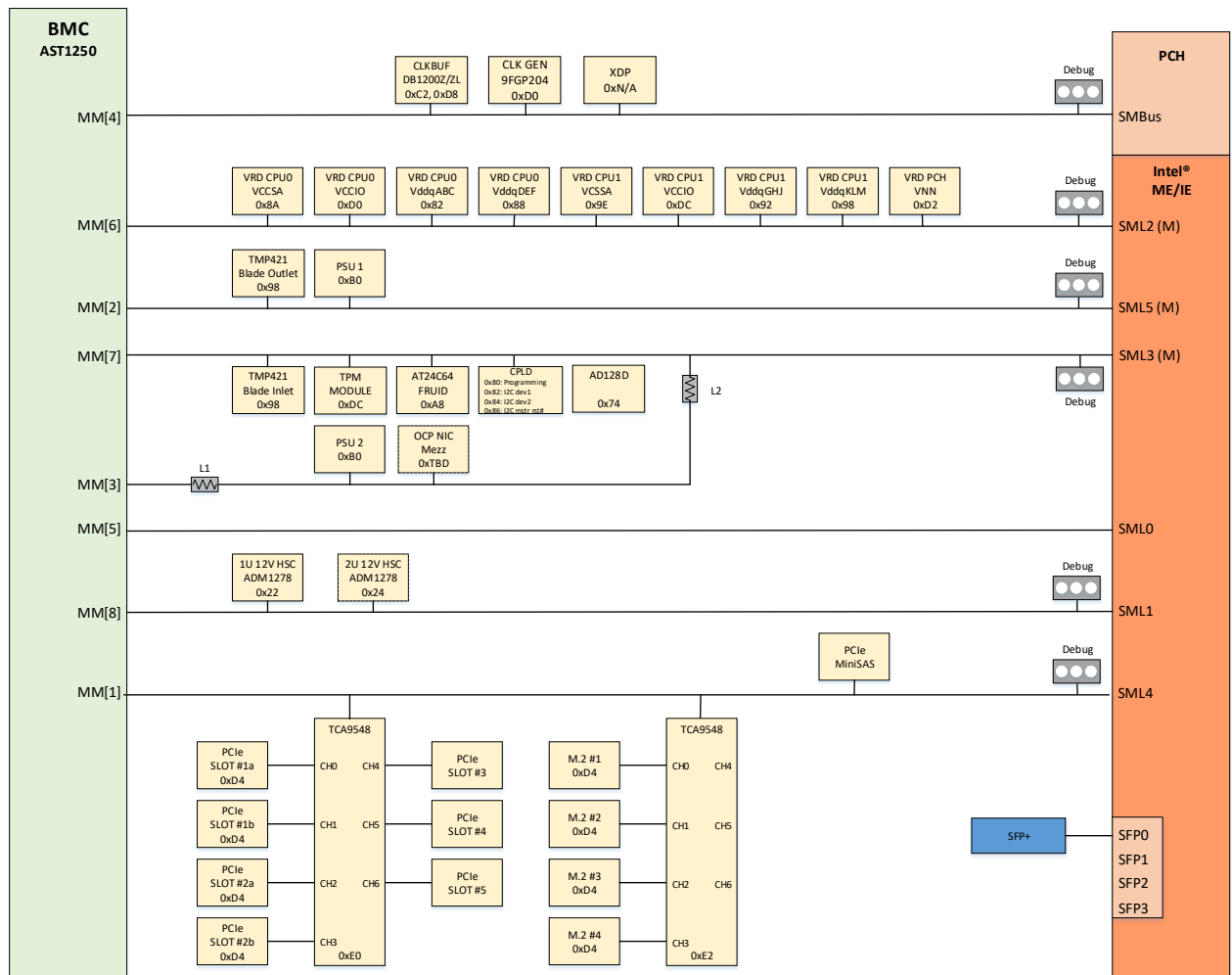


Figure 4. I2C Block Diagram

5.9.9.1 FRUID PROM

The motherboard includes I2C support for a 64Kb FRUID EEROM, MPN AT24C64 or equivalent, for storing manufacturing data.

5.9.9.2 Temperature Sensors

The Motherboard includes I2C support for two temperature sensors, MPN TMP411 or equivalent, for monitoring the inlet and outlet air temperatures of the motherboard. The motherboard includes provisions to support temperature monitoring of all DIMMs (SPD) and all PCIe slots including M.2 modules.

5.9.9.3 PCIe Devices

The motherboard includes I2C support for all PCIe devices including PCIe Slots and M.2 Modules. Communication is managed through TCA9548 (or equivalent) I2C switches to ensure that devices with the same I2C address are supported from a single I2C port on the BMC.

5.9.9.4 Voltage Regulators

The motherboard includes I2C support for all the CPU and Memory Subsystem voltage regulators enabling the BMC to monitor health of the individual power rails.

5.9.9.5 Hot Swap Controllers

The motherboard includes I2C support for up to two ADM1278-2A hot swap controllers for power monitoring and power-capping. Power is monitored by the PCH as part of the power capping function. Accuracy of the ADM1278-2A is +/-0.7%.

5.9.10 JTAG

The motherboard supports muxing of the JTAG master on the BMC to support multiple uses as follows.

- Programming of the primary CPLD
- Programming of PCIe Cards (FPGA) located in Slot #4

A block diagram is shown in Figure 5.

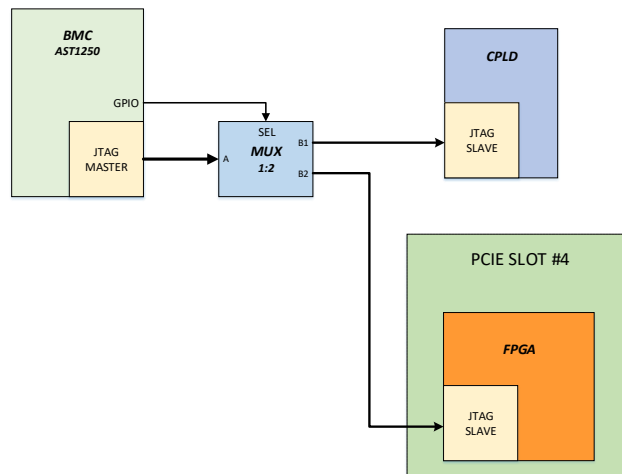


Figure 5. JTAG Block Diagram

5.9.11 Jumpers

The motherboard supports the jumpers listed in Table 4.

Table 4. Jumpers

Jumper Name	REF Des	Status	Function
BMC Disable (default)	JP21	1-2 Normal (default) 2-3 Hold BMC in Reset	Disables BMC (sets all pins to High impedance)
BMC Disable (backup)	TBD	High (not installed)	Disables BMC (holds BMC in reset. Disconnected by 0ohm resistor)
ME Recovery Mode	JP2	1-2 Normal (default) 2-3 Force ME Update	Force Intel® Manageability Engine (ME) update

BIOS USB Recovery	JP12	1-2 BIOS USB flash recovery mode 2-3 Normal (default)	Enables BIOS recovery via USB image update
BIOS A18 Top Swap	JP9	1-2 Normal (default) 2-3 Recovery BIOS	Swaps BIOS image by booting from other half of BIOS Flash
Clear CMOS	J13	1-2 Normal (default) 2-3 Clear RTC registers	Clears CMOS
Password Clear	JP11	1-2 Normal (default) 2-3 Password clear	Clears the password

5.10 LEDs

The following sections describe the light-emitting diodes (LEDs) used as indicators on the motherboard. Table 5 lists the minimum LEDs required and provides a brief description. Greater detail for some LEDs is included in subsequent sections below. The visible diameter, color (λ) and brightness requirements of the LEDs are TBD. All LEDs are visible at the front of the motherboard (cold aisle).

Table 5. LEDs

LED Name	Color	Description
UID LED	Blue	Unit Identification LED
Attention LED	Red	Indicates that Server requires servicing
Power Status LED	Amber/Green	Indicates Power Status of the Server
SATA HDD Activity	Green	Indicates R/W activity to HDDs
Post Code	Green	Indicates the Boot status of the Server (Port 80)
Catastrophic Error	Red	Indicates that a CPU catastrophic error has occurred
BMC Heartbeat	Green	Blinks to indicate BMC is alive
GbE Port 0 Activity	Green	Indicates activity on 10GbE Port 0 (not supported for production)
GbE Port 0 Speed	Green/Orange	Green=high speed, Orange=Low speed (not supported for production)
PSU1 Status LED1 (P2010)	Green	Status LED for PSU1 - Solid Green = AC and DC Power Good - Blinking Green = Battery Power Good
PSU1 Status LED2 (P2010)	Amber	Status LED for PSU1 - Solid Amber = Failure of PSU Phase - Blinking Amber = Failure of 2 PSU Phases
PSU2 Status LED1 (P2010)	Green	Status LED for PSU2 (optional) - Solid Green = AC and DC Power Good - Blinking Green = Battery Power Good
PSU2 Status LED2 (P2010)		Status LED for PSU2 (optional) - Solid Amber = Failure of PSU Phase - Blinking Amber = Failure of 2 PSU Phases

5.10.1 UID LED

The motherboard supports a blue UID (unit ID) LED used to help visually locate a specific server within a datacenter.

5.10.2 Power Status LED

When a server is initially inserted, the Power Status LED shall turn amber if 12V is present at the output of the hot swap controller. This assures that the 12V power is connected and present at the motherboard and that the hot swap controller is enabled.

When the server management software turns on the system power (CPU/Memory/PCIe), the Power Status LED turns green. Note that the power status LED may be driven by an analog resistor network tied directly to a power rail and is not an indication of the health of the server. Table 6 describes the operation of the Power Status LED.

Table 6. Power Status LED Description

LED status	Condition
Off	12V power is absent or PWR_EN# is de-asserted
Solid Amber ON	PWR_EN# is asserted and 12V power output of the hot swap controller is present.
Solid Green ON	Indicates that the management (BMC) is booted and system power is enabled (CPU/Memory/PCIe).

5.10.3 Attention LED

The Attention LED directs the service technicians to the server that requires service. When possible, server diagnostics are used to direct repairs. The LED is driven by a single BMC GPIO. Table 7 describes the operation of the Attention LED.

Table 7. Attention LED Description

LED status	Condition
Off	No attention indicated
Solid RED	System needs attention

5.10.4 PSU Status LEDs

The motherboard support four PSU status LEDs (2 per PSU). Each PSU is comprised of 2 individual status LEDs indicating the PSU status as shown in Table 5. These LEDs support the WCS P2010 PSU. Standard PSUs may not support external LEDs.

5.11 Fan Control

The motherboard supports control of twelve 40mm fans located at the rear of the server assembly. Fan control is divided between two connectors enabling two separate fan zones. Each connector supports 12V power, a single PWM, and six TACH signals for controlling up to 6 fans in a single zone.

6 Power Management

The motherboard provides a rear connector for interfacing the motherboard to a 12V PSU. The motherboard also provides a separate rear management connector for enabling external control of server power. A block diagram of the interface is shown Figure 6.

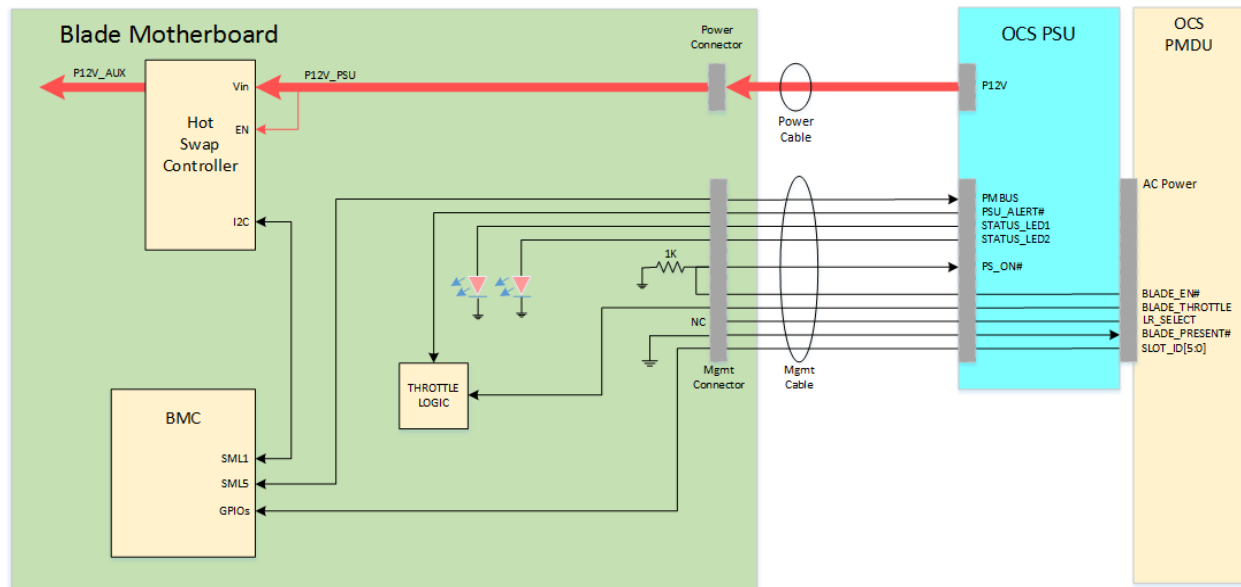


Figure 6. Power Management Block Diagram

6.1 Rack Management

The motherboard supports server control through the PMDU. The following describes the management interfaces.

- **PWR_EN#** - Active low signal used to enable/disable power to the P2010 PSU. A 1K ohm pulldown resistor is used on the motherboard to ensure a default low state (active) if the Rack Manager is not present. This signal connects to the PS_ON# signal of the PSU. When in high state (inactive), this signal disables output power from the P2010 PSU.
- **SERVER_PRESENT#** - Active low signal used to communicate physical presence of the server to the Rack Manager. This signal should be tied to GND on the motherboard.
- **SERVER_THROTTLE** - Active high signal used to put the motherboard into a low power (power cap) state. This signal should default low (inactive) if the Rack Manager is not present. This signal is fanned out from the Rack Manager to multiple servers and therefore the circuit design must support electrical isolation of this signal from the motherboard power planes.
- **SLOT_ID[5:0]** – Identifies the physical rack slot in which the server is installed. ID is hard set by the PMDU. The ID decoding is shown below in Table 8.

- **LR_SELECT** – Spare signal. Used to differentiate between left and right slots for a dual-node implementation.

Table 8. Slot ID Decode

Slot	SLOT_ID[5:0]	Slot	SLOT_ID[5:0]
Slot 1	000000	Slot 25	100000
Slot 2	000001	Slot 26	100001
Slot 3	000010	Slot 27	100010
Slot 4	000011	Slot 28	100011
Slot 5	000100	Slot 29	100100
Slot 6	000101	Slot 30	100101
Slot 7	001000	Slot 31	101000
Slot 8	001001	Slot 32	101001
Slot 9	001010	Slot 33	101010
Slot 10	001011	Slot 34	101011
Slot 11	001100	Slot 35	101100
Slot 12	001101	Slot 36	101101
Slot 13	010000	Slot 37	110000
Slot 14	010001	Slot 38	110001
Slot 15	010010	Slot 39	110010
Slot 16	010011	Slot 40	110011
Slot 17	010100	Slot 41	110100
Slot 18	010101	Slot 42	110101
Slot 19	011000	Slot 43	111000
Slot 20	011001	Slot 44	111001
Slot 21	011010	Slot 45	111010
Slot 22	011011	Slot 46	111011
Slot 23	011100	Slot 47	111100
Slot 24	011101	Slot 48	111101

6.2 PSU Management

The motherboard supports management of the P2010 PSU. Below is a description of the signals supported by the PMDU.

- **PS_ON#** - Active low signal used to enable/disable power to the PSU. This signal is driven by the **PWR_EN#** signal from the Rack Manager. A 1K ohm pulldown resistor is used on the motherboard to ensure a default low state if the RM is not present.
- **PSU_ALERT#** - Active low signal used to alert the motherboard that a fault has occurred in the PSU. Assertion of this signal by the PSU shall put the motherboard into a low power (PROCHOT) state. This signal is also connected to the BMC for monitoring of PSU status.

- PMBUS – I²C interface to the PSU. The BMC uses this signal is used by the BMC to read the status of the PSU.
- STATUS_LED – Controls LED to provide visual indication of a PSU fault.

6.3 Hot Swap Controller

The motherboard supports a hot swap controller (HSC), MPN ADM1278, for in-rush current protection and power monitoring. The HSC includes support for the PMBUS interface.

6.4 Power Capping

The motherboard supports throttling of the processors using the Fast PROCHOT mechanism based on monitoring of the motherboards input voltage and power. A block diagram detailing these triggers is shown in Figure 7.

The following triggers are monitored by the BMC and PCH and can directly generate PROCHOT# events. Each trigger is filtered by the CPLD and the CPLD ensure that any trigger event generates a minimum 100mS PROCHOT# pulse.

- Undervoltage – A comparator monitors the 12V output of the HSC and asserts if this voltage falls below 11.5V.
- Overcurrent Alert – The HSC monitors the input current and asserts the trigger if the input current exceeds 93A.
- Overcurrent Protect – The HSC monitors the input current and disables power to the motherboard if the current exceeds 95A.
- HSC ALERT #1 and #2 – The HSC provides two programmable alerts. These alerts are spare inputs and are disabled by default.

Note that the CPU voltage regulators also can generate PROCHOT triggers to the CPUs.

The motherboard enables power capping of the server from different trigger sources. Assertion of either of the following causes the motherboard to assert PROCHOT and the PCH to initiate power capping of the server.

- RM THROTTLE# - Throttle signal driven by the Rack Manager indicating that the rack has exceeded its power limit.
- PSU ALERT# - Alert signal driven by the PSU. Assertion indicates an over-current event or that the Olympus PSU has transitioned its power source from AC to battery backup.
- FM_THROTTLE# - Test signal that allows BMC to assert power cap

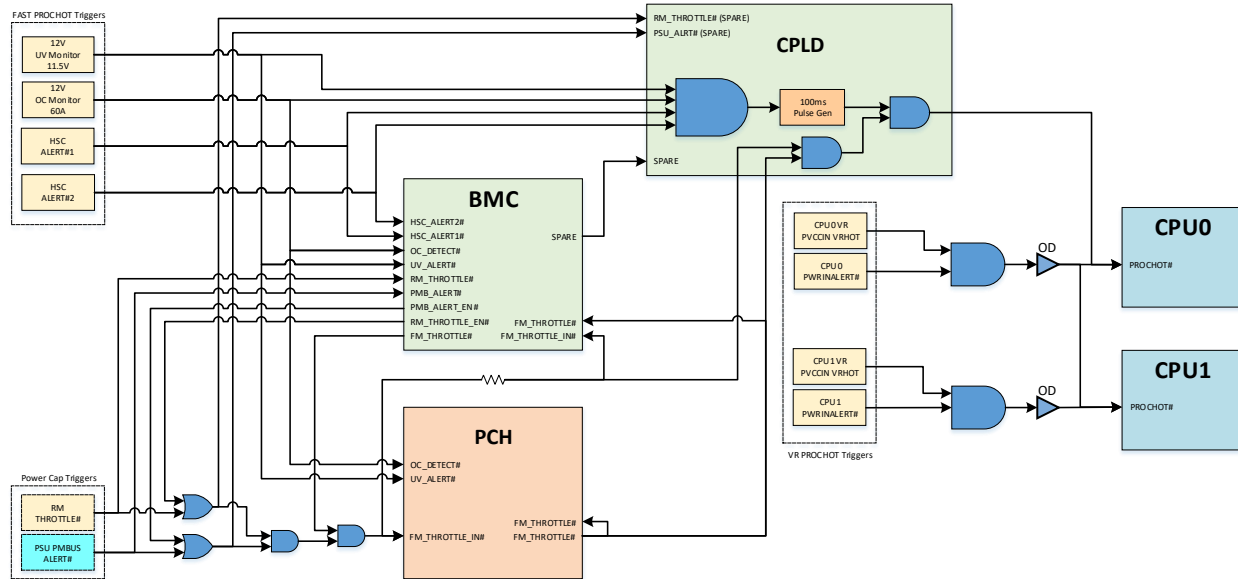


Figure 7. PROCHOT Block Diagram

6.5 PWRBRK#

The motherboard supports Emergency Power Reduction mechanism (PWRBRK#) for the x16 PCIe slots. The primary purpose is to provide a power reduction mechanism for GPGPU cards as part of the throttle and power capping strategy. Figure 8 shows the block diagram for PWRBRK#. PWRBRK# can be triggered by either the RM_THROTTLE# or PSU2_ALERT#. Logic for PWRBRK# is contained in the CPLD. The BMC controls enable/disable monitoring of the two triggers and can also force an event.

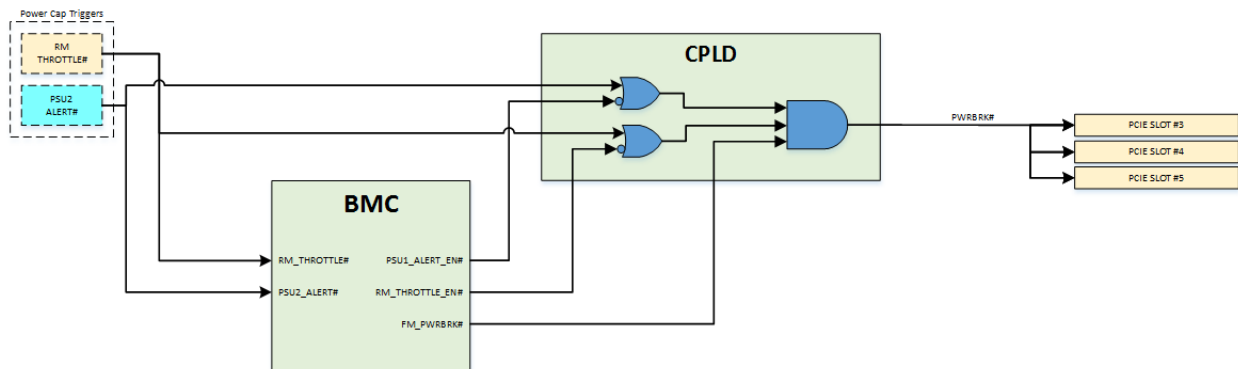


Figure 8. PWRBRK# Block Diagram

7 Motherboard Layout

Figure 9 shows a representative layout of the motherboard with the approximate location of critical components and connectors.

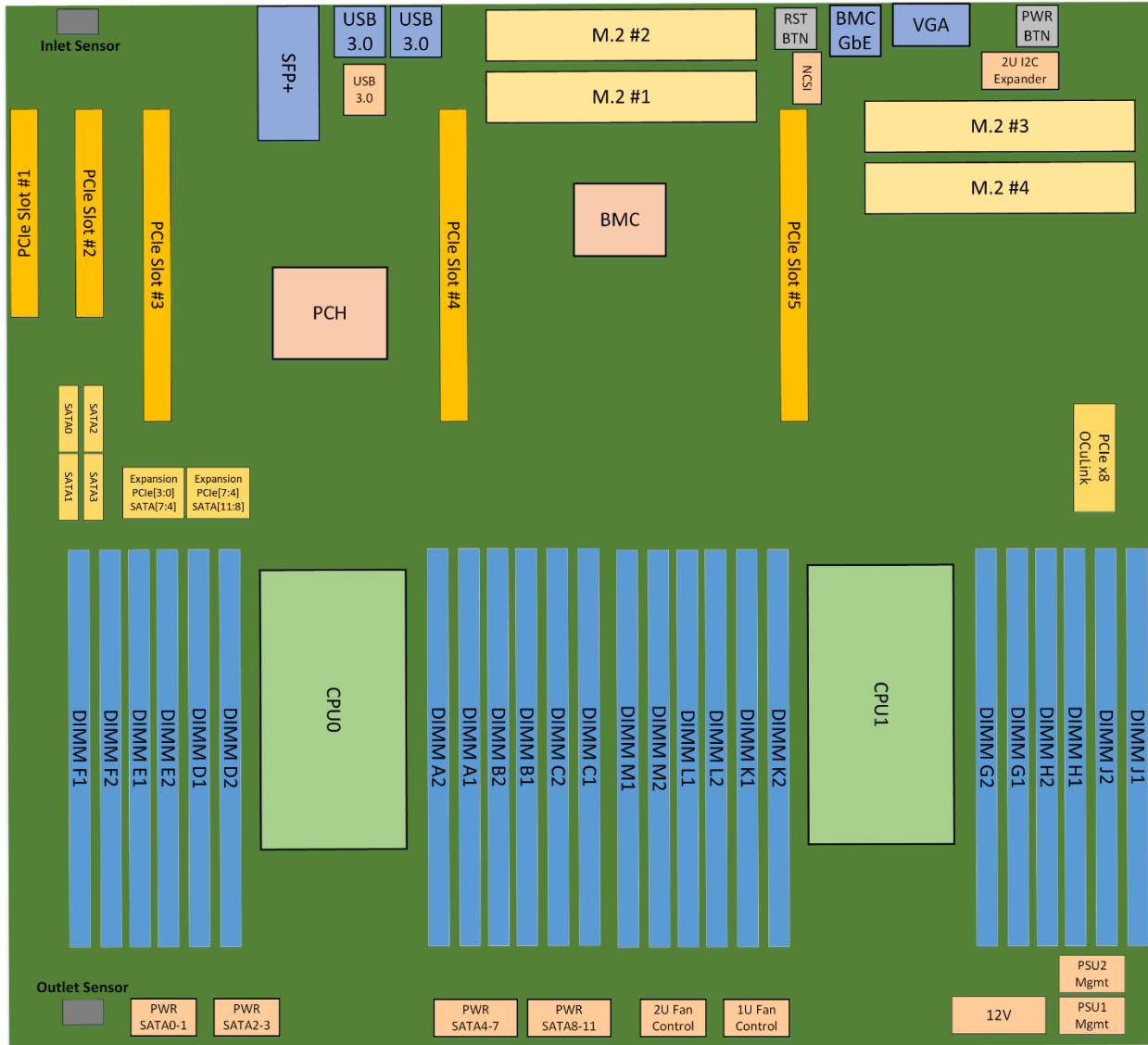


Figure 9. Motherboard Layout

8 Serviceability

8.1 Debug features

The motherboard supports the following debug features:

- I2C Debug headers on all I2C ports. Headers are compatible with standard I2C Protocol Analyzers such as Beagle or Aardvark.
- Debug connector on all UARTS. 4-pin 2.54mm headers.
- POST LEDs.

- BIOS Debug Support Including:
 - Two socketed BIOS Flash (socket to be removed for production)
 - BIOS recovery jumper connected to PCH GPIO
 - Flash security override driven from BMC GPIO (to PCH)
- CPU and PCH XDP60 support.
- Intel® Trace Hub and Direct Connect Interface (DCI)
 - DCI is supported in an open chassis through XDP60 connector and Intel® ITP-XDP3BR.
 - DCI Boundary Scan Side Band (BSSB) is supported in a closed chassis through USB3.0 and Intel® SVT Closed Chassis Adapter.
 - DCI USB3 is supported through front panel USB3 connector and USB3 Debug Cable
- Two USB 3.0 debug ports connected to PCH USB1 Port 2 and Port 3 available at the front of motherboard (cold aisle)
- PCH Recovery Mode Jumper
- HW jumper to enable BIOS serial debug output

8.2 LED Visibility

The following LEDs determined to be important for communicating status to service personnel are visible at the front (cold aisle) of the motherboard.

- UID LED
- Power Status LED
- Attention LED

9 Motherboard Interfaces

This section describes the connector interfaces to the motherboard.

9.1 PCIe x8 Connectors

The PCIe x8 connectors interfaces are designed to support a standard PCIe x8 card as well as the M.2 riser card. The M.2 riser card is a custom edge card PCA that supports two M.2 SSD Modules (NGFF form factor cards) in the SSD Socket 3 format per the PCI Express M.2 Specification. To support two M.2 modules, the PCIe connector interface is altered to support two x4 PCIe Gen3 interfaces as well as the SSD specific signals per the PCIE M.2 specification. Table 9 describes the connector pinout. The signals satisfy the electrical requirements of the PCIe Card Electromechanical Specification. The following is a list of pin assignment deviations from that specification needed to support two M.2 modules. These signals are highlighted in red.

- SUSCLK is assigned to pin A6 replacing JTAG TDI pin. Support for SUSCLK is not required.
- LINKWIDTH is assigned to pin A17 replacing PRSNT#2. Enables auto-detection of 2x4 M.2 Interposer or 1x8 standard PCIe card. The design is not required to support PCIe x1 cards.
- REFCLK2+/- is assigned to pins A32/A33 replacing two Reserved pins.
- SMBCLK2 and SMBDAT2 are assigned to pins A6/A7 replacing TDO and TMS pins.

Table 9. PCIe x8 connector pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK1	SMBus clock	JTAG2	TCK
6	SMDAT1	SMBus data	SUSCLK	Suspend Clk
7	GND	Ground	SMCLK2	SMBus clock
8	+3.3v	+3.3 volt power	SMDAT2	SMBus data
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PGOOD	Powergood
Mechanical Key				
12	CLKREQ#	Request Running Clock	GND	Ground
13	GND	Ground	REFCLK1+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK1-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	LINKWIDTH	0= 2 x4 1= 1 x8	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,

26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	RSVD	Reserved	PERN(3)	Differential pair
31	PRSNT#2	Presence Detect	GND	Ground
32	GND	Ground	REFCLK2+	Reference Clock
33	PETP(4)	Transmitter Lane 4,	REFCLK2-	Differential pair
34	PETN(4)	Differential pair	GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4,
36	GND	Ground	PERN(4)	Differential pair
37	PETP(5)	Transmitter Lane 5,	GND	Ground
38	PETN(5)	Differential pair	GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5,
40	GND	Ground	PERN(5)	Differential pair
41	PETP(6)	Transmitter Lane 6,	GND	Ground
42	PETN(6)	Differential pair	GND	Ground
43	GND	Ground	PERP(6)	Receiver Lane 6,
44	GND	Ground	PERN(6)	Differential pair
45	PETP(7)	Transmitter Lane 7,	GND	Ground
46	PETN(7)	Differential pair	GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7,
48	PRSNT#2	Presence detect	PERN(7)	Differential pair
49	GND	Ground	GND	Ground

9.2 PCIe x16 Connectors

The PCIe x16 connector interface is designed to support a standard PCIe x16 full-height card. The pinout for supporting PCIe x16 described in Table 10. This interface also supports the PWRBRK# power reduction feature. Note that this signal is declared on pins B12 and B30. This enables support for the feature on existing platforms (B12) and meets the latest PCI SIG definition (B30). For further information, refer to the PCI Express® Card Electromechanical Specification.

Table 10. PCIe x16 connector pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description

1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	PWRBRK#	Power Reduction	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	PRSNT#2	Presence detect	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	PWRBRK#	Power Reduction	PERN(3)	Differential pair
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETP(4)	Transmitter Lane 4,	RSVD	Reserved
34	PETN(4)	Differential pair	GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4,

36	GND	Ground	PERN(4)	Differential pair
37	PETP(5)	Transmitter Lane 5,	GND	Ground
38	PETN(5)	Differential pair	GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5,
40	GND	Ground	PERN(5)	Differential pair
41	PETP(6)	Transmitter Lane 6,	GND	Ground
42	PETN(6)	Differential pair	GND	Ground
43	GND	Ground	PERP(6)	Receiver Lane 6,
44	GND	Ground	PERN(6)	Differential pair
45	PETP(7)	Transmitter Lane 7,	GND	Ground
46	PETN(7)	Differential pair	GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7,
48	PRSNT#2	Hot plug detect	PERN(7)	Differential pair
49	GND	Ground	GND	Ground
50	PETP(8)	Transmitter Lane 8,	RSVD	Reserved
51	PETN(8)	Differential pair	GND	Ground
52	GND	Ground	PERP(8)	Receiver Lane 8,
53	GND	Ground	PERN(8)	Differential pair
54	PETP(9)	Transmitter Lane 9,	GND	Ground
55	PETN(9)	Differential pair	GND	Ground
56	GND	Ground	PERP(9)	Receiver Lane 9,
57	GND	Ground	PERN(9)	Differential pair
58	PETP(10)	Transmitter Lane 10,	GND	Ground
59	PETN(10)	Differential pair	GND	Ground
60	GND	Ground	PERP(10)	Receiver Lane 10,
61	GND	Ground	PERN(10)	Differential pair
62	PETP(11)	Transmitter Lane 11,	GND	Ground
63	PETN(11)	Differential pair	GND	Ground
64	GND	Ground	PERP(11)	Receiver Lane 11,
65	GND	Ground	PERN(11)	Differential pair
66	PETP(12)	Transmitter Lane 12,	GND	Ground
67	PETN(12)	Differential pair	GND	Ground
68	GND	Ground	PERP(12)	Receiver Lane 12,
69	GND	Ground	PERN(12)	Differential pair
70	PETP(13)	Transmitter Lane 13,	GND	Ground
71	PETN(13)	Differential pair	GND	Ground

72	GND	Ground	PERP(13)	Receiver Lane 13,
73	GND	Ground	PERN(13)	Differential pair
74	PETP(14)	Transmitter Lane 14,	GND	Ground
75	PETN(14)	Differential pair	GND	Ground
76	GND	Ground	PERP(14)	Receiver Lane 14,
77	GND	Ground	PERN(14)	Differential pair
78	PETP(15)	Transmitter Lane 15,	GND	Ground
79	PETN(15)	Differential pair	GND	Ground
80	GND	Ground	PERP(15)	Receiver Lane 15,
81	PRSNT#2	Hot plug present detect	PERN(15)	Differential pair
82	RSVD#2	Hot Plug Detect	GND	Ground

9.3 PCIe MiniSAS HD Connectors

The motherboard optionally supports vertical MiniSAS HD connectors for cabling PCIe from the motherboard to PCIe expansion cards. The connector supports 4 lanes of PCIe and the necessary management signals (clocks, PERST#) to operate as a standalone PCIe interface. The pinout is shown in Table 11.

Table 11. PCIe Cable Connector Pinout

PCIe Cable Connector Pinout		
Pin	Signal	Description
D9	GND	Ground
D8	TX2-	PCIe Transmit Lane 2
D7	TX2+	PCIe Transmit Lane 2
D6	GND	Ground
D5	TX0-	PCIe Transmit Lane 0
D4	TX0+	PCIe Transmit Lane 0
D3	GND	Ground
D2	SB6	BMC_SMB_CLK
D2	SB5	BMC_SMB_DAT
C1	NC	NC
C2	NC	NC
C3	GND	Ground
C4	TX1+	PCIe Transmit Lane 1
C5	TX1-	PCIe Transmit Lane 1
C6	GND	Ground
C7	TX3+	PCIe Transmit Lane 3

C8	TX3-	PCIe Transmit Lane 3
C9	GND	Ground
B9	GND	Ground
B8	RX2-	PCIe Receive Lane 2
B7	RX2+	PCIe Receive Lane 2
B6	GND	Ground
B5	RX0-	PCIe Receive Lane 0
B4	RX0+	PCIe Receive Lane 0
B3	GND	Ground
B2	GND	GND
B1	PERST#	PERST#
A1	REFCLK+	PCIe Reference Clock
A2	REFCLK-	PCIe Reference Clock
A3	GND	Ground
A4	RX1+	PCIe Receive Lane 1
A5	RX1-	PCIe Receive Lane 1
A6	GND	Ground
A7	RX3+	PCIe Receive Lane 3
A8	RX3-	PCIe Receive Lane 3
A9	GND	Ground

9.4 M.2 Connectors

M.2 connectors are integrated into the motherboard for supporting flash memory expansion. The M.2 connector pinout is shown in Table 12. For more information about the M.2 interface, refer to the PCI Express M.2 Specification.

Table 12. M.2 connector pinout

M.2 Module Standard Pinout					
Pin	Signal	Description	Pin	Signal	Description
74	3.3V	3.3V Power	75	GND	Ground
72	3.3V	3.3V Power	73	GND	Ground
70	3.3V	3.3V Power	71	GND	Ground
68	SUSCLK(32KHz)	Reduce Power Clock	69	NC	Reserved
66	KEY	Module Key	67	GND	Ground
64	KEY	Module Key	65	KEY	Module Key
62	KEY	Module Key	63	KEY	Module Key
60	KEY	Module Key	61	KEY	Module Key

58	NC	Reserved	59	KEY	Module Key
56	NC	Reserved	57	GND	Ground
54	PEWAKE#	PCIe PME Wake (Open Drain)	55	REFLKCP	PCIe Reference Clock
52	CLKREQ#	Reference Clock Request	53	REFLKCN	PCIe Reference Clock
50	PERST#	PCIe Reset	51	GND	Ground
48	NC	Reserved	49	PETP0	PCIe Transmit Lane 0
46	NC	Reserved	47	PETN0	PCIe Transmit Lane 0
44	ALERT#	SMBus ALERT	45	GND	Ground
42	SMB_DATA	SMBus Data	43	PERP0	PCIe Receive Lane 0
40	SMB_CLK	SMBus Clock	41	PERN0	PCIe Receive Lane 0
38	DEVSLP	Device Sleep	39	GND	Ground
36	NC	Reserved	37	PETP1	PCIe Transmit Lane 1
34	NC	Reserved	35	PETN1	PCIe Transmit Lane 1
32	NC	Reserved	33	GND	Ground
30	NC	Reserved	31	PERP1	PCIe Receive Lane 1
28	NC	Reserved	29	PERN1	PCIe Receive Lane 1
26	NC	Reserved	27	GND	Ground
24	NC	Reserved	25	PETP2	PCIe Transmit Lane 2
22	NC	Reserved	23	PETN2	PCIe Transmit Lane 2
20	NC	Reserved	21	GND	Ground
18	3.3V	3.3V Power	19	PERP2	PCIe Receive Lane 2
16	3.3V	3.3V Power	17	PERN2	PCIe Receive Lane 2
14	3.3V	3.3V Power	15	GND	Ground
12	3.3V	3.3V Power	13	PETP3	PCIe Transmit Lane 3
10	DAS/DSS#	Drive Active Signal (Open Drain)	11	PETN3	PCIe Transmit Lane 3
8	NC	Reserved	9	GND	Ground
6	NC	Reserved	7	PERP3	PCIe Receive Lane 3
4	3.3V	3.3V Power	5	PERN3	PCIe Receive Lane 3
2	3.3V	3.3V Power	3	GND	Ground
			1	GND	Ground

9.5 SATA Cable Ports

The motherboard supports four x1 SATA standard 7-pin connectors. The motherboard optionally supports up to two x4 MiniSAS HD connectors for expansion cabling of up to 8 additional SATA devices (12 total).

9.6 SATA Power Connector

The motherboard supports two 4-pin Mini-Fit® Jr™ 5566 series power connectors, Molex P/N 39-28-1043 or equivalent for supplying power to up to 4 SATA devices. Each connector pin has a maximum 13A current capacity. Table 13 describes the connector pinout. Figure 10 shows a top view of the physical pin numbering.

Table 13. SATA Power Connector

Pin	Signal name	Capacity (in A)
Pin 1 & 2	GND	13A (Black)
Pin 3	12V	9A (Yellow)
Pin 4	5V	9A (Red)

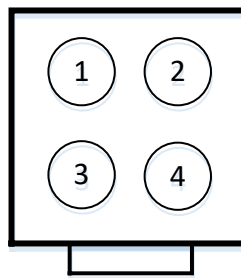


Figure 10. SATA Power Connector Pin Numbering

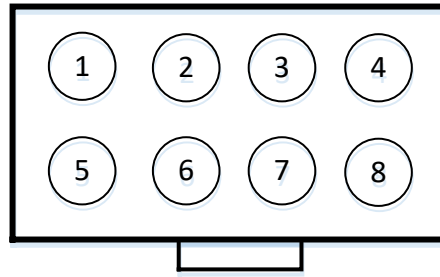
9.7 SATA Power Expansion Connector

The motherboard supports two 8-pin Mini-Fit® Jr™ 5566 series power connectors, Molex P/N 39-28-1083 or equivalent for supplying power to up to 8 additional SATA devices. Each connector has a maximum 13A current capacity. Table 14 describes the connector pinout. Figure 11 shows a top view of the physical pin numbering.

Table 14. SATA Power Expansion Connector Pinout

Pin	Signal name	Capacity (in A)
Pin 1-4	GND	13A (Black)
Pin 5,6	12V	9A (Yellow)
Pin 7,8	5V	9A (Red)

Figure 11. SATA Power Expansion Connector Pin Numbering



9.8 12V Power Connector

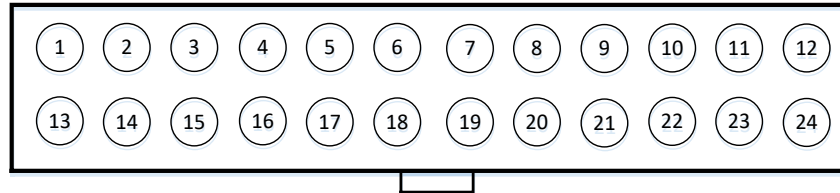
The motherboard supports a 24-pin Mini-Fit® Jr™ 5569 series power connector, Molex P/N 3930-0240 or equivalent to support 12V cabling from the motherboard to the PSU. The connector supports a maximum of 13A per pin. Table 15 describes the connector pinout. Figure 12 shows a top view of the physical pin numbering. For further information, refer to the Project Olympus PSU Specification.

Table 15. 12V Power Connector

Management Connector				
Pin	Signal	I/O	Voltage	Description
1	GND	I	0V	GND from PSU
2	GND	I	0V	GND from PSU
3	GND	I	0V	GND from PSU
4	GND	I	0V	GND from PSU
5	GND	I	0V	GND from PSU
6	GND	I	0V	GND from PSU
7	P12V_PSU	I	12V	12V Power from PSU
8	P12V_PSU	I	12V	12V Power from PSU
9	P12V_PSU	I	12V	12V Power from PSU
10	P12V_PSU	I	12V	12V Power from PSU
11	P12V_PSU	I	12V	12V Power from PSU
12	P12V_PSU	I	12V	12V Power from PSU
13	GND	I	0V	GND from PSU
14	GND	I	0V	GND from PSU
15	GND	I	0V	GND from PSU
16	GND	I	0V	GND from PSU
17	GND	I	0V	GND from PSU
18	GND	I	0V	GND from PSU
19	P12V_PSU	I	12V	12V Power from PSU
20	P12V_PSU	I	12V	12V Power from PSU
21	P12V_PSU	I	12V	12V Power from PSU
22	P12V_PSU	I	12V	12V Power from PSU

23	P12V_PSU	I	12V	12V Power from PSU
24	P12V_PSU	I	12V	12V Power from PSU

Figure 12. Mini-Fit Connector Pin Numbering



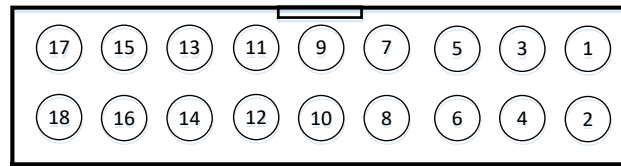
9.9 Management Connector

The motherboard supports a connector for interfacing management signals from the motherboard to the WCS P2010 PSU. The connector for supporting the cable is an 18 pin Molex Picoblade™ series connector, Molex part number 87831-1820 or equivalent. Table 16 describes the connector pinout. Figure 13 shows a top view of the physical pin numbering.

Table 16. Management Connector

1U Management Connector				
Pin	Signal	I/O	Voltage	Description
1	PWR_EN#	I	3.3V	Enable signal from Rack Manager to HSC on the Server
2	LR_SELECT	I	RS232	Left/Right Node Select
3	SLOT_ID0	I	3.3V	SLOT ID from PMDU to the Server
4	SLOT_ID1	I	3.3V	SLOT ID from PMDU to Server
5	SERVER_THROTTLE#	I	3.3V	Server Throttle control from Rack Manager
6	PRESENT#	O	3.3V	Indicates Server presence to the Rack Manager
7	I2C_SCL	O	3.3V	I ² C Clock to PSU (PMBus)
8	I2C_SDA	I/O	3.3V	I ² C Data to PSU (PMBus)
9	I2C_GND	I	0V	GND reference for I ² C bus
10	PS_ON#	O	3.3V	Turns on PSU. Pulled low on MB
11	PSU_ALERT#	I	3.3V	I ² C Alert from the PSU
12	PSU_LED0	I	3.3V	PSU LED 0(Green)
13	PSU_LED1	I	3.3V	PSU LED 1(Yellow)
14	SLOT_ID2	I	3.3V	SLOT ID from PMDU to Server
15	SLOT_ID3	I	3.3V	SLOT ID from PMDU to Server
16	SLOT_ID4	I	3.3V	SLOT ID from PMDU to Server
17	SLOT_ID5	I	3.3V	SLOT ID from PMDU to Server
18	NC	NA	NA	No Connect

Figure 13. Management Connector Pin Numbering



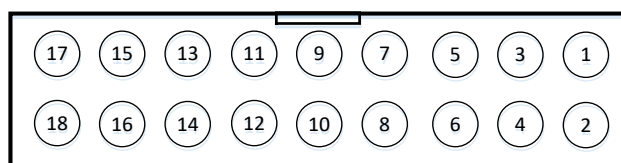
9.10 Management Expansion Connector

The motherboard includes a connector for enabling management and power control of expansion hardware. The connector for supporting the cable is an 18 pin Molex Picoblade™ series connector, Molex part number 87831-1820 or equivalent. Table 17 describes the connector pinout. Figure 14 shows a top view of the physical pin numbering.

Table 17. Management Expansion Connector

Management Connector				
Pin	Signal	I/O	Voltage	Description
1	NC	NA	NA	No Connect
2	I2C1_SDA	I	3.3V	I2C Data (expansion)
3	I2C1_SCL	I	3.3V	I2C Clock (expansion)
4	GND	I	0V	Ground
5	NC	I	0V	Server Throttle control from Rack Manager
6	PRESENT#	O	3.3V	Indicates Server presence to the Rack Manager
7	I2C2_SCL	O	3.3V	I2C Clock to expansion PSU (PMBus)
8	I2C2_SDA	I/O	3.3V	I2C Data to expansion PSU (PMBus)
9	GND	I	0V	Ground
10	PS_ON#	O	3.3V	Turns on PSU. Pulled low on MB
11	PSU_ALERT#	I	3.3V	I ² C Alert from the PSU
12	PSU_LED0	I	3.3V	PSU LED 0(Green)
13	PSU_LED1	I	3.3V	PSU LED 1(Yellow)
14	NC	NA	NA	No Connect
15	NC	NA	NA	No Connect
16	NC	NA	NA	No Connect
17	NC	NA	NA	No Connect
18	NC	NA	NA	No Connect

Figure 14. Management Expansion Connector Pin Numbering



9.11 OCuLink x8 Connector

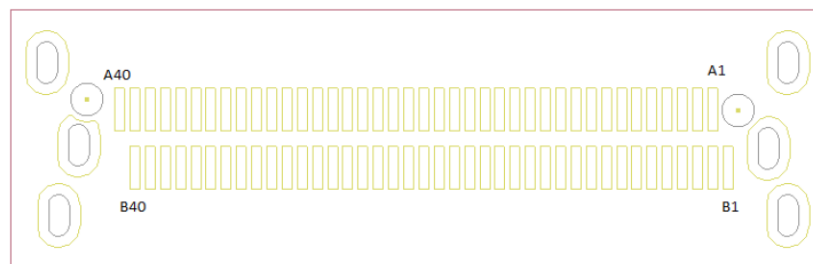
The motherboard supports a connector for cabling PCIe x8 from the motherboard to the FPGA Card. The connector for supporting the cable is an 80-pin vertical Molex Nanopitch™ series connector, (Molex part number 173162-0334 or equivalent). Table 18 describes the connector pinout. Figure 15 shows a top view of the physical pin numbering.

Table 18. OCuLink x8 Connector Pinout

Row A			Row B		
Pin	Signal Name	Description	Pin	Signal Name	Description
A1	GND	Ground	B1	GND	Ground
A2	PERp0	PCIe Receive Data to CPU	B2	PETp0	PCIe Transmit Data from CPU
A3	PERn0	PCIe Receive Data to CPU	B3	PETn0	PCIe Transmit Data from CPU
A4	GND	Ground	B4	GND	Ground
A5	PERp1	PCIe Receive Data to CPU	B5	PETp1	PCIe Transmit Data from CPU
A6	PERn1	PCIe Receive Data to CPU	B6	PETn1	PCIe Transmit Data from CPU
A7	GND	Ground	B7	GND	Ground
A8	NC	No Connect	B8	NC	No Connect
A9	NC	No Connect	B9	NC	No Connect
A10	GND	Ground	B10	GND	Ground
A11	NC	No Connect	B11	NC	No Connect
A12	NC	No Connect	B12	CPRSNT#	Cable Present
A13	GND	Ground	B13	GND	Ground
A14	PERp2	PCIe Receive Data to CPU	B14	PETp2	PCIe Transmit Data from CPU
A15	PERn2	PCIe Receive Data to CPU	B15	PETn2	PCIe Transmit Data from CPU
A16	GND	Ground	B16	GND	Ground
A17	PERp3	PCIe Receive Data to CPU	B17	PETp3	PCIe Transmit Data from CPU
A18	PERn3	PCIe Receive Data to CPU	B18	PETn3	PCIe Transmit Data from CPU
A19	GND	Ground	B19	GND	Ground
A20	RSVD	Reserved	B20	RSVD	Reserved
A21	RSVD	Reserved	B21	RSVD	Reserved
A22	GND	Ground	B22	GND	Ground
A23	PERp4	PCIe Receive Data to CPU	B23	PETp4	PCIe Transmit Data from CPU
A24	PERn4	PCIe Receive Data to CPU	B24	PETn4	PCIe Transmit Data from CPU
A25	GND	Ground	B25	GND	Ground
A26	PERp5	PCIe Receive Data to CPU	B26	PETp5	PCIe Transmit Data from CPU
A27	PERn5	PCIe Receive Data to CPU	B27	PETn5	PCIe Transmit Data from CPU
A28	GND	Ground	B28	GND	Ground
A29	NC	No Connect	B29	NC	No Connect
A30	NC	No Connect	B30	NC	No Connect

A31	GND	Ground	B31	GND	Ground
A32	NC	No Connect	B32	NC	No Connect
A33	NC	No Connect	B33	NC	No Connect
A34	GND	Ground	B34	GND	Ground
A35	PERp6	PCIe Receive Data to CPU	B35	PETp6	PCIe Transmit Data from CPU
A36	PERn6	PCIe Receive Data to CPU	B36	PETn6	PCIe Transmit Data from CPU
A37	GND	Ground	B37	GND	Ground
A38	PERp7	PCIe Receive Data to CPU	B38	PETp7	PCIe Transmit Data from CPU
A39	PERn7	PCIe Receive Data to CPU	B39	PETn7	PCIe Transmit Data from CPU
A40	GND	Ground	B40	GND	Ground

Figure 15. OCUlink x8 Pin Numbering



9.12 NCSI Connector

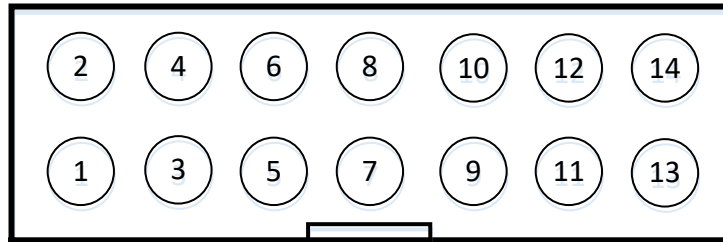
The motherboard supports a connector for cabling NCSI signals from the motherboard to a Network Interface Controller (NIC). The connector for supporting the cable is a 14-pin header connector, Molex part number 87831-1428 or equivalent. Table 19 describes the connector pinout. Table 19 shows a top view of the physical pin numbering.

Table 19. NCSI Connector

NCSI Connector				
Pin	Signal	I/O	Voltage	Description
1	RXER	O	3.3V	Enable signal from Rack Manager to HSC on the motherboard
2	GND	I	0V	Ground
3	TXD1	I	3.3V	Transmit Data from BMC to NIC
4	CLK_50M	I	0V	50Mhz Clock
5	TXD0	I	3.3V	Transmit Data from BMC to NIC
6	GND	I	0V	Ground
7	TXEN	I	3.3V	Transmit Enable from BMC to NIC
8	GND	I	0V	Ground
9	CRSDV	O	3.3V	Receive carrier sense and data valid from NIC to BMC
10	GND	I	0V	Ground
11	RXD1	O	3.3V	Receive Data from NIC to BMC

12	GND	I	0V	Ground
13	RXD0	O	3.3V	Receive Data from NIC to BMC
14	GND	I	0V	Ground

Figure 16. NCSI Connector Pin Numbering



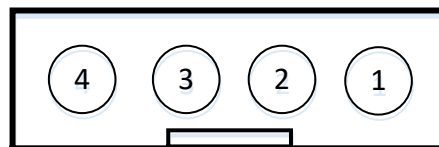
9.13 USB 2.0 Internal Header

The motherboard supports a header connector for enabling USB 2.0 communication with the FPGA card. The connector is TE 440054-4 or equivalent. Table 20 describes the connector pinout. Figure 17 shows a top view of the physical pin numbering.

Table 20. Internal USB Connector

Pin	Signal Name	I/O	Logic	Name/Description
1	P5_USB			5V (500mA max)
2	USB_N	I/O		USB Data
3	USB_P	I/O		USB Data
4	GND			Ground

Figure 17. Internal USB Connector Pinout



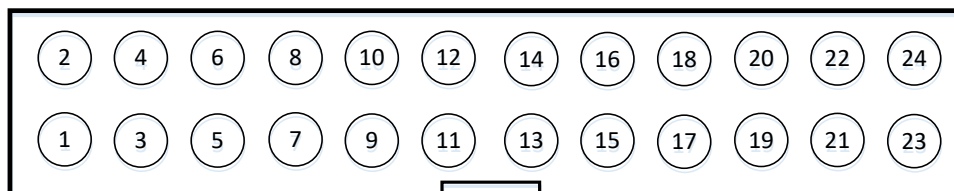
9.14 Fan Control Connector

The motherboard supports two header connectors for enabling fan control. The connectors are Molex 87831-2420 or equivalent. Table 21 describes the connector pinout. Figure 18 shows a top view of the physical pin numbering.

Table 21. Fan Control Connector

Management Connector				
Pin	Signal	I/O	Voltage	Description
1	FAN5_PWM	O	5V	Fan #5 PWM
2	FAN4_PWM	O	5V	Fan #4 PWM
3	FAN5_TACH	I	5V	Fan #5 Tachometer
4	FAN4_TACH	I	5V	Fan #4 Tachometer
5	P12V	O	12V	12V Fan Power
6	P12V	O	12V	12V Fan Power
7	GND	O	0V	Ground
8	GND	O	0V	Ground
9	FAN3_PWM	O	5V	Fan #3 PWM
10	FAN2_PWM	O	5V	Fan #2 PWM
11	FAN3_TACH	I	0V	Fan #3 Tachometer
12	FAN2_TACH	I	3.3V	Fan #2 Tachometer
13	P12V	I	3.3V	12V Fan Power
14	P12V	I	3.3V	12V Fan Power
15	GND	O	0V	Ground
16	GND	O	0V	Ground
17	FAN1_PWM	O	5V	Fan #1 PWM
18	FAN0_PWM	O	5V	Fan #0 PWM
19	FAN1_TACH	I	5V	Fan #1 Tachometer
20	FAN0_TACH	I	5V	Fan #0 Tachometer
21	P12V	O	12V	12V Fan Power
22	P12V	O	12V	12V Fan Power
23	GND	O	0V	Ground
24	GND	O	0V	Ground

Figure 18. Fan Control Connector Pin Numbering



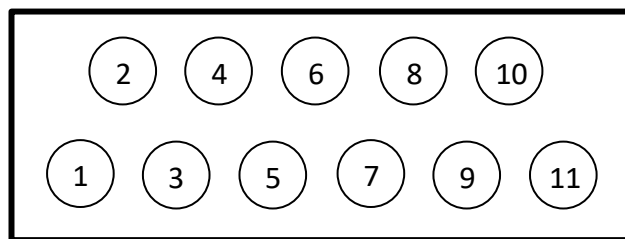
9.15 TPM Connector

The motherboard supports a header connector for interfacing to a TPM Module. The connector is FCI 91932-32111L or equivalent. Table 22 describes the connector pinout. Figure 19 shows a top view of the physical pin numbering.

Table 22. TPM Connector Pinout

TPM Connector				
Pin	Signal	I/O	Voltage	Description
1	SPI_CLK	O	3.3V	SPI Clock
2	RESET#	O	3.3V	Reset
3	SPI_MOSI	O	3.3V	SPI Data Out
4	SPI_MISO	I	3.3V	SPI Data In
5	SPI_CS#	O	3.3V	SPI Chip Select
6	I2C_SDA	I/O	3.3V	I2C Data
7	P3V3_STBY	O	3.3V	3.3V Standby Power
8	TPM_PRESENT#	I	3.3V	Indicates physical presence of TPM
9	SPI_IRQ#	I	3.3V	Interrupt
10	I2C_SCL	O	3.3V	I2C Clock
11	GND	O	0V	Ground

Figure 19. TPM Connector Pin Numbering



9.16 Connector Quality

The Project Olympus system is designed for use in datacenters with a wide range of humidity. The connectors for these deployments are be capable of withstanding high humidity during shipping and installation. The baseline for plating DIMMs and PCIe connectors is required to be 30μ"-thick gold. DIMM connectors also required to include lubricant/sealant applied by the connector manufacturer that can remain intact after soldering and other manufacturing processes. The sealant is required to displace any voids in the connector gold plating.

10 Electrical Specifications

The following sections provide specifications for the blade input voltage and current, as well as the primary blade signals.

10.1 Input Voltage, Power, and Current

Table 23 lists the nominal, maximum, and minimum values for the motherboard input voltage. The maximum and minimum voltages include the effects of connector temperature, age, noise/ripple, and dynamic loading.

Table 23. Input Power Requirements

	Minimum	Nominal	Max
Input voltage	11V DC	12.3V DC	14V DC
Input Power	n/a	n/a	750W
Inrush Rise Time	5ms	n/a	200ms

12V power to the motherboard is supplied through a 24 pin Mini-Fit Jr or equivalent connector. The blade provides inrush current control through the 12V bus rail; return-side inrush control is not used. The inrush current rises linearly from 0A to the load current over a minimum 5 millisecond (ms) period (this time period must be no longer than 200ms).

10.2 Current Interrupt Protection and Power, Voltage, and Current Monitoring

The blade provides a cost-effective way to measure and report blade voltage and current consumption, and to make instance reporting available to the system. The blade shall include power consumption measurements at the inrush controller. (Accuracy of the measurement shall be +/- 2%)

The blade also provides a way to interrupt current flow within 1 microsecond (μ s) of exceeding the maximum current load.

10.3 Filtering and Capacitance

The blade should provide sufficient input filtering and capacitance to support operation with the power supply as specified in the P2010 PSU Specification.

10.4 Grounding and Return

The blade chassis grounding/return is provided to the motherboard from the tray assembly through the alignment and mounting holes that secure the motherboard to the tray. The motherboard is also tied to the PSU ground through the 12V power connector. Chassis ground and Logic ground are tied together on the motherboard.

11 PCB Stack-up

Figure 20 shows the 8-layer PCB stack-up. The stackup uses standard mid-loss FR4 PCB material. The PCB thickness is 72 mils.

0.072", 8 Layers, TU863/IT170GRA/NPG171 Lead-Free / OSP / Tg>170 All dimensions in mils				Differential										Single Ended					
			Signals ->	PCIe; UPI; DMI; Diff Clocks; USB2/3; SATA3; SATAe			SFI; 10G-KR, option 1 (*5)			10G-KR, option 2 (*5)			Signal Integrity		DDR (1 SPC DQ/DQS); Misc I/O; SE clocks		DDR (2 SPC DQ/DQS; all C/A/CLK)		
				Z0->	85 Ohms			93 Ohms			100 Ohms			Insertion Loss		50 Ohms		40 Ohms	
Layer Name	Plane Description		Copper Weight (oz)	Layer Thickness (mil)	Width	Space	Z0 tol.	Width	Space	Z0 tol.	Width	Space	Z0 tol.	Max SDD21 4GHz	Max SDD21 8GHz	Width	Z0 tol.	Width	Z0 tol.
	solder mask			0.5															
L1	SIGNAL		0.5 oz.	1.9	5.00	7.00	+/-15%	4.50	13.50	+/-10%	4.01	13.99	+/-10%	0.69	1.33	4.00	+/-15%	6.50	+/-15%
	prepreg			2.7															
L2	GND	POWER	1.0 oz.	1.3															
	core			4.0															
L3	SIGNAL	GND	1.0 oz.	1.3	5.00	6.50	+/-10%	4.90	10.30	+/-10%	4.40	13.00	+/-10%	0.65	1.25	4.75	+/-10%	7.75	+/-10%
	prepreg			19.7															
L4	GND	POWER	2.0 oz.	2.6															
	Core			4.0															
L5	GND	POWER	2.0 oz.	2.6															
	prepreg			19.7															
L6	SIGNAL	GND	1.0 oz.	1.3	5.00	6.50	+/-10%	4.90	10.30	+/-10%	4.40	13.00	+/-10%	0.65	1.25	4.75	+/-10%	7.75	+/-10%
	core			4.0															
L7	GND	POWER	1.0 oz.	1.3															
	prepreg			2.7															
L8	SIGNAL		0.5 oz.	1.9	5.00	7.00	+/-15%	4.50	13.50	+/-10%	4.01	13.99	+/-10%	0.69	1.33	4.00	+/-15%	6.50	+/-15%
	solder mask			0.5															
			9.0 oz.	72.0															

Figure 20. PCB Stackup

12 Physical Specification

The motherboard is fully compatible with the mechanical requirement of the Project Olympus Universal Motherboard Specification. The motherboard is intended to be deployable in a variety of server mechanical configurations. Figure 21 depicts the dimensions of the motherboard. The front of the chassis is on the bottom side. For detailed mechanical information including mounting hole location and dimensions, reference the Project Olympus mechanical data package.

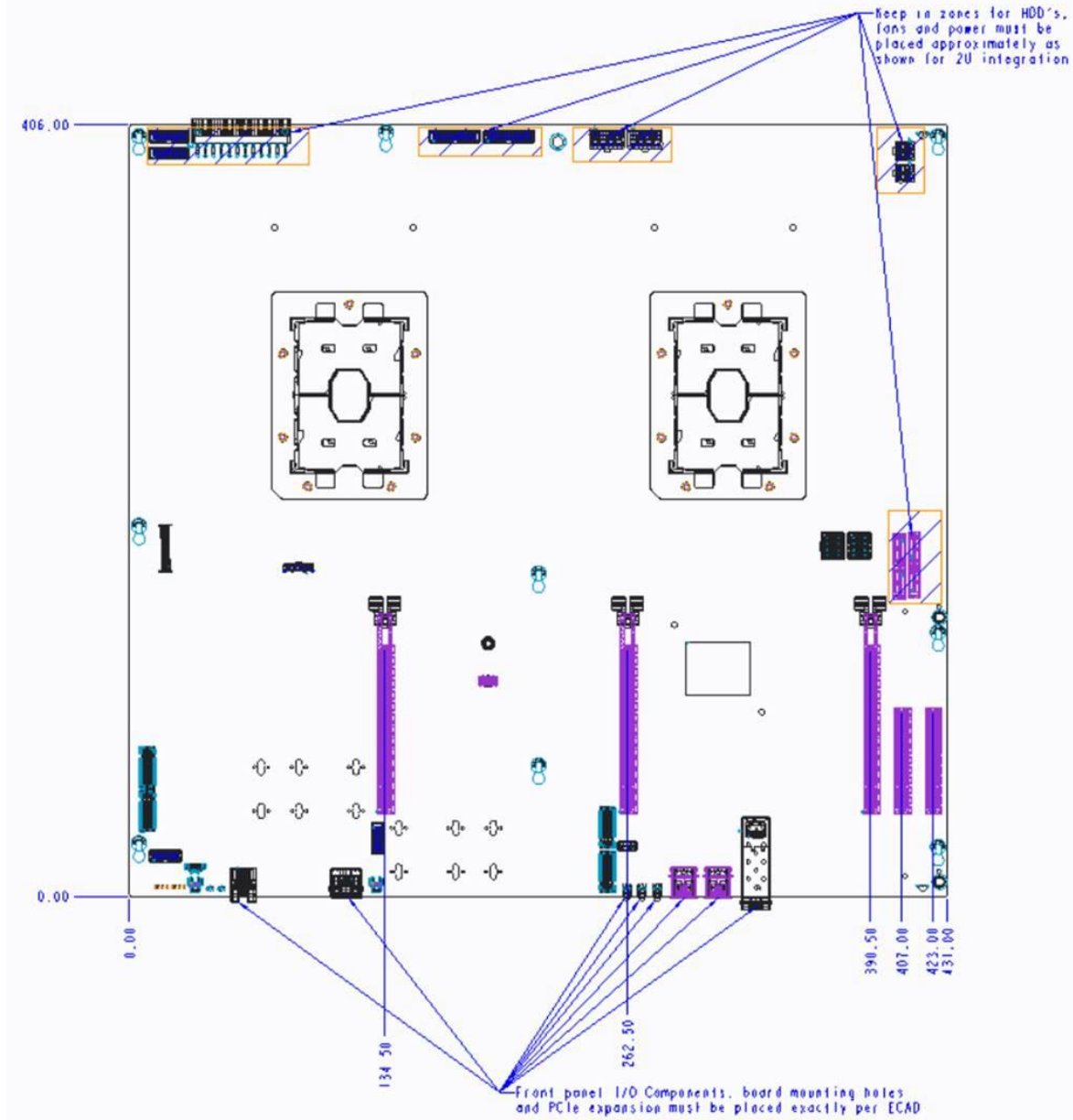


Figure 21. Example Motherboard Drawing

13 Environmental

The motherboard is designed to be deployed in an environmentally controlled location meeting the environmental requirements describe in Table 24. The server must have the capability to provide full functional operation under the conditions given.

Table 24. Environmental Requirement

Specification		Requirement
Inlet temperature	Operating	• 50°F to 95°F (10°C to 35°C) • Maximum rate of change: 18°F (10°C)/hour • Allowable derating guideline of 1.6°F/1000ft (0.9°C/304m) above 3000 ft.
	Non-operating	• -40°F to 140°F (-40°C to 60°C) • Rate of change less than 36°F (20°C)/hour

14 Electromagnetic Interference Mitigation

Electromagnetic interference (EMI) containment, EMI shielding and grounding must be accounted for at the server assembly level.