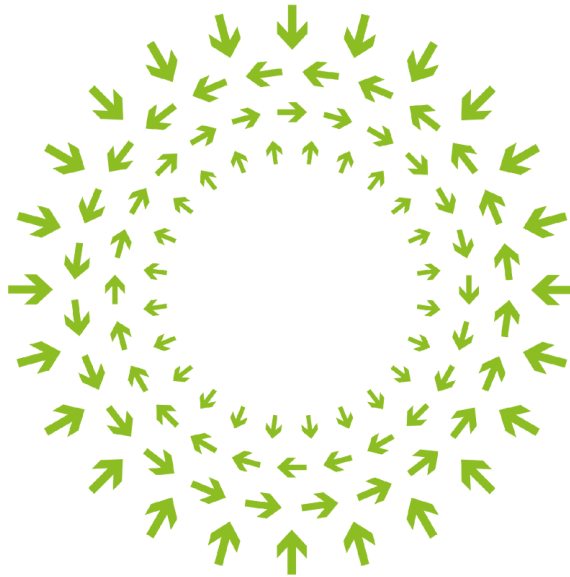




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Meta Minipack3 OCP-Specification-All-in-One

1.0.0

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Version History

Note, refer to the OCP Contribution Versions, Revisions and Errata best practices documentation. Generally speaking, Versions and revisions are made to this document and logged here. Errata is a separate document such that the contribution specification document it refers to was not revised. Ex: Version 1, Errata E1

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1. License

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- ☒ ~~OPTION A: OCP CLA~~
- ☐ OPTION B: Open Web Foundation (OWF) CLA

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2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following for their feedback:

List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

3. Compliance with OCP Tenets

Please describe how this Specification complies to the following OCP tenets. Compliance is required for at least four of the five tenets (Sustainability is a required tenet). The ideals behind open sourcing stipulate that everyone benefits when we share and work together. Any open source project is designed to promote sharing of design elements with peers and to help them understand and adopt those contributions. There is no purpose in sharing if all parties aren't aligned with that philosophy. The OCP Incubation Committee will look beyond the contribution for evidence that the contributor is aligned with this philosophy. The contributor actions, past and present, are evidence of alignment and conviction to all the tenets.

A full explanation of the OCP core tenets can be seen [here](#).

3.1. Openness

The electrical design and mechanical design of Minipack3 is fully open. All the PCB, BOM and chassis design files have been included in the design package that has been submitted to the OCP community.

3.2. Efficiency

The Minipack3 system has a PHY-less design and traditional single-lam PCB construction. It improves operational efficiency over its predecessors. It has significantly lower latency than its predecessors. Its weight is less and its dimensions are smaller than its predecessors.

3.3. Impact

Minipack3 is based on the industry latest and largest 51.2T switch ASIC. It introduces several groundbreaking innovations, such as BMC-lite and PlatformManage, which greatly improved the system performance and the NPI efficiency.

3.4. Scale

Minipack3's major switching role is for the front-end network applications. Its 100G QSFP28 management port allows it to serve some back-end network applications too. Minipack3 can be equipped with either AC PSU or DC PSU. It can be installed on either 19" EIA rack or OpenRackv3 rack. These features allow Minipack3 to be deployed at scale on versatile racks to serve versatile switch roles.

Minipack3 has built-in many sensors to be monitored in the large data centers. The FWs on Minipack3 are field-upgradeable. These features allow Minipack3 can be deployed and maintained at large scale.

3.5. Sustainability

Minipack3 consumes less than 2,100w in the worst case for Meta's applications. It achieves a power efficiency of about 40pj/bit, which is significantly better than its predecessors.

4. Scope

This document defines Meta 51.2T Ethernet open switch hardware base, design and product specification. It applies to Meta's Minipack3 Ethernet switch.

5. Overview

Meta's Minipack3 is a high performance 51.2T Ethernet switch based on Broadcom Tomahawk5 ASIC. It provides 128x400G non-blocking switch capacity, and is backward compatible to 200GE and 100GE standards. The system design aims to improve system reliability, resiliency, operational efficiency and NPI efficiency.

6. Base Specifications

6.1. Repository Location (Strongly Recommended)

N/A

6.2. Environmental Regulatory Compliance and Requirements

The following compliance reports must be from labs accredited to a current version of IEC 17025.

- CE Declaration to the following Regulatory Directives
 - EMC Directive 2014/30/EU
 - Low Voltage (LVD) Directive 2014/35/EU
- Safety Certification
 - CB certificate/report to IEC 62368-1 including all national deviations
 - CB certificate/report to IEC/EN 60950-1 including all national deviations
 - UL/CSA/IEC/EN 60950-1 with all latest amendments
 - UL/IEC 62368-1 with all latest amendments
 - CNS14336 Taiwan BSMI safety regulation
 - EN 60825-1 Safety of Laser products – part 1
 - UL 94-V0 Flammability rating
- EMC certification and report
 - FCC Part 15 (Class A)
 - ICES-003 (Canada) Class A
 - EN55032 (Europe) Class A
 - CISPR32 (International) Class A
 - AS/NZS CISPR32 (Australia and New Zealand) Class A
 - VCCI CISPR 32 (Japan) Class A
 - CNS 13438 (Taiwan) Class A
 - EN61000-3-2
 - EN61000-3-3
 - EN55024
 - EN 61000-4-2 ESD
 - EN 61000-4-3 Radiated Immunity
 - EN 61000-4-4 EFT
 - EN 61000-4-5 Surge
 - EN 61000-4-6 Low Frequency Conducted Immunity
 - EN 61000-4-11 Voltage Variations and Dips

The immunity levels are defined in the following table.

Network Equipment						
Immunity Standard	Description	Standard Criteria (Required)	FB Criteria (Goal)	Standard Level (Required)	FB Level (Goal)	Remarks
IEC 61000-4-2	Electrostatic Discharge (ESD)	B	A	4 kV Cont. / 8 kV Air	8 kV Cont. / 15 kV Air	Criteria A (FB Goal) is highly desirable for any level
IEC 61000-4-3	Radiated Immunity	A	A	3 V/m	10 V/m	For communication cables >3 meters
IEC 61000-4-4	EFT	B	B	0.5 kV		Ports: Signal & Telecom (>3 meters), DC power input
		B	B	1 kV		Ports: AC power input & AC/DC Converter
IEC 61000-4-5	Surges	C	A	1 kV		Ports: Signal and Telecom connected to outdoor cables
		B	A	0.5 kV		Ports: DC power input
				1 kV L-L / 2 kV L-GND		Ports: AC power input & AC/DC Converter
IEC 61000-4-6	Conducted Immunity	A	A	3 V	10 V	Ports: Signal & Telecom (>3 meters), AC and DC power input
IEC 61000-4-8	Magnetic Field	A	A	1 A/m		Only EUT containing devices susceptible to magnetic fields
IEC 61000-4-11	Voltage Dips	B	B	>95% Reduction		Ports: AC power input & AC/DC Converter (0.5 Period)
		C	C	30% Reduction		Ports: AC power input & AC/DC Converter (25 Periods)
	Voltage Interruptions	C	C	>95% Reduction		Ports: AC power input & AC/DC Converter (250 Periods)

The following is the environmental compliance requirement.

- Environmental Compliance
 - RoHS 2
 - REACH (SVHC & Annex 17)
 - WEEE
 - POP Regulation

- Prop 65
- Batteries Directive
- Halogen-free IEC/EN 61249-2-21 (900 ppm Br or Cl, 1500 ppm combined)
- Phthalate (DEHP, DBP, DiBP, BBP)-free (1000 ppm)
- Arsenic-free (1000 ppm)
- CE Declaration to the following environmental Directives by ODM:
 - RoHS Directive 2011/65/EU

6.3. Physical Specifications

Meta's Minipack3 Ethernet switch is capable of 128x400GE non-blocking switch capacity. The following are the key system features and requirements.

- Chassis
 - 4RU
 - Designed to mount in an EIA 19" rack
 - Can be mounted to Open Rack with a purpose-build rack mount kit
 - The depth is specified as 661mm with the max depth of 716.4mm.
- Switch Main Board (SMB) sub-chassis
 - Broadcom Tomahawk5 (TH5) Ethernet switch ASIC, 51.2Tbps with 512x106GPAM4 SERDES lanes.
 - The system architecture doesn't limit the switch ASIC to Broadcom TH5. It could be an equivalent switch ASIC with 512x106GPAM4 SerDes that satisfies the similar hardware interface, thermal, and application software requirements.
 - A 50GbE or 100GbE in QSFP28 form factor is required for the switch ASIC management Ethernet interface. This QSFP28 port shall be downgradable to support 10G SFP+ pluggable module with a QSFP-to-SFP+ adapter.
 - SMB sub-chassis is a Field Replaceable Module (FRU) that is accessible from the front of the main chassis.
- Switch Control Module (SCM)
 - Intel IceLake-D1736 CPU
 - The system architecture doesn't limit the CPU selection to Intel Ice Lake-D1736. An alternative CPU is possible as long as it satisfies the hardware interface, thermal, and application software requirements.
 - Minimum 64GB DDR4 DIMM w/ ECC
 - Minimum 512GB NVMe SSD
 - TPM 2.0 device (soldered down)
 - Front panel RJ45 as RS232 console
 - Front panel RJ45 as Out-Of-Band (OOB) management Ethernet, 1000Base-T
 - Front panel USB 2.0 Type-A port

- SCM is a FRU that is accessible from the front of the main chassis.
- Board Management Controller (BMC)
 - The BMC is hosted on a RunBMC module that is a FRU.
 - Aspeed AST2620 Baseboard Management Controller (Dual ARM core)
 - The system architecture doesn't limit the BMC selection to Aspeed AST2620. An alternative BMC is possible as long as it satisfies the hardware interface, thermal, and application software requirements.
 - Minimum 2GB DDR4 DRAM
 - Minimum 8GB eMMC
 - An OOB management GbE switch connecting the front panel 1000Base-T RJ-45 port, the BMC, and the CPU. The GbE switch shall be managed by BMC via the MDIO bus.
- Power Supply Unit (PSU)
 - The system supports either 1+1 AC PSU or a single DC PSU
 - Typical system power consumption should be less than 2,100W
 - [5°C, 30°C] up to 6000ft
 - [5°C, 35°C] at sea level
 - With Meta's 64x 2x400G-FR4 OSFP optics modules
- Thermal
 - Air cooling
 - Front-to-back airflow
 - The airflow needed for system cooling should not exceed 0.145CFM/W at sea level, or 0.18CFM/W at 6000 ft.

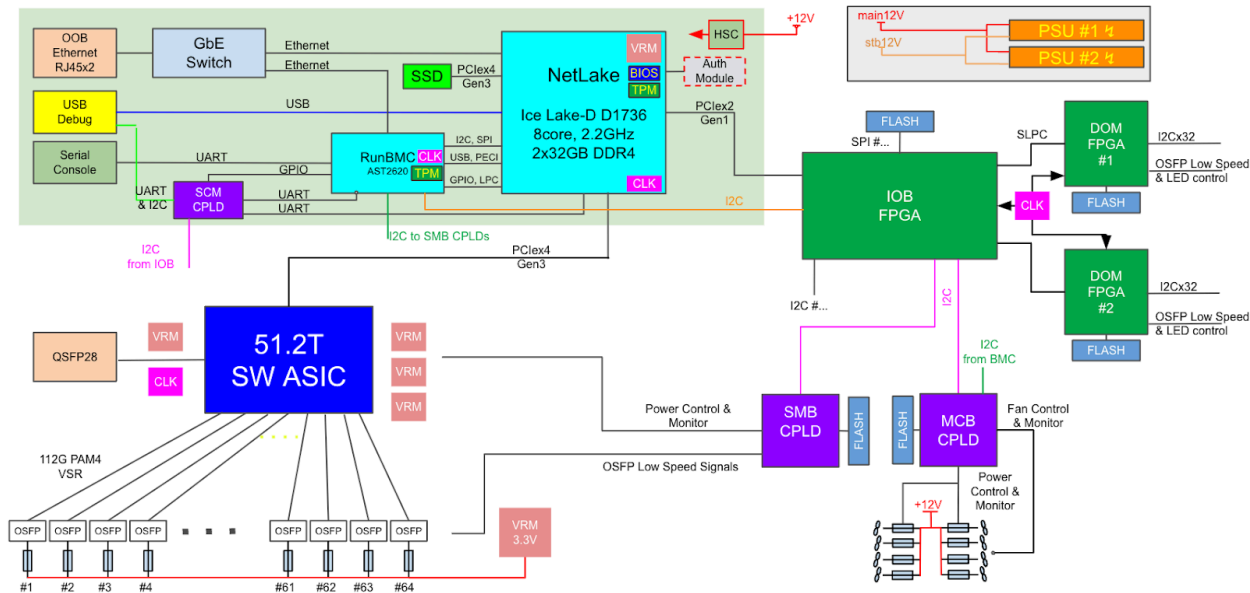
The following table lists the key parameters of Minipack3.

Attributes	Quantity	Notes
Chassis Form Factor	4RU, 19", <30" deep	
Total number of 400GbE-FR4 ports	128	
Total number of 200GbE-FR4 ports	128	
Total number of 100GbE-FR4 ports	128	
Total number of ASIC SERDES lanes	512	
Total number of ASIC PCIe lanes	4, Gen 3	
SCM	1	
BMC	1	

OOB Management GbE switch	1	
Typical Power Consumption	<2,100	
System Airflow	<0.145CFM/W at sea level, and 0.18CFM/W at 6000 ft.	

The Minipack3 system architecture is illustrated in the following diagram. The system contains several major subsystems besides the FRUs such as OSFPs, fans and PSUs:

- SMB carries the switch ASIC, OSFPs and two DOM FPGAs
- SCM carries the Netlake CPU daughter-card, RunBMC daughter-card, OOB GbE switch and SCM CPLD. Netlake is a CPU daughter-card inspired by the COM Express form factor.
- MCB (Main Carrier Board) carries the IOB FPGA, MCB CPLD and fan control hot-swap controllers.



This system uses IOB to offload the I2C and the SPI management tasks from the BMC. It is the first time that Meta introduces this BMC-lite architecture in Meta's network equipment designs.

6.4. Mechanical

Minipack3 chassis maintains the compact 4RU/19" form factor as its predecessors, ensuring seamless integration to Meta's data centers.

There are 64 OSFPs connectors in 2x1 belly-to-belly layout on the front panel. Switch Main Board (SMB) module is a FRU accessible from the front of the chassis. Supervisor Controller Module (SCM) is horizontally orientated, accessible from the front of the chassis. A QSFP28 port on the front panel connects to the ASIC Ethernet management port.

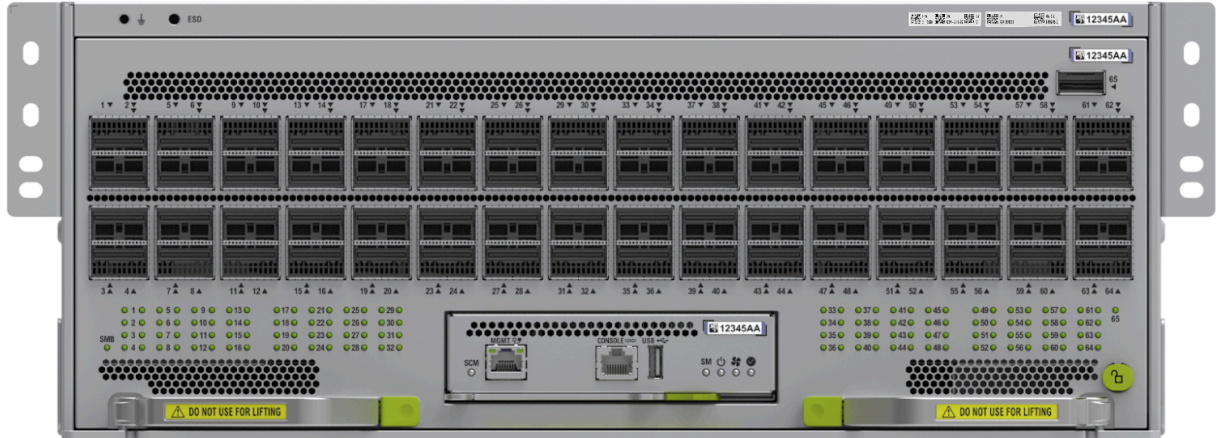


Figure 6-1: Minipack3 Chassis Front View

The Minipack3 has 8 fan-trays in 7+1 redundancy accessible from the rear. There are two 3000W CRPS PSU slots accessible from the rear.



Figure 6-2: Minipack3 Chassis Rear View



Figure 6-3: Minipack3 Chassis Exploded View

6.4.1. Rack Compatibility

Minipack3 can be mounted in the following racks with corresponding rack mount kit

- EIA 19" rack:
 - At 4RU spacing using ORv3N rail kits
 - At 4.25RU spacing using Minipack2 rail kits with Minipack air baffles in between
- ORv3N rack:
 - At 4RU spacing using ORv3N rail kits
 - At 4.25RU spacing using Minipack2 rail kits with Minipack air baffles in between
- ORv3 rack:
 - At 4OU spacing using Minipack2 outer chassis with inner rail kits

6.4.2. General Requirements

N/A

6.5. Electrical Requirements

The system shall operate at either redundant AC power inputs or single DC power input. The power line shall have 3,000W power capacity to the system at the specified operating ranges.

The system max power consumption at the power line is 2,100W at Meta's typical operating conditions.

The universal AC line input voltage in the range 90VAC to 305VAC shall be supported. The input frequency in the range 47Hz to 63Hz shall be supported. Full load operation shall be supported with high line input (Nominal 208V and above).

The DC line input voltage range is 45 - 53 Vdc at the steady state, and 41 - 57 Vdc at transient conditions less than 2 ms.

6.6. Thermal Design Requirements

The thermal design of Minipack3 is optimized to support a 51.2T-generation switch ASIC and OSFP 128x400G-FR4 optics (up to 16 W per OSFP) in a 2x1 stacked configuration with a maximum case temperature limit of 70°C. It is also backward compatible with OSFP 200G-FR4 and 100G-FR4 optics.

The maximum ambient temperature is 35°C. The highest altitude condition is 6000 ft. Airflow is directed from the front to the rear of the chassis, driven by 8x (80mm x 80mm x 86mm) fans at the rear of the chassis with N+1 redundancy. The BMC monitors the thermal condition of the system based on readings from key temperature sensors, including system inlet ambient, switch ASIC on-die, CPU, and optics. The fan speed is controlled by a combined algorithm of a step function based on system inlet ambient temperature and PID controllers for critical components, including the switch ASIC on-die, CPU, and optics. The system fan speed control should also support indefinite service time for one fan tray or one PSU.

The system airflow should not exceed 0.145 CFM/W at sea level and 0.181 CFM/W (total system airflow/total system power) at an altitude of 6000 ft when the system is fully populated with any of the supported optics (and at maximum traffic). The system is designed to consume the minimum airflow necessary to maintain all components below specified operating temperature limits.

The acoustic requirements are listed in the following table.

Network Equipment

	OHSA (Required)	Directive 2003/10/EC (Goal)	FB Design Goal	Remarks
Sound Limit (dBA)	85	80	78	Under normal operation at 25 °C, the system must not produce a A-weighted sound power level above the required limit. The FB design goal should be targeted during development of the product. The Directive goal represents the limit that requires hearing protection to be provided to our Data Center Staff in Europe. The ODM must provide the result of the formal testing.

6.7. Interfaces

6.7.1. AC Power Connector

The system shall provide AC power cords that connect to C20 AC power connectors for Meta data center operations. The power cables shall have a latch mechanism to prevent loose power connections.

6.7.2. DC Power Connector

The system shall provide DC power cords that connect to Meta ORv3N rack busbars. The system shall optionally provide DC power cords that connect to Meta ORv3 rack busbars. The power cables shall have a latch mechanism to prevent loose power connections.

6.7.3. OSFP User Ports

The system shall have 64x OSFP user ports that are compliant to OSFP MSA specifications. Each OSFP port shall support 16W power consumption. Optionally half of the user ports should support 26W power consumption per port, with the remaining user ports supporting 16W each.

The OSFP user ports shall be OIF CEI-112G-VSR-PAM4 compliant to support Meta 2x400G optics modules. The OSFP user ports should also support up to 3.0m/26awg DAC cables.

Lattice Semi MachXO3 and ECP5 FPGA devices are used as the OSFP low speed signal host controller to interface with OSFP 3-state present/lpmode and interrupt/reset signals directly.

Each OSFP user port shall have two tri-color LEDs for two of its sub-ports when using Meta's 2x400G optics modules.

6.7.4. QSFP28 Ethernet Management Port

The system shall have one QSFP28 Ethernet management port connected to the switch ASIC management port. The port shall support either 100GbE-CR4 or 50GbE-CR2. When 50GbE-CR2 is supported, lane 1 and lane 2 will be active, while lane 3 and lane 4 are unused.

With a QSFP28-to-SFP+ adaptor, the QSFP28 Ethernet management port should support 10GE SFP+.

The QSFP28 port shall have one tri-color LED for its status.

6.7.5. RJ45 Ethernet Management Port

The system shall have one RJ45 Ethernet management port for 1000Base-T applications. The connector shall support CAT6/6A copper cable. The connector shall have two LEDs for link status indication.

6.7.6. RJ45 Console Port

The system shall have one RJ45 console port for RS232 applications at 9600 baud rate. The connector shall have the following pinout definition.

Pin Number	Pin Name
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS

6.7.7. USB Management Port

The system shall have a USB 3.0 type-A connector. An OCP debug card can be plugged into the system USB 3.0 connector for debugging purposes. This connector shall support three debugging functions: a USB 2.0 High Speed interface, a debug UART interface and a debug I2C interface. Its pinout is defined in the following table.

Pin Number	Pin Name	Note
1	VBUS	
2	USB 2.0 DP	
3	USB 2.0 DN	
4	GND	
5	I2C_SCL, 3.3V	
6	I2C_SDA, 3.3V	
7	debug_card_present	Active high to indicate OCB debug card is present to enable debug UART buffer.
8	UART_RX, 3.3V	from remote to the system
9	UART_TX, 3.3V	from the system to remote

6.7.8. System LEDs

Besides the OSFP user port and QSFP28 LEDs, the system has several management LEDs.

- SMB Status LED on SMB sub-chassis panel
 - A tri-color LED for SMB sub-chassis status
- SCM Status LED on SCM panel
 - A tri-color LED for SCM status
- SYS LED on SCM panel
 - A tri-color LED for the whole system
- SMB LED on SCM panel
 - A tri-color LED for SMB status
- PWR LED on SCM panel
 - A tri-color LED for PSU status
- FAN LED on SCM panel

- A tri-color LED for fan tray status
- PSU LED on PSU
 - A blue/amber bi-color LED for PSU status
- Fan LED on fan tray
 - A blue/amber bi-color LED for fan tray status

6.8. Onboard Power System

The system onboard power design shall meet the system operating requirements. It needs to have enough power capacity and also meets the devices power-up/down sequence requirements.

6.9. Prescribed Materials

N/A

6.10. System Firmware

System firmwares is critical to system functions. A corrupted firmware could cause the system to fail. The Minipack3 system requires that all the BIOS, FPGA and CPLD FW images shall support in-field upgrade.

After the firmware programming, the system requires a cold power cycle to make the new firmwares effective.

6.11. Hardware Management

Minipack3 implements BMC-lite management architecture. The BMC manages the most critical platform management tasks, such as power-on control, fail recovery and system event logging. The x86 microserver takes care of the other tasks such as VRM control, sensors management, fan speed control algorithm, FW programming, etc.

6.12. Compliance

N/A

6.13. Security

The Minipack3 switch is capable of a security mechanism that is supported by the Intel Ice Lake-D processor, which can be extended and be used as the root of the trust mechanism / chain, as well as attestation.

On the BMC side, the BMC CPU is also capable of secure boot / verified boot mechanism by enabling this mechanism at u-boot, and using the locked bootloader partition in one of the BMC SPI flash chips.

6.14. Software Support (*Strongly recommended*)

Meta is running FBOSS SW (open-sourced) along with FBOSS platform services (also open-sourced) on Minipack3 X86 CPU. On the BMC side, BMC image for Minipack3 (open-sourced) can be used; which supports all standard features that other Meta switch systems support. Note that Minipack3 uses the new “BMC-Lite” architecture, where most of the platform management features have been moved from BMC to x86 CPU, with the help of platform controllers (FPGAs and CPLDs.) Anyone that wants to develop SW stack on Minipack3 is strongly recommended to start with the open-sourced FBOSS Software stack and Meta OpenBMC software source tree.

6.15. Arm SystemReady (only for Arm-based Systems) Requirement

N/A

6.16. References (recommended)

N/A

7. Design Specifications

7.1. Repository Information

7.2. Environmental Regulatory Compliance and Requirements

7.3. Physical Specifications

7.4. Mechanical

7.4.1. Rack Compatibility

7.4.2. General Requirements

7.5. Electrical Requirements

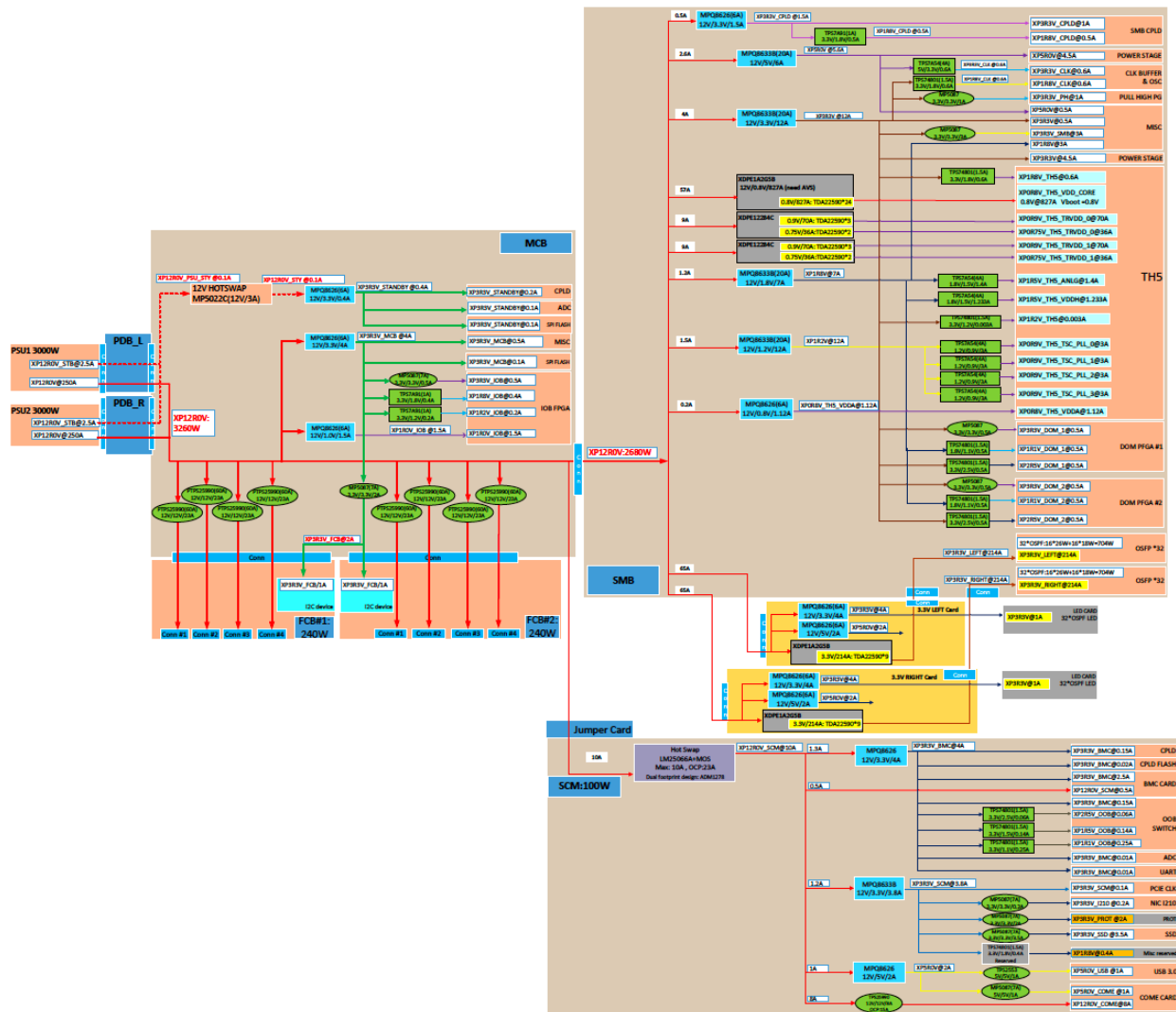
7.6. Thermal Design Requirements

7.7. Interfaces

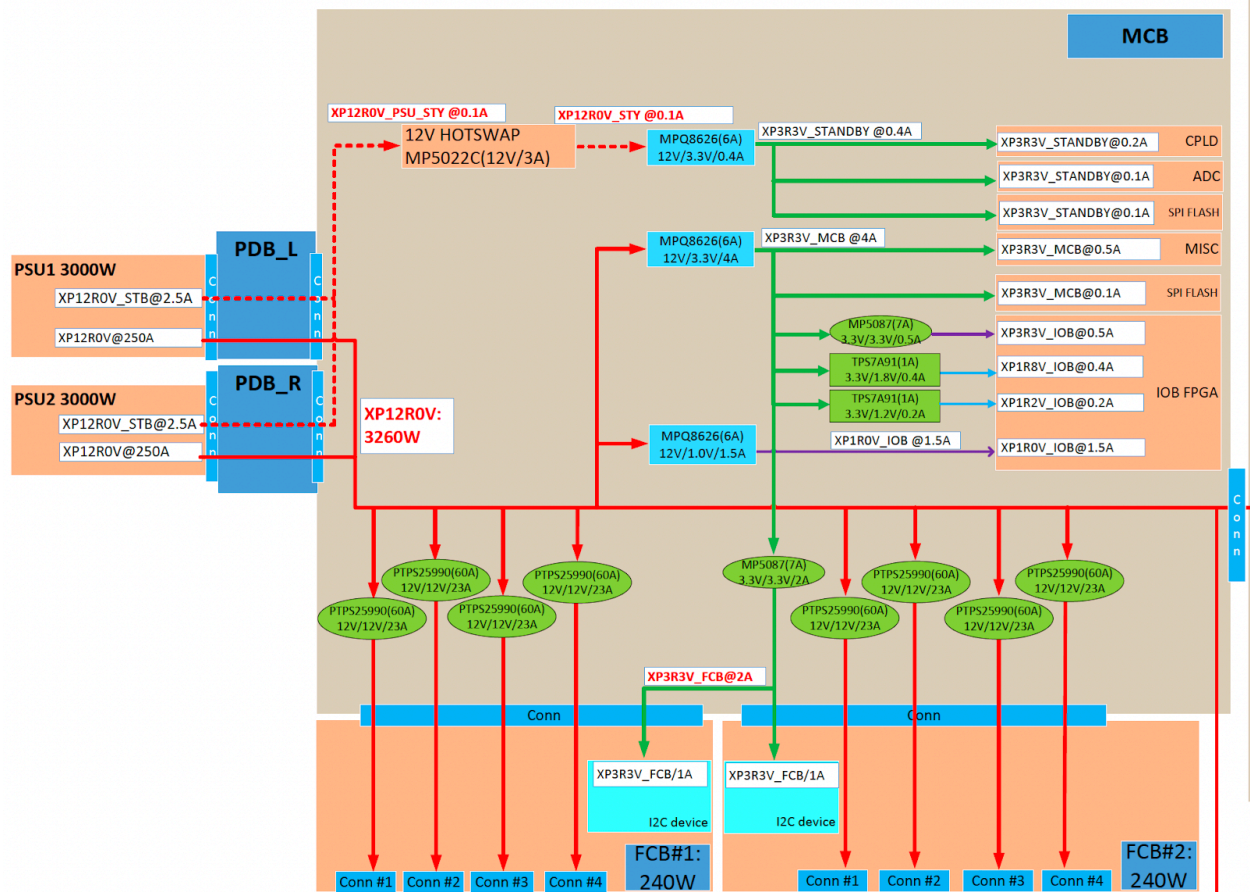
7.7.1. Signal List

7.8. Onboard Power System

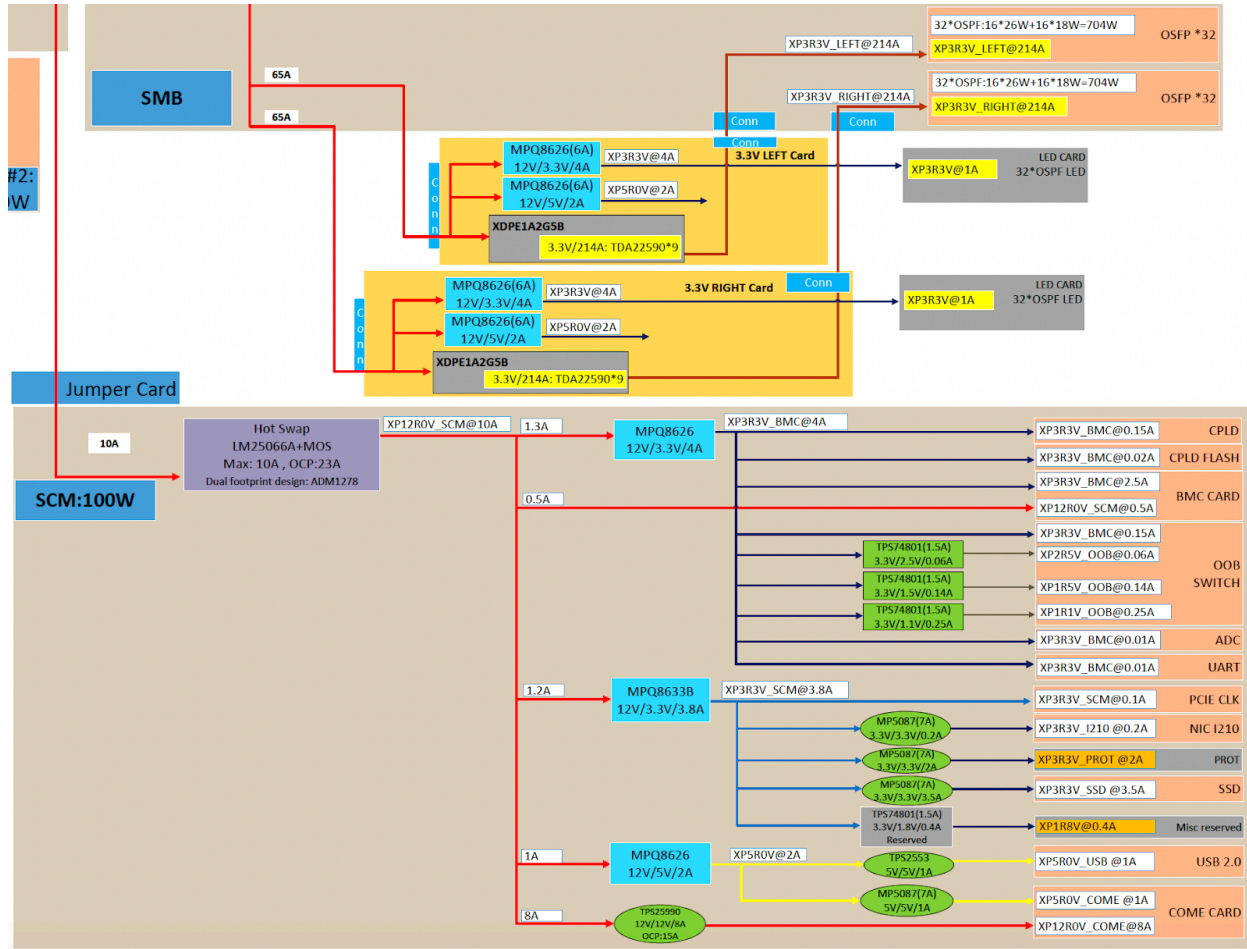
The following diagram illustrates the Minipack3 system power tree.



MCB (Main Carrier Board) Power Tree is shown below



SCM (Supervisor Control Module) and LED boards power tree is shown below:



7.9. Prescribed Materials

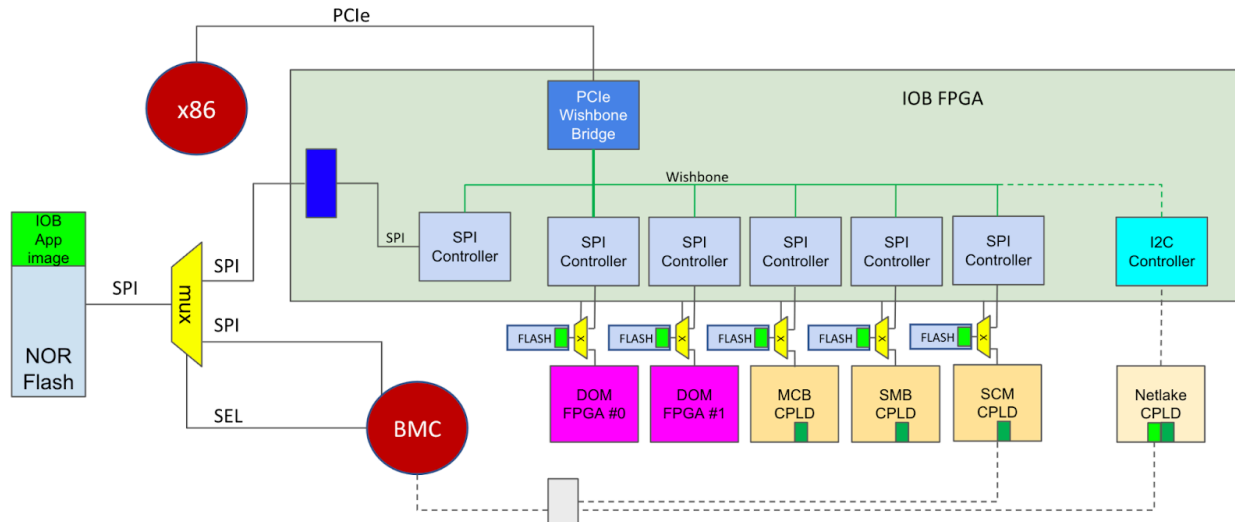
7.10. System Firmware

Minipack3 has the following FW items that can be in-field upgraded.

- BIOS
- MCB CPLD
 - Manage system power on/off sequence, and fan tray management.
- SCM CPLD
 - Manage power on/off sequence, reset controls, UART selection etc management on the SCM.
- SMB CPLD

- Manage power on/off sequence, reset controls, OSFP present/interrupt status management on the SMB.
- IOB FPGA
 - IO bridge FPGA to translate PCIe commands to peripheral bus protocols, such as I2C, SPI and SLPC.
- DOM FPGA
 - FPGA to translate SLPC commands to I2C protocols for optics module management.

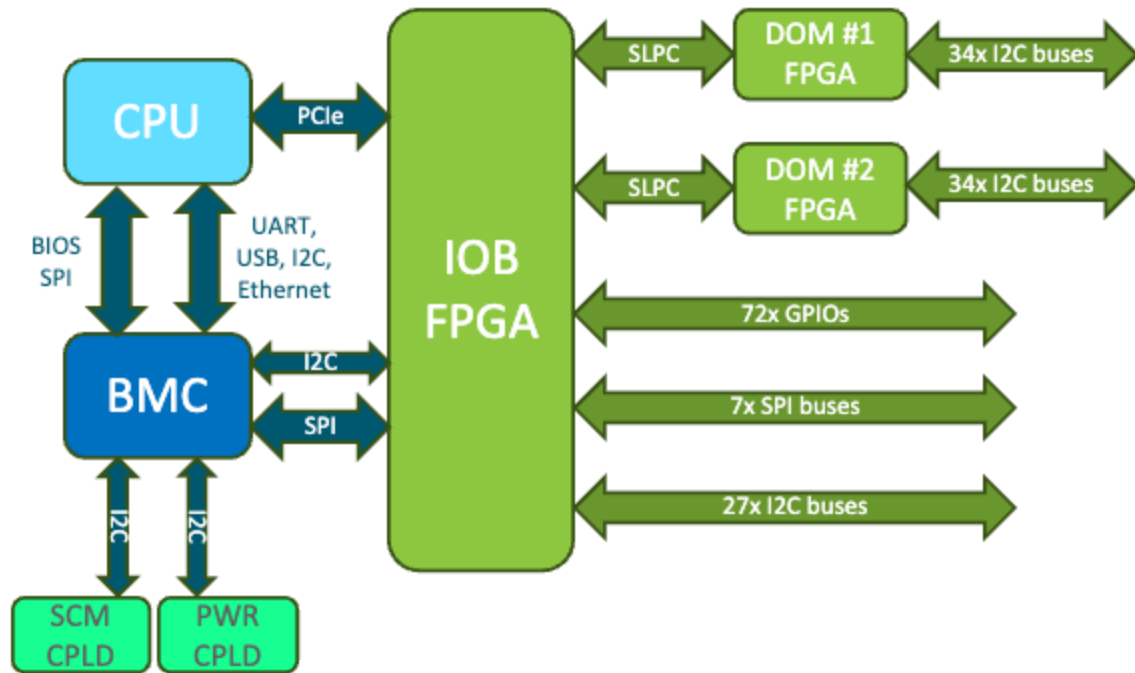
All these firmwares are stored in Flash devices. All the CPLD devices have golden images that will not be in-field upgraded. Only the application images stored in the external SPI Flash devices can be in-field upgraded. They all can be upgraded by x86 CPU. BIOS and IOB FPGA can be in-field upgraded by BMC too.



7.11. Hardware Management

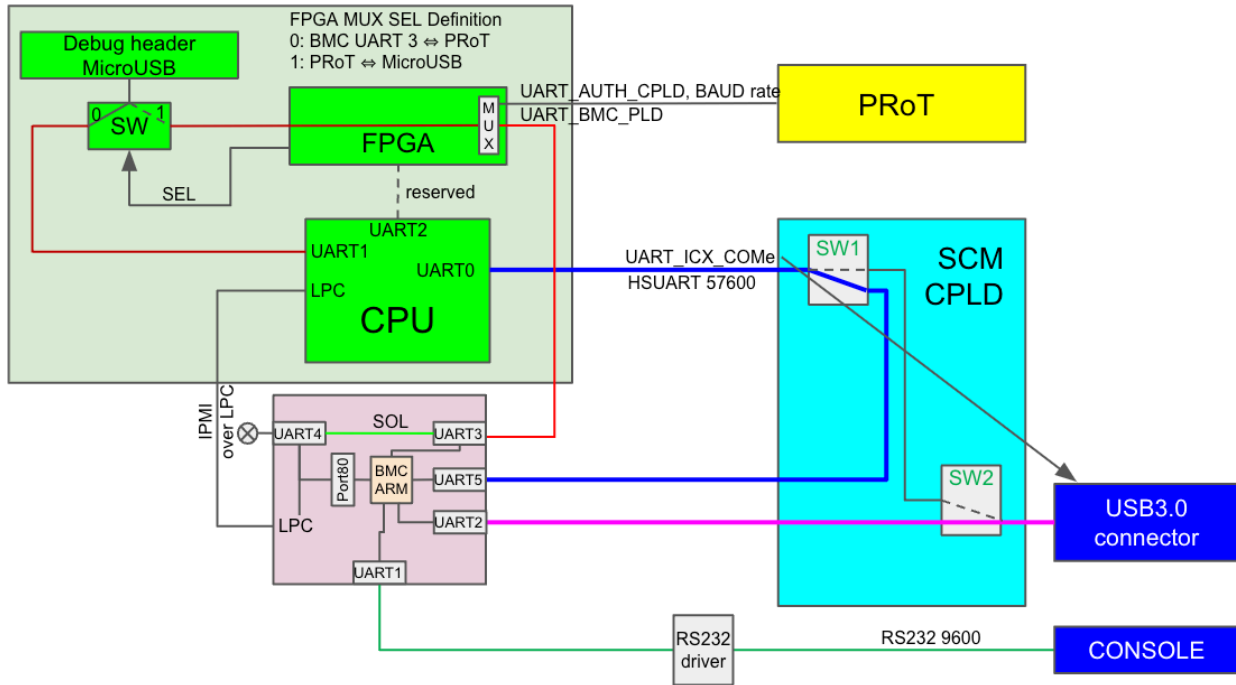
Under the BMC-lite architecture on Minipack3, the following logic devices in the system assist BMC and CPU to execute the platform management tasks:

- IOB FPGA from AMD Artix7,
- two DOM FPGA from Lattice Semi ECP5,
- CPLDs from Lattice Semi MachXO3



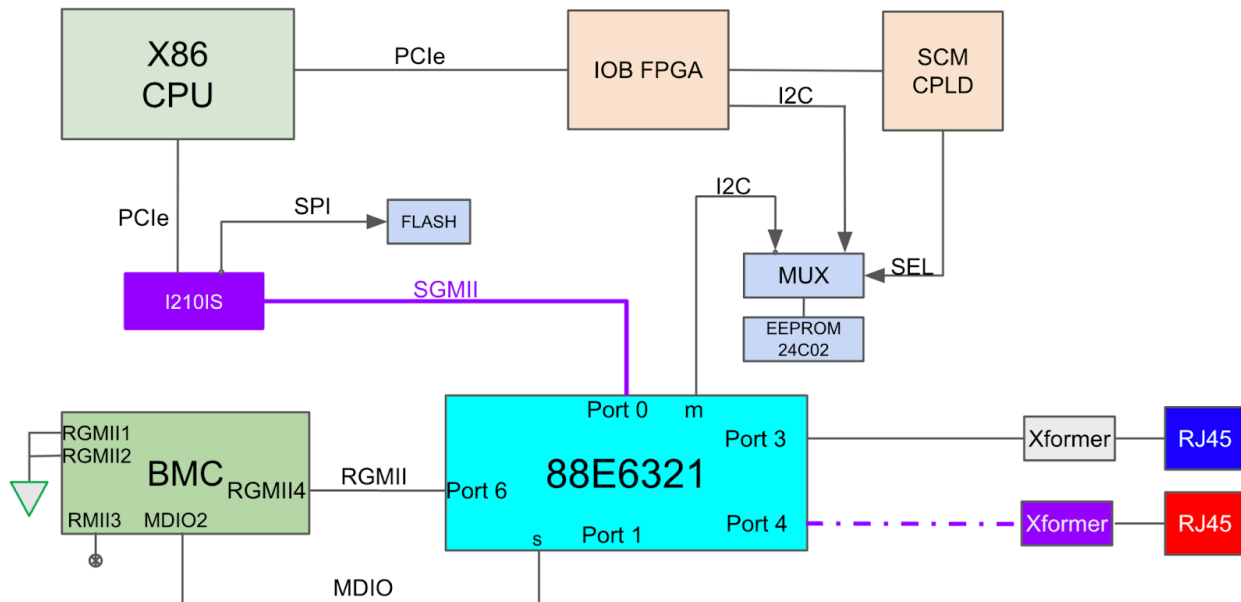
UART

The system has one RS232 port connected to the BMC directly. CPU UART0 connects to BMC UART5 through the SCM CPLD for SOL application. The system also has one UART port connected to the SCM CPLD. The SCM CPLD can switch between CPU UART0 and BMC UART2 for debugging purposes at the UART port. The UART connections are illustrated in the following diagram.

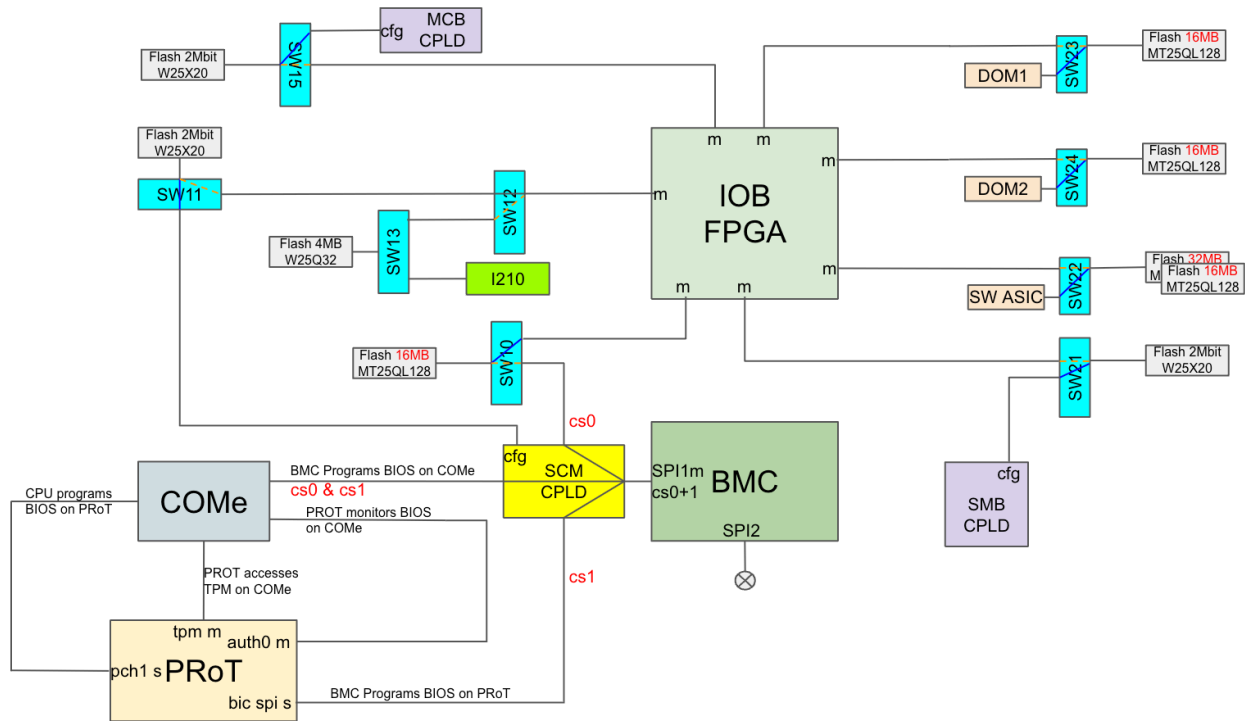


OoB Ethernet

The system has one OoB management accessible through the 1000Base-T RJ45 port. As shown in the following diagram, the 1000Base-T RJ45 in blue is connected to the OoB GbE switch. The RJ45 in red is reserved in the existing design. The switch has one RGMII port connected to the BMC, and one SGMII port connected to the CPU through I210S.



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Sensors

There are a lot of sensors in the system to monitor the system health status. They are divided into three major categories: VRM sensors, temperature sensors and voltage sensors. Fan control algorithm running on the CPU monitors the temperature sensors all the time to adjust the fan speed in the system. VRM sensors and voltage sensors are being monitored to help the field support team in troubleshooting. Most of these sensors are connected to the FPGA and the CPLD devices directly.

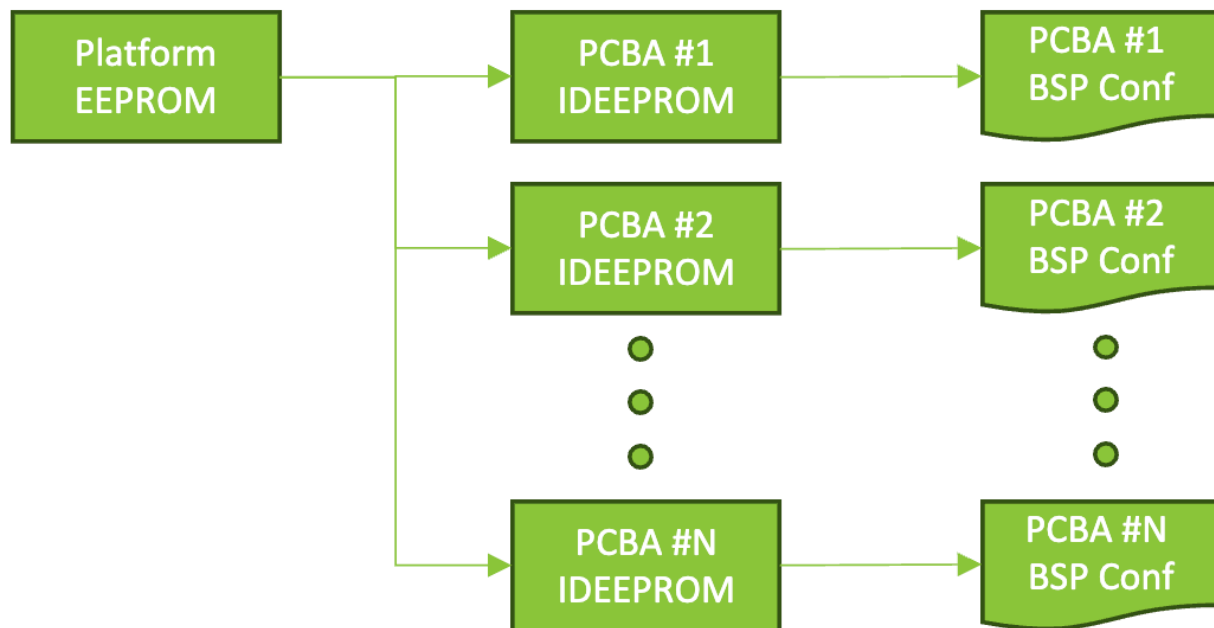
Fan PWM and RPM

There are eight fan trays in the system. Four of them are connected to FCB-T on the top, and the other four are connected to FCB-B on the bottom.

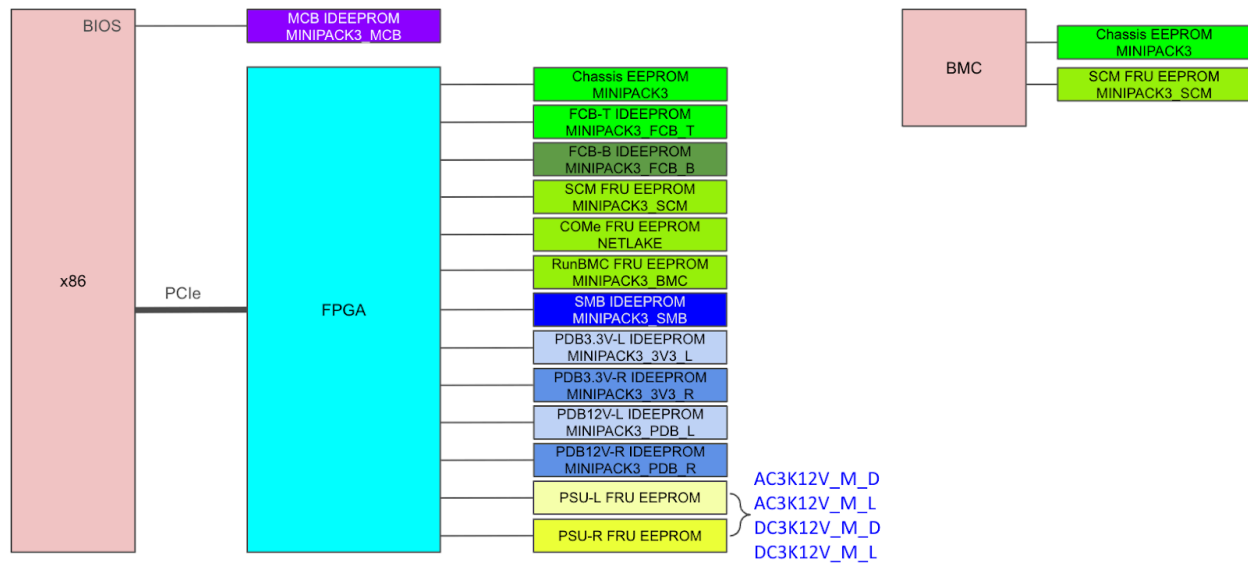
Fans are managed through a virtual fan CPLD in the physical MCB CPLD. The fan PWM frequency is around 25KHz. The fan RPM is monitored by fan CPLD and reported to the microserver through CPLD registers. If the fan RPM is too low, fan CPLD will report a warning in its register and drive the fan LED to amber.

Platform Management

To mitigate the supply chain risk, Minipack3 has enabled multi-source parts in the hardware design. Although these multi-source parts are interchangeable from the hardware perspective, their drivers sometimes are not compatible with each other. To allow the software to automatically load the proper drivers, the system incorporates an IDEEPROM for each PCBA that requires drivers. The IDEEPROM contents define the driver information for each PCBA. The location and the address of the IDEEPROM are indexed in the platform EEPROM. FBOSS reads the platform EEPROM to create a map to access the IDEEPROMs in the system to retrieve the BSP driver information, and load the drivers accordingly. This mechanism is named as Platform Manager at Meta FBOSS.



The following diagram shows all the EEPROMs used in Minipack3 to self-identify the driver types in the system.



LEDs

Each OSFP port have two tri-color LEDs. The LED data streams are driven by the two DOM FGAs, and decoded by a simple serial-to-parallel shift register array to light all the LEDs.

SMB FRU LED is a tri-color LED driven by the MCB CPLD.

QSFP28 port 65 LED is a tri-color LED driven by DOM FPGA.

SCM FRU LED, SYS, PWR, SMB fan FAN LEDs on SCM are driven by SCM CPLD.

Fantray LEDs are driven by MCB CPLD through a simple serial-to-parallel shift register array. PSU LEDs are driven by PSU MCU.

7.12. Compliance

7.13. Security

7.14. Software Support (*Strongly recommended*)

7.15. Arm SystemReady (only for Arm-based Systems) Requirement

7.16. References (recommended)

8. Product Specifications

8.1. Repository Information

8.2. Environmental Regulatory Compliance and Requirements

8.3. Physical Specifications

8.4. Mechanical

8.4.1. Rack Compatibility

8.4.2. General Requirements

Chassis dimensions: 4RU

- 176.2mm(H) x 440.4mm(W) x 661mm (D)
- 76mm (~3") shorter than Minipack2 chassis
- Rear adapter bracket to engage with rail kits (56.6mm deep)

Weight: Fully loaded chassis with all FRUs: 46.7kg (103 lbs)

- Main chassis: 19 kg (42 lbs)
- SMB sub-chassis: 17 kg (37.5 lbs)
- 1 SCM module, reside inside SMB sub-chassis: 1.4 kg (3 lbs)
- 8 fan modules, reside inside main chassis: 0.83 kg (1.83 lb) each
- 2 AC/DC PSUs, reside inside main chassis: 1.3 kg (2.9 lbs) each

Handles: Four handles on top of the chassis

- SMB Sub-chassis:
- FRU-able from front side (not hot swappable)
- Two (2) ejector handles for ejection and injection
- Stop feature for operation safety
- Hosts the Switch Control Module (SCM)

- 8.5. Electrical Requirements**
- 8.6. Thermal Design Requirements**
- 8.7. Interfaces**
 - 8.7.1. Signal List**
- 8.8. Onboard Power System**
- 8.9. Prescribed Materials**
- 8.10. System Firmware**
- 8.11. Hardware Management**
- 8.12. Compliance**
- 8.13. Security**
- 8.14. Software Support (*Strongly* recommended)**
- 8.15. Arm SystemReady (only for Arm-based Systems) Requirement**
- 8.16. References (recommended)**

Appendix A - Checklist for Steering Committee (SC) approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes	If no, please state the reason.
Was it approved in the OCP Contribution Portal?	Yes	If no, please state the reason.
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	List Supplier Name(s)
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	If more time is required, please state the timeline and reason for extension request. Please have each Supplier fill out Appendix B.

Appendix B-__ Meta Platforms, Inc. - OCP Supplier Information and Hardware Product Recognition Checklist

Company: **Meta Platforms, Inc**
Contact Info: **Rongchun Zhou**

Product Name: **Minipack3**
Product SKU#:
Link to Product Landing Page:

The following is needed for OCP hardware product recognition:

For OCP Inspired™

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Declare product is 100% compliant with specification
- Complete the [OCP Inspired™ Product Recognition Checklist](#), which includes hardware management conformance checks and security profile.

For OCP Accepted™

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Complete the [OCP Accepted™ Product Recognition Checklist](#), which includes hardware management conformance checks, security profile and open system firmware conformance checks.
- Submit a design package meeting [OCP Hardware Design Guideline Contribution Checklist](#) (if not already submitted by the contributor). If already submitted, declare the product is 100% compliant with the design package.
- Submit a firmware package including a firmware image, build scripts, documentation, test results and a tool that verifies modifications
- Submit the BMC source code, if applicable to product type

Please complete the OCP Inspired™ Product Recognition Submission Checklist or OCP Accepted™ Product Recognition Checklist and the following table.

Item	Details	Links
Which product recognition?	OCP Accepted™	Provide link for the appropriate Product Checklist
If OCP Accepted™, who provided the Design Package?		Link to OCP Contribution Database
Where can a potential adopter purchase the product?		Link to OCP Marketplace

Appendix C - Contribution Process FAQs

As a contributor to a hardware specification, here are some questions that often come up.

Q1. What are acceptable types of hardware specification am I able to contribute to OCP? Is it any of the below?

- a. base, design or product specification for a de-facto standard (new standard with no hardware product on the horizon)
- b. base, design or product specification for an intended physical <hardware product type> (product may be coming but within the next 12-15 months for base and design specification, with a product specification with design files resulting in a product in 3-6 months)
- c. modification of an existing specification (state which existing spec is being modified)
 - i. either a complete revision update or
 - ii. a minor version update
 - iii. Note: errata does not require a specification update. Only an errata statement.
- d. an architectural specification for <product types> that may incorporate several/multiple specifications, types, standards and other components into a logical system for given purposes.
 - i. this may include a/specification(s) that strictly conforms to an architectural specification
 - ii. this may include a/specification(s) that is/are standalone or conforms to an architectural specification
- e. A Base, Design and Product Specification in a single document.
- f. *If none of the above, please contact OCP Staff for consultation.*

Q2. How do I know if what I am contributing will be accepted by OCP?

- a. Before contributing any specifications, please contact either OCP Staff (Michael Schill, Rob Coyle or Bijan Nowroozi) or the Project Lead for the Project that best represents your contribution. For example, if you are contributing a Server Specification, please contact one of the Server Project Leads. You can see all the Projects [here](#).
- b. The OCP Foundation, Project Leadership and OCP Community are resources to help you navigate the process.

Q3. What is the contribution process for my hardware spec?

- a. Follow the flow for your spec type [here](#).
- b. This flow is subject to change so please check with the OCP Staff for more information or any questions.

Q4. What if my spec is not developed yet and I want to collaborate with other companies?

- a. Please contact either OCP Staff (Michael Schill, Rob Coyle or Bijan Nowroozi) or the Project Lead for the Project that best represents your contribution.
- b. They will help you find other collaborators and help you with the contribution process for a multi-party contribution.

Q5.I have a question on the Contribution License Agreement.

- a. Please contact OCP Staff and we can help you with questions.

Q6.Do I need to have a product in order to contribute a spec?

- a. Please see Q1. Some types of specs do not require an immediate product. Some do. Please work with the OCP Staff on better direction on your specification type.

Q7.How do I know if someone else is already working on this idea?

- a. Please discuss with the Project Leadership and/or the OCP Foundation staff.

Q8.What other considerations are there?

- a. The OCP Foundation encourages contributors to consult with the Project Leadership and/or the OCP Foundation staff as early as possible in the development cycle. There may be others in the community who are willing and able to help share some of the development effort.
- b. It may be desirable for speed to gather key collaborators and work together outside of public meetings, with a closed CLA. Just be aware of the tradeoffs such as potential collaboration is missed and the idea may not be as strong as it could be with additional eyes on it. Some recommendations are:
 - i. even if the idea is worked on in a closed CLA group, find ways to hold regular public briefings
 - ii. consider opening the CLA group as soon as possible and
 - iii. be open to the possibility of duplication of effort by others whom were not aware and chance this approach will end up fracturing of the potential total market by having subsequent exclusive groups working in parallel