Stack-up and impedance requirements

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Date:	5/19/2015
P/N:	PCB000952
Layers:	18
Total Thickness:	125.93mil
Finish:	Imersion silver

Material:	Panasonic Megtron 6 HVLP
PCB size and PCB units per array	Board: 413 mm x 184 mm 1 unit per array
PCB Utilization (%)	
Gold finger:	No
Back dril depth/width types on CS:	5
Back dril depth/width types on PS:	9

All dimensions are in mils unless otherwise stated

	Copper parameters				Resin parameters				Impedance parameters							
									Differential pairs parameters					SE signal parameters		
										Default		Neck-down				
Layer	**signal/ Power/ GND**	**Copper weight [oz]**	**Copper thickness after plaiting [Mil]**	**Copper roughness**	**Dielectric thickness**	**Material**	**Glass type**	**Resin content [%]**	**Imp. [Ω]**	**Width**	**Space**	**Width**	**Space**	**Imp.[Ω]**	**Default Width**	**Neck-down Width**
Layer 1 - CS	Signal	0.3333	1.8	HTE					90±10%	7.38	4.87			55	8.38	
									95±10%	8.88	9.62					
									95±10%	6.25	4.75					
Prepreg					5.2	Prepreg R5670K 1035(73)/1035(73)	1035	73								
Layer 2	GND	0.5	0.55	HVLP												
Prepreg					8	Core R5775K 8mils 2x3313 .5 oz / .5 oz	2x3313									
Layer 3	Signal	0.5	0.55	HVLP					95±10%	6.13	5.12			55	6.25	
									95±10%	7.88	13.12					
									90±10%	6.65	4.6					
									90±10%	8.6	12.4					
Prepreg					6.4	Prepreg R5670K 1078(68)/1078(68)	1078/1078	68								
Layer 4	GND	0.5	0.55	HVLP												
Prepreg					8	Core R5775K 8mils 2x3313 .5 oz / .5 oz	2x3313									
Layer 5	Signal	0.5	0.55	HVLP					95±10%	6.13	5.12			55	6.25	
									95±10%	7.88	13.12					
									90±10%	6.65	4.6					
									90±10%	8.6	12.4					
Prepreg					6.4	Prepreg R5670K 1078(68)/1078(68)	1078/1078	68								
Layer 6	GND	0.5	0.55	HVLP												
Prepreg					8	Core R5775K 8mils 2x3313 .5 oz / .5 oz	2x3313									
Layer 7	Power	0.5	0.55	HVLP												
Prepreg					6.49	Prepreg R5670K 1078(68)/1078(68)	1078/1078	68								
Layer 8	Power	1	1.15	RTF												
Prepreg					4	Core R5775K 4mils 1x3313 1 oz / 2 oz	1x3313									
Layer 9	Power	2	2.4	RTF												
Prepreg					3.92	Prepreg R5670K 1035(73)/1035(73)	1035	73								
Layer 10	Power	2	2.4	RTF												
Prepreg					4	Core R5775K 4mils 1x3313 1 oz / 2 oz	1x3313									
Layer 11	GND	1	1.15	RTF												
Prepreg					6.22	Prepreg R5670K 1078(68)/1078(68)	1078/1078	68								
Layer 12	Signal	0.5	0.55	HVLP					95±10%	6.13	5.12			55	6.25	
									95±10%	7.88	13.12					
									90±10%	6.65	4.6					
									90±10%	8.6	12.4					
Prepreg					8	Core R5775K 8mils 2x3313 .5 oz / .5 oz	2x3313									
Layer 13	GND	0.5	0.55	HVLP												
Prepreg					6.4	Prepreg R5670K 1078(68)/1078(68)	1078/1078	68								
Layer 14	Signal	0.5	0.55	HVLP					95±10%	6.13	5.12			55	6.25	
									95±10%	7.88	13.12					
									90±10%	6.65	4.6					
									90±10%	8.6	12.4					
Prepreg					8	Core R5775K 8mils 2x3313 .5 oz / .5 oz	2x3313									
Layer 15	GND	0.5	0.55	HVLP												
Prepreg					6.4	Prepreg R5670K 1078(68)/1078(68)	1078/1078	68								
Layer 16	Signal	0.5	0.55	HVLP					95±10%	6.13	5.12			55	6.25	
									95±10%	7.88	13.12					
									90±10%	6.65	4.6					
									90±10%	8.6	12.4					
Prepreg					8	Core R5775K 8mils 2x3313 .5 oz / .5 oz	2x3313									
Layer 17	GND	0.5	0.55	HVLP												
					5.2	Prepreg R5670K 1035(73)/1035(73)	1035	73								
Layer 18 - PS	Signal	0.3333	1.8	HTE					90±10%	7.38	4.87			55	8.38	
									95±10%	8.88	9.62					
									95±10%	6.25	4.75					

If you have any queries please do not hesitate to contact:
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Notes:	
1	The dialectric thickness, line widths and differential space values are nominal values. Minor changes can be done to meet the impedance requirements.(HW desiner approval is a must)
2	Trace widths are nominal finished dimensions.

Revision control:		
Revision	**Date**	**Description**
X1	9/7/2014	First release
X2	12/24/2014	Neck-Down for 90ohm, PCB shoren from 186 mm to 184 mm line width adjustment for ViaSystems - HY Adjusting line width in order to be symmetrical
00	5/19/2015	PCB Tape Out