

Revision History

Rev	Group	Date	Description
X100	G00/G02/G03	Nov, 2018	Initial Release
R100	G00/G02/G03	Dec, 2018	Beta0 Release
R101	G00/G02/G03	Dec27, 2018	Beta1 Release
R200	G00/G02/G03	Jan 27, 2019	Beta2 Release

Variants

Feature	G00	G02	G03
PCB	-0189	-0190	-0190
SoC SKU	D-1577	D-1541	D-1517
Cores	16	8	4
DIMM Slots	4	2	2
EMMC	Yes	No	No
PCIe x16 Side Ex.Slot	V.T.H	Straddle	Straddle
PCIe x8 Side Ex.Slot	V.T.H	Straddle	Straddle

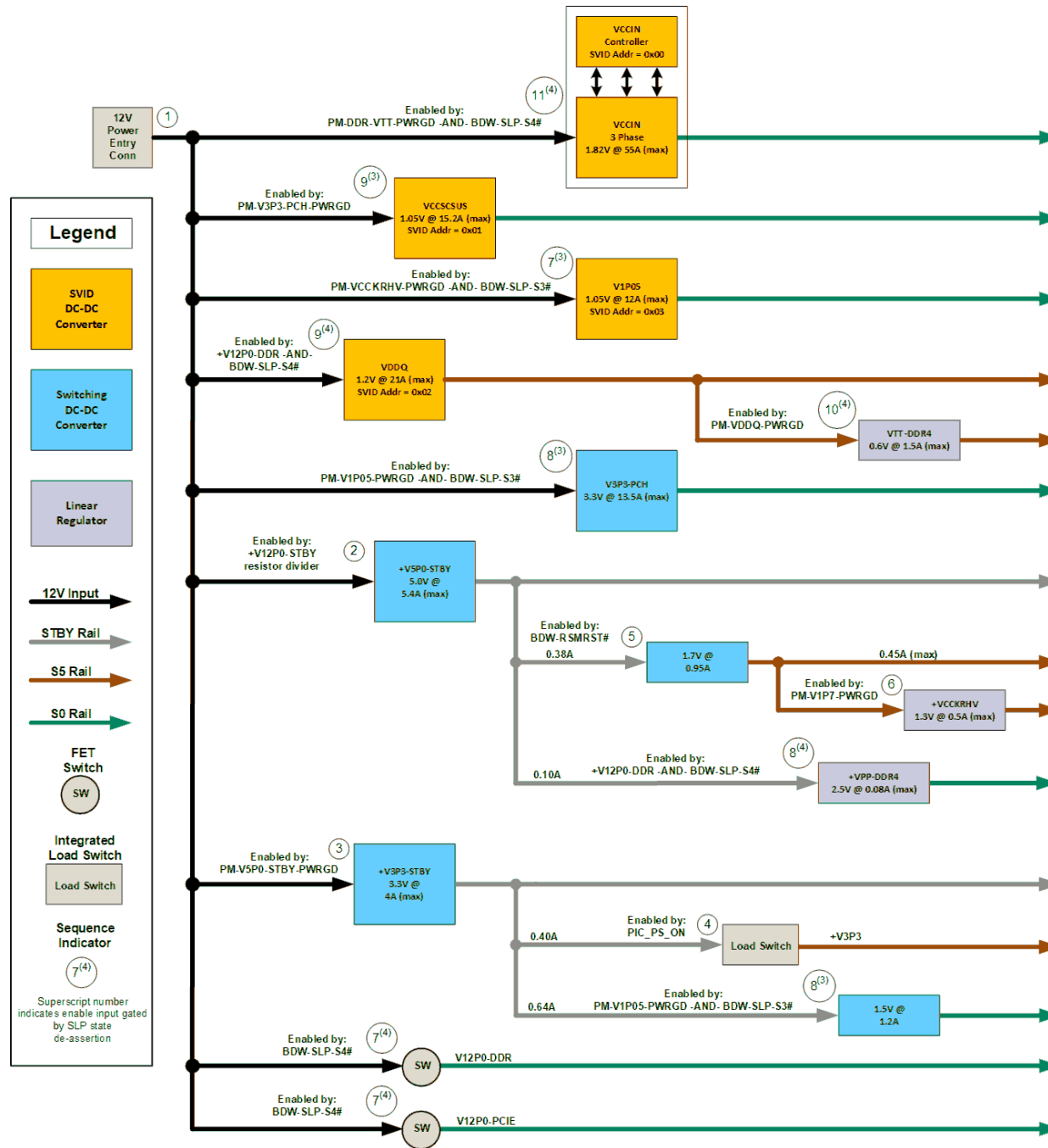
Notes

- * Schematic prepared for two PCB boards in three variants:
PCB1 80204-0189-G00 for Compute Large
PCB2 80204-0190-G02 for Compute Medium
PCB2 80204-0190-G03 for Compute Small
- * Schematic supports V2 and Y0 CPU (none -NS) steppings only
In order support -NS chip, need change layout as following:
 - Remove SHRT1
 - connect U1 pins T40, T42 & V40 to +VCCSCSUS
- * PCB boards difference
 - 0189 Side Expansion Slots True Holes mount
 - 0190 Side Expansion Slots Straddle mount
- * To see variant:
 1. Open View menu
 2. Choose Variant View Mode menu
 3. Choose one of the variants
 4. Press OK

Table of Contents

Sheet Num	Description
01	Revision History and Notes
02	Table of Contents
03	Block Diagram
04	Power Tree Diagram
05	Power Sequencing
06	Clocking Diagram
07	Broadwell DDR Interface
08	Broadwell PCIe Interfaces
09	Broadwell LAN Interfaces
10	Broadwell SATA and USB
11	Broadwell Clocking
12	Broadwell Misc. Interfaces
13	Broadwell Straps and Power Mgmt
14	Broadwell Power
15	Broadwell Grounds
16	Broadwell Decoupling
17	Blank
18	DDR Ch 0, DIMM 0
19	DDR Ch 0, DIMM 1
20	DDR Ch 1, DIMM 0
21	DDR Ch 1, DIMM 0
22	LAN Level Shifters
23	CPU Debug Headers
24	PCH Debug Headers
25	Blank
26	Blank
27	eMMC and USB Controller
28	SATA Connectors
29	M.2 Connectors - SATA
30	mPCIe, M.2 and TPM
31	Blank
32	LEDs
33	Side Expansion Slots
34	Front Panel Interfaces
35	Power Monitor ADC
36	Isolation Buffers
37	Power Sequencing
38	Power Sequencing and Level Shift
39	Thermal and Fan Circuits
40	PIC Controller
41	Mechanical
42	5V and 3.3V STBY Regulators
43	3.3V PCH Regulator
44	VDDQ SVID Regulator
45	VCCIN SVID Controller
46	VCCIN Power Stage Regulators
47	1P05V SVID Regulator
48	VCCSCSUS SVID Regulator
49	Downstream Regulators
50	Power Entry / Downstream Regulators





DRAWING No. : 80504

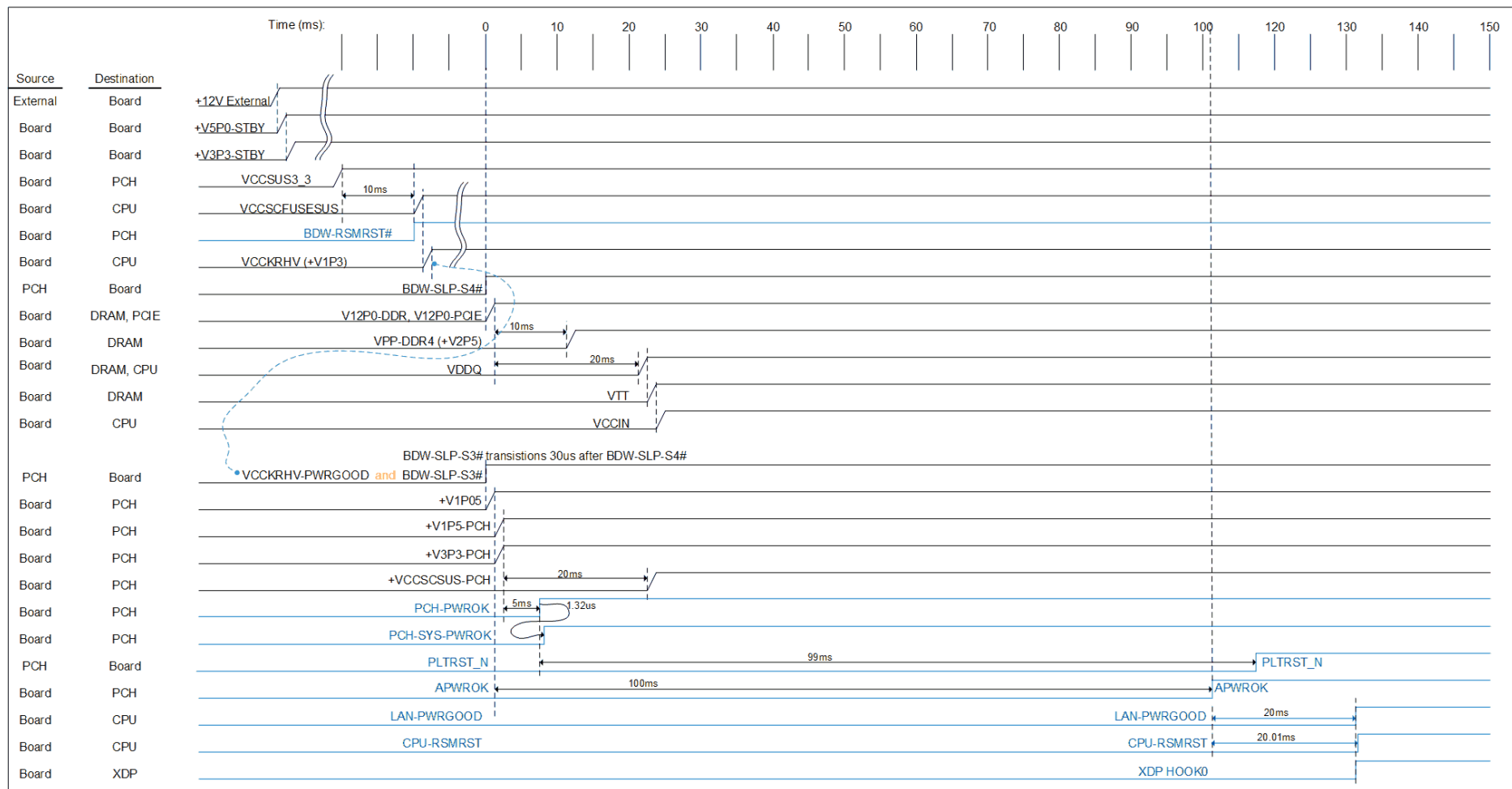
SIZE : Custom REV No. : R200

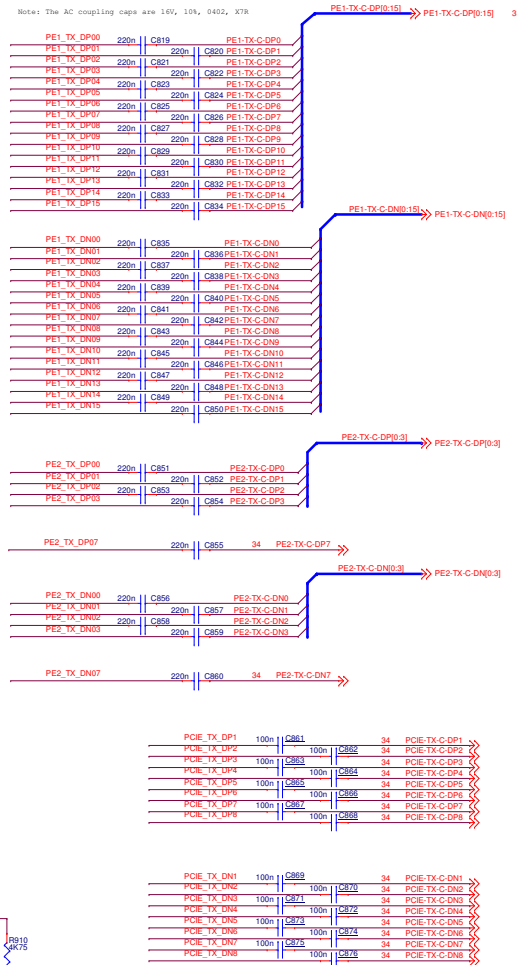
DATE : Sunday, April 07, 2019
Monday, June 11, 2018

Power Tree Diagram
0190M002 Medium
AT&T Compute Board

APPROVALS		
CHECK	NAME	SIGN
APPROV.		
SHEET : 4	of SHEETS : 30	

SILICOM Ltd.
Connectivity Solutions
A Member of RAD Group





DRAWING No. : 80204	
SIZE : Custom	REV No. : R200
DATE : Sunday, April 07, 2019 Saturday, Mar 19, 2018	

PCIe Interface

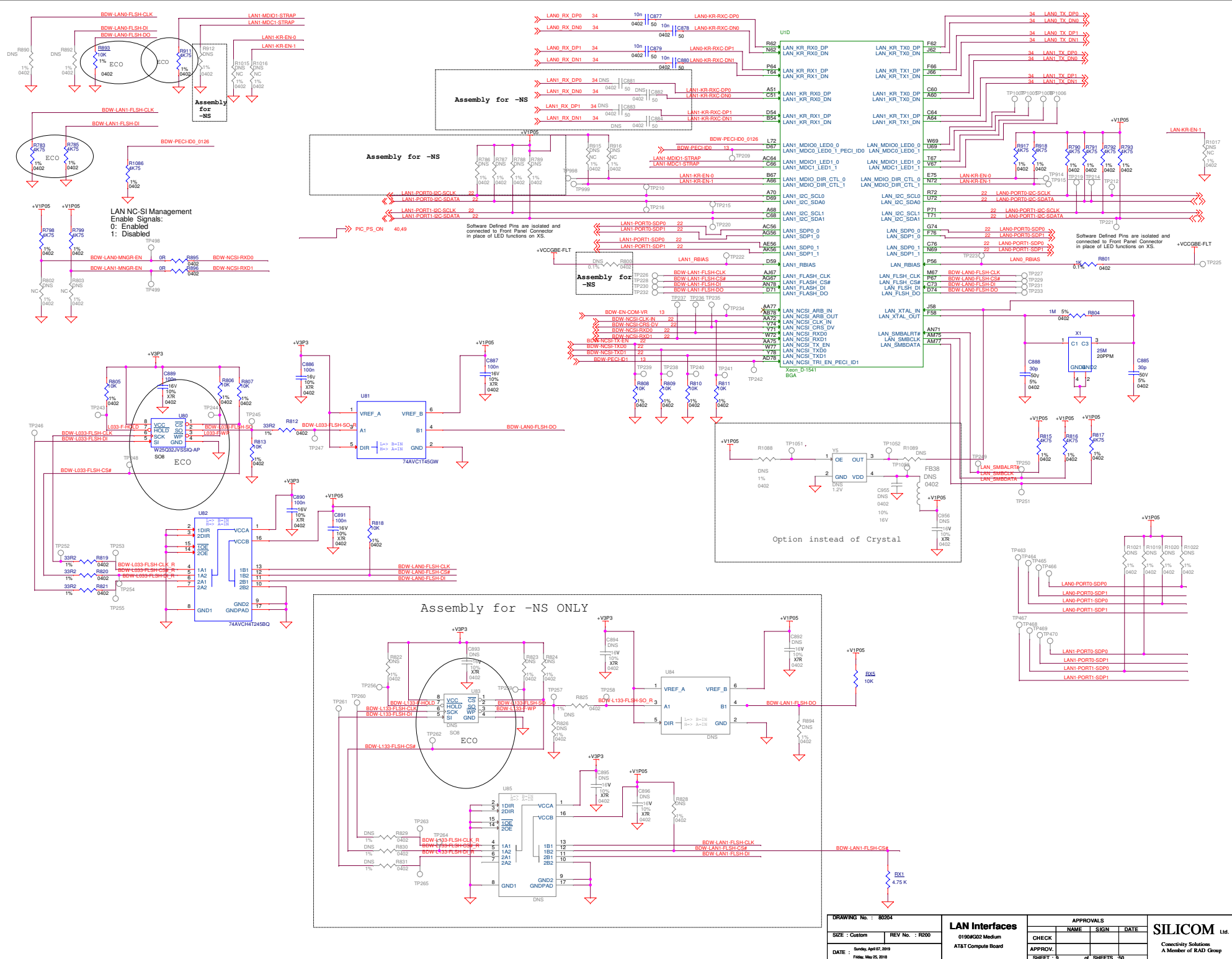
01906G2 Medium

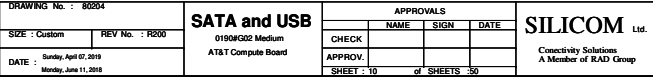
AT&T Compute Board

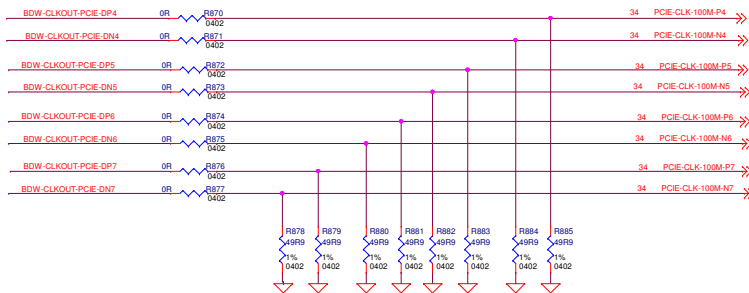
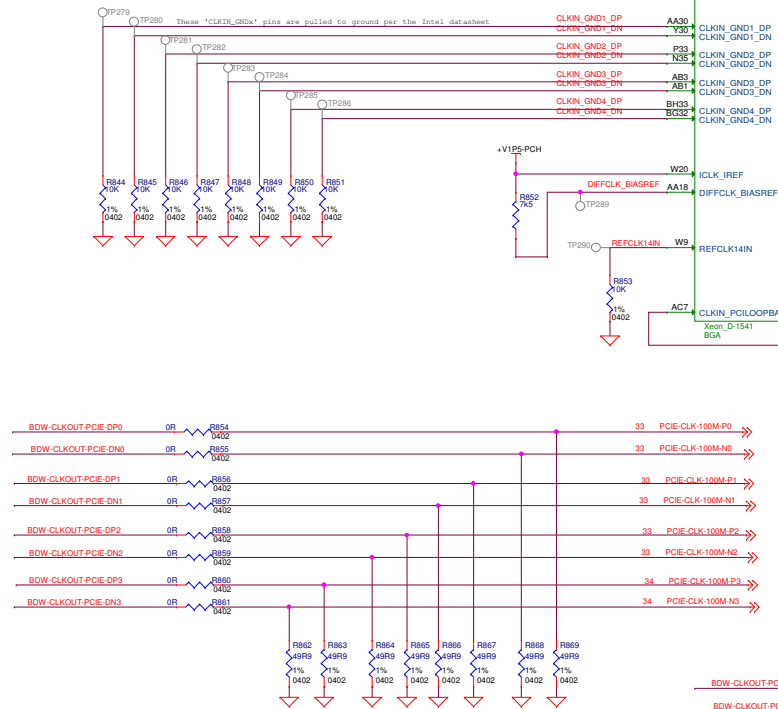
APPROVALS			
	NAME	SIGN	DATE
CHECK			
APPROV.			
SHEET : 1 of 4 SHEETS : 50			

SILICOM Ltd.

Connectivity Solutions
A Member of RAD Group

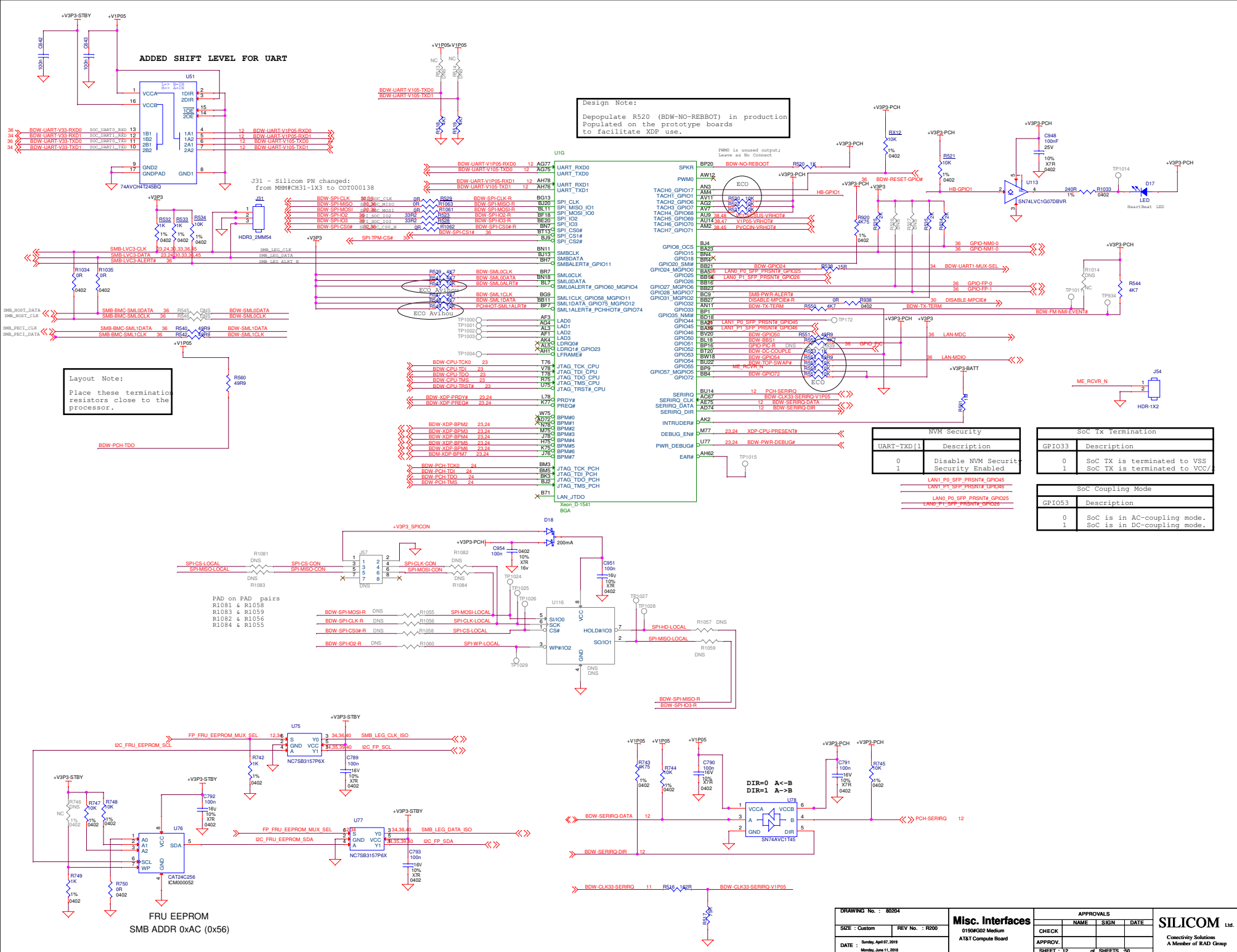


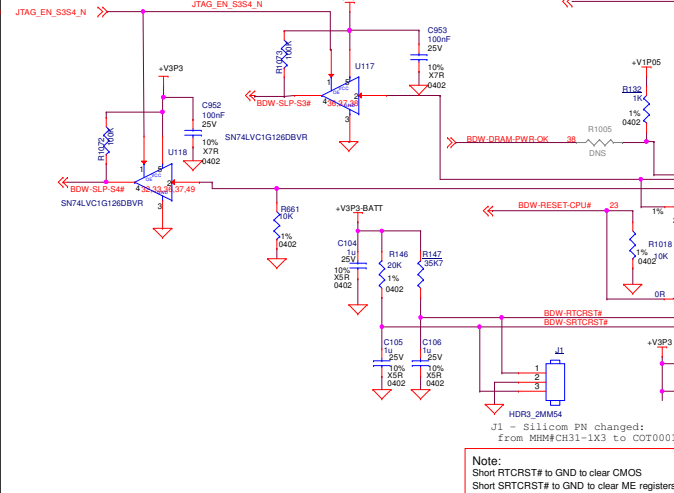




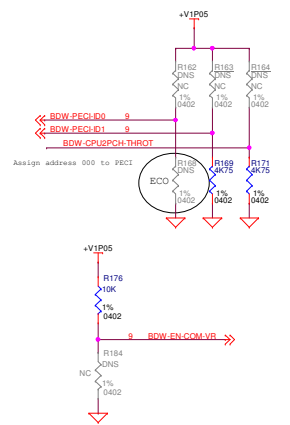
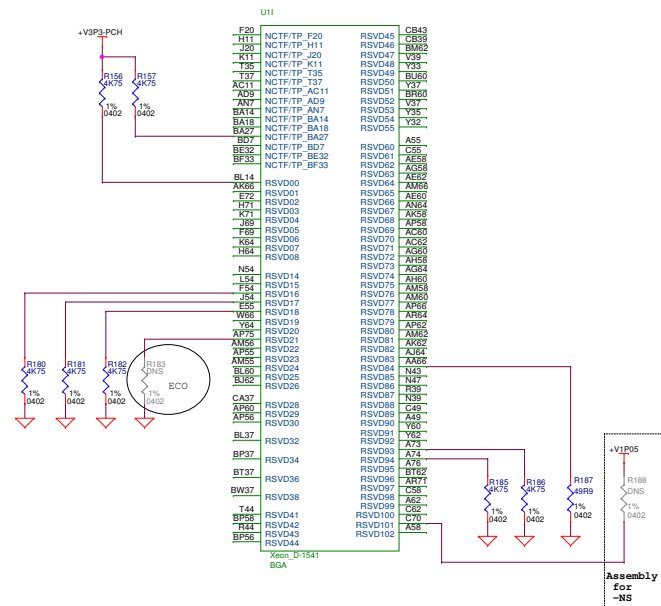
Straddle Mount
Edge Fingers
Straddle Mount
NM1
Management Module
NM1
NM0
NM0

Management Module
NM1
NM0
NM0





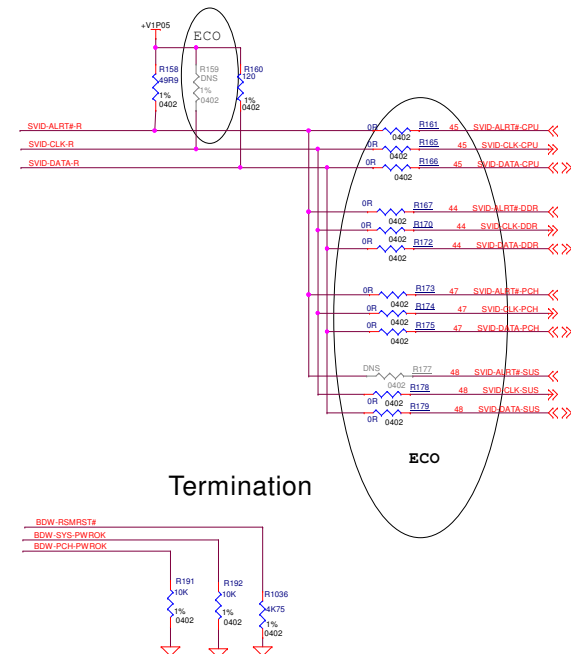
Functional Straps



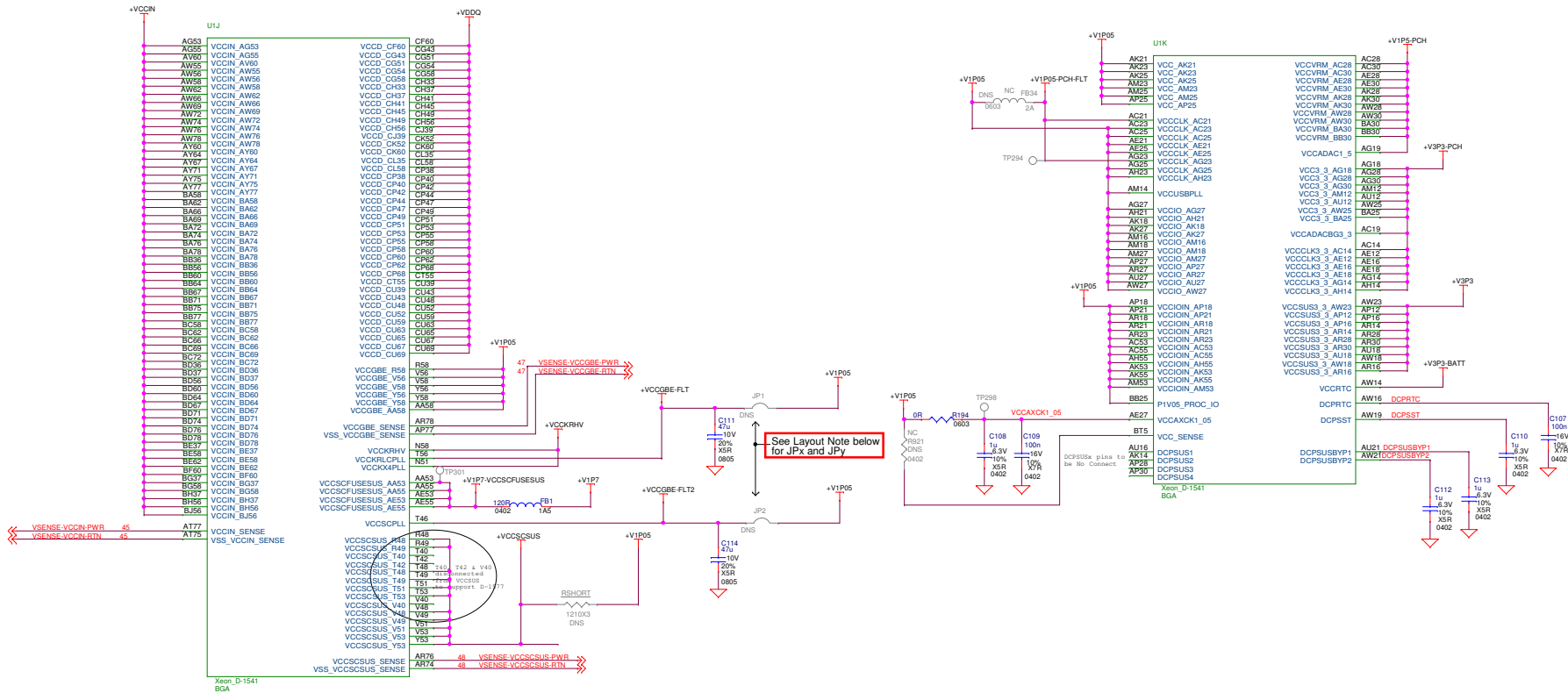
SVID VR Configuration

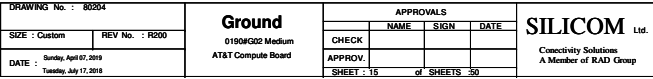
NCSI-ARB-OUT pin BDW-EN-COM-VR net	Description
0	Separate Regulators
1	Combined Regulators: VCCSUS, V1P05-PCH, VCCGBE and VCCIOIN are combined into a single regulator (SVID controlled)

SVID Distribution

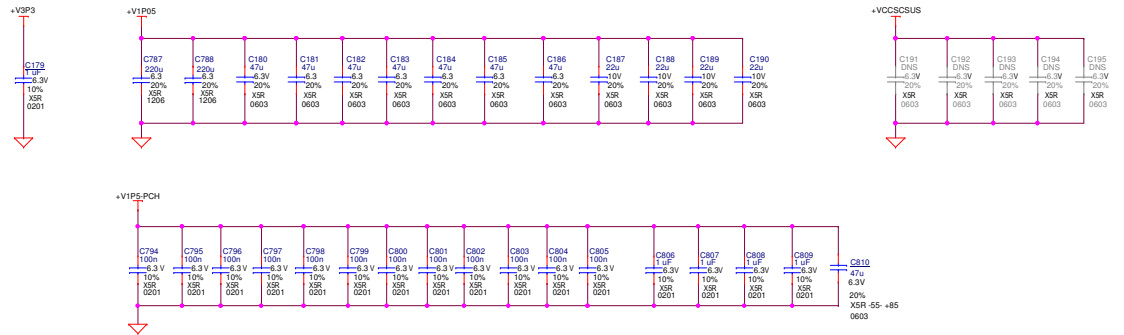


Termination



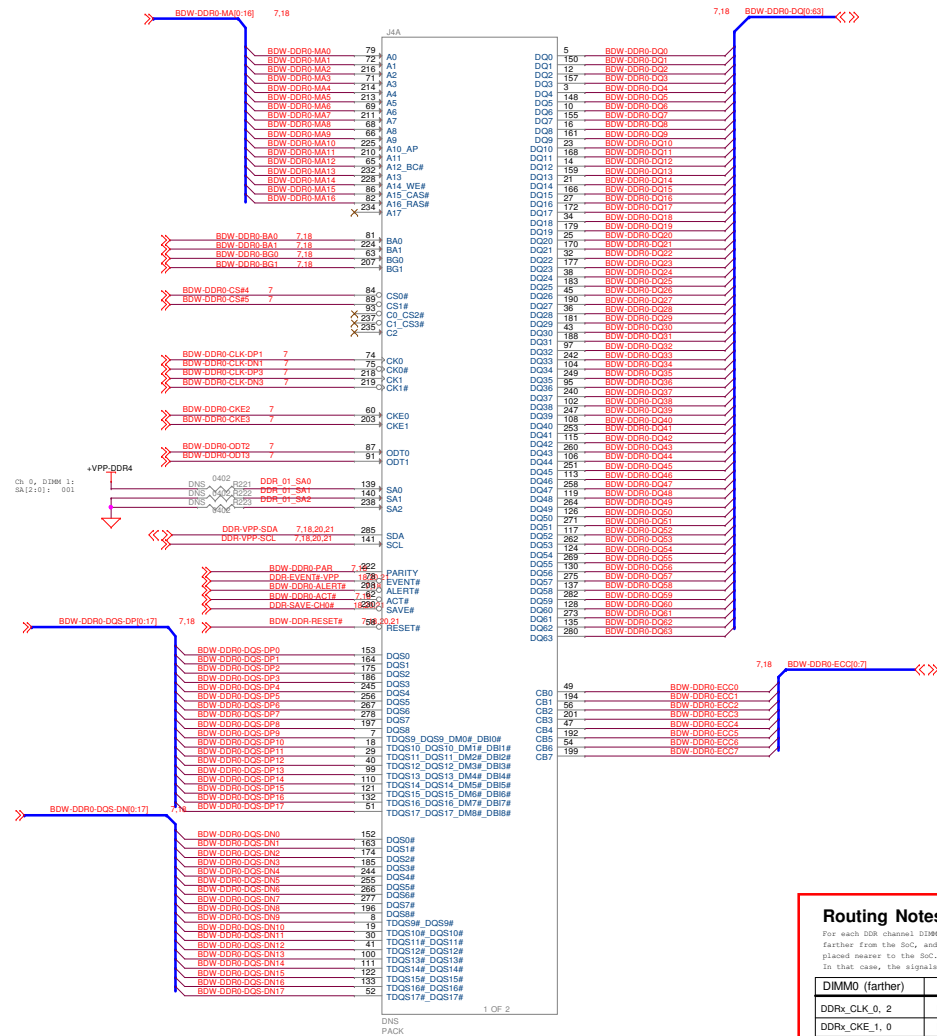


Place the caps in this box in the cavity of the backer plate under the Broadwell-NS SoC



DRAWING No. : 80204		Decoupling 0190G02 Medium AT&T Compute Board	APPROVALS			SILICOM Ltd. Concivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200		NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019			CHECK			
Saturday, May 19, 2018			APPROV.			
			SHEET : 16	of SHEETS : 50		

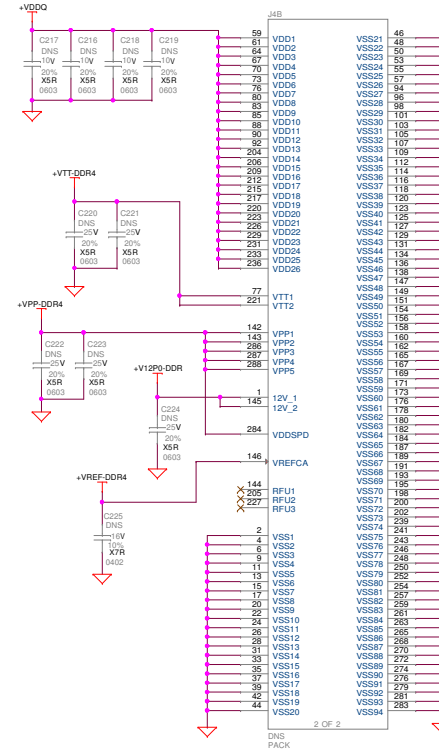
BLANK PAGE



Routing Notes:

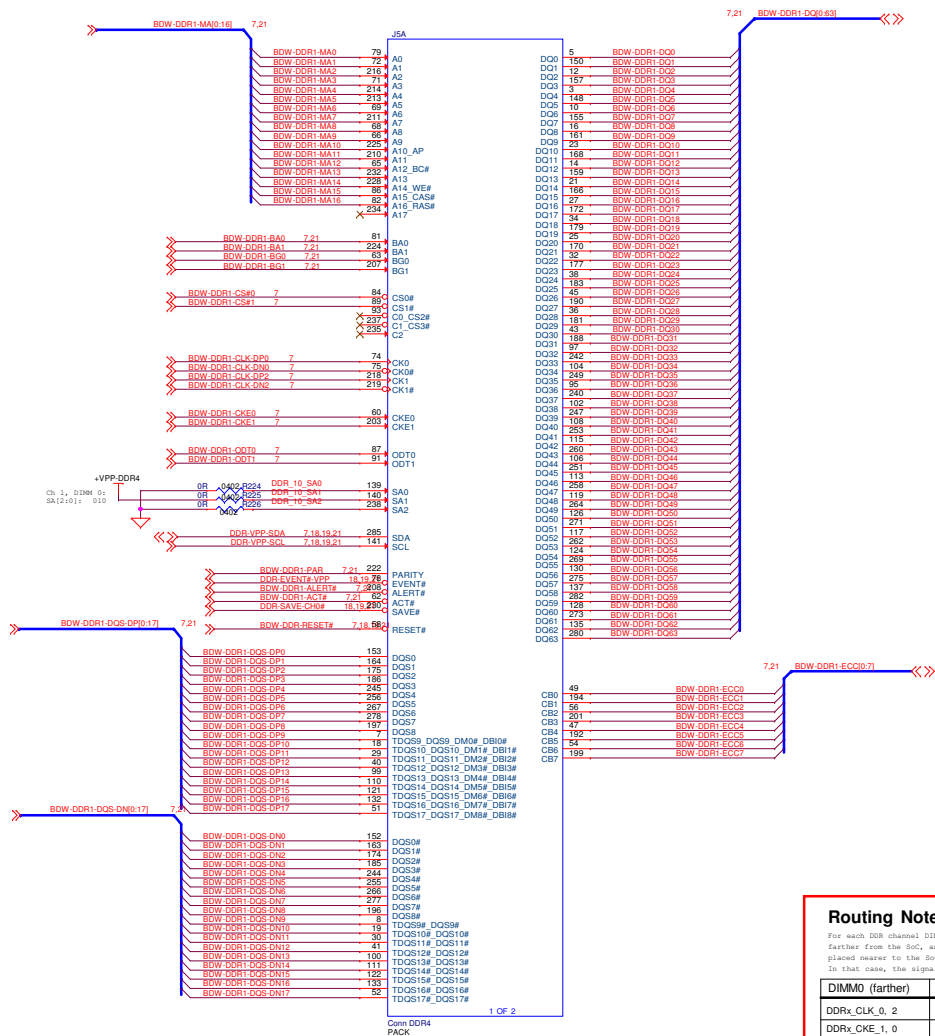
For each DDR channel DIMM0 is to be placed farther from the SoC, and DIMM1 is to be placed nearer to the SoC.
In that case, the signals are to be routed as:

DIMM0 (farther)	DIMM1 (nearer)
DDR _R _CLK_0_2	DDR _R _CLK_1_3
DDR _R _CKE_1_0	DDR _R _CKE_3_2
DDR _R _ODT_1_0	DDR _R _ODT_3_2
DDR _R _CS_1_0	DDR _R _CS_5_4



DDR4 Channel 0, DIMM 1

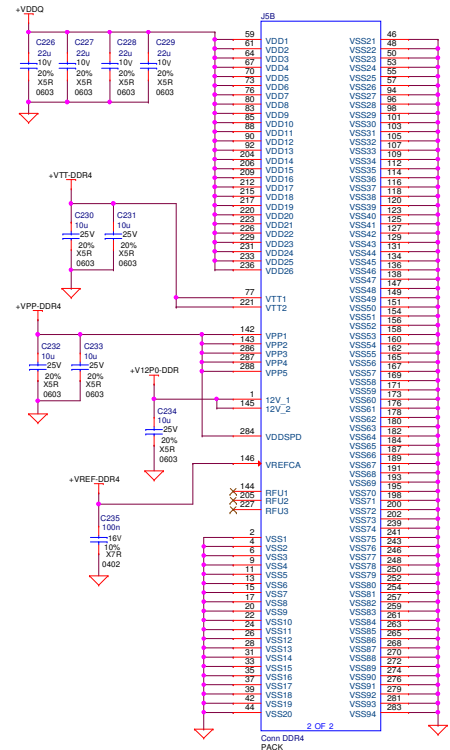
DRAWING No. : 80504	REV No. : R200	0100K000 Medium AT&T Compute Board	APPROVALS	SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	DATE : Sunday, April 07, 2019	Tuesday, July 17, 2018	CHECK	
DATE : Sunday, April 07, 2019	DATE : Tuesday, July 17, 2018	DATE : Tuesday, July 17, 2018	APPROV.	
DATE : Sunday, April 07, 2019	DATE : Tuesday, July 17, 2018	DATE : Tuesday, July 17, 2018	SHEET : 18 of SHEETS : 30	



Routing Notes:

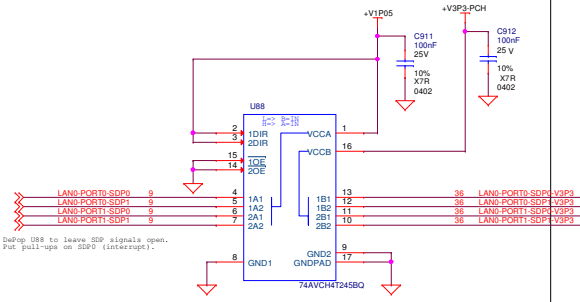
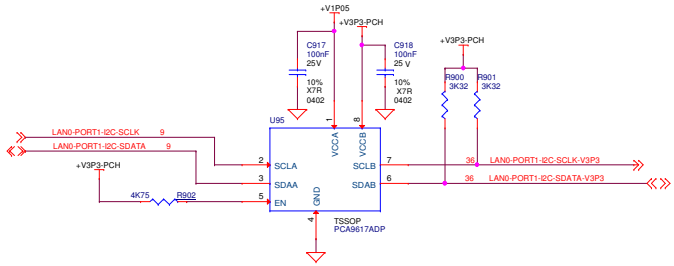
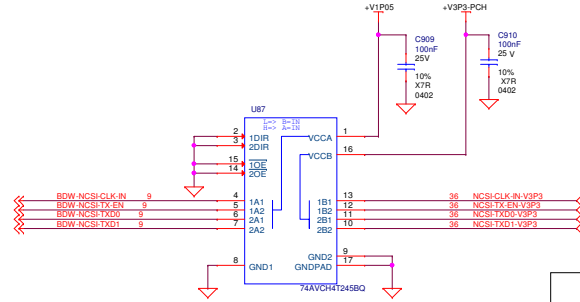
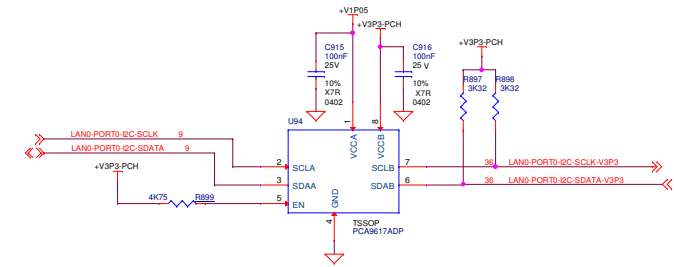
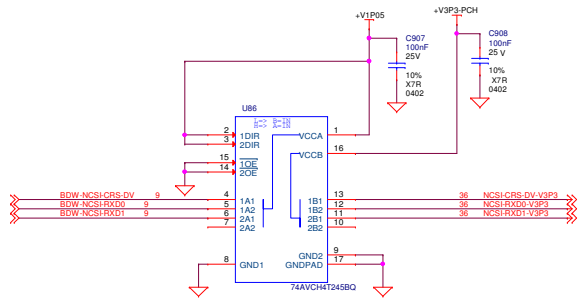
For each DDR channel DIMM0 is to be placed farther from the SoC, and DIMM1 is to be placed nearer to the SoC.
In that case, the signals are to be routed as:

DIMM0 (farther)	DIMM1 (nearer)
DDR _x _CLK_0_2	DDR _x _CLK_1_3
DDR _x _CKE_1_0	DDR _x _CKE_3_2
DDR _x _ODT_1_0	DDR _x _ODT_3_2
DDR _x _CS_1_0	DDR _x _CS_5_4

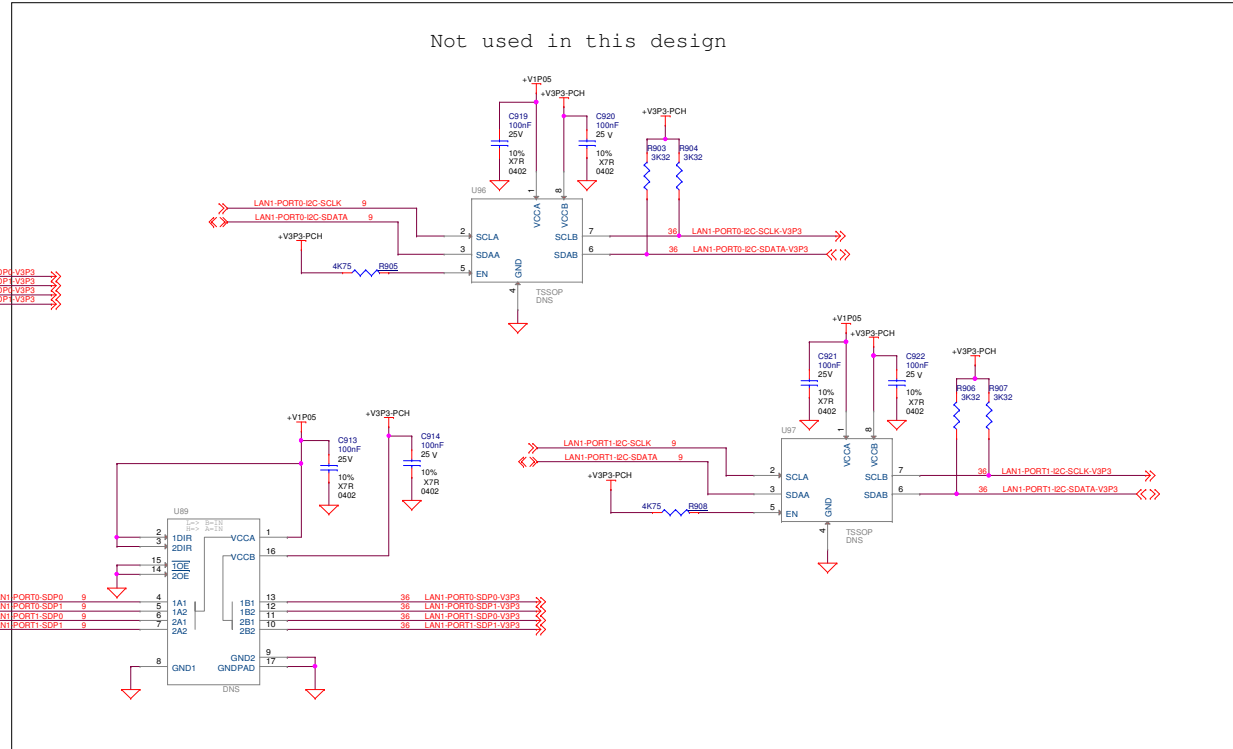


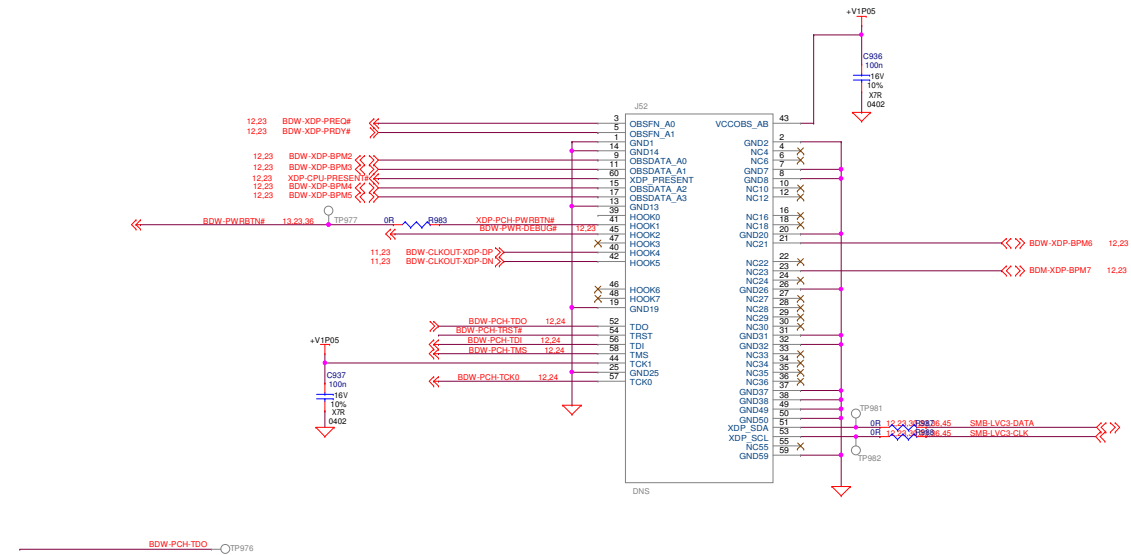
DDR4 Channel 1, DIMM 0

DRAWING No. : 80004		DDR Ch 1, DIMM 0 01900G2 Medium AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200		CHECK	NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019 Tuesday, July 17, 2018			APPROV.				
			SHEET : 20 of SHEETS : 30				

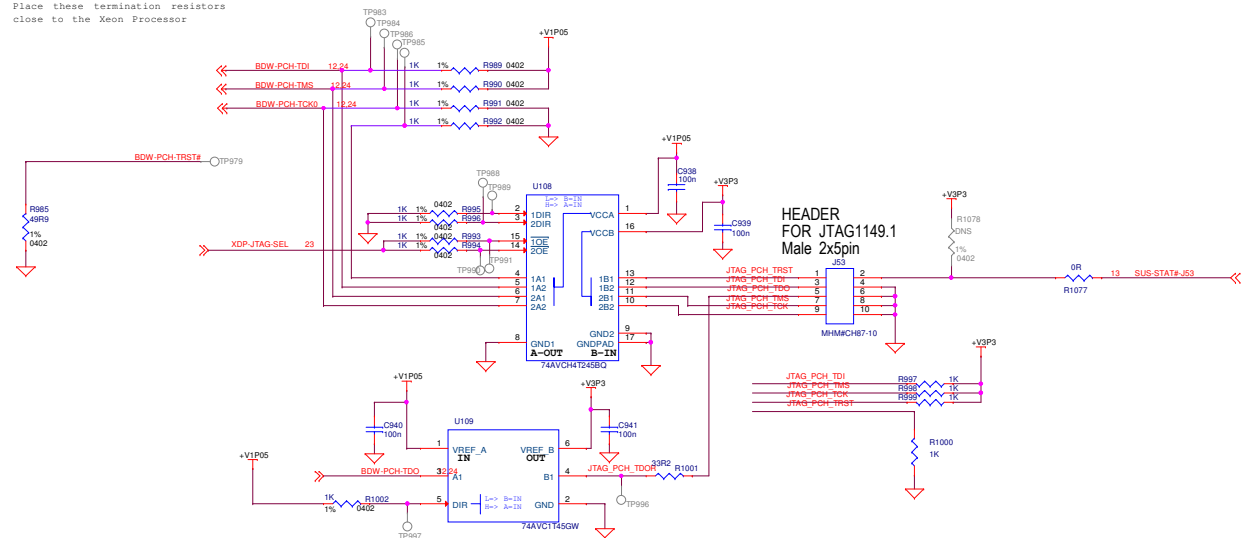


Put pull-ups on SDP0 (interrupts).





Layout Note:
Place these termination resistors
close to the Xeon Processor



DRAWING No. : 80504		PCH Debug Connectors		APPROVALS				SILICOM Ltd. Concivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			0190G02 Medium				
DATE : Sunday, April 07, 2019 Monday, June 11, 2019		AT&T Compute Board		CHECK	NAME	SIGN	DATE	
				APPROV.				
				SHEET : 24	of SHEETS : 30			

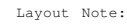
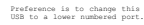
Connectivity Solutions
A Member of RAD Group

BLANK PAGE

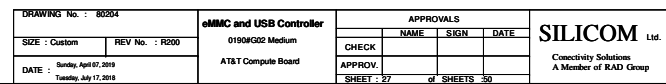
DRAWING No. : 80504		Blank 0190KG02 Medium AT&T Compute Board	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group	
SIZE : Custom	REV No. : R200			NAME	SIGN		DATE
DATE : Sunday, April 07, 2019			CHECK				
Monday, June 11, 2018			APPROV.				
			SHEET : 25	of SHEETS : 30			

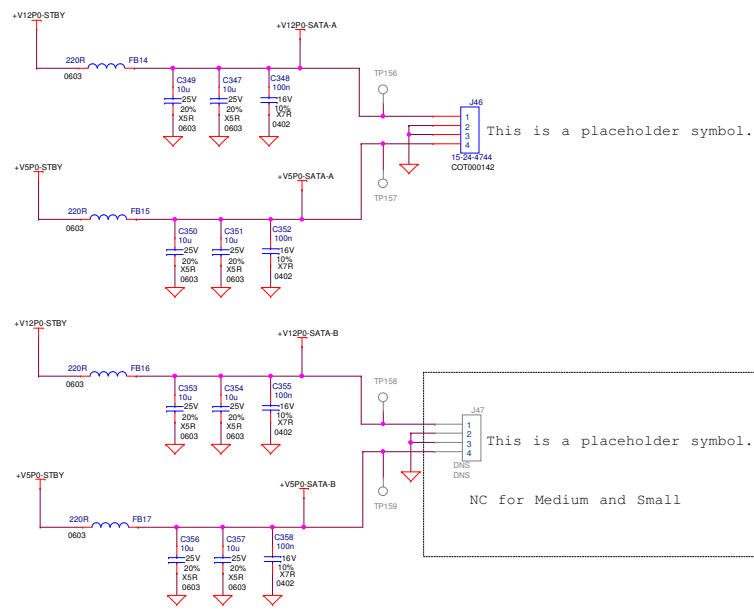
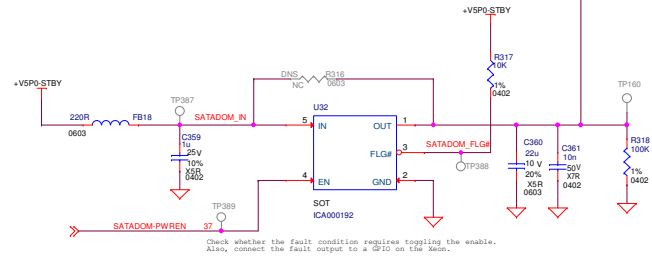
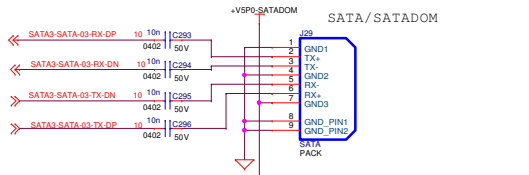
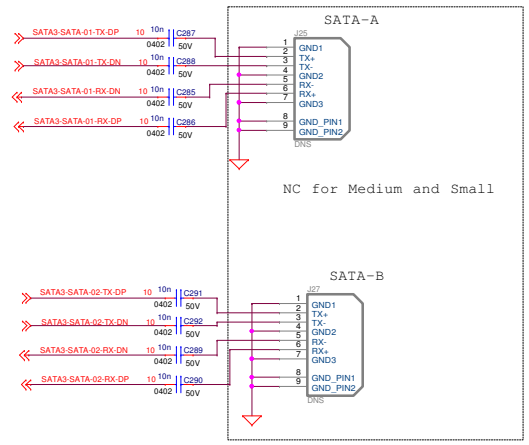
BLANK PAGE

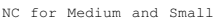
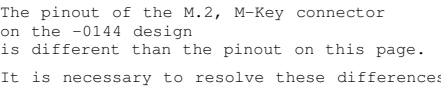
DRAWING No. : 80504		Blank 0190RG02 Medium AT&T Compute Board	APPROVALS			SILICOM Ltd. Connectivity Solutions A Member of RAD Group	
SIZE : Custom	REV No. : R200			NAME	SIGN		DATE
DATE : Sunday, April 07, 2019			CHECK				
Monday, June 11, 2019			APPROV.				
			SHEET : 28 of SHEETS : 30				



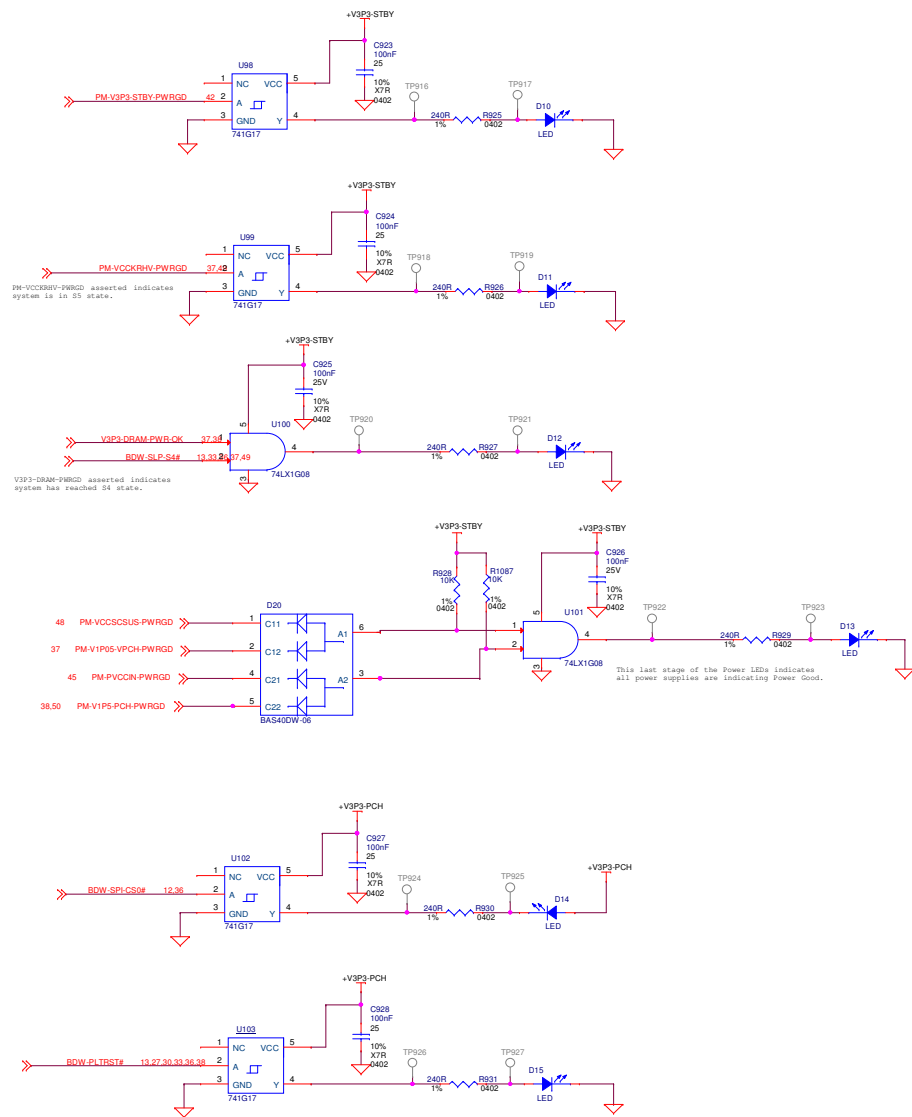
Route through NC and RFU pins to break-out
with standard TH vias.







BLANK PAGE



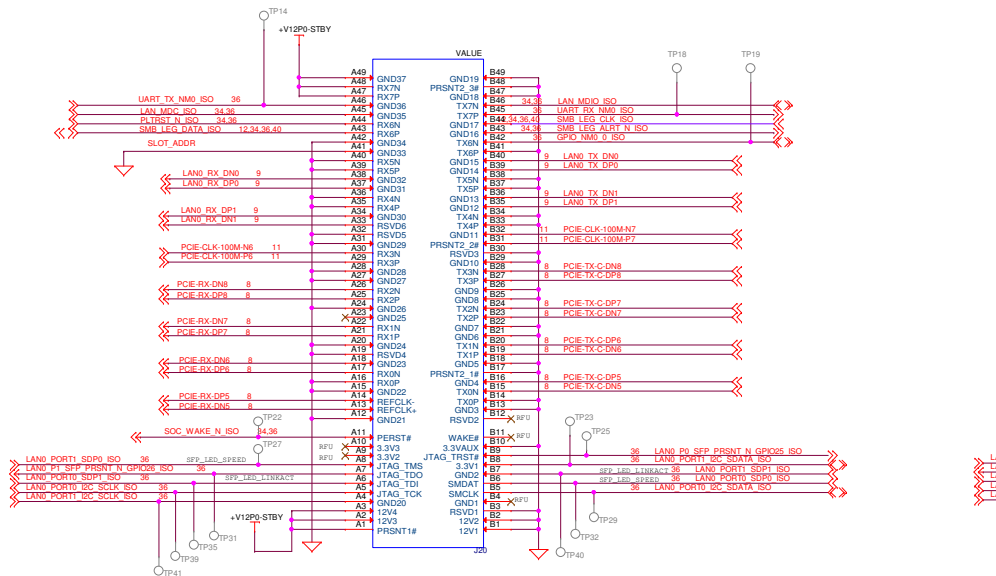
12V DDR Core Load Switch



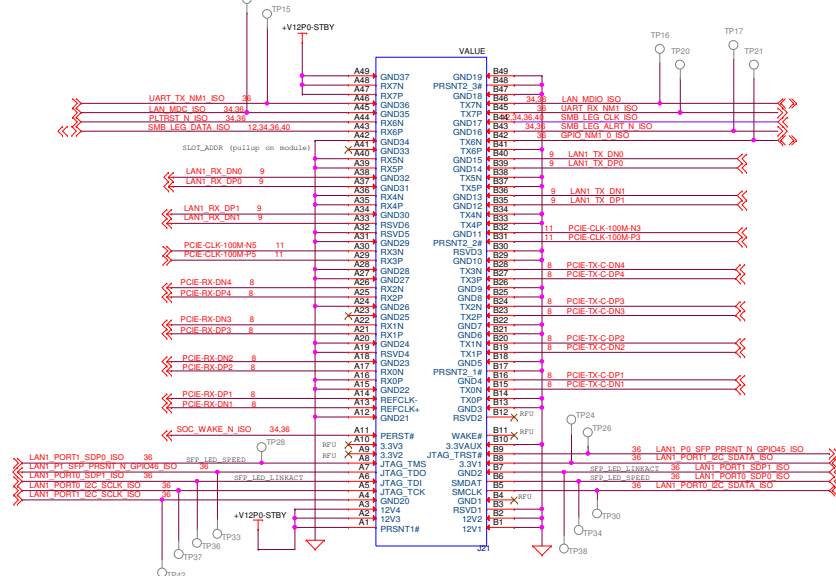
SILICOM Ltd.
Connectivity Solutions
A Member of RAD Group

NOTE:
The net names on these connectors
were copied from the -0150 schematic.
They will need to be updated to reflect their use
in this design, once the Xeon is placed.

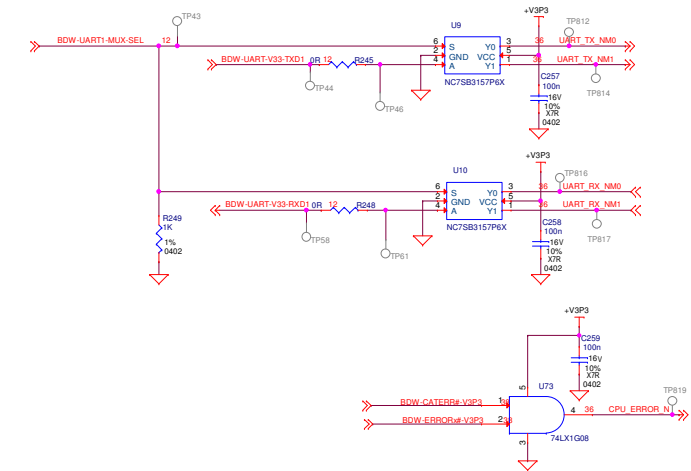
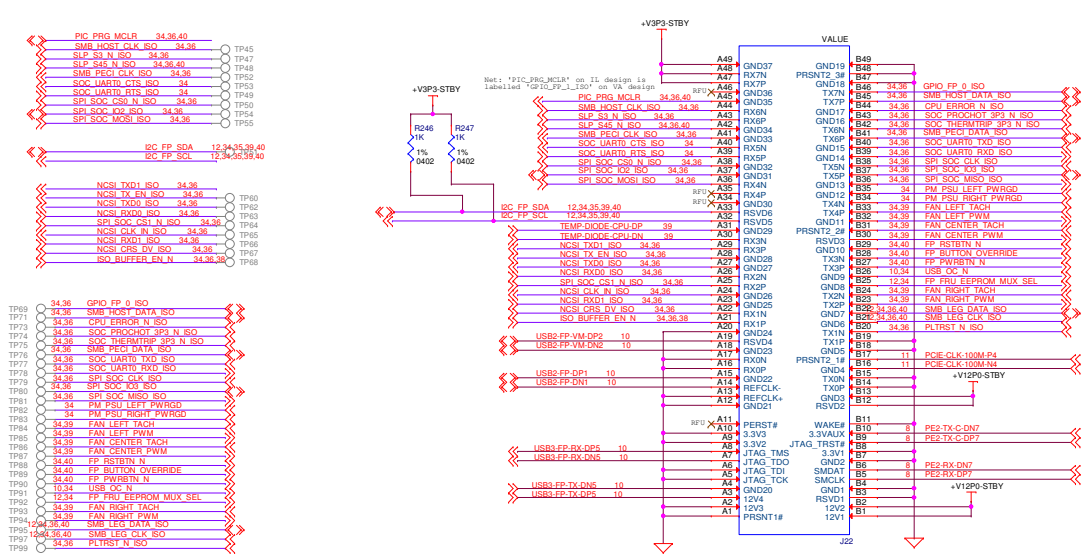
Network Module 0



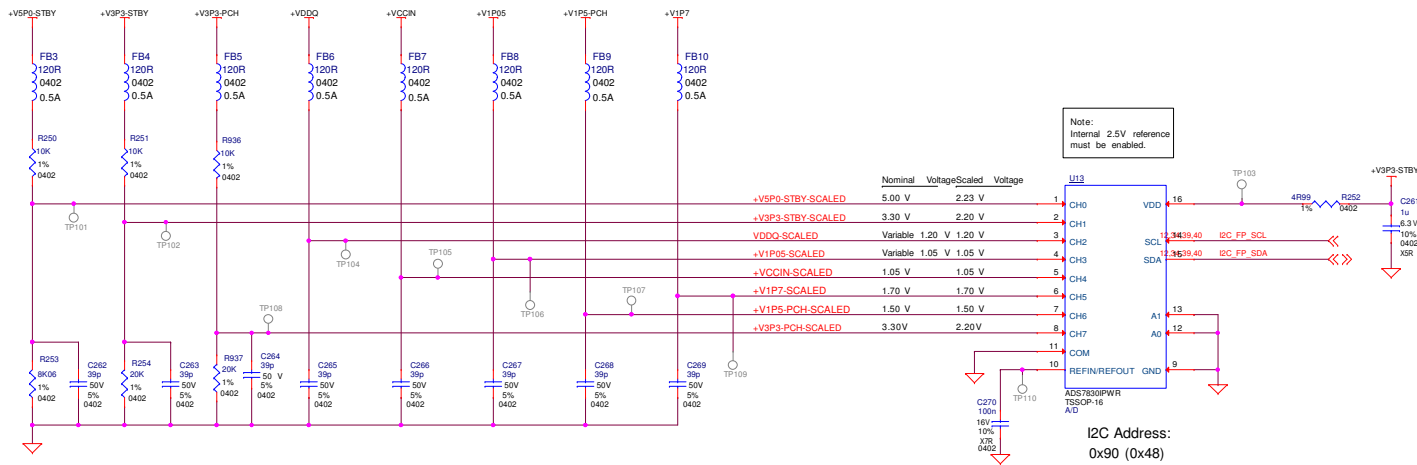
Network Module 1



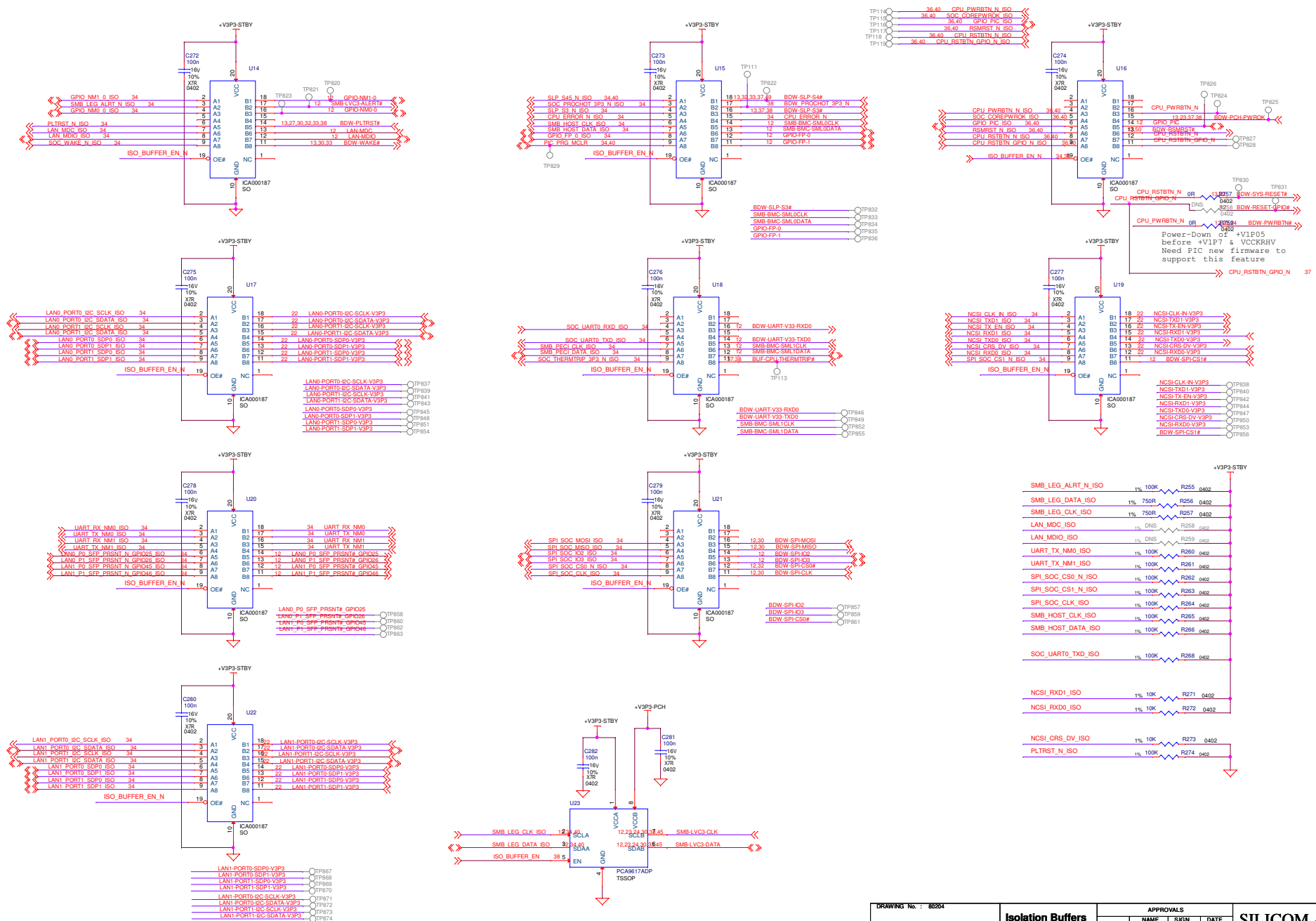
Front Panel I/O Module



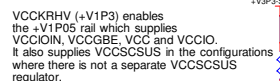
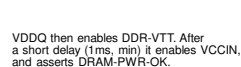
ADC Voltage Monitor
(0 to +2.5 V Range)



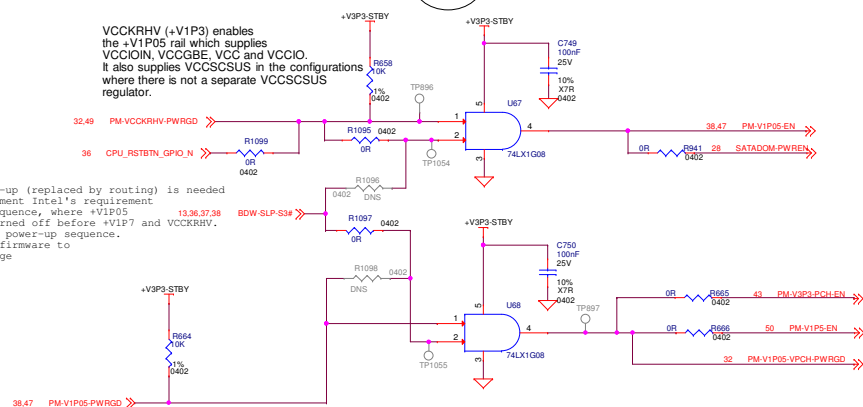
3.3V Isolation Buffers



+V12P0-DDR enables +V2P5-DDR and VDDQ.
+V2P5 is delayed approx 10ms and VDDQ is delayed another 10-12 ms.

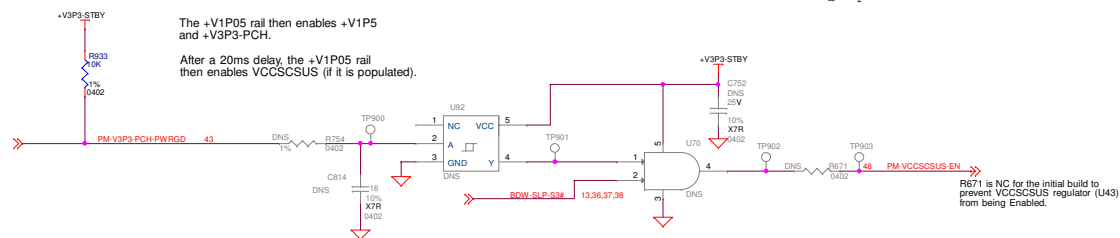


This manual touch-up (replaced by routing) is needed in order to implement Intel's requirement for power-down sequence, where +V1P05 13.36.37.38 rail should be turned off before +V1P7 and VCCKRHV. Doesn't impact on power-up sequence. Required new PIC firmware to support this change



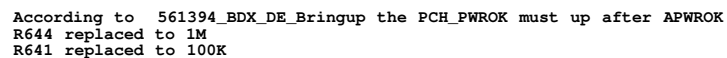
The +V1P05 rail then enables +V1P5 and +V3P3-PCH.

After a 20ms delay, the +V1P05 rail then enables VCCSCSUS (if it is populated).

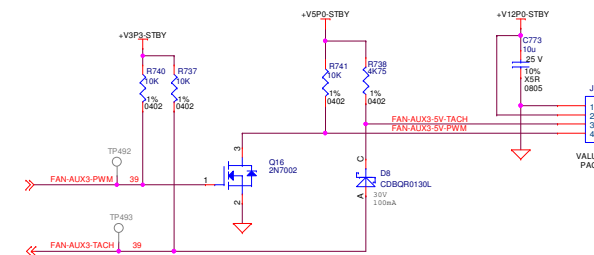
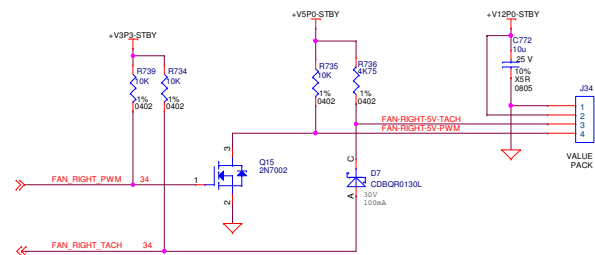
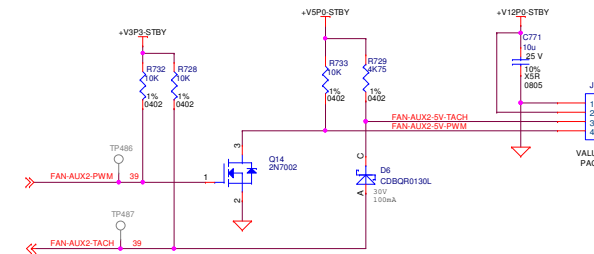
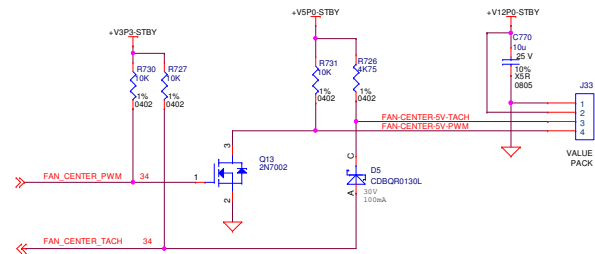
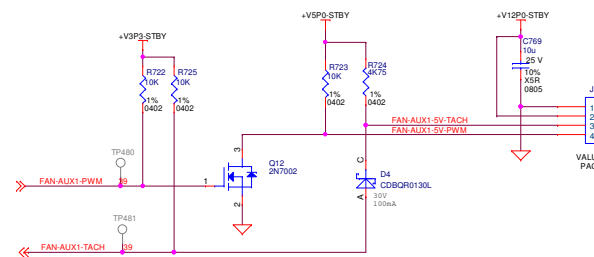
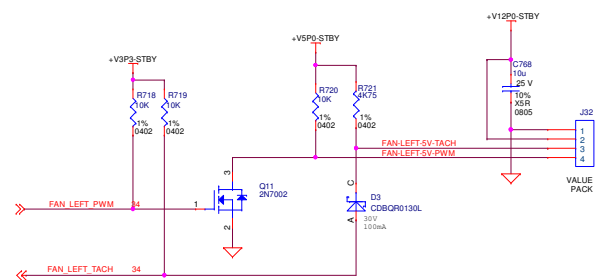
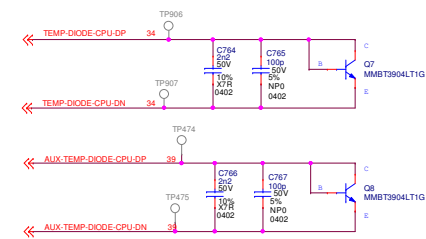
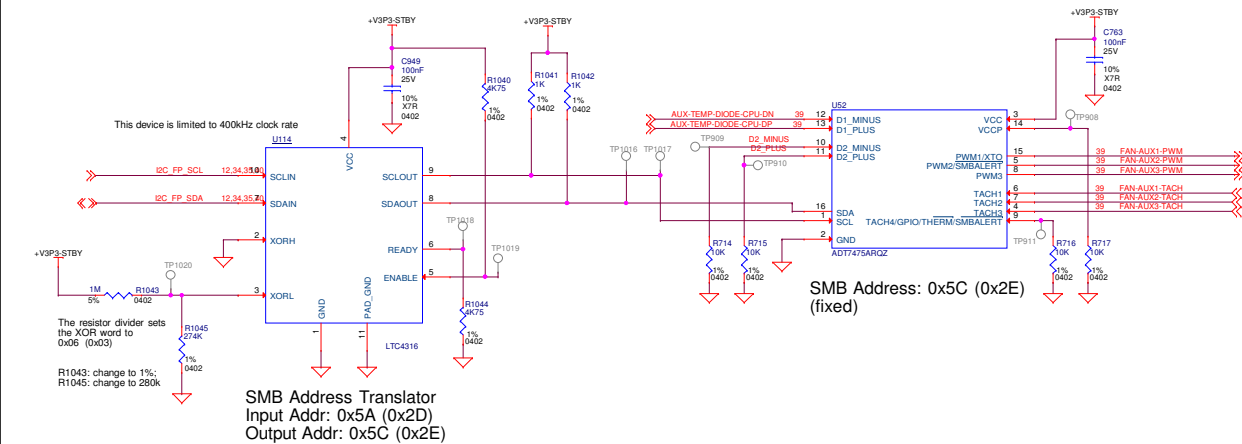


R671 is NC for the initial build to prevent VCCSCSUS regulator (U43) from being Enabled.

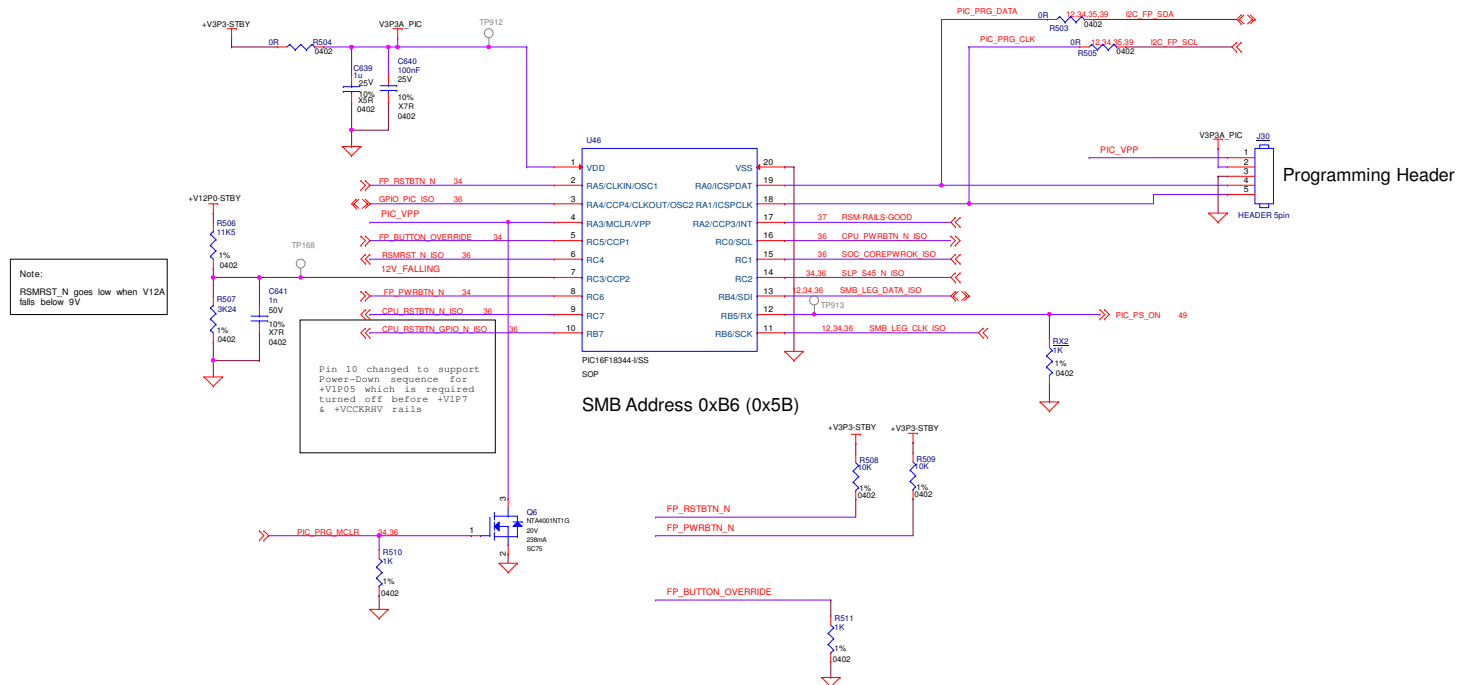
3.3V <--> 1.05V Level Shifting



DRAWING No. : 80264		Power Sequencing & Level Shifters 0100K002 Medium AT&T Compute Board	APPROVALS				SILICOM Ltd. Concivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019 Thursday, July 19, 2018			CHECK				
			APPROV.				
			SHEET : 18	of SHEETS : 50			

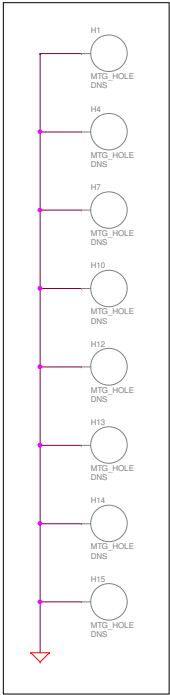


PIC Microcontroller

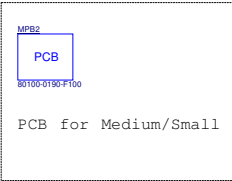
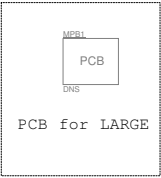
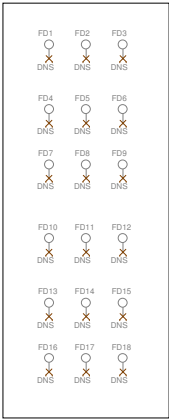


DRAWING No. : 80204		PIC Controller 0100002 Medium AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			NAME	SIGN	DATE	
			CHECK				
			APPROV.				
DATE : Sunday, April 07, 2019 Thursday, July 15, 2018			SHEET : 40		SHEETS : 50		

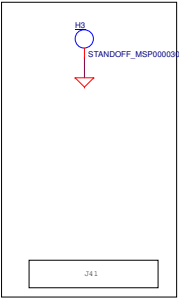
Mounting Holes



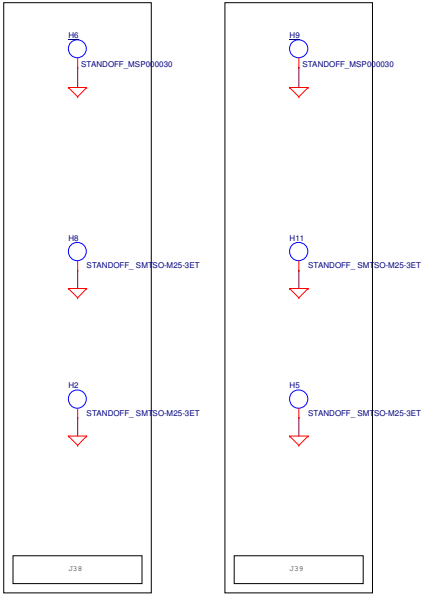
Fiducials



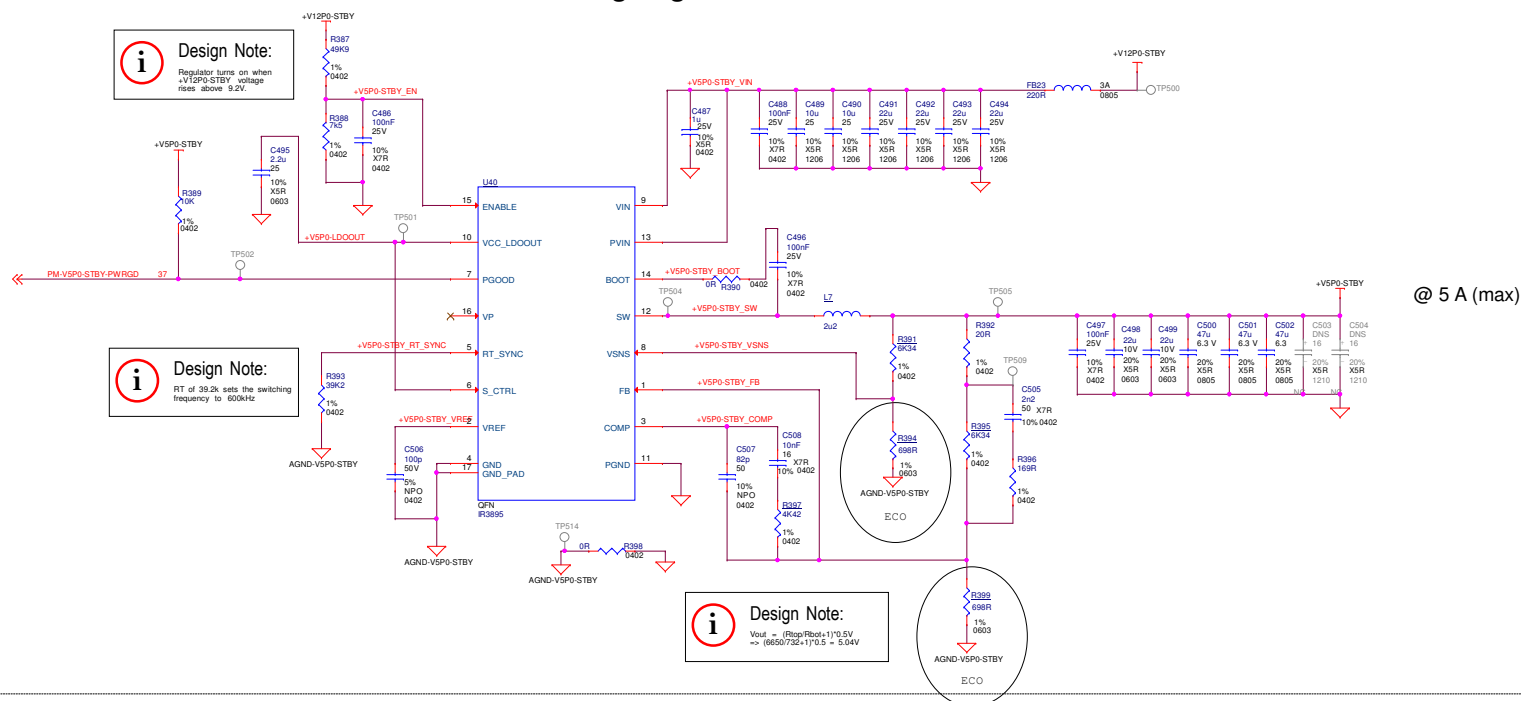
M.2 Standoffs



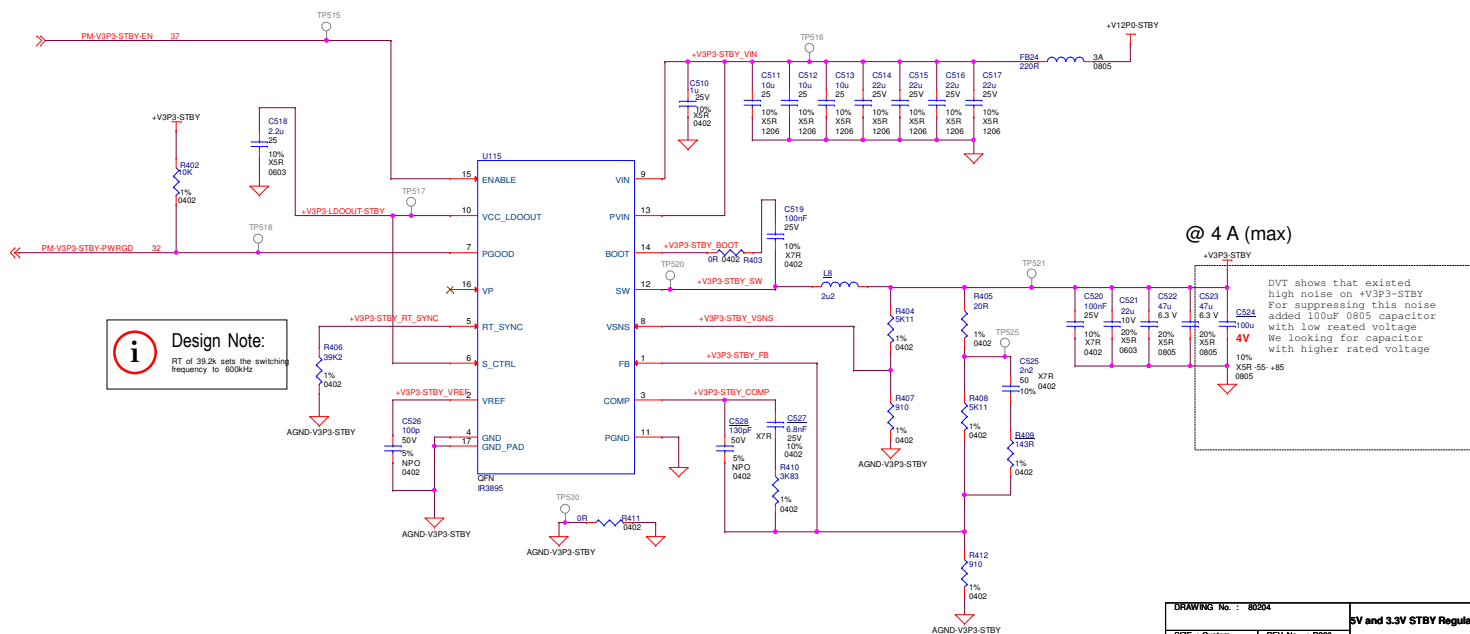
M.2 Standoffs



5V STBY Switching Regulator

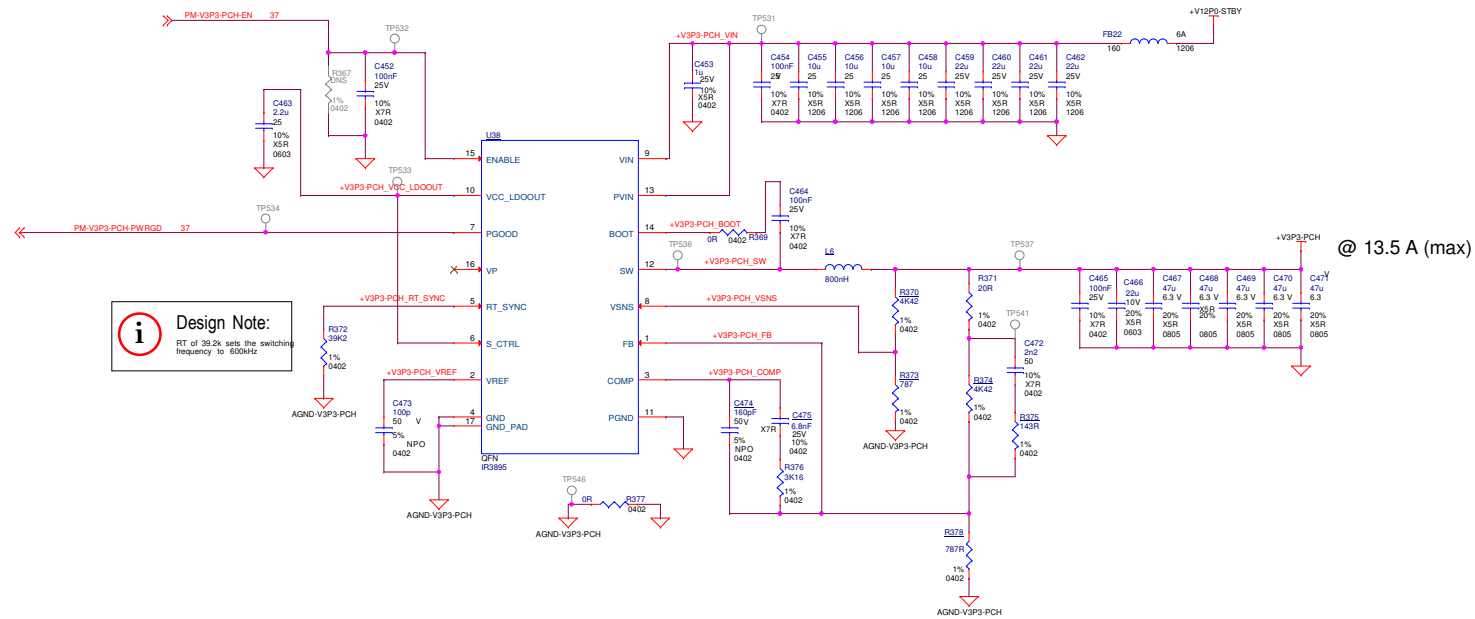


3.3V STBY Switching Regulator



DRAWING No. : 80204		5V and 3.3V STBY Regulators 0190G022 Module AT&T Compute Board	APPROVALS			SILICOM Ltd Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200		NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019 Wednesday, July 18, 2018			CHECK			
			APPROV			
			SHEET : 02	of SHEETS : 50		

3.3V PCH Switching Regulator



DRAWING No. : 80204		3.3V PCH Regulator 0190K02 Medium AT&T Compute Board	APPROVALS				SILICON Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019			CHECK				
Wednesday, July 18, 2018			APPROV.				
			SHEET : 43	of SHEETS : 50			

Design Note:
Rfreq of 15k sets the switching frequency to 650kHz



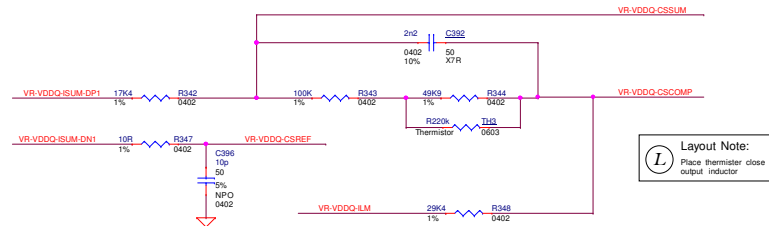
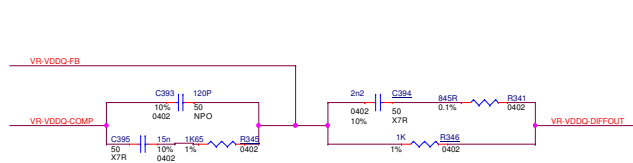
Layout Note:
Place thermister close to output inductor

Layout Note:
Route current sense lines from inductor as a differential pair

SVID Address Selection	
Address	Riboot (kOhms)
0x0	0
0x1	14.0
0x2	22.1
0x3	30.1
0x4	39.2
0x5	48.7
0x6	57.6
0x7	68.1
0x8	78.7
0x9	88.7
0xA	100
0xB	113
0xC	124
0xD	137
0xE	150
0xF	165
0x7	178
0x8	196

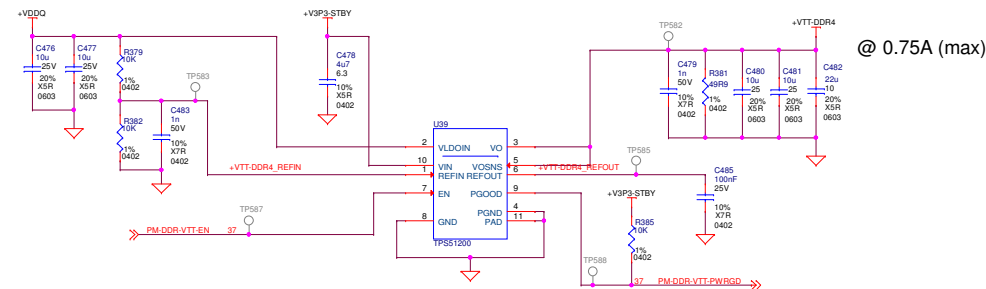
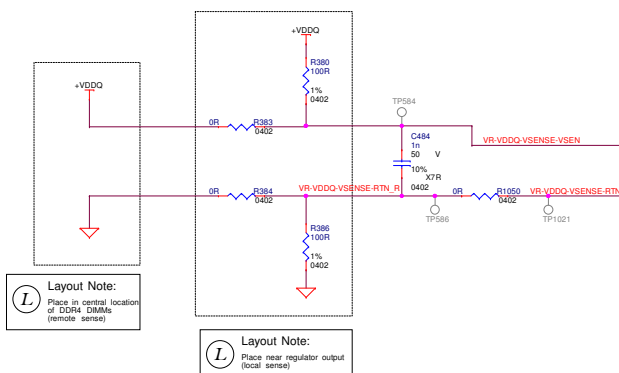
$$\begin{aligned} \text{ICC-MAX} &= R(\text{icc-max})^3 \cdot 3.2 \cdot 10^4 \cdot (-4) \\ \text{ICC-MAX} &= 15.2 \text{ A} \\ \text{ICC-MAX} &= 47500 \cdot 3.2^\circ \end{aligned}$$

VDDQ Current Loop Compensation



Layout Note:
Place thermister close
output inductor

Sink / Source DDR Termination Regulator



@ 0.75A (max)

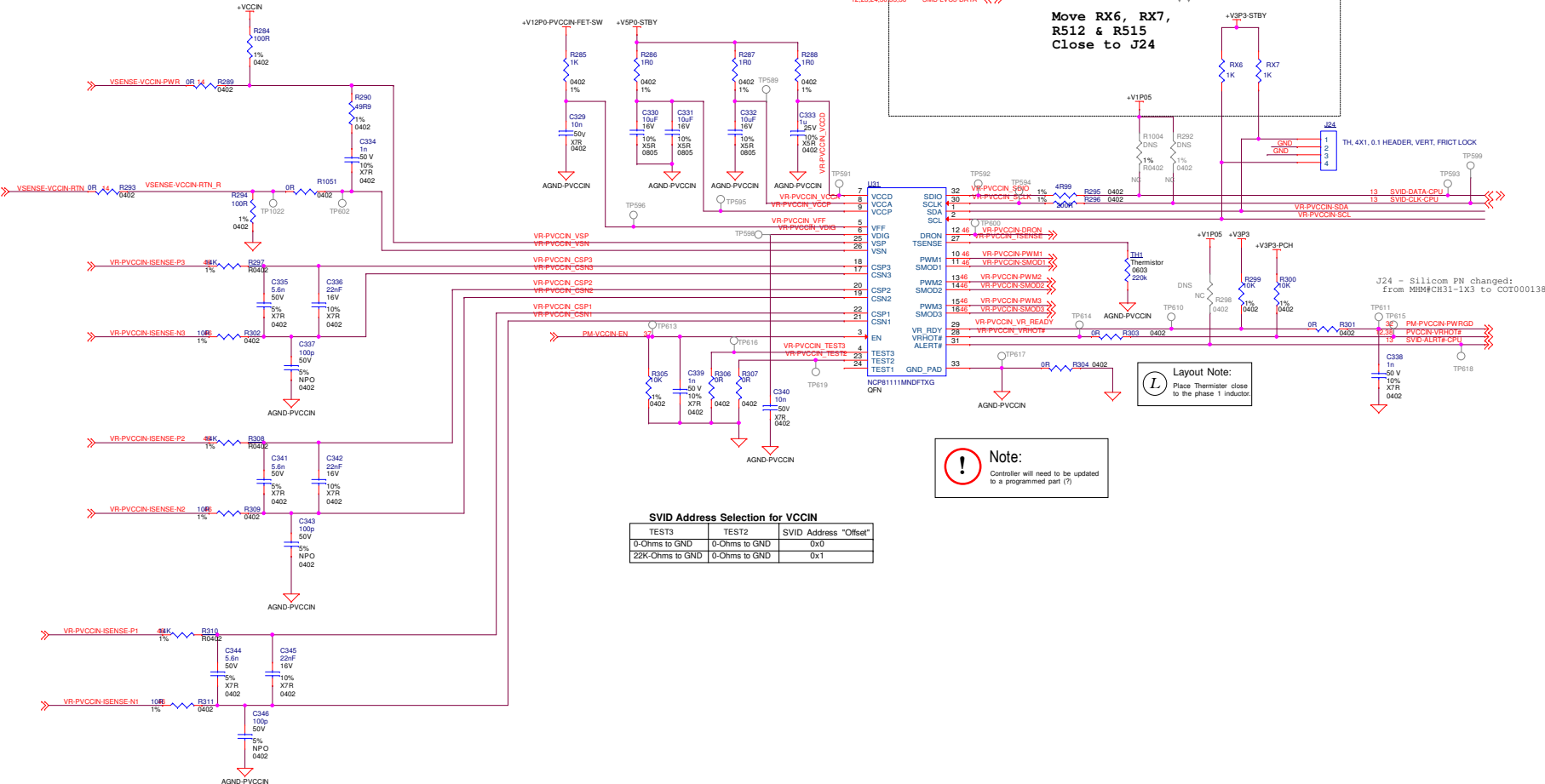
DRAWING No. : 80204		VDDB SVID Regulator 0190G02 Medium AT&T Compute Board	APPROVALS				SILICON Ltd. Connectivity Solutions A Member of RAD Group																
SIZE : Custom REV No. : R200			<table><tr><td></td><td>NAME</td><td>SIGN</td><td>DATE</td></tr><tr><td>CHECK</td><td></td><td></td><td></td></tr><tr><td>APPROV.</td><td></td><td></td><td></td></tr><tr><td colspan="2">SHEET : 44</td><td>of</td><td>SHEETS : 50</td></tr></table>						NAME	SIGN	DATE	CHECK				APPROV.				SHEET : 44		of	SHEETS : 50
	NAME		SIGN	DATE																			
CHECK																							
APPROV.																							
SHEET : 44		of	SHEETS : 50																				
DATE : Sunday, April 07, 2019 Wednesday, July 18, 2018																							

Power: VCCIN SVID Controller



Design Note:

If NCP81111 needs to be reprogrammed in-circuit, use DeepFlash USB to I2C adapter (PN: R286-USB-I2C) and GUI from On-Sem. See On-Sem: NCP81111 programming presentation for overview.



Note:

Controller will need to be updated to a programmed part (7)

SVID Address Selection for VCCIN

TEST3	TEST2	SVID Address "Offset"
0-Ohms to GND	0-Ohms to GND	0x0
22K-Ohms to GND	0-Ohms to GND	0x1

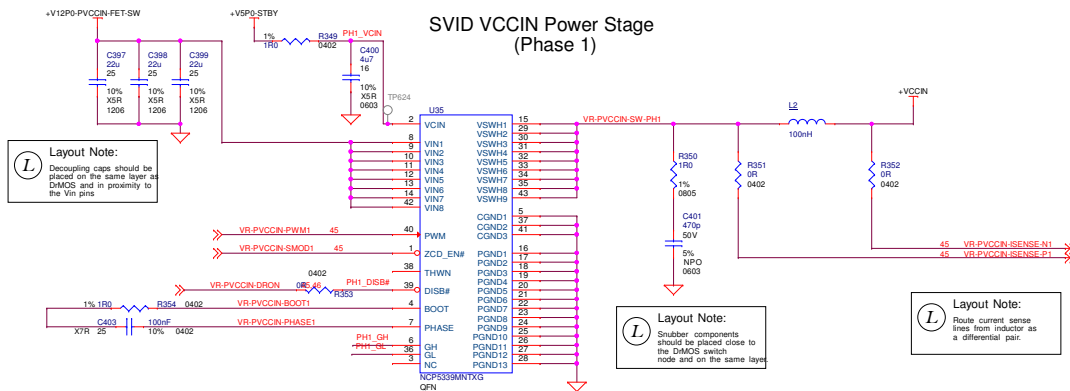
DRAWING No. : 80504

SIZE : Custom
DATE : Sunday, April 07, 2019
Wednesday, July 18, 2018

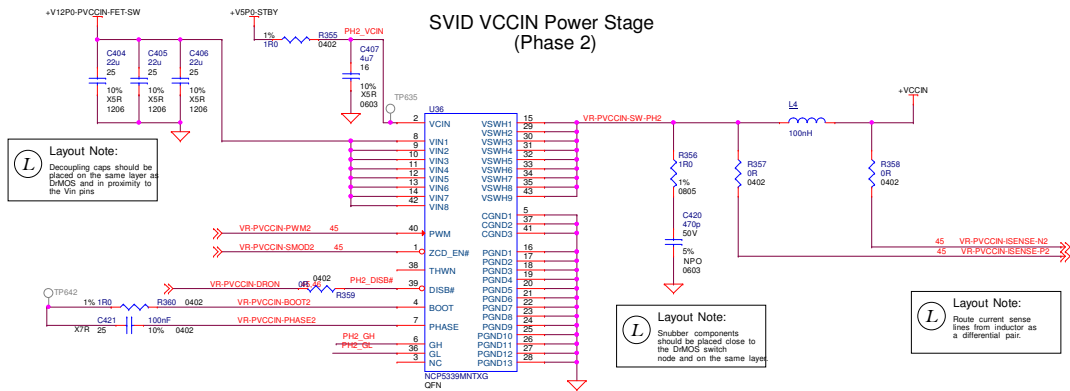
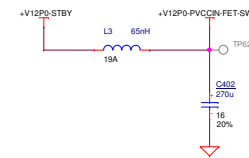
REV No. : R200
0190MG02 Medium
AT&T Compute Board

APPROVALS
NAME SIGN DATE
CHECK
APPROV.
SHEET : 45 of SHEETS : 30

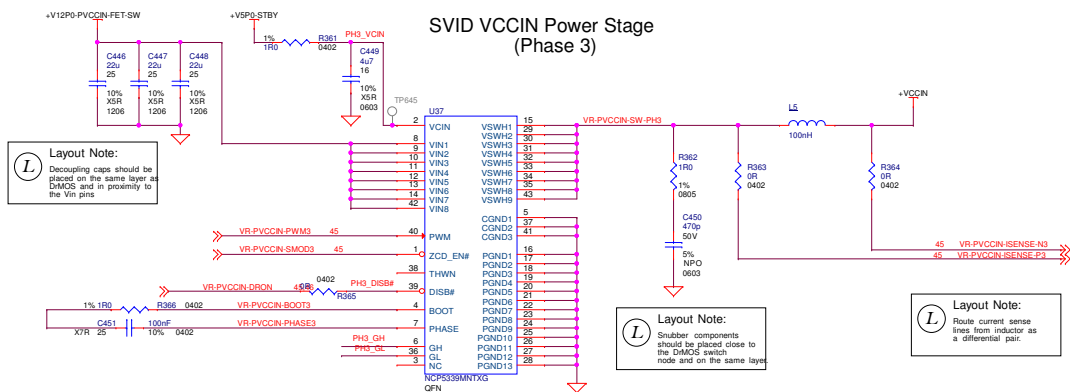
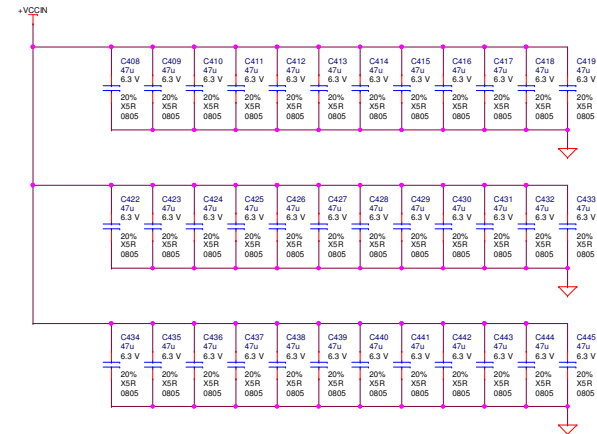
SILICOM Ltd.
Connectivity Solutions
A Member of RAD Group



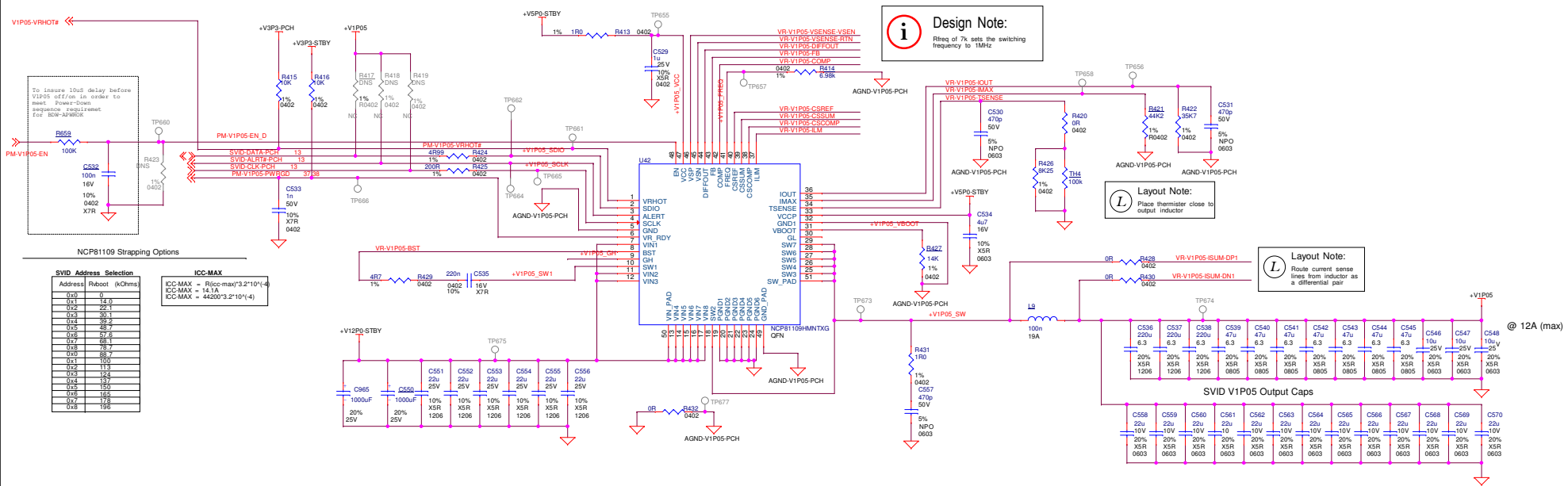
SVID VCCIN Power State Power Entry Filter



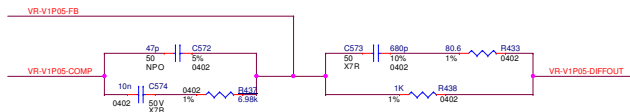
SVID VCCIN Output Caps (Place Near Inductors)



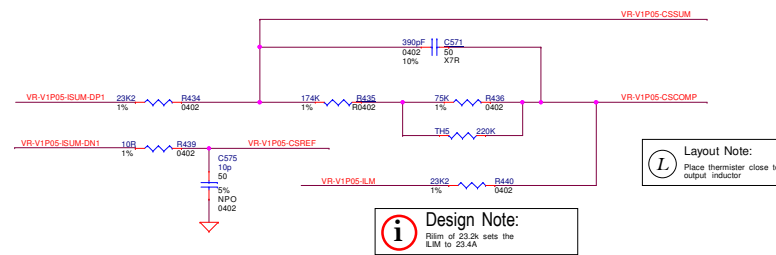
SVID V1P05 "Combined" Regulator



V1P05 Regulator Loop Compensation Network

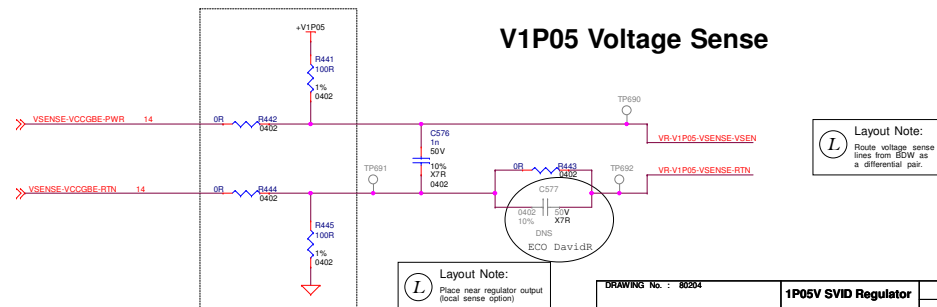


V1P05 Current Loop Compensation



12V DDR Core Load Switch

V1P05 Voltage Sense



DRAWING No. : 80304

SIZE : Custom REV No. : R200

DATE : Sunday, April 07, 2019

Wednesday, July 18, 2018

1P05V SVID Regulator

0190K02 Medium

AT&T Compute Board

APPROVALS

CHECK NAME SIGN DATE

APPROV.

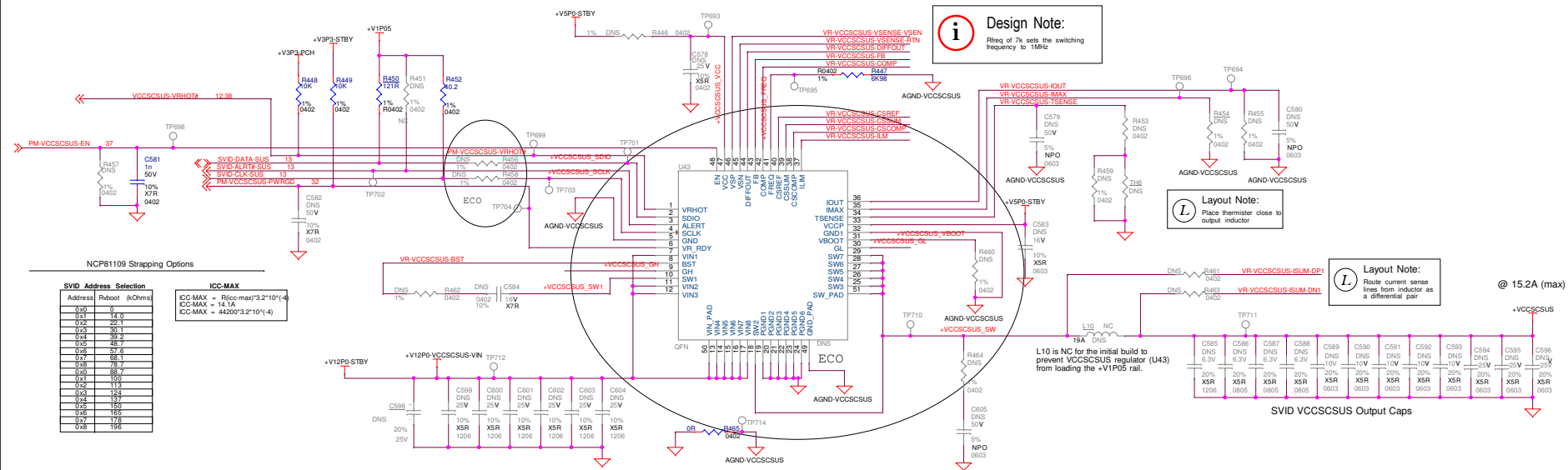
SHEET : 47 of SHEETS : 30

SILICONIC Ltd.

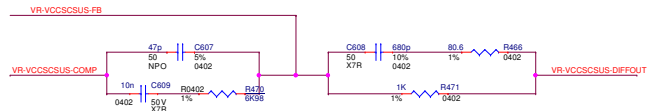
Connectivity Solutions

A Member of RAD Group

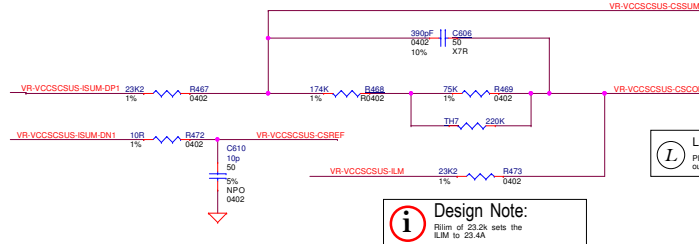
SVID VCCSCSUS Regulator



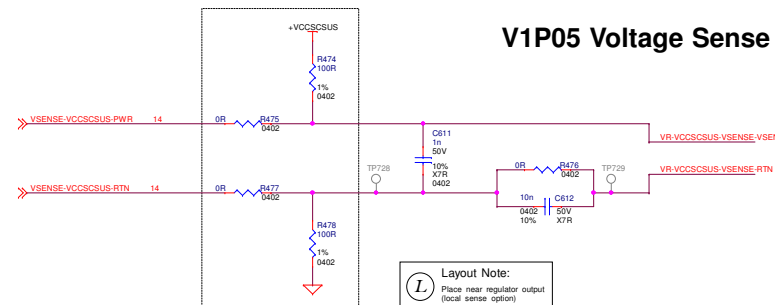
VCCSCSUS Voltage Loop Compensation Network



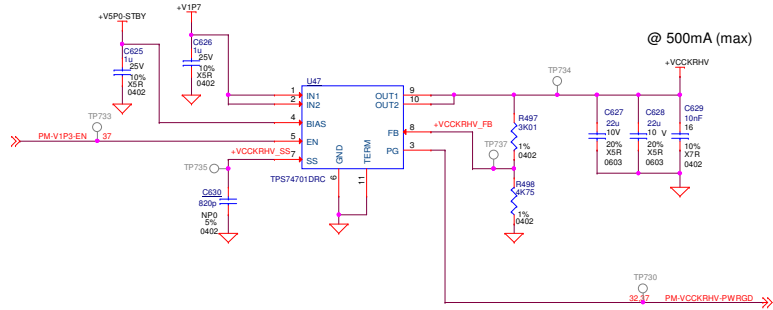
V1P05 Current Loop Compensation



V1P05 Voltage Sense



1.3V Linear Regulator



@ 500mA (max)

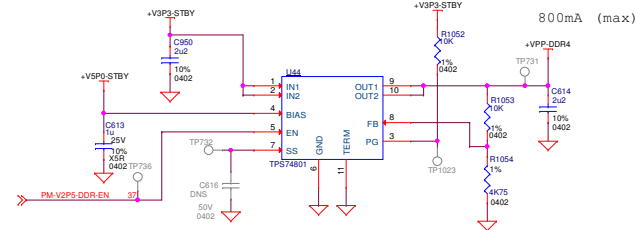
Design Note:

$t_{ss} = C_{625} \times 0.8V / 0.44\mu A$
 $t_{ss} = 0.00082 \times 0.8 / 0.44$
 $t_{ss} = 1.49msec$

Design Note:

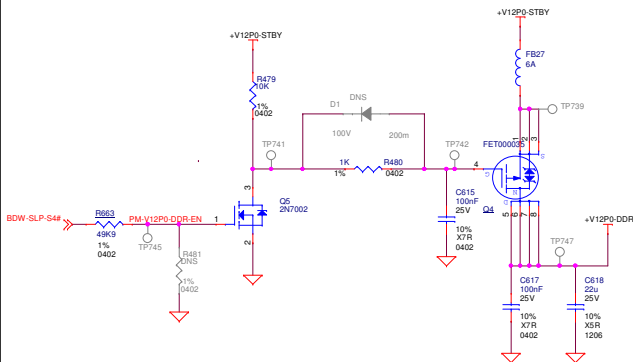
$V_{out} = (R_{487}/R_{498} + 1) \times 0.8V$
 $\Rightarrow (3.01/4.75 + 1) \times 0.8 = 1.31V$

2.5V Linear Regulator for DDR4

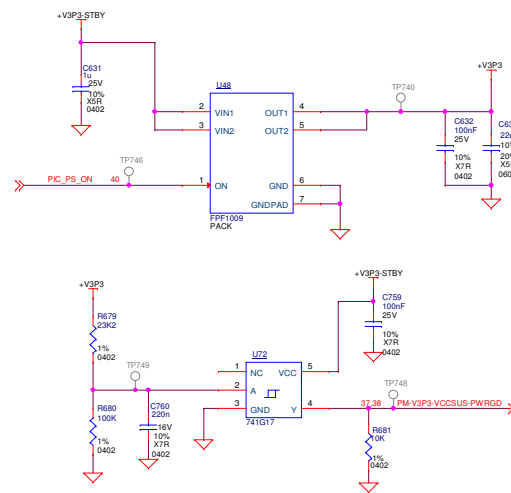


800mA (max)

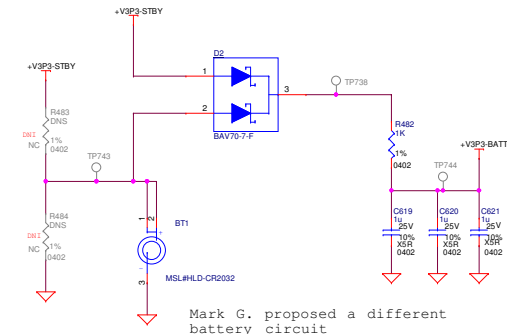
12V DDR Core Load Switch



3.3V Suspend Load Switch



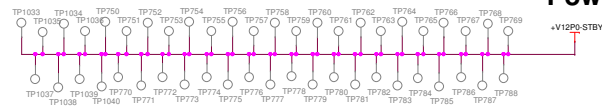
Battery Backup



Mark G. proposed a different battery circuit

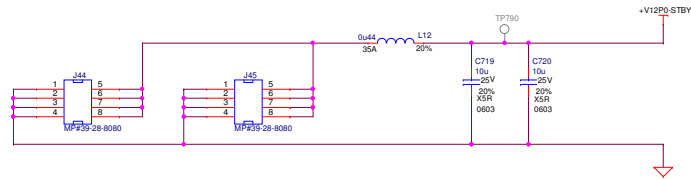
DRAWING No. : 80304		Downstream Regulators 0190G02 Medium AT&T Compute Board	APPROVALS				SILICOM Ltd. Connectivity Solutions A Member of RAD Group
SIZE : Custom	REV No. : R200			NAME	SIGN	DATE	
DATE : Sunday, April 07, 2019			CHECK				
Wednesday, July 18, 2018			APPROV.				
			SHEET : 49	of	SHEETS : 50		

Power Entry and Downstream Regulators (Switching)

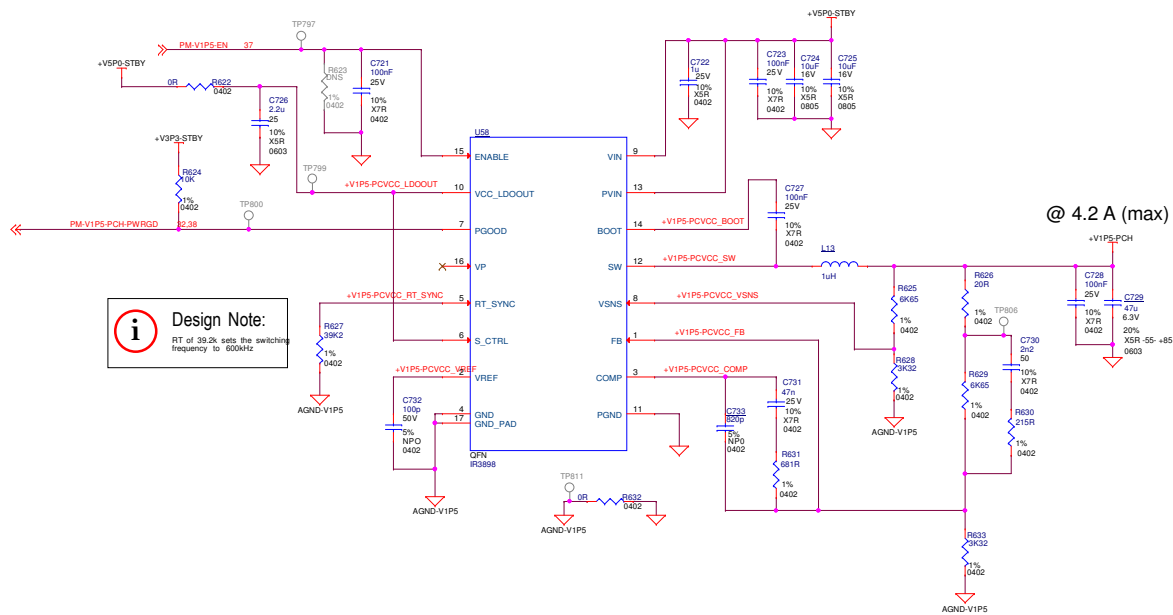


12V Power Entry

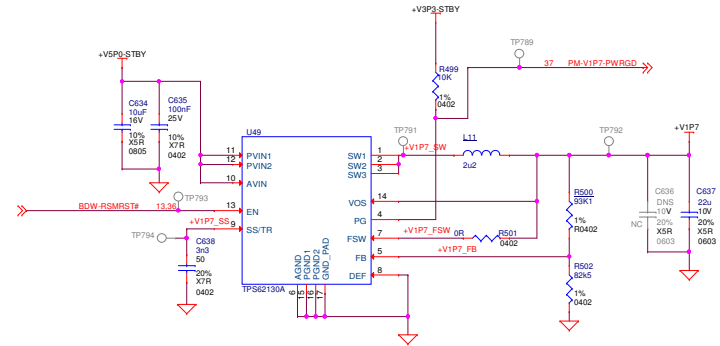
Anticipated current:
Nominal: 11A
Max: 23A



1.5V Switching Regulator



1.7V Switching Regulator



Design Note:
I_{ss} = C_{ss} * 1.25/2.5uA
I_{ss} = 0.0033 * 1.25/2.5
I_{ss} = 1.65msec

Design Note:
V_{out} = (R₃₀/R₃₁) * 1.70.8V
=> (80.1825/170.8) * 1.70V