



# Modular - Extensible IO (M-XIO) Base Specification

Part of the  
Datacenter - Modular Hardware Systems (DC-MHS) Rev 1.0 family  
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## 1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

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## 2. Version Table

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| Date     | Version #   | Description  |
|----------|-------------|--|
| 04/27/22 | v0.7        | Initial public release   |
| 06/22/22 | v0.8        | Minor clarifications throughout the document.<br>Updated section 5.7 FlexIO requirements.<br>Swapped pins A8 and A9 on section 7.x<br>Added requirements on x8 vs x16 routing for section 7.2<br>SFF-TA-1016 variant with split & power.   |
| 08/22/22 | v0.9        | Updates Section 5 and 5.1 regarding 3.3V AUX MGMT.<br>Updates on Section 5.6 regarding 3.3V AUX MGMT.<br>Update on Section 5.7 Flexible I/O requirements.<br>Added section 6.1.3 power sequencing recommendations.<br>Update on Section 7.2 to add SFF-TA-1033, pin naming and table orientation to match mechanical drawings. |
| 09/19/22 | v1.0<br>RC3 | Clean-up with grammar and typo fixes overall.<br>Updated section 5.8 to better explain USB2.0 use cases.   |
| 10/13/22 | v1.0<br>RC4 | Fixed typos around FLEXIO_[1:2] in sections (5.7 & 6.1.2)<br>Updated power sequencing diagram example – figure 10<br>Updated Contact Naming in Figure 11   |

### 3. Scope

This document defines technical specifications for the DC-MHS Modular Extensible I/O used in Open Compute Project. This document shall comprise the hardware product types base specification.

Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with any and all features or requirements described in this specification.

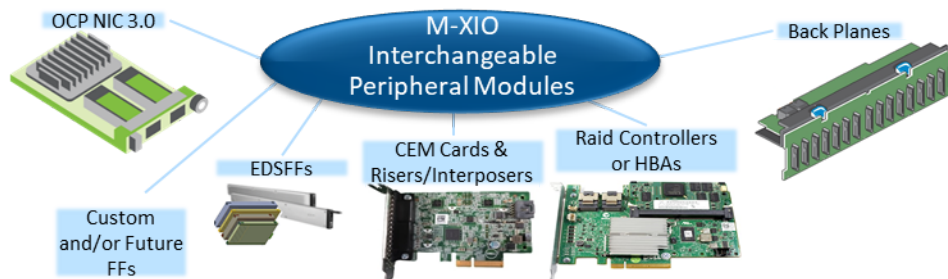
The objective of this specification is to outline the Modular Extensible I/O (M-XIO) source connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers, and peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.

An M-XIO source connector (M-XIO port) can be considered a universal hardware API intended to enable the connectivity (PCIe and Sideband) requirements of multiple different peripheral modules. SAS and SATA support has been deemed out of scope for M-XIO.

This specification does not require specific connector choices, allowing this specification to be used across multiple generations of products and connectors.

This specification covers the following elements for M-XIO source connectors:

- Requirements.
- Signal List.
- Addendums with specific pinouts for a selection of connector models.



**Figure 1: M-XIO's intended Peripheral Module Interconnect Portfolio**

#### 3.1 Items not in Scope of Specification

The following items are not explicitly supported via M-XIO specification:

| Function  |
|---|
| Power: Peripheral Module 12V Main, 3.3V Main, 3.3VAUX, etc.           |
| SAS / SATA  |
| x16 – to x4x4x4x4 on different destination cards                      |
| M-XIO use for external chassis cabling                                |
| Considerations for coupling to accelerator modules such as OAM or UBB |
| M-XIO cable hotplug, even in S5                                       |

**Table 1: Not Explicitly Supported via M-XIO**

#### 3.2 Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

Rack Compatibility  
Physical Spec  
Thermal Design  
Rear Side Power, I/O, Expansion  
Mechanical  
Onboard Power System  
Environmental Regulations/Requirements  
Prescribed Materials  
Software Support  
System Firmware  
Hardware Management  
Security



## 4. M-XIO Ports Overview

---

M-XIO “ports” (i.e., M-XIO connectors on a Host Processor Module (HPM)) contain a minimalist set of sideband signals which relies on circuitry to serialize/deserialize virtual wires that are tunneled over a 1-wire interface, called the “Modular-Peripheral Sideband Tunneling Interface” (M-PESTI).

This signal set, albeit minimalist in signal quantity, is an upgradable/pay-as-you-go hardware management architecture. This architecture propagates to/from many of today’s various peripheral modules and is fully extensible to accommodate more devices without adding physical signals/pins in a port. This management scheme is meant to withstand and manage several future generations of end-device upgrades/revisions with incremental firmware add-ons, where a “plug and extend” practice is leveraged.

### 4.1 M-XIO Port Requirements

A “port” refers to an IO connector on a Host Processor Module, intended to distribute PCIe/CXL lanes to devices.

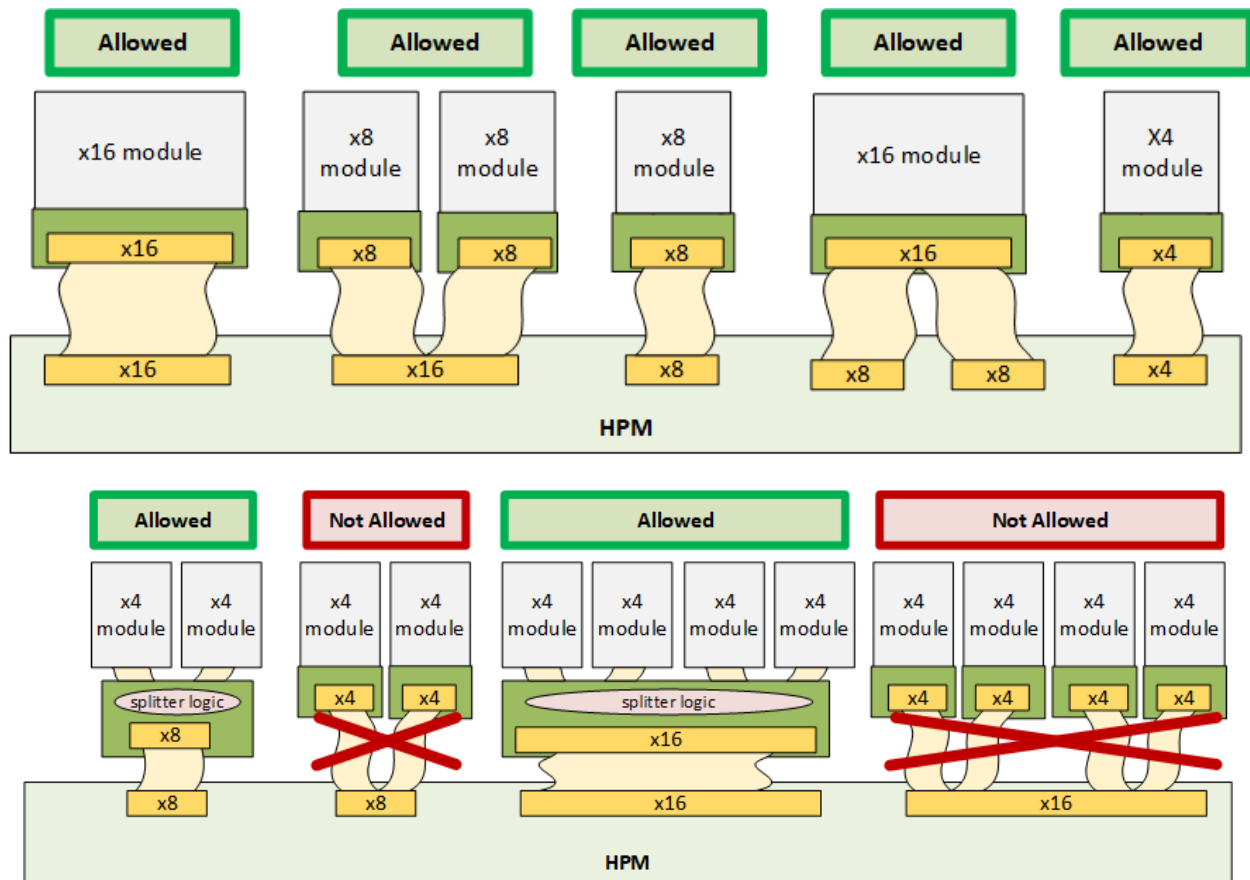
- A port may connect to the following:
  - o An “adaptor” that assists with power and sidebands prior to an end-point device (e.g., a “paddle-card”, a multi-cable connector)
  - o A carrier/module that accepts multiple devices/media (e.g., Riser with multiple CEM slots, EDSFF backplane)
- All ports must support connections that are cabled; direct riser connections are optional
- All ports must support link subdivision down to x1 (exceptions noted for specific downstream facing controllers/switches/re-timers, etc.). Note that this is a statement of the intent for cabled or direct PCIe riser connection flexibility but not indicative of the capabilities of the HPM downstream facing port (or root port) sourcing this connector.
- All ports support the below example of device form factors and /interposer categories. This is purely to illustrate some major use cases and does not imply the M-XIO spec fully teaches what destinations/interposers should do locally to achieve such functionality.
  - o PCIe CEM cards
  - o Open Compute Project NIC R3.0
  - o EDSFF devices, both NVMe (x4, x2, x1 in E.1 or E.3 form factors) and SCMs (storage class devices, such as CXL, x16, x8, x4)
  - o Backplanes with distribution to U.2 and EDSFF devices, both directly attached to root complexes or with PCIe switches in between
  - o Inline-able Host Bus Adapters or RAID controllers between HPM/Root ports and storage backplane for example
  - o x16 ports must be able to support a mixture of device/form-factor classes (x8 to CEM + x8 to EDSFF backplane)
- All ports are scalable with the use of switches.
- Allowance for recombining x4 and x8 ports sourced contiguously by the same x16 source complex.
- All multi-device modules (e.g., EDSFF backplane) and paddle-cards with circuitry must support a discovery mechanism.
- All x16 ports must duplicate all sidebands if desired to support x8x8 at two different PCB destinations (i.e. via a physical cable split) intended to maximize flexibility. It is not required for a x16 to duplicate sidebands if, for example, a user has a known system configuration and knows they will only connect a x16 m-xio port to a x16 destination.

### 4.2 M-XIO Connector and Cable Options

Even though any homogeneous combination of link subdivisions are possible, the only physical cable split allowed is a x16 source to x8x8 at different PCB destinations OR x8x8 sources that combine to a x16 destination, if and only if the x16 connector(s) are plumbed with a duplicate of the x8 sidebands. It is important to note that all x16 destinations supported in platforms that provide any x8 capable source (standalone or as part of a 2 in 1 connector) must assume that sidebands only exist on the lower x8

(PCIe lanes 0-7). Also care must be made to ensure that the lanes in the x8x8 are in contiguous order as half bus lane reversal is not supported by PCIe.

Note that the splitter logic depicted below is indicative of necessary sideband fanout circuits with optional selective remote and autonomous local controls. This is typically but not limited to PERST, clock and device presence fan out / in / masking, override, etc. and not pcie switch(es).



**Figure 2: M-XIO Connector and Cable Options**

*Note that HPM stands for Host Processor Module as an example configuration. M-XIO is not limited to HPMs sourcing the downstream facing ports to the M-XIO source connector(s). The above is not an exhaustive list of possible or not possible cable/connector configurations, it is just meant to showcase what are considered common configurations.*

### 4.3 M-XIO Sideband Scaling Strategy

M-XIO Sidebands are defined as Baseline and Extended groups, where x4 has Baseline only. x8 has Baseline plus extended sidebands. A HPM x16 source connector may be plumbed to duplicate all sidebands between the lower and upper x8 when maximum flexibility is desired such as splitting into x8x8 to different destination PCBs. Duplicating zero sidebands is acceptable when an HPM design is known to only need x16 interconnects to peripheral subsystems. Hybrids of duplicating some or excluding some interfaces is not advised.

# Common Cabled PCIe Sideband Scaling

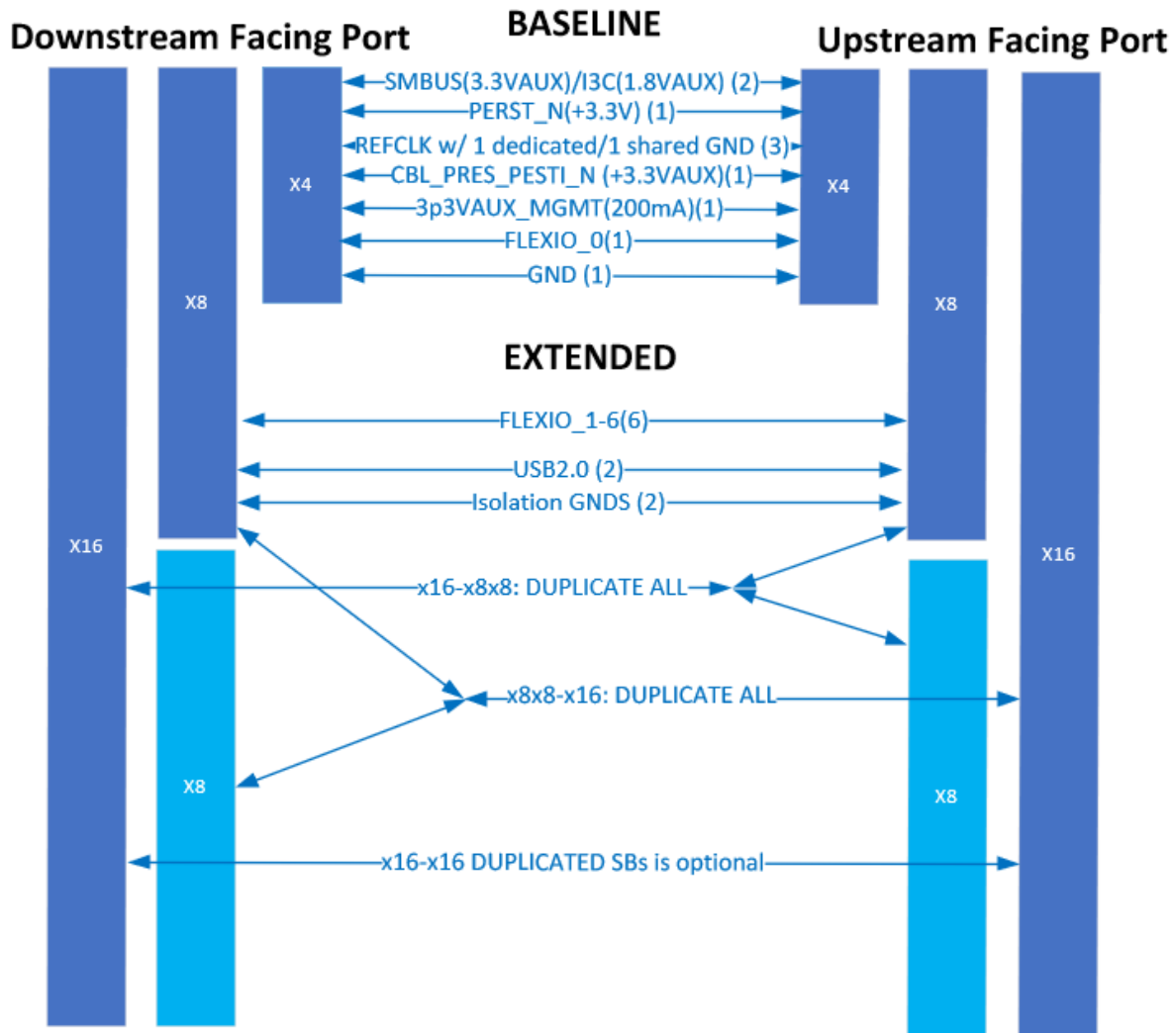


Figure 3: M-XIO sideband signal scale strategy

## 5. M-XIO Port Signal List

This chapter covers the signal summary and definitions for M-XIO ports. Signal directions (I/O) are with respect to the PCIe source (e.g., Downstream facing port such as a root complex on a HPM CPU socket). All signals are mandatory unless otherwise specified. Note that HPMs that are special purpose to support only x16 destinations may optionally choose to not connect the upper x8 sideband signals. Otherwise, duplicating the sidebands between a lower x8 and upper x8 connection section enables multi-cable/splits and/or multiple destinations/end-devices and/or reduced interposer fanout logic.

When baseline or extended signals are duplicated, such as in the x16 source to two x8 destinations on a different peripheral scenario, a signal name should insert A or B instance nomenclature after the primary function name and before polarity if applicable.

| Interface  | Signal Name      | Input/<br>Output<br>(HPM<br>Perspective) | Function   |
|--|------------------|--|--|
| PCIe   | PER[p/n]         | I  | PCIe RX Differential signals defined by the PCI Express Base Specification.  |
|  | PET[p/n]         | O  | PCIe TX Differential signals defined by the PCI Express Base Specification.  |
| Clocks   | REFCLK_D[p/n]    | O  | PCIe Reference Clock signals (100 MHz) defined by the PCI Express Base Specification.  |
| 2Wire Bus  | SMSCL / I3CSCL   | O  | SMBus Clock, Open Drain with pull-up on host. 3p3AUX_MGMT, Up to 400kHz. OR after discovery, I3C mode compliant with I3C Basic 1.1.1 @ +1.8VAUX; Note that this 2-wire bus is for the management (BMC) domain and not for Host domain (such as NVMe hotplug VPP, which can be performed via HPM FPGA emulation of hotplug I2C I/O expanders) |
|  | SMSDA / I3CSDA   | I/O                                      | SMBus Data, Same as above  |
| Reset  | PERST_N          | O  | Active low, push-pull at source. A discrete functional reset to the peripheral module(s) as defined as PERST# by the PCI Express Base Specification. Override, fanout or blocking logic may be needed on destination cards such as in hot plug applications.   |
| Destination card is attached + PESTI communication | CBL_PRES_PESTI_N | I/O                                      | Signal used to indicate the attachment of a cable assembly and/or a module to a port. Optional use as bi-directional interface for form-factor specific sideband-tunneling/virtual-wires. This signal does not indicate endpoint presence.   |
| Power and Grounds                                  | 3p3AUX_MGMT      | O  | Optional power for discovery on cables and interposers. If not used leave as not connected. Power limits are defined. Cross power domain isolation is the peripheral's duty and not explicitly defined here.   |
|  | GND              | O  | Isolation and return current path  |
| FLEXIO   | FLEXIO_[0:6]     | I/O                                      | Note: Implementers should note that some FLEXIO pins are pinned out as being high speed differential friendly for the best possible future proofing of future high speed interfaces. Example FLEXIO functions may be INT, Device presence, PWRBRK, etc. when PESTI is not used.  |
| USB 2  | USB2[p/n]        | I/O                                      | Universal Serial Bus 2.0 (meaning High Speed or Full Speed, but not Low Speed from USB 1.1)  |

Table 2: M-XIO Port Signal List

### 5.1 Power and Grounds

The M-XIO source connector optionally supports a 3p3AUX\_MGMT power source to provide a limited 200mA of trickle power for discovery logic only, such as for FRU and cable identification. Cross power domain isolation is the duty of the peripheral/ interposer and not explicitly defined here.

3p3AUX\_MGMT is enabled before de-assertion of PCIe Reset and PCIe clock activation. This power is NOT to be used by end form factor peripherals such as a PCIe CEM slots' pin B10 AUX power.

See the [Power Supply Requirements section](#) of this specification for electrical characteristics.

## 5.2 High Speed PCIe Signals

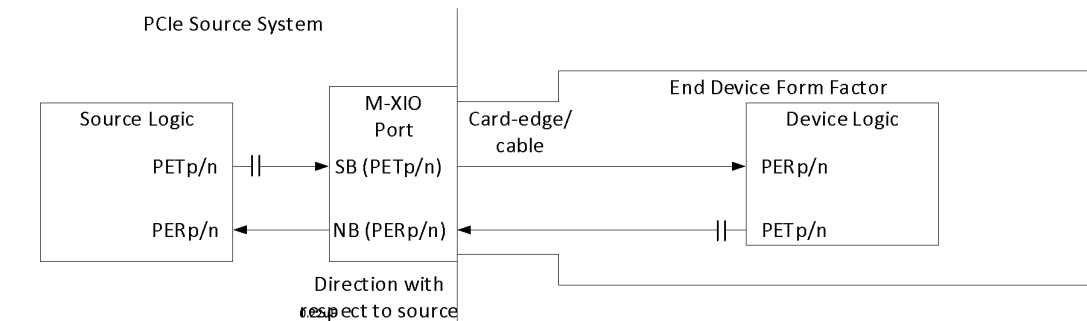
An M-XIO compliant source connector implements a minimum of four PCIe lanes, with link subdivision support down to X1. A lane consists of an input and output differential pair. Additional lanes are optional. Refer to the PCI Express Base Specification for more details on the functional requirements of the interface signals.

The PET signals on the host shall connect to the PET[p/n] signals on the connector and the PER signals on the Peripheral Module Logic. The PER signals on the host shall connect to the PER[p/n] signals on the connector and the PET signals on the Peripheral Module Logic. For a high-level wiring diagram, see Figure 4.

Lane Polarity Inversion is optional at a M-XIO port depending on host and end-device requirements. Polarity inversion is used to simplify host and device PCB trace routing constraints.

Lane reversal may be supported on both the host and device. If it is supported, then the transmitting and receiving lanes can be connected using reverse ordering at a M-XIO port. It is required that on the source side, any lane reversals match contiguously if the port is subdivided in any fashion (e.g. x4x4 at the source cannot lane reverse only one x4 and expect the same connector to work when link subdivided as one X8).

Lane speed: It is expected that the self-describing I/O (e.g., a paddle/interposer or cable identification) provide information to the system (BIOS and firmware) to cap training speeds when any channel element cannot guarantee the max speed of the entire channel. M-XIO port specification is intended as PCIe speed/generation neutral. For more details regarding self-describing IO refer to the M-PESTI specification.



**Figure 4: M-XIO Port Example – PET and PER**

## 5.3 PCIe Reference Clock

The REFCLK\_D[p/n] signals are used to assist the synchronization of legacy devices' PCI Express interface timing circuits with no SRIS/SRNS support. Refer to the PCI Express Card Base Specification for more details on the functional and tolerance requirements for the reference clock signals.

All M-XIO ports implement REFCLK\_D[p/n]. If an end-device needs physical clock signals and supports bifurcation/lane-subdivision/dual-port mode, then the intermediary-board/paddle-card may buffer/fanout the remaining REFCLK signals. REFCLK\_D[p/n] signals are required at every M-XIO port.

If SRIS or SRNS is supported by both the system and the device, then a reference clock is still required at the source connector. The required reference clock helps enable homogenous/universal M-XIO ports to enable a wide variety of peripheral hardware (i.e., multiple peripheral module connectivity enabled with any M-XIO port). Device's negotiating or entering SRIS/SRNS mode is outside the scope of this specification version.

It is optional and generally recommended that there are no free running clocks into missing or disabled peripheral modules. Methods for disabling clocks at the source or destination are out of scope for this documentation. For unused clocks, it is optional and recommended, in most cases, that the end-device/paddle-card/intermediary-board terminates the reference clock signals at the closest coupled connector/termination/PCB.

## 5.4 PCIe Reset

All M-XIO ports shall implement PERST0\_N for fundamental reset. Refer to the PCI Express Base Specification for more details on the functional requirements of PERST#.

## 5.5 2-wire Interface

### 5.5.1 SMBUS Mode

The SMBus interface shall be implemented within the baseline sidebands for all M-XIO (cabled PCIe) ports. The interface must default to SMBUS 3.1 compliant, 3.3VAUX, open drain mode. The pull-ups (~2.2KΩ) for SMSDA and SMSCL are required on the upstream system to ensure no floating inputs and proper bus operation. Note that 400KHz SMBUS support @ 3.3VAUX is required.

The destination subsystem is responsible for 1) electrical protection of local circuitry if say the peripheral/subsystem is unpowered, 2) any cross power domain isolation (such as when connecting MAIN powered only targets to the upstream AUX powered bus) and 3) any necessary voltage level translation in SMBUS mode.

Since the SMBUS interface often extends to legacy form factors that allow for any target address, it is imperative that the HPM not have any upstream targets on the bus where such addresses traverse the M-XIO. This could lead to addressing conflicts.

### 5.5.2 I3C Mode

I3C Basic 1.1.1 compliant mode of operation is optionally supportable on the 2 wire interface. Great care must be taken by system designers to ensure proper logical and electrical operation of this bus

All directly attached I3C capable targets must be +3.3V tolerant for the discovery phase.

Although supported in I3C Basic 1.1.1 with constraints such as glitch filtering and prohibiting clock stretching, for the sub-segment traversing M-XIO, SMBUS and I3C device mixing on the same bus is prohibited.

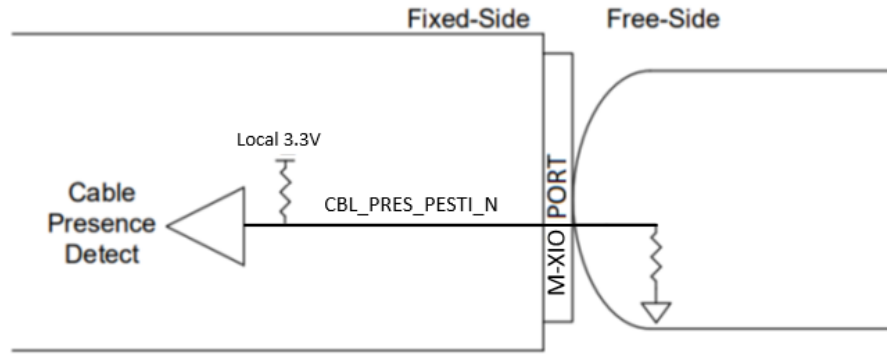
The I3C mode required low voltage is 1.8V. Exactly one low voltage level, such as 1.8V, must be the same on all downstream (sub)segment instances, including throughout the bus from initiator to the final target. This is because the I3C hub definition requires the same push-pull mode voltage level on the upstream and downstream subsegments.

Note: It is beyond the scope of this specification to dictate precise margin allowances on parameters like capacitance, or bus length for the 2-wire interface running in SMBUS mode or I3C Basic mode.

## 5.6 Cable Present Detect & M-PESTI

A cable assembly presence detection mechanism is specified and required through CBL\_PRES\_PESTI\_N to indicate the attachment of a cable assembly and/or a peripheral card to a fixed-side module (e.g., HPM PCB) with PCIe downstream facing port. If not using the optional Peripheral Sideband Tunneling Interface (M-PESTI) functionality, then the free-side (Cable/Interposer Side) should assert this signal low to indicate cable attachment, see figure below. It is recommended that it is asserted with a pull-down (< 500Ω) or an active driver. The fixed-side should provide a pull-up resistor (>7.5KΩ & < 200KΩ) on CBL\_PRES\_PESTI\_N to System V\_3P3\_AUX typically sourced via 12V\_PRIMARY and enabled in S5 (i.e before S0) to passively de-assert CBL\_PRES\_PESTI\_N. However, to implement the

optional Peripheral Sideband Tunneling Interface functionality of this signal please refer to the M-PESTI specification.



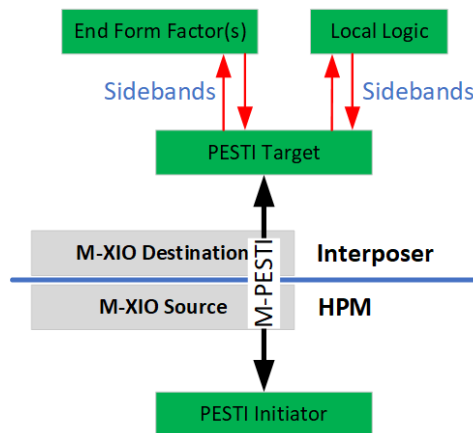
**Figure 5: CBL\_PRES\_PESTI\_N Circuit (when PESTI is not supported at the destination)**

### 5.6.1 PCIe Sideband Tunneling Interface (M-PESTI)

The CBL\_PRES\_PESTI\_N may also be used as dual-purpose, bidirectional M-PESTI wire where custom, standard, or future form-factor-specific sidebands become Virtual Wires (vWires).

- Supports bidirectional, low-latency, real-time virtual wires over this point-to-point interface between real-time link partners (CPLD/MCU/ASIC) without the loss of basic presence.
- Decouples wires from higher level management operations like MCTP better suited for I2C and non-real time handlers.
- Payload + protocol contains self-describing I/O fields + virtual wires that surface as real or terminate as bidirectional control/status.
- Future extensibility from cabled interposers to include peripheral modules over device presence wires. Carrier card / nested target handling is feasible.
- Includes update & optional immutable attestation of the out of band link partner's FW.

Reference M-PESTI spec for more details.



**Figure 6: Example PESTI usage at destination**



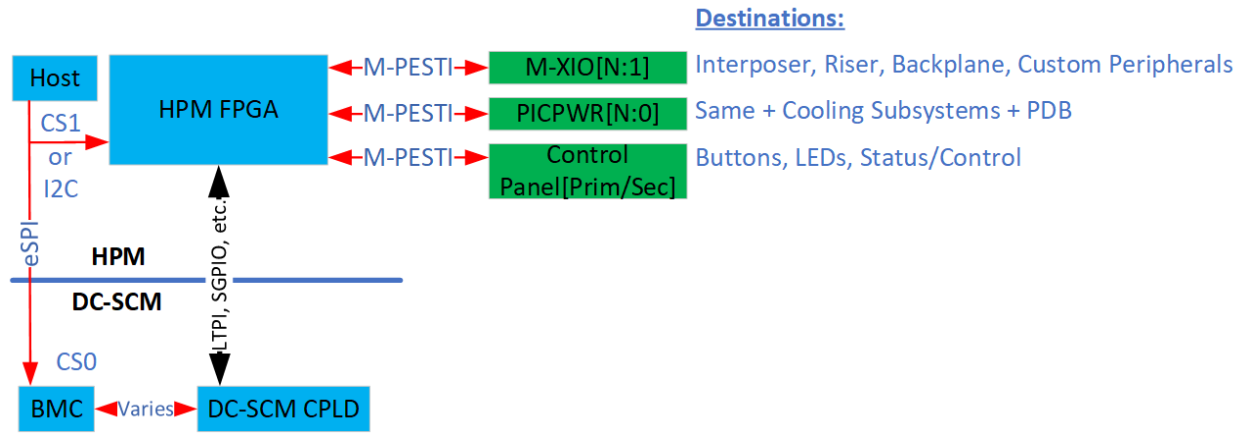


Figure 7: Example PESTI usage at destination

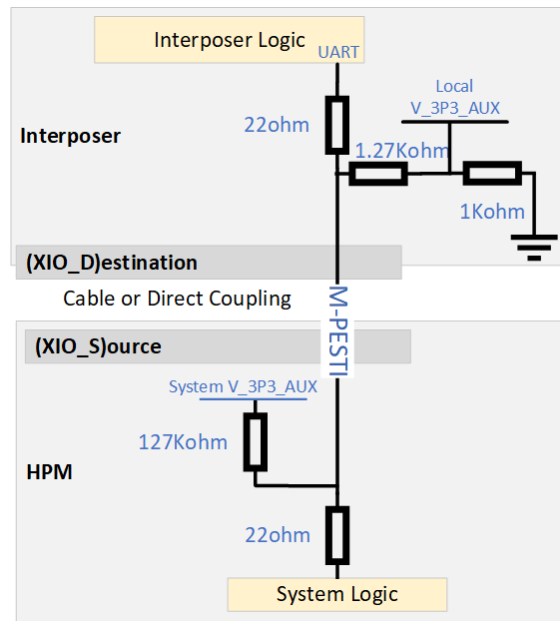


Figure 8: CBL PRES\_PESTI\_N Example Diagram – PESTI functionality

| <u>Interposer/Target State</u> | <u>PESTI Initiator Observation</u>                                     |
|--------------------------------|--|
| 1) Nothing installed           | Sees logic high  |
| 2) Present + No power          | Bleed resistor pulls PESTI low; Assumes no local power                 |
| 3) Power + Target HW Default   | Target powered; HW defaults HiZ to induce rising edge; CMDs are NACKed |
| 4) Power + Target app code     | Target issues break (low pulse), then listens for incoming CMDs        |

Table 3: Expected PESTI Signal States

## 5.7 Flexible I/O

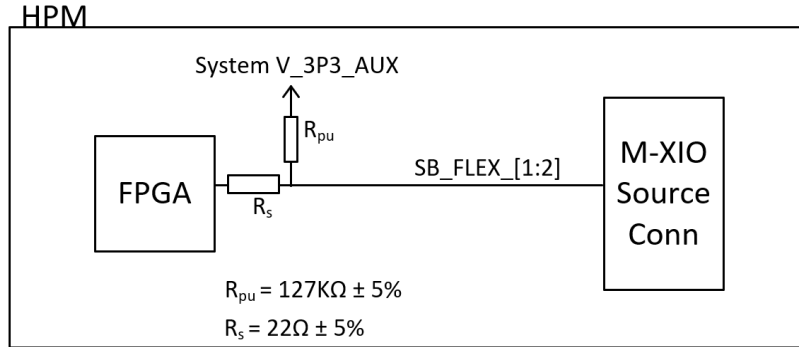
Due to the variable nature of system needs, M-XIO defines 7 signals within the baseline and extended sideband region, FLEXIO\_[0:6]. There are assigned pins such that high speed differential links are



acceptable for these interfaces because they are surrounded by isolation grounds on the pinouts, but these do not need to be routed differentially on the HPM.

Flex I/O pins are configurable for different modes based on negotiation between the entities on either side of the cable. By default, FLEXIO\_[1:2] signals must be pulled up to system V\_3P3\_AUX typically sourced via 12V\_PRIMARY and enabled in S5 (i.e. before S0), see figure 9.

For FLEXIO\_[1:2] the assumption is the default state until negotiation has happened and both HPM and paddle card have agreed on sideband usage. The mechanism of negotiation is out of the scope of this specification but could be done by either 2 wire management bus or 1 wire management bus.



**Figure 9: SB\_FLEX[1:2] Default Configuration**

For FLEXIO\_[0,3:6] no bias is allowed at the M-XIO interface until after the discovery phase which guarantees electrically safe plug-ins, power-ups, etc. as relevant to these flex signals. FLEXIO\_[0,3:6] are also assumed to take on functions as needed only after negotiation between HPM and paddle card have agreed on sideband usage. FLEXIO\_[0,3:6] are not required to default connect to an HPM FPGA unlike FLEXIO\_[1:2].

| Signal name | Default initialization | Comments   |
|-------------|------------------------|--|
| FLEXIO_0    | No Function & No Bias  | Single Ended Optimized From M-XIO Pinout Perspective             |
| FLEXIO_1    | SB_FLEX_1              | Differentially Coupled to FLEXIO_2 From M-XIO Pinout Perspective |
| FLEXIO_2    | SB_FLEX_2              | Differentially Coupled to FLEXIO_1 From M-XIO Pinout Perspective |
| FLEXIO_3    | No Function & No Bias  | Differentially Coupled to FLEXIO_4 From M-XIO Pinout Perspective |
| FLEXIO_4    | No Function & No Bias  | Differentially Coupled to FLEXIO_3 From M-XIO Pinout Perspective |
| FLEXIO_5    | No Function & No Bias  | Differentially Coupled to FLEXIO_6 From M-XIO Pinout Perspective |
| FLEXIO_6    | No Function & No Bias  | Differentially Coupled to FLEXIO_5 From M-XIO Pinout Perspective |

**Table 4: M-XIO's flexible I/O Selection Table**

## 5.8 USB 2.0

M-XIO USB 2.0 high-speed management interface shall be on the BMC domain (e.g. direct or bridged NC-SI RBT replacement, Smart NIC management, fast image management to add-in cards, bridges, etc.). The USB host(s) are to be on the M-XIO source connector side and not on the peripheral module (USB device side). On-the-go host negotiation is not expected to be needed.

For USB electrical requirements refer to the Universal Serial Bus 2.0 (meaning High Speed or Full Speed, but not Low Speed from USB 1.1). The method to interface USB2 to CEM cards is described in the PCI SIG CEM 5.0 proposal.

USB 2.0 is only required for certain connector widths and certain subsections, refer to connector pinouts for more details.

A x16 is allowed to provide only 1 set of baseline sidebands on the lower x8 IF the system (HPM and peripheral) knowingly will not split the connections between different peripheral subsystems (e.g. need  $\geq 1$  set of sidebands / fanout / splitter logic). Only when you need a generic option to split x16 to separate subsystems should baseline sidebands be duplicated in the upper x8. USB was decided to be an exceptional extended sideband interface that is not required in the upper x8 for the reasons mentioned above.

## 6. Electrical Requirements

This chapter covers the electrical requirements of an M-XIO port. Unless otherwise specified, follow the PCI Express Card Electromechanical Specification.

### 6.1 Power Supply Requirements

#### 6.1.1 3p3AUX\_MGMT Power Supply Requirements

| Reference                          | Parameter  | Value       | Unit | Comment                |
|------------------------------------|--|-------------|------|------------------------|
| 3p3AUX_MGMT tolerance              | 3p3AUX_MGMT supply tolerance   | 3.3V +/- 5% | V    |                        |
| 3p3AUX_MGMT Maximum Supply Current | 3p3AUX_MGMT maximum allowed current through each M-XIO port that the supply must provide | 200         | mA   | Maximum Supply Current |

**Table 5: 3p3AUX\_MGMT Power Supply Requirements**

#### 6.1.2 3.3V Logic Signal Requirements

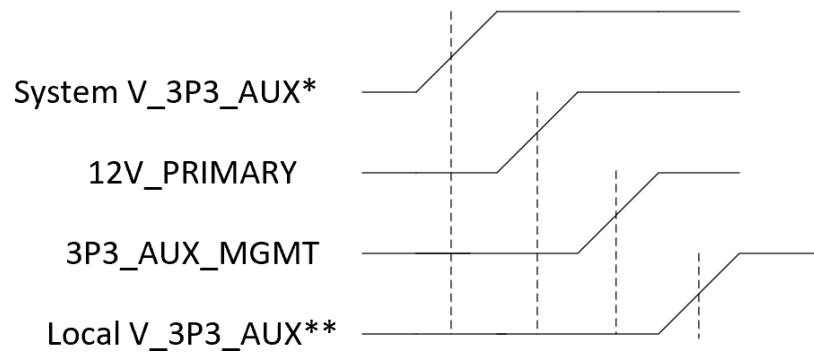
The M-XIO port logic levels for single-ended digital signals (PERST[B:A]\_N, CBL\_PRES[B:A]\_PESTI[B:A]\_N) and FLEXIO\_[1:2] are defined in the table directly below. For SMBus signals (SMCLK, SMSDA) logic levels, refer to the System Management Bus (SMBus) Specification, Version 3.1 unless otherwise specified. For USB, reference Universal Serial Bus Specification. Inputs and outputs are referenced from the signal destination's standpoint.

**DC Specification for 3.3 V Logic Signaling**

| Symbol | Parameter                 | Min   | Max   | Unit | Notes |
|--------|---------------------------|-------|-------|------|-------|
| Vddsmb | SMBus Nominal bus voltage | 3.135 | 3.465 | V    |       |
| Vih    | Input High Voltage        | 2.0   | 3.465 | V    |       |
| Vil    | Input Low Voltage         | -0.3  | 0.8   | V    |       |
| Voh    | Output High Voltage       |       | 3.465 | V    |       |
| Vol    | Output Low Voltage        |       | 0.2   | V    |       |

**Table 6: 3.3V Logic Signal Requirements**

### 6.1.3 Power Sequencing



\*System V\_3P3\_AUX is typically sourced via 12V\_PRIMARY; however, System V3P3\_AUX can be up before 12V\_PRIMARY and sourced via +12V\_STBY from CRPS for various purposes.

\*\*Local V\_3P3\_AUX here is referencing the 3P3\_AUX rail located on intermediary boards and/or at peripheral device.

**Figure 10: Recommended Power Sequencing**

## 7. Connectors & Pinout

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For connectors referenced, these part-numbers/standards-references are current as of publication, please refer to connector vendors or [Current Connector List](#) for part numbers that best meet the application.

The below M-XIO connector requirements are intended to enhance cross compatibility between HPM and peripheral module subsystems by limiting connector options. These requirements also help prevent M-XIO from going stale when new and better connector designs are released into the market showing new connectors can be added while also filtering out exotic connector solutions.

### Minimum connector requirements:

1. Correct number of pins to meet M-XIO high-speed and sideband requirements.
2. Supports cabled or directly-coupled subsystems, based on connector/cable capabilities and platform needs.
3. Support 30AWG or larger diameter twin-ax dual-drain cable.
4. Meets minimum SI capability metric/standard including any additional paddle design when used in a cabled application.
5. Multi-sourced.

### Pinouts:

Users should take care of (cable / connector mating) adjustments required for mechanical and electrical (diff pair) compliance. All PCIe TX/RX (PET/PER) are from the perspective of the downstream source port (i.e. HPM's perspective).

## 7.1 SFF-TA-1016

Both cabled and card edge interconnection is assumed for SFF-TA-1016. M-XIO pinout attempts to follow the physical connector construction (i.e. connector datasheet with A1 at top left).

Only 38, 74 and 148 pin versions of the connector are listed for maximum flexibility.

The 124-pin option is not recommended since it does not have enough pins to enable 2x8 mode with all required sideband signals.

Separate power connector is required for both cabled or card edge cases unless using an M-XIO connector with integrated power. Refer to M-PIC specification for more details on power connectors, signal lists, and pinout.

### 7.1.1 x4 M-XIO Source Connector Pinout (SFF-TA-1016)

Assumes x4 SFF-TA-1016 (MCIO) – 38 Pins

*Pinout Update v1.0*

| Pin | Signal      | Signal               | Pin |
|-----|-------------|----------------------|-----|
| A1  | GND         | GND                  | B1  |
| A2  | PERp0       | PETp0                | B2  |
| A3  | PERn0       | PETn0                | B3  |
| A4  | GND         | GND                  | B4  |
| A5  | PERp1       | PETp1                | B5  |
| A6  | PERn1       | PETn1                | B6  |
| A7  | GND         | GND                  | B7  |
| A8  | 3p3AUX_MGMT | SMSCL_A              | B8  |
| A9  | FLEXIO0_A   | SMSDA_A              | B9  |
| A10 | GND         | GND                  | B10 |
| A11 | REFCLK_A_Dp | PERST_A_N            | B11 |
| A12 | REFCLK_A_Dn | CBL_PRES_A_PESTI_A_N | B12 |
| A13 | GND         | GND                  | B13 |
| A14 | PERp2       | PETp2                | B14 |
| A15 | PERn2       | PETn2                | B15 |
| A16 | GND         | GND                  | B16 |
| A17 | PERp3       | PETp3                | B17 |
| A18 | PERn3       | PETn3                | B18 |
| A19 | GND         | GND                  | B19 |

## 7.1.2 x8 M-XIO Source Connector Pinout (SFF-TA-1016)

Assumes x8 SFF-TA-1016 – 74 Pins

*Revision v1.0*

| Pin | Signal      | Signal               | Pin |
|-----|-------------|----------------------|-----|
| A1  | GND         | GND                  | B1  |
| A2  | PERp0       | PETp0                | B2  |
| A3  | PERn0       | PETn0                | B3  |
| A4  | GND         | GND                  | B4  |
| A5  | PERp1       | PETp1                | B5  |
| A6  | PERn1       | PETn1                | B6  |
| A7  | GND         | GND                  | B7  |
| A8  | 3p3AUX_MGMT | SMSCL_A              | B8  |
| A9  | FLEXIO0_A   | SMSDA_A              | B9  |
| A10 | GND         | GND                  | B10 |
| A11 | REFCLK_A_Dp | PERST_A_N            | B11 |
| A12 | REFCLK_A_Dn | CBL_PRES_A_PESTI_A_N | B12 |
| A13 | GND         | GND                  | B13 |
| A14 | PERp2       | PETp2                | B14 |
| A15 | PERn2       | PETn2                | B15 |
| A16 | GND         | GND                  | B16 |
| A17 | PERp3       | PETp3                | B17 |
| A18 | PERn3       | PETn3                | B18 |
| A19 | GND         | GND                  | B19 |
| A20 | PERp4       | PETp4                | B20 |
| A21 | PERn4       | PETn4                | B21 |
| A22 | GND         | GND                  | B22 |
| A23 | PERp5       | PETp5                | B23 |
| A24 | PERn5       | PETn5                | B24 |
| A25 | GND         | GND                  | B25 |
| A26 | FLEXIO1_A   | FLEXIO3_A            | B26 |
| A27 | FLEXIO2_A   | FLEXIO4_A            | B27 |
| A28 | GND         | GND                  | B28 |
| A29 | USB2_A_Dp   | FLEXIO5_A            | B29 |
| A30 | USB2_A_Dn   | FLEXIO6_A            | B30 |
| A31 | GND         | GND                  | B31 |
| A32 | PERp6       | PETp6                | B32 |
| A33 | PERn6       | PETn6                | B33 |
| A34 | GND         | GND                  | B34 |
| A35 | PERp7       | PETp7                | B35 |
| A36 | PERn7       | PETn7                | B36 |
| A37 | GND         | GND                  | B37 |

### 7.1.3 x16 M-XIO Source Connector Pinout (SFF-TA-1016)

Assumes x16 SFF-TA-1016 – 148 Pins

*Pinout Update v1.0*

| Pin | Signal      | Signal               | Pin |
|-----|-------------|----------------------|-----|
| A1  | GND         | GND                  | B1  |
| A2  | PERp0       | PETp0                | B2  |
| A3  | PERn0       | PETn0                | B3  |
| A4  | GND         | GND                  | B4  |
| A5  | PERp1       | PETp1                | B5  |
| A6  | PERn1       | PETn1                | B6  |
| A7  | GND         | GND                  | B7  |
| A8  | 3p3AUX_MGMT | SMSCL_A              | B8  |
| A9  | FLEXIO0_A   | SMSDA_A              | B9  |
| A10 | GND         | GND                  | B10 |
| A11 | REFCLK_A_Dp | PERST_A_N            | B11 |
| A12 | REFCLK_A_Dn | CBL_PRES_A_PESTI_A_N | B12 |
| A13 | GND         | GND                  | B13 |
| A14 | PERp2       | PETp2                | B14 |
| A15 | PERn2       | PETn2                | B15 |
| A16 | GND         | GND                  | B16 |
| A17 | PERp3       | PETp3                | B17 |
| A18 | PERn3       | PETn3                | B18 |
| A19 | GND         | GND                  | B19 |
| A20 | PERp4       | PETp4                | B20 |
| A21 | PERn4       | PETn4                | B21 |
| A22 | GND         | GND                  | B22 |
| A23 | PERp5       | PETp5                | B23 |
| A24 | PERn5       | PETn5                | B24 |
| A25 | GND         | GND                  | B25 |
| A26 | FLEXIO1_A   | FLEXIO3_A            | B26 |
| A27 | FLEXIO2_A   | FLEXIO4_A            | B27 |
| A28 | GND         | GND                  | B28 |
| A29 | USB2_A_Dp   | FLEXIO5_A            | B29 |
| A30 | USB2_A_Dn   | FLEXIO6_A            | B30 |
| A31 | GND         | GND                  | B31 |
| A32 | PERp6       | PETp6                | B32 |
| A33 | PERn6       | PETn6                | B33 |
| A34 | GND         | GND                  | B34 |
| A35 | PERp7       | PETp7                | B35 |
| A36 | PERn7       | PETn7                | B36 |
| A37 | GND         | GND                  | B37 |
| A38 | GND         | GND                  | B38 |
| A39 | PERp8       | PETp8                | B39 |
| A40 | PERn8       | PETn8                | B40 |
| A41 | GND         | GND                  | B41 |
| A42 | PERp9       | PETp9                | B42 |
| A43 | PERn9       | PETn9                | B43 |
| A44 | GND         | GND                  | B44 |
| A45 | 3p3AUX_MGMT | SMSCL_B              | B45 |



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|     |             |                      |     |
|-----|-------------|----------------------|-----|
| A46 | FLEXIO0_B   | SMSDA_B              | B46 |
| A47 | GND         | GND                  | B47 |
| A48 | REFCLK_B_Dp | PERST_B_N            | B48 |
| A49 | REFCLK_B_Dn | CBL_PRES_B_PESTI_B_N | B49 |
| A50 | GND         | GND                  | B50 |
| A51 | PERp10      | PETp10               | B51 |
| A52 | PERn10      | PETn10               | B52 |
| A53 | GND         | GND                  | B53 |
| A54 | PERp11      | PETp11               | B54 |
| A55 | PERn11      | PETn11               | B55 |
| A56 | GND         | GND                  | B56 |
| A57 | PERp12      | PETp12               | B57 |
| A58 | PERn12      | PETn12               | B58 |
| A59 | GND         | GND                  | B59 |
| A60 | PERp13      | PETp13               | B60 |
| A61 | PERn13      | PETn13               | B61 |
| A62 | GND         | GND                  | B62 |
| A63 | FLEXIO1_B   | FLEXIO3_B            | B63 |
| A64 | FLEXIO2_B   | FLEXIO4_B            | B64 |
| A65 | GND         | GND                  | B65 |
| A66 | USB2_B_Dp   | FLEXIO5_B            | B66 |
| A67 | USB2_B_Dn   | FLEXIO6_B            | B67 |
| A68 | GND         | GND                  | B68 |
| A69 | PERp14      | PETp14               | B69 |
| A70 | PERn14      | PETn14               | B70 |
| A71 | GND         | GND                  | B71 |
| A72 | PERp15      | PETp15               | B72 |
| A73 | PERn15      | PETn15               | B73 |
| A74 | GND         | GND                  | B74 |

## 7.2 SFF-TA-1033

Refer to connector manufacturer(s) for connector collateral. If using this connector with only a single x8 instead of the full x16 capability, then that single x8 and associated sideband signal set must route through the pin section 'L\_x', i.e. closest to the power section. This is similar to PCI-SIG CEM slot pinout where the lower x8 lanes are closest to the power section.

### Pinout Update v1.0

| Pin            | Signal   | Signal      | Pin   |
|----------------|--|-------------|-------|
| PB2            | 12V_PRIMARY  | 12V_PRIMARY | PA2   |
| PB1            | GND  | GND         | PA1   |
| SB6            | Refer to the latest M-PIC spec for more pinout details in this block |             | SA6   |
| SB5            |  |             | SA5   |
| SB4            |  |             | SA4   |
| SB3            |  |             | SA3   |
| SB2            |  |             | SA2   |
| SB1            |  |             | SA1   |
| Mechanical Key |  |             |       |
| L_B37          | GND  | GND         | L_A37 |
| L_B36          | PETn0  | PERn0       | L_A36 |
| L_B35          | PETp0  | PERp0       | L_A35 |
| L_B34          | GND  | GND         | L_A34 |
| L_B33          | PETn1  | PERn1       | L_A33 |
| L_B32          | PETp1  | PERp1       | L_A32 |
| L_B31          | GND  | GND         | L_A31 |
| L_B30          | FLEXIO6_A  | USB2_A_Dn   | L_A30 |
| L_B29          | FLEXIO5_A  | USB2_A_Dp   | L_A29 |
| L_B28          | GND  | GND         | L_A28 |
| L_B27          | FLEXIO4_A  | FLEXIO2_A   | L_A27 |
| L_B26          | FLEXIO3_A  | FLEXIO1_A   | L_A26 |
| L_B25          | GND  | GND         | L_A25 |
| L_B24          | PETn2  | PERn2       | L_A24 |
| L_B23          | PETp2  | PERp2       | L_A23 |
| L_B22          | GND  | GND         | L_A22 |
| L_B21          | PETn3  | PERn3       | L_A21 |
| L_B20          | PETp3  | PERp3       | L_A20 |
| L_B19          | GND  | GND         | L_A19 |
| L_B18          | PETn4  | PERn4       | L_A18 |
| L_B17          | PETp4  | PERp4       | L_A17 |
| L_B16          | GND  | GND         | L_A16 |
| L_B15          | PETn5  | PERn5       | L_A15 |
| L_B14          | PETp5  | PERp5       | L_A14 |

|                |                    |             |       |
|----------------|--------------------|-------------|-------|
| L_B13          | GND                | GND         | L_A13 |
| L_B12          | CBL_PREA_PESTI_A_N | REFCLK_A_Dn | L_A12 |
| L_B11          | PERST_A_N          | REFCLK_A_Dp | L_A11 |
| L_B10          | GND                | GND         | L_A10 |
| L_B9           | SMSDA_A            | FLEXIO0_A   | L_A9  |
| L_B8           | SMSCL_A            | 3p3AUX_MGMT | L_A8  |
| L_B7           | GND                | GND         | L_A7  |
| L_B6           | PETn6              | PERn6       | L_A6  |
| L_B5           | PETp6              | PERp6       | L_A5  |
| L_B4           | GND                | GND         | L_A4  |
| L_B3           | PETn7              | PERn7       | L_A3  |
| L_B2           | PETp7              | PERp7       | L_A2  |
| L_B1           | GND                | GND         | L_A1  |
| Mechanical Key |                    |             |       |
| U_B37          | GND                | GND         | U_A37 |
| U_B36          | PETn8              | PERn8       | U_A36 |
| U_B35          | PETp8              | PERp8       | U_A35 |
| U_B34          | GND                | GND         | U_A34 |
| U_B33          | PETn9              | PERn9       | U_A33 |
| U_B32          | PETp9              | PERp9       | U_A32 |
| U_B31          | GND                | GND         | U_A31 |
| U_B30          | FLEXIO6_B          | USB2_B_Dn   | U_A30 |
| U_B29          | FLEXIO5_B          | USB2_B_Dp   | U_A29 |
| U_B28          | GND                | GND         | U_A28 |
| U_B27          | FLEXIO4_B          | FLEXIO2_B   | U_A27 |
| U_B26          | FLEXIO3_B          | FLEXIO1_B   | U_A26 |
| U_B25          | GND                | GND         | U_A25 |
| U_B24          | PETn10             | PERn10      | U_A24 |
| U_B23          | PETp10             | PERp10      | U_A23 |
| U_B22          | GND                | GND         | U_A22 |
| U_B21          | PETn11             | PERn11      | U_A21 |
| U_B20          | PETp11             | PERp11      | U_A20 |
| U_B19          | GND                | GND         | U_A19 |
| U_B18          | PETn12             | PERn12      | U_A18 |
| U_B17          | PETp12             | PERp12      | U_A17 |
| U_B16          | GND                | GND         | U_A16 |
| U_B15          | PETn13             | PERn13      | U_A15 |
| U_B14          | PETp13             | PERp13      | U_A14 |
| U_B13          | GND                | GND         | U_A13 |
| U_B12          | CBL_PREB_PESTI_B_N | REFCLK_B_Dn | U_A12 |

|       |           |             |       |
|-------|-----------|-------------|-------|
| U_B11 | PERST_B_N | REFCLK_B_Dp | U_A11 |
| U_B10 | GND       | GND         | U_A10 |
| U_B9  | SMSDA_B   | FLEXIO0_B   | U_A9  |
| U_B8  | SMSCL_B   | 3p3AUX_MGMT | U_A8  |
| U_B7  | GND       | GND         | U_A7  |
| U_B6  | PETn14    | PERn14      | U_A6  |
| U_B5  | PETp14    | PERp14      | U_A5  |
| U_B4  | GND       | GND         | U_A4  |
| U_B3  | PETn15    | PERn15      | U_A3  |
| U_B2  | PETp15    | PERp15      | U_A2  |
| U_B1  | GND       | GND         | U_A1  |

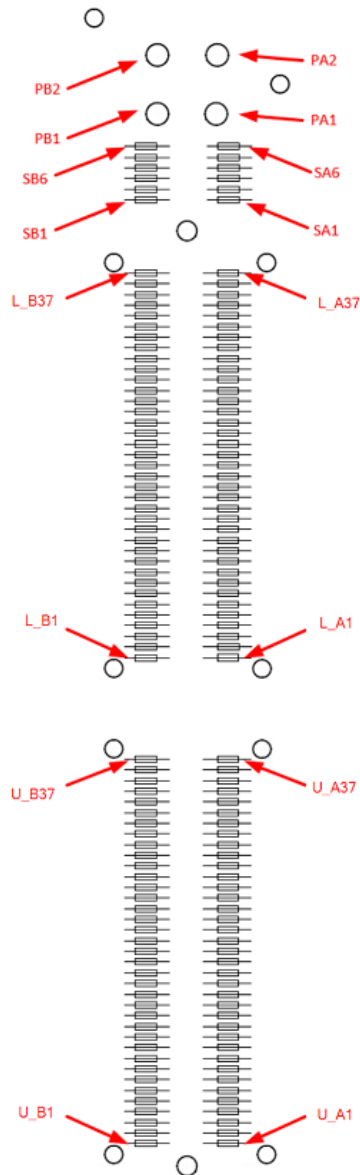


Figure 11: SFF-TA-1033 – Pinout Configuration

## 7.3 SFF-TA-1026

*Pinout Update v1.0*

| Pin | Signal               | Signal    | Pin |
|-----|----------------------|-----------|-----|
| 1   | GND                  | GND       | 72  |
| 2   | PERp0                | PETp0     | 71  |
| 3   | PERn0                | PETn0     | 70  |
| 4   | GND                  | GND       | 69  |
| 5   | PERp1                | PETp1     | 68  |
| 6   | PERn1                | PETn1     | 67  |
| 7   | GND                  | GND       | 66  |
| 8   | PERp2                | PETp2     | 65  |
| 9   | PERn2                | PETn2     | 64  |
| 10  | GND                  | GND       | 63  |
| 11  | PERp3                | PETp3     | 62  |
| 12  | PERn3                | PETn3     | 61  |
| 13  | GND                  | GND       | 60  |
| 14  | PERp4                | PETp4     | 59  |
| 15  | PERn4                | PETn4     | 58  |
| 16  | GND                  | GND       | 57  |
| 17  | PERp5                | PETp5     | 56  |
| 18  | PERn5                | PETn5     | 55  |
| 19  | GND                  | GND       | 54  |
| 20  | PERp6                | PETp6     | 53  |
| 21  | PERn6                | PETn6     | 52  |
| 22  | GND                  | GND       | 51  |
| 23  | PERp7                | PETp7     | 50  |
| 24  | PERn7                | PETn7     | 49  |
| 25  | GND                  | GND       | 48  |
| 26  | REFCLK_A_Dp          | USB2_A_Dp | 47  |
| 27  | REFCLK_A_Dn          | USB2_A_Dn | 46  |
| 28  | GND                  | GND       | 45  |
| 29  | GND                  | GND       | 44  |
| 30  | CBL_PRES_A_PESTI_A_N | FLEXIO1_A | 43  |
| 31  | SMSCL_A              | FLEXIO2_A | 42  |
| 32  | SMSDA_A              | GND       | 41  |
| 33  | GND                  | GND       | 40  |
| 34  | PERST_A_N            | FLEXIO3_A | 39  |
| 35  | 3p3AUX_MGMT          | FLEXIO4_A | 38  |
| 36  | FLEXIO0_A            | GND       | 37  |