



OPEN
Compute Project

Modular Scalable DeNsity Optimized
HPM Form Factor (M-SDNO)
Base Specification

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Part of the
Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family
Version 1.0 RC2

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6/13/2024

PLEASE READ: ABOUT THIS DOCUMENT

M-SDNO defines a new family of M-DNO style HPMs with expanded scope for 19” and 21” Rack Ecosystems. In this definition, the workgroup took a new approach of defining HPM layouts which provide more flexibility in otherwise interoperable HPM outlines.

While most features and requirements are consistent with M-DNO R1.x, due to the increased scope, certain features of these new M-SDNO R1.x HPMs deviate from the requirements of M-DNO Type 2-4.

Due to these differences and new “Scalable” approach to HPM outlines, this “M-SDNO” document will remain a separate specification from “M-DNO” while highlighting the significant compatibility between M-DNO and M-SDNO HPMs (See **Section 14.4**).

Note: This specification no longer defines HPM “Types”, refer to **Section 8** for more information.

Note: For the latest information on M-DNO Type 2-4 please refer to the latest M-DNO release on the DC-MHS Wiki <https://www.opencompute.org/wiki/Server/DC-MHS>

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30

Table of Contents

1	License.....	10
35	1.1 Open Web Foundation (OWF) CLA	10
	1.2 Acknowledgements.....	10
2	Version Table	11
3	Scope	14
	3.1 Items Not in Scope of Specification.....	14
40	3.2 Typical OCP Sections Not Applicable	14
4	M-SDNO Base Specification Compliance Table	15
5	Overview	16
6	DC-MHS Family of Specifications.....	17
7	Terminology	18
45	8 Background and Assumptions	20
	8.1 M-SDNO HPM Classes and Common Chassis Intervals (CCIs).....	20
	8.2 Scalable HPM Intent and Methodology	22
	8.3 M-SDNO HPM Designators	23
	8.4 M-SDNO Interoperability Goals.....	23
50	8.5 Common Industry Platform Features Considered	25
	8.6 Architecture Specific Assumptions	26
	8.7 HPM Outline Scalability Enablement – Fixed and Floating Features.....	27
	8.8 HPM Outline Scalability Examples	28
	8.9 Chassis Design Approach for HPM Interoperability - Example.....	29
55	9 HPM Concepts and Layouts	31
	9.1 Class A HPM Layout.....	32
	9.2 Class B HPM Layout.....	33
	9.3 Class C HPM Layout.....	34
	9.3.1 19" Common Chassis Supporting Classes A, B and C.....	35
60	9.4 Class D HPM Layout.....	36
	9.4.1 21" Common Chassis Supporting Classes A, B, and D.....	37
	9.5 Class C and D Two Socket (CPU) Assumptions	38
10	Mechanical Requirements	39
	10.1 HPM Outlines.....	39
65	10.1.1 Class A HPM Board Outline.....	40
	10.1.2 Class B HPM Board Outline.....	41

	10.1.3	Class C HPM Board Outline.....	42
	10.1.4	Class D HPM Board Outline.....	43
	10.1.5	Allowance for Negative PCB Features	44
70	10.2	Board Datum and Mounting Hole Information	46
	10.2.1	Class A HPM Mounting/Riser Holes.....	48
	10.2.2	Class B HPM Mounting/Riser Holes.....	49
	10.2.3	Class C HPM Mounting/Riser Holes	50
	10.2.4	Class D HPM Mounting/Riser Holes	51
75	10.3	Secondary Side Zones and Height Restrictions	52
	10.3.1	Zone 1: Secondary Side Height Restriction.....	52
	10.3.2	Zone 2: Chassis to HPM Bracket (Board Pan) KOZ Requirements	54
	10.3.3	Zone 3: HPM Secondary Support Requirements	64
	10.3.4	Zone 4: CPU Backing Plate Requirements	65
80	10.4	HPM Board and Assembly Thickness	66
	10.5	HPM to Chassis Retention Mounting	68
	10.6	HPM Handle Hole	70
	10.7	OCP NIC R3 and DC-SCM R2.x at Near Side Edge Locations	72
	10.7.1	OCP NIC and DC-SCM.....	72
85	10.8	Platform Infrastructure Connector Placement (non-power).....	73
	10.8.1	Connector Requirements	73
	10.8.2	Class A and Class B M-PIC Connector Locations (non-power).....	74
	10.8.3	Class C M-PIC Connector Locations (non-power).....	78
	10.8.4	Class D M-PIC Connector Locations (non-power).....	80
90	10.9	High Speed I/O (HSIO) Connectors	82
	10.9.1	DC-MHS Compliant HSIO Connectors.....	83
	10.9.2	Near Side Fixed Riser Connectors.....	84
	10.9.3	Other HSIO Connectors.....	87
	10.10	Primary Side Component Height Restrictions and KOZs	88
95	10.10.1	Class A HPM Primary Side Component Height Restrictions	90
	10.10.2	Class B HPM Primary Side Component Height Restrictions	91
	10.10.3	Class C HPM Primary Side Component Height Restrictions	92
	10.10.4	Class D HPM Primary Side Component Height Restrictions	93
	10.11	Class B Platform Custom Zone.....	94
100	10.11.1	Class B Direct Dock E1.S	94
	10.12	Class C Platform Custom Zone.....	95

	10.12.1	Class C Second OCP SFF NIC R3 and/or Second OCP SCM 2.X.....	95
	10.12.2	Class C OCP NIC R3 DSFF.....	97
	10.13	Class D Platform Custom Zone	99
105	10.13.1	Class D Second OCP SFF NIC R3 and/or Second OCP SCM 2.X.....	99
	10.13.2	Class D OCP NIC R3 DSFF.....	100
	10.13.3	Class D Direct Dock E1.S	101
11		Power Zones	102
	11.1	HPM Power Zone Overview	102
110	11.2	Near and Far Bi-Directional (Ingress / Egress) Power Zones	103
	11.2.1	Ingress / Egress Cabled Power Connector	103
	11.2.2	Power Requirements (All Classes).....	104
	11.2.3	Class A Ingress / Egress Power Connector Locations	105
	11.2.4	Class B Ingress / Egress Power Connector Locations	106
115	11.2.5	Class C HPM Ingress / Egress Power Connector Locations	107
	11.2.6	Class D HPM Ingress / Egress Power Connector Locations	108
	11.3	Fixed I/O Riser Power	110
	11.4	DC-SCM R2.x Power	110
	11.5	OCP NIC R3.0 Power	110
120	11.6	Platform Custom Zone Power	110
	11.7	PICPWR Labeling Order	111
12		I/O System (Electrical Interfaces)	112
13		References.....	113
14		Supplemental Material.....	114
125	14.1	M-SDNO Conceptual Implementation Examples.....	114
	14.1.1	Class B	114
	14.1.2	Deep HPMs (A555, B555) in OpenRack v3	115
	14.1.3	Class D	117
	14.1.4	Multi-Node Specific	119
130	14.2	M-SDNO Power Zone Usage Examples	121
	14.3	Example Chassis Base Geometry for Chassis-to-Board Bracket interface	125
	14.4	M-DNO and M-SDNO 305.59mm HPM Compatibility.....	126
	14.4.1	Implications for HPM Designers	127
	14.4.2	Implications for System Designers	128
135	14.5	M-SDNO CAD Files	129
	14.6	Future Material.....	130

Table of Figures

	Figure 1: M-SDNO HPM Framework.....	20
140	Figure 2: M-SDNO HPM with Multi-node Interface Board.....	22
	Figure 3: HPM Class Interoperability Goals.....	23
	Figure 4: 19" M-SDNO Chassis Examples	24
	Figure 5: Example of Fixed and Floating Features	27
	Figure 6: Example of Variable Length Scaling.....	28
145	Figure 7: Example of HPM Consistency Across Class Fixed Width Variability	29
	Figure 8: Example Chassis Interface and Pan Strategy for Shorter HPMs	30
	Figure 9: Near and Far Terminology Example (Class A Depicted)	31
	Figure 10: Class A HPM Overview (PRIMARY SIDE)	32
	Figure 11: Class B HPM Overview (PRIMARY SIDE)	33
150	Figure 12: Class C HPM Overview (PRIMARY SIDE)	34
	Figure 13: Common 19" Chassis Supporting Class A, B and C (PRIMARY SIDE)	35
	Figure 14: Class D HPM Overview (PRIMARY SIDE)	36
	Figure 15: Common 21" Chassis Layout for Class A, B and D (PRIMARY SIDE).....	37
	Figure 16: M-SDNO HPM First CPU Assumed Position (Class D PRIMARY SIDE Shown)	38
155	Figure 17: Class A HPM Board Outline (PRIMARY SIDE)	40
	Figure 18: Class B HPM Board Outline (PRIMARY SIDE)	41
	Figure 19: Class C HPM Board Outline (PRIMARY SIDE)	42
	Figure 20: Class D HPM Board Outline (PRIMARY SIDE)	43
	Figure 21: A335 HPM with Compliant Negative PCB Features	44
160	Figure 22: Hole Detail Reference	46
	Figure 23: Class A HPM Mounting/Riser Holes (PRIMARY SIDE)	48
	Figure 24: Class B HPM Mounting/Riser Holes (PRIMARY SIDE)	49
	Figure 25: Class C HPM Mounting/Riser Holes (PRIMARY SIDE)	50
	Figure 26: Class D HPM Mounting/Riser Holes (PRIMARY SIDE)	51
165	Figure 27: Secondary Side Zone Definitions (Class A Example Depicted)	52
	Figure 28: Example of Chassis-to-Board Bracket (Board Pan).....	54
	Figure 29: Class A Chassis Hook Locations (SECONDARY SIDE).....	56
	Figure 30: Extended Length Class A Chassis Hook Locations (SECONDARY SIDE)	57
	Figure 31: Class B Side Chassis Hook Locations (SECONDARY SIDE).....	58
170	Figure 32: Extended Length Class B Chassis Hook Locations (SECONDARY SIDE)	59
	Figure 33: Class C Chassis Hook Locations (SECONDARY SIDE).....	60
	Figure 34: Extended Length Class C Chassis Hook Locations (SECONDARY SIDE)	61
	Figure 35: Class D Chassis Hook Locations (SECONDARY SIDE).....	62
	Figure 36: Extended Length Class D Chassis Hook Locations (SECONDARY SIDE)	63
175	Figure 37: Example Secondary Side Supports	64
	Figure 38: Secondary Side Components (Zone 1)	67
	Figure 39: Chassis Hook Keepouts (Zone 2).....	67
	Figure 40: HPM Secondary Support (Zone 3)	67
	Figure 41: CPU Backing Plate (Zone 4)	67
180	Figure 42: HPM Assembly to Chassis Retention Enablement (Class A Depicted).....	68
	Figure 43: Class C Assembly to Chassis Details (SECONDARY SIDE)	69

	Figure 44: Class D Assembly to Chassis Details (SECONDARY SIDE)	69
	Figure 45: Example Board Handling Feature	70
	Figure 46: Geometry and KOZ for HPM Handle Hole and Optional Placement Location	71
185	Figure 47: OCP NIC 3.x and DC-SCM R2.x (PRIMARY SIDE)	72
	Figure 48: Class A-B Platform Infrastructure Connector Recommended Placements.....	74
	Figure 49: Class A Intrusion, Control Panel, USB and PDB Management Placement Zones	75
	Figure 50: Class B Intrusion, Control Panel, USB and PDB Management Placement Zones	76
	Figure 51: Class A Cabled Boot Connector Placement Zone	77
190	Figure 52: Class B Cabled Boot Connector Placement Zone	77
	Figure 53: Class C Platform Infrastructure Connector Recommended Placements.....	78
	Figure 54: Class C Intrusion, Control Panel, USB and PDB Management Placement Zones	79
	Figure 55: Class C Cabled Boot Connector Placement Zone	79
	Figure 56: Class D Platform Infrastructure Connector Recommended Placements	80
195	Figure 57: Class D Intrusion, Control Panel, USB and PDB Management Placement Zones	81
	Figure 58: Class D Cabled Boot Connector Placement Zone	81
	Figure 59: Class A-B Required Riser Locations with Recommended Connector	85
	Figure 60: Class C Required Riser Locations with Recommended Connector	85
	Figure 61: Class D Required Riser Locations with Recommended Connector	86
200	Figure 62: Class A Component Height Restriction Zones (PRIMARY SIDE)	90
	Figure 63: Class B Component Height Restriction Zones (PRIMARY SIDE)	91
	Figure 64: Class C Component Height Restriction Zones (PRIMARY SIDE)	92
	Figure 65: Class D Component Height Restriction Zones (PRIMARY SIDE)	93
	Figure 66: Class B HPM with Direct Dock E1S in Custom Zone.....	94
205	Figure 67: Class C HPM 2nd OCP SFF NIC and/or 2nd DC-SCM in Platform Custom Zone	95
	Figure 68: Class C HPM OCP DSFF NIC in Platform Custom Zone.....	97
	Figure 69: Class D HPM 2nd OCP SFF NIC and/or 2nd DC-SCM in Platform Custom Zone	99
	Figure 70: Class D HPM OCP DSFF NIC in Platform Custom Zone.....	100
	Figure 71: Class D HPM with Direct Dock E1S in Platform Custom Zone 2	101
210	Figure 72: M-SDNO Power Zone Overview (Class A and D Depicted).....	102
	Figure 73: Example 2x3 + 6SB (Right Angle) and 2x6 + 12SB PICPWR Connector (Vertical) ..	103
	Figure 74: Class A HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE) ..	105
	Figure 75: Class B HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE) ..	106
	Figure 76: Class C HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE) ..	107
215	Figure 77: Class D HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE) ..	108
	Figure 78: Class D HPM Near Power Zone with Risers 1, 2, 4, and 5 Utilized	109
	Figure 79: Class D HPM Near Power Zone with Riser 3 Utilized	109
	Figure 80: Recommended PICPWR labeling order, Class B Shown	111
	Figure 81: M-SDNO Class B with 1U PCIe Risers.....	114
220	Figure 82: Two Class B HPMS in ORv3 Chassis	114
	Figure 83: ORv3 High Level Layout with 2x B555	115
	Figure 84: B555 Depth Stackup Example View	116
	Figure 85: Class D Example – 10U with 4 FH AICs.....	117
	Figure 86: Class D Example – 10U with 2 FH and 3 HH AICs	117
225	Figure 87: Class D Example – 10U with 1 FH, 1 HH AICs and 16 E1.S.....	117
	Figure 88: Class D Example – 20U with 12 FH AICs	117
	Figure 89: Class D Example – 20U with 6 FH and 9 HH AICs	117
	Figure 90: Class D Example – 20U with 4 FH AICs and 30 E1.S	118

	Figure 91: Class D Example – 2OU with 6 FH AICs and 14 E3.S	118
230	Figure 92: Multi-Node Adaptation Example	119
	Figure 93: Multi-Node Management Example	120
	Figure 94: Power Zone Example 1: Monolithic Basic One Zone Ingress	121
	Figure 95: Power Zone Example 2: Monolithic Leveraging Both Zones.....	122
	Figure 96: Power Zone Example 3: Multi-node with Far Side PDB.....	123
235	Figure 97: Power Zone Example 4 : Multi-node with Near Side PDB	124
	Figure 98: Example Chassis Base Geometry for Board Bracket Interface.....	125
	Figure 99: Superset KOZ M-DNO T2 + M-SDNO Class A (SECONDARY SIDE)	127
	Figure 100: M-DNO and M-SDNO 305.59mm HPMs (PRIMARY SIDE).....	128
	Figure 101: CAD Snapshot (A305 Example PRIMARY SIDE).....	129
240		

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1.2 Acknowledgements

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback of various individuals and companies that participated in DC-MHS.

2 Version Table

290

Date	Version #	Description
05/16/2023	0.3	- Initial Public Release based on M-DNO R1.0 V1.0 Specification -----RC2----- - Fixed Typo in Figure 11, 303.59mm changed to 305.59mm - Updated Contributor List - Fixed typo in Section 8 - Fixed Implementor Note in Section 10.4
09/25/2023	0.5 RC1	*** DUE TO THE NATURE OF CHANGES IMPACTING MOST SECTIONS OF THE DOCUMENT ONLY VERY HIGH-LEVEL CHANGES ARE LISTED *** - Refactored document to reflect new M-SDNO approach (elimination of Types, addition of Classes) - Removed coloring and markup associated with “Old” vs “New” content - Updated spec title and contributors list - Added initial draft of compliance table (CH 4) - Updated CH 5 (Overview) - Added M-SDNO to CH 6 - Added additional terms to CH 7 (Terminology) - Re-wrote majority of CH 8 (Background and Assumptions) - Re-worked the majority of CH 9 (Concepts and Layouts) - Updated majority of drawings in CH 10 to align with HPM Classes, including change of 21” Full Wide HPM from 500mm to 512mm - Updated CH 11 (Power) to better encompass all HPM Classes - Added section detailing HPM outline scalability (CH 13) - Updated implementation concepts (15.1) to reflect HPM Classes - Added section discussing M-DNO and M-SDNO compatibility (15.5)
10/02/2023	0.5 RC2	- Completed section 4 - Updated DC-SCM r2 to r2.1 - Added mockup of Class C to section 9 - Added section names to all section references - Cleaned up duplicate PICPWR requirements (Section 11) - Fixed missing references in section 12
1/22/2024	0.7 RC1&2	Requirement and Recommendation Changes All HPM Classes - Zone 2 (Secondary Side KOZs) updated (10.3.2) - Zone 3 requirements simplified (10.3.3) - Added allowance for notches and other negative board features (10.1.5) - Updated max Z height stack up from 5.86mm to 6.2mm (10.3.4, 10.4) - Updated approach to mounting hole requirements and recommendations (10.2)

		- Removed alternate fixed riser connector keep in zones (10.9.2) - Added preliminary information for a board-to-board power ingress connector option (11.2.7) Class A Specific - Added a placement zone for “Far Side” PICPWR Connectors (11.2.3) Class B Specific - Added a placement zone for “Far Side” PICPWR Connectors (11.2.4) Class C Specific - Added figures and text descriptions through the document. - HPM Width changes from preliminary 423mm to 426mm (10.1.3) - Moved DC-SCM to common location with Class A and B (9.3.10.7) Class D Specific - Moved DC-SCM to common location with Class A and B (9.4, 10.7) - Updated custom zone options (10.11, 10.12, 10.13) - Updated CPU 0 Assumption to reflect new guidance (9.5) - Increased zone of the Cabled Boot Connector (10.8.3) Specification Clarifications and Layout - Updated layout drawings to show OCP NIC location as a part of the custom zone (9) - Rewrote high speed IO sections to increase clarity of requirements and recommendations (10.9) - Moved riser retention hole information from 10.9 to 10.2 - Consolidated common PICPWR requirements (11.2) - Moved HSIO connector compliance table from 12.2 to 10.9 - Various text and note updates - Various figures cleaned up
1/29/2024	0.7 RC3	- Figure 17, Removed extra circle on a mounting hole - Figure 21, fixed handle sub hole location - Figures 28-29, added missing KOZ @ 234mm - Figure 33 – Fixed typo on KOZ quantity - Figure 45, Corrected DIMs and leader lines - Clarified some compliance table items - Minor grammar corrections in text
4/4/2024	0.9 RC1	- Consolidated to a single Figure in Section 9.5 - Updated various Class C and Class D figures to suppress custom zone options on the near side edge - Moved connector requirement information from Chapter 12 to Section 10.8 and 10.9 for better document flow - Alphabetized Section 6 - Misc. non substantive figure corrections (leader lines, missing dims) - Added option for second DC-SCM in custom zone for Class C/D

		(Section 10.12 & 10.13) - Added option for DSFF in custom zone for Class C/D (Section 10.12 & 10.13) - Clarified text describing riser locations per Class in 10.9.2 - Removed Section 13.x (HPM Outline Scalability) and moved content to Section 8.7 <-> 8.9 to improve document flow for first time readers - Updated PICPWR numbering recommendation to include Risers and moved to dedicated Section (11.7) - Updated language describing DC-SCM and OCP NIC Power (11.4, 11.5) - Added a Future Material section describing potential future additions to the specification (14.6) and moved the alternate board to board power connector from 11.2 to 14.6 while the workgroup continues to study options for this connector - Added Zone 1 (Secondary side component height restrictions) exception allowance (10.3.1.1)
04/16/2024	0.9 RC2	Fixed some typos/formatting, cleaned up compliance table, removed far side B2B compliance line.
06/03/24	1.0 RC1	- Updated MHS group contact list - Updated contributors and alphabetized companies - Updated Figures 49-50 to extend primary control panel and intrusion switch zone to far side board edge on Class A/B. Also updated MCAD photo in Figure 101 to match. - Added second option for Control Panel location for Class C (Figure 53, 54) - Updated 10.12 (PCZ for C) and 10.13 (PCZ for D) for DSFF NIC. Updated names and added Implementor's Notes when >1 NIC is used and warnings when DSFF NIC is used. - Updated Figures 10/11 to show I/O Regions - Updated 10.3.1 to allow more flexibility for secondary side component height exceptions - Cleaned up Figures 1,5,6,7,17,18,27,29,31,42,55,66, - Updated labeling of DC-SCM and NIC slots in Figures 13, 15, 16, 67, 68, 69, 70, - Various text fixes of typos, grammar, etc. which are not substantive to M-SDNO designs - Labeled figures PRIMARY and SECONDARY side where applicable to provide clarity - Clarified exceptions for Near Side HSIO connectors relative to component height exceptions (10.10) - Added implementors notes to Class C and Class D custom zone sections to provide OCP NIC implementation guidance - Removed alternate far side B2B power connector information, will be added back in if the workgroup decides to move forward with this option
6/13/2024	1.0 RC2	Updated Figures 10 and 11 with Region instead of Zone

3 Scope

This document defines technical specifications for the Scalable Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.

Any supplier seeking OCP recognition for a hardware product based on this specification shall be 100% compliant with all features or requirements listed in **Section 4** of this specification.

3.1 Items Not in Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc.).

3.2 Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

- Rack Compatibility (Discussed in **Section 8**)
- Physical Spec
- Thermal Design
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management (Leverages OCP DC-SCM R2.x)
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

4 M-SDNO Base Specification Compliance Table

330

The following table is meant to point the reader to sections containing Base Spec compliance required items. The table should not be used as a checklist as each row could contain multiple requirements. Base Spec compliance items are underlined and use the word “shall”.

Item	Base Spec Requirement	Reference
1	Any supplier seeking OCP recognition for a hardware product based on this specification shall be 100% compliant	4
2	Follow the defined PCB tolerances in Table 2	Table 2 (multiple items)
3	Follow the defined board outlines for Class A-D	10.1 (multiple items)
4	If negative PCB features are implemented, follow section rules	10.1.5 (multiple items)
5	All HPM and Riser mounting holes, as well as additional holes, shall follow required Figure 19 padstacks. Not allowed to delete the Riser mounting holes.	10.2 (multiple items)
6	Zone 1 Secondary side component HRZ of 1.6mm and exception rules	10.3.1 (multiple items)
7	Maximum length of a connector's Alignment Post or Retention Barb in Zone 2 <= 3.2mm (see implementor's note)	10.3.2
8	Multiple Zone 2 KOZs are required see Section 10.3.2	10.3.2 (multiple items)
9	If scalable HPM depth >372.5mm (from origin), additional Zone 2 KOZs shall be implemented.	10.3.2 (multiple items)
10	Zone 4 Board Thickness + CPU Backplate Thickness <= maximum defined (Backplate max thickness calculated as specified)	10.3.4
11	HPM Board thickness <= 3.18mm	10.4
12	HPM to chassis retention hole and associated KOZ	10.5
13	Additional secondary side KOZ required for Class C and D HPMs	Figure 43 and Figure 44
14	Far side hole for board handle with defined geometry and KOZs	10.6 (multiple items)
15	If OCP NIC R3.0 is implemented, connector shall be placed per Figure 47 and power provided per OCP NIC R3.0 specification	10.7, 11.5, OCP NIC R3
16	DC-SCM connector shall be placed per Figure 47 and power provided per DC-SCM R 2.x specification	10.7, 11.4, DC-SCM R2.x
17	HPM shall implement battery backed voltage interface per DC-SCM R2.x “Battery Voltage” requirement	10.7
18	Control panel connector placed within specified zone	10.8
19	Intrusion switch header placed within specified zone	10.8
20	Host USB connector placed within specified zone	10.8
21	PDB Management connector placed within specified zone	10.8
22	Boot Connector placed within specified zone	10.8
23	Required Int. USB3 connector, electrical implementation follows the M-PIC specification	10.8, M-PIC
24	Required Intrusion Switch connector, electrical implementation follows the M-PIC specification.	10.8, M-PIC
25	If implemented, Boot Storage connector electrical implementation follows the M-PIC specification.	10.8, M-PIC
26	Required Primary Control Panel connector and Optional Control Panel connector electrical implementation follows the M-PIC specification.	10.8, M-PIC
27	Required PDB Management connector electrical implementation follows the M-PIC specification	10.8, M-PIC
28	All HSIO connectors shall be compliant with the M-XIO specification and DC-MHS Connector List	10.9.1
29	Required HSIO connectors electrical implementation follows the M-XIO specification	10.9.1 (multiple items), M-XIO
30	HPMs which implement near side fixed B2B risers shall place connectors in defined locations and use SFF-TA-1033 connectors w/ 21A power block	10.9 (multiple items)
31	All non-exempt soldered components adhere to required Primary Side component height restrictions in the 11.3mm and 6mm HRZs.	10.10 (multiple items)
32	All “Near” and “Far” Ingress / Egress zones implement the 2x6+12SB and/or 2x3+6SB PICPWR connector	11.2
33	All HPMs implement a minimum of one 2x6+12SB PICPWR connector in far side Ingress / Egress zone. Enough connectors shall be placed within the zone such that the far power zone can meet the full HPM power budget when used for ingress.	11.2.2.1 (multiple items)
34	Class C and D HPMs shall use vertical connectors in the Near Side PICPWR zone	11.2.5 and 11.2.6
35	HPM delivers at least 87W to each implemented B2B Fixed Riser location	11.3
36	HPM delivers enough power to Platform Custom Zone if implemented	11.6

5 Overview

335 The M-DNO R1.0 specification, published within the OCP **Data Center Modular Hardware Systems (DC-MHS)** sub-project, defined multiple interoperable Host Processor Module (HPM) form factors intended for DeNsite Optimized 19" EIA-310 rack server solutions.

340 The objective of this **Scalable DeNsite Optimized (M-SDNO)** specification is to build upon the M-DNO R1.0 framework and expand the scope to scale to a broader collection of infrastructure solutions. Specifically, M-SDNO defines HPMS optimized for 19" EIA-310, 21" OpenRack v3 as well as HPMS that can operate in either rack ecosystem. In addition, the M-SDNO framework covers a broad scope of HPM depths and configurations from short depth monolithic systems through extended length multi-node system architectures.

345 This specification will define attributes and design requirements that are common and critical to the use and deployment of Enterprise and Cloud solutions which may also apply to Edge optimized service provider products. Examples of these attributes are mechanical form factor, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections. Most M-SDNO attributes are consistent with those of M-DNO compliant HPMS, and this specification will highlight differences and compatibility enablement.

350 The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs, implemented to the specification, to enable reuse of chassis and system level components over multiple generations. Implementing to this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

Implementors Note:

As a Base Specification, M-SDNO contains and allows for optionality in many areas. In addition to this base specification, it is recommended that HPM designers create and maintain an HPM Design Specification that further details the needs and requirements of their own unique design.

Examples of information that may be included in a Design Specification are:

- Quantity and location of fixed/hybrid risers
- Quantity and location of other HSIO connectors
- Power zone requirements
- Innovation zone use case
- Etc.

6 DC-MHS Family of Specifications

The Data Center – Modular Hardware System (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specifications:

- **M-CRPS (Modular Hardware System Common Redundant Power Supply Specification)** – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-DNO (Modular Hardware System Partial Width DeNsity Optimized Specification)** – Host Processor Module (HPM) specification targeted to partial width (i.e. $\frac{1}{2}$ width or $\frac{3}{4}$ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments.
- **M-FLW (Modular Hardware System Full Width Specification)** – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-PESTI (Modular Hardware System Peripheral Sideband Tunneling Interface)** – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (i.e., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- **M-PIC (Modular Hardware System Platform Infrastructure Connectivity Specification)** – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-SDNO (Modular Hardware System Scalable DeNsity Optimized Specification)** – Builds upon M-DNO, defines partial and full width HPMs with variable board outlines covering 19" EIA-310 and 21" OpenRack v3 infrastructure.
- **M-SIF (Modular Hardware System Shared Infrastructure Specification)** – Specifies data and management plane interfaces along with power and cooling connections that are expected to be present within a modular platform utilizing shared elements.
- **M-XIO (Modular Hardware System Extensible I/O)** – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **Current Connector List** – Vendor and part number information for all connectors referenced by DC-MHS specifications, updated as needed. Full URL: https://docs.google.com/spreadsheets/d/1Vg_JxzZ43ysxBNHJ928vnzlcshA95GYGocaKmJCBC80/
- To access additional DC-MHS specifications please visit the DC-MHS Project Wiki: <https://www.opencompute.org/wiki/Server/DC-MHS>

400 **7 Terminology**

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for Base Spec compliance	Must
DC-SCM	Datacenter Secure Control Module as defined by OCP DC-SCM R2.x spec	SCM
PCB	Printed Circuit Board	PCBA
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
Chassis-Board Bracket	Bracket that attaches to an HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan Sub Pan
Datum	A plane, axis or point location from which dimensions and tolerances are referenced.	
Near	Board location or zone, related to section of board closer to the datum	Near Side
Far	Board location or zone, opposite of location of datum	Far Side
Platform	Complete system including HPM, power, peripherals, etc.	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc.	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
CSP	Cloud Service Provider	

19" ½ Width HPM	210mm wide HPM, enables systems with 2 HPMs side by side in 19" Rack	
19" Full Width HPM	426mm wide HPM, uses full width of 19" Rack	
21" ½ Width HPM	250mm wide HPM, enabled systems with 2 HPMs side by side in 21" Rack, also used in 19" systems	
21" Full Width HPM	512mm wide HPM, intended only for 21" Rack	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	
Platform Infrastructure Connectivity Specification	Refer to Section 6	M-PIC
Full Width Specification	Refer to Section 6	M-FLW
Common Redundant Power Supply Specification	Refer to Section 6 (References)	M-CRPS, CRPS PSU
Extensible I/O Specification	Refer to Section 6	M-XIO
KOZ	Keep Out Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
Compliant HPM	An HPM which meets every item listed in this base specification compliance table.	
Adapted HPM	An HPM that utilizes a Compliant HPM as a construct, with a specific set of repeatable modifications which form the adaptation.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements this base specification.	
System Designer	The person or organization designing a system which incorporates HPMs (whether compliant or adapted) into the system design.	
Common Chassis Interval	Refers to the maximum HPM Length supported within common chassis infrastructure. Exceeding these intervals will impact addressable market for HPM designs.	CCI
HPM Class	Defines HPM width and feature set	
Floating Feature	Features that shift relative to the HPM board edge as the length changes	
Fixed Feature	HPM features with a consistent location relative to the datum	

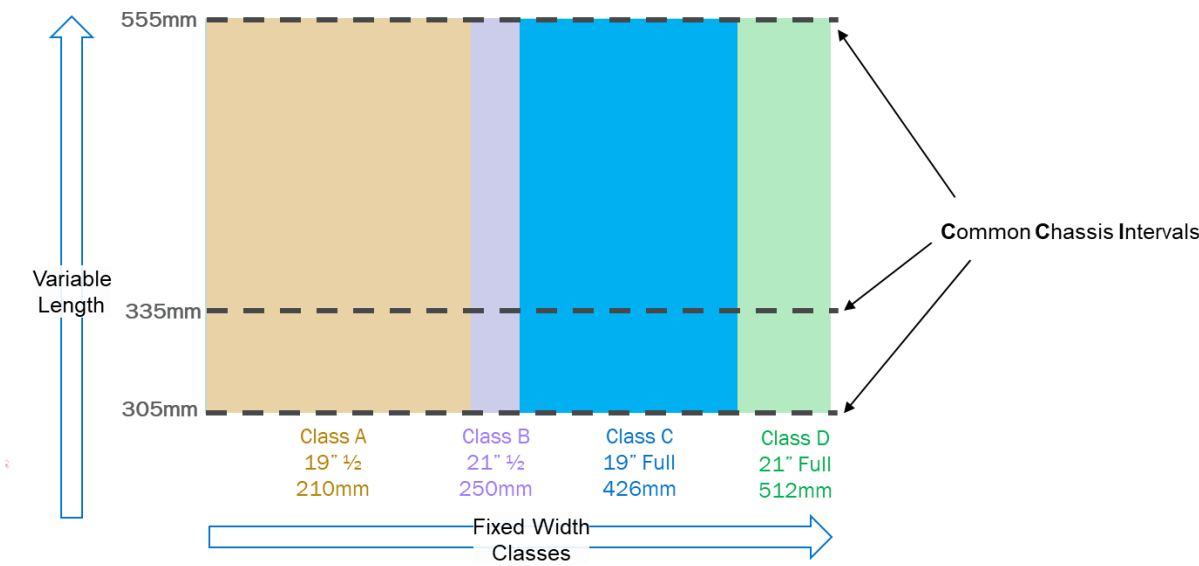
8 Background and Assumptions

A Note on Board Types:

Previous DC-MHS R1.0 HPM specifications (M-FLW R1.0, M-DNO R1.0) defined board “Types” with explicit fixed length and width dimensions. As M-SDNO enables more flexibility in HPM outline dimensions it does not define “Types”. As of the time of this specification release there is no plan to change the Types defined by M-FLW or M-DNO.

8.1 M-SDNO HPM Classes and Common Chassis Intervals (CCIs)

Figure 1: M-SDNO HPM Framework



Note: Length dimensions shown represent the longer board edge

M-SDNO is intended to enable a wide variety of interoperable HPMs for both 19" and 21" rack ecosystems. For purposes of this specification, 19" refers to EIA-310 19" racks and 21" refers to OpenRack v3 style racks. M-SDNO targets both monolithic and multi-node systems across Enterprise, Cloud and Edge applications. To cover this diverse solution space, M-SDNO defines 4 "HPM Classes" as shown in Figure 1.

An HPM Class defines a fixed HPM width and corresponding feature set, for example, all Class A HPMs are 210mm wide and support 2 Riser locations, while Class B are 250mm wide and support 3 Riser locations.

For each HPM class, length is variable up to a specification defined maximum. HPMs are defined such that the only major difference between different length HPMs of the same class is the space available for the compute core.

M-SDNO HPM Classes Include:

- 420 • Class A – 19" ½ Width – 210mm
 - Primarily targets 19" racks but can also be used in 21" racks.
 - Can be used in a traditional monolithic chassis, placed with two HPMs in a horizontal side-by-side scheme or in a vertical orientation.
 - Dense multi-node architectures are a possible use case.
- 425 • Class B – 21" ½ Width – 250mm
 - Targets both 19" and 21" racks.
 - In 19" rack this Class can be used in a traditional monolithic chassis with a single HPM or in a vertical scheme.
 - 430 ○ In a 21" rack this Class can be placed in a monolithic chassis, with two HPMs in a horizontal side-by-side scheme or in a vertical orientation.
 - Dense multi-node architectures are a possible use case.
- 435 • Class C – 19" Full Width – 426mm
 - Exclusively targets 19" racks.
 - Typically horizontally oriented and consume the full 19" rack width.
 - 21" racks are not the intended optimization point for this Class.
- 440 • Class D – 21" Full Width – 512mm
 - Exclusively targets 21" racks.
 - Typically horizontally oriented and consume the full 21" rack width.
 - 19" racks are not the intended optimization point for this Class.

445 M-SDNO also specifies "Common Chassis Intervals" (CCIs). These are important design points that are common in the industry which HPM designers should take careful consideration of when selecting the length of an HPM. The value specified by CCI 'N' means that common industry chassis infrastructures support HPMs up to a maximum length of N. For example, with a CCI at 305mm HPM designers should be aware that an HPM length of 306mm reduces the addressable market of that HPM.

450 M-SDNO Common Chassis Intervals, as depicted in **Figure 1**, include:

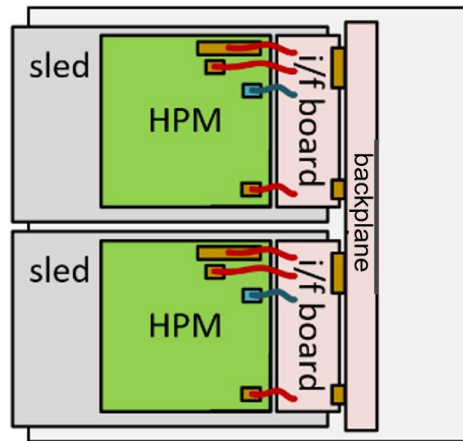
- 305mm
 - Short / dense chassis, particularly if the DC-SCM module is floating / cabled.
 - Typically, 1S or 2S "Spread" socket layout
- 455 • 335mm
 - Mid length chassis
 - Typically, 1S or 2S "Spread" socket layout
- 555mm
 - Extended length chassis
 - Typically for enablement of 2S "Shadowed" socket layouts

460 This specification will focus on products targeted to these primary chassis environments.
Section 14.1 M-SDNO Conceptual Implementation Examples illustrates design scenarios for

each of these solutions providing the reader a clearer understanding of each category. This specification does not prohibit alternate environments.

This version of the M-SDNO specification does not address native “direct plug” or “blind mate” options for HPMs, these scenarios may be added in a future release. At this time, it is assumed that compliant HPMs will leverage an interface board to enable these use cases as demonstrated in **Figure 2**.

Figure 2: M-SDNO HPM with Multi-node Interface Board



8.2 Scalable HPM Intent and Methodology

Previous DC-MHS form factor specifications (M-FLW and M-DNO) effectively required the HPM outline to be exactly the same as the Common Chassis Interval (e.g. 305mm) for compliance. The goal of M-SDNO enabling a variable HPM outline is to:

1. Allow HPM designers more flexibility in optimizing their designs (e.g. to reduce panelization cost)
2. Provide highly interoperable solutions so system designers do not experience chassis proliferation

The “scaled” or variable HPM outline is enabled by dimensioning features of the HPM in two different ways:

- Fixed features are features which are dimensioned to the datum, these features simply “fall off” the HPM if they are outside the board outline.
- Floating features are features which are dimensioned to a board edge, these features are always present in a consistent location relative to the HPM boundary and never “fall off” the HPM.

More detailed information is provided in **Section 8.7** through **8.9**.

8.3 M-SDNO HPM Designators

M-SDNO HPMs will be referred to as 'N####', where:

N = HPM Class (A, B, C or D)

= The length of the HPM in mm, rounded down to the nearest mm

Following this methodology, as shown in **Table 1**, a 305.59mm Class 'A' HPM would be referred to as M-SDNO 'A305'.

Table 1: HPM Designators at CCIs

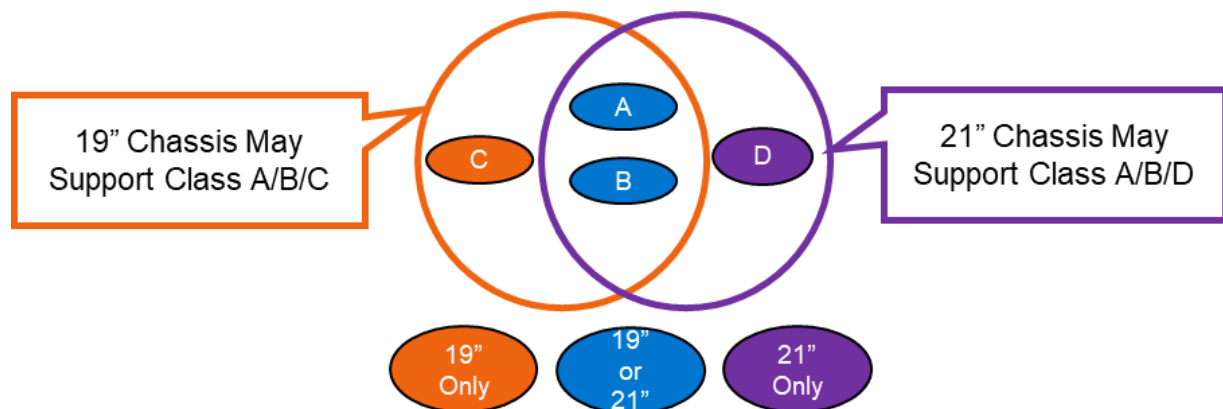
	305 CCI	335 CCI	555 CCI
Class A HPM	A305	A335	A555
Class B HPM	B305	B335	B555
Class C HPM	C305	C335	C555
Class D HPM	D305	D335	D555

8.4 M-SDNO Interoperability Goals

The goal of this specification is to provide HPM Interoperability of *most* smaller M-SDNO HPMs in systems designed for larger M-SDNO HPMs with minimal modifications (e.g. HPM tray or cable changes). The exception to this rule is that Class C HPMs are *not* expected to be interoperable with Class D HPMs. This incompatibility is due to the different “pitch” between ½ width HPMs in 19” and 21” infrastructures. In summary, the HPM Class interoperability goals, as depicted in **Figure 3**, are as follows:

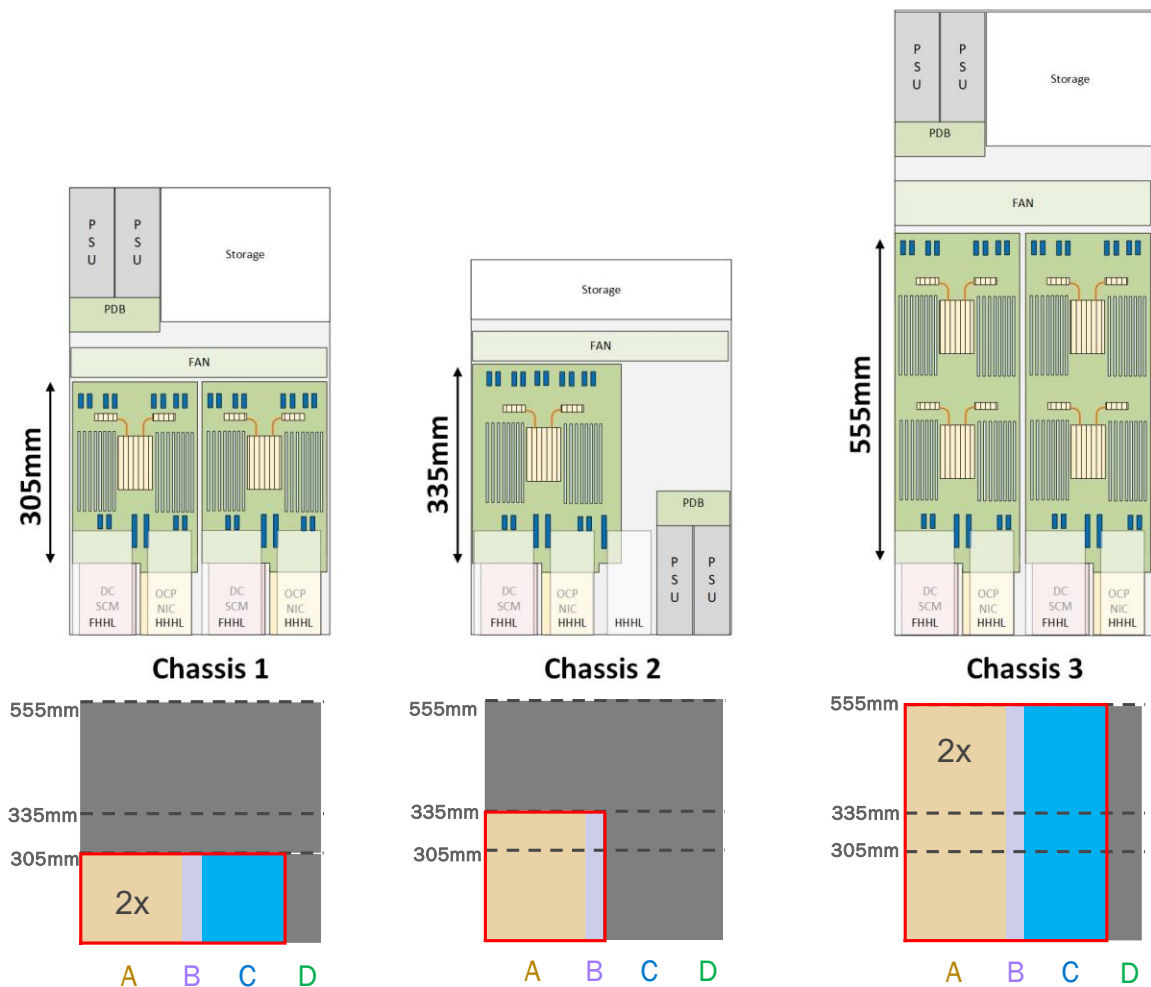
1. All M-SDNO HPMs of the same class are interoperable
2. Class A HPMs are interoperable with Class B, C and D
3. Class B HPMs are interoperable with Class A, C and D
4. Class C HPMs are interoperable with Class A and B
5. Class D HPMs are interoperable with Class A and B

Figure 3: HPM Class Interoperability Goals



- 510 This high degree of interoperability is intended to minimize chassis proliferation amongst M-SDNO system providers, this concept is demonstrated in **Figure 4:**
- Chassis 1 supports 19" Full width HPMs, as such it supports Class A (2x), B and C HPMs, but only to the 305 CCI.
 - Chassis 2 does not support 19" Full width HPMs due to the location of the power supplies (PSUs), however, it supports Class A and B up to the 335 CCI.
 - Chassis 3 supports not only 19" Full width HPMs, but also extended length solutions at the 555 CCI. This chassis supports ALL Class A (2x), B and C HPMs.
 - This example also demonstrates the benefit of HPMs being designed to the smallest Class and CCI possible, all three chassis can support an A305 or B305 HPM, whereas only Chassis 3 can support A555.
- 515
- 520

Figure 4: 19" M-SDNO Chassis Examples



525 **8.5 Common Industry Platform Features Considered**

Mechanical

- Chassis installation within EIA-310-E (19") and OpenRack V3 (21") racks
- High Speed I/O Riser Connector fixed placement
- High Speed I/O Cable route considerations
- 530 • Additional fixed connector placements
- Board pan (HPM tray) enablement
- 1RU chassis constraints

I/O

- 535 • PCIe (Version 3.0, 4.0, 5.0, 6.0 and future) Card configurations typically offered by Enterprise OEMs/CSPs/CoSPs
- Use of Open Compute peripherals connectors on the HPM
 - OCP NIC R3.0
 - DC-SCM R2.x

540 **Power**

- HPM supplied power to each fixed riser locations
- HPM Power Ingress and Egress connector placement for a variety of power layouts (PSUs with Cabled PDB, blind mate to bus bar, multi-node backplane, etc.)
- Considerations for Power Delivery to important chassis subsystems.

545

Thermal

- Thermal Design considerations including keep-out zone to enable thermal solutions that extend beyond the CPU and Memory sockets.

550 8.6 Architecture Specific Assumptions

Mechanical / Systems

- M-SDNO based systems
 - Do not direct plug PSUs into the HPM but instead leverage Power Distribution Boards (PDB) or other system / rack level power infrastructure
 - 555 ○ Use remote fan designs in air cooled platforms (there is no HPM spec provision for Fan connectors on the HPM)
 - Support riser based I/O cards, cable based I/O cards or a mix of both
 - Leverage a variety of front and rear service models of I/O, PSU, HPM, etc.
- 560 • Systems designed for longer HPMS may support use of shorter HPMS of the same Class in a common chassis or sled with minimal changes (e.g. cables, riser quantities, standoff locations)
- Chassis Width Assumptions
 - 565 ○ 19" Multi-node (2x ½ Width) chassis designs leverage static rails with overall inner chassis opening width of 443mm (in 19" rack)
 - 19" Monolithic chassis designs leverage slide rails with overall inner chassis width of 431mm (in 19" rack)
 - 21" Multi-node (2x ½ Width) chassis assumes opening width of 513mm or greater
 - 570 ○ 21" Full Width HPMS assume an internal chassis opening width of 513mm or greater. Chassis could be supported via fixed mounting rails or slide rails

I/O

- All M-SDNO HPM specify (but do not require) use of "off the shelf" OCP NIC R3.0
- 575 • Most systems will *typically* leverage Coplanar OCP NIC layouts
- However, short depth (i.e. Edge) systems may require alternate implementation such as "floating" the OCP NIC (or no-pop)
- PCIe CEM based I/O will be the predominant use case for consideration but alternate form factors are not prohibited

580 DC-SCM

- All M-SDNO HPM Classes enable (but do not require systems to utilize) use of "off the shelf" HFF DC-SCM R2.x
- Most systems will *typically* leverage Coplanar HFF DC-SCM
- 585 • However, short depth (i.e. Edge) systems will often require alternate implementation such as "floating" DC-SCM

8.7 HPM Outline Scalability Enablement – Fixed and Floating Features

M-SDNO dimensions various HPM “Features” in two different ways, an example is shown in **Figure 5**.

Fixed Features

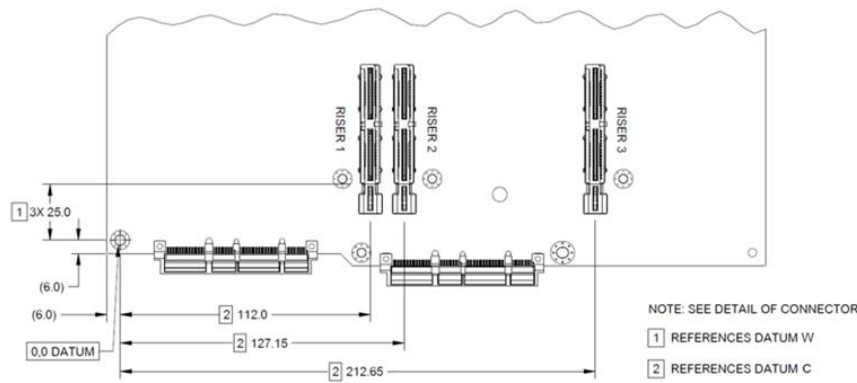
- Are dimensioned to the Common Datum
- Never move when HPM outline changes
- In some instances, may “drop off” and be not applicable to a smaller HPM
- Examples include Risers, the DC-SCM connector, HPM retention hole, etc.

Floating Features

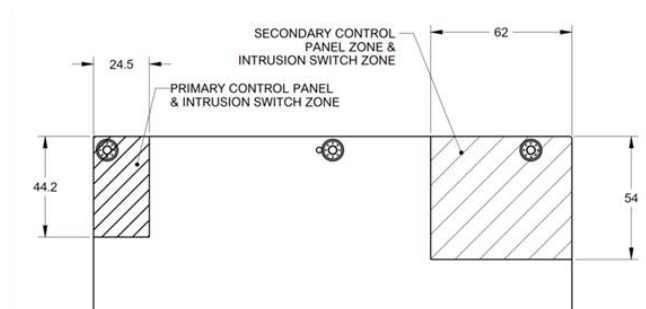
- Are dimensioned to board edges
- Move with the board edges as the edge changes relative to the datum
- Never “drop off” the HPM
- Examples include the Far Side Ingress / Egress power zone, control panel headers, far side mounting holes, etc.

Figure 5: Example of Fixed and Floating Features

Fixed Feature Example



Floating Feature Example

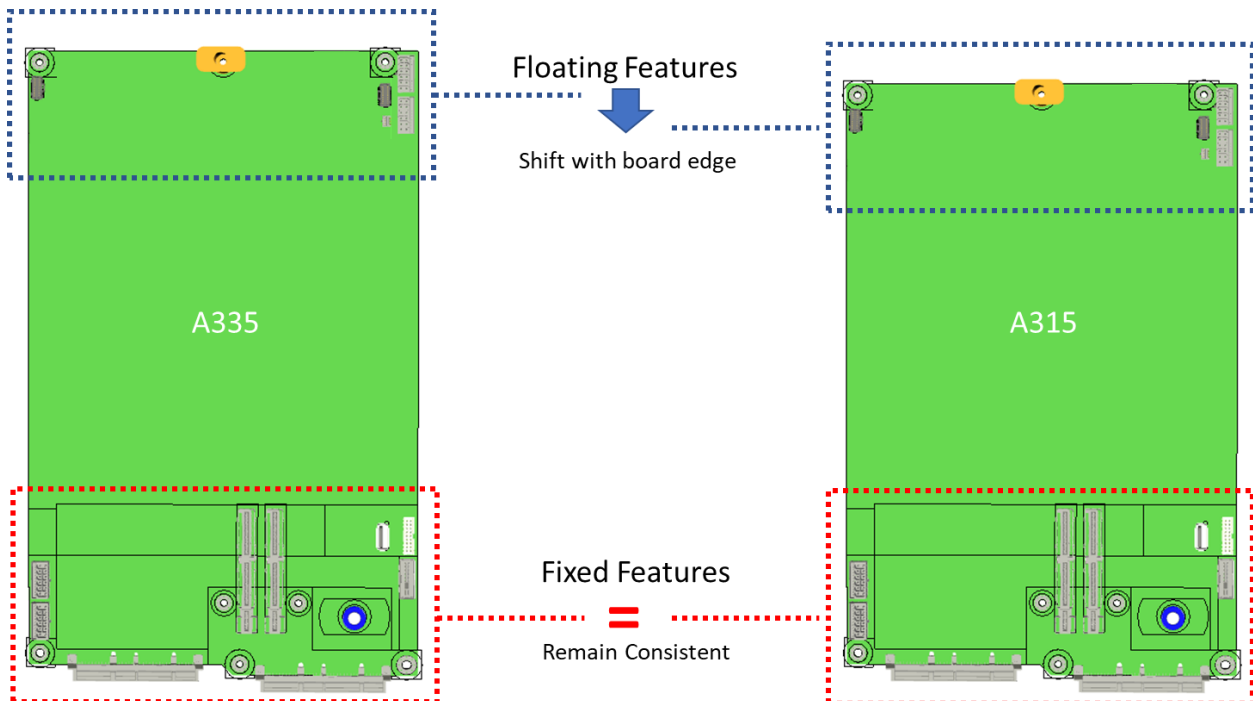


8.8 HPM Outline Scalability Examples

The intent of M-SDNO scalability is to provide additional flexibility to HPM designers without causing proliferation of chassis designs required by System designers. This is enabled by ensuring interoperability of smaller HPMs in Chassis designed for larger HPMs (Refer to **Section 8.4 M-SDNO Interoperability Goals**) and encouraging HPM designers to carefully consider when their HPM crosses a Common Chassis Interval boundary.

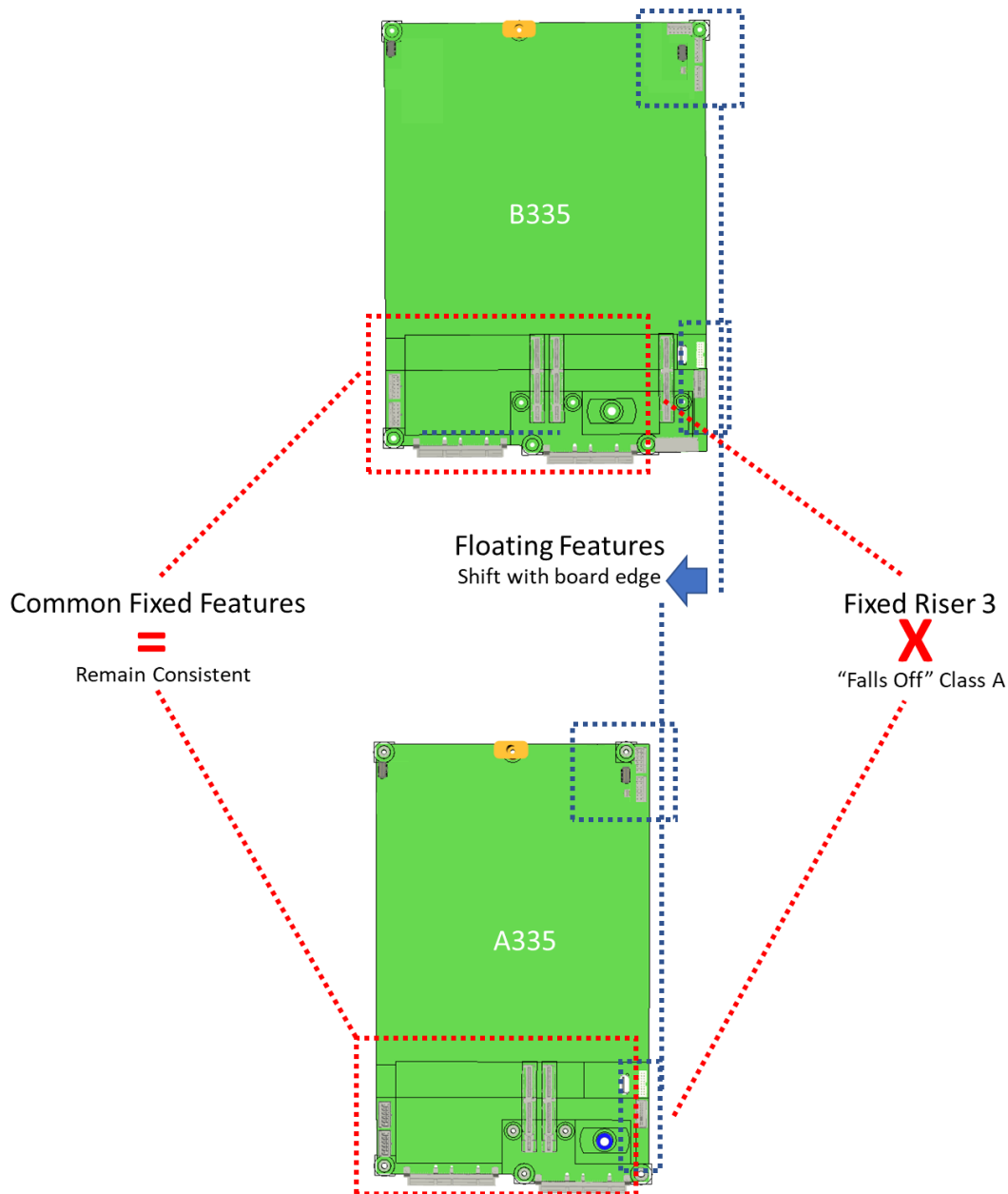
Figure 6 provides an example of Fixed and Floating features when choosing to scale the length of the HPM down from the 335 CCI to a shorter length. Note that both the A335 and A315 HPM can be deployed in a chassis designed to the 335 CCI. If instead the length was scaled longer to A340, the HPM would be incompatible with 335 CCI chassis reducing the scope of systems that HPM could intercept.

Figure 6: Example of Variable Length Scaling



While the width of M-SDNO HPMs is not entirely variable, the same Fixed and Floating feature concepts are used to provide consistent layouts across HPM Classes. **Figure 7** demonstrates how Fixed and Floating features enable Class A and Class B HPMs to be leveraged with minimal change into a common system infrastructure. These same principles hold true for Class C and Class D HPMs.

Figure 7: Example of HPM Consistency Across Class Fixed Width Variability



8.9 Chassis Design Approach for HPM Interoperability - Example

Chassis to HPM interoperability is built on the premise that an HPM tray is used as a form of physical abstraction. This tray will employ features for:

1. Mounting the HPM to the tray
2. Interlocking the HPM tray to the chassis base

The details of these features (standoffs, sheet metal forms, etc.) are outside the scope of this specification, however an example is provided in **Section 14.3 Example Chassis Base Geometry for Chassis-to-Board Bracket interface**.

The bottom side zone 2 KOZs of the deepest HPM supported will dictate the location of the chassis-to-tray interlock features – see **Section 10.3.2 Zone 2: Chassis to HPM Bracket (Board Pan) KOZ Requirements)** for KOZ details.

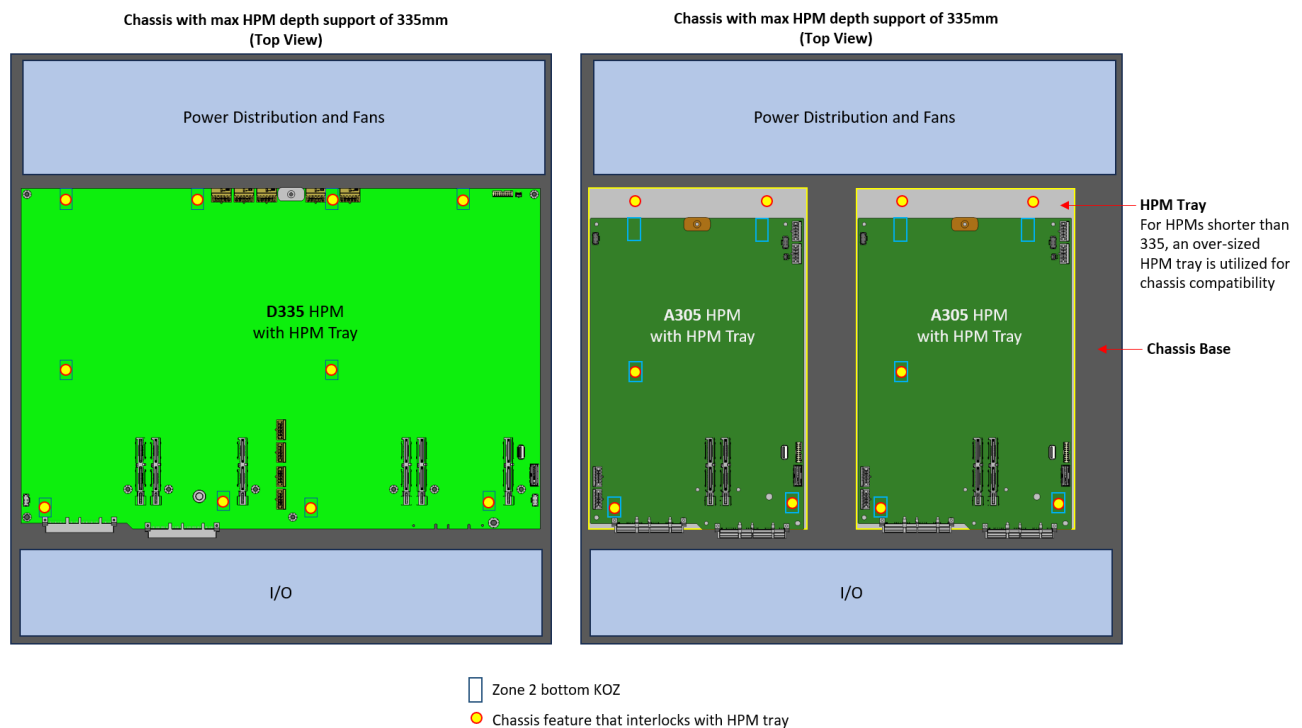
The chassis design will dictate the maximum supportable HPM depth. Any HPM of a lesser depth should also be supportable via an HPM tray that is deeper than the HPM and designed to be fully compatible with the chassis' fixed interlock features.

The following example illustrates this concept. While this example uses two specific HPMs (D335 and A305), the same concept applies to any interoperable HPM combination noted in **Section 8.4 M-SDNO Interoperability Goals**.

In this hypothetical example, a chassis has been designed for compatibility with a 21" rack. The chassis design also limits the maximum HPM depth to 335mm. The left-side image of **Figure 8** depicts a D335 HPM in this chassis. The blue rectangles represent the HPM zone 2 bottom side KOZs. The yellow circles represent the chassis features used to interlock with the HPM tray. In the left image the HPM tray is not visible because it is fully under the HPM.

The right-side image of **Figure 8** represents this same chassis but now populated with two A305 HPMs (placed on a 262mm pitch). The same chassis interlock features are used for securing these two HPM assemblies. But note that the A305 tray is longer than the HPM and includes the mating interlock features just beyond the HPM Far Side edge.

Figure 8: Example Chassis Interface and Pan Strategy for Shorter HPMs



Finally, note that the A305 HPM, when assembled in this example chassis, does not make use of its Far Side edge bottom side zone 2 KOZs. This does not mean these KOZs are not required to be implemented on this HPM. They are needed in a scenario where this same HPM is utilized in different chassis that is limited to maximum HPM depth equal to ~305mm.

9 HPM Concepts and Layouts

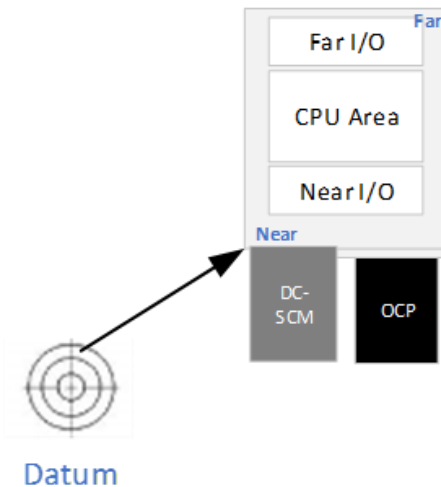
Definitions and concepts that apply to M-SDNO HPMs are described below:

- Due to the wide array of potential HPM and Chassis configurations, this specification defines a **Near** <<Element>> as the <<Element>> closer to the Datum (0,0 reference) and **Far** <<Element>> as the <<Element>> further from the Datum, examples for <<Element>> include:

- Side
- Corner
- Edge
- I/O Zone

An example of Near and Far terminology usage is shown in **Figure 9**.

Figure 9: Near and Far Terminology Example (Class A Depicted)



- The location of the DC-SCM and primary OCP NIC connectors is common across all HPM classes.

- Consistent Riser locations are used across interoperable M-SDNO HPMs

- HPM width references refer to the following dimensions:

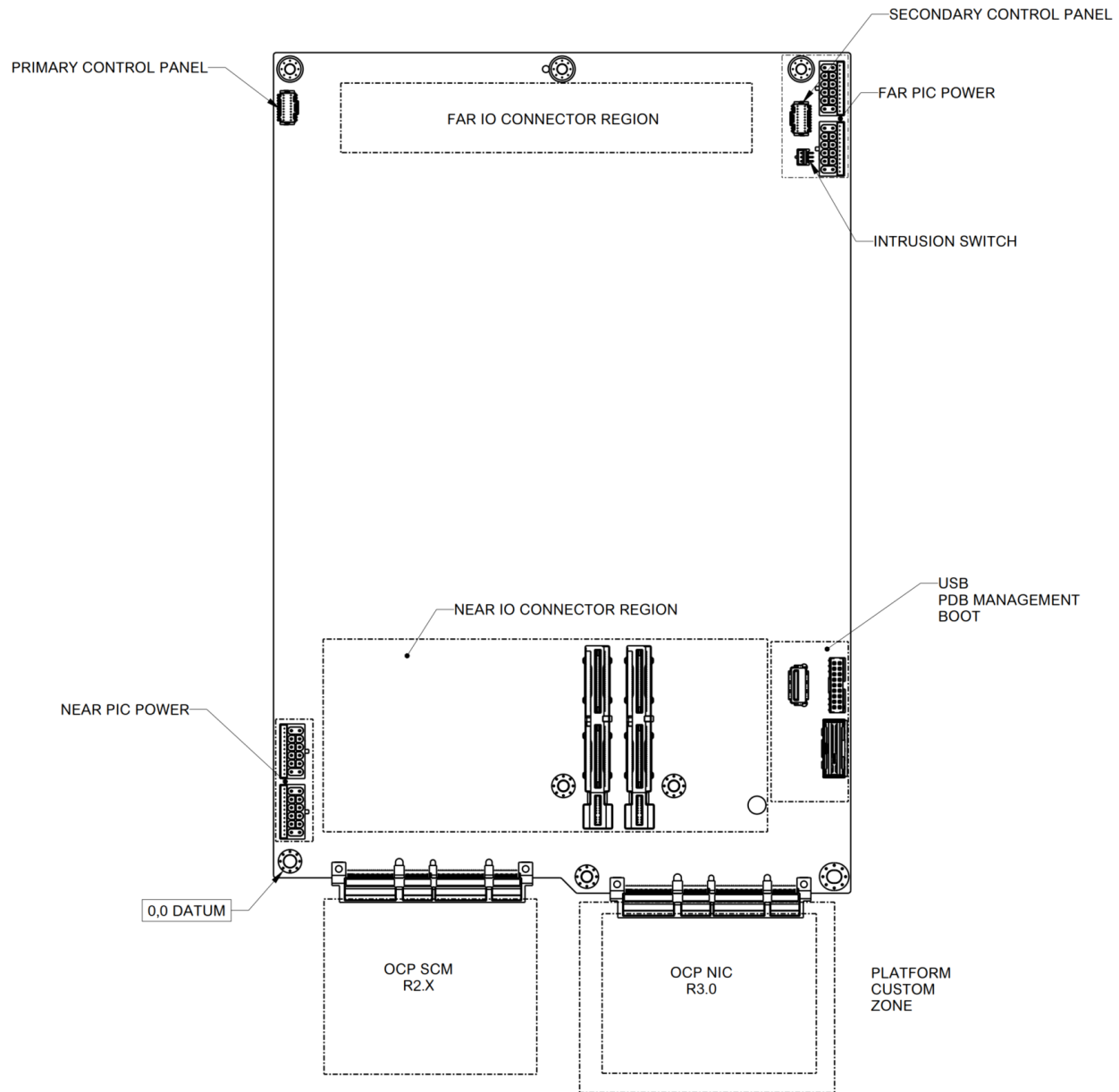
- 19" ½ Width refers to the common 210mm HPM width shared by all Class A HPMs
- 19" Full Width refers to the common 426mm HPM width shared by all Class C HPMs
- 21" ½ Width refers to the common 250mm HPM width shared by all Class B HPMs
- 21" Full Width refers to the common 512mm HPM width shared by all Class D HPMs

- HPMs narrower than 19" ½ Width are outside the scope of this specification due to the inability of supporting common DC-SCM R2.x and OCP NIC R3.0 connector locations as described in #2. The DC-MHS workgroup may consider narrower HPM designs in the future.

9.1 Class A HPM Layout

Class A is considered a half-width form factor optimized for 19" rack environments. **Figure 10** shows the layout and approximate locations of major subsystems of this HPM. IO Connector regions depicted are representative only and not strictly defined.

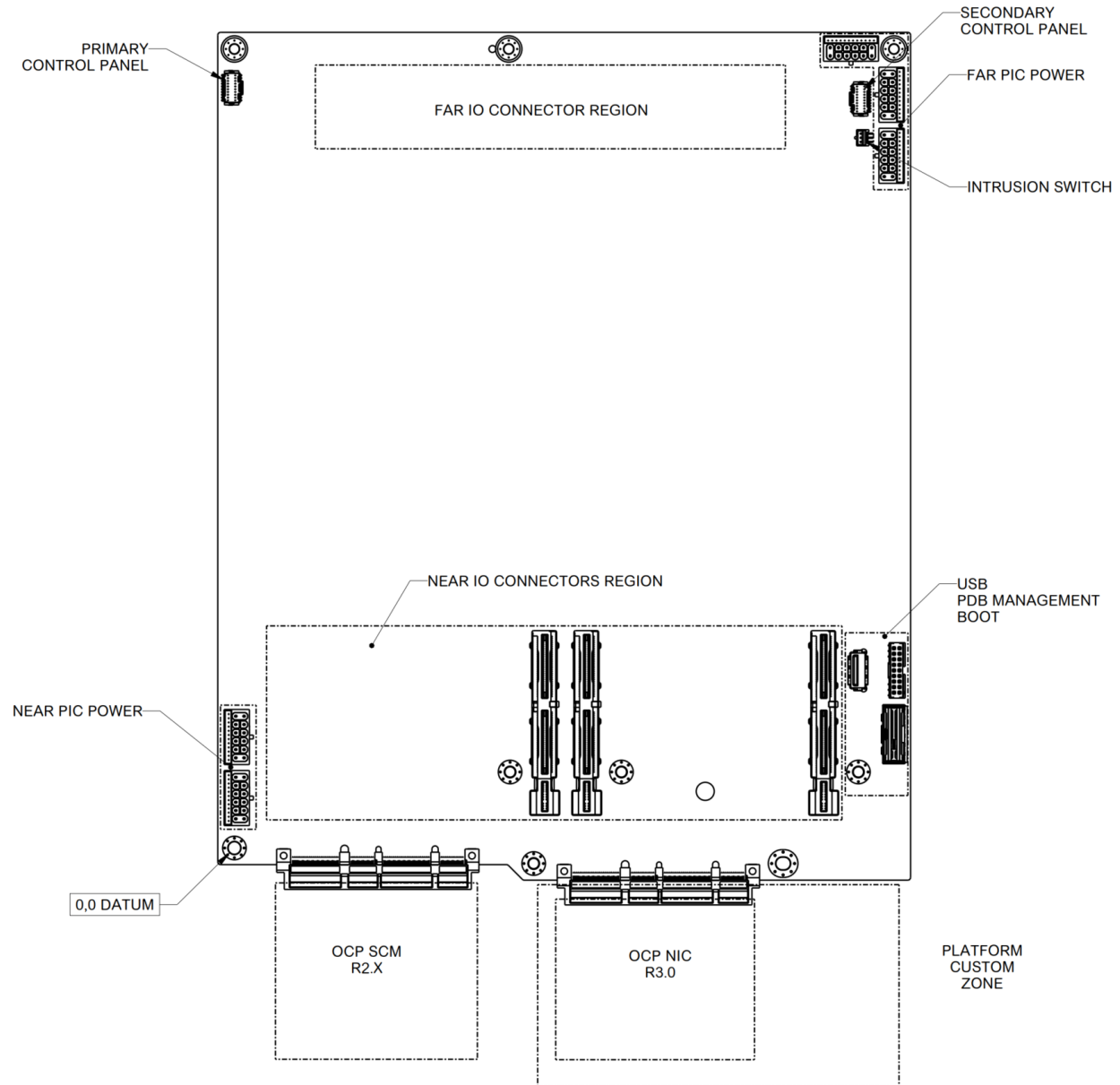
Figure 10: Class A HPM Overview (PRIMARY SIDE)



9.2 Class B HPM Layout

Class B is considered a half-width form factor optimized for 21" rack environments. **Figure 11** shows the layout and approximate locations of major subsystems of this HPM. IO Connector regions depicted are representative only and not strictly defined.

Figure 11: Class B HPM Overview (PRIMARY SIDE)

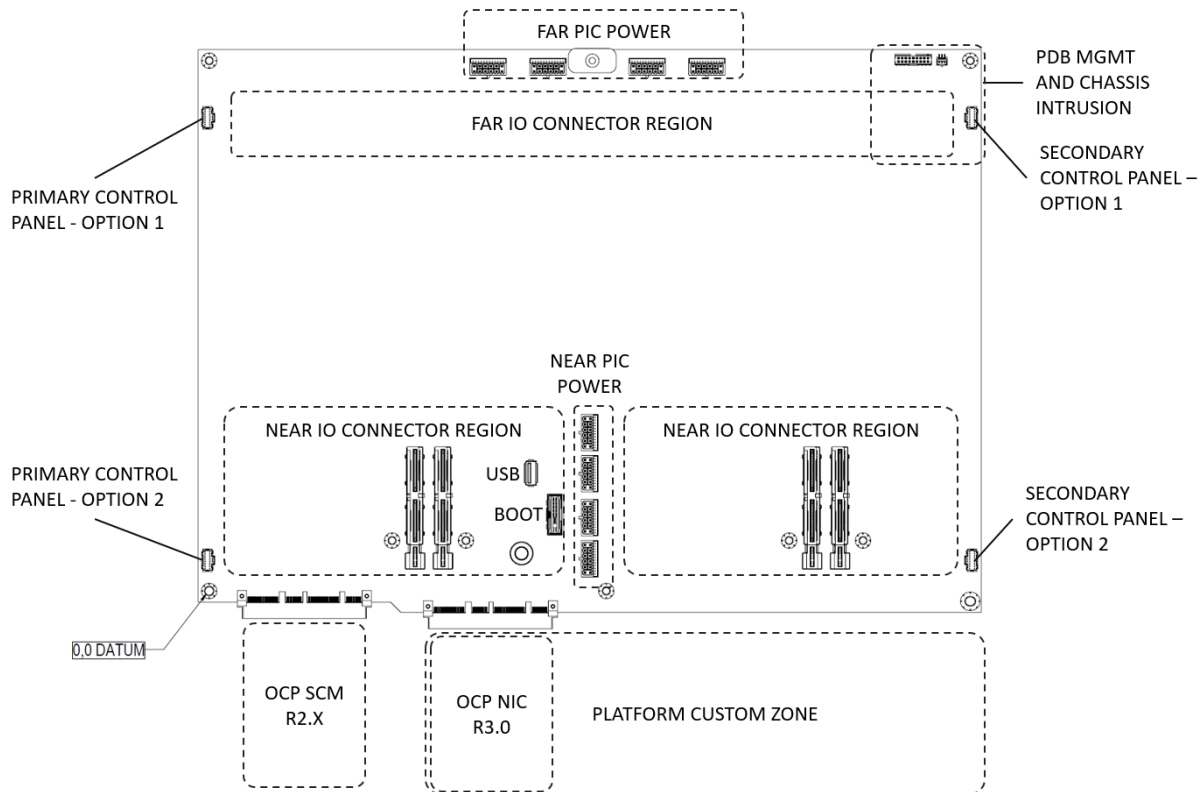


9.3 Class C HPM Layout

705 Class C is considered a full-width form factor optimized for 19" rack environments. **Figure 12** shows the layout and approximate locations of major subsystems of this HPM. IO Connector regions depicted are representative only and not strictly defined.

710

Figure 12: Class C HPM Overview (PRIMARY SIDE)



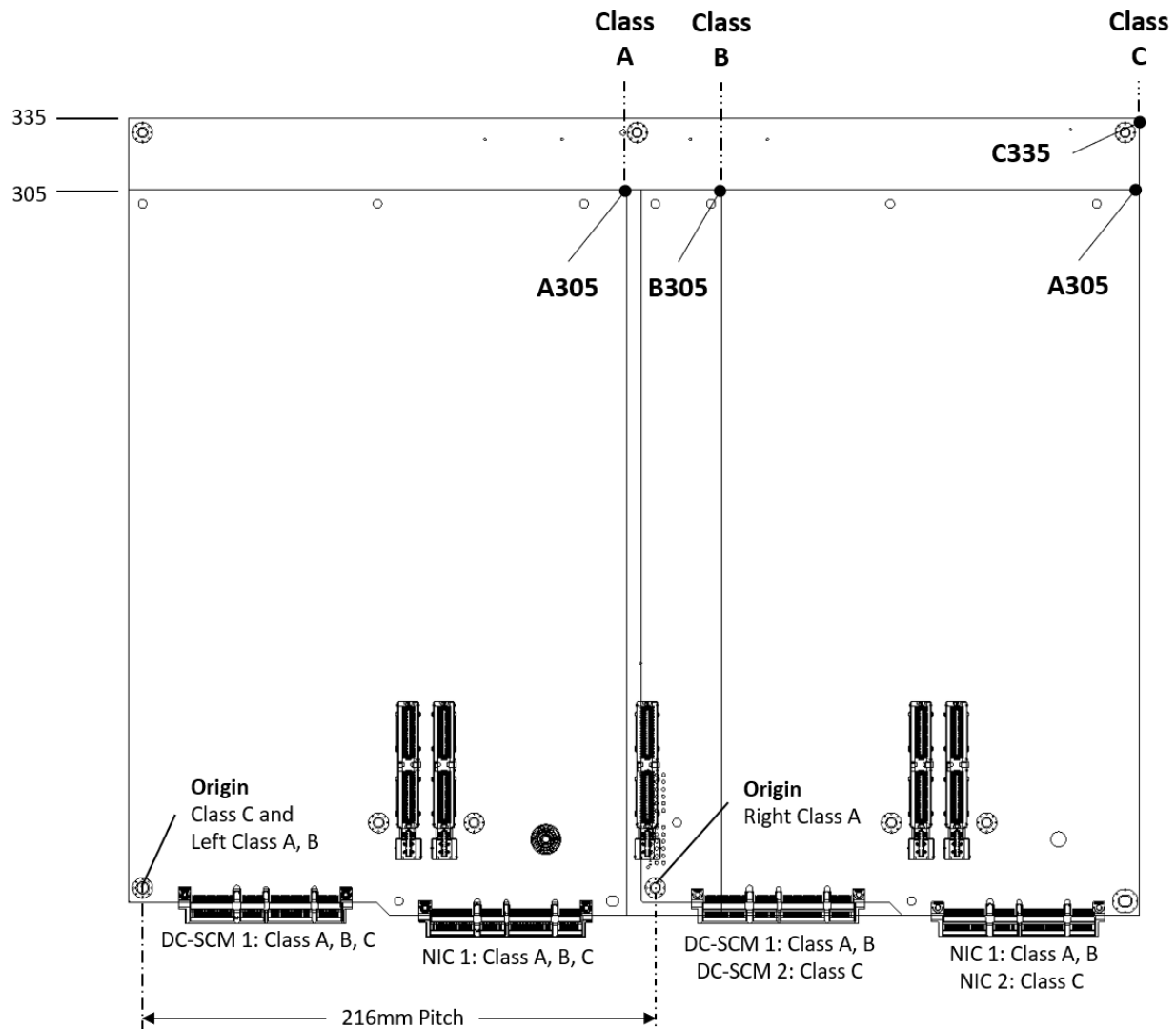
9.3.1 19" Common Chassis Supporting Classes A, B and C

HPM Classes A, B, and C are defined such that they can share a common 19" chassis if desired. The chassis could be designed to support a single Class C, a single Class B, or two Class A HPMs. A single Class A HPM is also possible.

Figure 13 illustrates the HPM positioning required for such a common chassis. The HPMs on the left are aligned at their origins. The Class A HPM on the right is offset from the left Class A HPM by 216mm. When positioned in this manner the DC-SCM R2.x, NIC R3, the SFF-TA-1033 riser connectors, and the HPM retention holes are all aligned. HPM trays are utilized to facilitate this chassis compatibility.

The HPM depths shown are illustrative only. The scheme can apply to any HPM depth combinations. The maximum supportable HPM depth is determined by the chassis design which is outside the scope of this specification. Whatever maximum depth is supported, any HPM of a lesser depth should also be be supportable.

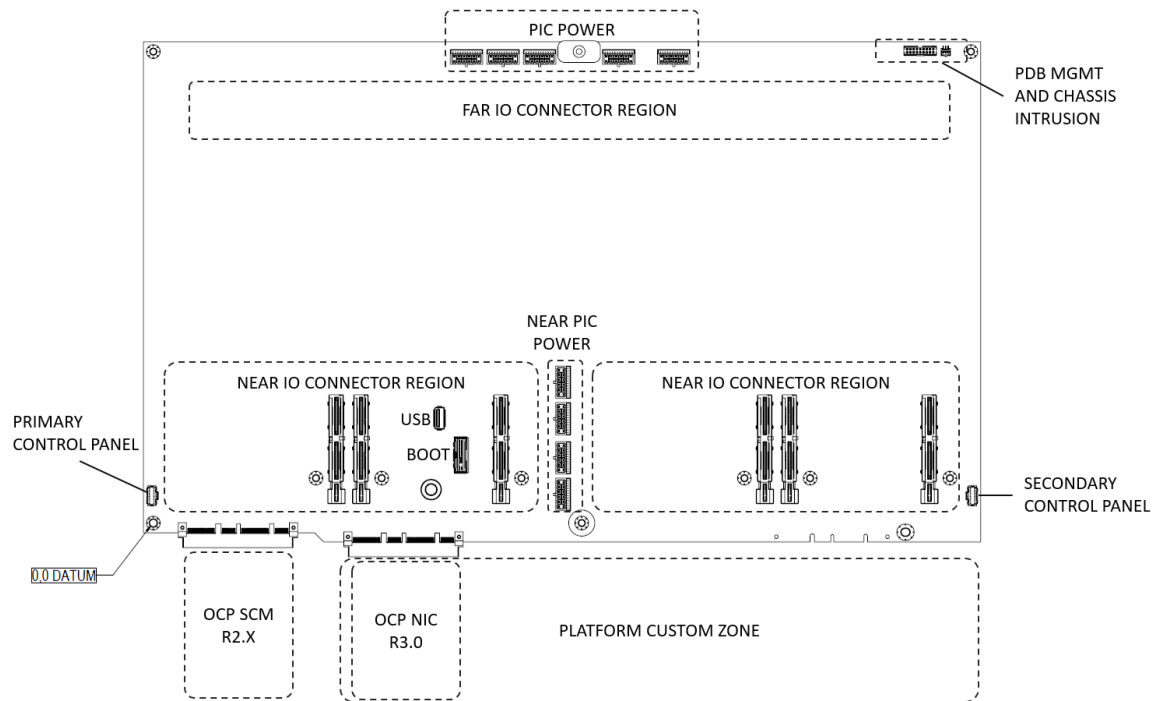
Figure 13: Common 19" Chassis Supporting Class A, B and C (PRIMARY SIDE)



9.4 Class D HPM Layout

Class D is considered a full-wide form factor optimized for 21" rack environments. **Figure 14** shows the layout and approximate locations of major subsystems of this HPM. IO Connector regions depicted are representative only and not strictly defined.

Figure 14: Class D HPM Overview (PRIMARY SIDE)



Implementors Note:

The M-SDNO HPM definition philosophy attempts to enable a level of compatibility between HPM classes including consistency of connector locations. However, there are some notable exceptions made to better align some HPM definitions with their targeted rack environment.

As described in **Section 8.4**, Class D is optimized for 21" rack environments. Therefore, the Class D definition assumes the HPM Near Side edge is on the cold isle (i.e., front IO) and a power distribution board is positioned closer to the HPM Far Side edge. Given these assumptions, the Class D control panel connectors are placed at the Near Side edge and the power management connector is placed at the Far Side edge to minimize cable routing. You may note this connector placement is different from Class A and Class B. Class C provides the option for the HPM designer to place control panel connectors on the Far Side (for commonality with Class A and B) or on the Near Side if the HPM is optimized for front IO similar to Class D.

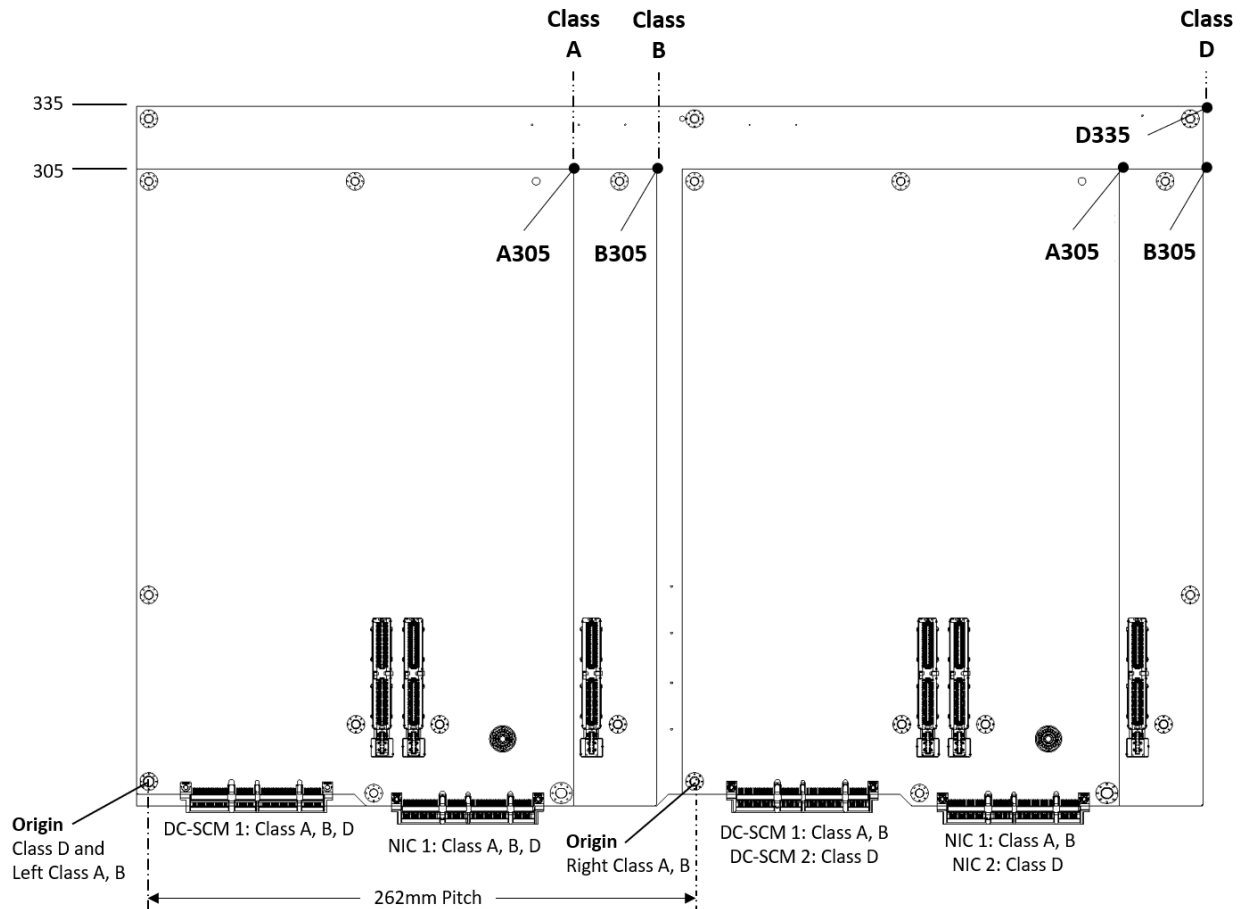
9.4.1 21" Common Chassis Supporting Classes A, B, and D

HPM Classes A, B, and D are defined such that they can share a common chassis if desired. This common chassis must be a 21" rack full width form factor. The chassis could be designed to support a single Class D, two Class A, or two Class B HPMs. A single Class A and a single Class B in the same chassis is also possible.

Figure 15 illustrates the HPM positioning required for such a common chassis. The HPMs on the left are aligned at their origins. The HPMs on the right are offset from the left HPMs by 262mm. When positioned in this manner the DC-SCM R2.x, NIC R3, the SFF-TA-1033 riser connectors, and the HPM retention holes are all aligned. HPM trays are utilized to facilitate this chassis compatibility.

The HPM depths shown are illustrative only. The scheme can apply to any HPM depth combinations. The maximum supportable HPM depth is determined by the chassis design which is outside the scope of this specification. Whatever maximum depth is supported, any HPM of a lesser depth should also be supportable.

Figure 15: Common 21" Chassis Layout for Class A, B and D (PRIMARY SIDE)



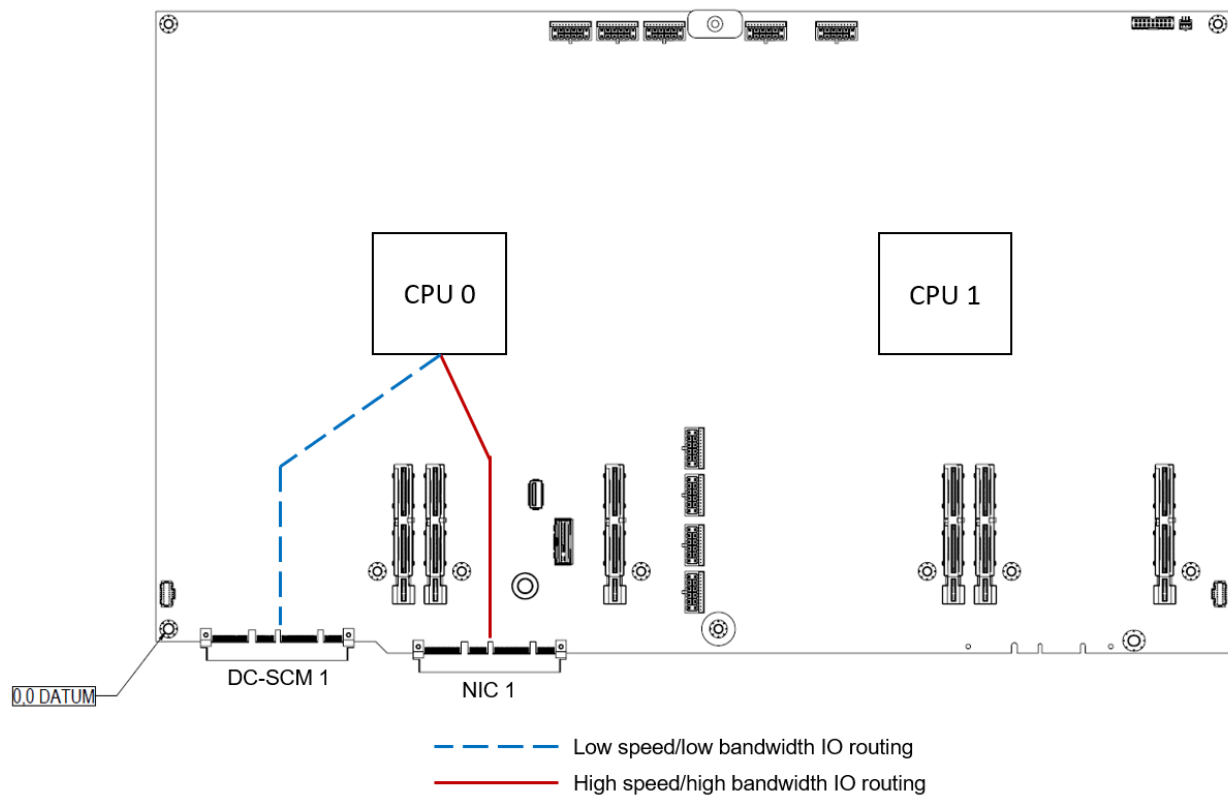
9.5 Class C and D Two Socket (CPU) Assumptions

The primary NIC R3.0 is positioned to the left, as seen in **Figure 16**, and is based on these two assumptions:

- In a two socket (CPU) HPM the first/boot CPU is positioned to the left.
- OCP NIC R3.0 is directly routed through the HPM PCB to the first/boot CPU.

The OCP NIC R3.0 is intended to be closer to this boot CPU to best enable the high-speed IO routing. The OCP NIC R3.0 will usually require high bandwidth routing, and thus should be optimized for material selection and cost impacts.

Figure 16: M-SDNO HPM First CPU Assumed Position (Class D PRIMARY SIDE Shown)



10 Mechanical Requirements

In addition to the drawings and details within this document, DFX/CAD files will be provided for further detail (**Section 14.5: M-SDNO CAD Files**).

Unless otherwise specified all units are in mm.

Unless otherwise specified, PCB dimensions shown in this specification shall comply to **Table 2**.

Table 2: Standard Tolerances

Dimension Type	Tolerance, unless otherwise specified
FROM Origin/Datum hole center TO round fiducial center	+/- 0.076mm (+/- 0.003 inch)
FROM Origin/Datum hole center TO profiled card edge	+/- 0.254mm (+/- 0.010 inch)
FROM Origin/Datum hole center TO drilled hole center	+/- 0.127mm (+/- 0.005 inch)
FROM Profiled card edge TO profiled card edge	+/- 0.127mm (+/- 0.005 inch)
Feature of size (hole diameter, slot width, etc.)	+/- 0.100mm (+/- 0.004 inch)
PCB thickness	+/- 10% of nominal

Route KOZ's referenced in this specification, at a minimum, refer to surface layers and microstrip routing. Further application of the Route KOZ to other layers is the choice of the HPM designer and/or Design specification.

10.1 HPM Outlines

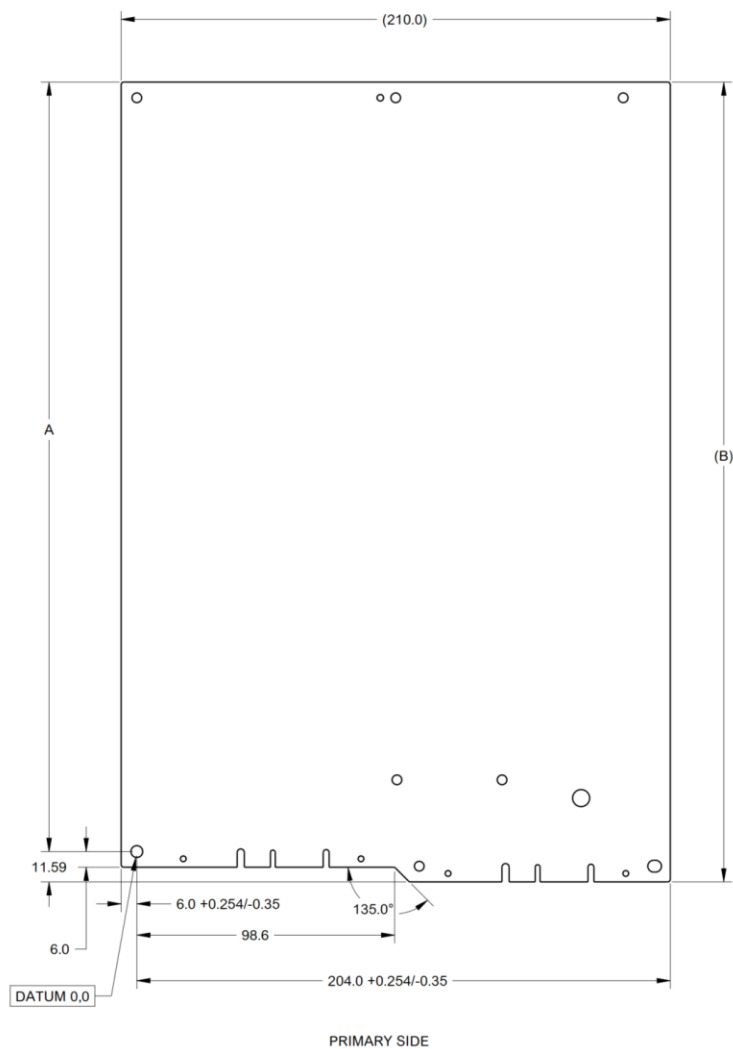
There are four classes of HPMs in this specification release, each class has three recommended depths aligned to Common Chassis Intervals. The required board outlines are defined in **Figure 17** to **Figure 20**, M-SDNO HPMs shall comply with these board outlines.

10.1.1 Class A HPM Board Outline

The Class A HPM is defined as a fixed 210mm width and an allowed depth ranging between 305.59mm and 555.59mm. Although a compliant HPM may be designed to any depth within this range, there exists three distinct Common Chassis Intervals (CCI) which it is recommended that HPM designers attempt to utilize for maximum ecosystem compatibility.

Note that **Figure 17** contains unique tolerances when dimensioning the HPM width. These asymmetric width tolerances allow the HPM designer to optionally choose to set the nominal total width to 209.55mm if desired for use within a single-height half-width (SHHW) “brick”.

Figure 17: Class A HPM Board Outline (PRIMARY SIDE)

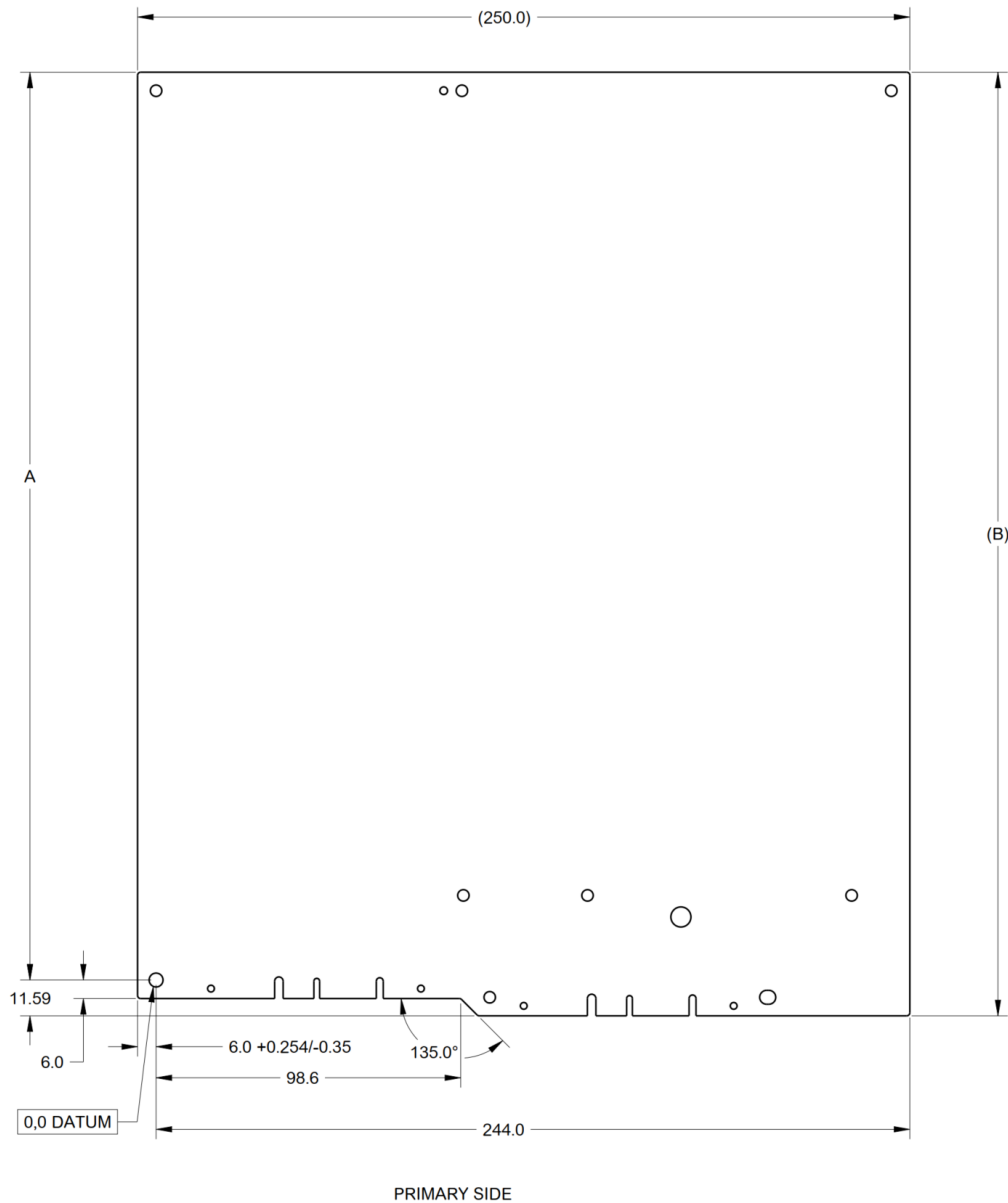


HPM Designator	A	B (Reference)
A305	294mm	305.59mm
A335	324mm	335.59mm
A555	544mm	555.59mm

10.1.2 Class B HPM Board Outline

795 The Class B HPM is defined as a fixed 250mm width and an allowed depth ranging between 305.59mm and 555.59mm. Although a compliant HPM may be designed to any depth within this range, there exists three distinct Common Chassis Intervals (CCI) which it is recommended that HPM designers attempt to utilize for maximum ecosystem compatibility.

Figure 18: Class B HPM Board Outline (PRIMARY SIDE)

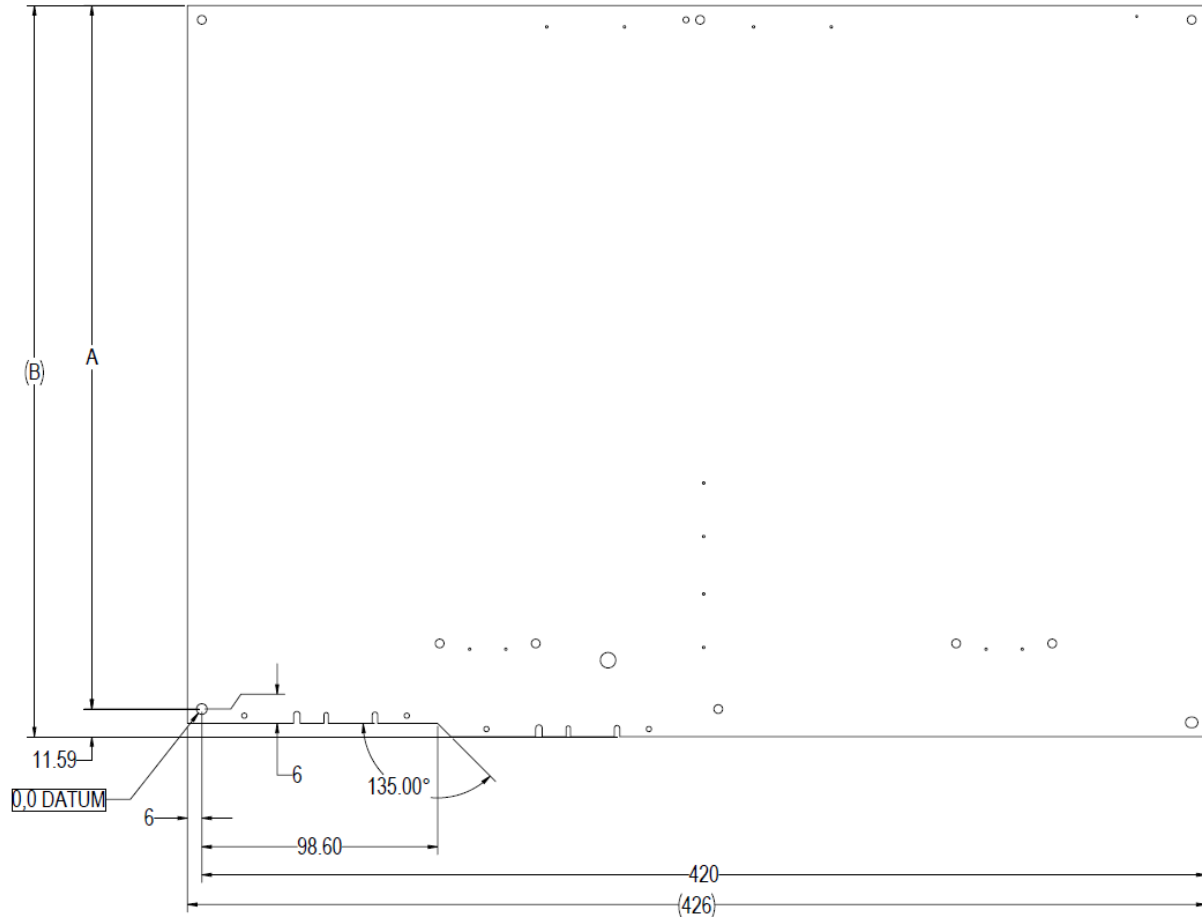


HPM Designator	A	B (Reference)
B305	294mm	305.59mm
B335	324mm	335.59mm
B555	544mm	555.59mm

10.1.3 Class C HPM Board Outline

800 The Class C HPM is defined as a fixed 426mm width and an allowed depth ranging between 305.59mm and 555.59mm. Although a compliant HPM may be designed to any depth within this range, there exists three distinct Common Chassis Intervals (CCI) which it is recommended that HPM designers attempt to utilize for maximum ecosystem compatibility.

805 **Figure 19: Class C HPM Board Outline (PRIMARY SIDE)**



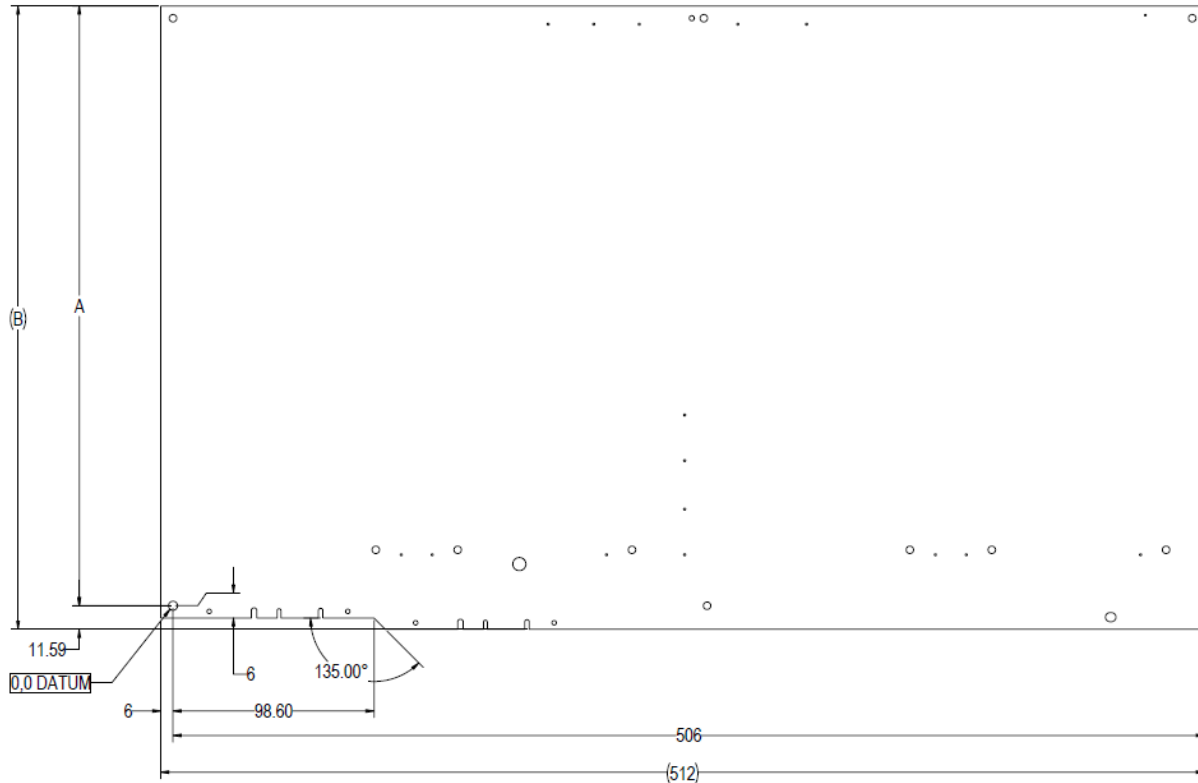
PRIMARY SIDE

HPM Designator	A	B (Reference)
C305	294mm	305.59mm
C335	324mm	335.59mm
C555	544mm	555.59mm

10.1.4 Class D HPM Board Outline

810 The Class D HPM is defined as a fixed 512mm width and an allowed depth ranging between 305.59mm and 555.59mm. Although a compliant HPM may be designed to any depth within this range, there exists three distinct Common Chassis Intervals (CCI) which it is recommended that HPM designers attempt to utilize for maximum ecosystem compatibility.

Figure 20: Class D HPM Board Outline (PRIMARY SIDE)



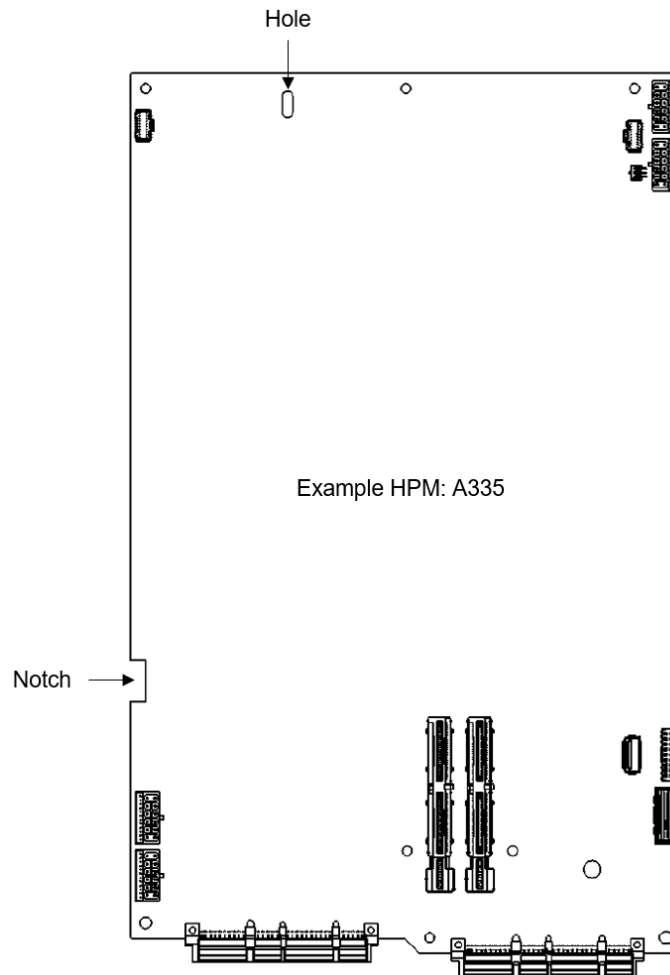
PRIMARY SIDE

HPM Designator	A	B (Reference)
D305	294mm	305.59mm
D335	324mm	335.59mm
D555	544mm	555.59mm

10.1.5 Allowance for Negative PCB Features

All HPM Classes may include “negative PCB features” with the noted limitations. A negative PCB feature is defined as removal of PCB material in localized areas of the HPM outline. Examples of negative PCB features include notches along a board edge or openings of any geometric shape within the HPM outline. See **Figure 21** for illustrative example.

Figure 21: A335 HPM with Compliant Negative PCB Features



All negative PCB features implemented shall comply to the following restrictions:

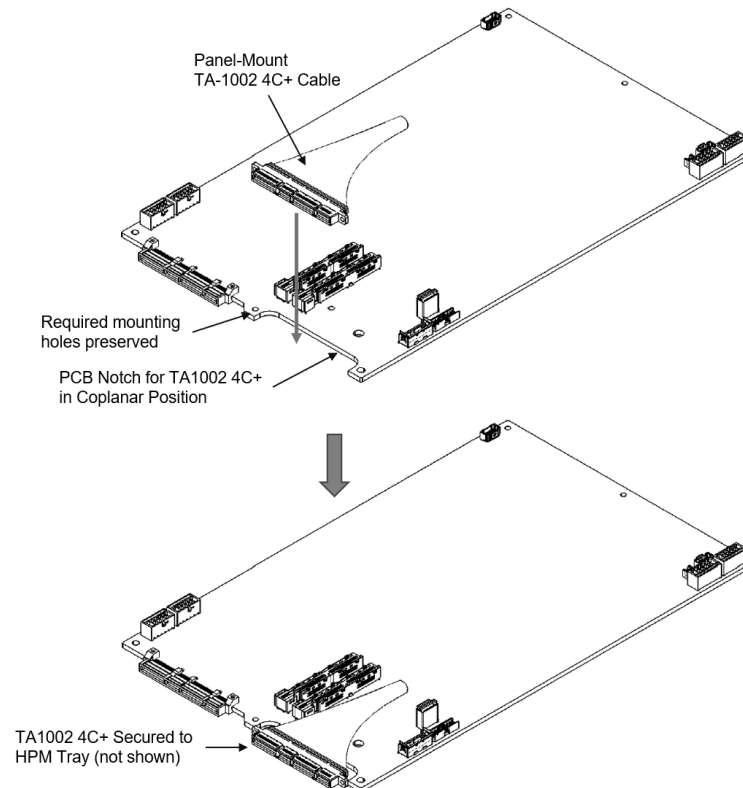
1. Negative PCB features shall not violate or conflict with any required features such as mounting holes and connector placement.
2. The negative PCB feature shall not extend the full length of the left or right edge of an HPM (i.e., this feature shall not be used to essentially create a non-standard HPM width).

Implementors Notes:

HPM-level and system-level manufacturing, handling, shipping, and operational environments must be considered by the HPM designer. When implementing negative PCB features the HPM designer should consider the implications on HPM structural integrity.

The use of a negative PCB feature can afford the option of a chassis or HPM tray feature to reside within this evacuated area. However, it should be noted that if this chassis or HPM tray feature must always be present, then other specification compliant HPMs that do not have these negative PCB features may not be interoperable with this system. An ideal system implementation would not require these negative PCB features to be present on all supported HPMs.

An example application of a negative PCB feature is the use of a notch at the M-SDNO reference OCP NIC3 connector location combined with the use of a cabled panel-mount TA-1002 4C+ connector. The use of the cabled NIC3 connector enables flexible NIC3 location within the system. The shown notch preserves the option to position the NIC3 in the reference location, thereby mimicking a straddle-mount coplanar 4C+ on the HPM. The PCB notch geometry would be a function of the specific panel-mount 4C+ connector chosen for this application.



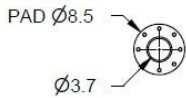
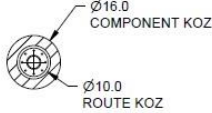
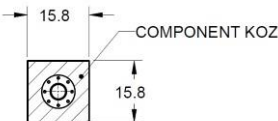
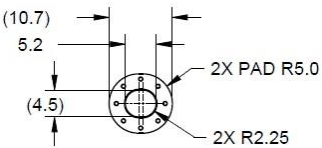
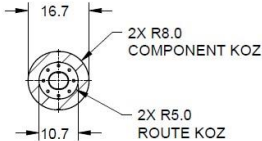
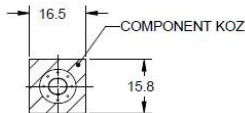
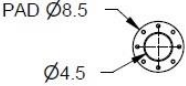
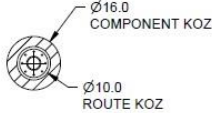
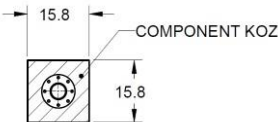
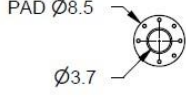
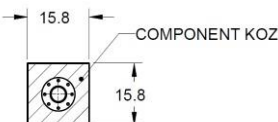
10.2 Board Datum and Mounting Hole Information

835 All M-SDNO board Classes leverage a common datum location at the center of a specific near side edge mounting hole as illustrated in **Figure 23** to **Figure 26**. This allows for fixed elements (riser connectors, peripheral connectors, ...) to have a common reference across all board Classes.

840 Detailed hole information common to all board Classes are provided in **Figure 22**. The vias that are shown in Figures are for reference only. Via requirements are NOT in scope of this specification. All holes shall adhere to the specified size, ground pad dimensions, component KOZ and route KOZ.

845 The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension (i.e. a DIMM connector), it is considered more robust, and may encroach on the Component KOZ's.

Figure 22: Hole Detail Reference

	Hole and Pad Sizes	Top Side KOZs	Bottom Side KOZs
DETAIL A Standard Mounting Hole			
DETAIL B Unique Alignment Slot			
DETAIL C Unique Alignment Hole			
DETAIL D Riser Retention Holes			

850 It is expected that HPM designers will add additional mounting holes based on their HPM layout. All additional holes shall adhere to Standard Mounting Hole requirements (Detail A in **Figure 22**).

A design should follow good engineering practices in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

855 There are required holes associated with each Near IO fixed riser location (Detail D in **Figure 22**) that shall be implemented regardless of whether the riser connector is implemented. The intent of requiring these holes is to always make retention holes available to system designers (including systems with cable based I/O).

860 Riser retention holes are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). System designers may choose the hardware and utilization method for riser retention.

Required and recommended board mounting hole locations are specified for M-SDNO HPM Class A, B, C, and D in **Figure 23 to Figure 26**.

Implementors Note:

The PCB Datum hole (Detail C) is defined such that a collared standoff with tight tolerance fit can be used to control X-Y tolerances in HPM mounting. Additionally, a slotted hole (Detail B) is defined to control rotation around the datum, by allowing, as an example, a collared standoff to be used with tight fit to the top/bottom edge of the slot.

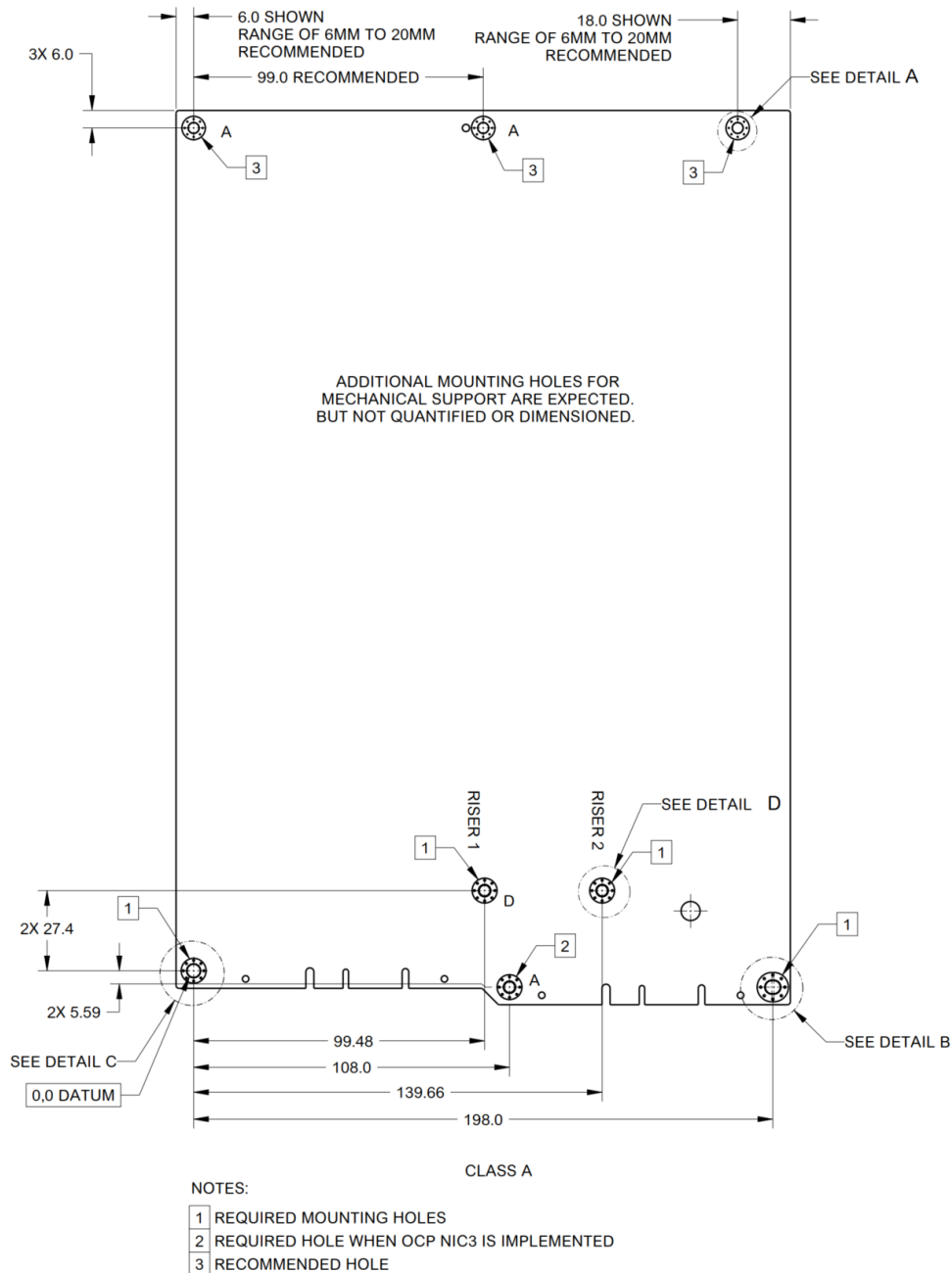
All other mounting holes follow standard mounting hole guidance (Detail A). These mounting holes are expected to have clearance fits to screw hardware.

865 10.2.1 Class A HPM Mounting/Riser Holes

There are four required mounting/riser holes on the Class A near side that shall be implemented. There is one additional required near side hole if the OCP NIC3 is implemented.

870 There are three recommended mounting holes on the Class A Far Side. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm with a recommended span of 99mm. **Figure 23** shows the placement of the required and recommended holes.

Figure 23: Class A HPM Mounting/Riser Holes (PRIMARY SIDE)

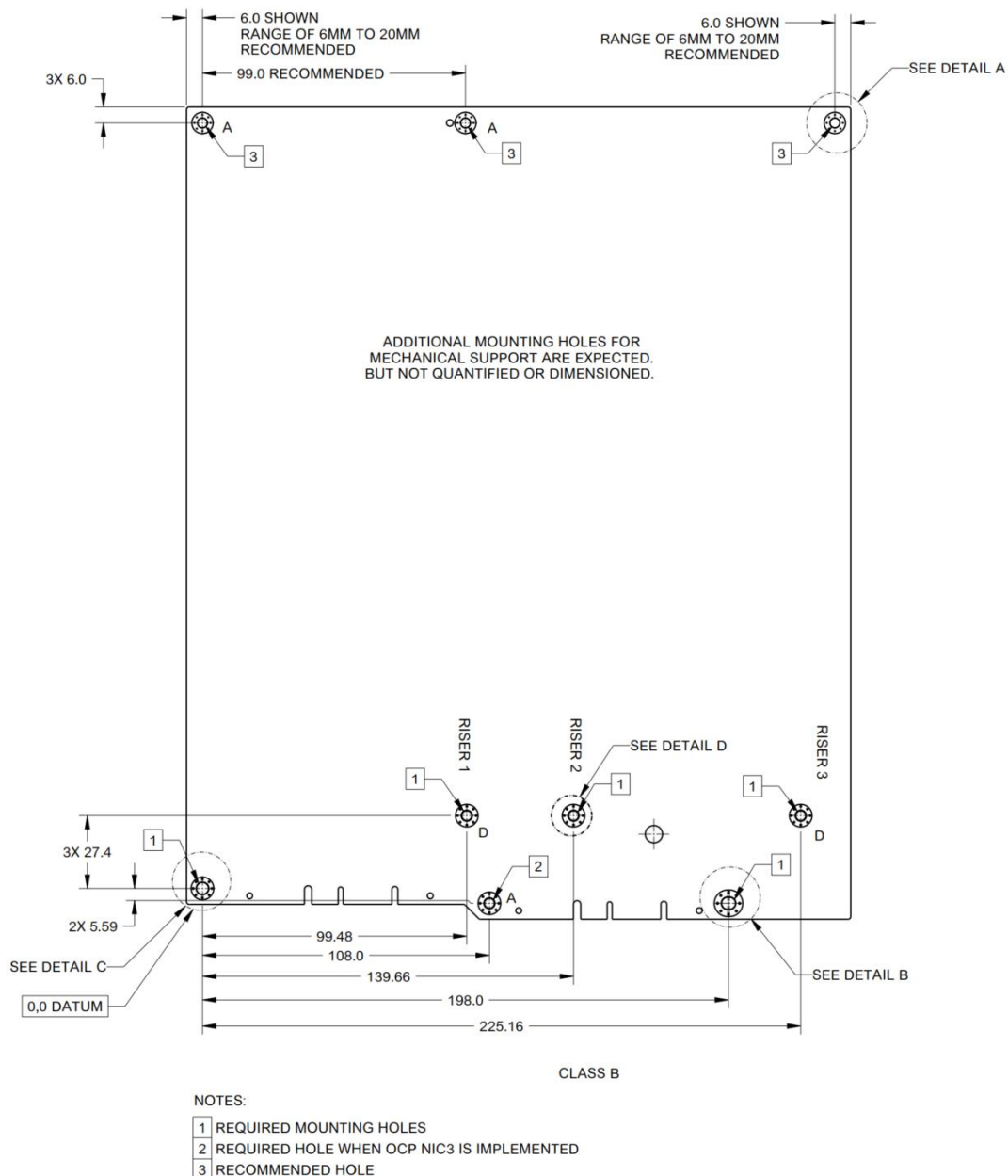


10.2.2 Class B HPM Mounting/Riser Holes

875 There are five required mounting/riser holes on the Class B near side that shall be implemented.
There is one additional required near side hole if the OCP NIC3 is implemented. Additional recommended mounting holes for specific optional near side custom zone implementations are indicated in **Section 10.11: Class B Platform Custom Zone**.

880 There are three recommended mounting holes on the Class B Far Side. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm with a recommended span of 99mm. **Figure 24** shows the placement of the required and recommended holes.

Figure 24: Class B HPM Mounting/Riser Holes (PRIMARY SIDE)

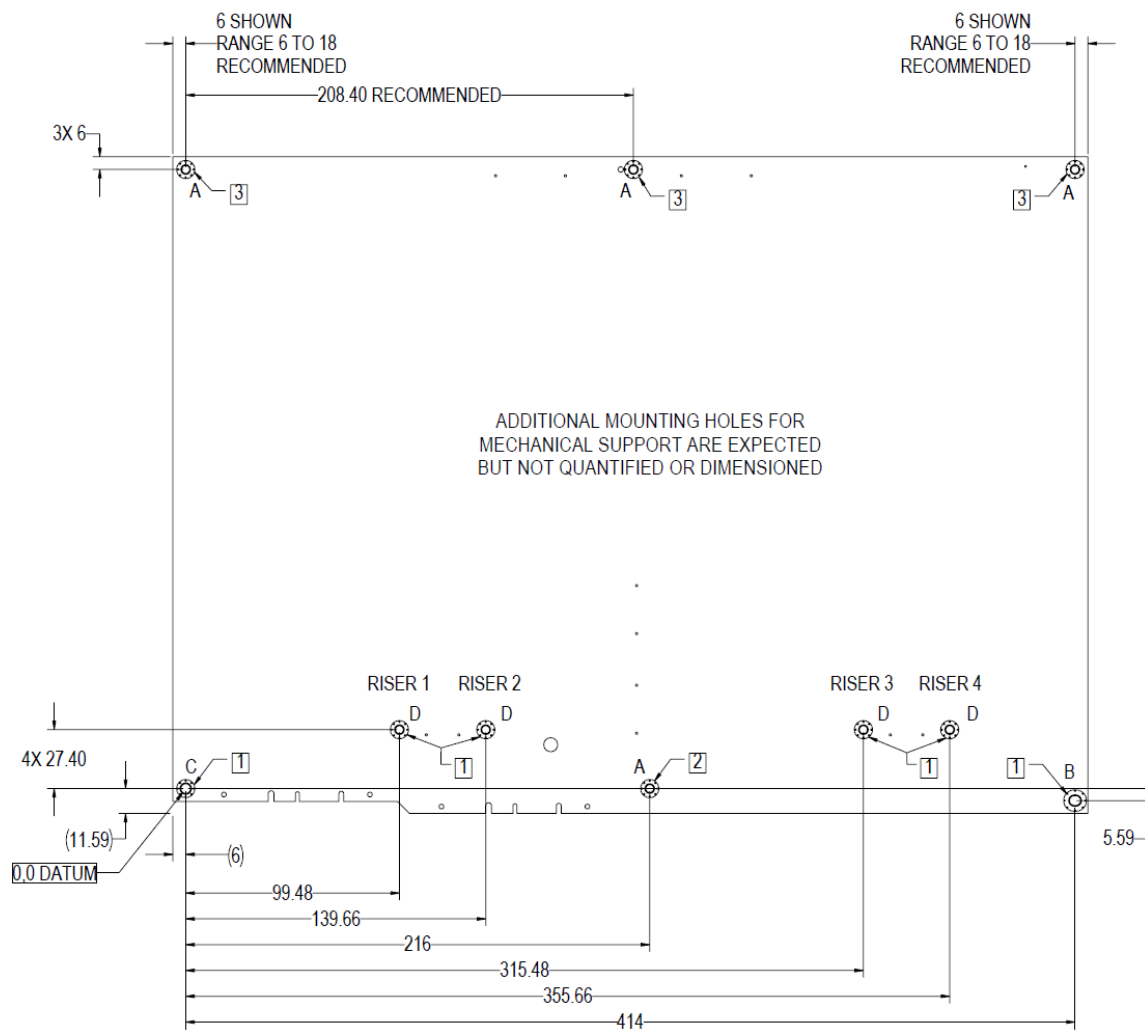


885 10.2.3 Class C HPM Mounting/Riser Holes

There are six required mounting/riser holes on the Class C near side that shall be implemented. There is one additional required near side hole if the OCP NIC3 is implemented. Additional recommended mounting holes for specific optional near side custom zone implementations are indicated in **Section 10.12: Class C Platform Custom Zone**.

890 There are five recommended mounting holes on the Class C Far Side. **Figure 25** shows the placement of the required and recommended holes. The position of the remaining two recommended mounting holes (not shown) is at the discretion of the HPM designer. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm.

895 **Figure 25: Class C HPM Mounting/Riser Holes (PRIMARY SIDE)**



PRIMARY SIDE

NOTES:

- [1] REQUIRED MOUNTING HOLE.
- [2] REQUIRED MOUNTING HOLE WHEN OCP NIC3 IS IMPLEMENTED.
- [3] RECOMMENDED MOUNTING HOLE.

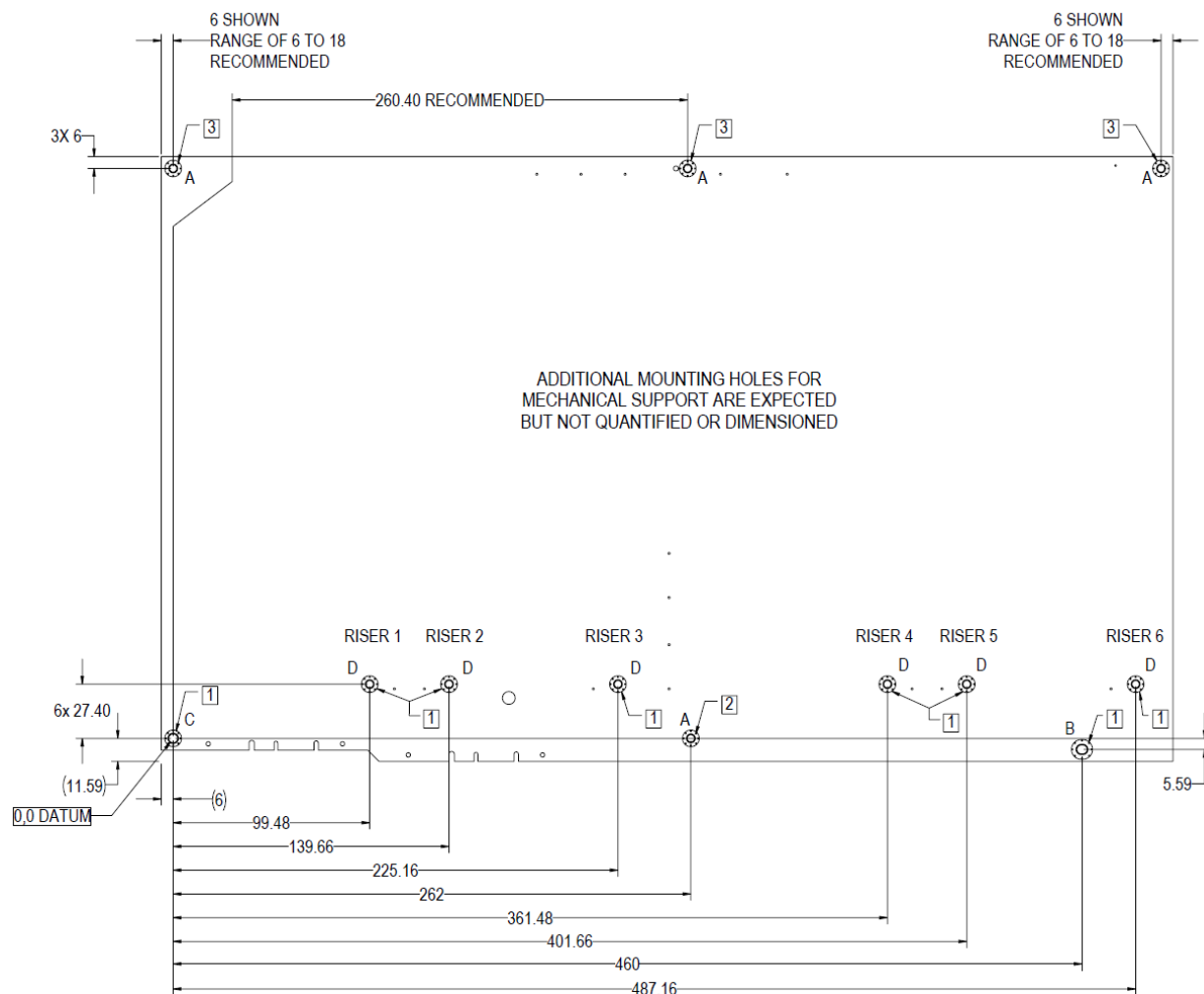
10.2.4 Class D HPM Mounting/Riser Holes

There are eight required mounting/riser holes on the Class D near side that shall be implemented. There is one additional required near side hole if the OCP NIC3 is implemented.

900 Additional recommended mounting holes for specific optional near side custom zone implementations are indicated in **Section 10.13: Class D Platform Custom Zone**.

There are five recommended mounting holes on the Class D Far Side. **Figure 26** shows the placement of the required and recommended holes. The position of the remaining two recommended mounting holes (not shown) is at the discretion of the HPM designer. It is further
 905 recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm.

Figure 26: Class D HPM Mounting/Riser Holes (PRIMARY SIDE)



PRIMARY SIDE

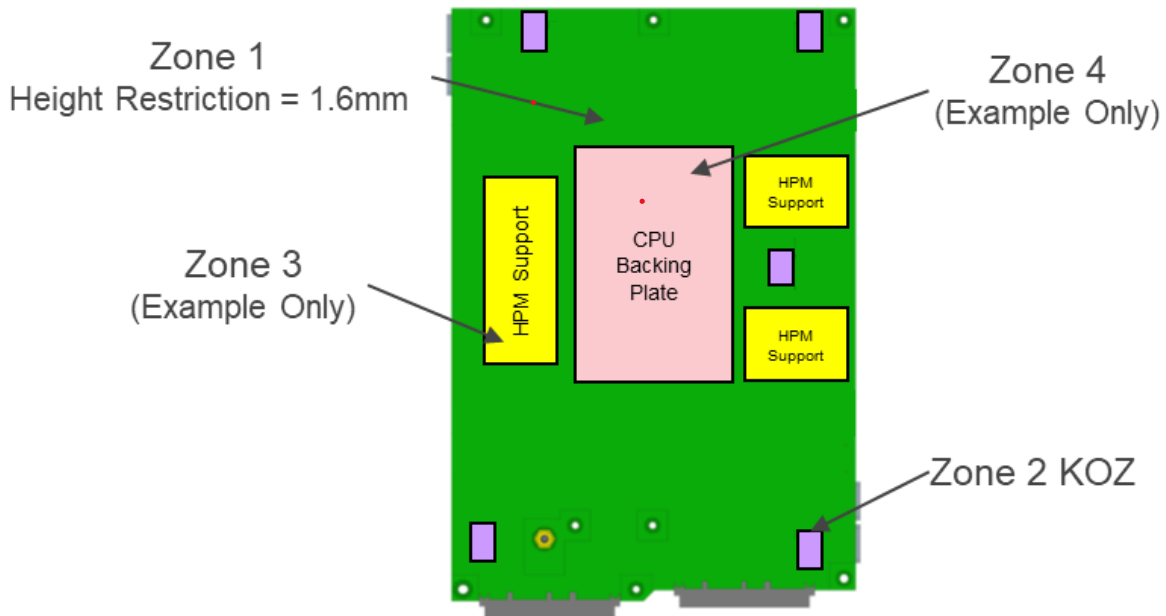
NOTES:

- ① REQUIRED MOUNTING HOLE.
- ② REQUIRED MOUNTING HOLE WHEN OCP NIC3 IS IMPLEMENTED.
- ③ RECOMMENDED MOUNTING HOLE.

10.3 Secondary Side Zones and Height Restrictions

910 There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 27**. Each zone serves a unique purpose. Zones 1, 2, 3 and 4 define different requirements for compliance.

Figure 27: Secondary Side Zone Definitions (Class A Example Depicted)



915

10.3.1 Zone 1: Secondary Side Height Restriction

Zone 1 universally applies to the entire secondary side of the HPM, except for the defined Zones 2, 3, and 4. HPM electrical components are expected to utilize Zone 1.

920 All M-SDNO HPMs shall implement the Zone 1 universal secondary side component height restriction of 1.6mm for all board Classes. This requirement ensures HPM component clearances to chassis base or board pan structures. This is especially important with a max allowable board thickness as defined in **Section 10.4: HPM Board and Assembly Thickness**.

925

10.3.1.1 Zone 1 Exceptions for Secondary Side Tall Components

In some instances, an HPM Designer may desire placement of tall secondary side components (such as special capacitors) that exceed the secondary side height restriction. Although this should be avoided, an HPM Designer may implement local exceptions if the following conditions are met:

930

1. Exceptions are contained to small areas of the secondary side and shall not exceed 400mm² area per instance.
2. No two instances of a secondary side exception shall be closer than 10mm, as to not drive excessive cutouts in Chassis-to-HPM bracketry.

935

It is recommended that (HPM Thickness + Height of Components) in Exception Areas never exceed 5.2mm. This total height enables common 2mm components on all M-SDNO compliant HPM thicknesses while mitigating potential system compatibility issues, for example:

- 5.2mm – 2.36mm thick HPM = 2.84mm max component thickness
- 5.2mm – 3.18mm thick HPM = 2.02mm max component thickness

940

Care should be taken to ensure that there is no risk if components in exception areas touch uninsulated chassis elements.

Implementors Note:

Secondary side exceptions for tall components may cause compatibility challenges between the HPM and System. HPM designers should work closely with the intended System Designers to ensure the exception locations and specific component heights are acceptable.

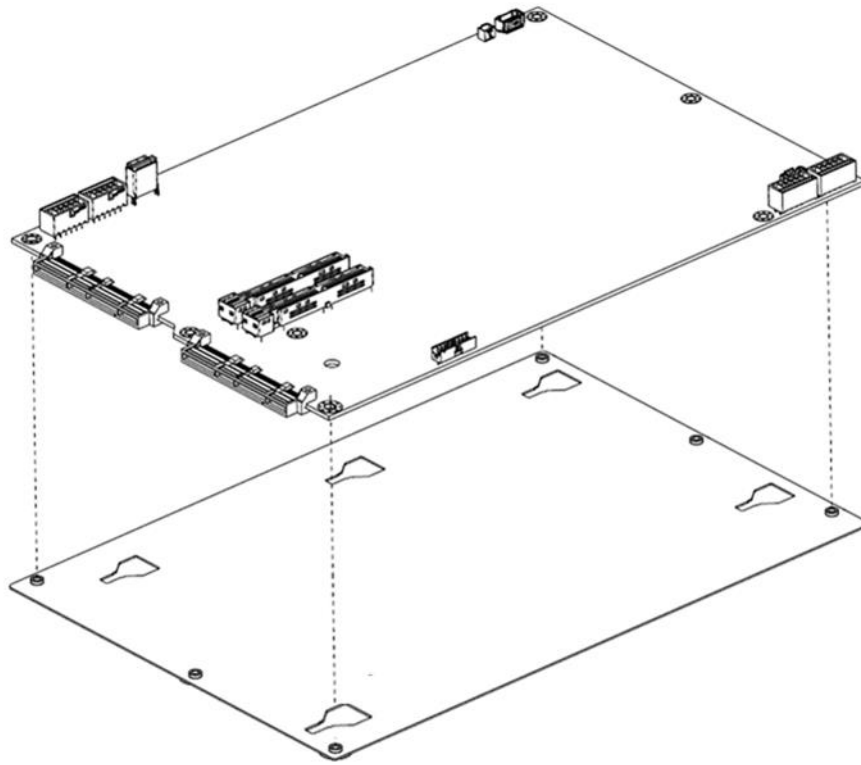
Numerous considerations outside the scope of this specification will determine the severity of compatibility issues. Examples include but are not limited to shock and vibration, chassis mechanical features, HPM uniformity, tolerancing, solder thickness, etc.

10.3.2 Zone 2: Chassis to HPM Bracket (Board Pan) KOZ Requirements

945 M-SDNO HPMs allow for a Chassis-to-Board Bracket (Board Pan) which enables different board layouts (and mounting hole locations) between HPM Classes and Compute Core designs, while maintaining compatibility to a common chassis.

An example M-SDNO Class A Board Pan is shown in **Figure 28**.

Figure 28: Example of Chassis-to-Board Bracket (Board Pan)



Implementors Note:

While most monolithic server designs benefit from a Board Pan, it is NOT expected that all systems supporting M-SDNO HPMs will require a Board Pan. Specifically, sled-based designs common in multi-node systems typically do not require a board pan. An example sled based secondary side zone stack-up can be derived by referring to Table 3 and replacing the space allocated to item 'F' and 'G' with the sled mechanicals.

950

A supporting chassis base must provide geometry to interface the cutouts on the Chassis-to-Board Bracket (Board Pan). For an example of a chassis hook concept, see **Section 14.3 Example Chassis Base Geometry for Chassis-to-Board Bracket interface**. The geometry of the Board Bracket is not specified and is a design choice for the System Designer.

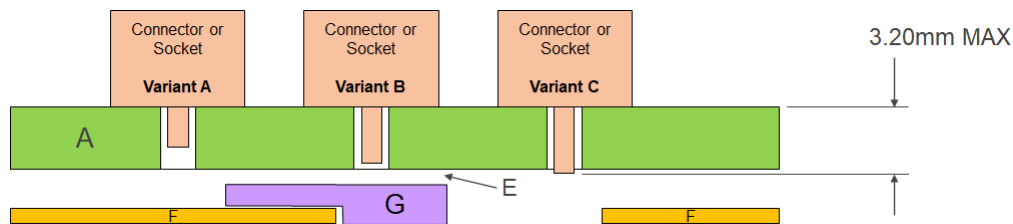
Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb shall be 3.20mm MAX such that it will not interfere with chassis hook features.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout.

Implementors Note:

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly. Refer to **Table 3: Example Z-Height Compliant Stack-Up, Per Zone** for details on 'A', 'E', 'F' and 'G'.



Each M-SDNO HPM Class shall support required zero height KOZ locations for chassis hook features that interface between the chassis base and the chassis to board bracket (board pan) as depicted in Figure 29 through Figure 36.

The floating far side edge KOZs shall be required for all HPM depths.

For each HPM Class, two drawings are provided.

Figure 29, Figure 31, Figure 33, and Figure 35 depict all KOZ locations for HPMs $\leq 372.5\text{mm}$ in length from the datum. **Figure 30, Figure 32, Figure 34, and Figure 36** depict an additional row of KOZs for HPMs $> 372.5\text{mm}$ in length from the datum.

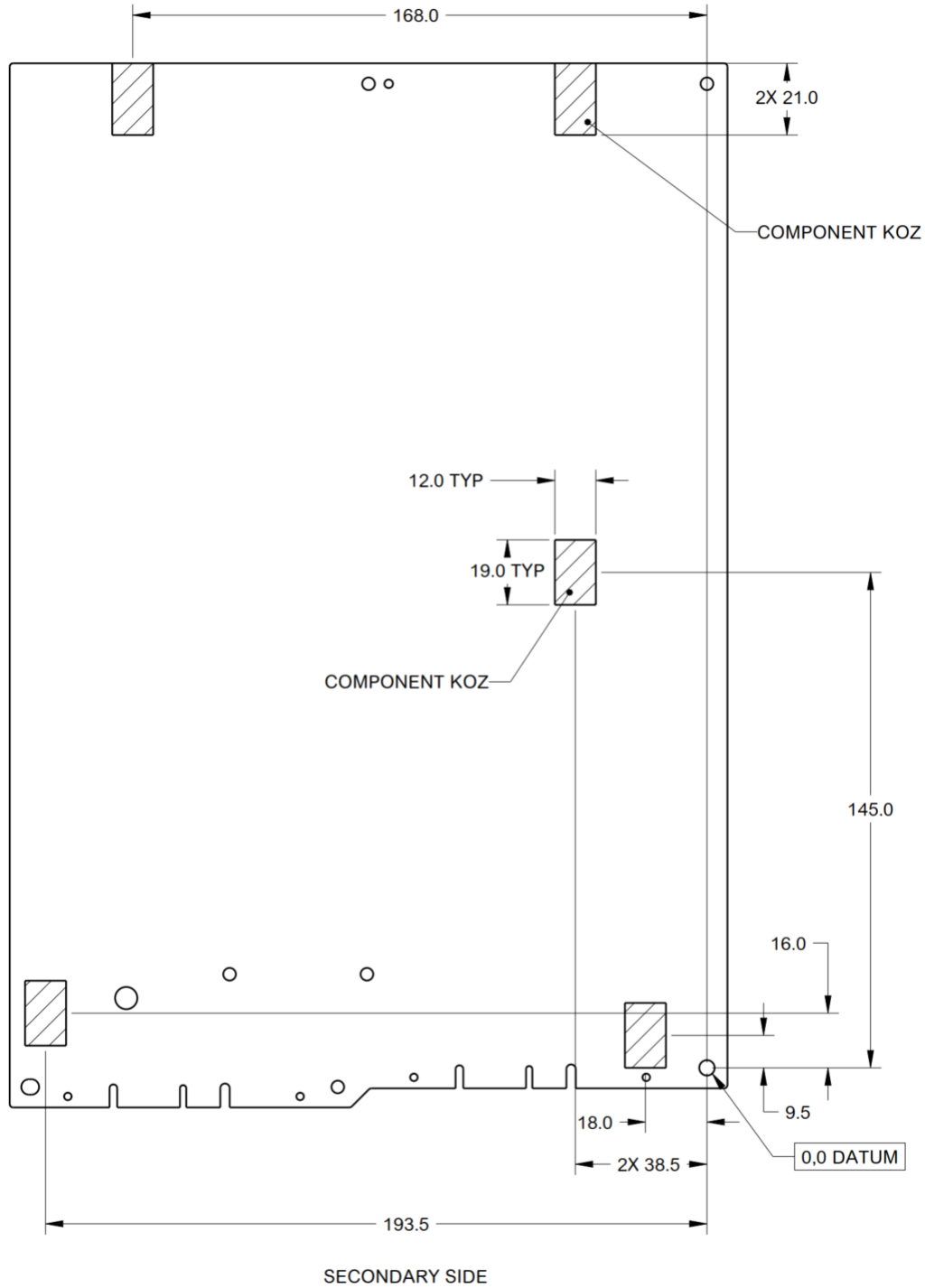
For HPMs $> 372.5\text{mm}$ in length from the datum, Class A and B have two additional KOZs labeled A1 and A2. Class C and D HPMs have four additional KOZs labeled A1 through A4. If the far side edge of the HPM intersects this KOZ area, then a partial KOZ shall be implemented. The resulting KOZ should be colinear with the PCB edge.

For additional information, refer to **Section 8.9 Chassis Design Approach for HPM Interoperability - Example**.

10.3.2.1 Class A HPM Zone 2 Secondary Side Chassis KOZ

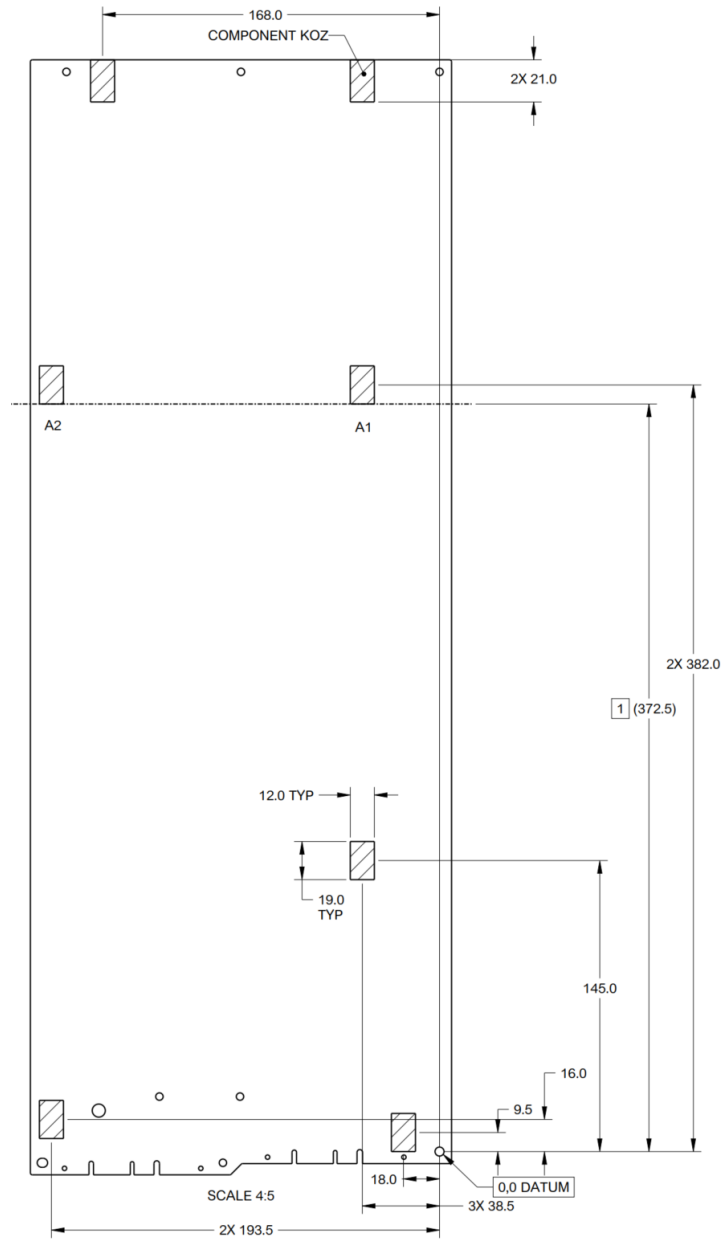
980

Figure 29: Class A Chassis Hook Locations (SECONDARY SIDE)



NOTES:
ALL KOZ'S ARE ZERO HEIGHT RESTRICTION
REFER TO UNIVERSAL SECONDARY SIDE COMPONENT HEIGHT
RESTRICTION FOR MORE INFORMATION

Figure 30: Extended Length Class A Chassis Hook Locations (SECONDARY SIDE)



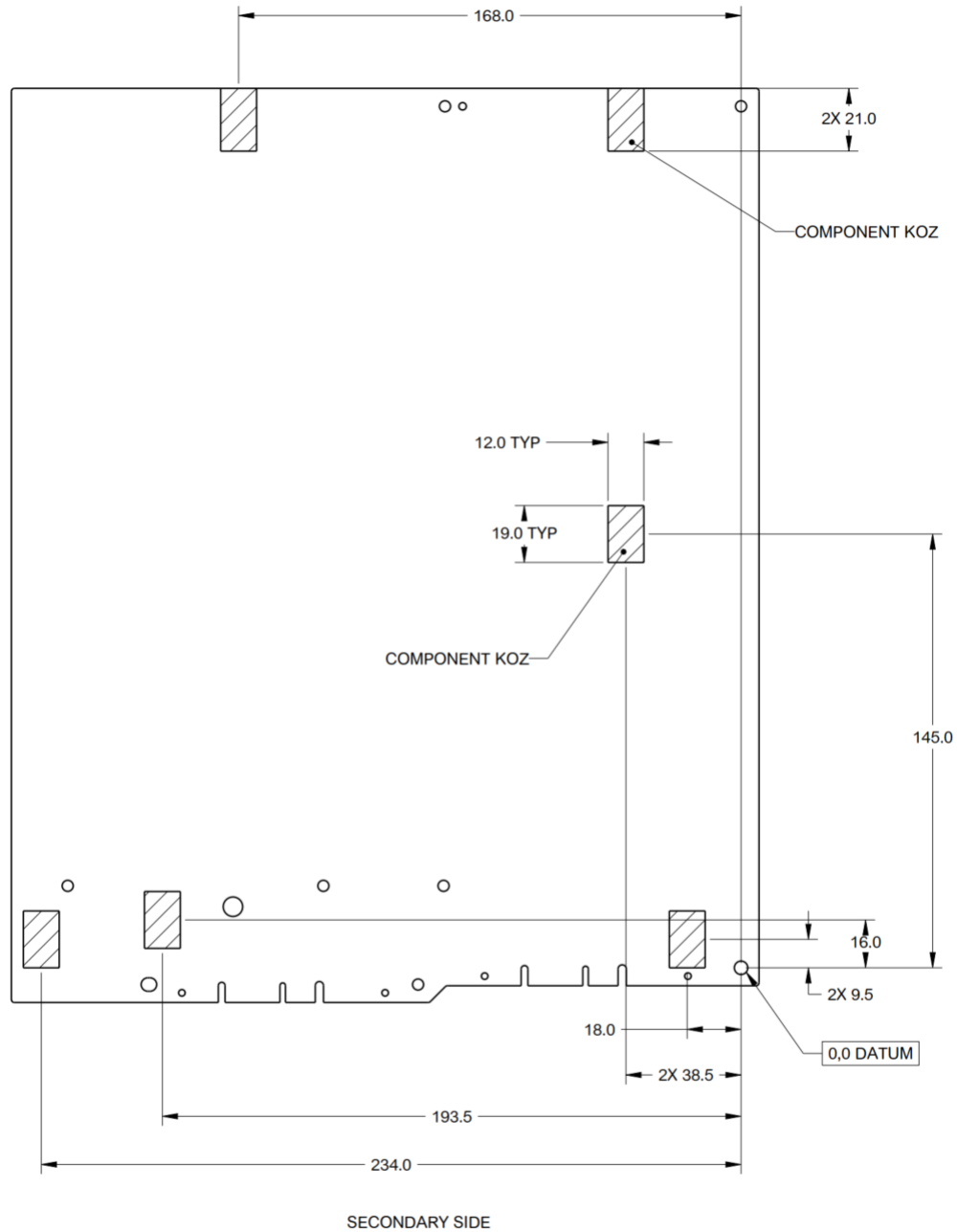
CLASS A555-SECONDARY SIDE

NOTES:

- 1 ALL CLASS A HPMS LONGER THAN THIS VALUE SHALL INCLUDE THE FIXED ZONE 2 KOZS LABELED A1 AND A2. THIS MAY INCLUDE A FULL OR PARTIAL KOZ DEPENDING ON HPM LENGTH.

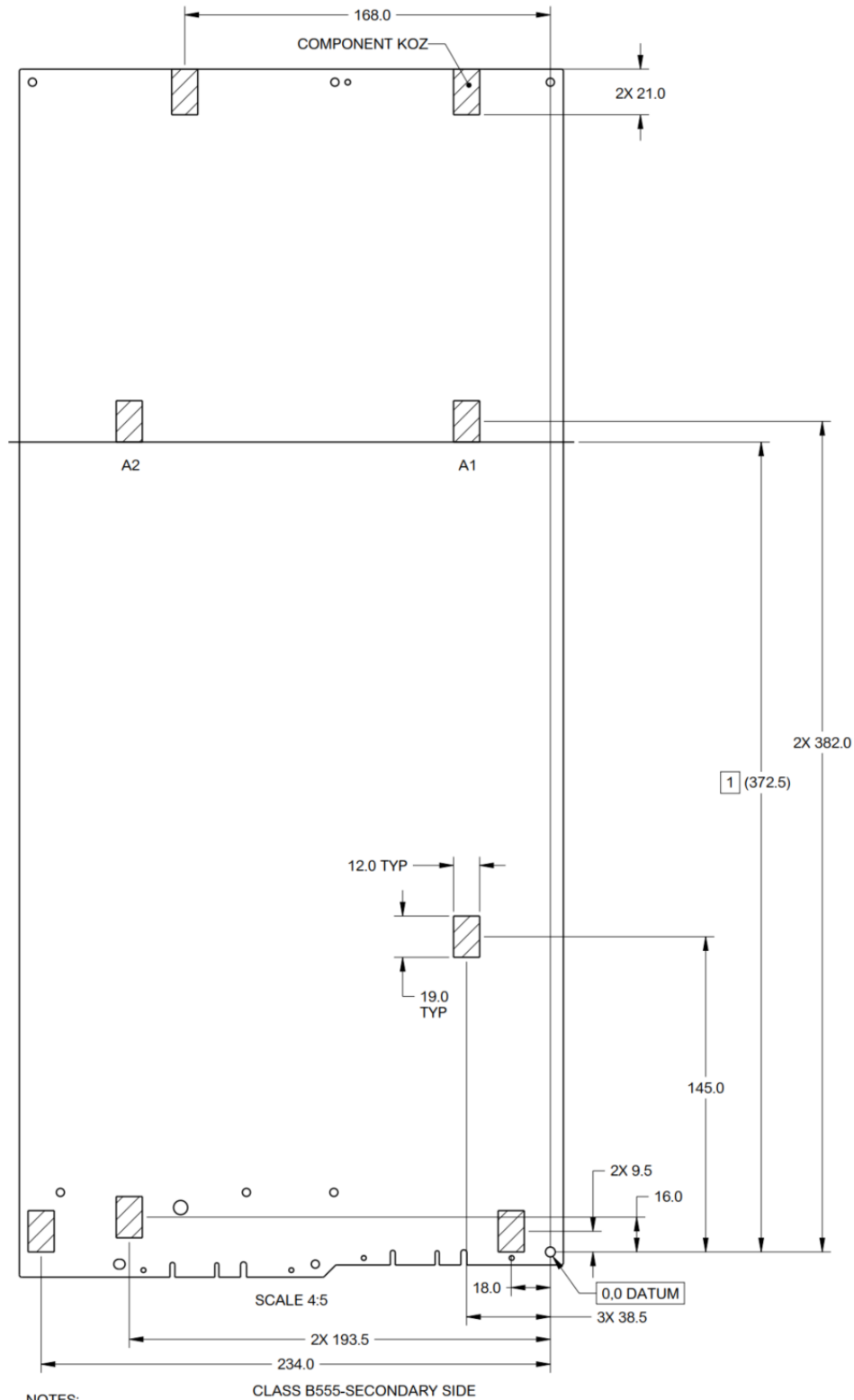
10.3.2.2 Class B HPM Zone 2 Secondary Side Chassis KOZ

Figure 31: Class B Side Chassis Hook Locations (SECONDARY SIDE)



NOTES:
ALL KOZ'S ARE ZERO HEIGHT RESTRICTION
REFER TO UNIVERSAL SECONDARY SIDE COMPONENT HEIGHT
RESTRICTION FOR MORE INFORMATION

Figure 32: Extended Length Class B Chassis Hook Locations (SECONDARY SIDE)



NOTES:

- 1 ALL CLASS B HPMS LONGER THAN THIS VALUE SHALL INCLUDE THE FIXED ZONE 2 KOZS LABELLED A1 AND A2. THIS MAY INCLUDE A FULL OR PARTIAL KOZ DEPENDING ON HPM LENGTH.

10.3.2.3 Class C Zone 2 Secondary Side Chassis KOZ

995

Figure 33: Class C Chassis Hook Locations (SECONDARY SIDE)

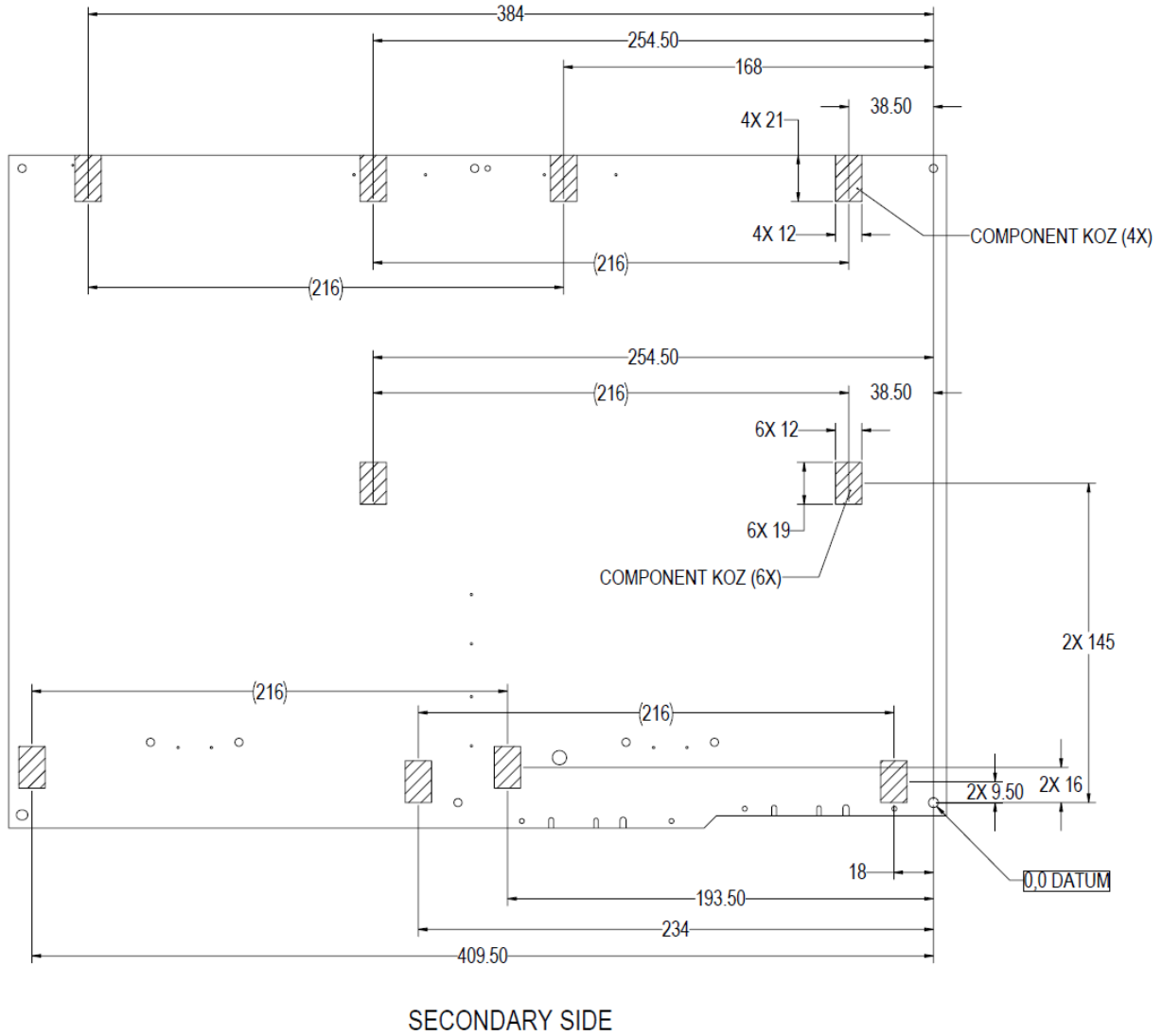
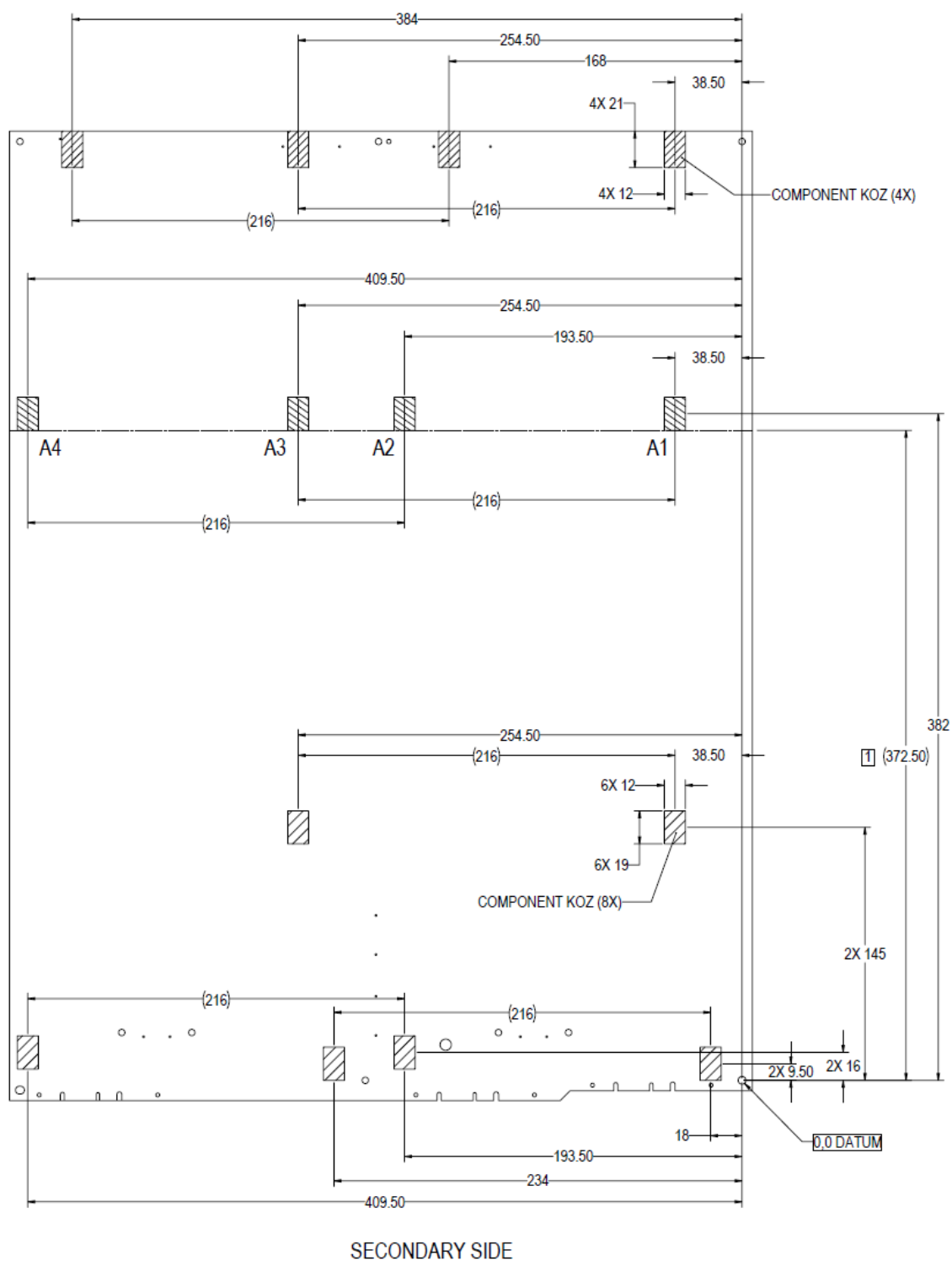


Figure 34: Extended Length Class C Chassis Hook Locations (SECONDARY SIDE)



Notes:

1 ALL CLASS C HPMs LONGER THAN THIS VALUE SHALL INCLUDE THE FIXED ZONE 2 KOZs LABELED A1, A2, A3, AND A4. THIS MAY INCLUDE A FULL OR PARTIAL KOZ DEPENDING ON HPM LENGTH.

1000 10.3.2.4 Class D Zone 2 Secondary Side Chassis KOZ

Figure 35: Class D Chassis Hook Locations (SECONDARY SIDE)

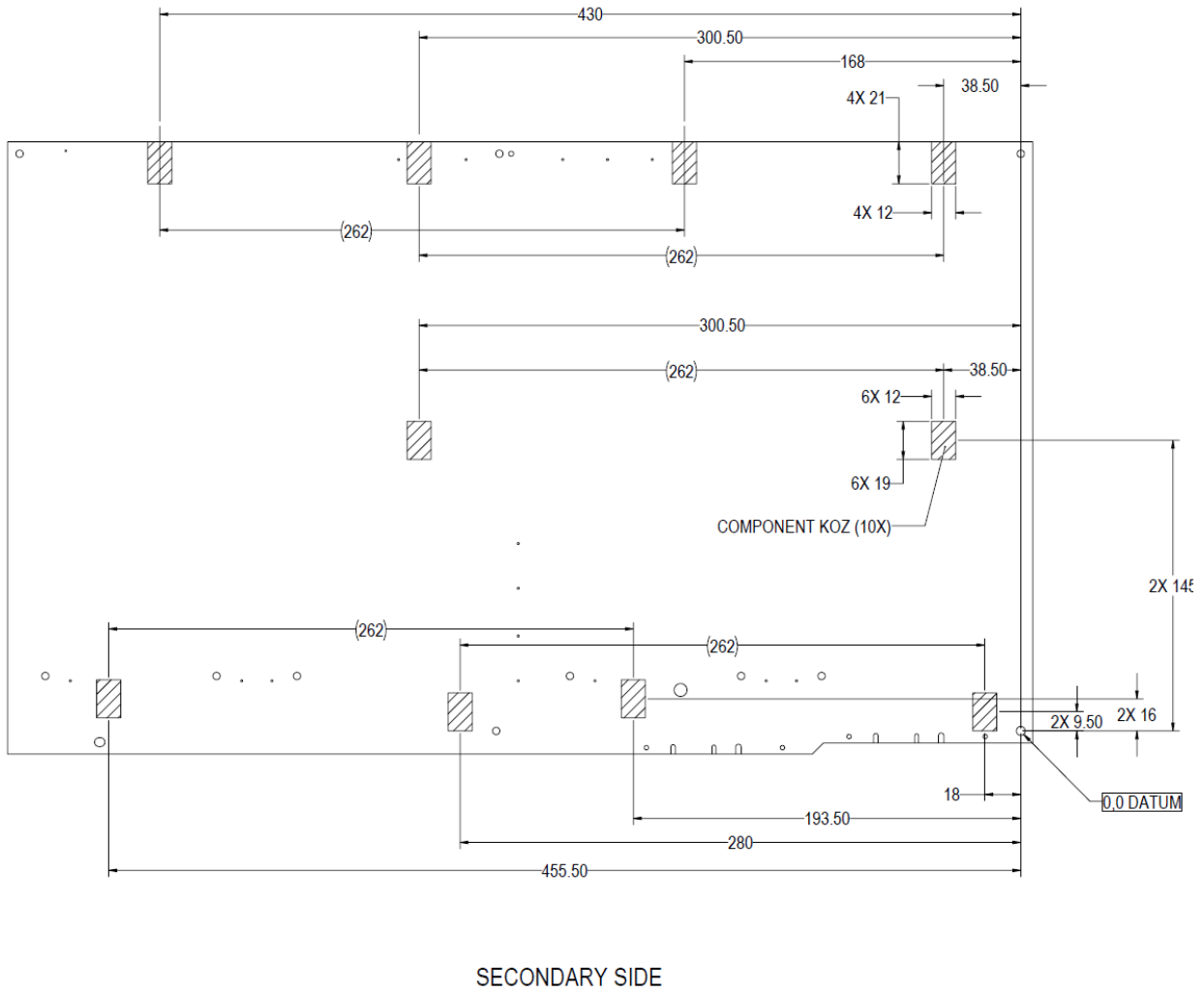
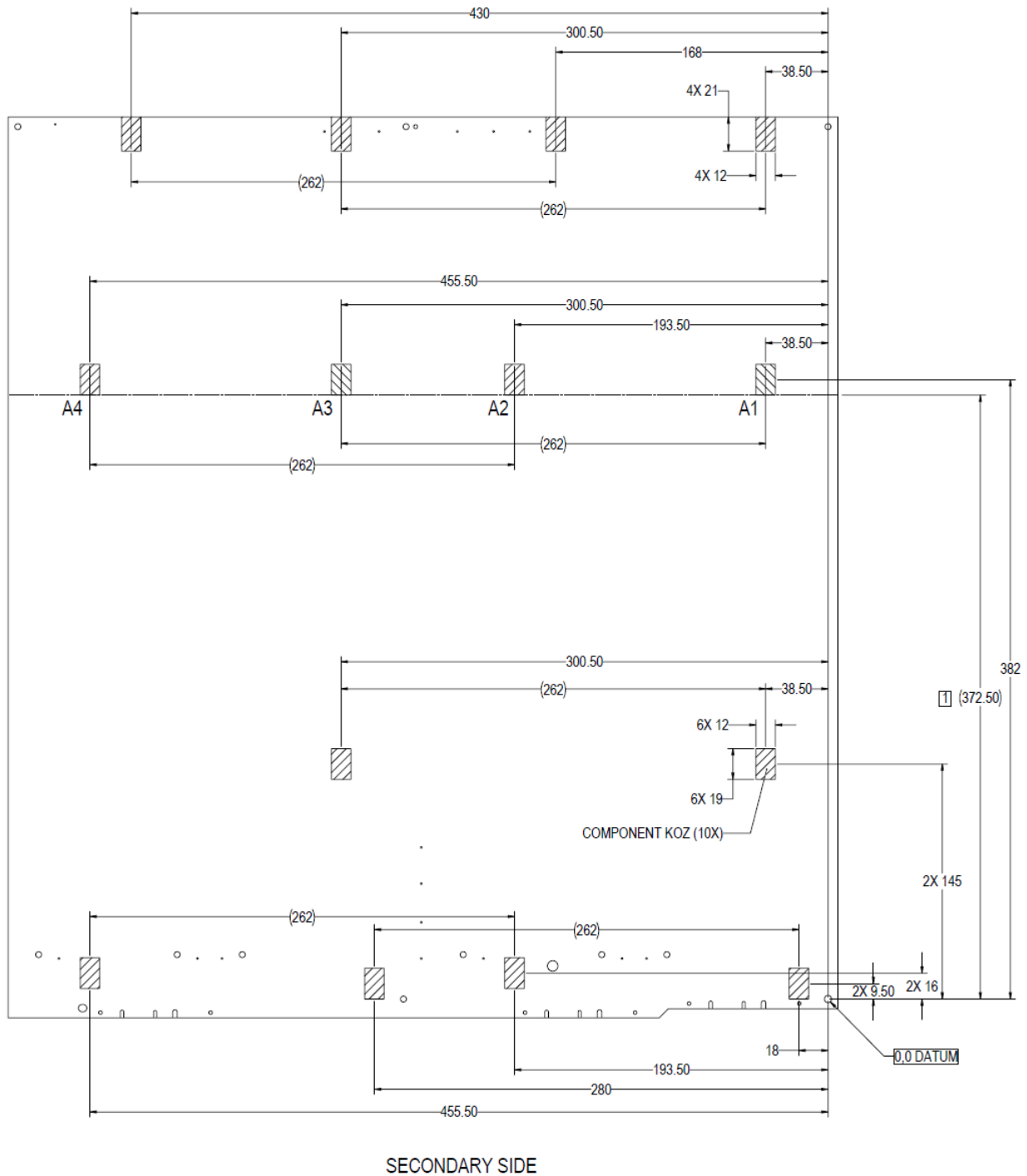


Figure 36: Extended Length Class D Chassis Hook Locations (SECONDARY SIDE)



NOTES:

- 1 ALL CLASS D HPMs LONGER THAN THIS VALUE SHALL INCLUDE THE FIXED ZONE 2 KOZs LABELED A1, A2, A3, AND A4. THIS MAY INCLUDE A FULL OR PARTIAL KOZ DEPENDING ON HPM LENGTH.

1005

10.3.3 Zone 3: HPM Secondary Support Requirements

HPMs may require secondary side support under the DIMMS and other semi-supported areas where HPM deflection is likely to occur during normal assembly processes. Two common design approaches to provide this support are:

1. HPMs can identify and provide areas for chassis designs to directly support the HPM PCB surface. These areas need to be clearly identified and free from any conductors or risk of shorting (no exposed vias, traces or components). Chassis designers may choose to support these areas with Board Pan formed features (metal) or bumpers/fillers (rubber or plastic).
2. HPMs can include bumpers or fillers in their design that are tuned in Z height (2.12mm +/- 0.10mm) to match with the Board Pan and exceed the height of all bottom side components.

Figure 37: Example Secondary Side Supports



10.3.4 Zone 4: CPU Backing Plate Requirements

1025 Most server HPM designs need to support CPU backing plates or stiffeners placed under the CPU as part of the CPU Socket design.

The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by:

- Backing Plate allowed Height = 6.2mm – HPM thickness - 0.08mm standoff height tolerance – allowances for other backplate design req's (insulators, deflections, etc.)
- 1030 • See Implementors Note below for examples.

Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and / or HPM sled as shown in **Figure 41: CPU Backing Plate (Zone 4)**.

Implementors Note:

HPM and CPU designers should consider these example scenarios supported by DC-MHS HPM board and Backing plate thickness requirements.

Board Thickness (Nominal, mm)	Maximum Allowable CPU Backing Plate Including Allowances (mm)
1.57	4.55
1.93	4.19
2.36	3.76
2.55	3.57
3.18	2.94

10.4 HPM Board and Assembly Thickness

- The maximum allowed thickness and zone heights in the specification assume a minimum 6.2mm board mounting height within a system chassis.
 - Thickness and zone heights are established to ensure forward compatibility with 1U & 2U System Chassis assumptions.
- Exceeding the thickness and zone height target values would result in system design impacts and incompatibilities.
- The board mounting height for a given system is not within scope of the HPM specification and is at discretion of the System designer.
- The maximum allowed HPM thickness shall be 3.18mm nominal and assumes +/-10% tolerance is allowed.
 - Note that PCB Tolerances of +/- 10% are supported but are not a factor in determining the fit of the CPU Backing Plate when the HPMs are mounted to standoffs by their bottom surfaces.

Implementors Note:

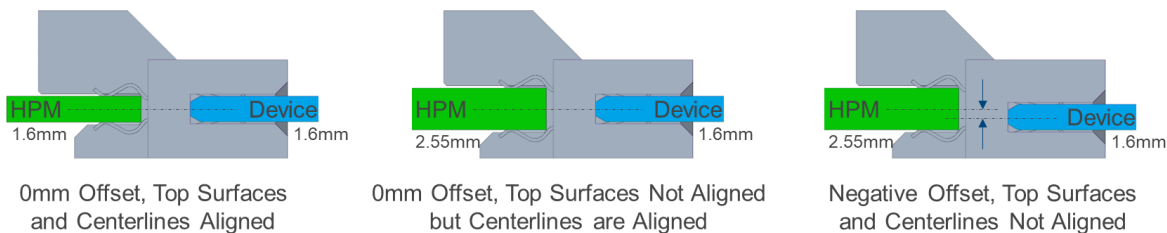
Offset connector choices and requirements may vary if a common chassis design needs to support varying HPM thicknesses. For the M-SDNO specification, this could include connectors for OCP NIC R3 and DC SCM R2.x.

Failure to choose the proper offset could result in peripheral cards not aligning to the chassis opening, demonstrated by card alignment in the figure below.

There is no recommendation for connector offset for MHS compliance. Connector offset is out of scope of DC-MHS HPM specifications.

Connector offset is a BOM (bill of material) choice by the system / HPM designers.

Refer to the latest OCP NIC R3.0 and DC-SCM R2.x specifications for a list of connector choices available at the time those specifications were published. Refer to connector vendors for the latest connector offset options.

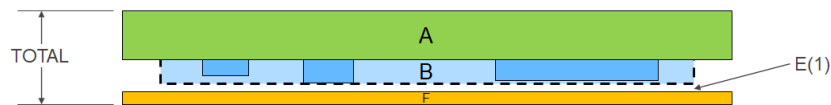
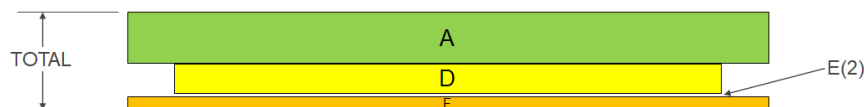
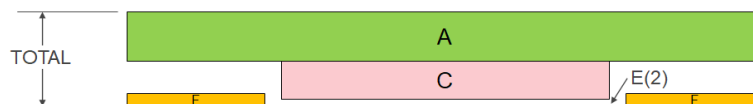


Implementors Note:

HPM and Chassis designers should consider the height stack-up of each of the 4 zones identified in **Section 10.3: Secondary Side Zones and Height Restrictions**. **Table 3** and **Figure 38 - Figure 41** demonstrate an example of a compliant stack-up for consideration. Note that the “total Z” value across the 4 zones must always be equivalent (maximum allowed value of 6.2mm shown for example only).

Table 3: Example Z-Height Compliant Stack-Up, Per Zone

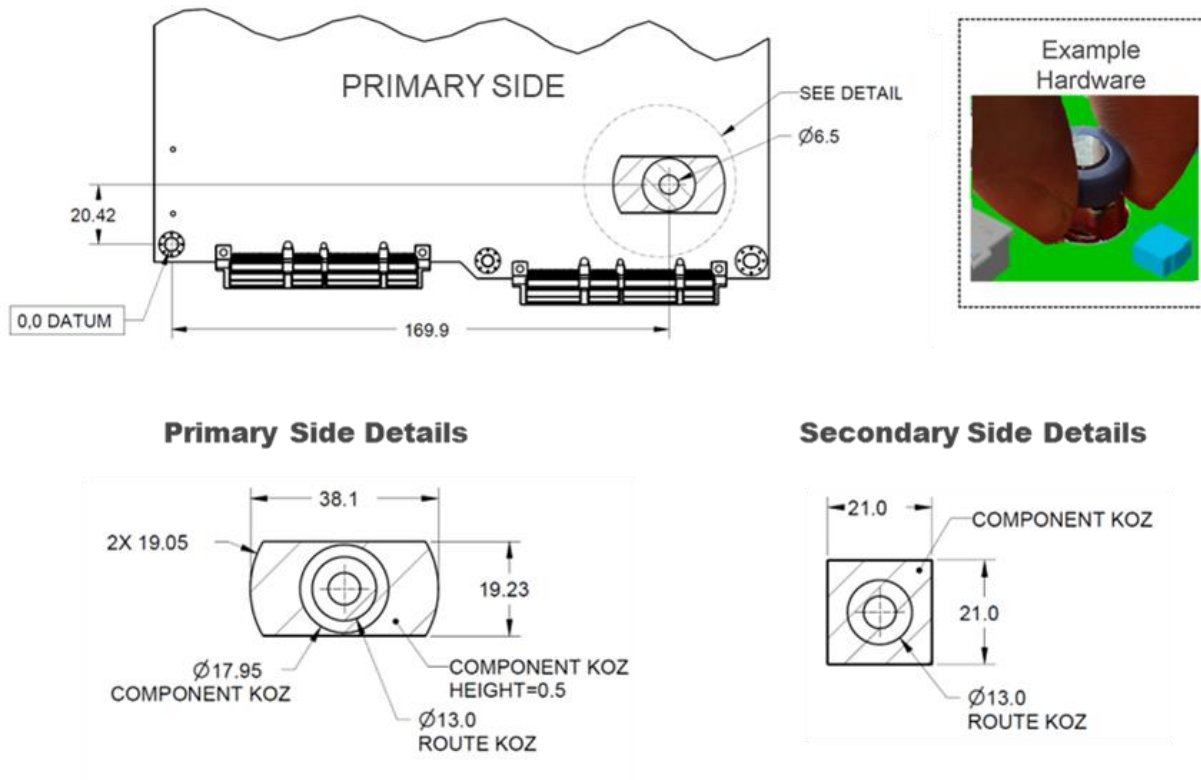
		Zone 1	Zone 2	Zone 3	Zone 4	
Item	Description	Z Value (mm)	Z Value (mm)	Z Value (mm)	Z Value (mm)	Notes
A	HPM	3.18	3.18	3.18	3.18	MAX Thickness (w/o Added tolerance, Assumes bottom mounting)
B	Bottom Component Z	1.60	0			MAX Height
C	CPU Backing Plate				2.94	MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray
D	HPM Bottom Support			2.12		HPM Support Thickness +/- 0.10mm, must exceed Bottom Component Z
E(1)	Resultant Gap	0.62	0.58			Gap is Larger, Requires Insulation and/or Clearance
E(2)	Resultant Gap			0.10	0.08	Gap is Small, Contact between Parts is either Desired or Permissible
F	Board Pan	0.80		0.80		
G	Chassis Hook		2.44			MAX Height from Inside Surface of Chassis
	TOTAL	6.2	6.2	6.2	6.2	Example Solution Stack-up

Figure 38: Secondary Side Components (Zone 1)**Figure 39: Chassis Hook Keepouts (Zone 2)****Figure 40: HPM Secondary Support (Zone 3)****Figure 41: CPU Backing Plate (Zone 4)**

10.5 HPM to Chassis Retention Mounting

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required for HPM retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc., hole size required Primary / Secondary side KOZs (and height restrictions around this hole), are defined in **Figure 42**. This definition applies to all HPM classes.

Figure 42: HPM Assembly to Chassis Retention Enablement (Class A Depicted)



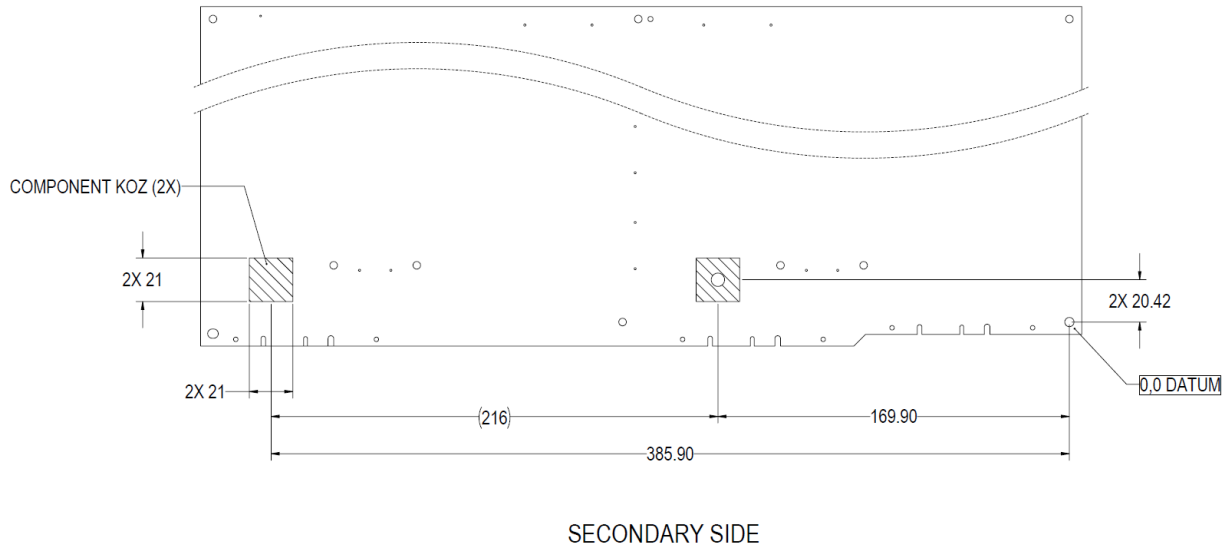
Implementors Note:

The wide shaped primary side 0.5mm Height Restriction in **Figure 42** is in place for finger grip allowances around the retention hardware (which could be a plunger, thumbscrew, wing screw, etc.). Due to hardware and touchpoints being in this area, the goal is to minimize the size of components that could potentially be damaged by fingers coming in close contact to the board surface.

1065

The Class C HPM is defined in a manner to be compatible with two Class A HPMs in a shared chassis with these half-wide HPMs set on a 216mm pitch. Due to this relationship, Class C shall include two bottom side KOZs located in the position compatible with the associated chassis retention features. These Class C bottom KOZs are defined in **Figure 43.**

Figure 43: Class C Assembly to Chassis Details (SECONDARY SIDE)

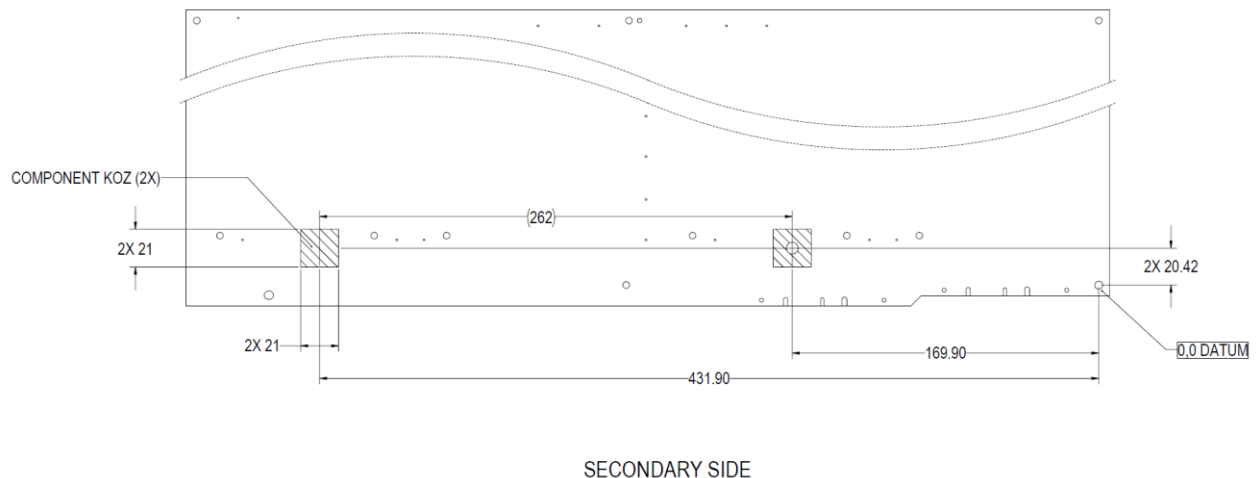


1070

The Class D HPM is defined in a manner to be compatible with two Class A or two Class B HPMs in a shared chassis with these half-wide HPMs set on a 262mm pitch. Due to this relationship, Class D shall include two bottom side KOZs located in the position compatible with the associated chassis retention features. These Class D bottom KOZs are defined in **Figure 44.**

1075

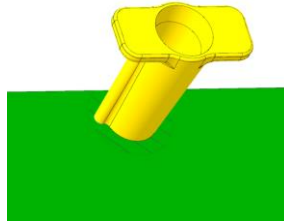
Figure 44: Class D Assembly to Chassis Details (SECONDARY SIDE)



10.6 HPM Handle Hole

1080 The HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with, but is not limited to, a plastic handle. An example is shown in **Figure 45**.

Figure 45: Example Board Handling Feature



Implementors Note:

While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

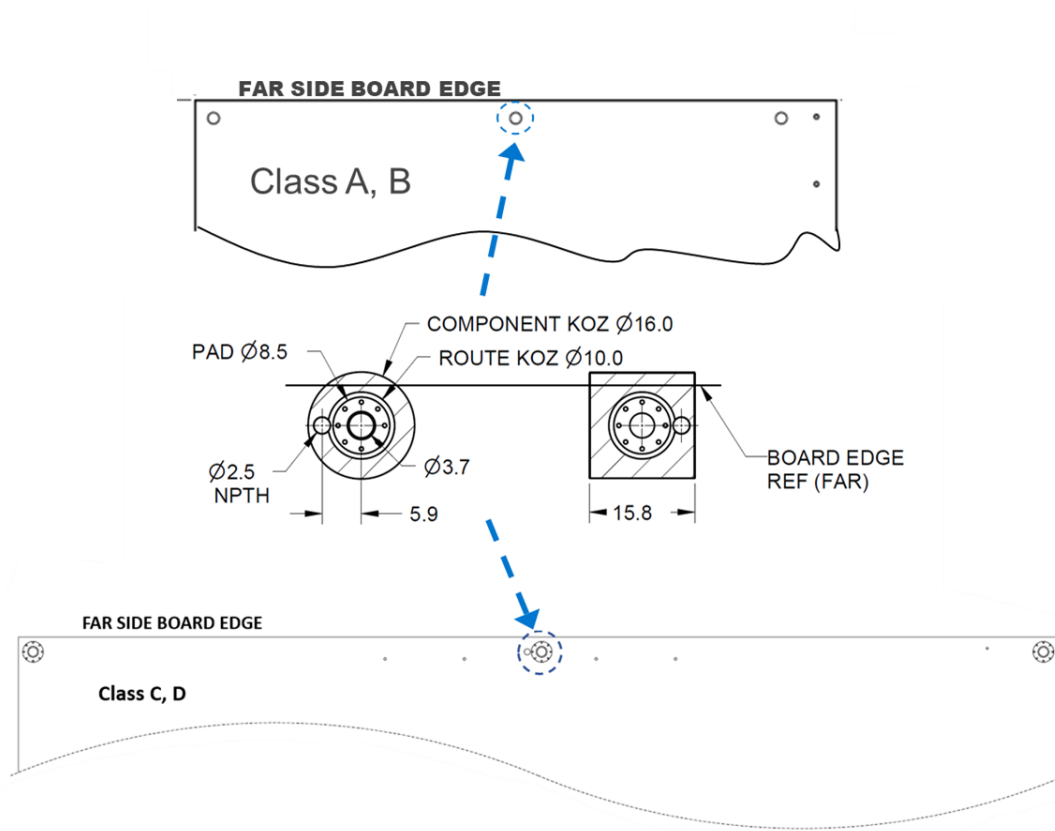
The hole location shall be near the Far side edge of the HPM. HPM Designers may choose to either:

- 1085 1. Replace a recommended mid-board mounting hole along the Far Side edge with the board handle hole. **Figure 46** demonstrates this approach.
2. Add an additional hole near the Far Side Edge with consideration for Compute Core Details such as cabling for HSIO.
- 1090

The Board Handle hole may also be considered a mounting hole for structural purposes. For example, a designer does NOT need to place a board mounting hole in close proximity to the Board Handle Hole.

1095 The board handle hole shall follow the required dimensions and KOZ in **Figure 46**.

Figure 46: Geometry and KOZ for HPM Handle Hole and Optional Placement Location



1100 10.7 OCP NIC R3 and DC-SCM R2.x at Near Side Edge Locations

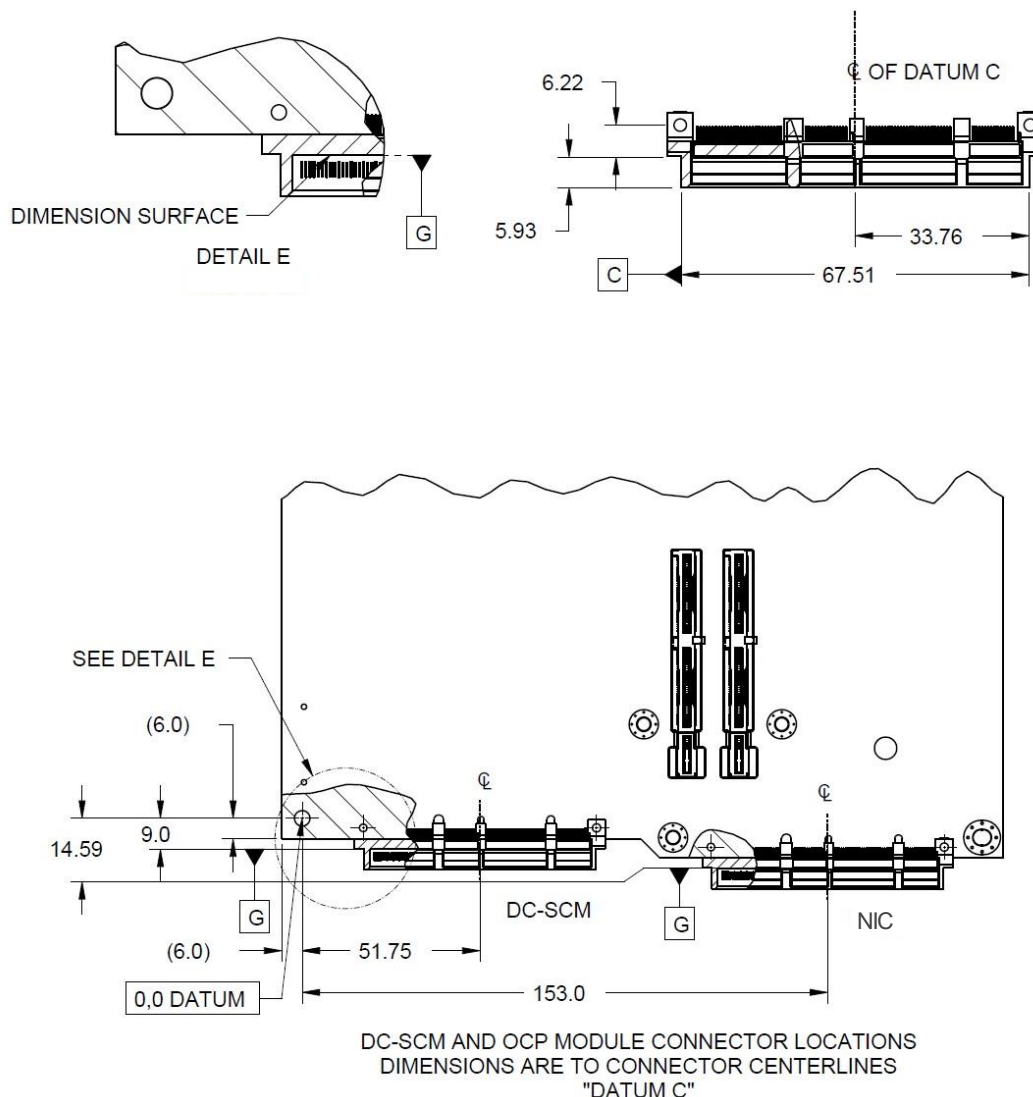
This specification defines fixed placement for certain peripheral connectors to maximize reuse across designs. These fixed peripheral subsystem connectors are OCP NIC R3.0 and HFF DC-SCM R2.x. Each of these peripherals leverage connectors defined by SFF-TA-1002, including centerline definitions referenced in the figures of this specification (Refer to the **DC-MHS Connector List** for vendor part number details).

1105 10.7.1 OCP NIC and DC-SCM

The DC-SCM R2.X connector shall be implemented as defined in **Figure 47**. The HPM shall implement a battery backed voltage interface per DC-SCM R2.x "Battery Voltage" requirement.

The OCP NIC R3.0 connector is strongly recommended, if implemented, it shall be placed as defined in **Figure 47**.

Figure 47: OCP NIC 3.x and DC-SCM R2.x (PRIMARY SIDE)



10.8 Platform Infrastructure Connector Placement (non-power)

10.8.1 Connector Requirements

1115 The electrical implementation for each connector shall follow the M-PIC specification.

Internal USB

- **M-PIC Section Reference:** “Internal USB3 Connector”
- **Connector Requirement:** Shall be Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- 1120 • **Connector:** Type A or C USB Compliant. It is strongly recommended that HPMS implement a Type A connector.

Intrusion Switch

- **M-PIC Section Reference:** “Intrusion Switch”
- **Connector Requirement:** Shall be Required (may be de-populated)
- 1125 • **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

Boot Storage

- **M-PIC Section Reference:** “Boot Storage”
- **Connector Requirement:** Recommended
- 1130 • **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

Due to HPM layout density it is expected that the Cable Optimized connector will be more prevalent in Class A designs. Class B, C and D HPMS may choose to utilize the platform custom zone to enable the Direct Attach Boot Storage option.

1135 Control Panels

- **M-PIC Section Reference:** “Control Panel Interfacing”
- **Connector Requirement:** Primary Shall Be Required (may de-pop), Secondary Optional
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

1140 PDB Management Connector

- **M-PIC Section Reference:** “PDB Management Connector”
- **Connector Requirement:** Shall Be Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

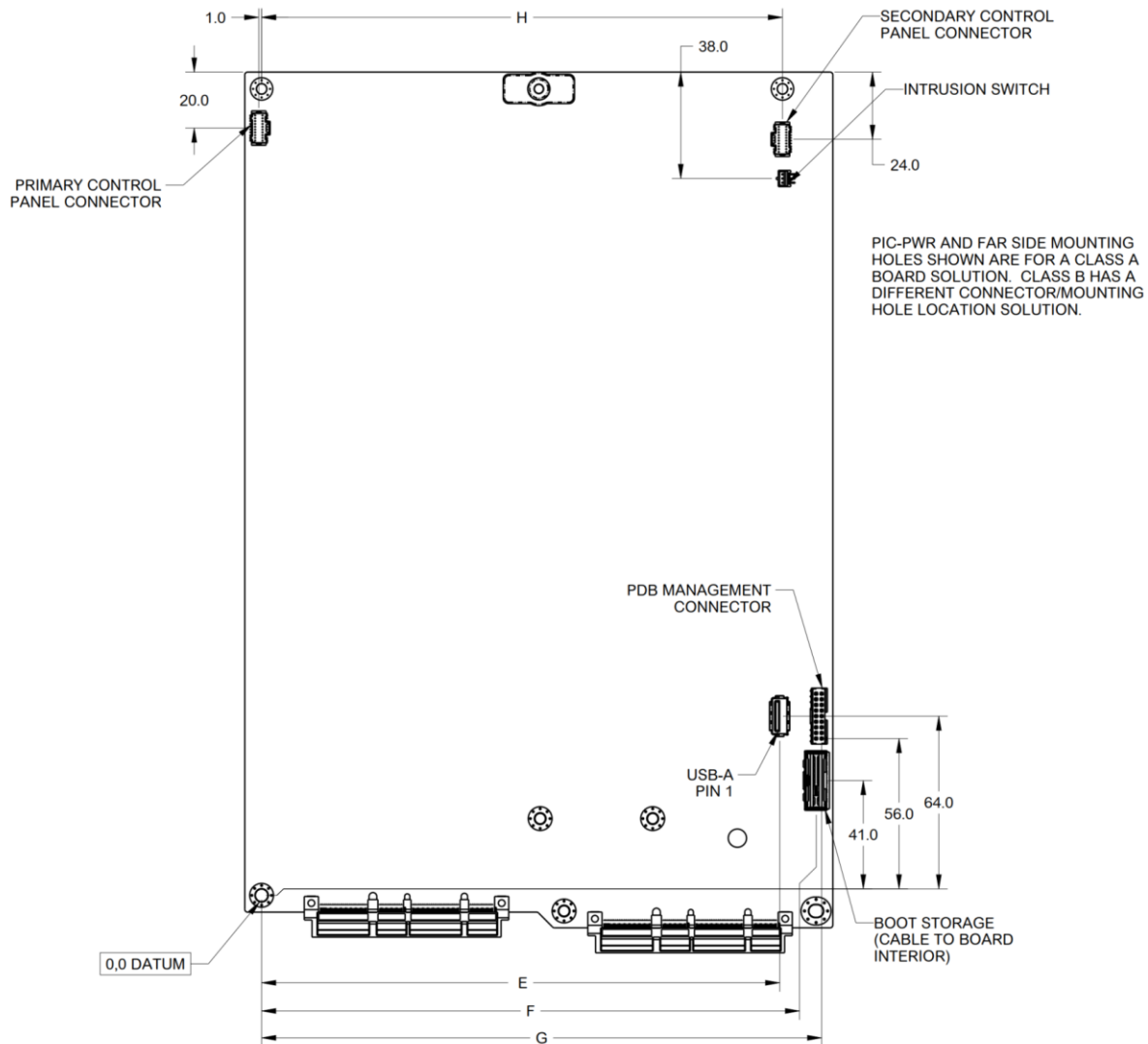
1145

10.8.2 Class A and Class B M-PIC Connector Locations (non-power)

Figure 48 depicts the recommended location of the miscellaneous connectors defined in the M-PIC specification which are relevant to M-SDNO HPMs Class A and B. Additional information on these connectors is available in **Section 10.8.1**.

1150 These dimensions are intended to provide recommended connector locations that are consistent relative to the closest board corner across all Class A and B HPMs.

Figure 48: Class A-B Platform Infrastructure Connector Recommended Placements



Class	E (MID)	F (MID)	G (Pin 1)	H (MID)
A	185	198	200	186
B	225	238	240	226

1155

To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 49** through **Figure 52** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone. Note that the intrusion switch can share either the primary or secondary control panel zone.

1160

Figure 49: Class A Intrusion, Control Panel, USB and PDB Management Placement Zones

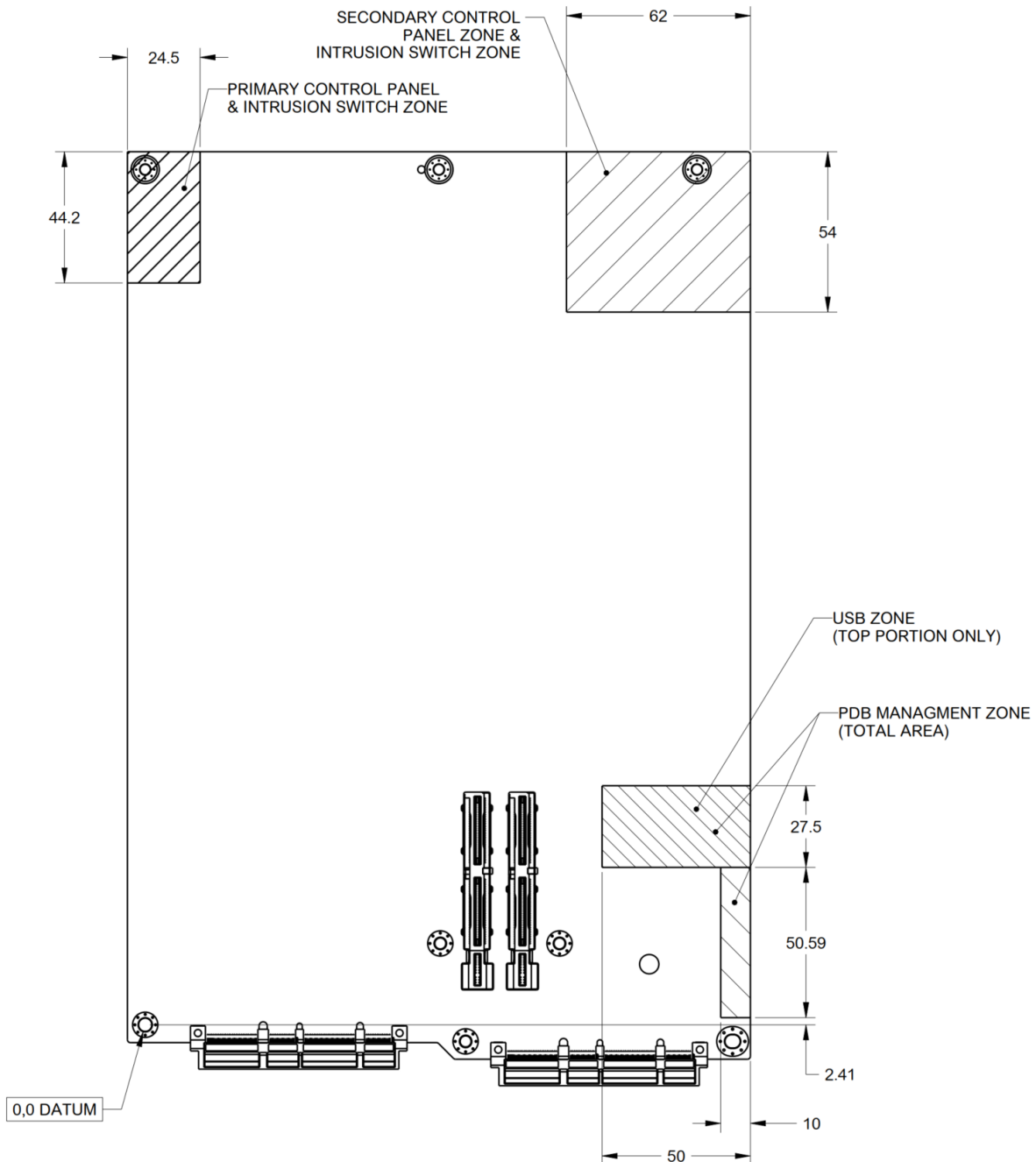
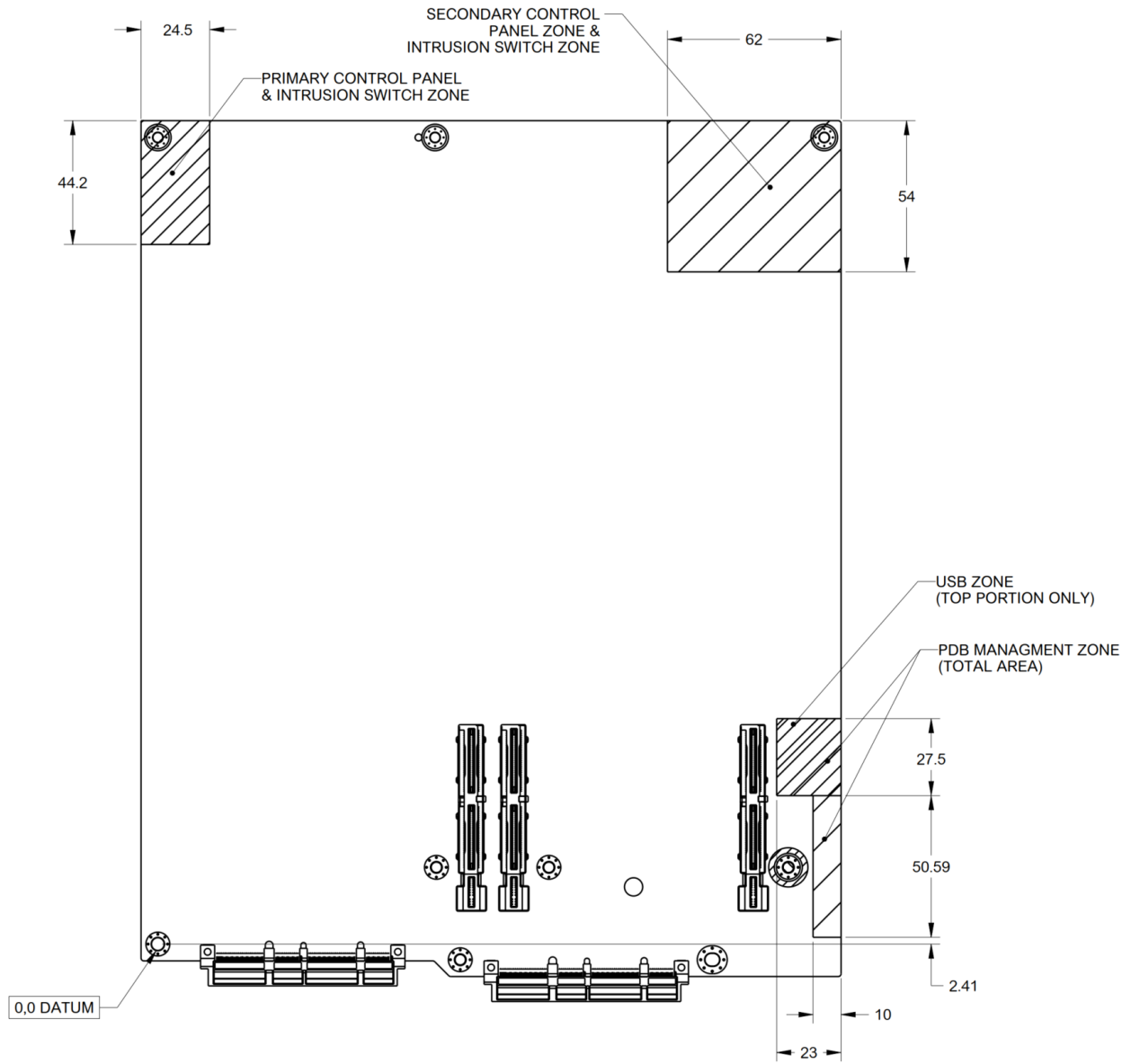


Figure 50: Class B Intrusion, Control Panel, USB and PDB Management Placement Zones



1165

Figure 51: Class A Cabled Boot Connector Placement Zone

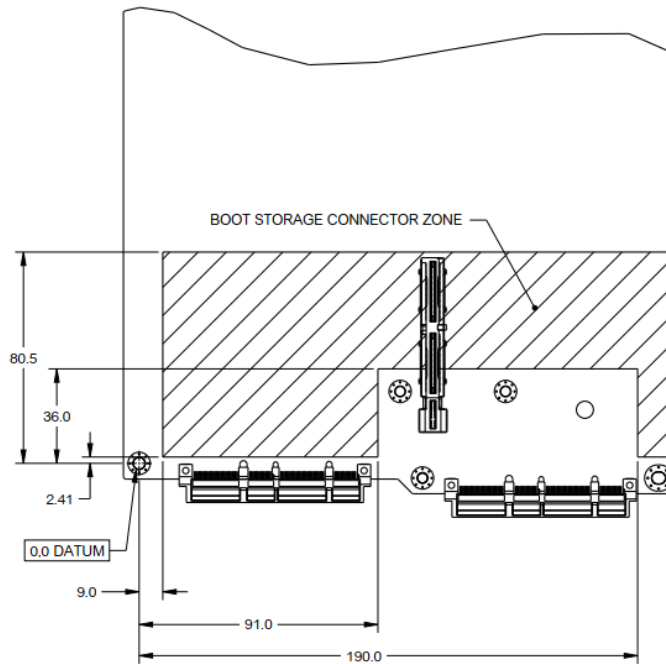
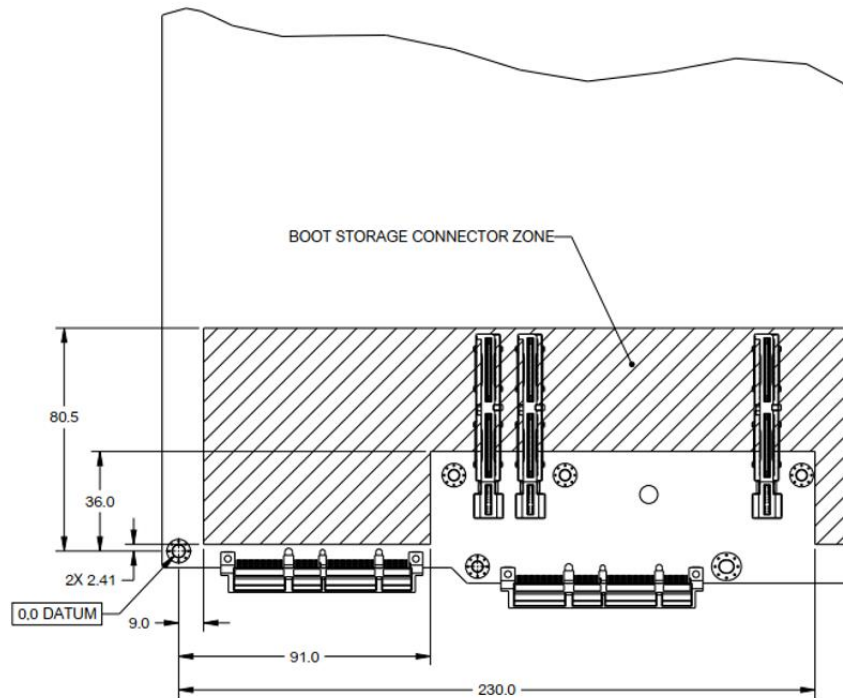


Figure 52: Class B Cabled Boot Connector Placement Zone



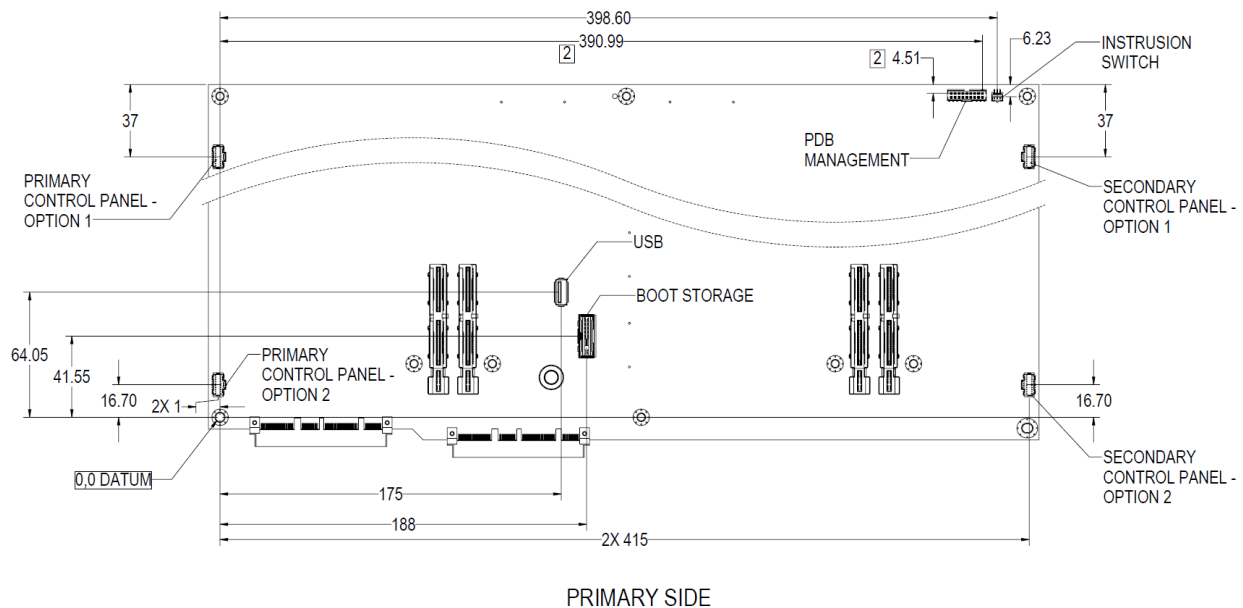
10.8.3 Class C M-PIC Connector Locations (non-power)

Figure 53 depicts the recommended location of the miscellaneous M-PIC connectors defined in the M-PIC specification for Class C HPMs. Additional information on these connectors is available in **Section 10.8.1**.

1175 To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 54** and **Figure 55** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone.

1180 Note that Class C HPMs contain the option for Near Side or Far Side control panel placement. Class C HPMs may choose to implement either Option 1 or Option 2. Option 1 aligns with the locations for Class A and B HPMs which may be used in a common chassis with Class C HPMs. Option 2 is optimized for systems where the Near Side is facing the Cold Aisle (i.e. "Front I/O").

Figure 53: Class C Platform Infrastructure Connector Recommended Placements



NOTES:
1. ALL DIMENSIONS TO CONNECTOR MIDPLANE UNLESS OTHERWISE NOTED.
[2] DIMENSION TO CONNECTOR PIN 1.

Figure 54: Class C Intrusion, Control Panel, USB and PDB Management Placement Zones

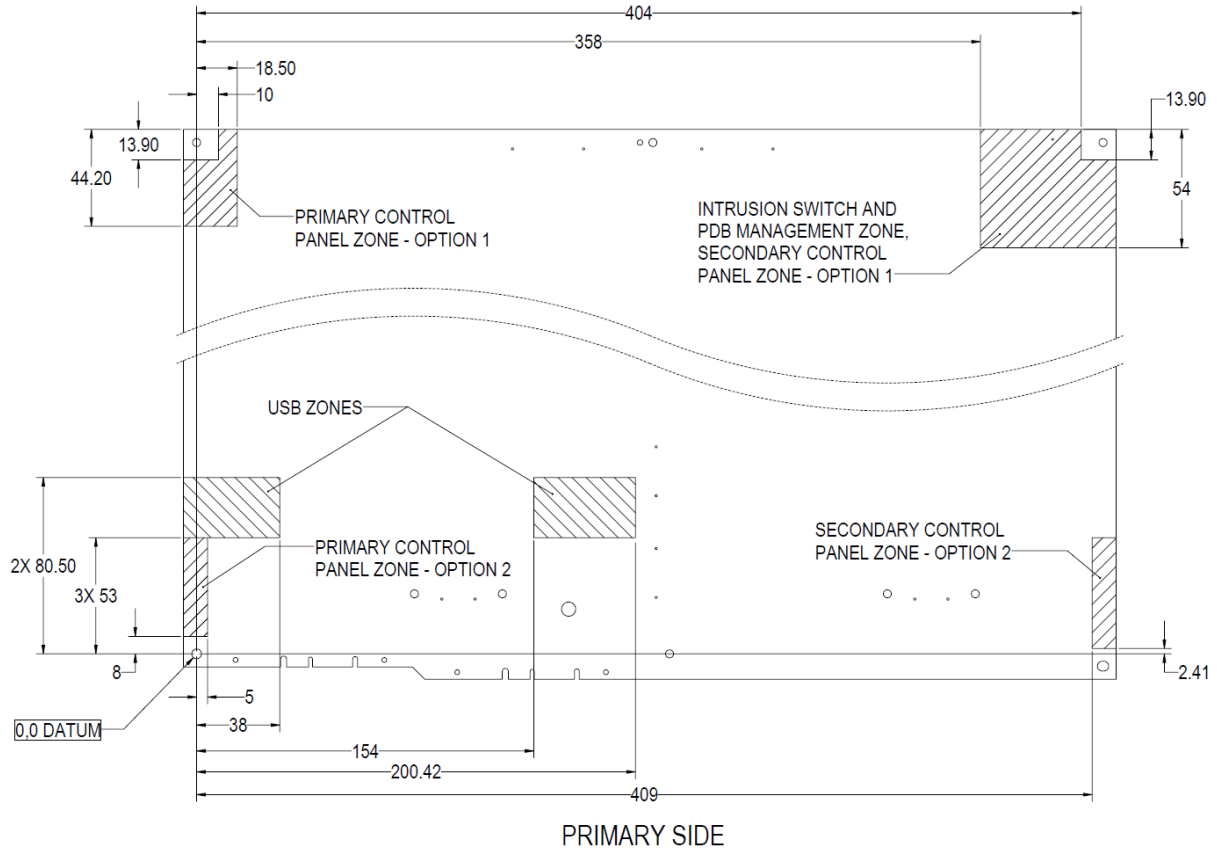
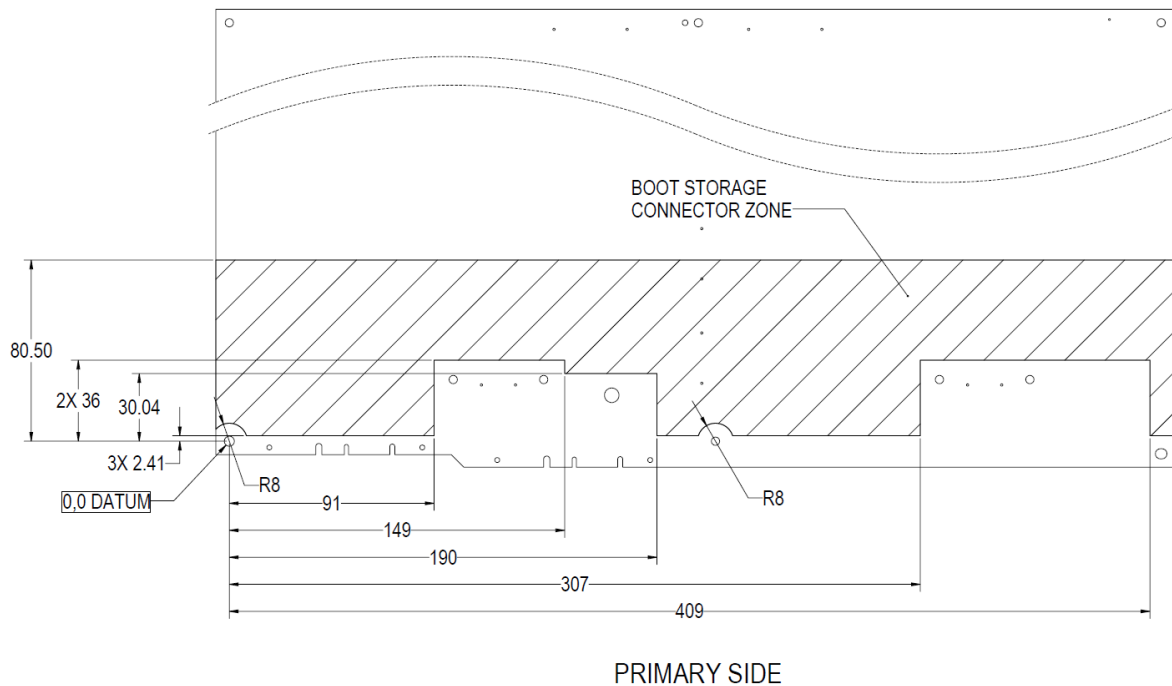


Figure 55: Class C Cabled Boot Connector Placement Zone

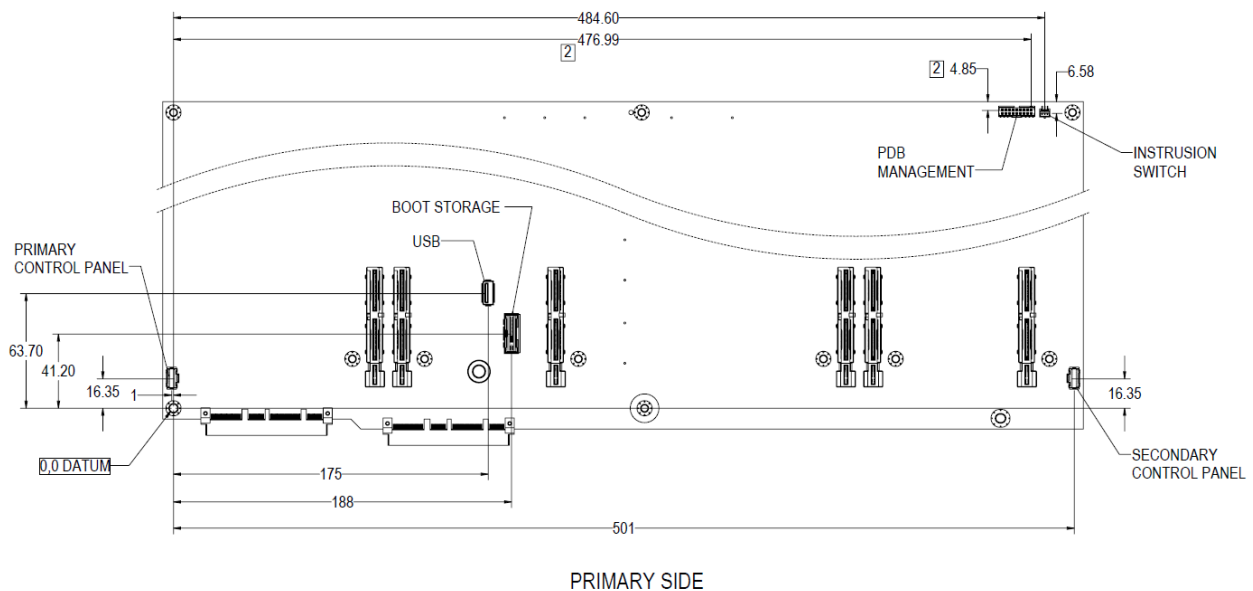


1190 10.8.4 Class D M-PIC Connector Locations (non-power)

Figure 56 depicts the recommended location of the miscellaneous M-PIC connectors defined in the M-PIC specification for Class D HPMs. Additional information on these connectors is available in **Section 10.8.1**.

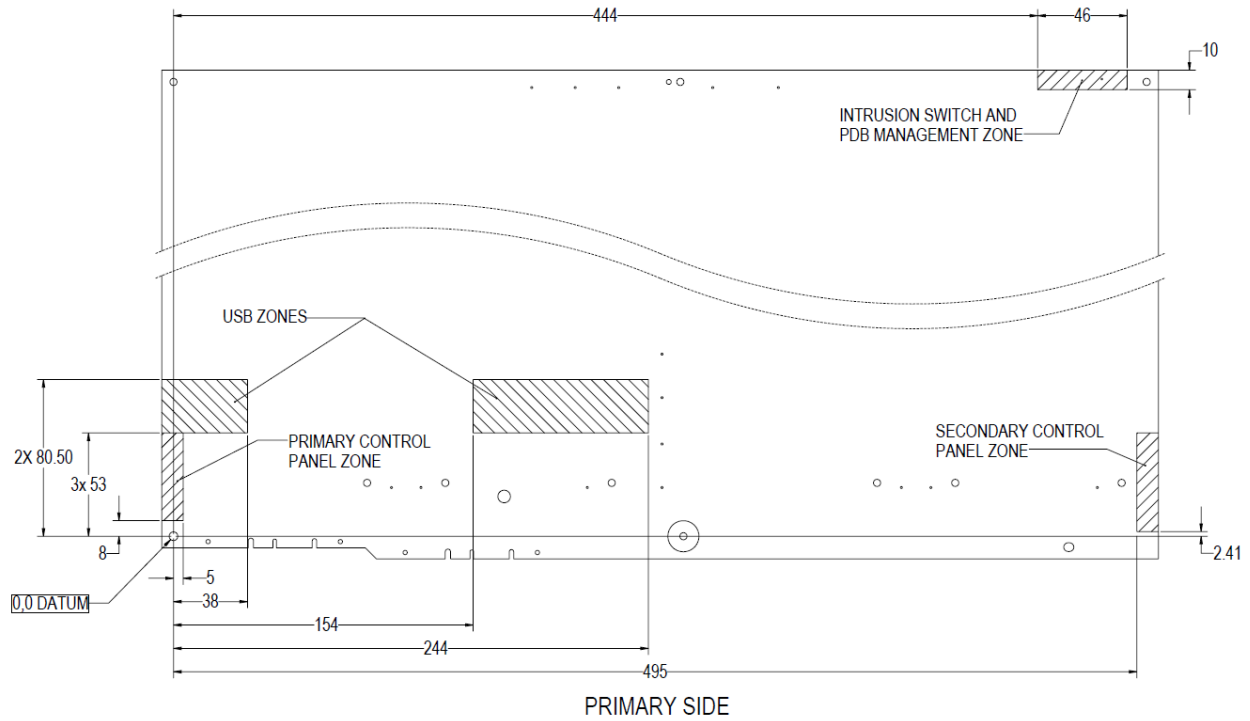
To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 57** and **Figure 58** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone.

Figure 56: Class D Platform Infrastructure Connector Recommended Placements



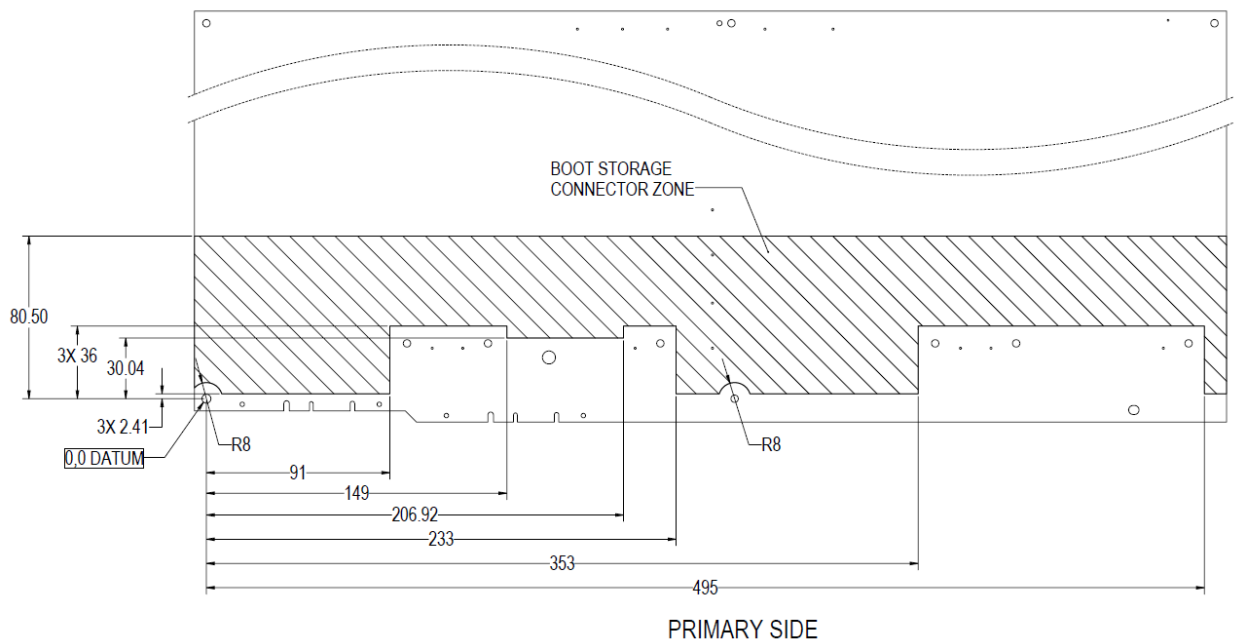
Notes:
 1. ALL DIMENSIONS TO CONNECTOR MIDPLANE UNLESS OTHERWISE NOTED.
 2. DIMENSION TO CONNECTOR PIN 1.

Figure 57: Class D Intrusion, Control Panel, USB and PDB Management Placement Zones



1205

Figure 58: Class D Cabled Boot Connector Placement Zone



1210 10.9 High Speed I/O (HSIO) Connectors

This base specification seeks to allow for flexible high speed I/O (HSIO) routing options while also enabling HPM to system compatibility.

Board-to-Board (B2B) connections are defined as connections that mate two separate PCBs entirely without cabling. B2B connections are typically used to route HSIO from the HPM to a riser PCB or direct dock peripherals (i.e. DC-SCM R2.x, OCP-NIC R3).

Board-to-Cable (B2C) connections are defined as connections that mate two separate PCBs entirely with cabling. B2C connections are typically used to route HSIO from the HPM to a riser PCB or to other subsystems such as NVMe storage devices or backplanes.

Hybrid connections are defined as those which utilize both B2B and B2C elements to create a single mated interface between two PCBs. For example, if a Riser has a PCB with card edge fingers utilizing B2B to receive Power and Low Speed IO while also using a Twinax B2C connection for HSIO.

Implementors Note:

SFF-TA-1033 is an example of a connector supporting Hybrid connections, it can be used for B2B, B2C or Hybrid connections. While the HPM designer places the SFF-TA-1033, they do not necessarily know beforehand what style of connection the System designer will implement.

B2C

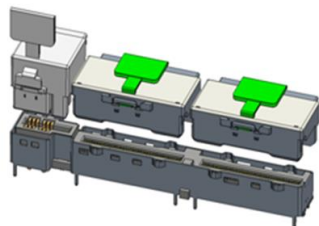


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

B2B

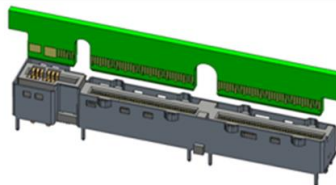


Figure 4-1 Combo x16+21A Power AIC Application

Hybrid

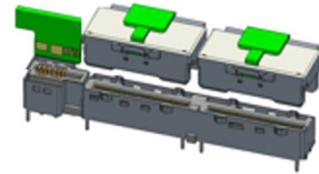


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

1225

10.9.1 DC-MHS Compliant HSIO Connectors

All HSIO connectors shall be compliant with the M-XIO specification and be listed in **Table 4**. Refer to the **DC-MHS Connector List** for vendor part number details.

Table 4: M-SDNO Specification Compliant HSIO Connectors

Use	Compliant Connectors
Near Side Fixed Risers Locations	SFF-TA-1033 (with 21A Power)
All Other HSIO	SFF-TA-1016 SFF-TA-1026 SFF-TA-1033

Note: Additional connectors may be added to future revisions of this specification *after* electrical definition by M-XIO.

DC-MHS HPMs allow for B2B, B2C or Hybrid risers. For best compatibility with many DC-MHS system designs, HPMs should implement riser connectors adhering to the guidance in **Section 10.9.2**.

All other HSIO connectors adhere to common guidance in **Section 10.9.3**.

Implementors Note:

HSIO cable choices are outside the scope of M-SDNO. The SFF-TA-1016 and SFF-TA-1033 connectors can accept both cable types but mixing cable/connector types may result in loss of the anti-tilt feature.

10.9.2 Near Side Fixed Riser Connectors

A DC-MHS riser may utilize B2B, B2C or Hybrid connectivity schemes. Riser and other endpoint device definition are outside of the scope of this specification.

To enable chassis and I/O subsystem compatibility and reuse, fixed riser locations are defined:

- M-SDNO HPM Class A supports two riser locations.
- M-SDNO HPM Class B supports three riser locations.
- M-SDNO HPM Class C supports four riser locations.
- M-SDNO HPM Class D supports six riser locations.

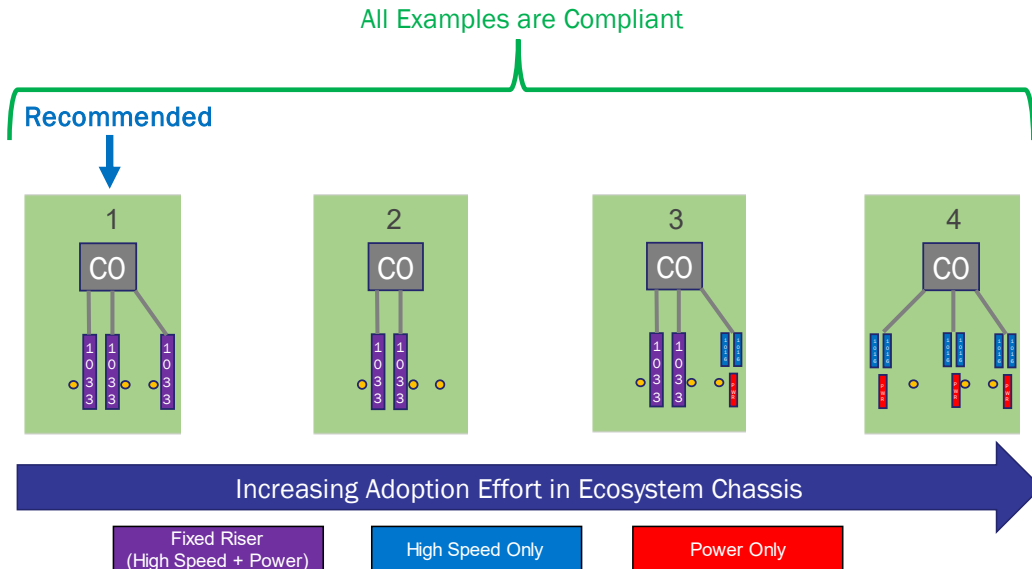
Note that the location of Riser 3 and Riser 4 differ relative to the HPM datum for different Classes. This is due to the different “pitch” of half wide HPMs when deployed in a common chassis with Class C and D. Refer to **Section 9: HPM Concepts and Layouts** for more information.

HPMs which implement near side fixed risers shall:

- Use a Fixed Riser connector defined in **Section 10.9.1**
- Place them in the location(s) defined in **Section 10.9.2.1**
- Full population of all Near Side Fixed Risers Locations is not required, as there may be technical or other reasons to exclude certain positions. It is recommended to implement as many fixed riser locations as possible.

Implementors Note:

For maximum ecosystem compatibility, designing an HPM to utilize as many Fixed Riser locations as possible is strongly encouraged. Utilizing these connectors in a fixed location allows System Designers to use B2B, B2C or Hybrid connections as best suits their use case. In the figure below, all four Class B layouts are M-SDNO compliant, however, layout ‘1’ is recommended because it implements all defined Fixed Riser connectors.



10.9.2.1 SFF-TA-1033 Fixed Riser Implementation Details

SFF-TA-1033 fixed riser connectors which are implemented shall follow **Figure 59**, **Figure 60**, and **Figure 61** which define the required location of the SFF-TA-1033 connectors.

Note that SFF-TA-1033 has various versions. All SFF-TA-1033 Near Side Fixed riser connectors shall use a 21A power block version. Refer to the **DC-MHS Connector List** for vendor part number details.

Figure 59: Class A-B Required Riser Locations with Recommended Connector

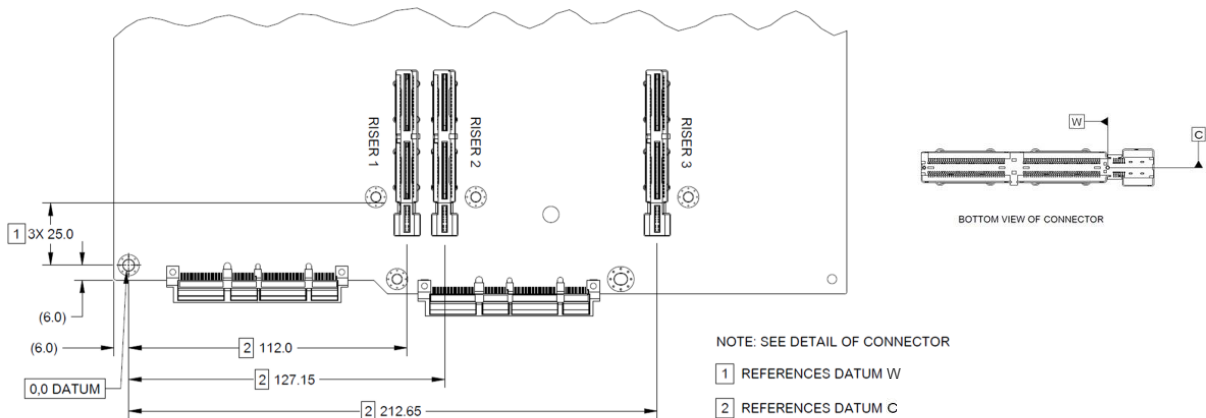
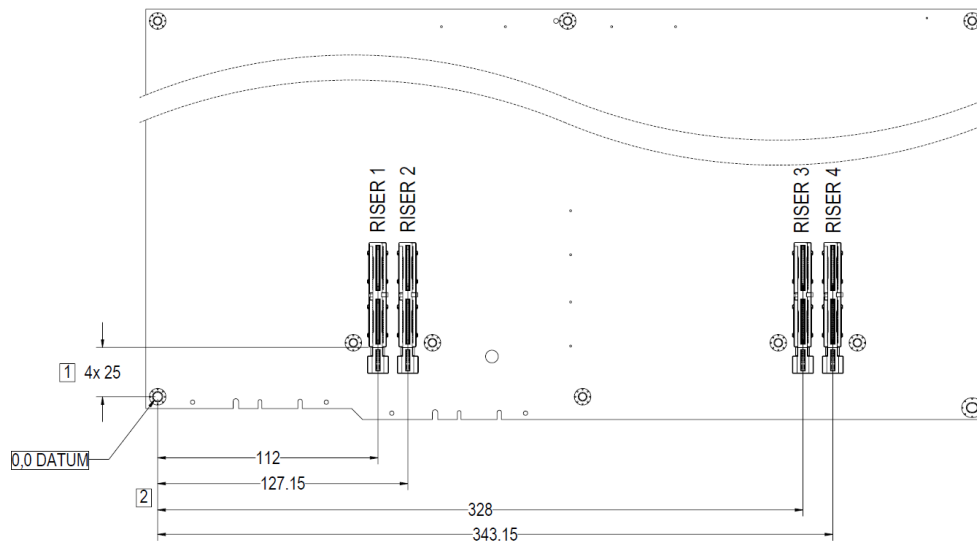


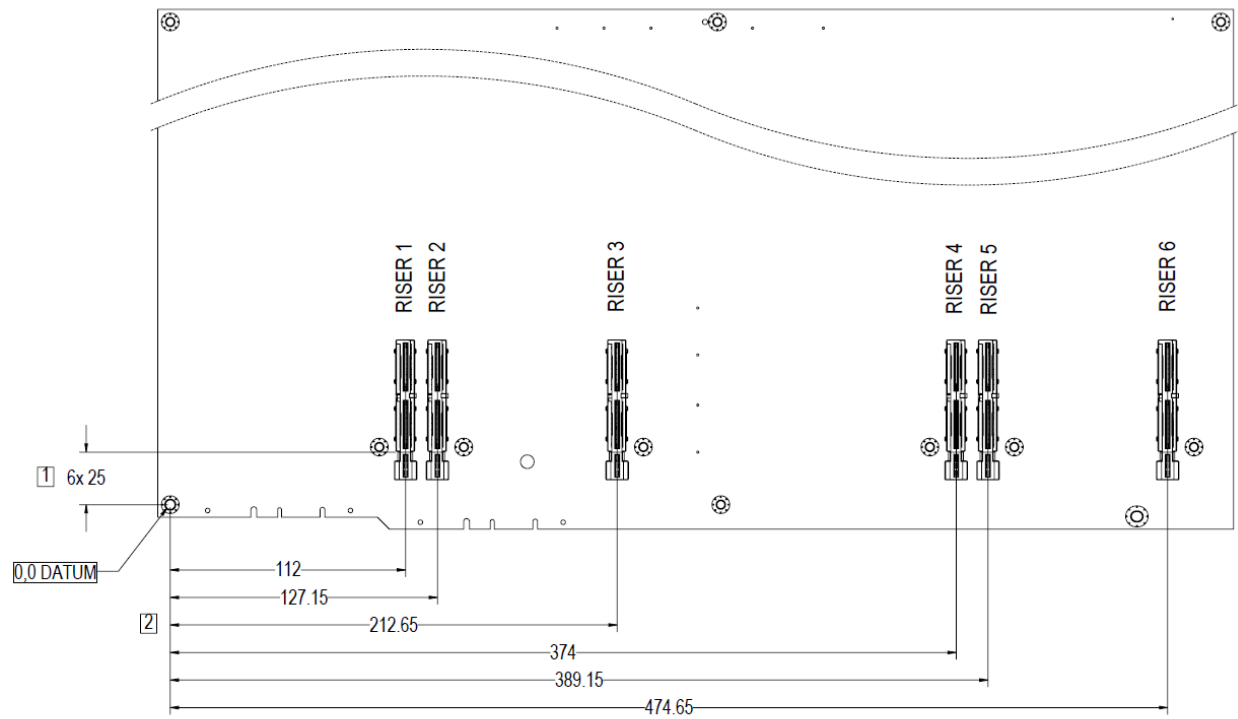
Figure 60: Class C Required Riser Locations with Recommended Connector



NOTES:

- 1] VERTICAL DIMENSION TO SFF TA-1033 DATUM W.
- 2] HORIZONTAL DIMENSIONS TO SFF TA-1033 DATUM C.

Figure 61: Class D Required Riser Locations with Recommended Connector



PRIMARY SIDE

NOTES:

- [1] VERTICAL DIMENSION TO SFF TA-1033 DATUM W.
- [2] HORIZONTAL DIMENSIONS TO SFF TA-1033 DATUM C.

1285

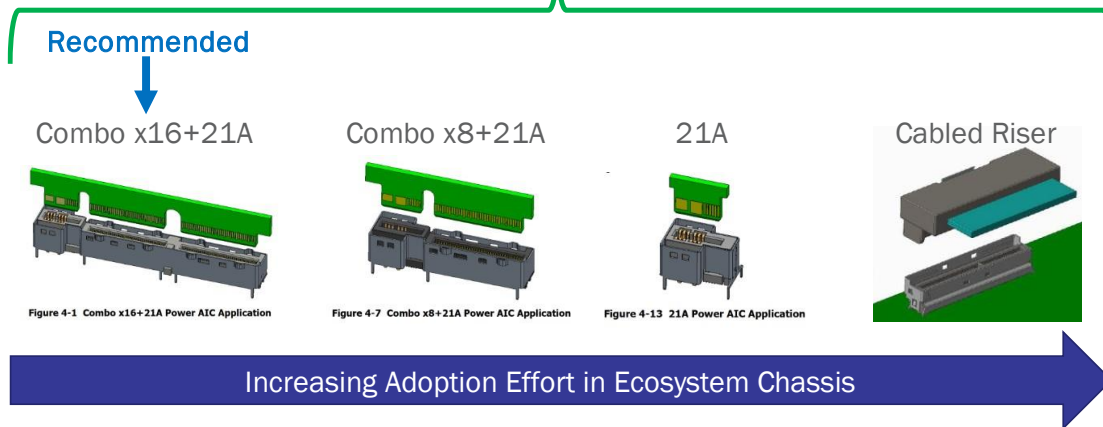
Implementors Note:

Use of the Combo x16+21A connector, wired as a x16, is highly recommended for ecosystem compatibility. If HPMs are unable to support the maximum number of Fixed Riser connectors, it is recommended that the HPM designer consider reduced ecosystem compatibility in the following order:

- 1) Use the SFF-TA-1033 Combo x16+21A, wired as a x8 in compliance with M-XIO
- 2) Change the SFF-TA-1033 Combo x16+21A to the SFF-TA-1033 Combo x8+21A
- 3) Change the SFF-TA-1033 Combo x16+21A to the 21A Power only
- 4) Change to a B2C Riser with connectors adhering to **Section 10.9.3**

SFF-TA-1033 Fixed Riser Connector Options

All Examples are Compliant

**10.9.3 Other HSIO Connectors**

Except for the Fixed Riser Connectors described in **Section 10.9.2**, HSIO connector positions and quantity are not defined by this DC-MHS base specification. The HPM Designer is free to place them wherever they wish so long as they do not interfere with other required features (e.g. a required mounting hole) and while adhering to the component height restrictions in **Section 10.10**.

All implemented HSIO connectors shall be defined in M-XIO and listed in **Table 4**. Any combination of these connectors is allowed.

10.10 Primary Side Component Height Restrictions and KOZs

All M-SDNO Classes shall adhere to a common approach of three different component height restriction zones as shown in **Figure 62** through **Figure 65**.

- 1300 • The **12mm Zone** is intended to allow for extended heatsinks and other thermal solutions while not prohibiting cabling of HSIO. Adherence to the 12mm zone is strongly recommended. While deviations are allowed, HPM designers should limit component selections which exceed the restriction to reduce interference with system design elements which will expect to inhabit this space and may cause system compatibility issues.
- 1305 • The **11.3mm Zone** is intended to avoid interference with PCIe CEM cards directly above the HPM and its peripherals. Adherence to the 11.3mm Zone shall be required.
- The **6mm Zone** is the most restrictive and is intended to prevent interference with mechanical elements in support of the fixed riser locations and retention holes. Adherence to the 6mm Zone shall be required.

1310 Zone height restrictions apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of soldered components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

Allowed exceptions to these zones are:

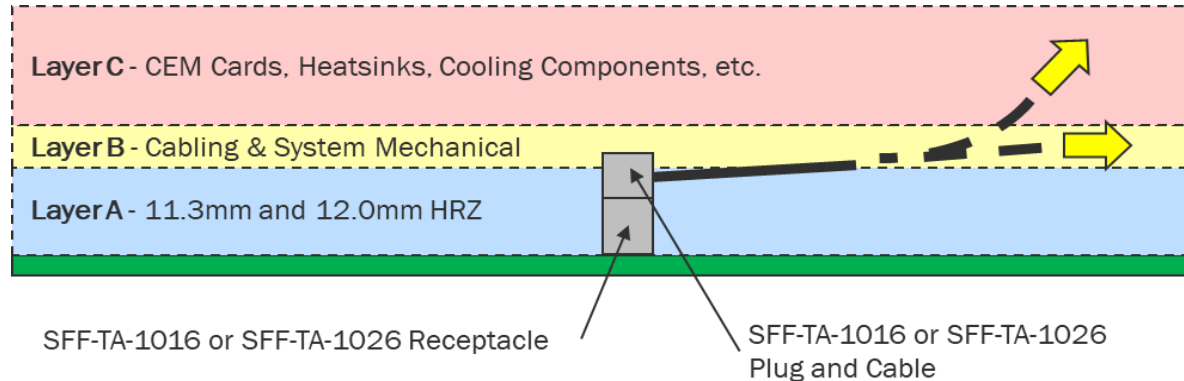
- 1315 • DIMM connectors
- Connectors in specified Fixed Riser locations (**Section 10.9.2**)
- Plugs to connectors placed by this specification (e.g. vertical PICPWR or USB plugs).
- Connectors listed in **Table 4: M-SDNO Specification Compliant HSIO Connectors** may be placed in the 11.3mm and 12.0mm Component Height Restriction Zones. The
- 1320 mating plugs for these connectors may exceed the HRZ depending on which connectors and plug types are chosen. As a result, an exception is allowed for these two connector types in the 11.3mm and 12.0mm HRZs. HPM designers should place these connectors with careful consideration of potential system use cases for their HPM.

This specification does not specify a specific Keep Out Zone for cable enablement.

1325

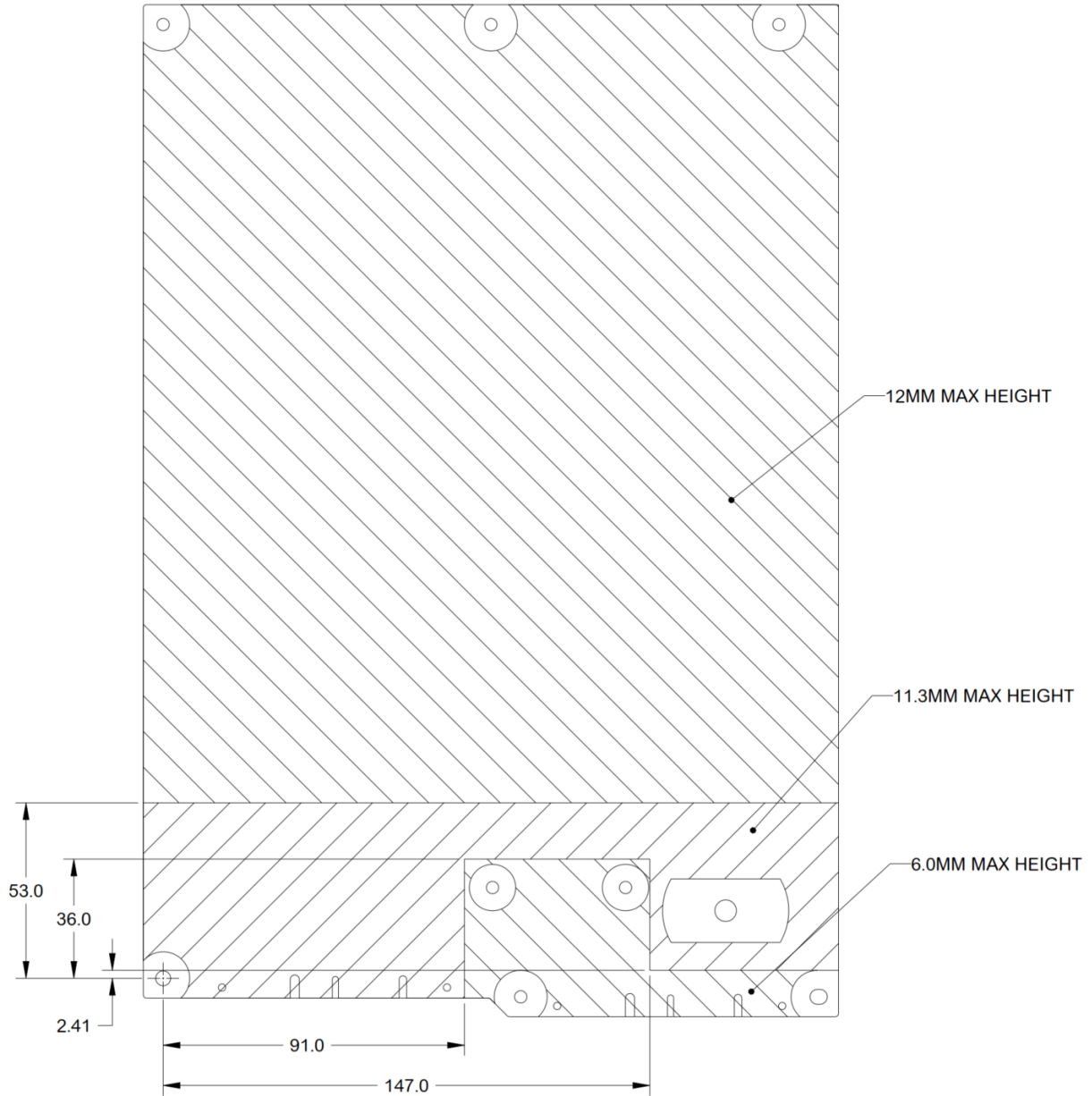
Implementors Note:

A height exception may be needed for the SFF-TA-1016 & SFF-TA-1026 connector + cable plug based on an understanding that a system design layer exists between the HPM HRZs (Layer A) and the Major Component Layer of a system (Layer C). Layer B is a mechanical design layer where cabling may route and sheet metal structures may be created in the system's chassis design. A system designer needs to understand the mated heights of plug + receptacle for the SFF-TA-1016 and SFF-TA-1026 connectors to be able to accommodate their occasional and purposeful intrusions into Layer B.



10.10.1 Class A HPM Primary Side Component Height Restrictions

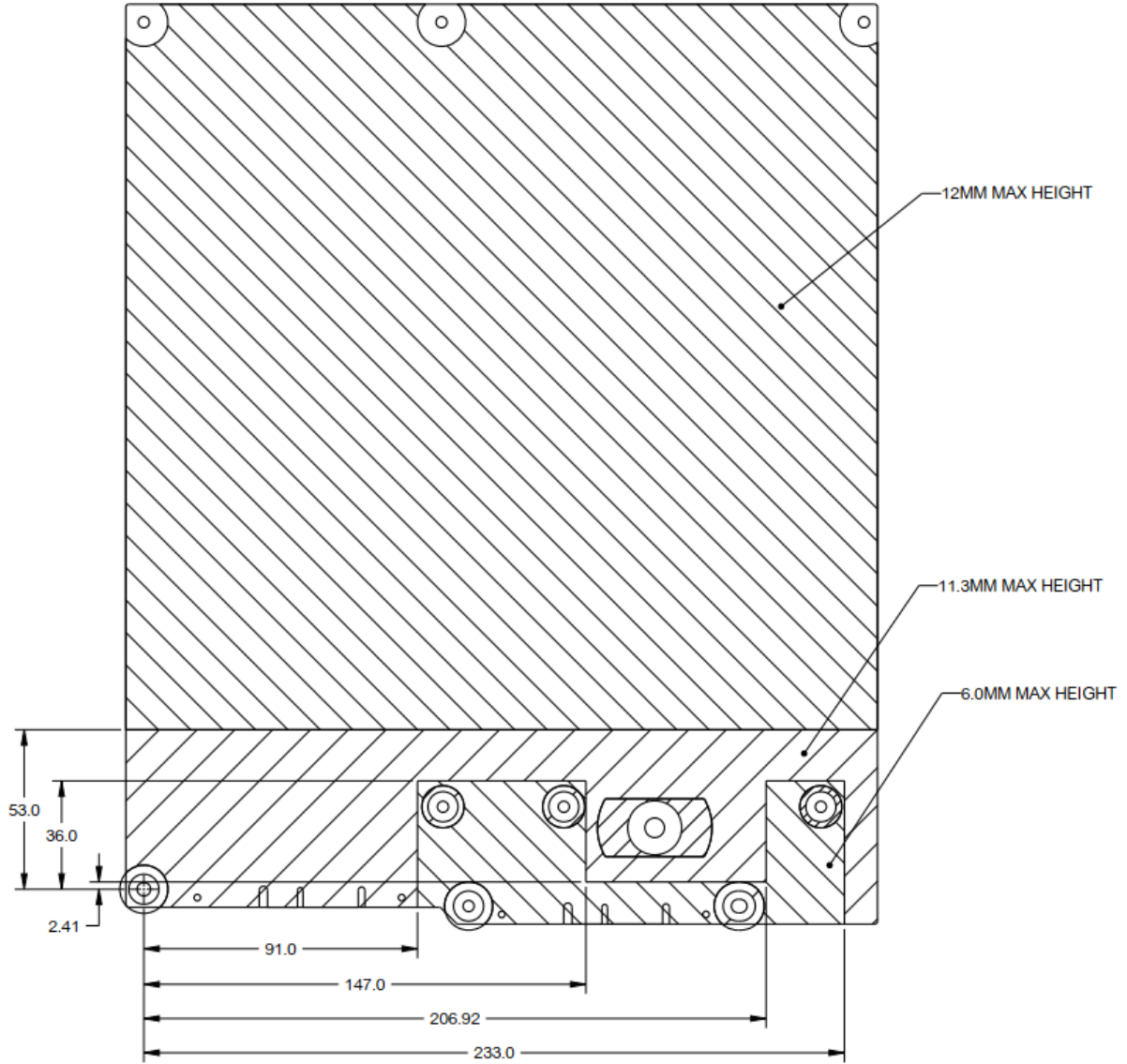
Figure 62: Class A Component Height Restriction Zones (PRIMARY SIDE)



1330

10.10.2 Class B HPM Primary Side Component Height Restrictions

Figure 63: Class B Component Height Restriction Zones (PRIMARY SIDE)



1335

Technical drawing of the primary side of a component, showing a cross-section with dimensions and labels.

Dimensions and labels include:

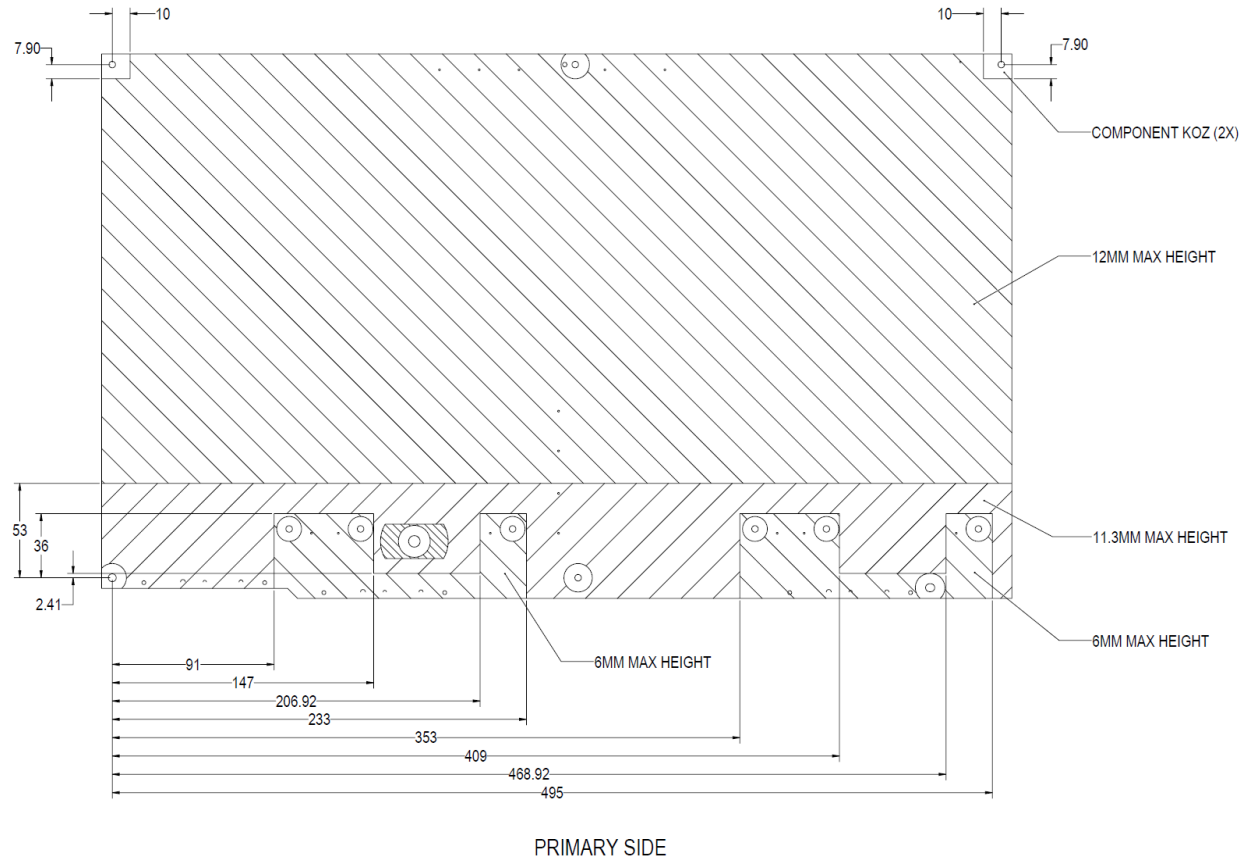
- 10 (top left corner dimension)
- 7.90 (top left corner dimension)
- 10 (top right corner dimension)
- 7.90 (top right corner dimension)
- COMPONENT KOZ (2X) (top right corner label)
- 12MM MAX HEIGHT (right side label)
- 53 (left side vertical dimension)
- 2X 36 (left side vertical dimension)
- 2X 2.41 (left side vertical dimension)
- 91 (bottom horizontal dimension)
- 147 (bottom horizontal dimension)
- 206.92 (bottom horizontal dimension)
- 307 (bottom horizontal dimension)
- 363 (bottom horizontal dimension)
- 6MM MAX HEIGHT (bottom center label)
- 6MM MAX HEIGHT (bottom right label)
- 11.3MM MAX HEIGHT (bottom right label)

PRIMARY SIDE

1340

10.10.4 Class D HPM Primary Side Component Height Restrictions

Figure 65: Class D Component Height Restriction Zones (PRIMARY SIDE)



1345

10.11 Class B Platform Custom Zone

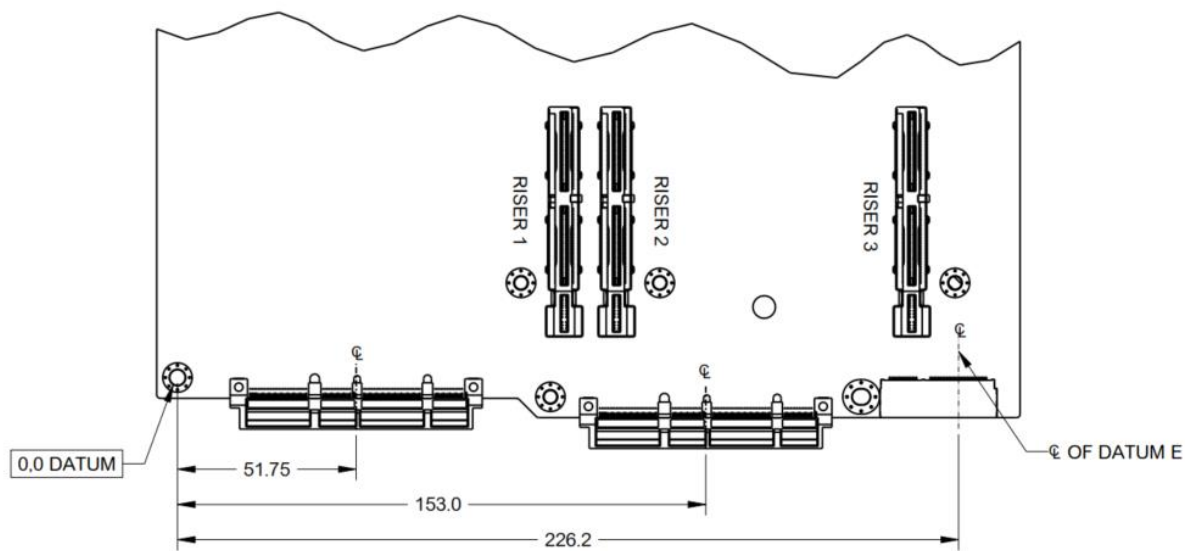
The Class B Platform Custom Zone runs along the near side board edge from the OCP NIC R3 to the “right” side board edge as shown in **Section 9.2: Class B HPM Layout**. The specification defines some options that are considered common use cases to promote greater compatibility between future HPMs.

10.11.1 Class B Direct Dock E1.S

An HPM design may want to support direct docking E1.S (SNIA EDSFF) in the Platform Custom Zone. These HPM designs should follow the recommended placement guidance for SFF-TA-1002, 2C connector in **Figure 66**. Refer to the M-PIC specification, chapter “E1.S Direct Attach Boot Storage” for complete connector and pinout guidance.

Note that dimensioning has been changed from early specification revisions to reference the centerline of Datum E in the SFF-TA-1002 connector specification. Additionally, the defined location allows for either 1C or 2C connector variants to be placed (only 2C is shown).

Figure 66: Class B HPM with Direct Dock E1S in Custom Zone



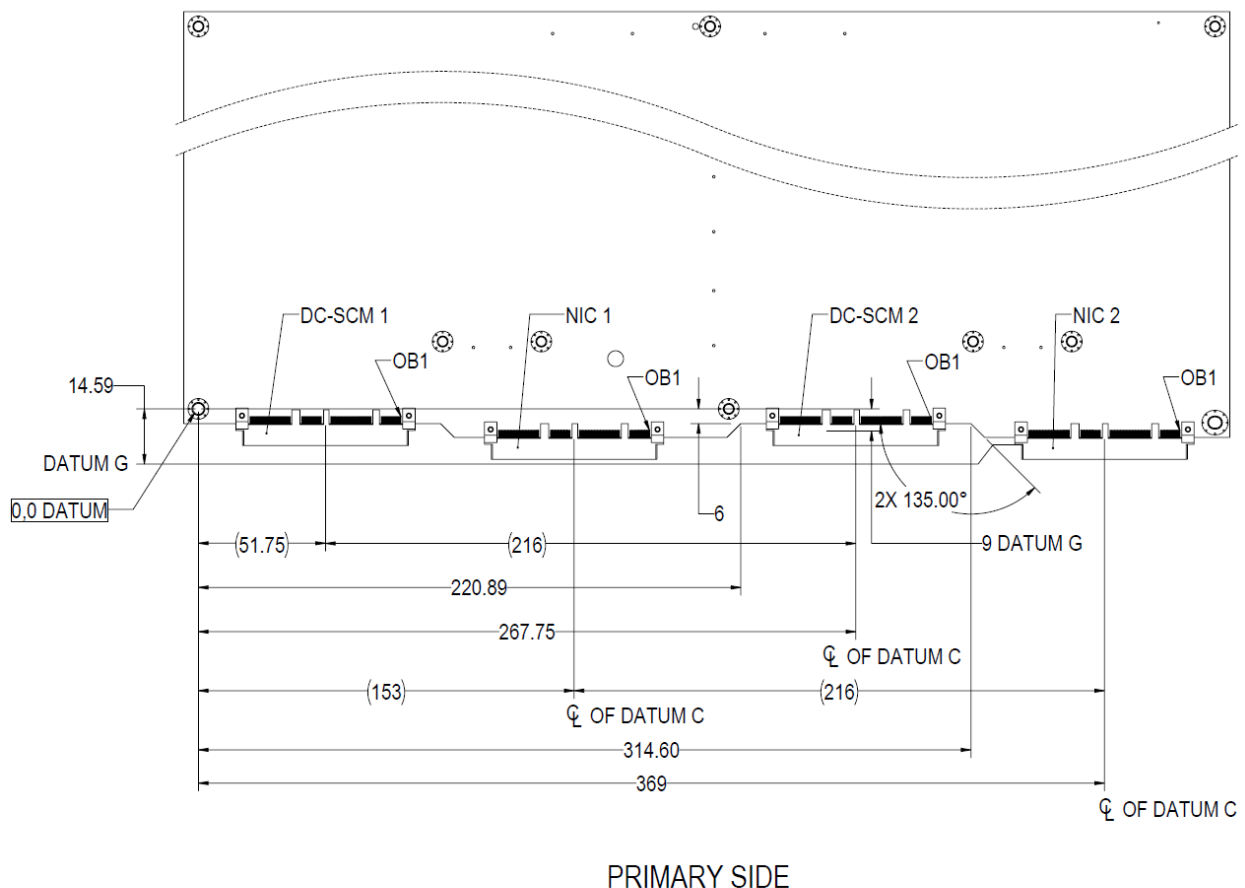
10.12 Class C Platform Custom Zone

Class C includes a Platform Custom Zones that runs along the near side board edge between the SCM R2.x connector and the “right” board edge of the PCB as shown in **Section 9.3: Class C HPM Layout**. The specification defines some options that are considered common use cases to promote greater compatibility between future HPMs.

10.12.1 Class C Second OCP SFF NIC R3 and/or Second OCP SCM 2.X

A Class C HPM design may want to support a second OCP NIC R3.0 and/or a second OCP SCM 2.X. When implementing either of these secondary functions, HPM designs should follow the placement in **Figure 67** for the second connector(s). This placement ensures the common SDNO A/B/C chassis as described in **Figure 13: Common 19” Chassis Supporting Class A, B and C**. The OCP DSFF NIC3 would not be supported in this case.

Figure 67: Class C HPM 2nd OCP SFF NIC and/or 2nd DC-SCM in Platform Custom Zone



NOTES:
1. REFER TO SFF TA-1002 SPECIFICATION FOR 4C+ DATUM C
AND DATUM G DEFINITIONS.

Implementors Note:

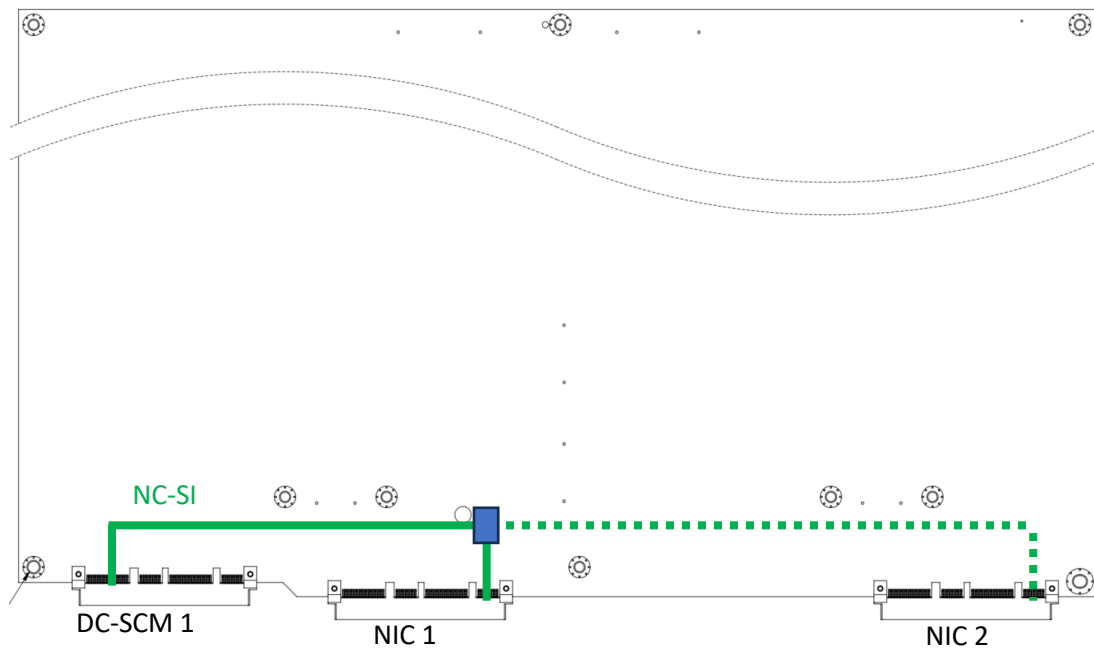
The DC-SCM DC-SCI is designed to support up to two RMII/NC-SI RMII-based transport interfaces, facilitating sideband communication between the DC-SCM to the NIC(s).

For DC-SCM applications utilizing a single NC-SI, it is advised to employ the first NC-SI interface instance (utilizing pins B43-B49). Upon integrating NIC 2 into the HPM with a single DC-SCM, it is strongly recommended to establish an NC-SI RBT connection to NIC 2, rather than leaving it disconnected. The connection of NC-SI to NIC 2 can be achieved through one of the following methods:

1. A multidrop topology extending from the first NC-SI, or
2. An active MUX/Switch derived from the first NC-SI, or
3. A second NC-SI originating from the DC-SCM (illustration not provided).

The selection of the optimal topology is not covered within this specification; for further guidance, please consult the OCP NIC & DC-SCM Base Specifications. For additional information on NC-SI, refer to DMTF DSP0222.

NOTE: When implementing DC-SCM 2 (illustration not provided), DC-SCM 1 and NIC 1 may share a dedicated NC-SI, while DC-SCM 2 and NIC 2 can utilize a dedicated NC-SI.



10.12.2 Class C OCP NIC R3 DSFF

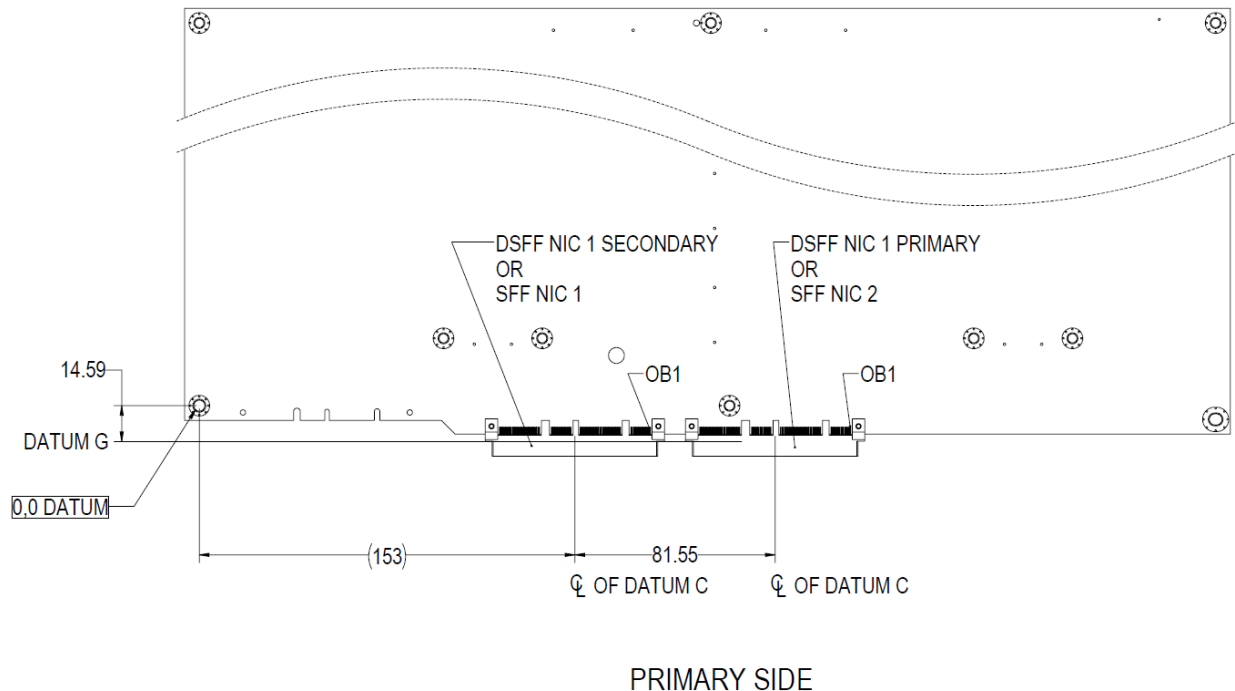
1380 A Class C HPM design may want to support the DSFF variant of the OCP NIC R3. When
 implementing this optional feature, the HPM design should follow **Figure 68: Class C HPM OCP**
 DSFF NIC in Platform Custom Zone. This feature requires the use of two SFF-TA-1002 4C+
 connectors. Note that the use of “secondary” and “primary” connector naming convention in
 1385 **Figure 68: Class C HPM OCP DSFF NIC in Platform Custom Zone** was chosen for consistency
 with the naming convention used in the OCP NIC R3 specification for DSFF.

Also note that the use of DSFF is incompatible with the use of the secondary DC-SCM2.X
 option described in **Section 10.12.1**.

This placement also does NOT support the common SDNO A/B/C chassis as described in
Figure 13: Common 19” Chassis Supporting Class A, B and C.

1390

Figure 68: Class C HPM OCP DSFF NIC in Platform Custom Zone



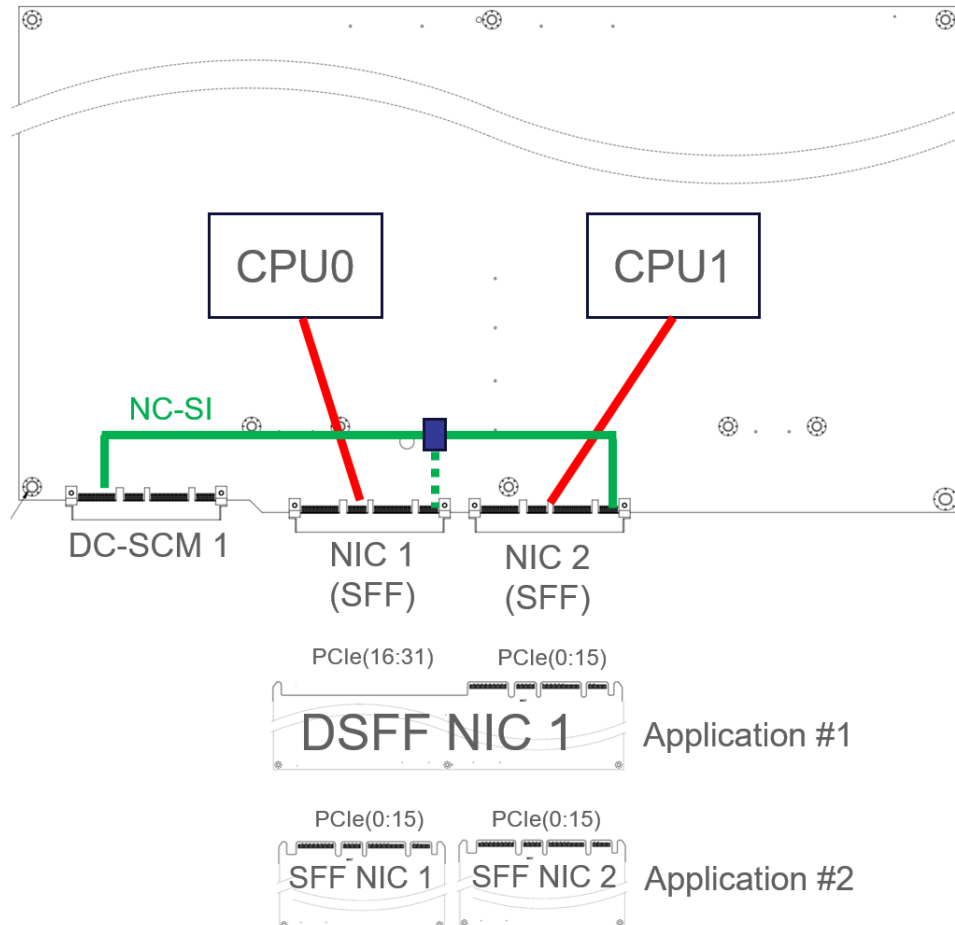
NOTES:

1. REFER TO SFF TA-1002 SPECIFICATION FOR 4C+ DATUM C AND DATUM G DEFINITIONS.

Implementors Note:

OCP DSFF NICs have the option to implement downshifting on the Secondary Connector card edge when operating with 16 or fewer lanes of PCIe and when the power consumption is 80W or less. It is important for HPM designers to recognize that NIC1's connector is still adjacent to DC-SCM 1 but the DSFF's Primary Connector moves to the NIC 2 (SFF) position and shall always incorporate the sideband and power functionality.

In configurations utilizing dual CPUs, it is typical for the PCIe lanes from CPU0 to connect to NIC 1, and those from CPU1 to connect to NIC 2. However, when employing a dual CPU setup alongside DSFF NICs, special attention is required as CPU1 may be unpopulated and/or brought offline. The use of a downshifted DSFF NIC could result in CPU0 losing its PCIe connection. Given that the purpose of having two SFF-TA-1002 4C+ connectors is to accommodate either one DSFF NIC or two SFF NICs, the M-SDNO Base Specification strongly advises HPM implementations to use a complete set of OCP NIC sideband functionalities on both the Primary and Secondary DSFF 4C+ connectors. (This includes NC-SI, as previously mentioned in **Section 10.12.1**).



10.13 Class D Platform Custom Zone

1395 Class D includes a Platform Custom Zones that runs along the near side's board edge between the SCM R2.x connector and the "right" edge of the PCB as shown in **Section 9.4: Class D HPM Layout**. The specification defines some options that are considered common use cases to promote greater compatibility between future HPMs.

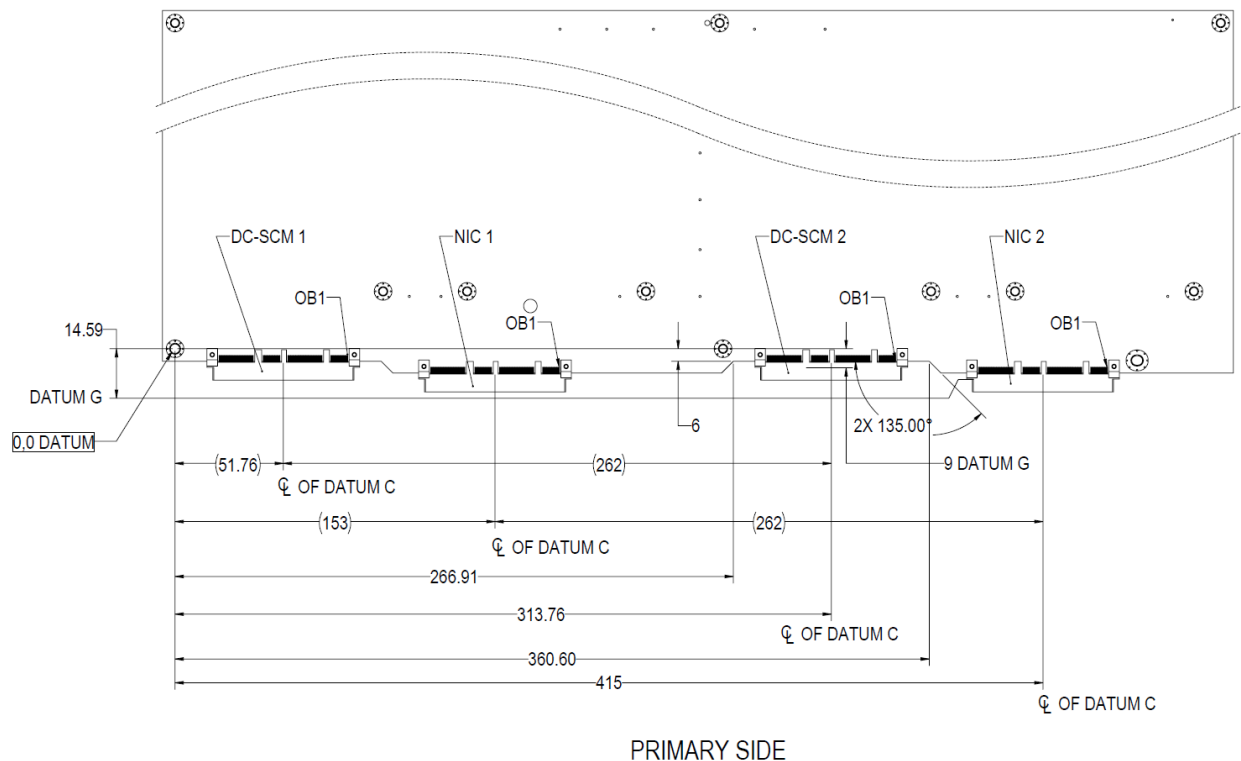
10.13.1 Class D Second OCP SFF NIC R3 and/or Second OCP SCM 2.X

1400 A Class D HPM design may want to support a second OCP NIC R3.0 and/or a second OCP SCM 2.X. When implementing either of these secondary functions, the HPM designs should follow the placement in

Figure 69 for the second connector(s). This placement ensures the common SDNO A/B/D chassis as described in **Figure 15: Common 21" Chassis Layout for Class A, B and D**. The OCP DSFF NIC3 would not be supported in this case.

Please see NC-SI Implementor's Note in **Section 10.12.1 Class C Second OCP SFF NIC R3 and/or Second OCP SCM 2.X**

Figure 69: Class D HPM 2nd OCP SFF NIC and/or 2nd DC-SCM in Platform Custom Zone



NOTES:
1. REFER TO SFF-TA-1002 SPECIFICATION FOR 4C+ DATUM C AND DATUM G DEFINITIONS.

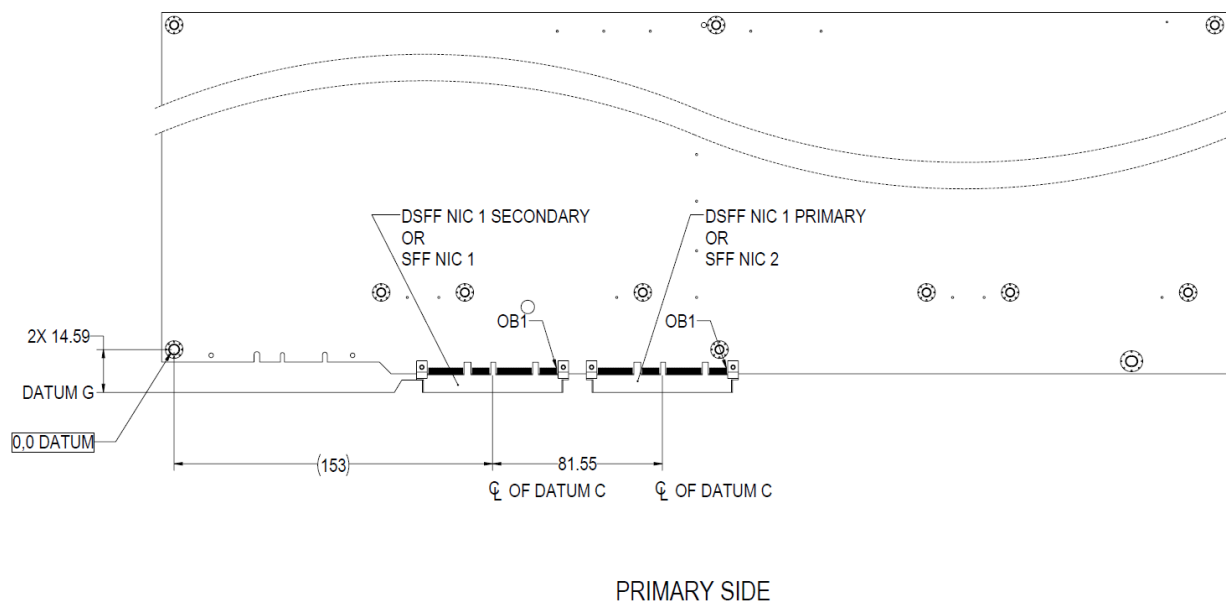
10.13.2 Class D OCP NIC R3 DSFF

A Class D HPM design may want to support the DSFF variant of the OCP NIC R3. When implementing this optional feature, the HPM design should follow **Figure 70**. This feature requires the use of two SFF-TA-1002 4C+ connectors. Note that the use of “secondary” and “primary” connector naming convention in **Figure 70** was chosen for consistency with the naming convention used in the OCP NIC R3 specification for DSFF.

Also note that the use of DSFF is incompatible with the use of the secondary DC-SCM2.X option described in **Section 10.13.1** and the direct dock E1.S described in the following section. This placement also does not support the common SDNO A/B/D chassis as described in **Figure 15: Common 21" Chassis Layout for Class A, B and D**.

Please see DSFF Implementor’s Note in **Section 10.12.2 Class C OCP NIC R3 DSFF**

Figure 70: Class D HPM OCP DSFF NIC in Platform Custom Zone



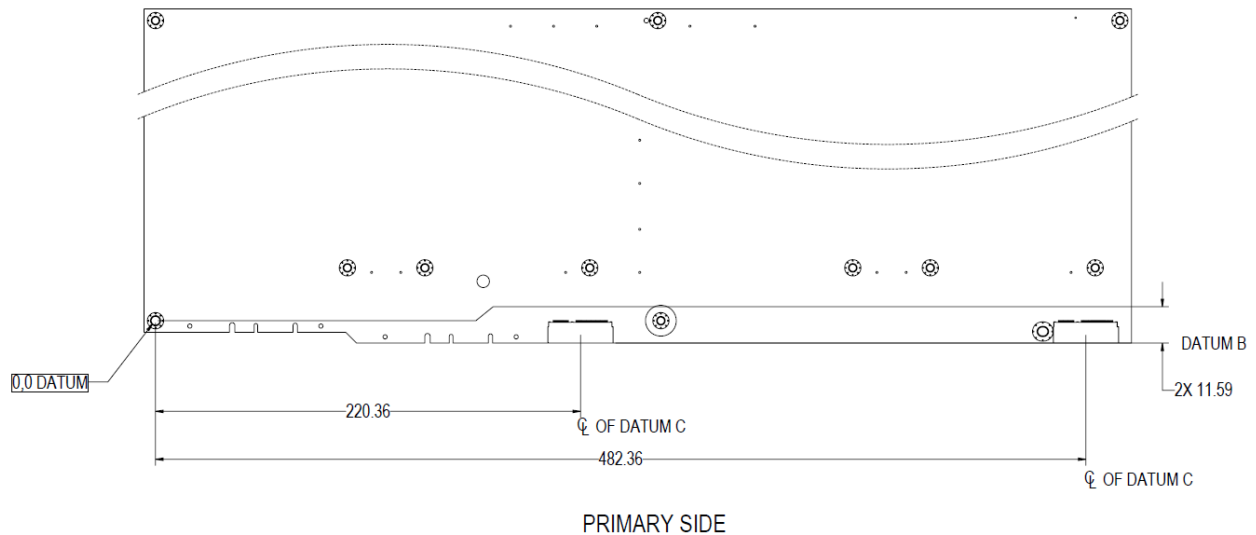
NOTES:
1. REFER TO SFF TA-1002 SPECIFICATION FOR 4C+ DATUM C AND DATUM G DEFINITIONS.

10.13.3 Class D Direct Dock E1.S

An HPM design may want to support direct docking E1.S (SNIA EDSFF) in the Platform Custom Zone. These HPM designs should follow the placement guidance for SFF-TA-1002, 2C connector in **Figure 71**. See M-PIC specification, chapter “E1.S Direct Attach Boot Storage” for complete connector and pinout guidance.

The defined location allows for either 1C or 2C connector variants to be placed (only 2C is shown).

Figure 71: Class D HPM with Direct Dock E1S in Platform Custom Zone 2



NOTES:

1. SFF TA-1002 2C OPTION SHOWN.
2. SFF TA-1002 1C IS ALTERNATE OPTION.
3. 1C POSITION SHOULD BE DERIVED FROM INDICATED 2C POSITION.
4. REFER TO SFF TA-1002 SPECIFICATION FOR 2C DATUM B AND DATUM C DEFINITION.

11 Power Zones

1440 M-SDNO compliant HPMs are assumed to Ingress / Egress 12V DC. While alternate voltages are under consideration for future versions (e.g. 48V DC implementations), this version assumes the burden for alternate power sources is placed on the system power delivery infrastructure (PDB, bus bar, etc.). For information on Power Management (including Power Gating and use of sideband signals) refer to the M-PIC specification.

Implementors Note:

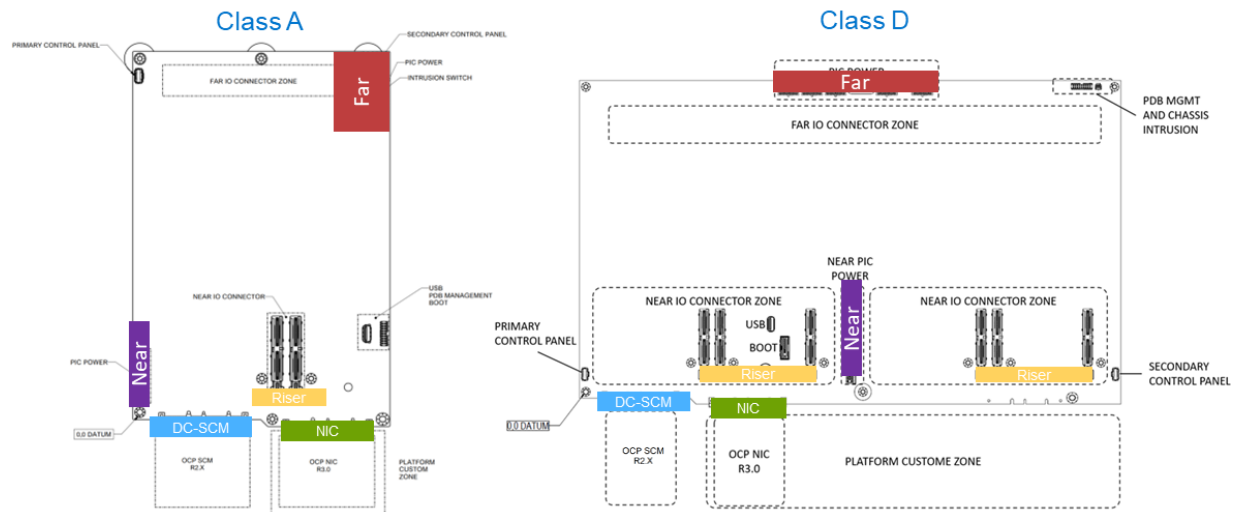
The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in private and/or public HPM design specification(s) for system configurations supported per HPM design.

1445 11.1 HPM Power Zone Overview

To enable a variety of system power configurations (See **Section 14.2 M-SDNO Power Zone Usage**) there are two defined bi-directional power zones for each HPM Class referred to as the “Near” and “Far” Ingress / Egress zones as shown in **Figure 72**. These zones are intentionally placed on opposing sides of the HPM to maximize flexibility of system orientation.

1450 Additional power zones include power egress to DC-SCM, OCP NIC and each fixed Riser location.

Figure 72: M-SDNO Power Zone Overview (Class A and D Depicted)



11.2 Near and Far Bi-Directional (Ingress / Egress) Power Zones

11.2.1 Ingress / Egress Cabled Power Connector

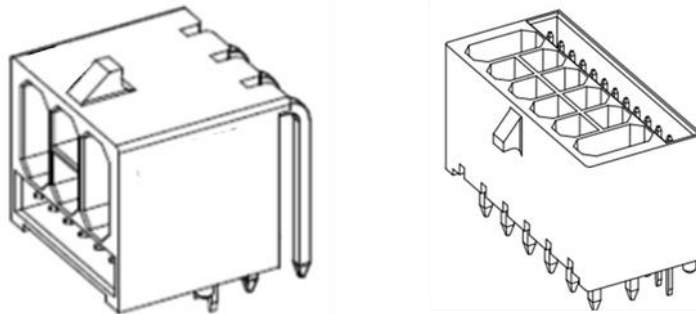
- **Power Connector Type:** 2x6+12SB and/or 2x3+6SB PICPWR
Refer to M-PIC Specification and DC-MHS Connector List for additional details.
- **Connector Power Rating:** 864W (2x6) / 486W (2x3)
- **Typical usage:** Power ingress to HPM and / or egress to peripheral subsystems

It is assumed that most systems will provide power to M-SDNO based HPMs via a cabled solution from a Power Distribution Board (PDB).

To maximize reuse of power delivery across all M-SDNO HPMs, the required connectors for all cabled Ingress / Egress power shall be the 2x6+12SB or 2x3+6SB PICPWR. An example of the 2x3+6 and 2x6+12SB is depicted in **Figure 73**.

Refer to the M-PIC specification for more information on PICPWR compliant connectors.

Figure 73: Example 2x3 + 6SB (Right Angle) and 2x6 + 12SB PICPWR Connector (Vertical)



Implementors Note:

HPMs which implement the cabled PICPWR connectors may still be used in multi-node systems via an interposer or interface board to enable blind mate into system backplane / infrastructure. Refer to **Section 14.1 M-SDNO Conceptual Implementation Examples** for an example of such a system.

11.2.2 Power Requirements (All Classes)

11.2.2.1 Common Far Power Zone Requirements

1475 Each HPM Class defines a Far side Zone where PICPWR connectors must be placed. In addition, recommended placements are provided within the Zone for each HPM Class.

1480 The far power zone shall include the body of at least 1 2x6+12SB PICPWR connector, additionally, enough connectors shall be placed within the zone such that the far power zone is capable of meeting the full HPM power budget when used for ingress.

2x3+6SB may also be used within the far power zone.

Dimensioning of PICPWR is to Circuit 1 and is intended to be consistent for 2x6+12SB or 2x3+6SB selections.

1485 There are no additional Class specific requirements for the Far Power Zone.

11.2.2.2 Common Near Power Zone Requirements

1490 Each HPM Class defines a Near side Zone where PICPWR connectors may be placed. In addition, recommended placements are provided within the Zone for each HPM Class.

2x6+12 and 2x3+6SB may be used within the near power zone.

Dimensioning of PICPWR is to Circuit 1 and is intended to be consistent for 2x6+12SB or 2x3+6SB selections.

1495 Additional Class specific requirements are provided in **Section 11.2.3** through **11.2.6**.

Implementors Note:

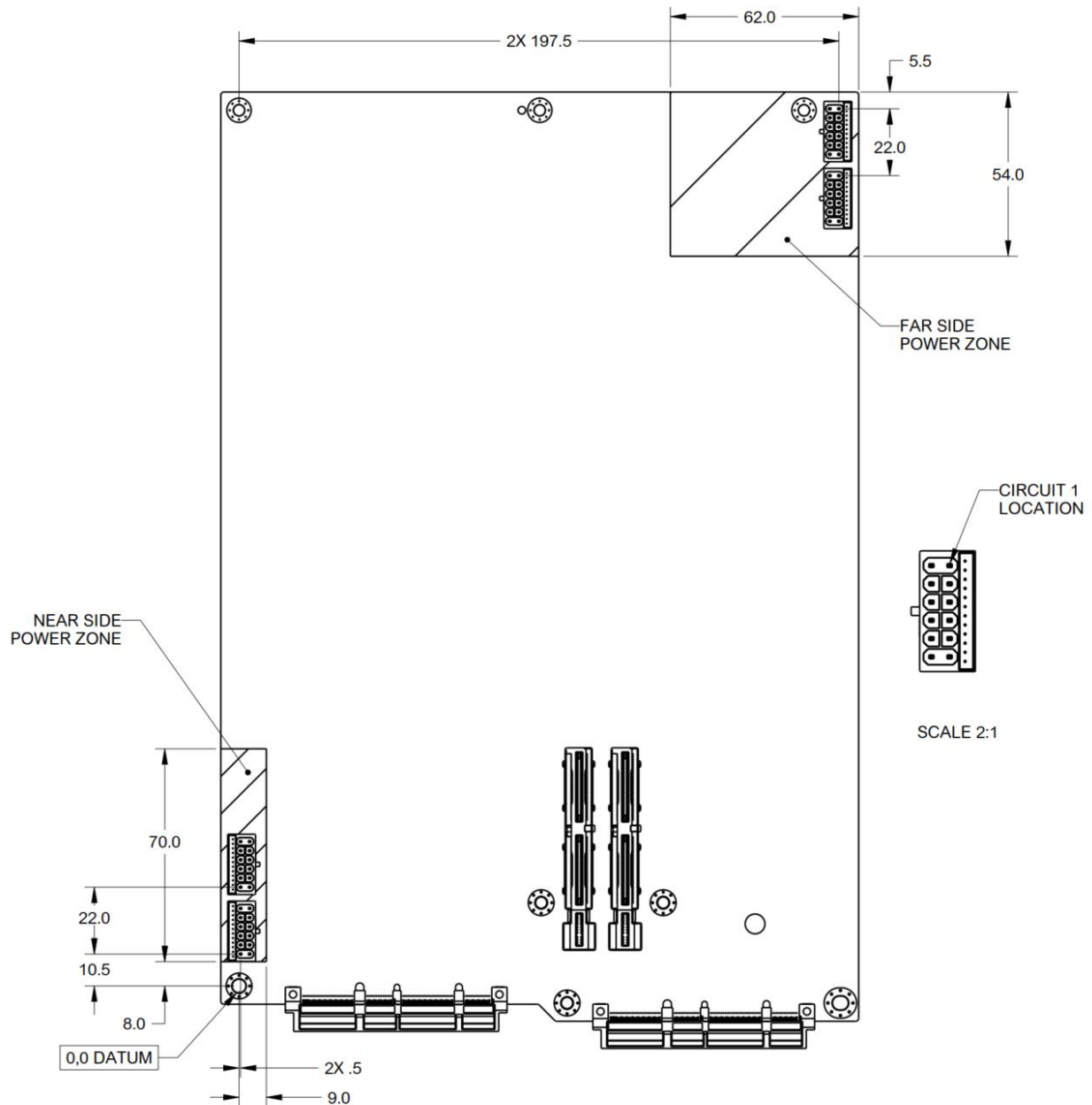
If providing Ingress power via the Near Power Zone is desired, it is recommended that the connector configuration matches the connector configuration of the Far Power zone to maximize flexibility for Power Ingress / Egress.

11.2.3 Class A Ingress / Egress Power Connector Locations

11.2.3.1 Near Side Power Zone– Class A Specific

The Near Side Power Zone is not required for Class A HPMs, at a minimum, a single 2x3+6 (for egress to a peripheral subsystem) is strongly recommended.

Figure 74: Class A HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE)



11.2.4 Class B Ingress / Egress Power Connector Locations

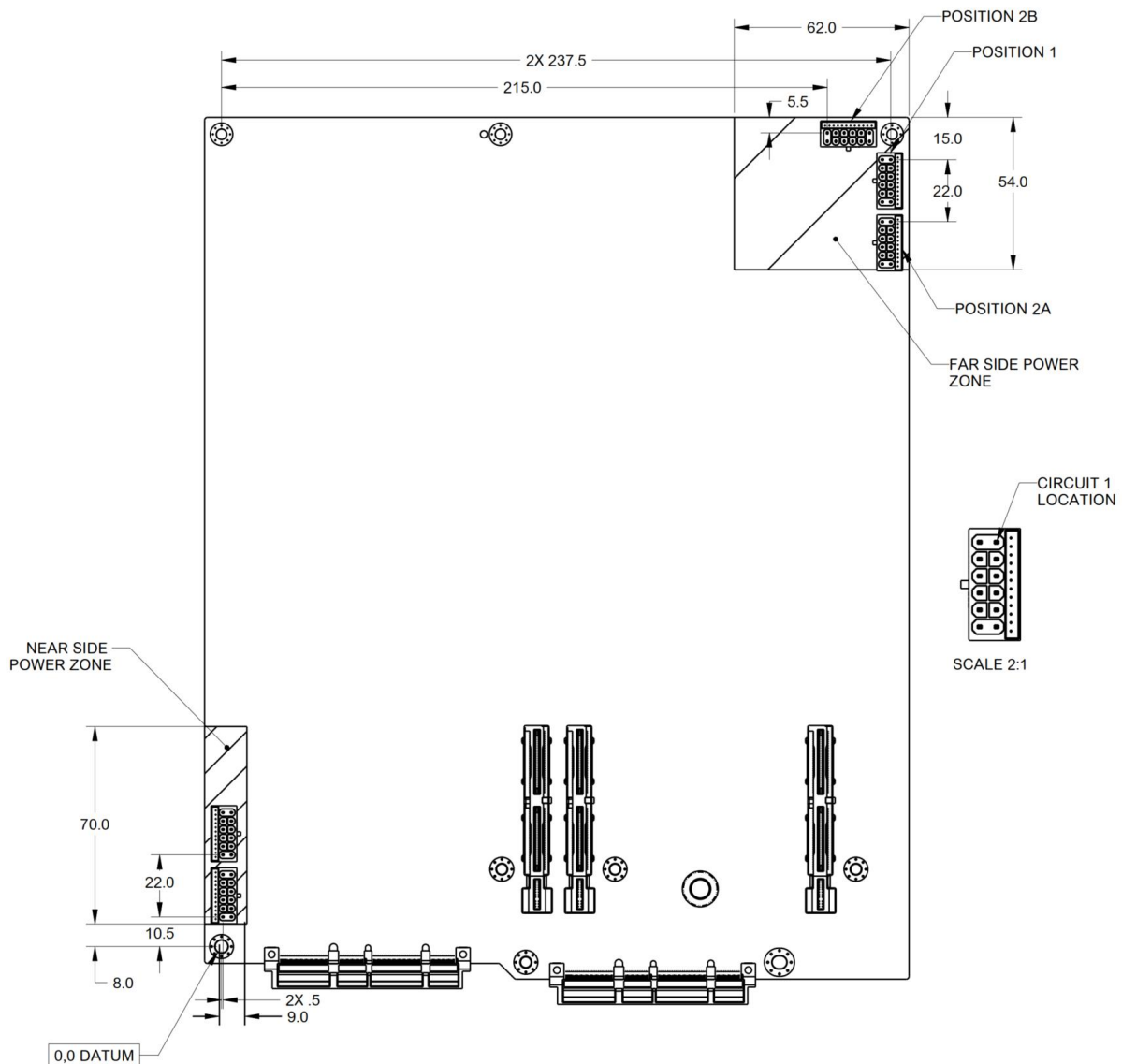
11.2.4.1 Near Side Power Zone– Class B Specific

The Near Side Power Zone is not required for Class B HPMs, at a minimum, a single 2x3+6 (for egress to a peripheral subsystem) is strongly recommended.

11.2.4.2 Far Side Power Zone– Class B Specific

Figure 75 depicts three recommended positions for PICPWR connectors in the Class B Far Side Zone. It is recommended that HPMs implement Position 1 and *either* Position 2A or Position 2B. Position 2A enables a right-angled cable exit while Position 2B may ease HPM layout placement. HPMs which require additional power capability (i.e. to support near side egress power) may choose to implement all three recommended positions.

Figure 75: Class B HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE)

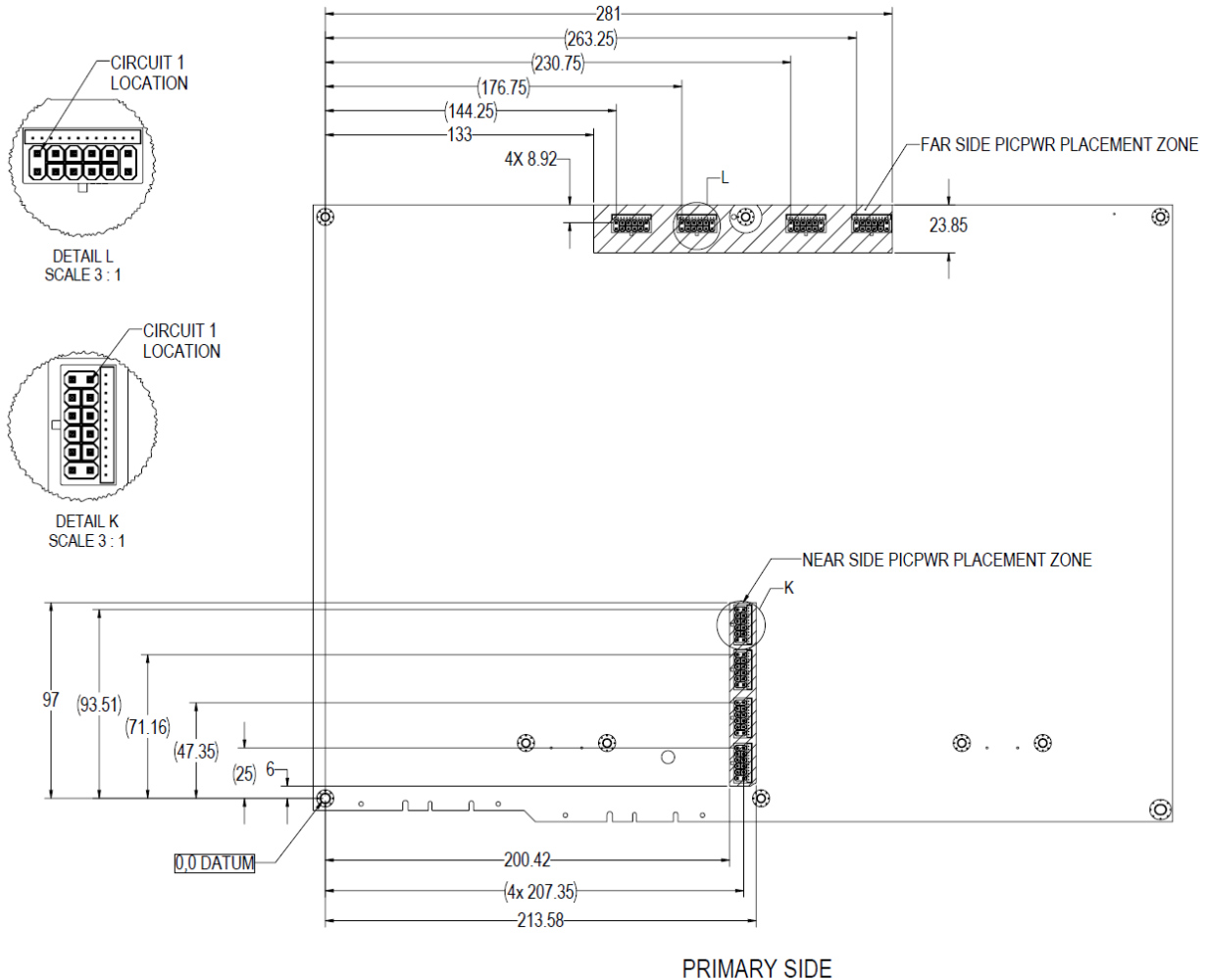


11.2.5 Class C HPM Ingress / Egress Power Connector Locations

11.2.5.1 Near Side Power Zone– Class C Specific

A minimum of one 2x6+12SB PICPWR connector shall be implemented within the zone. The Near Power Zone shall use vertical PIC power connectors.

Figure 76: Class C HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE)



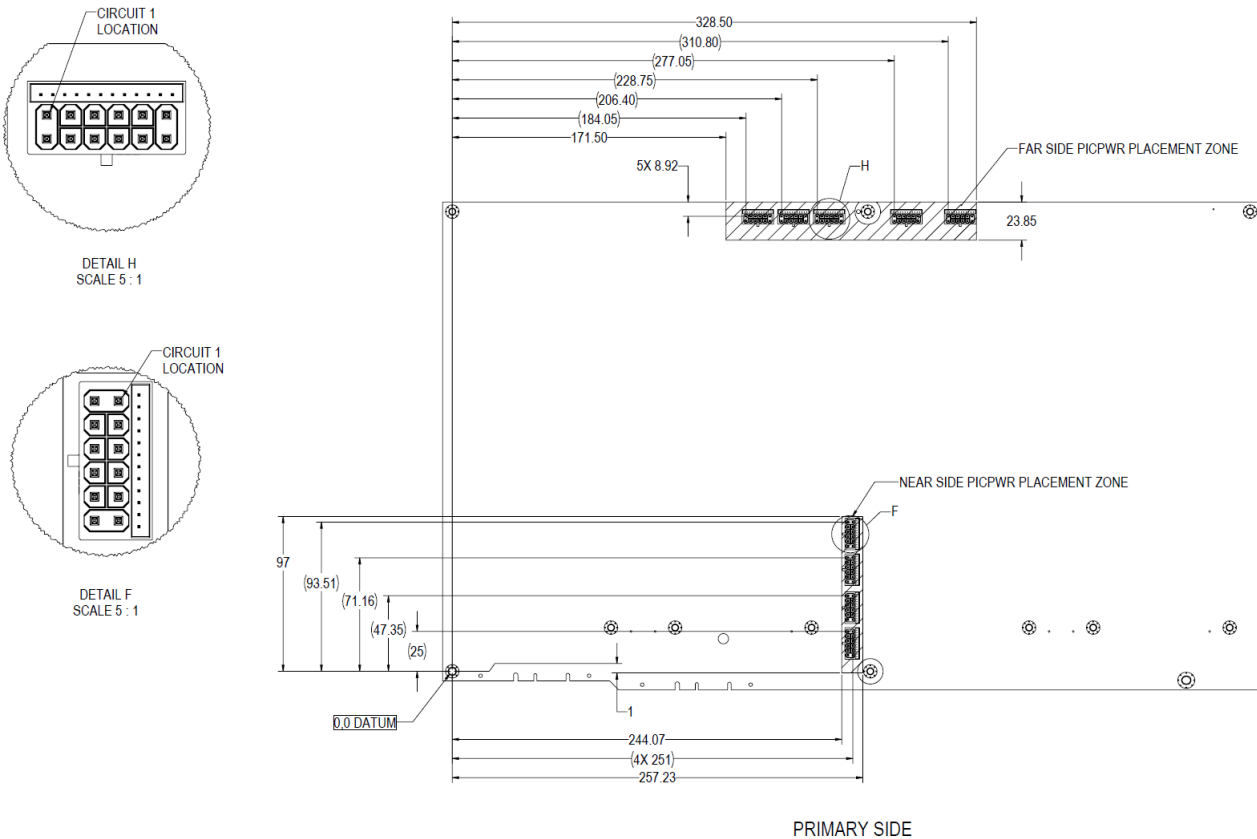
- NOTES:
1. ALL REFERENCE DIMENSIONS ARE TO CONNECTOR PIN CIRCUIT 1.
 2. CROSS-HATCHED AREA IS KEEP IN ZONE FOR PICPWR CONNECTORS.
 3. FAR SIDE ZONE MAY USE VERTICAL OR RIGHT ANGLE PICPWR CONNECTORS.

11.2.6 Class D HPM Ingress / Egress Power Connector Locations

11.2.6.1 Near Side Power Zone– Class D Specific

1525 A minimum of one 2x6+12SB PICPWR connector shall be implemented within the zone. The Near Power Zone shall use vertical PIC power connectors.

Figure 77: Class D HPM Near and Far Power Zone Connector Locations (PRIMARY SIDE)



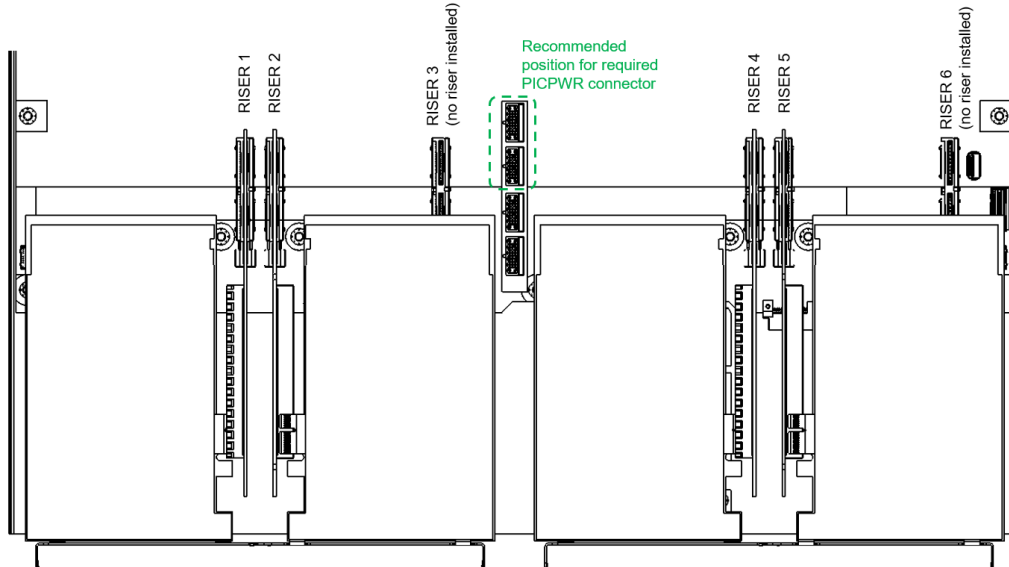
NOTES:
 1. ALL REFERENCE DIMENSIONS ARE TO CONNECTOR PIN CIRCUIT 1.
 2. CROSS-HATCHED AREA IS KEEP IN ZONE FOR PICPWR CONNECTORS.
 3. FAR SIDE ZONE MAY USE VERTICAL OR RIGHT ANGLE PICPWR CONNECTORS.

1530

The Class D Near Side Power Zone is positioned such that when Risers 2 and 4 are used and the associated PCIe CEM slot(s) are populated with Full Height PCIe CEM cards, there is clearance for the M-PIC power cables to egress upwards from the HPM. See **Figure 78**.

1535

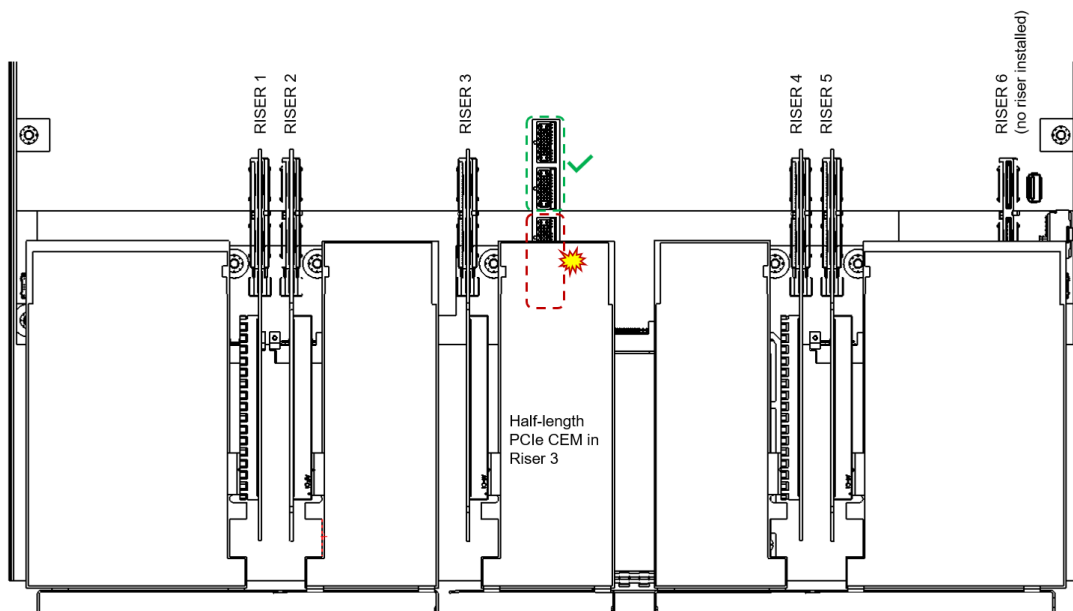
Figure 78: Class D HPM Near Power Zone with Risers 1, 2, 4, and 5 Utilized



When Riser 3 is utilized, the associated PCIe CEM card may obstruct some of the PIC power connectors as shown in **Figure 79**. To minimize this impact, it is recommended that Near Side Power Zone M-PIC power connector population begin within the indicated green box (see check mark in **Figure 79**).

1540

Figure 79: Class D HPM Near Power Zone with Riser 3 Utilized



11.3 Fixed I/O Riser Power

- 1545 • **Power Connector Type:** Integrated within SFF-TA-1033 Recommended Refer to M-PIC Specification and **DC-MHS Connector List** for additional details.
- **Connector Power Rating:** 252W
- **Minimum Power Delivered to Connector by HPM:** 87W
- 1550 • **Typical usage:** Power egress for 1 (required) or more (optional) 75W PCIe CEM Devices per Riser

For each implemented fixed riser location, as specified in **Section 10.9.2** (up to six):

- 1555 • HPMs shall deliver a minimum of 87W of power to the riser connector (See **Table 5** for calculation of 87W effective total power required *per riser*). This requirement is defined to guarantee each riser location can support a minimum of one 75W PCIe CEM card and reduce power cabling requirements in dense systems.
- HPMs may deliver additional power to the riser connector to enable additional cards at each riser location.
- 1560 • Additional supplemental I/O power (e.g. auxiliary power for a GPU) is not defined and is assumed to be provided directly by system infrastructure (e.g. cable from PDB).
- Riser connector shall comply with M-PIC PICPWR sideband signaling requirements.

Table 5. Minimum HPM Power Provided to Fixed Riser Locations

Power Rail	75 W Slot ¹
+3.3Vaux	Generated on PCIe riser. Derived from +12V
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from +12V
+12V Voltage Current	12V nominal 7.25A total: 5.5 A (CEM 5.0) + 1.0A (VR conversion to V_{cc3_3}) + 0.35A (VR conversion to +3.3Vaux) + 0.40A (misc.)

11.4 DC-SCM R2.x Power

- 1565 M-SDNO HPMs shall provide power to the DC-SCM R2.x connector as defined in the OCP DC-SCM R2.x spec (Refer to **Section 13**). As the power requirements of DC-SCM peripherals will vary, HPM designers are encouraged to support as close to the specification defined maximum power as possible to optimize ecosystem compatibility.

11.5 OCP NIC R3.0 Power

- 1570 When implemented, M-SDNO HPMs shall provide power to the OCP NIC R3.0 connector(s) as defined in the OCP NIC R3.0 spec (Refer to **Section 13**). As the power requirements of NIC peripherals will vary, HPM designers are encouraged to support as close to the specification defined maximum power as possible to optimize ecosystem compatibility.

11.6 Platform Custom Zone Power

Power to the Platform Custom Zone is not defined as it is considered implementation specific.

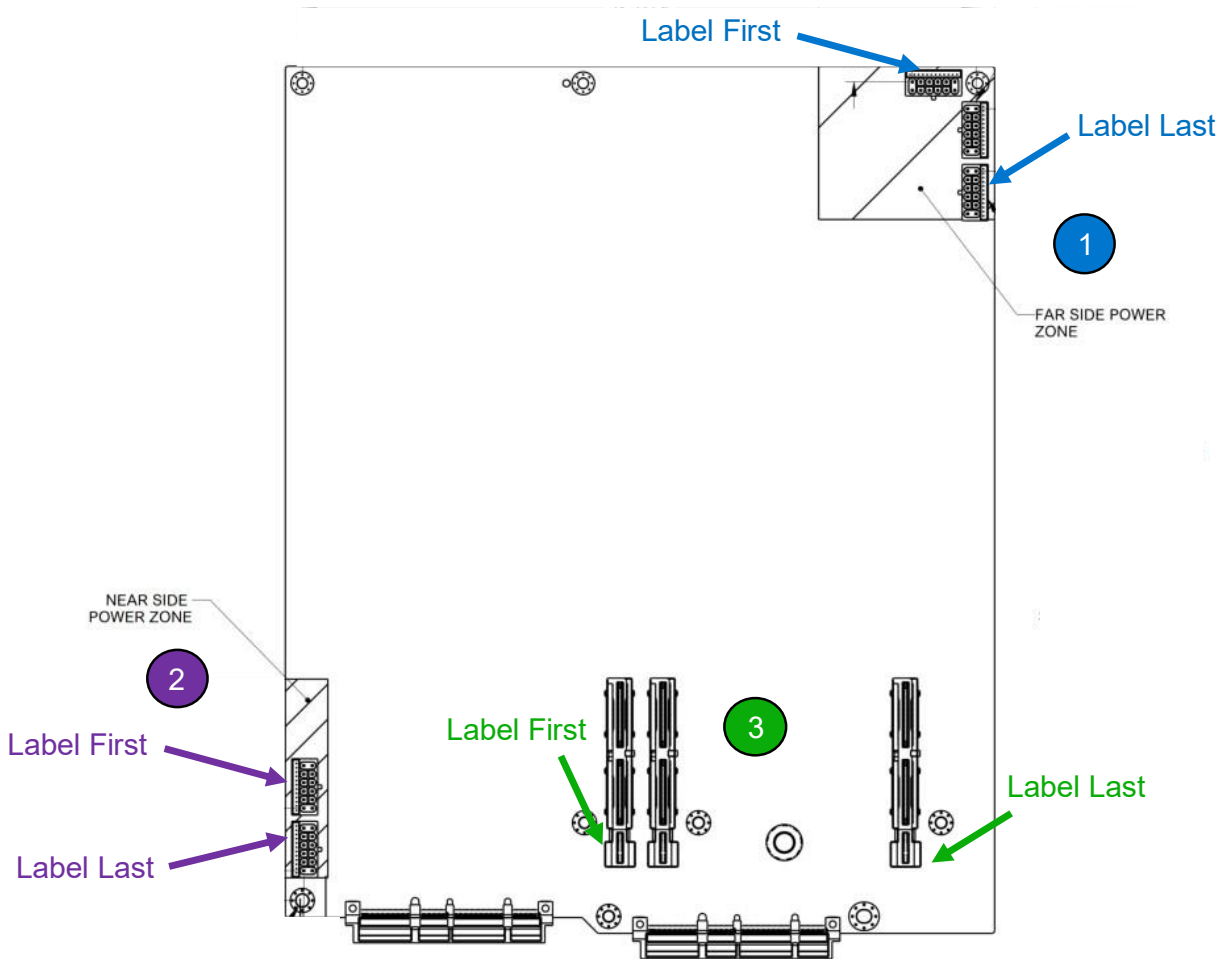
11.7 PICPWR Labeling Order

It is recommended to label PICPWR connectors in the following order, as shown in **Figure 80**:

1. Label PICPWR connectors in the Far power zone based on Circuit 1 location beginning at the Far Side board edge and moving towards the Near Side board edge. When multiple connectors are aligned horizontally, label connectors from left to right.
2. Label PICPWR connectors in the Near power zone based on Circuit 1 location beginning at the Far Side board edge and moving towards the Near Side board edge. When multiple connectors are aligned horizontally, label connectors from left to right.
3. Label PICPWR sections of any implemented fixed I/O risers from left to right.

For specific details on how to label each PICPWR connector, refer to the M-PIC specification.

Figure 80: Recommended PICPWR labeling order, Class B Shown



12 I/O System (Electrical Interfaces)

1595 The HPM shall be required to implement electrical interfaces that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details, specifically M-PIC, M-XIO, M-CRPS, and M-PESTI specifications.

For information on connector placements, refer to **Section 10.8: Platform Infrastructure Connector Placement (non-power)** and **Section 10.9: High Speed I/O (HSIO) Connectors**.

13 References

1600 Relevant Open Compute Specifications

This specification also relies on the following Open Compute Project specifications.

1. OCP Server Network Interface Card (NIC) R3 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
[Mezz \(NIC\) » Open Compute Project](#)
- 1605 2. OCP Datacenter Secure Control Module (DC-SCM) R2.x – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
[Hardware Management/Hardware Management Module - Open Compute](#)
- 1610 1. OCP Open Rack V3 - Class B and D were developed with Open Rack v3 use cases in mind, please refer to the Open Compute Project specifications for more information
https://www.opencompute.org/wiki/Open_Rack/SpecsAndDesigns

1615 Additional Industry References

- ASMEY14.5 – 2018 Dimensioning and Tolerancing
- Open Rack V3
- SNIA SFF-TA-1002
- SNIA SFF-TA-1016
- 1620 • SNIA SFF-TA-1026
- SNIA SFF-TA-1033
- Open19

14 Supplemental Material

14.1 M-SDNO Conceptual Implementation Examples

The M-SDNO specification has multiple form factor classes to address various product types and sizes. In this section some of the possible configurations and usages for the different classes will be shown.

It is understood that the configurations shown represents a small sample of what could be possible. This section also conveys the reasoning behind the different sizes of HPM associated with the HPM classes.

14.1.1 Class B

The Class B can support 2x FHHL or 2x LPHL CEM cards in 1U. For 2x FHHL CEM cards, only one E1.s can be placed in the Platform Custom Zone. If the right CEM card is changed to LPHL a second E1.s can be added to the Platform Custom Zone horizontally or vertically (not shown).

Figure 81: M-SDNO Class B with 1U PCIe Risers

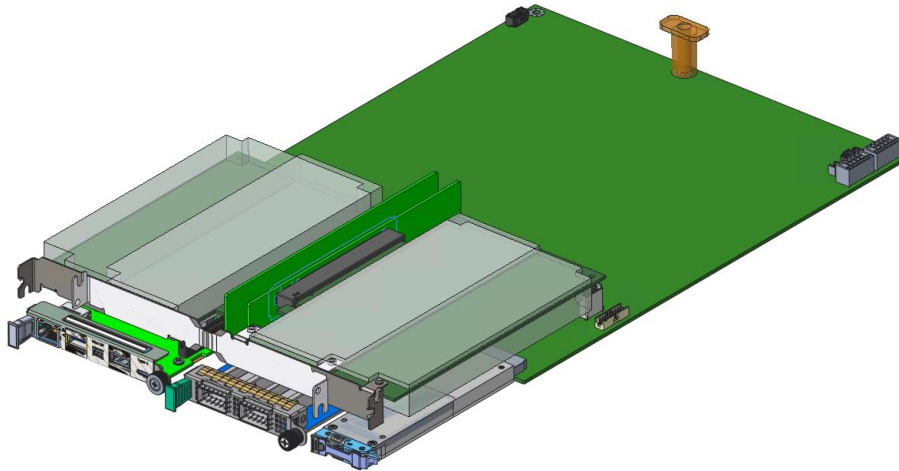
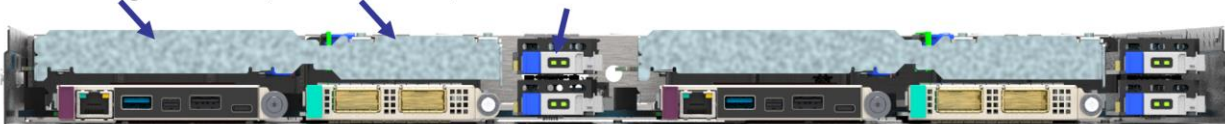


Figure 82: Two Class B HPMs in ORv3 Chassis

One Full height PCIe card, one LP PCIe card, and two E1.S



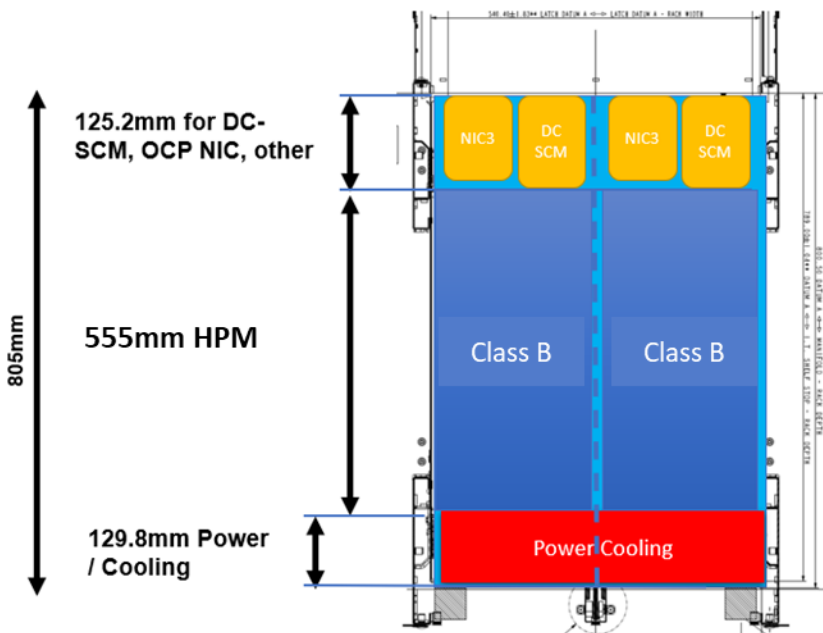
Two Full height PCIe cards and one E1.S



14.1.2 Deep HPMs (A555, B555) in OpenRack v3

Figure 83 depicts assumed ORv3 chassis layout constraints based on Rack Option 1 demonstrating how two B555 HPMs can be used in conjunction with the standard peripherals (OCP NIC and DC-SCM) as well as allocating a region for rack power ingress, PDB and cooling infrastructure (fans or liquid). Two A555 HPMs could also be supported.

Figure 83: ORv3 High Level Layout with 2x B555

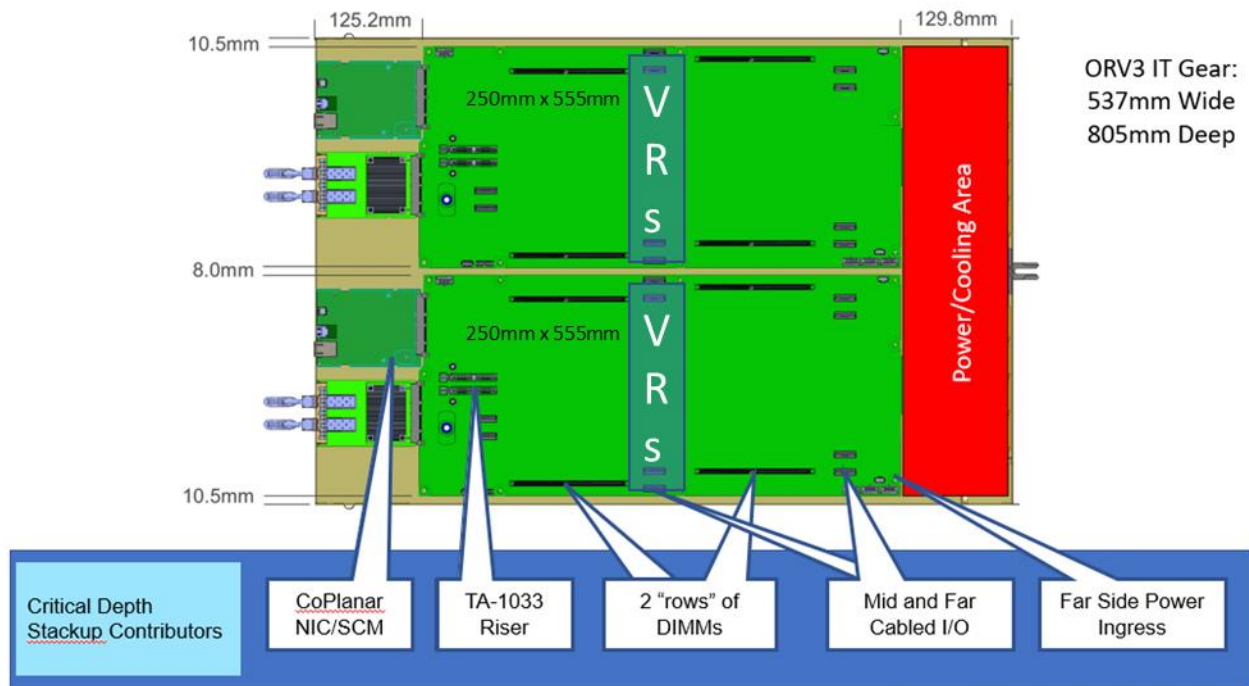


- Based on 802.6mm version (Rack Option 1 in ORv3)
- ~805mm chassis length (face to face)
- Horizontal DC-SCM use
- Full Width and Half Width Service models (will impact HPM width)
- Support co-planar DC SCM / NIC R3 approximately 125mm
- Power /cooling distribution zone is approximately 130mm

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Figure 84 provides a similar view with more detail on the HPM itself, notably we show why the 555mm length was chosen to support the critical depth stack up of Coplanar peripherals, I/O, two CPU + DIMM complexes and power ingress.

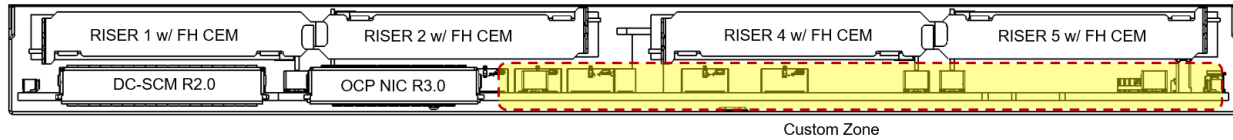
Figure 84: B555 Depth Stackup Example View



1655 **14.1.3 Class D**

Figure 85 to Figure 91 illustrate possible 1U and 2U system IO examples. This is not an exhaustive list of possibilities.

Figure 85: Class D Example – 10U with 4 FH AICs



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Figure 86: Class D Example – 10U with 2 FH and 3 HH AICs

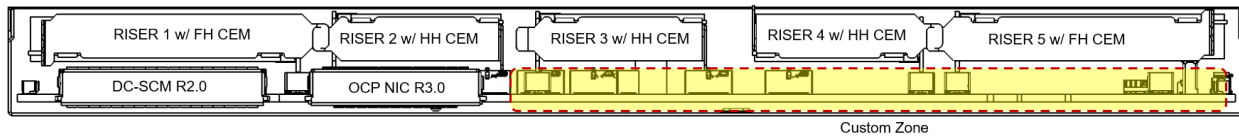
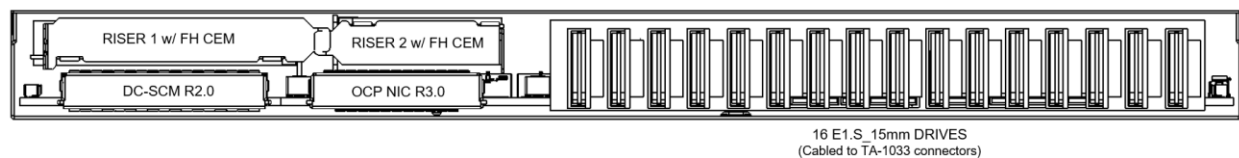


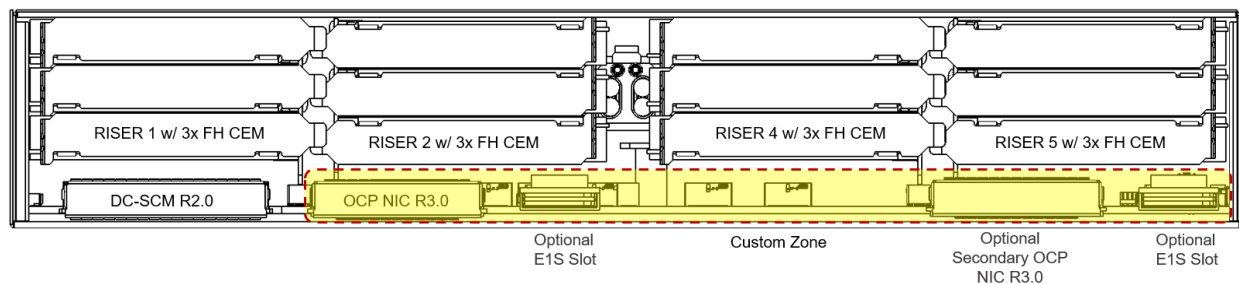
Figure 87: Class D Example – 10U with 1 FH, 1 HH AICs and 16 E1.S



2U risers with more than one PCIe CEM slot would likely need more lanes than a single SFF-TA-1033 can support (max x16). These additional required lanes could be provided via cables from the HPM.

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Figure 88: Class D Example – 20U with 12 FH AICs



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Figure 89: Class D Example – 20U with 6 FH and 9 HH AICs

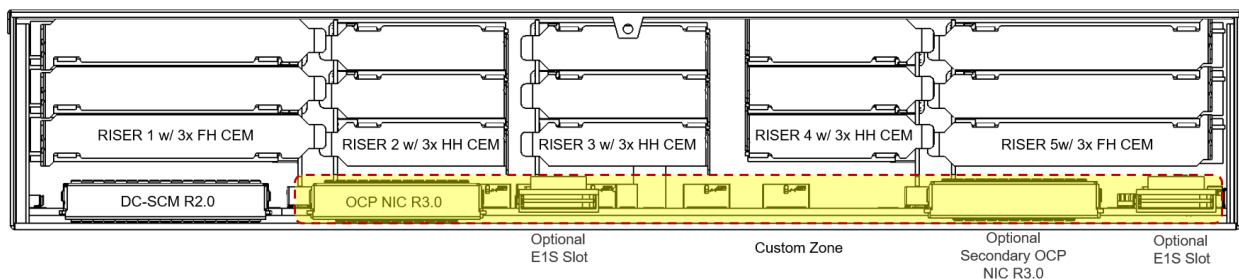


Figure 90: Class D Example – 2OU with 4 FH AICs and 30 E1.S

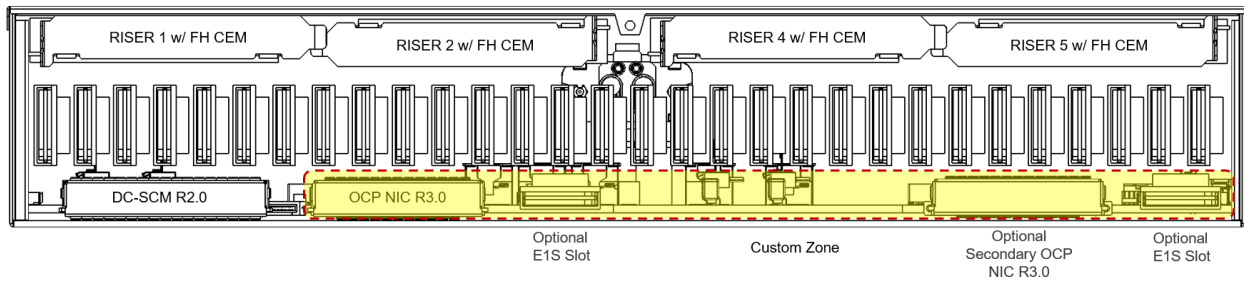
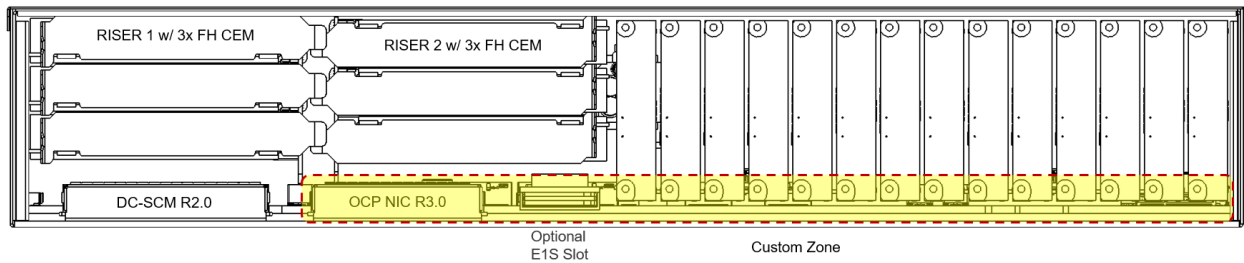


Figure 91: Class D Example – 2OU with 6 FH AICs and 14 E3.S



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14.1.4 Multi-Node Specific

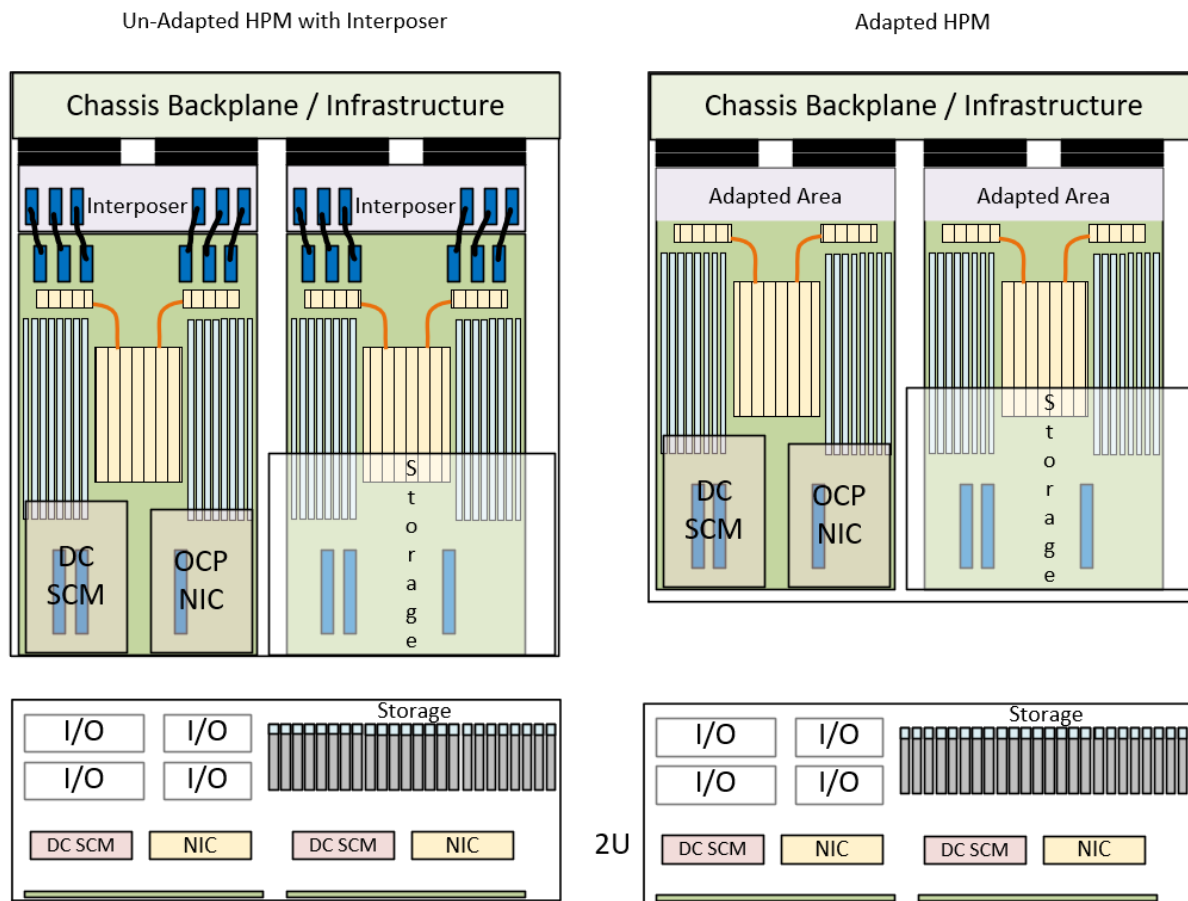
Multi-Node Adaptation

As described in the Power Zone **Section 11.1 HPM Power Zone Overview**, multi-node HPMs may choose to adapt the HPM to add board to board connectors on the Far board edge intended to directly mate into chassis power infrastructure (mid-plane, PDB, bus bar etc.).

Un-adapted HPMs can also be leveraged with this type of chassis infrastructure by leveraging an interposer board between the HPM and the chassis infrastructure.

The example below depicts using an un-adapted HPM on the left and an adapted HPM on the right in a similar system. For this example, shown is a Class A node opting to “float” the DC-SCM and NIC cards as opposed to placing them Co-Planar. Additionally, a 21” chassis is depicted.

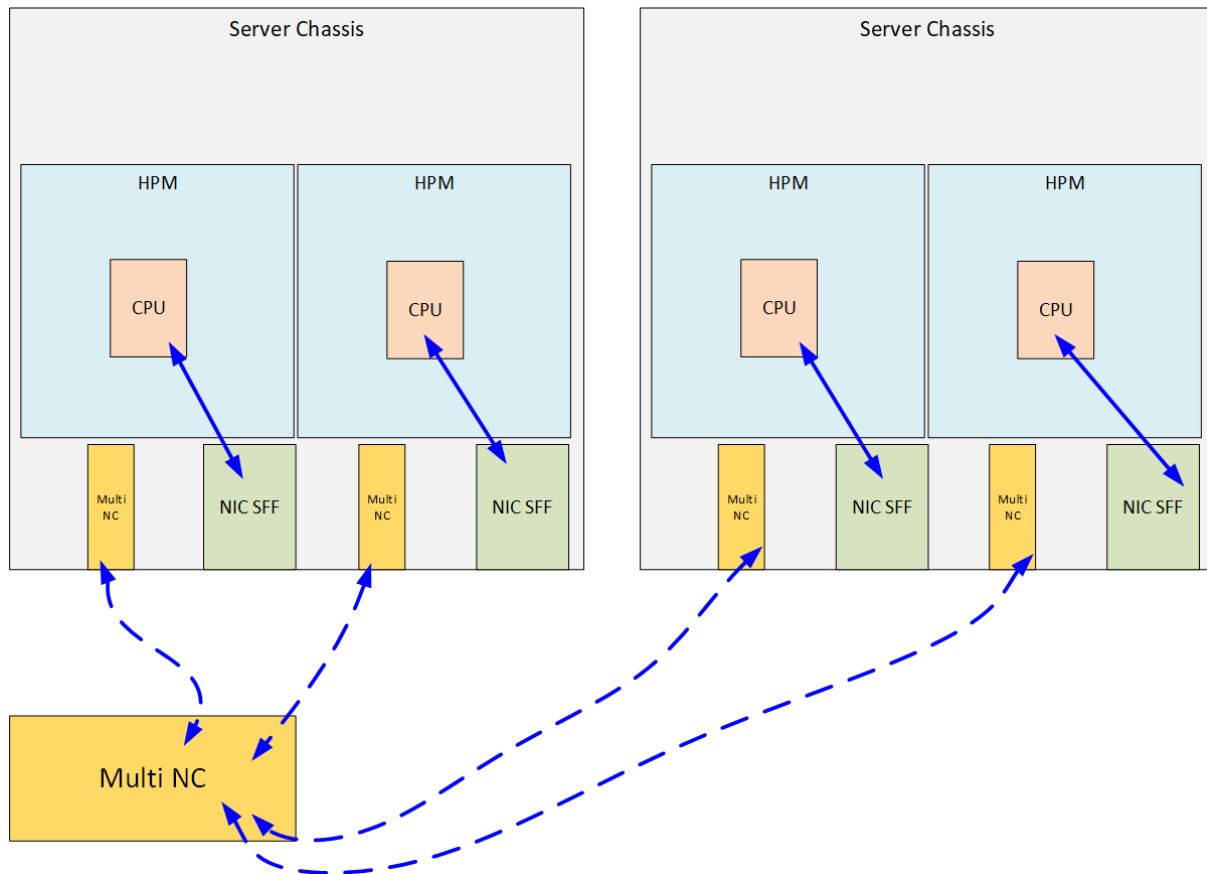
Figure 92: Multi-Node Adaptation Example



Multi-Node Management

How to deploy a multi-node management infrastructure using base specification compliant HPMs is outside of the scope of this specification. However, various common methodologies were evaluated to ensure that M-SDNO compliant HPMs could be leveraged into these infrastructures. As an example, a small low-cost local node controller could be connected to the DC-SCM 4C+ connector and then connected to a chassis manager or multi-node controller.

Figure 93: Multi-Node Management Example



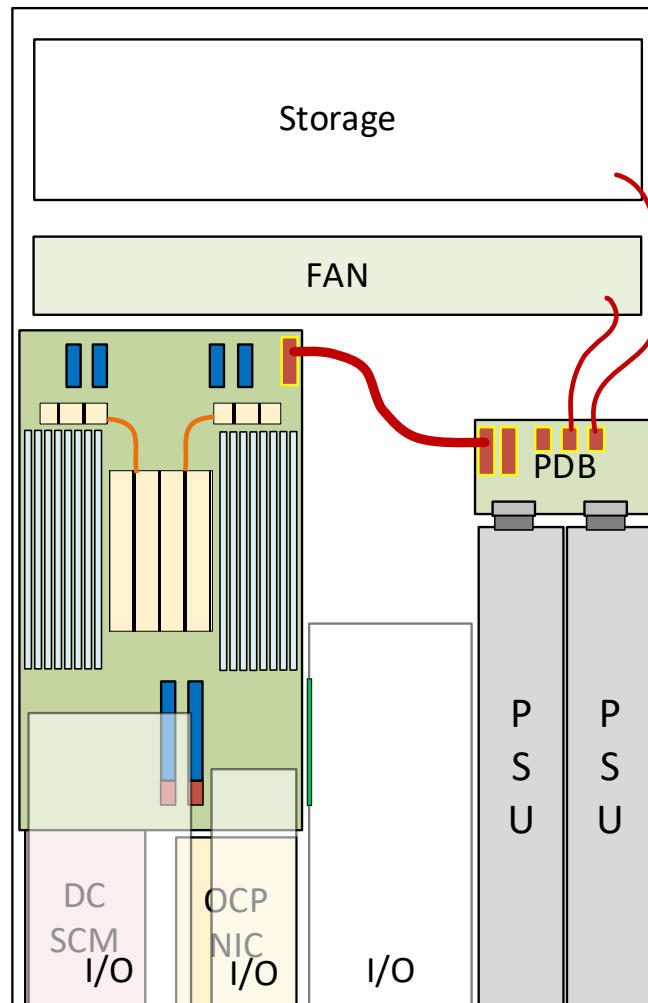
1700 14.2 M-SDNO Power Zone Usage Examples

The M-SDNO specification provides some flexibility to HPM implementors and system designers when it comes to Power Zone Usage. In this section, demonstration of some expected configurations leveraging these various options are conveyed. For simplicity's sake, the different power flows are demonstrated using the same Class A HPM board, however the power zone use case flexibility is similar across all Classes.

The first example listed below shows a simple monolithic (one HPM) system where PSUs feed power to the system PDB, the HPM power zones are utilized in the minimum required model:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: None

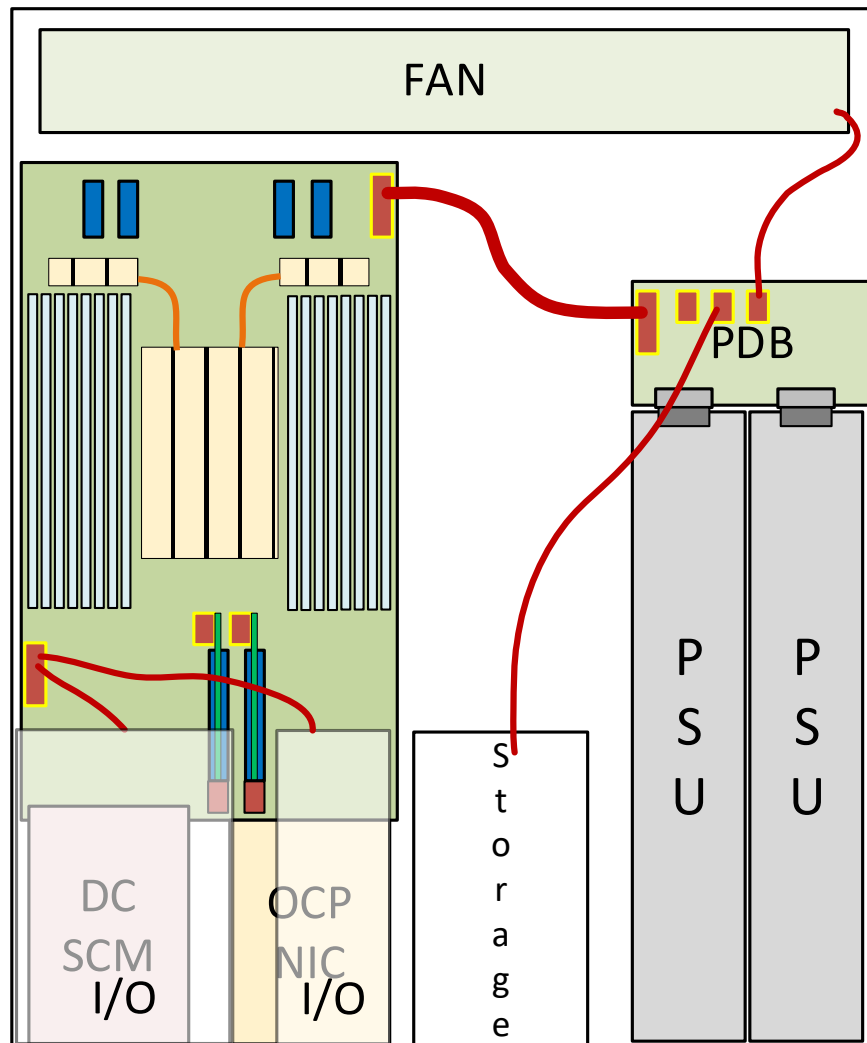
Figure 94: Power Zone Example 1: Monolithic Basic One Zone Ingress



1715 In the second example below, a monolithic (one HPM) system where PSUs feed power to the
 1720 system PDB is shown. However, in this example, the optional Near Side power zone is
 1725 leveraged:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: Supplemental power cable to CEM card aux (Note that the PICPWR definition requires an active cable to power gate these cables)
- Supplemental Power to I/O: From Near Zone (These cables could also be sourced from the PDB directly and would not require an active cable to power gate as control logic could be based on the PDB.)
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which leverage the far side for ingress power

Figure 95: Power Zone Example 2: Monolithic Leveraging Both Zones

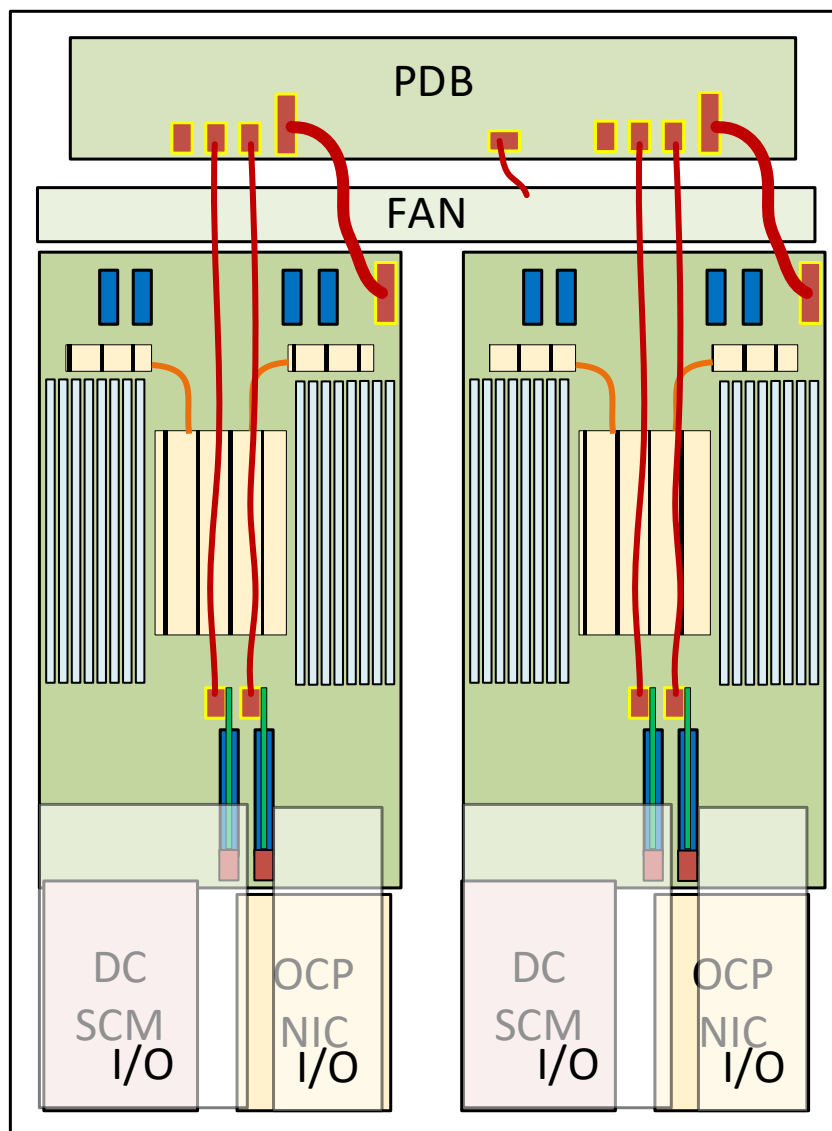


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The third example below illustrates a multi-node (>1 HPM) system with a Far Side PDB that could be supplied via PSUs, system level bus bars, or even rack level power distribution.

- Far Side Ingress: Power from PDB to HPM (while these connections are depicted with cables the HPM could also be adapted to support a board-to-board connector to chassis power infrastructure like a PDB as noted in **Section 11.1 HPM Power Zone Overview**)
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: From the PDB directly (does not require a “puck” as control logic could be based on the PDB)

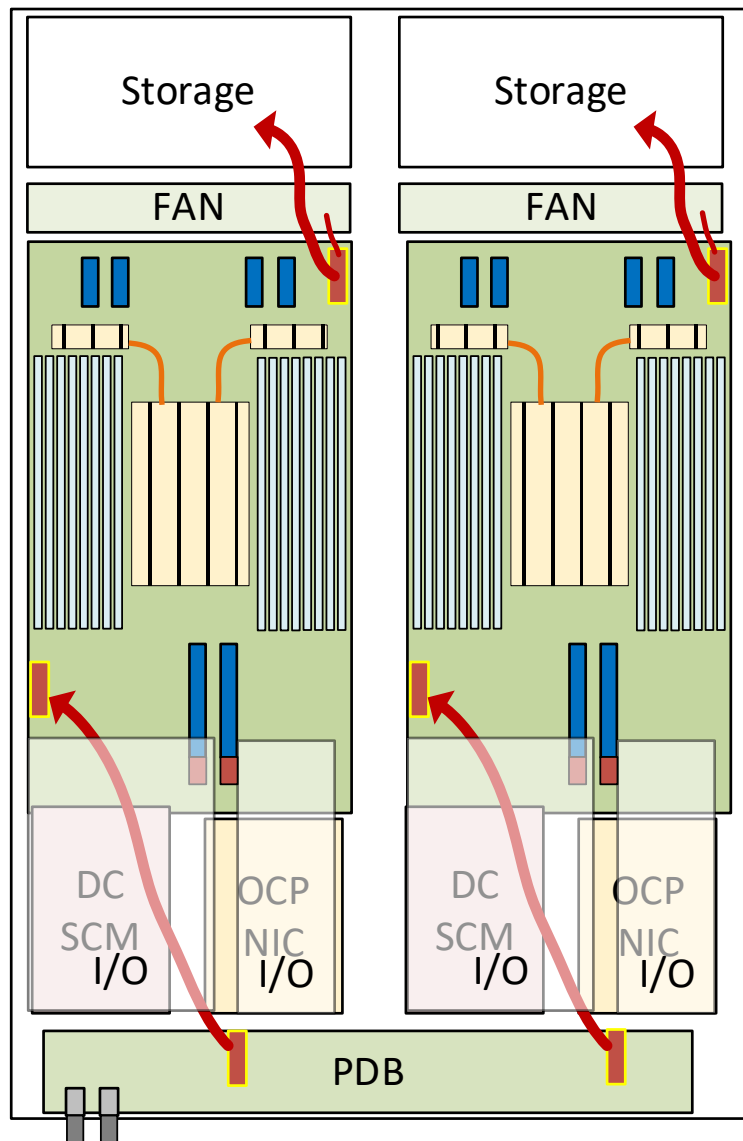
Figure 96: Power Zone Example 3: Multi-node with Far Side PDB



The fourth example below demonstrates a multi-node (>1 HPM) system with a Near Side PDB that could be supplied via PSUs, system level bus bars or even rack level power distribution.

- Far Side Ingress: None
- Far Side Egress: Used to power Storage peripheral subsystem,
- Near Side Ingress: Power from PDB to HPM (cabled)
- Near Side Egress: None
- Supplemental Power to I/O: None
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which use to leverage the far side for ingress power

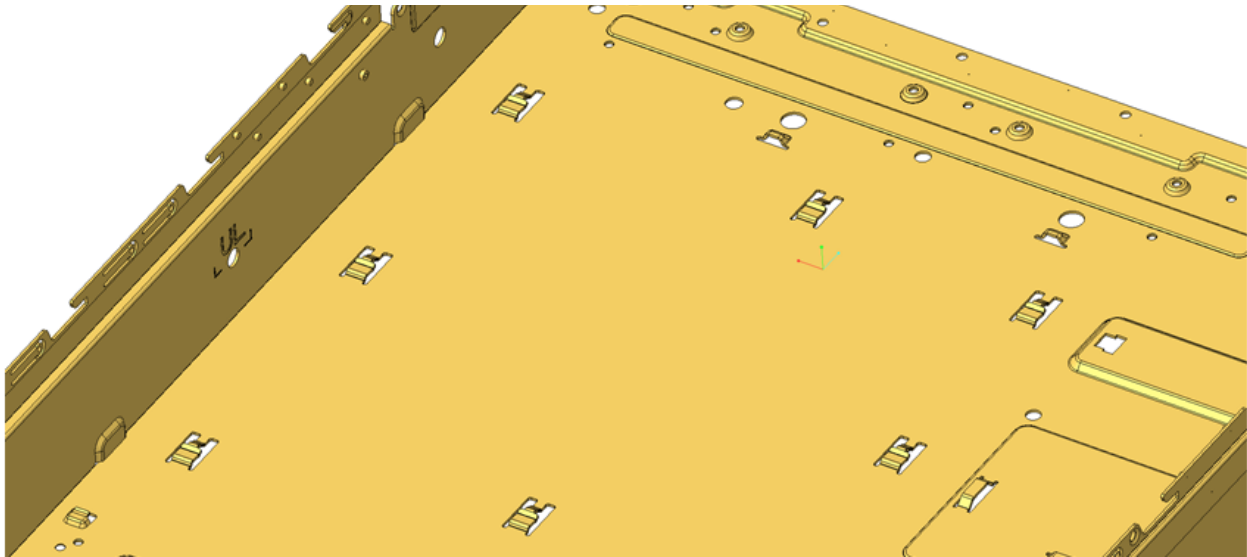
Figure 97: Power Zone Example 4 : Multi-node with Near Side PDB



14.3 Example Chassis Base Geometry for Chassis-to-Board Bracket interface

Below is an example geometry required in the chassis base to interface to the Chassis-to-HPM bracketry in **Figure 28: Example of Chassis-to-Board Bracket (Board Pan)**. The exact geometry is not specified, but considerations must be made for maximum board thickness (see **Section 10.4 HPM Board and Assembly Thickness**) and HPM Keepout Zone sizes (See **Section 10.3 Secondary Side Zones and Height Restrictions**)

Figure 98: Example Chassis Base Geometry for Board Bracket Interface



14.4 M-DNO and M-SDNO 305.59mm HPM Compatibility

M-DNO R1.1 defines the following HPM “Types”

- 1770
 - Type 2: 19" ½ Width 210 x 305.59mm
 - Type 3: 19" ½ Width 210 x 555.59mm
 - Type 4: 19 ¾ Width 295 x 305.59mm

This section will focus on compatibility of 305.59mm HPMs DNO T2/T4 and SDNO A305 / B305.

The vast majority of the HPM features and compliance requirements are common between M-DNO and M-SDNO, including:

- 1775
 - ½ Width HPM Outline (Common with Class A)
 - ½ Width HPM Hole Locations (Common with Class A)
 - Hole sizes, pads and KOZs
 - Secondary side component height restrictions
 - HPM secondary side support requirements
- 1780
 - CPU backing plate and HPM thickness limitations
 - HPM to chassis retention mounting location, sizes and KOZs
 - HPM Handle hole requirements
 - DC-SCM and OCP NIC location
 - M-PIC connector (USB, Control Panel, Storage, etc....) locations
- 1785
 - Near and far side cabled I/O connectors
 - Fixed riser positions, retention holes and connectors
 - Primary side component height restrictions
 - Power Zones
 - I/O System requirements

1790 There are two key differences between M-DNO and M-SDNO

1. M-SDNO does not define HPMs for 19" ¾ width 295mm (i.e. Type 4), instead it defines Class B which is essentially identical except 45mm less width and options for the platform custom zone are more limited.
- 1795 2. The “Zone 2” Chassis to HPM Bracket component KOZ locations have changed to enable more space for centrally placed CPUs/Memory. The A/B/C and A/B/D compatibility was not part of the M-DNO Scope. See **Figure 3: HPM Class Interoperability Goals**

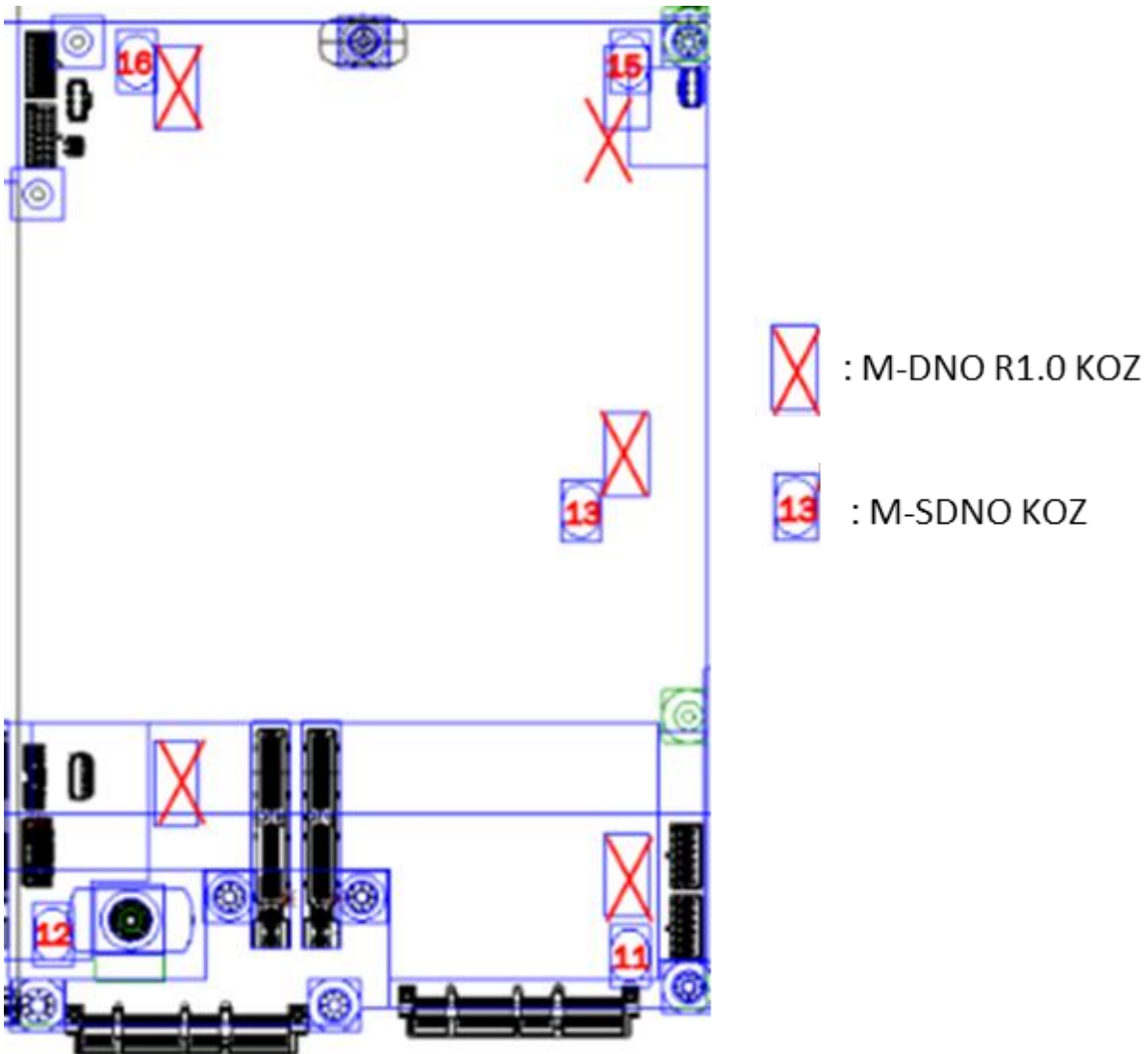
1800

14.4.1 Implications for HPM Designers

While otherwise interoperable, the Zone 2 change (#2 above) means that a chassis designed for M-DNO will have (SECONDARY SIDE) board pan interface features in different locations than a chassis designed to M-SDNO.

- 1805 Designers of A305 or B305 M-SDNO HPMS can enable the HPM to be used in both M-DNO chassis and M-SDNO chassis if they implement a superset of the Type 2 “Zone 2” (SECONDARY SIDE) KOZs from M-DNO and the Class A/B “Zone 2” (SECONDARY SIDE) KOZs detailed in this M-SDNO base specification. An example is shown in **Figure 99**.

Figure 99: Supetset KOZ M-DNO T2 + M-SDNO Class A (SECONDARY SIDE)



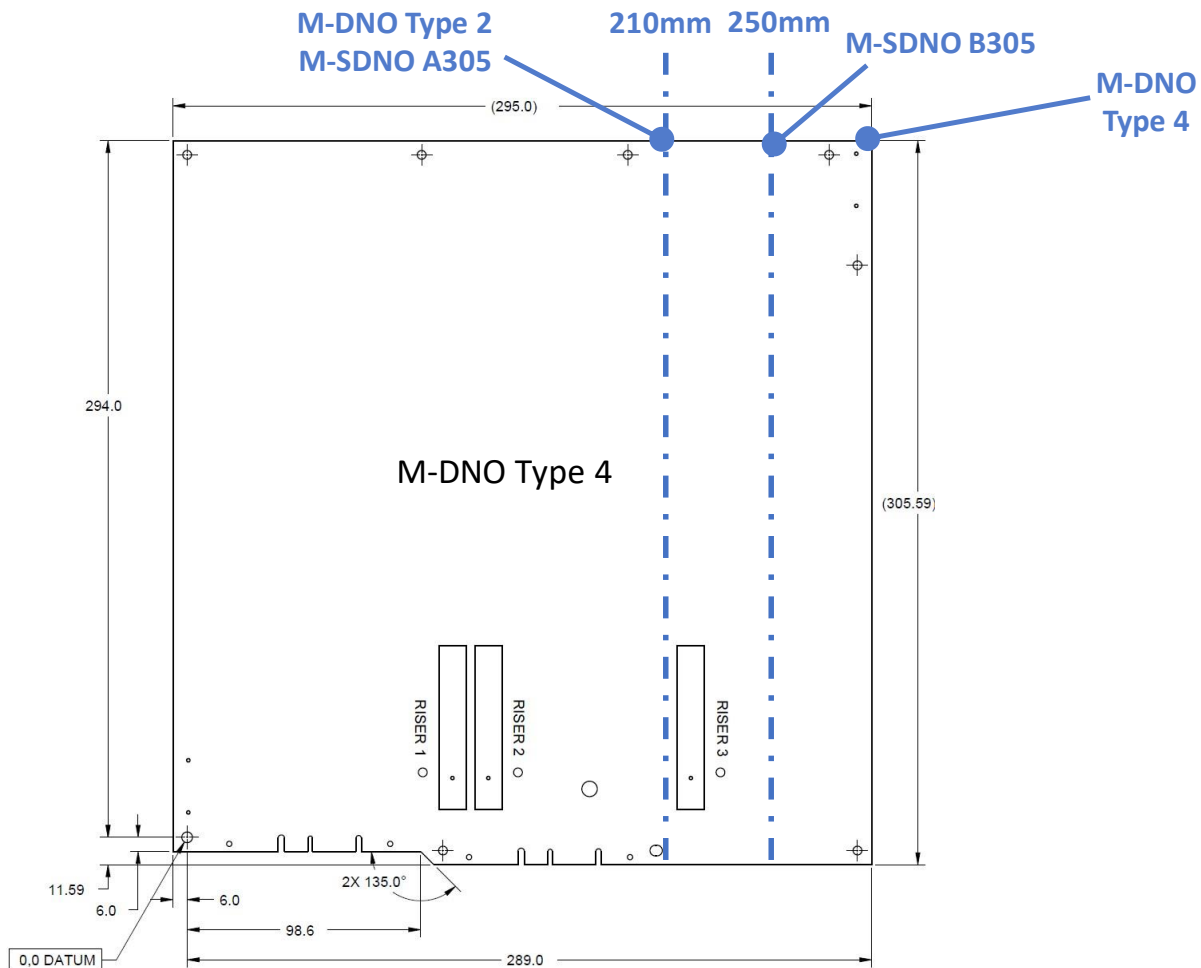
14.4.2 Implications for System Designers

As described above in #2, the fundamental difference for System designs is which locations are used for interfacing the board pan to the chassis base. A given chassis assembly will need to either implement M-DNO R1.0 locations or M-SDNO R1.0 locations.

Enablement of a chassis BOM population option for either M-DNO or M-SDNO locations is possible using installable self-clinching standoffs, sometimes referred to as “T-Pins”.

Otherwise, all chassis interfacing features (Risers, DC-SCM, OCP NIC, cabled connector locations, ...) are consistent for M-DNO T2, M-DNO T4, M-SDNO A305 and M-SDNO B305, and a system could support all four HPM varieties. **Figure 100** depicts all four 305.59mm HPMS overlayed for reference.

Figure 100: M-DNO and M-SDNO 305.59mm HPMS (PRIMARY SIDE)



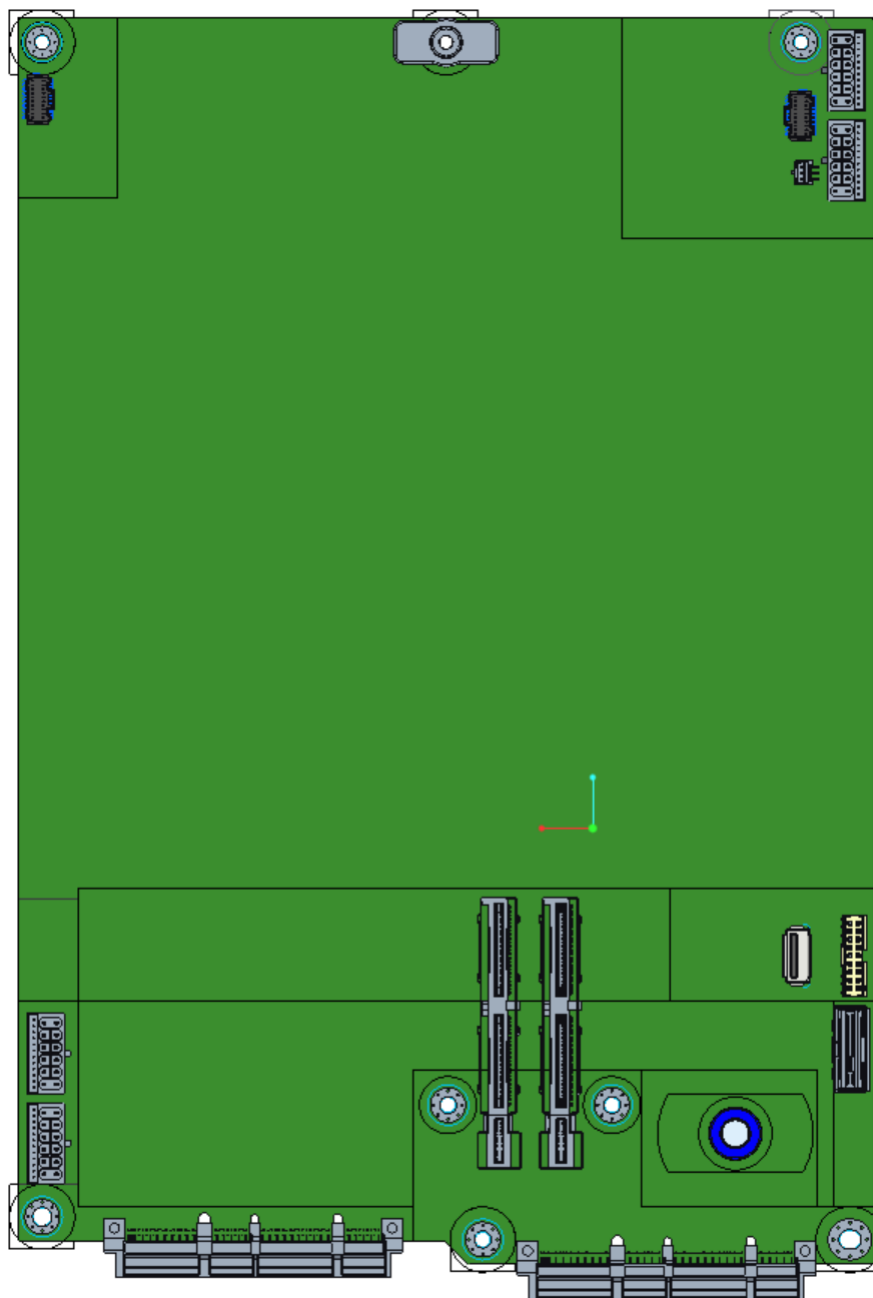
14.5 M-SDNO CAD Files

M-SDNO CAD files are available at the following link:

https://drive.google.com/drive/folders/11m9Oday1BqK38J_tu4vqC9FyJk5WDEvM

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Figure 101: CAD Snapshot (A305 Example PRIMARY SIDE)



1835 **14.6 Future Material**

- 48V Power Enablement
- M-SIF Enablement
- Alternate Board to Board Far Side Power Ingress Option