



OPEN
Compute Project

Platform Infrastructure Connectivity (M-PIC) Base Specification

Part of the
Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family
Version 1.11
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1.2. Acknowledgements

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback of various individuals and companies that participated in DC-MHS.

2. Version Table

Date	Version #	Description
April 22 nd 2022	0.70	Initial public release.
June 8 th 2022	0.71	- Added a note about PICPWR signal naming and updated document for consistency in section 10.1.2. - Added notes to allow fusing to protect connectors, cables, and traces and requiring back-feed prevention on modules docking into M-CRPS connectors in section 10.1.4. and section 10.1.5. - Added clarification and guidance allowing peripherals to consume initial power in section 10.1.6. - Added a note about PESTI and recommended usages for PICPWR_A/B_SB1 and PICPWR_A/B_SB4 in <i>Table 2</i>, <i>Table 23</i>, and <i>Table 25</i>. - Added ratings for power connectors in section 10.1.6. - Added a power only riser connector and pinout in section 10.1.7.5. - Updated the connector in section 10.1.7.6. from 12S to 16S to include analog signals, and +12VStby pins. - Removed "Analog" and prepared for the new connector with +12VStby and PDB management signals in section 10.2.14. - Updated the Internal USB connector to recommend type A but allow type C in section 11.3. - Added a note to <i>Table 23</i> and <i>Table 25</i> recommending overcurrent protection for 12V_CP be added. - Updated control panel pin numbering in <i>Table 24</i> and <i>Table 26</i>. - Referred to M-XIO for USB2 usage Smart NIC interface in section 11.6. - Added Imon and Vmon signaling requirements in section 12. - Added physical connector pin numbering figures for multiple connectors.

June 14 th 2022	0.72	• Added a note about PESTI giving recommended usages for PICPWR_A/B_SB1 and PICPWR_A/B_SB4 missed in V0.71 for <i>Table 25</i>. • Updated control panel USB connectivity in <i>Figure 50</i>, <i>Table 23</i>, and <i>Table 25</i>. • Added a requirement for silkscreen labeling for PICPWR sideband channel positions in section 10.1.2. • Updated part numbers in sections 10.1.7.1, 10.1.7.2, and 10.1.7.5 • Updated <i>Figure 1</i> to use the near side riser connector. • Updated the SPI signaling voltage requirement note. • Updated <i>Figure 7</i>, and <i>Figure 23</i> to show +12VStby. • Updated to use “shall” for consistency. • Added section 12.3 for PMBus and section 12.6 for SGPIO. • Added trademark information for PMBus.
June 16 th 2022	0.73	• Corrected PESTI note from PICPWR_A/B in <i>Table 23</i> and <i>Table 25</i> for PCP and SCP. • Updated <i>Figure 21</i> PCIe AUX Signals. • Updated sections 10.1.8.3 and 10.2.14. defining the PDB management connector. • Added AMD in section 1.1.
June 17 th 2022	0.74	• Updated from AMD to use the official legal name. • Updated PDB management connector to allow for different packaging, different tail lengths, and use the plug that provides a mated height of 8 mm.
June 24 th 2022	0.75	• Aligned PDB and PIB terms with definitions in <i>Table 1</i>. • 2nd public release
August 23 2022	0.90	• General cleanup • Added a specification compliance table in section 4. • Simplified the definition of 12V_PRIMARY and figures in section 10.1. • Updated PDB management connector and near riser P/N(s). • Updated PICPWR, PCP, and SCP SB definitions. • Updated boot storage in section 11.1. • Removed 48V content for v0.9 • Updated SGPIO definition • Added 2x3+6SB 12V PICPWR connectors. • Updated 2x6+12SB channel definition to match <i>Figure 1</i>. • Specified contact plating for 2x6+12SB and 2x3+6SB headers. • Updated contributor list, grammatical errors • Moved “12V 3+16S+3 PICPWR Blind-mate right-angle Connector Pinout” to Supplemental backup section per core team agreements. • Added SFF-TA-1033 term to the PICPWR variant associated with the data combo connector defined in M-XIO and SNIA.

		• Section 1.2 Added some companies that assisted with connector investigations. • Updated section 11.1.1 with connector rendering and FLEX pin definition. • Removed connector P/Ns with pointers to main XLS. Removed the blind mate 3+16+3 from main body since it was duplicated with the agreed supplemental until >1.0. • Fixed PICPWR 3+16+3 back into main body and clarified that supplemental section is a placeholder for 48V and UBB 2.0 related investigations.
September 27, 2022	1.0 RC6	• Accepted prior release changes for a new baseline. • Updated Boot connector footprint image in <i>Figure 47</i>. • Updated Boot Connector Rendering in <i>Figure 45</i>. • Replaced PSU with M-CRPS • Moved figures closer to Figure references. • Removed Vendor markings throughout. • Clarified 12V management power switch output in section 10.1.4, and CP power • Added CP into power diagrams showing Management subsystems. • Changed boards to peripherals in section 8. • Added an image for <i>Figure 15</i>. • Clarified connector versions in section 10.1.7.5 and updated current per pin to match the datasheet. • Updated <i>Table 8</i> pinout and format aligned with M-XIO. • Removed requirement to prevent 12V and 48V mixing from sections 10.1.4 and 10.1.5 because M-CRPS is keyed. • Moved TPM to section 5.1 as out of scope. • Added the signal name to section 11.2 item 4. • Updated Section 11.3 to allow the USB3 source on HPM or DC-SCM. • Clarified section 11.4 SB[4:1] requirements. • Updated section 11.6 to align with M-XIO USB2 updates. • Added an implementation note in <i>Table 2</i> and <i>Figure 8</i> for maximum voltage drop on HPM to PICPWR Egress. • Updated section 1.2 to match DC-SCM format. • Added additional terms, alphabetized <i>Table 1</i>, and removed duplicate definitions. • Clarified the scope in section 10.2.14 • Updated section 11.1.1, <i>Table 22</i>, and <i>Figure 45</i> names to be consistent. • Updated section 11.1.1 connector current rating. • Updated section 13 to correct DC-MHS Rev to 1.0 • Deleted Appendix A and Appendix B since they do not apply to DC-MHS base specifications.

		• Updated section 1.2 to have a format like DC-SCM. • Updated CP USB2 to be optional and only require USB High Speed in <i>Table 23</i> and <i>Table 25</i>. • Added a description and changed the title for the section 4. • Defined 3.3Vaux in <i>Table 3</i> and updated <i>Figure 9</i>. • Clarified control panel discrete signal bias rule. • Changed SCP SB[4:3] to optional. • Updated formatting for consistency and grammar throughout. • Replaced hyperlink text throughout with “DC-MHS Connector Information” hyperlinks and added a reference with the text in section 13. • Corrected de-assertion to assertion in <i>Table 3</i> and <i>Figure 9</i>. • Updated “is” to “shall be” in section 11.4. • Updated capitalization and grammar to be consistent throughout. • Removed “strongly” from the USB3 connector in section 11.3. • Clarified the description of USB3 cabling to CP(s) in section 11.4. • Removed UBB2.0 note from the future material section since the M-PIC portion is already in the main spec. • Changed the future material section name to align with the description of the section. • Clarified section 10.1.3. • Updated DC-MHS connector information link in section 13. • Removed module reference from boot storage in section 5. • Clarified the peripheral sideband requirement in section 10.1.6. • Clarified section 11.1 to cover all 3 boot storage options. • Defined 3p3_AUX_MGMT in <i>Table 21</i>. • Clarified 12V_PRIMARY “sourced” in sections 10.1.4, section 10.1.5, and <i>Table 2</i>. • Moved the DC-MHS Family of Specifications to a new section (section 6) after overview to improve continuity. • Updated section 10.3 to reference DC-SCM requirements. • Corrected SB1 and SB2 in <i>Table 8</i>. • Moved pin definitions for PCP into section 11.4.1 and SCP into sections 11.4.2. • Clarified 12V boot power management note in section 11.1.1. • Clarified SPI speed in <i>Table 23</i>. • Updated Release dates for 1.0 RC6.
October 28, 2022	1.0 RC7	• Clarified +3.3Vaux. • Corrected typographic errors. • Updated connector list hyperlink text.
February 2, 2023	1.01	• Updated document outline to move “IO” and “Electrical” sections out of the “Power Delivery” section. • Added PDB presence detection and SDataIn termination in section 12.6.1 • Updated <i>Table 9</i> and <i>Figure 20</i> titles.

		• Address V1.0 RC7 Errata #1 - Update section 10.1 to avoid high-current in partial-mate conditions. • Added clarification for PICPWR hot plug within section 10.1. • Added a link to the M-PIC reference material location in 13. • Address V1.0 RC7 Errata #2 - Updated connector power rating and current in section 10.1.7.6 from 1080W to 2000W
March 13, 2023	1.02	• Underlined compliance requirement text throughout. • Identified missing compliance requirements with “shall”. • Corrected typographic errors. • Clarified pinouts, pin definitions, and electrical requirements as compliance requirements. • Updated Specification Compliance Checklist and added a note in section 4. • Updated section 10.1.5 “OR-ing” note to cover any +12V power source. • Clarified the number of SB channels in section 10.1.7.6. • Added Jabil in section 1.1. and page 2.
September 28, 2023	1.03	• Updated <i>Table 21</i> power definition from 25W to 48W to match the connector power rating. • Updated section 11.1.2.2 from SFF-TA-1009 Rev 3.0 to 3.1. • Added Ampere Computing in section 1.1. and page 2. • Clarified current rating for the cable optimized boot connector in text and <i>Figure 46</i>. • Clarified section 3 to reference the specification compliance checklist. • Corrected typographic errors. • Documented the, previously implicit, requirement that all +12V sources have controlled ramps in sections 10.1.4 and 10.1.5. • Added SFF-TA-1036 number to section 11.1.1. • Updated PDB Management pin B09 from RFU to FULL_PWR_CYCLE_N/FLEXIO in section 10.2.14. • Updated section 11.1.1 to include an option to use PWRDIS to enable/disable power on the cable optimized boot peripheral. • Changed SB* topologies in <i>Table 3</i> and <i>Figure 9</i> from 127kΩ to 100kΩ to improve signal DC margin. • Added M-SIF, M-SDNO, and a link to the Wiki in the Family of specifications in section 6. • Added I3C recommendations to section 12.2. • Replaced “12VHPWR” with “12V-2x6” and removed GPU from <i>Figure 8</i> and <i>Figure 21</i>. • Clarified SGPIO. • Removed the Future Material section since it is not applicable.
March 1, 2024	1.04	• Simplified section 3. • Addressed V1.03 Errata #1 - Updated FULL_PWR_CYCLE_N/FLEXIO to avoid power-up failures,

		moved pull-up circuit to be on PDB, changed pull-up to an equivalent value, and clarified signal type. • Added references to section 12 to applicable signals that reference 11.x to apply requirements early in section 12. • Updated PICPWR labeling requirements throughout. • Updated DC-SCM from 2.0 to 2.x to allow newer, backwards compatible versions and added underlined text in section 11.7 to match the requirement format. • Corrected typographic errors. • Added terms in section 7. • Updated section 11.7 to clarify the DC-SCM revision as a requirement. • Updated sections 10.1.4 and 10.1.5 “OR-ing” notes to include +12VStby sources. • Added a note for SPI use cases in <i>Table 23</i>. • Added cable construction expectations to PDB in section 10.2.14 and Control Panel in section 11.4. • Clarified the SFF-TA-1036 pinout as defined for HPM and added a note to draw attention to things that affect the far end mated cable assembly pinout.
May 17, 2024	1.05	• Clarified SB signals to be unique per channel instead of per connector. • Simplified peripheral input requirements in section 10.1.6.
September 27, 2024	1.06	• Updated <i>Table 2</i> format and added an implementation note for voltage tolerance. • Clarified SMBus PU to be on HPM in Section 12.2. • Added FLEXIO to section 12.1. • Clarified FLEXIO bias and destination requirements in <i>Table 21</i>. • Corrected the outline flow in section 11.1.1. • Removed extra text from the 12V_CP description in <i>Table 14</i> and <i>Table 16</i>. • Updated hyperlinks. • General cleanup.
December 12, 2024	1.1	• Merged the 48V addendum v0.9 content to add 48V support. • Clarified 12V PICPWR connectivity in section 10.1.5, section 10.1.6 and <i>Figure 21</i>. • Changed SMBus pull-ups from 100kΩ to R_{PU} for <i>Figure 9</i>. • Clarified SGPIO waveform bit ordering in <i>Figure 52</i>. • Added HPM and peripheral requirements for configurations with more than one 12V_PRIMARY domain. • Clarified 48V PICPWR connectivity in section 10.2.11. • General cleanup.
March 3, 2025	1.11	• Updated <i>Table 7</i> and <i>Table 16</i> names to match the connector configuration.

		• Updated Dedicated 48V Supply connector naming for consistency.
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3. Scope

This document defines technical specifications for the Platform Infrastructure Connectivity Base Specification used in the Open Compute Project, Data Center, Modular Hardware System.

Any supplier seeking OCP recognition for a hardware product based on this spec shall be 100% compliant with all features or requirements listed in section 4 of this specification.

3.1. Typical OCP Sections Not Applicable

This is a base specification, requiring other MHS specifications to fully define a design. The following typical sections of an OCP specification are not included because they are not applicable to this specification.

- Physical Spec
- Rear Side Power, I/O, Expansion
- Mechanical
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management
- Security

4. Specification Compliance Checklist

The following table is intended to summarize the list of attributes and requirements for a design to be DC-MHS M-PIC Base Specification compliant. Compliance requirements throughout this document can be identified by underlined text including the word “shall”.

#	Technical Specification	Document Reference
1	For each 12V and 48V PICPWR connector, minimum requirements shall be implemented.	Sections 10.1.1 and 10.2.3
2	For each PICPWR connector, labeling requirements shall be implemented.	Sections 10.1.2 and 10.2.4
3	If a 12V HPM supports M-CRPS or power subsystem with 12V output directly docking into the HPM, HPM power distribution architecture requirements shall be Implemented	Section 10.1.4
4	If a 12V HPM supports remote M-CRPS or power subsystems (PDB) with 12V output, HPM power distribution architecture requirements shall be implemented.	Section 10.1.5
5	12V PICPWR peripheral power distribution architecture requirements shall be implemented.	Section 10.1.6
6	12V PICPWR connector pin definitions, electrical requirements, and topologies shall be implemented.	Section 10.1.7
7	12V PICPWR parts specified (or equivalent) and pinouts shall be implemented.	Sections 10.1.7.1 thru 10.1.7.6 .
8	If an HPM supports remote M-CRPS or power subsystems (PDB) and uses PICPWR connectors to supplement PDB management, PDB Management Connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 10.2.14.1
9	For reach dedicated 48V supply connector, requirements shall be implemented.	Section 10.2.1
10	For each dedicated 48V supply connector, labeling requirements shall be implemented.	Section 10.2.2
11	If a 12V HPM is used with 48V rack remote power distribution architecture, requirements shall be implemented.	Section 10.2.5
12	If a 12V HPM is used with a 48V M-CRPS remote power distribution architecture, requirements shall be implemented.	Section 10.2.6
13	If a 12V HPM is used with 48V rack M-SIF remote power distribution architecture, requirements shall be implemented.	Section 10.2.7
14	If a 48V HPM is used with 48V rack remote power distribution architecture, requirements shall be implemented.	Section 10.2.8
15	If a 48V HPM is used with a 48V M-CRPS remote power distribution architecture, requirements shall be implemented.	Section 10.2.9
16	If a 48V HPM is used with 48V rack M-SIF remote power distribution architecture, requirements shall be implemented.	Section 10.2.10
17	48V PICPWR peripheral power distribution architecture requirements shall be implemented.	Section 10.2.11

18	If implementing 48V, dedicated 48V supply connector pin definitions, electrical requirements, and topologies shall be implemented.	Section 10.2.12
19	If implementing 48V, dedicated 48V supply parts specified (or equivalent) and pinouts shall be implemented.	Section 10.2.12.1
20	For 48V PICPWR, connector pin definitions, electrical requirements, and topologies shall be implemented.	Section 10.2.13
21	For 48V PICPWR, parts specified (or equivalent) and pinouts shall be implemented.	Sections 10.2.13.1 thru 10.2.13.4
22	If an HPM supports remote M-CRPS or power subsystems (PDB) but does not use PICPWR connectors to supplement PDB management, PDB Management Connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 10.2.14.2
23	Coin cell battery requirements shall be implemented.	Section 10.3
24	If a cable optimized boot storage subsystem is implemented, the required connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 11.1.1
25	If a direct dock boot storage subsystem is implemented, the requirements for M.2 or E1.S connector type and pinout shall be implemented.	Sections 11.1.2.1 and 11.1.2.2
26	Intrusion header part (or equivalent), pin definitions, connectivity, electrical requirements, and pinout shall be implemented.	Section 11.2
27	If the form factor specification for the form factor selected specifies an internal USB connector, internal USB connector generation and type requirements shall be implemented.	Section 11.3
28	Control panel connector naming (primary vs secondary), connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 11.4
29	DC-SCM 2.x shall be implemented.	Section 11.7
30	Electrical requirements shall be implemented.	Section 12

5. Overview

This specification defines and standardizes common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems within the DC-MHS 1.0 family of OCP servers. Standardization of the common interfaces and connectors enables hardware compatibility between DC-MHS HPMs and various DC-MHS system components.

The standardized common elements defined in this specification can be utilized by DC-MHS form factor specifications and/or DC-MHS peripherals. The elements defined within this specification are not inherently required with a DC-MHS form factor. The form factor specifications call out which of these elements are required or optional, the physical placement, and any additional details specific to that form factor.

This specification defines connectors, signals, and electrical interface requirements to enable connectivity and hardware compatibility to the following types of platform/chassis infrastructure:

1. Cooling infrastructure including:
 - a. **Cooling modules** with one or more intelligent fan controllers, interfaced to air movers.
 - b. Monitoring and control of **liquid-cooling infrastructure**, handled as intelligent cooling modules.
2. **Power distribution/management:** Connectors for input power from source or PDB (power distribution board) and connectors to output power to peripheral subsystems.
3. **Boot storage:** subsystem that provides minimal storage for a hyper-visor or OS, typically using USB or 1 to 4 lanes of PCIe, typically a monolithic storage device or a controller with RAID1 using two media devices.
4. **Intrusion switch** to detect physical access to the internals of a platform.
5. **Internal Host USB** for Internal Key functions, debug, or as an additional source for control panel USB.
6. **Control panels** for human interaction beyond what is offered on DC-SCM. This includes options for indirect support for buttons, LEDs, more complex displays, and external peripheral ports like USB.
7. **Smart NIC Management Interface:** for Smart NICs connected via M-XIO.
8. **Coin Cell Battery** to supply battery back-up power for features like RTC.
9. **DC-SCM** – Data Center Secure Control Module Revision 2.x is used with DC-MHS.

5.1. Items Not Included

- Designs or specific implementation requirements on platform infrastructure including those referenced above.
- Elements specified by DC-SCM
- Elements specified by DC-MHS XIO Specifications
- Elements supporting rack-level infrastructure
- NVMe Hot plug: attention and LEDs
- Edge/Telco: time-sync requirements
- TPM: location and connectivity

6. DC-MHS Family of Specifications

The Data Center – Modular Hardware System (DC-MHS) Rev 1.0 family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-CRPS (Modular Hardware System Common Redundant Power Supply Specification)** – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-DNO (Modular Hardware System Partial Width DeNsity Optimized Specification)** – Host Processor Module (HPM) specification targeted to partial width (i.e., $\frac{1}{2}$ width or $\frac{3}{4}$ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.

- **M-FLW (Modular Hardware System Full Width Specification)** – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-PESTI (Modular Hardware System Peripheral Sideband Tunneling Interface)** – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (i.e., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- **M-PIC (Modular Hardware System Platform Infrastructure Connectivity Specification)** – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-SDNO (Modular Hardware System Scalable DeNsity Optimized Specification)** – Builds upon M-DNO, defines partial and full width HPMs with variable board outlines covering 19” EIA-310 and 21” Open Rack v3 infrastructure.
- **M-SIF (Modular Hardware System Shared Infrastructure Specification)** – Specifies data and management plane interfaces along with power and cooling connections that are expected to be present within a modular platform utilizing shared elements.
- **M-XIO (Modular Hardware System Extensible I/O)** – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.

To access additional DC-MHS specification please visit the OCP, Server, [MHS Wiki](#).

7. Terminology

Table 1: Terminology

Standardized Term	Meaning	Alternative Terms
+12V	12V Main Power from CRPS	
+12VStby	12V Standby from CRPS	
48V	48V Power Source (typically ranges from 40 up to 60V)	54V, 51V
ACPI	Advanced Configuration and Power Interface	
CEM	Card Electromechanical specification	
DC-MHS	Data center - Modular Hardware System	
DC-SCM	Data Center - Secure Control Module	
FPGA	Field-Programable Gate Array	
HPM	Host Processor Module PCB or PCBA form factor defined in M-FLW or M-DNO	
IT Gear	The sum of all the components powered from a busbar clip.	
M-CRPS	Modular Hardware System Common Redundant Power Supply	PSU, CRPS
MCU	A microcontroller unit	uC
M-DNO	Modular Hardware System Partial Width DeNsity Optimized HPM Form Factor	DNO
M-FLW	Modular Hardware System Full Width HPM Form Factor	FLW
M-PESTI	Modular Hardware System PEripheral Sideband Tunneling Interface	PESTI
M-SDNO	Modular Hardware System Scalable DeNsity Optimized HPM Form factor	SDNO
M-SIF	Modular Hardware System Shared InFrastructure	SIF
MGMT	management	
M-XIO	Modular Hardware System eXtensible I/O	XIO
ORv3	Open Rack Base Specification version 3.0	
ORv2	Open Rack Standard version 2.x	
PCB	Printed Circuit Board	
PCBA	Printed Circuit Board Assembly	PBA
PCP	Primary Control Panel	CP
PDB	Power Distribution Board	
PIB	Power Interface Board	
PICPWR	Platform Infrastructure Connectivity Power distribution connector	
PMBus	Power Management Bus	PMB
SCP	Secondary Control Panel	CP
RFU	Reserved for Future Use	
SGPIO	Serial GPIO	
Smart NIC	A programmable Network Interface Card used to improve data center networking performance, security, features, and flexibility.	IPU or DPU
TDP	Thermal Design Point	
Power Sense	A voltage signal for power connectivity loss detection, power control, and consumption monitoring provided by the 48V supply connector.	Short Pin (ORv2)
Ground Return Sense	An ORv3 return channel for the sense signal that may be used for ground connectively loss detection and consumption monitoring provided by the 48V supply connector.	

8. Thermal Design

Systems have variable cooling requirements ranging from air movers to liquid cooling or hybrid solutions. This section describes the power and management interface for cooling systems which play a vital role in the overall thermal solution. The HPM interface covered for cooling addresses only cooling subsystems connected to HPM via separate cooling subsystem peripherals because the HPM formfactors standardized on off-HPM cooling solutions. The adoption of DC-SCM caused the change in air mover cooling system architecture from discrete fan controls via BMC to cooling system control over SMBus or I3C. The choice to use off HPM cooling solutions provides greater flexibility and applicability of an HPM to different platforms and cooling solutions. The method chosen for DC-MHS utilizes the managed power distribution connection (namely PICPWR) from the HPM or PDB for power and all remote cooling control management. The PICPWR connector includes an SMB/I3C interface and 4 additional sideband signals (per channel) that can be used to manage the cooling subsystem board. (See section 10.1 for the 12V PICPWR definition).

There is no intent to provide a dedicated remote cooling connector /interface definition.

In some cases, the cooling system may be managed and/or powered at a chassis or rack level so the HPM may play no role in the cooling system.

9. Rack Compatibility

This specification is compatible with the ORv2 and ORv3 specification busbar voltage ranges and connectivity when used in ORv2, ORv3, or other equivalent 48V output sources.

10. Power Delivery

10.1. 12V Power Distribution and Management

This section covers the minimum power distribution and management architecture requirements for a 12V HPM, and peripheral subsystems attached to the HPM. Example peripheral subsystems include, but not limited to, risers, backplanes, cooling, battery power, ingress from M-CRPS or higher-level power source (e.g., multimodal). The goal is for HPMs and PDBs to provide a homogeneous power + sideband interface for powering remote peripherals (like backplanes, risers, PCIe CEM AUX connections, etc.). This specification does not provide the necessary requirements to safely support hot plug functionality through 12V PICPWR connections. However, this specification does not preclude hot plug support using an implementation-specific method. Peripheral subsystems that do not require HPMs to supply or manage their ingress power source are outside the scope of this specification. If an HPM contains 12V PICPWR connectors, the use of those connectors is optional.

10.1.1. 12V PICPWR Power Connector Form Factor

Distribution of power within the HPM and to/from peripheral subsystems can be implemented in any connector form factor that meets minimum requirements:

- Connectors shall have power pins with equal capability for 12V PRIMARY power supply and return.
- Connectors shall have 6 sideband pins dedicated for power delivery management.
- Connector 12V PRIMARY and return circuits shall be 1st to mate and last to break.
- Connector dedicated sideband circuits shall be 2nd to mate and 1st to break.

Power connectors that meet the minimum requirements are referred to as 12V PICPWR connectors.

A 12V PICPWR connector can include an implementation that has additional function/signals (for example, high-speed IO) shared in a common connector housing. Additionally, a PICPWR connector can support multiple channels of sideband signals, where each channel shall contain the 6 sideband pins dedicated for power delivery management.

Figure 1 shows an example of a stand-alone 12V PICPWR connector as well as a 12V PICPWR implementation as part of a larger connector with additional functions/signals.

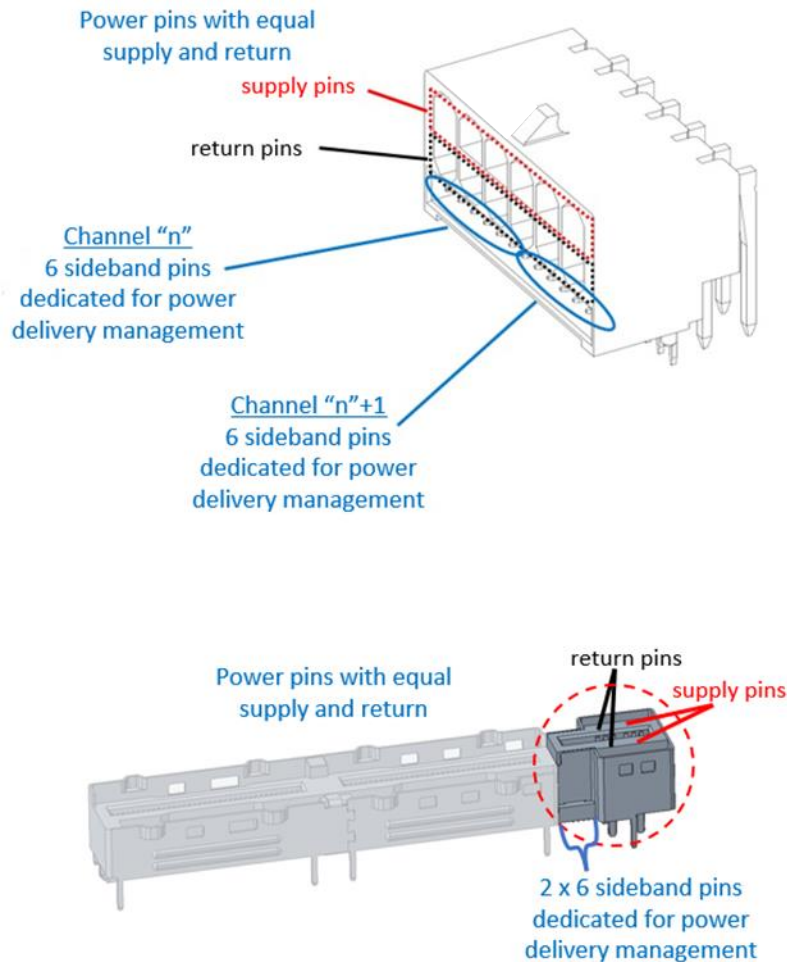


Figure 1: Examples of 12V PICPWR Connectors

10.1.2. 12V PICPWR Connector Power Labeling Requirements

This section defines clear, consistent, and short PICPWR connector naming strings to support various stakeholders including factory and field service as well as various firmware and software functions.

- Each PICPWR connector shall be identified by an all-capital character string that starts with “PWR n ”, where n is a unique decimal number for each PICPWR connector instantiation per board. It is recommended that the string be large, boxed, and bold. HPM PICPWR instances are recommended to start with 1.
- Any optional additional information provided shall be a suffix after the above string + underscore (e.g., PWR3 [More Optional Info]) so that it is simple for SW/FW to truncate the suffix if needed.
- To avoid confusion caused by duplicate names between HPM and PDB PICPWR instances, it is recommended to design PDBs with instance numbers that are higher than the maximum number of instances for various possible HPMs (e.g., If an HPM has PWR1 to PWR20, a PDB with 10 PICPWR instances that may couple to multiple HPM types may choose to number as PWR50 to PWR59).
- For PICPWR connectors that include two sideband channels (refer to *Figure 2* and *Figure 3*), it is recommended to add a 2nd unique string instance of the label described for the single channel connector. It is recommended that each string be located near each respective side. This avoids configuration complexities where each set of sideband signals and associated power related conductors may couple to different subsystems.

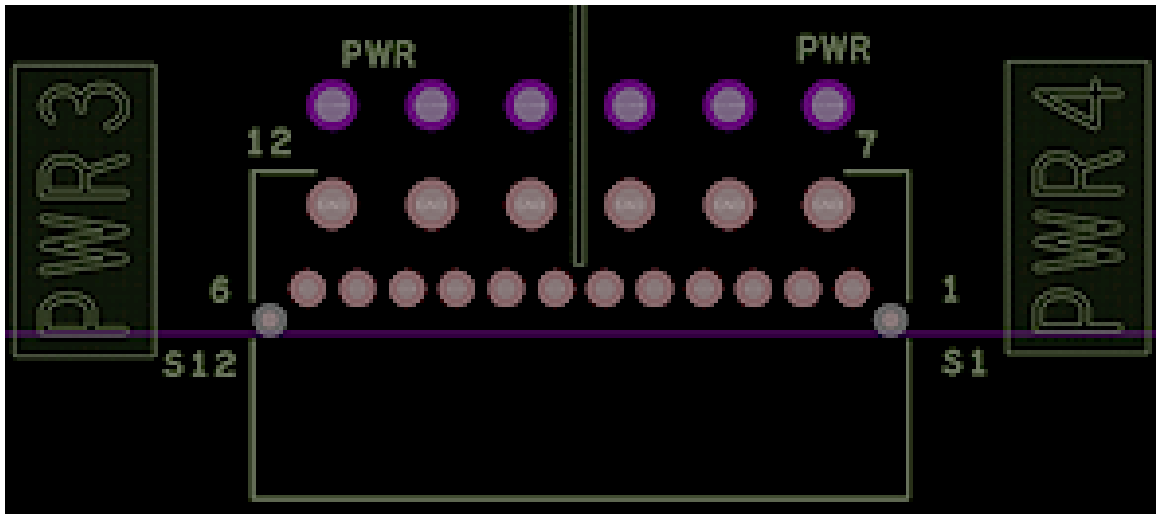


Figure 2: Example 12V 2X6+12 SB labeling with two 12V PICPWR regions.

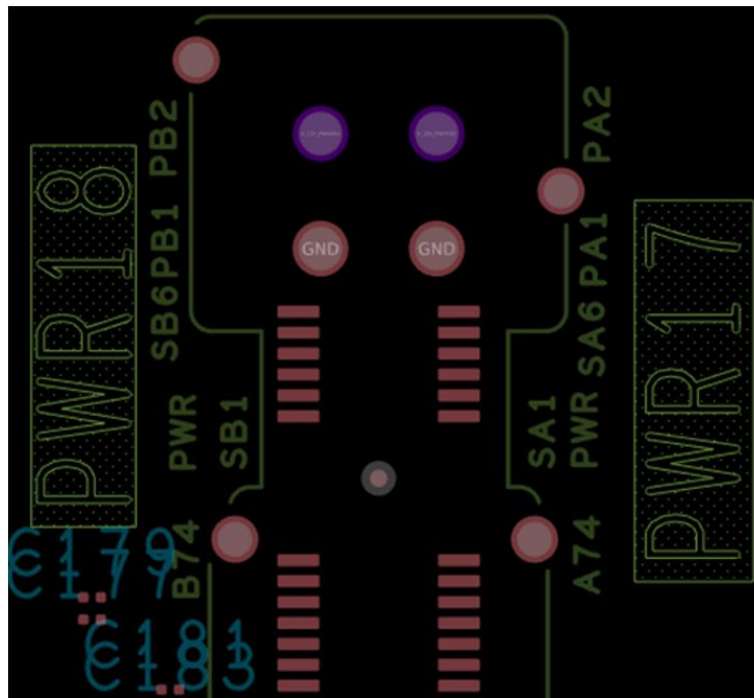


Figure 3: Example: SFF-TA-1033 with two PICPWR regions

10.1.3. 12V Management Signal Naming

The 12V PICPWR and PDB management connector signal naming shown in the rest of this specification is represented as “*location_PICPWRn_****” where; *location* is the destination board on which the connector will be located (*location* is blank since most are expected to be on HPM), *n* is the unique identifier per board and ***** is the signal function (SB[4:1], SCL, or SDA). Example: PDB_PICPWR3_SCL.

10.1.4. 12V HPM Power Distribution Architecture

This section describes implementations of the HPM where the M-CRPS or power subsystem is directly docking into the HPM as shown in *Figure 4*.

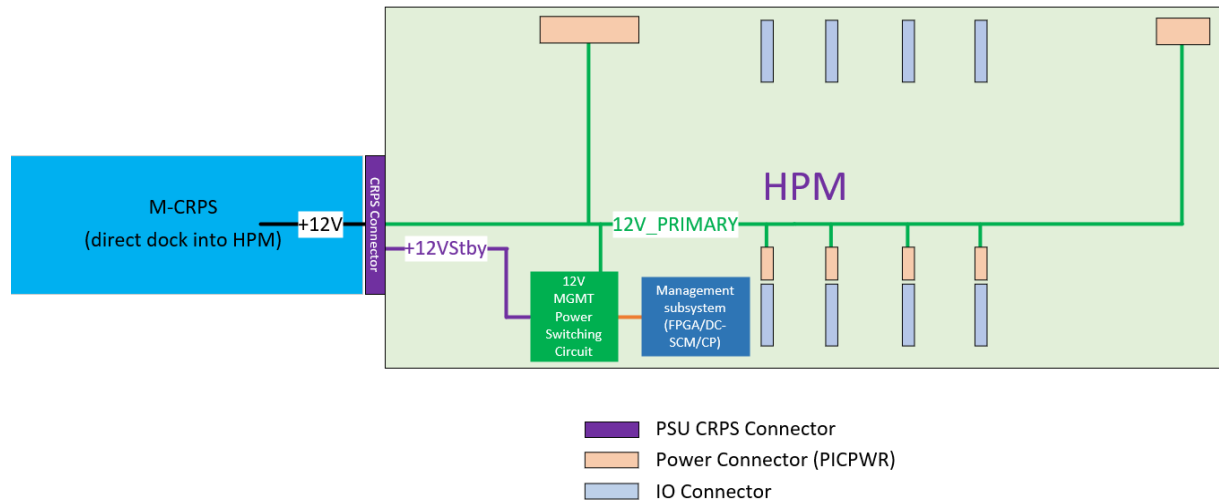


Figure 4: HPM 12V Power Distribution Architecture (M-CRPS Direct mate to HPM variant)

The HPM power distribution architecture has the following attributes:

- “12V_PRIMARY” shall be sourced by +12V (not +12VStby) and powered in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).
- All +12V (12V_PRIMARY) sources shall have controlled ramps.
- The 12V power MGMT switching circuit shall be located on the HPM.
- 12V PICPWR connectors shall only connect to 12V_PRIMARY.
- Individual HPMs shall not connect to more than one 12V_PRIMARY domain.
- 12V PICPWR connectors shall be bi-directional: can be either power source (power egress) or power sink (power ingress).
- Other than the power capability of the power connector, each 12V PICPWR connector on the HPM shall be logically equivalent.
- It is strongly recommended that HPM designs balance current flow through adjacent 12V PICPWR connectors to enable source or load sharing and without overloading one of the two current paths.
- There shall not be power gating to 12V PICPWR connectors on 12V_PRIMARY. However, the HPM may implement fusing to prevent damage to connectors, cables, and traces.
- Any module docking into the M-CRPS connector shall have an OR-ing circuits or hot swap circuits on +12V and +12VStby to prevent reverse current going into the module.

- When +12VStby is not available but 12V PRIMARY is available, the 12V management power switching circuit output shall be sourced by 12V PRIMARY.
- To avoid damage resulting from high currents in PICPWR connectors during partial-mate conditions, it is recommended that HPM and peripheral implementations use 2nd to mate/1st to break SB pins to detect partial-mate conditions. HPMs or Peripherals should also take the necessary actions to prevent high currents through PICPWR connectors (including per channel if a dual channel PICPWR connects to different loads) if a partial-mate condition exists.

10.1.5. 12V Remote Power Distribution Architecture

This section describes requirements of a Remote Power Distribution implementation where the M-CRPS or power subsystem is docking into the Remote PDB or PIB and powering the HPM via a 12V PICPWR connector on the HPM as shown in *Figure 5*.

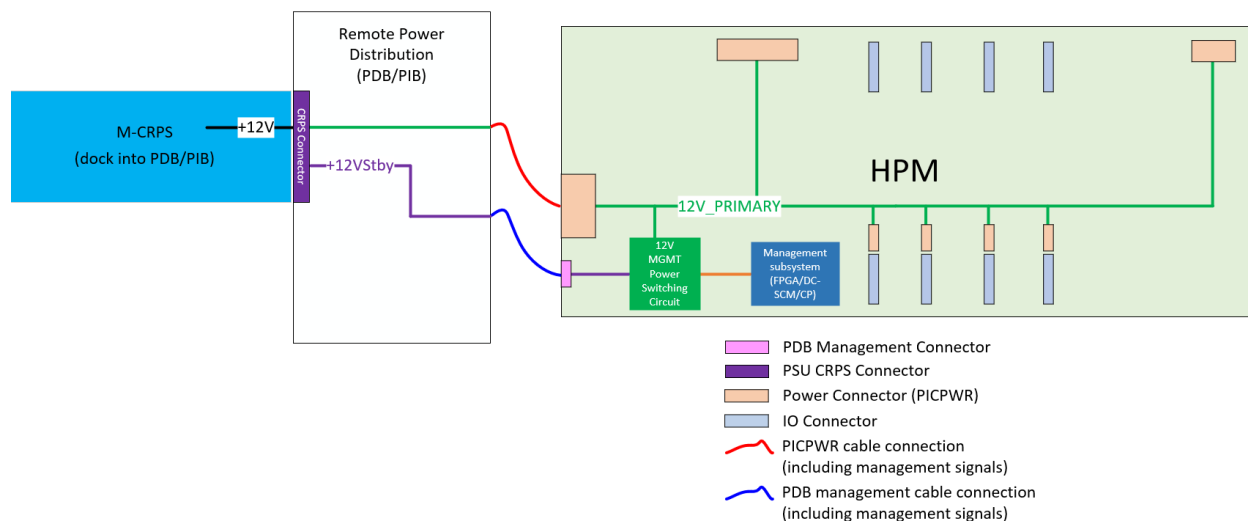


Figure 5: Remote 12V Power Distribution Architecture (M-CRPS mated to PDB/PIB variant)

The 12V remote power distribution architecture has the following attributes:

- “12V PRIMARY” shall be sourced by +12V (not +12VStby) and powered in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).
- All +12V (12V PRIMARY) sources shall have controlled ramps.
- The 12V power management switching circuit shall be located on the HPM.
- 12V PICPWR connectors shall only connect to 12V PRIMARY.
- Individual HPMs shall not connect to more than one 12V PRIMARY domain.
- Any +12V source for 12V PRIMARY and +12VStby source shall have OR-ing circuits or hot swap circuits on +12V and +12VStby to prevent reverse current going into the sources.

- **There shall not be power gating to 12V PICPWR connectors on 12V PRIMARY.** However, the PDB may implement fusing to prevent damage to connectors, cables, and traces.
- **If configurations with power subsystems directly docking into the HPM and connected to the HPM through a PDB exist, requirements for each attachment method shall be met.**
- To avoid damage resulting from high currents in PICPWR connectors during partial-mate conditions, it is recommended that HPM, PDB, and peripheral implementations use 2nd to mate/1st to break SB pins to detect partial-mate conditions. HPMs (and PDB by extension) or Peripherals should also take the necessary actions to prevent high currents through PICPWR connectors (including per channel if a dual channel PICPWR connects to different loads) if a partial-mate condition exists.

10.1.6. 12V Peripheral Subsystem Power Distribution Architecture

This section describes the 12V peripheral subsystem as shown in *Figure 6*.

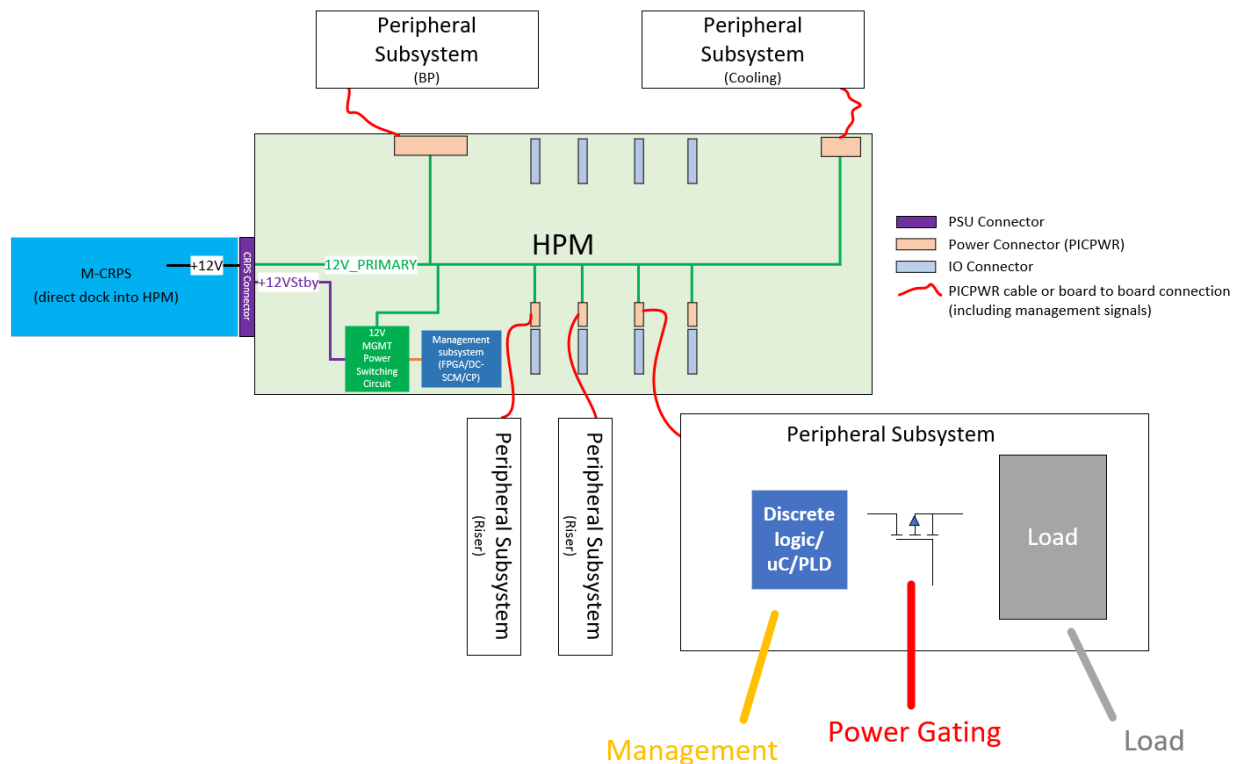


Figure 6: Peripheral Subsystem 12V Power Distribution Architecture

The 12V peripheral subsystem power architecture has the following attributes:

- 12V Peripheral subsystems can attach to any 12V PICPWR connector on the HPM that has the power capability to support loads of the peripheral subsystem.

- 12V PICPWR connectivity methods are dependent on system needs and connection type(s) supported at each 12V PICPWR location (e.g., card edge or a compatible cable).
- For cable applications with 12V PICPWR connectors, the pinouts shall both meet M-PIC pinout requirements.
- A 12V peripheral subsystem consists of a management subsystem, a power gating subsystem, and a power load.
- The 12V peripheral subsystem shall assume that the power rail supplied from the HPM will be operational in the ACPI-S5 power state. If the load on the peripheral subsystem is not intended to operate in the S5 domain, then the peripheral subsystem shall implement appropriate power gating for the load.
- Loads shall not be directly attached to 12V PICPWR connectors [e.g., PCIe AUX power cable attaching from 12V PICPWR to PCIe AIC (Add-In Card) is NOT supported]. Minimally, a power delivery management subsystem shall be implemented on the peripheral subsystem or the load so that it is compatible with the PICPWR sidebands and architecture.
- Individual 12V peripheral subsystems shall not be connected to more than one 12V PRIMARY domain.
- Peripherals may consume a small amount of power for inventory and sideband initialization prior to being transitioned to higher power states by the HPM. It is strongly recommended that peripheral designs minimize the initial power consumed. It is also recommended that system designers verify that the total system power consumed is within the total initial power available.
- Power gating in the peripheral subsystem is needed if loads are not intended to operate in ACPI-S5 state. Power gating can be implemented in a variety of forms including, but not limited to, load switches, hot-swap controller, voltage regulators. Peripherals shall include soft-start functionality to prevent inrush current greater than the connector DC current rating and 0.1A/us as peripherals are enabled and are powering up. Management of the Inrush current due to electrical shorts is optional.
- Per PICPWR sideband set (composed of an SMBus interface, 2 required sidebands, 2 optional sidebands), the SMBus and the 2 required sidebands shall be provided to the peripheral subsystem enabling the HPM to perform status, control, and inventory.
- It is strongly recommended that peripheral designs balance current flow through PICPWR connectors in applications that source power through more than one 12V PICPWR connector (on HPM or on the peripheral) to prevent overloading one of the two current paths.
- To avoid damage resulting from high currents in PICPWR connectors during partial-mate conditions, it is recommended that HPM, PDB, and peripheral implementations use 2nd to mate/1st to break SB pins to detect partial-mate conditions. HPMs (and PDB by extension) or Peripherals should also take the necessary actions to prevent high currents through PICPWR connectors (including per channel if a dual channel PICPWR connects to different loads) if a partial-mate condition exists.
- To avoid PICPWR connector damage resulting from high currents in partial-mate conditions, it is recommended that peripherals (including ones intended to operate in S5) be designed to ensure they do not draw high currents by default if SB pins are not connected when 12V_PRIMARY is powered up.

Figure 7 shows additional details of the power architecture of a peripheral subsystem.

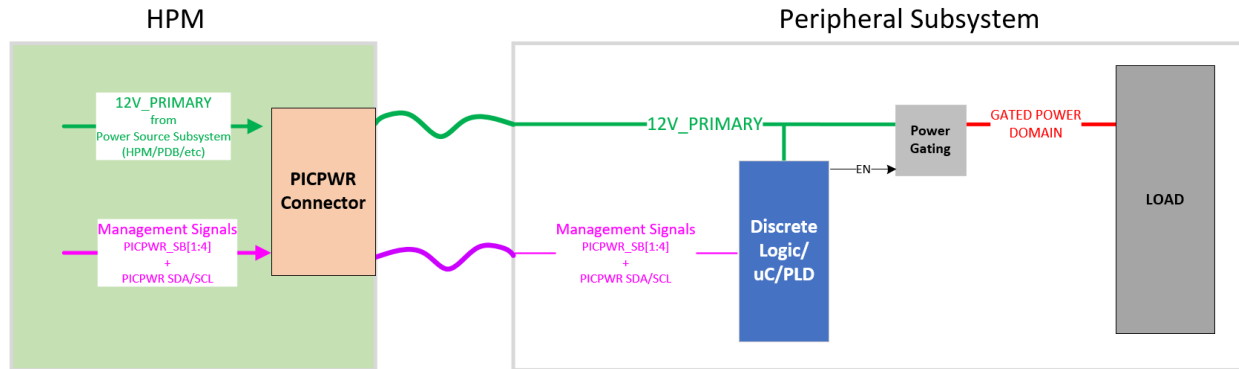


Figure 7: Peripheral Subsystem 12V Power Distribution Architecture Details

10.1.7. 12V PICPWR Connector Pin Definition

Table 2: 12V PICPWR Pin Definition

Pin(s)	Signal Name	Signal Requirements
PWR	12V_PRIMARY	Primary power rail from the power source subsystem used to power downstream loads & logic on peripheral subsystem. <u>12V_PRIMARY shall be sourced by +12V (not +12VStby) and powered in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).</u> Implementation Notes: The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in design specification(s) for system configurations supported per HPM design. Refer to <i>Figure 8</i> for an example configuration showing voltage drop, measurement and set point. <u>12V_PRIMARY tolerance is based on the voltage source setpoint.</u>
PWR	GND	Ground return for 12V_PRIMARY and side-band signals
SB1:4	PICPWR _n _SB[4:1]	<u>Sideband GPIOs for status, control, and inventory of peripheral subsystem; shall be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages.</u> For electrical

		requirements see sections 12 and 12.1 as well as <i>Table 3</i> and <i>Figure 9</i>. The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use PICPWR_SB1 for PRES_N or PESTI functionality and use PICPWR_SB2 as active high power enable or for PWREN (power enable) functionality. PICPWR_SB[4:3] terminations and connections are optional and may be omitted if not used.
SB5	PICPWR _n _SCL	See sections 12 and 12.2 . for SMBus and I3C electrical requirements.
SB6	PICPWR _n _SDA	

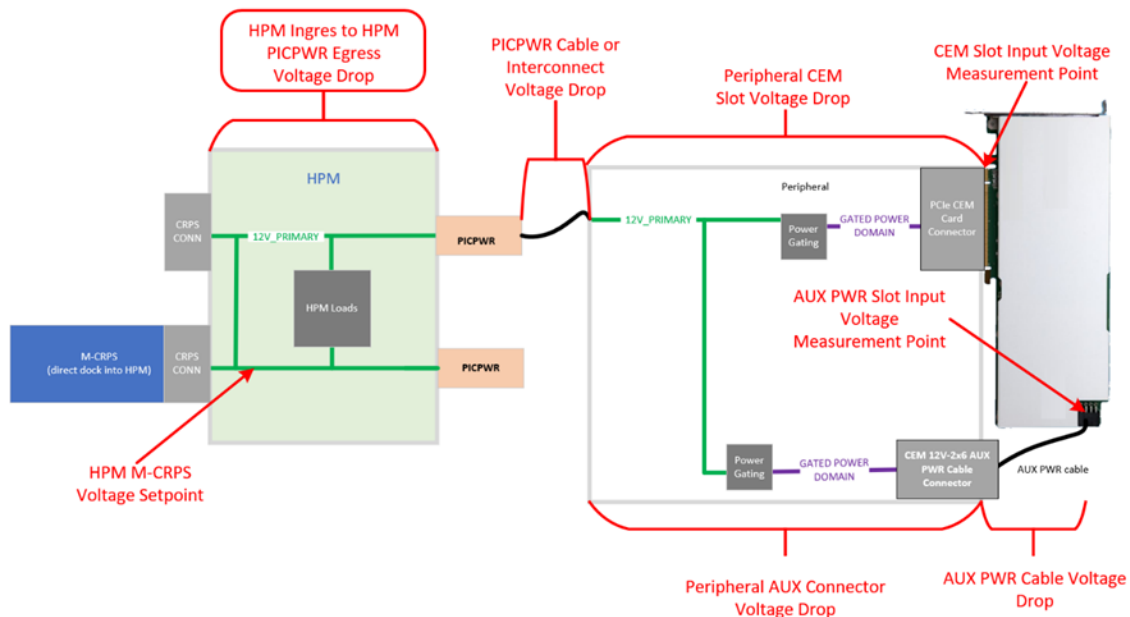


Figure 8: Example of a Configuration Showing Voltage Drop, Measurement, and Set Points

Each instantiation of a PICPWR connector shall implement a unique set of 6 sidebands. For connectors with more than one set of 6 sidebands, each set shall be unique. Additionally, Table 3 describes how the sideband signals on the HPM shall be implemented.

Table 3: Required HPM implementation for each set of 6 sidebands.

Pin	Signal Name	HPM Implementation Requirements		
		HPM Connections	Termination	HPM GPIO Buffer Type
SB1	PICPWR _n _SB1	connect to HPM FPGA GPIO	22Ω Series + 100kΩ pullup to +3.3Vaux **	Configurable as both open-drain AND push-pull
SB2	PICPWR _n _SB2	connect to HPM FPGA GPIO	22Ω Series + 100kΩ pulldown to GND	Configurable as both open-drain AND push-pull
*SB3	*PICPWR _n _SB3	*connect to HPM FPGA GPIO	*22Ω Series + *100kΩ pullup to +3.3Vaux**	*Configurable as both open-drain AND push-pull
*SB4	*PICPWR _n _SB4	*connect to HPM FPGA GPIO	*22Ω Series + *100kΩ pullup to +3.3Vaux**	*Configurable as both open-drain AND push-pull
SB5	PICPWR _n _SCL	connect to DC-SCM SMBus subsystem	See sections 12 and 12.2 for SMBus and I3C electrical requirements.	SMBus or I3C Basic compliant
SB6	PICPWR _n _SDA	connect to DC-SCM SMBus subsystem		SMBus or I3C Basic compliant

*These components and connections are optional and may be omitted if not used.

**+3.3Vaux shall be derived from the 12V management power switching circuit output.

Figure 9 shows the required HPM implementation with the example of two 12V PICPWR connector instantiations. Pullups (R_{PU}) on SCL and SDA are shown for reference, see Table 3 for details.

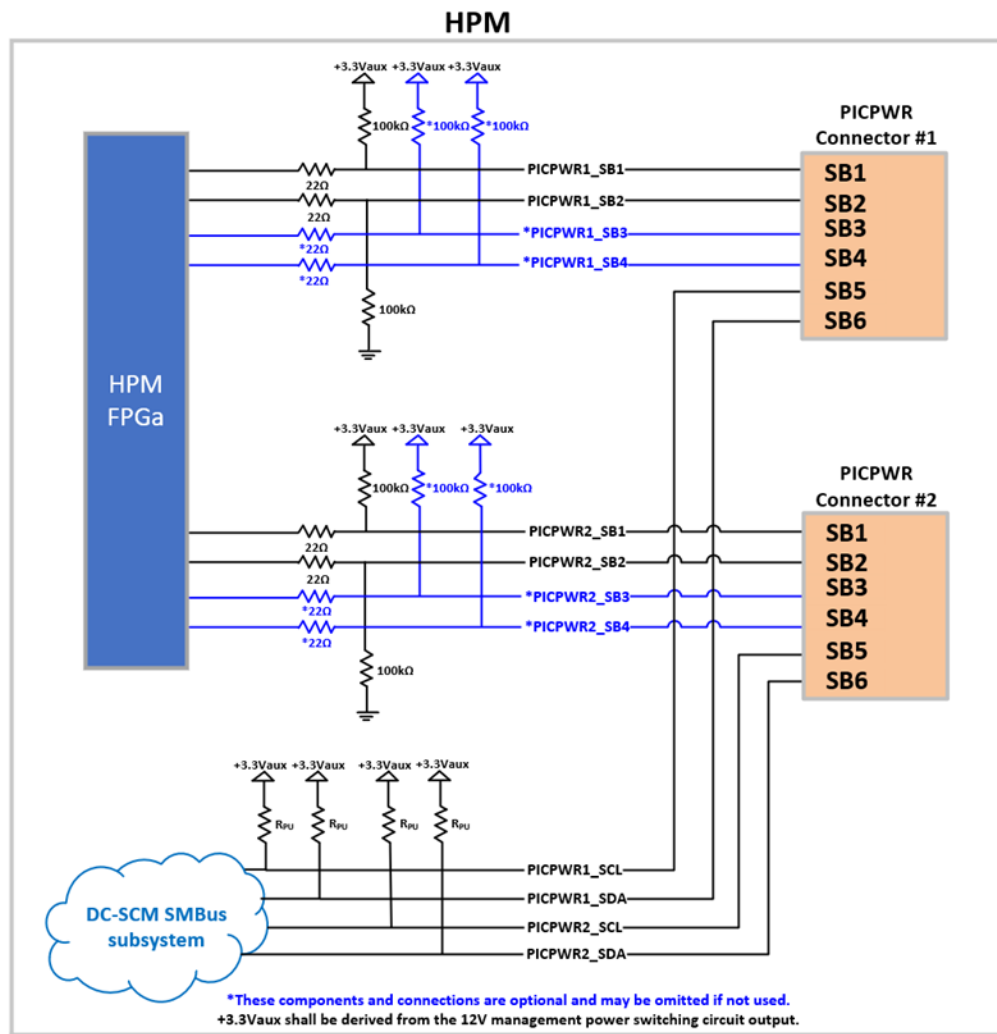


Figure 9: HPM implementation with two 12V PICPWR connectors

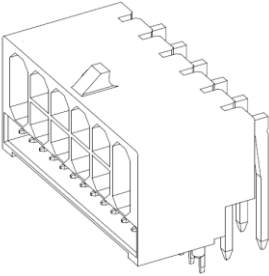
10.1.7.1. 12V 2x6+12SB PICPWR Right-angle Header Pinout

Figure 10: 12V 2x6+12SB Right-angle Header

Notes:

- Connector power rating shall be: 864W (12A per power pin).
- This connector shall have two independent channels of PICPWR sideband management signals.
- Connector shall be pinned out per *Table 4*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 4: 12V 2x6+12SB PICPWR Right-angle Header Pinout

Pin(s)	Signal Name
Circuits [1:6]	GND
Circuits [7:12]	12V_PRIMARY
SB1	PICPWR[n+1]_SB1
SB2	PICPWR[n+1]_SB2
SB3	PICPWR[n+1]_SB3
SB4	PICPWR[n+1]_SB4
SB5	PICPWR[n+1]_SCL
SB6	PICPWR[n+1]_SDA
SB7	PICPWR _n _SB1
SB8	PICPWR _n _SB2
SB9	PICPWR _n _SB3
SB10	PICPWR _n _SB4
SB11	PICPWR _n _SCL
SB12	PICPWR _n _SDA

12V 2x6+12SB physical connector pin numbering shall be implemented per *Figure 11*.

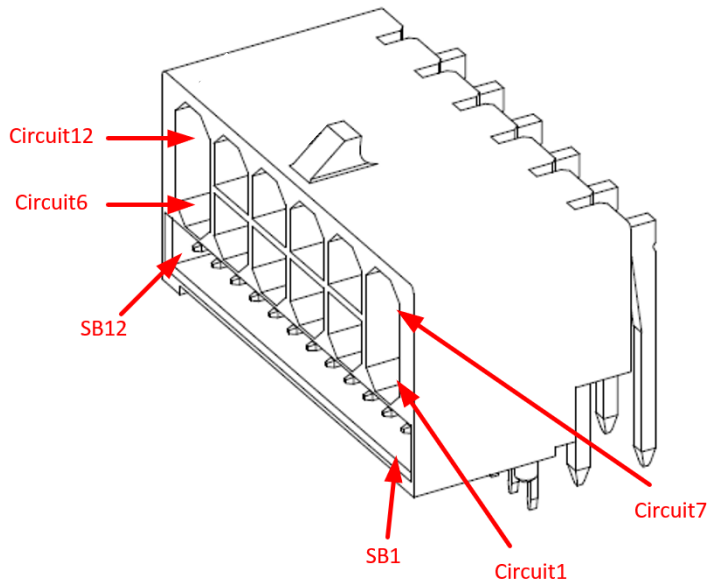


Figure 11: 2x6+12SB Physical Pin Numbering

10.1.7.2. 12V 2x6+12SB PICPWR Vertical Header Pinout

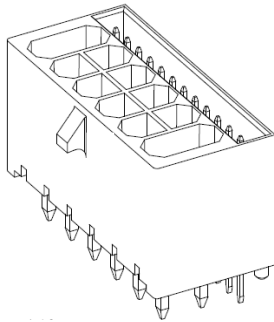


Figure 12: 12V 2x6+12SB Vertical Header

Notes:

- Connector power rating shall be: 864W (12A per power pin).
- This connector shall have two independent channels of PICPWR sideband management signals.
- Connector shall be pinned out per *Table 5*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 5: 12V 2x6+12SB PICPWR Vertical Header Pinout

Pin(s)	Signal Name
Circuits [1:6]	GND
Circuits [7:12]	12V_PRIMARY
SB1	PICPWR[n+1]_SB1
SB2	PICPWR[n+1]_SB2
SB3	PICPWR[n+1]_SB3
SB4	PICPWR[n+1]_SB4
SB5	PICPWR[n+1]_SCL
SB6	PICPWR[n+1]_SDA
SB7	PICPWR _n _SB1
SB8	PICPWR _n _SB2
SB9	PICPWR _n _SB3
SB10	PICPWR _n _SB4
SB11	PICPWR _n _SCL
SB12	PICPWR _n _SDA

12V 2x6+12SB physical connector pin numbering shall be implemented per Figure 11.

10.1.7.3. 12V 2x3+6SB PICPWR Right-angle Header Pinout

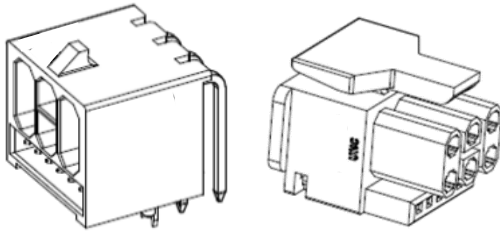


Figure 13: 12V 2x3+6SB Right-angle Header and associated plug.

Notes:

- Connector power rating shall be: 486W (13.5A per power pin).
- This connector shall have one channel of PICPWR sideband management signals.
- Connector shall be pinned out per Table 6.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 6: 12V 2x3+6SB Right-angle Header Pinout

Pin(s)	Signal Name
Circuits [1:3]	GND
Circuits [4:6]	12V_PRIMARY
SB1	PICPWR n _SB1
SB2	PICPWR n _SB2
SB3	PICPWR n _SB3
SB4	PICPWR n _SB4
SB5	PICPWR n _SCL
SB6	PICPWR n _SDA

12V 2x3+6SB physical connector pin numbering shall be implemented per *Figure 14*.

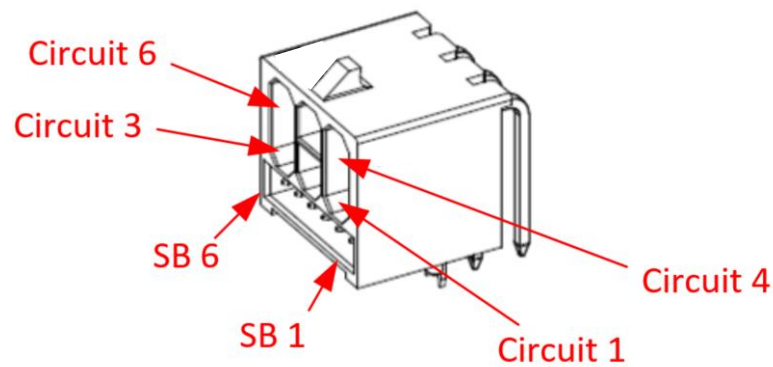


Figure 14: 2x3+6SB Physical Pin Numbering

10.1.7.4. 12V 2x3+6SB PICPWR Vertical Header Pinout

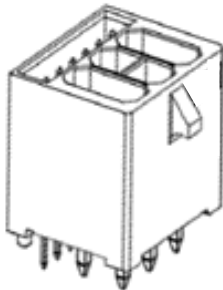


Figure 15: 12V 2x3+6SB Vertical Header

Notes:

- Connector power rating shall be: 486W (13.5A per power pin).

- This connector shall have one channel of PICPWR sideband management signals.
- Connector shall be pinned out per *Table 7*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 7: 12V 2x3+6SB PICPWR Vertical Header Pinout

Pin(s)	Signal Name
Circuits [1:3]	GND
Circuits [4:6]	12V_PRIMARY
SB1	PICPWR _n _SB1
SB2	PICPWR _n _SB2
SB3	PICPWR _n _SB3
SB4	PICPWR _n _SB4
SB5	PICPWR _n _SCL
SB6	PICPWR _n _SDA

12V 2x3+6SB physical connector pin numbering shall be implemented per *Figure 14*.

10.1.7.5. 12V Near Side Riser PICPWR Pinout

The SFF-TA-1033 specification defines versions with IO and a PICPWR section as shown in *Figure 16*.

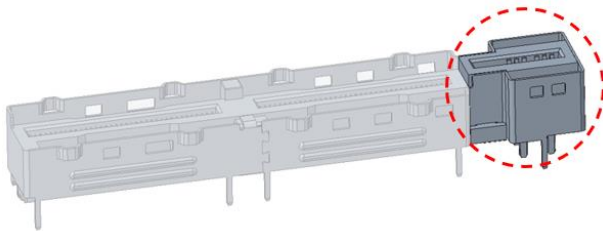


Figure 16: 12V SFF-TA-1033 (I/O Plus Power)

The SFF-TA-1033 specification also defines a version with only the PICPWR section as shown in *Figure 17*.

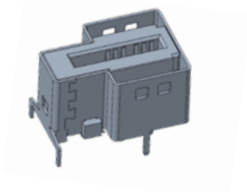


Figure 17: 12V SFF-TA-1033 (power only)

Notes:

- Connector power rating shall be: 252W (10.5A per power pin).
- SFF-TA-1033 (I/O plus power) includes M-XIO and PICPWR pins all within the same housing. The power section of this connector (circled in Figure 16) shall be pinned out per Table 8. Refer to M-XIO specification for additional pinout details.
- SFF-TA-1033 (power only) includes only the power section of this connector (shown in Figure 17). The power only version of this connector shall be pinned out per Table 8.
- All SFF-TA-1033 connectors shall include two independent channels of 12V PICPWR sideband management signals.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 8: 12V Near Side Riser PICPWR Pinout

Pin	Signal Name	Signal Name	Pin
PB2	12V_PRIMARY	12V_PRIMARY	PA2
PB1	GND	GND	PA1
SB6	PICPWR[n+1]_SDA	PICPWRn_SDA	SA6
SB5	PICPWR[n+1]_SCL	PICPWRn_SCL	SA5
SB4	PICPWR[n+1]_SB4	PICPWRn_SB4	SA4
SB3	PICPWR[n+1]_SB3	PICPWRn_SB3	SA3
SB2	PICPWR[n+1]_SB2	PICPWRn_SB2	SA2
SB1	PICPWR[n+1]_SB1	PICPWRn_SB1	SA1

12V near side riser PICPWR physical connector pin numbering shall be implemented per Figure 18.

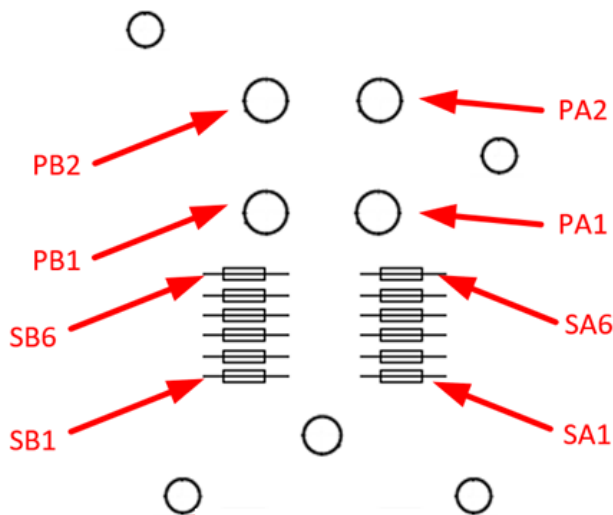


Figure 18: SFF-1033 (power only) Physical Pinout

10.1.7.6. 12V 3+16S+3 PICPWR Blind-mate Right-angle Connector Pinout

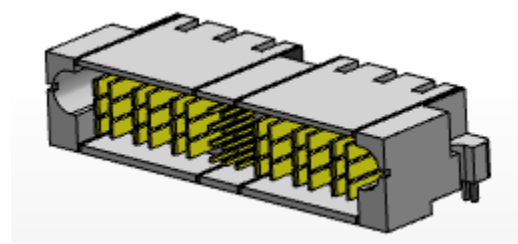


Figure 19: 12V 3+16S+3 PICPWR Blind-mate Connector.

Notes:

- Connector power rating shall be: 2000W (56A per high power contact, 3A per signal contact).
- This connector shall have two independent channels of PICPWR sideband management signals.
- Connector shall be pinned out per Table 9.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 9: 12V 3+16S+3 PICPWR Blind-mate Right-angle Connector Pinout

Pin(s)	Signal Name
P[1:3]_ [1:8]	GND
A1	PICPWR n _SCL
A2	PICPWR n _SDA
A3	PICPWR n _SB1
A4	IMON
B1	PICPWR n _SB2
B2	PICPWR n _SB3
B3	PICPWR n _SB4
B4	+12VStby
C1	PICPWR[$n+1$]._SCL
C2	PICPWR[$n+1$]._SDA
C3	PICPWR[$n+1$]._SB1
C4	VMON
D1	PICPWR[$n+1$]._SB2
D2	PICPWR[$n+1$]._SB3
D3	PICPWR[$n+1$]._SB4
D4	+12VStby
P[4:6]_ [1:8]	12V_PRIMARY

12V 3+16S+3 PICPWR blind-mate right-angle connector physical pinout shall be implemented per Figure 20.

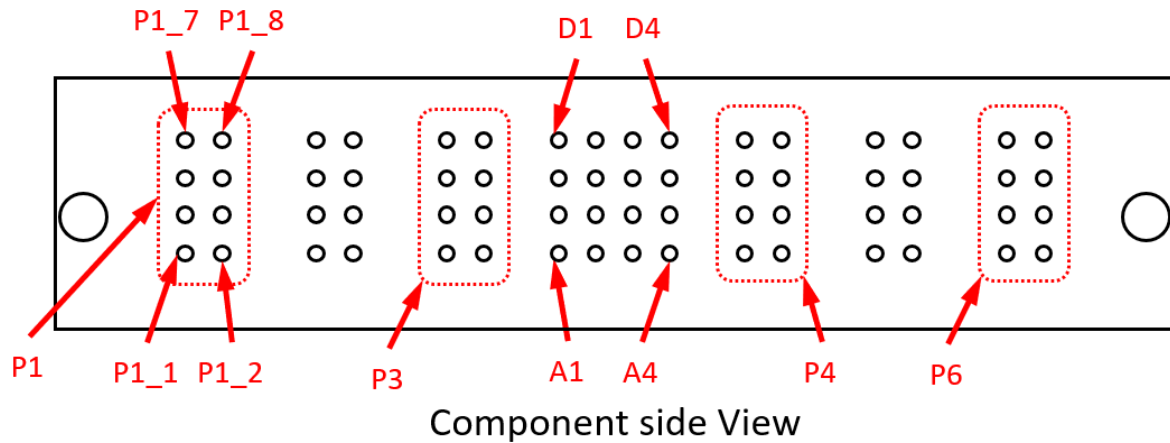
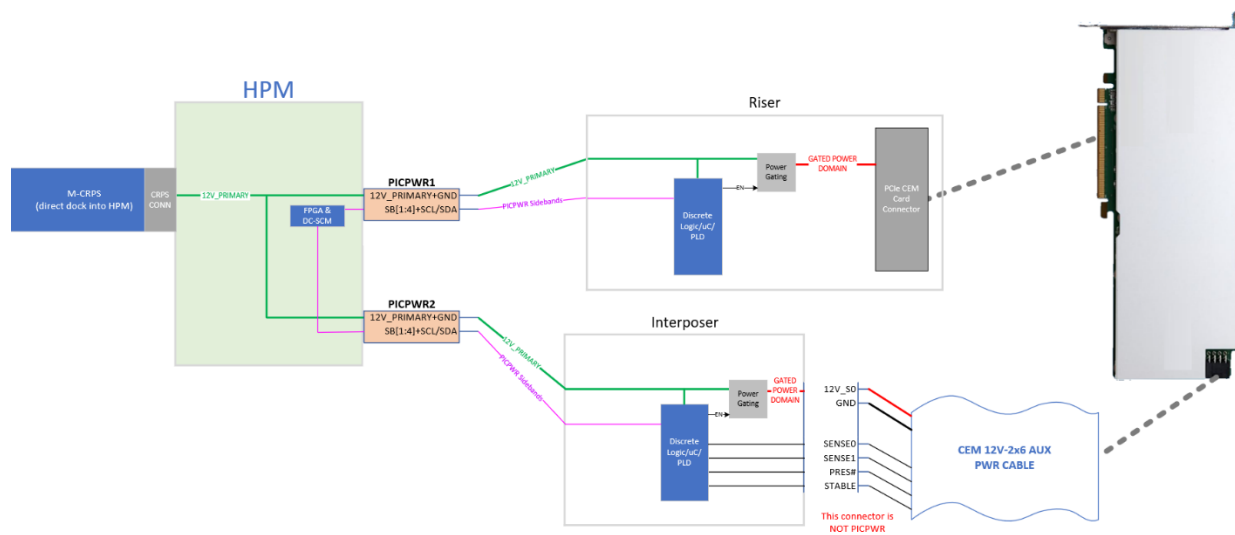


Figure 20: 12V 3+16S+3 PICPWR Blind-mate Right-angle Connector Physical Pinout

10.1.8. Example 12V Topologies

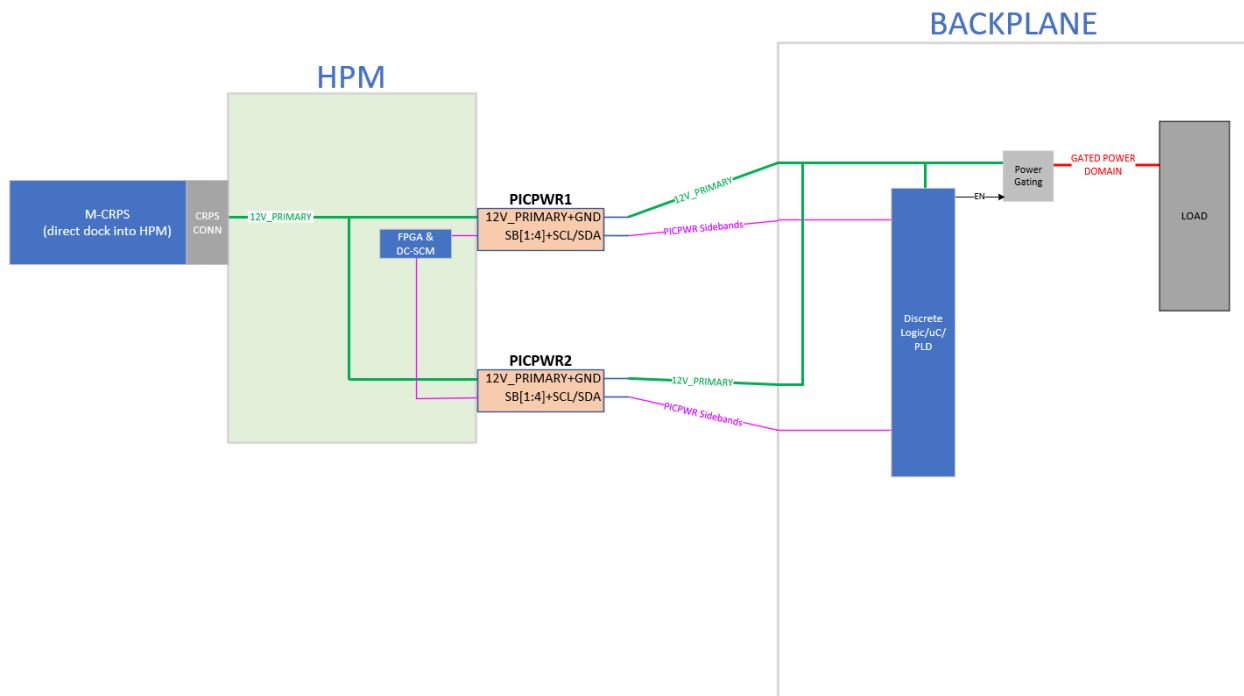
10.1.8.1. Powering a 12V PCIe Device with AUX Power Cable

Figure 21 shows a couple of example implementations of how to use 12V PICPWR to power a PCIe device with an AUX cable.



Note that the PCIe AUX power cable is not directly attached a 12V PICPWR connector. Instead, the AUX power cable comes from a PDB or a peripheral subsystem with management and power gating capability.

Figure 22 shows two 12V PICPWR connectors on the HPM powering a single peripheral subsystem to support the large power requirements of a single peripheral subsystem.



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It is strongly recommended that HPM, cable, and peripheral designs balance current flow through both PICPWR connectors in applications with shared sources or loads to prevent overloading one of the two current paths.

10.1.8.3. 12V PICPWR Implementation in a M-CRPS PDB Topology

In *Figure 23*, M-CRPS instances on a PDB provide power to the HPM through 12V PICPWR connectors.

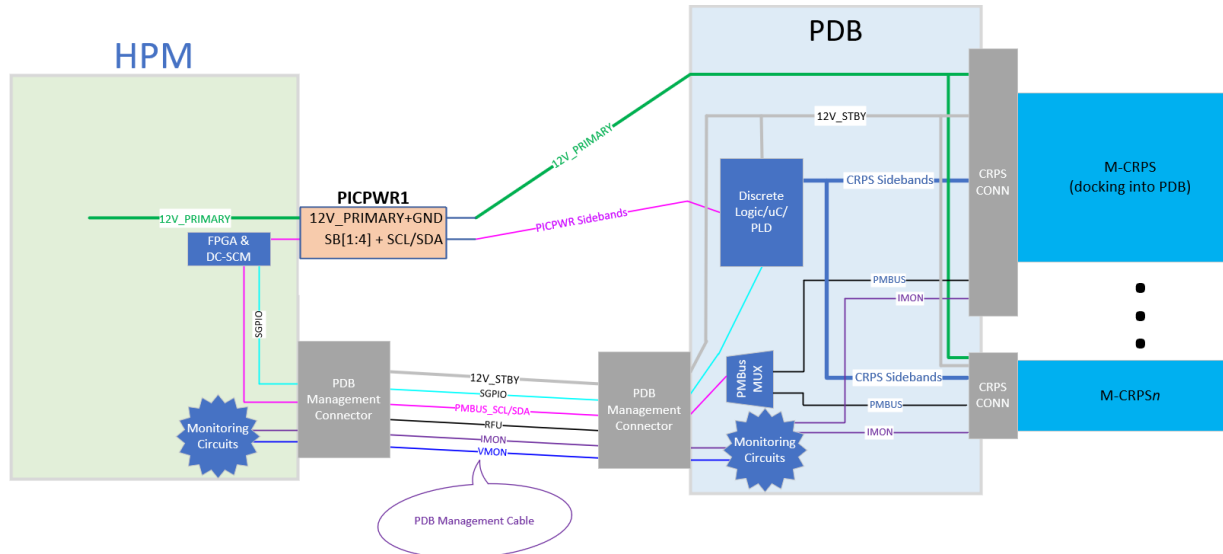


Figure 23: Power Supplies through a PDB

The HPM and the M-CRPS instances communicate all real-time control and status through the 12V PICPWR sideband and/or PDB management pins described in section 10.2.14. PDB management PMBus pins provide a mechanism for PMBus messages between the HPM and M-CRPS instances.

10.2. 48V Power Distribution and Management

This section describes 48V power distribution requirements as well as additional 12V power distribution requirements. The additional 12V power distribution requirements account for conditions that do not exist in the M-PIC architecture release V1.0 relating to 12V use in an environment where both 12V and 48V must coexist.

This section also addresses hot plug at the busbar clip but does not outline the necessary requirements to safely support hot plug functionality at dedicated 48V supply or 48V PICPWR connections. However, this specification does not preclude hot plug support of dedicated 48V supply or 48V PICPWR connections when using a designer-chosen, implementation-specific method.

10.2.1. Dedicated 48V Supply Connector Form Factor and Implementation

Distribution of 48V power from a source requiring voltage ramp control to a 48V HPM and/or 48V PDB may be implemented using a dedicated 48V supply connector which meets the following requirements:

- PCB mounted connector shall be a vertical or right-angle header.
- Wire side plug shall be a straight plug.
- Connectors shall have power pins with equal capability for 48V power supply and return.
- Connectors shall have 1 sideband circuit dedicated for Power Sense and 1 sideband circuit dedicated for Power Sense Return. Each sideband circuit shall support 1.5A continuous current load.
- 48V return circuits on the dedicated 48V supply connector shall be 1st to mate and last to break.
- 48V power supply circuits on the dedicated 48V supply connector shall be 2nd to mate and 2nd to break.
- Dedicated 48V sense sideband circuits of the dedicated 48V supply connector shall be last to mate and 1st to break.
- Connector shall be keyed to prevent mating with any 12V PICPWR, PCIe connectors, or other non-dedicated 48V supply connectors present in the design.
- HPMs whose input voltage is 48V shall source power from a 48V rack busbar, an M-SIF 48V connector, a dedicated 48V supply connector pass-through on a 48V PDB, or any equivalent source.
- PDBs whose input voltage is 48V may source power from a 48V rack busbar, 48V M-CRPS, M-SIF 48V connector, or from or any equivalent source.
- 48V enabled devices, other than HPM or PDB, shall not be attached directly to dedicated 48V supply connectors.
- *Figure 24 shows an example of a dedicated 48V supply connector.*

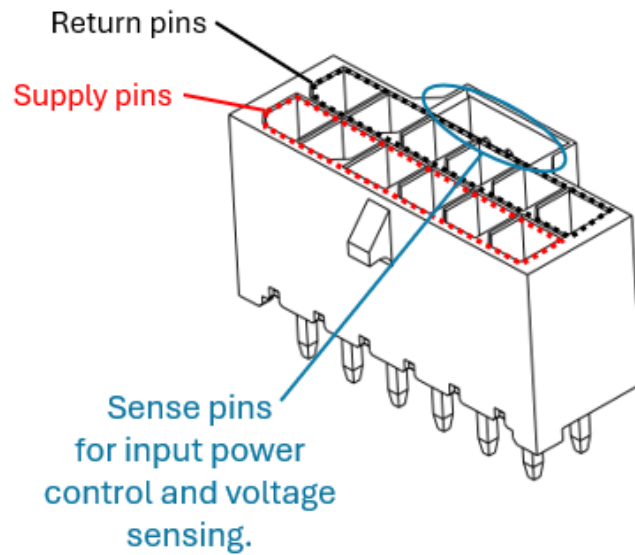


Figure 24: Example of a Dedicated 48V Supply Connector

10.2.2. Dedicated 48V Supply Connector Labeling Requirements

Dedicated 48V supply connector labeling requirements shall follow the 12V PICPWR labeling requirements in section [10.1.2](#) but replace “PWR” with “SPWR (for **S**upply **P**oWe**R**)”. Labeling for dedicated 48V supply connectors is recommended to include a suffix identifying the minimum operating voltage (e.g., “_40V”) because HPMS and PDBs may be designed to operate at different minimum voltages.

10.2.3. 48V PICPWR Connector Form Factor and Implementation

Distribution of ramp controlled 48V power from 48V HPMS and from 48V PDBs to peripheral subsystems may be implemented in any connector form factor that meets the following minimum requirements:

- Connectors shall have power pins with equal capability for 48V PRIMARY power supply and return.
- Connectors shall have 6 sideband pins dedicated for power delivery management.
- Connector 48V return circuits shall be 1st to mate and last to break.
- 48V PRIMARY circuits on the 48V PICPWR connector shall be 2nd to mate and 2nd to break.
- Connector dedicated sideband circuits shall be last to mate and 1st to break.
- Connector shall be keyed to prevent mating with any 12V PICPWR, PCIe connectors, or other non 48V PICPWR connectors present in the design.

Power connectors that meet the minimum requirements are referred to as 48V PICPWR connectors.

48V PICPWR connectors on PDBs and HPMs shall only be used for egress connections since the output from 48V HSCs does not include OR-ing capability.

A 48V PICPWR connector may include an implementation that has additional function/signals (for example, additional sideband signals) shared in a common connector housing. Additionally, a 48V PICPWR connector may support multiple channels of sideband signals, where each channel shall contain the 6 sideband pins dedicated for power delivery management.

A 48V PICPWR connector shall only be connected to 48V PRIMARY nets. For example, direct connection of 48V PICPWR to a 48V rack busbar voltage source is disallowed.

Figure 25 shows an example of a stand-alone 48V PICPWR connector.

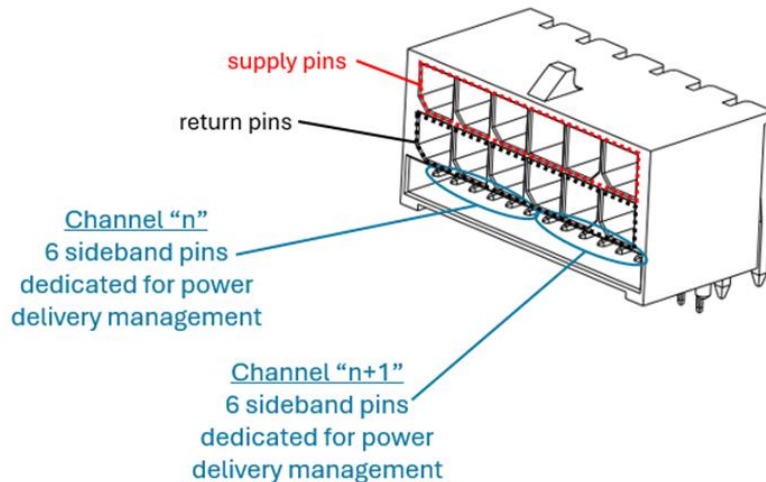


Figure 25: Example of a 48V PICPWR Connector

10.2.4. 48V PICPWR Connector Labeling Requirements

48V PICPWR labeling requirements shall follow 12V PICPWR labeling requirements in section 10.1.2. Labeling for dedicated 48V PICPWR connectors is recommended to include a suffix identifying the minimum operating voltage (e.g., "_40V") because HPMs and PDBs may be designed to operate at different minimum voltages.

10.2.5. 48V Rack Remote Power Distribution Architecture with a 12V HPM

This section describes requirements for a Remote Power Distribution implementation (shown in *Figure 26*) where a 48V rack source powers the Remote PDB via a dedicated 48V supply connector. In this implementation, the Remote Power Distribution or PDB/PIB powers a 12V HPM, 12V peripherals via 12V PICPWR connectors, and 48V peripherals via 48V PICPWR connectors as shown in *Figure 26*. 12V peripherals may be provided power by 12V PICPWR connection through 12V PICPWR connectors on the HPM instead of the PDB.

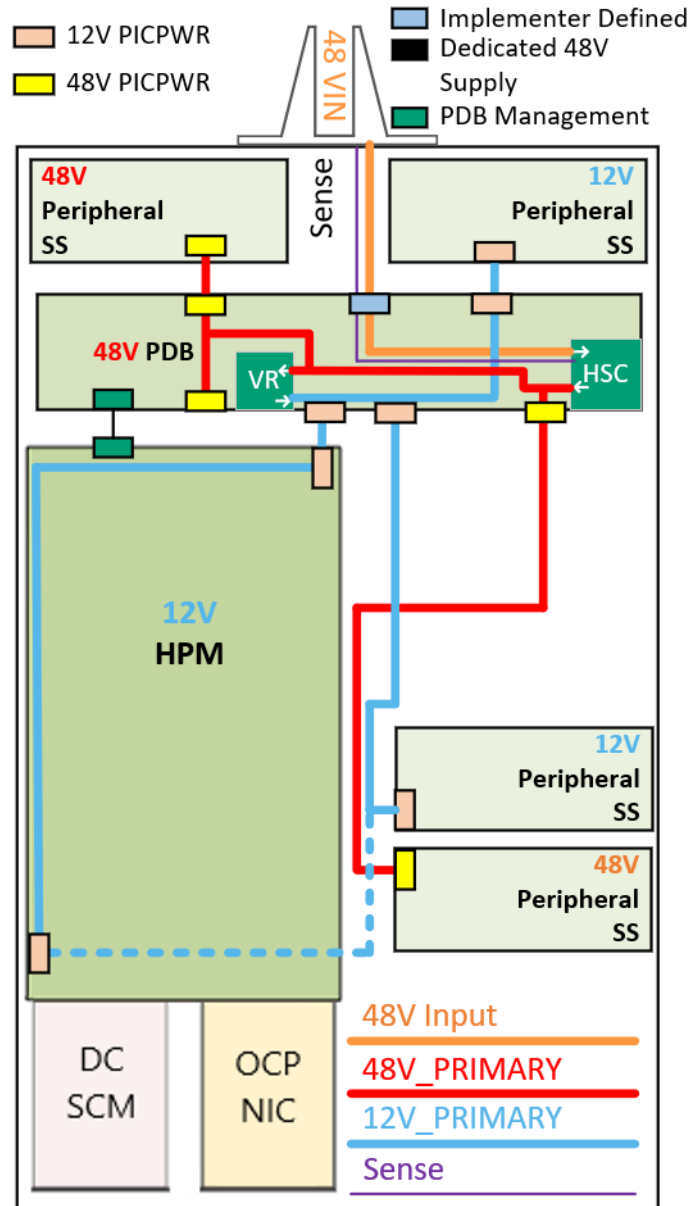


Figure 26: Remote 48V Rack Source Powering a PDB/PIB Variant with a 12V HPM.

Notes:

- The dashed line from HPM to peripheral indicates the option to connect 12V PICPWR to the peripheral from HPM instead of from PDB.
- +12VStby connectivity is not shown.

In addition to the remote power distribution attributes defined in section **10.1.5**, configurations with 48V rack sourced remote power distribution architecture and using a 12V HPM shall have the following attributes:

- This architecture shall implement a PDB.
- The PDB shall contain one or more HSC circuits to provide controlled ramp of 48V PRIMARY output to downstream devices.
 - Each HSC circuit shall be provided a 48V Power Sense signal from the 48V busbar clip or equivalent 48V source through a dedicated 48V supply connector or equivalent input connection.
 - Each HSC circuit shall not be enabled before 48V is present on the 48V Power Sense signal.
 - Each HSC circuit shall be disabled as soon as the system detects a loss of 48V on the Power Sense signal.
 - If there is more than one 48V input source, the input control circuits shall include OR-ing or isolation to prevent current from passing between input sources.
- PDB shall provide +12VStby to the HPM to enable management in power states when one or more HSC is enabled, and 12V PRIMARY is not powered.
- Any +12VStby source shall have an OR-ing circuit or a hot swap circuit on +12VStby to prevent reverse current going into the source.
- Individual 12V peripheral subsystems shall not be connected to more than one 12V PRIMARY domain.

10.2.6. 48V M-CRPS Remote Power Distribution Architecture with a 12V HPM

This section describes requirements for a Remote Power Distribution implementation where one or more 48V M-CRPS or power subsystems are docking into the Remote Power Distribution or PDB/PIB. In this implementation, the Remote Power Distribution or PDB/PIB powers a 12V HPM, 12V peripherals via 12V PICPWR connectors, and 48V peripherals via 48V PICPWR connectors as shown in *Figure 27*. 12V peripherals may be provided power by 12V PICPWR connection through 12V PICPWR connectors on the HPM instead of the PDB.

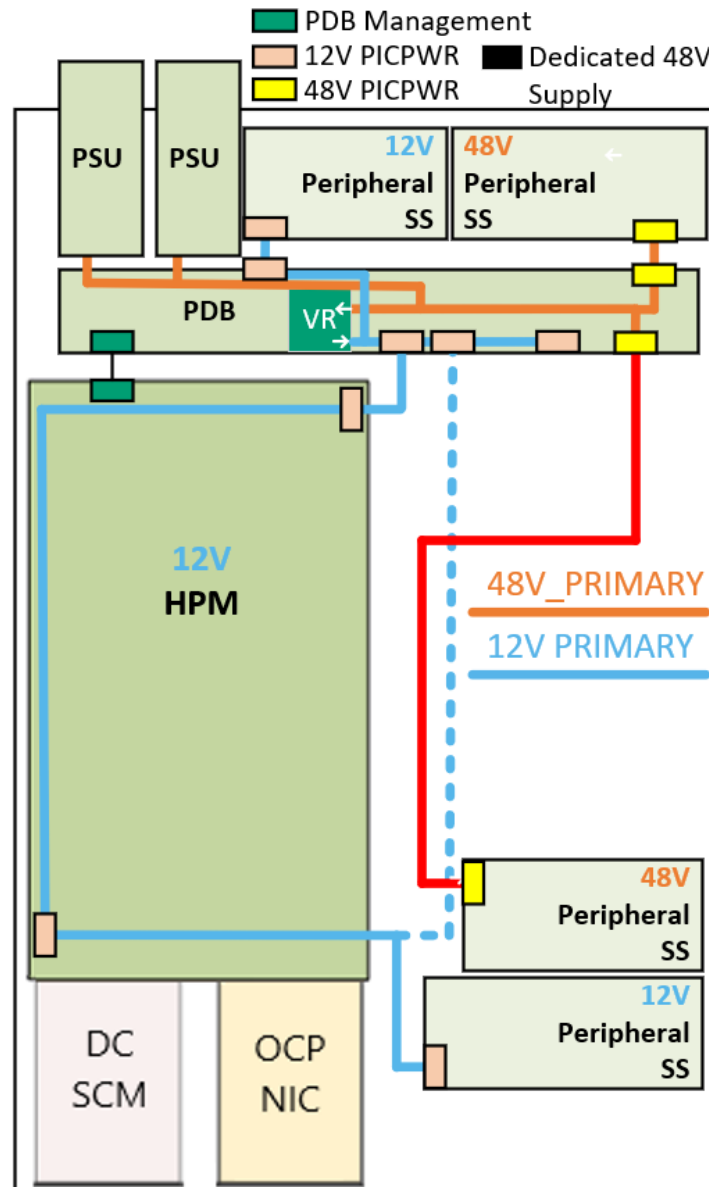


Figure 27: Remote 48V M-CRPS Source Powering a PDB/PIB Variant with a 12V HPM.

Notes:

- The dashed line from PDB to peripheral indicates the option to connect 12V PICPWR to the peripheral from PDB instead of from HPM.
- +12VStby connectivity is not shown.

In addition to the remote power distribution attributes defined in section **10.1.5**, configurations with 48V M-CRPS sourced remote power distribution architecture and a 12V HPM have the following attributes:

- PDB shall provide +12VStby to the HPM to enable management in power states when one or more CRPS is powered, and 12V PRIMARY is not powered.

- Any module docking into the M-CRPS connector shall have an OR-ing circuits or hot swap circuits on +48 and +12VStby to prevent reverse current going into the module.
- Individual 12V peripheral subsystems shall not be connected to more than one 12V PRIMARY domain.

10.2.7. 48V Rack to SIF Remote Power Distribution Architecture with a 12V HPM

This section describes requirements for a Remote Power Distribution implementation where a 48V rack source (via a SIF PDB) powers multiple M-SIF components including a sled level Remote Power Distribution or PDB/PIB via a 48V SIF CONN and powers a sled level 12V HPM and 12V peripherals via 12V PICPWR (on either HPM or PDB), as well as any 48V peripherals via a 48V PICPWR connector on the sled level PDB as shown in *Figure 28*.

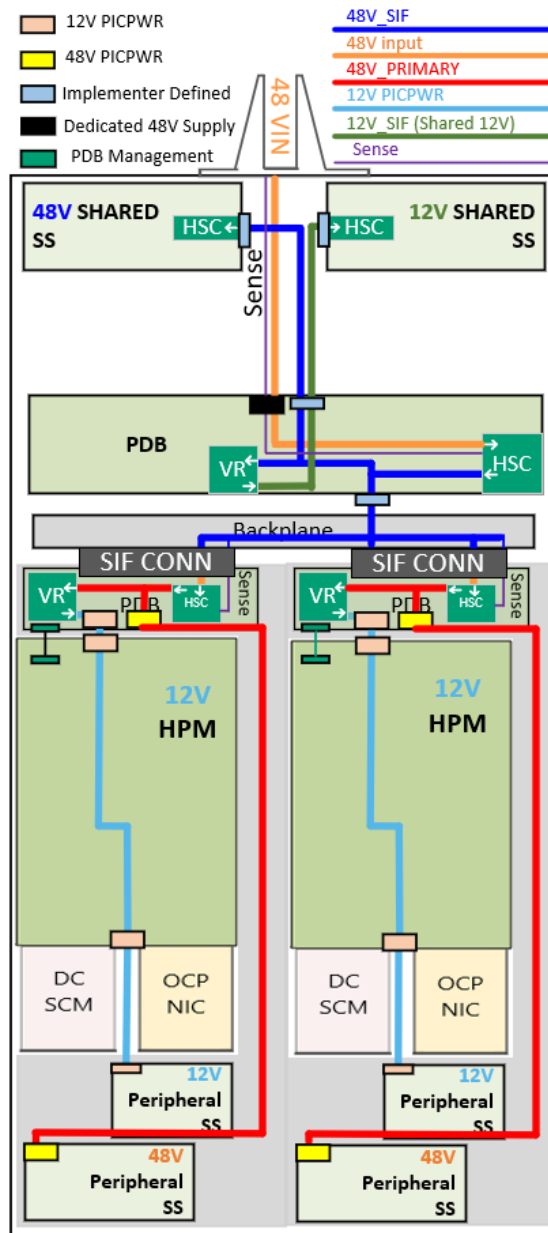


Figure 28: Remote M-SIF PDB Powering a PDB/PIB Variant with a 12V HPM.

Note: +12VStby connectivity is not shown.

In addition to the remote power distribution attributes defined in section **10.1.5**, configurations with M-SIF sourced remote power distribution architecture and a 12V HPM have the following attributes:

- PDB (after SIF CONN) shall provide +12VStby to the HPM to enable management in power states when the HSC is enabled, and 12V PRIMARY is not powered.
- Individual 12V peripheral subsystems in each SIF sled shall not be connected to more than one 12V PRIMARY domain.

10.2.8. 48V Rack Remote Power Distribution Architecture with a 48V HPM

This section describes requirements for a Remote Power Distribution implementation where a 48V rack source powers a PDB and/or HPM via a dedicated 48V supply connector. The PDB and/or HPM then powers 12V peripherals via the 12V PICPWR connector(s) and 48V peripherals via the 48V PICPWR connector(s) located on the PDB or HPM as shown in.

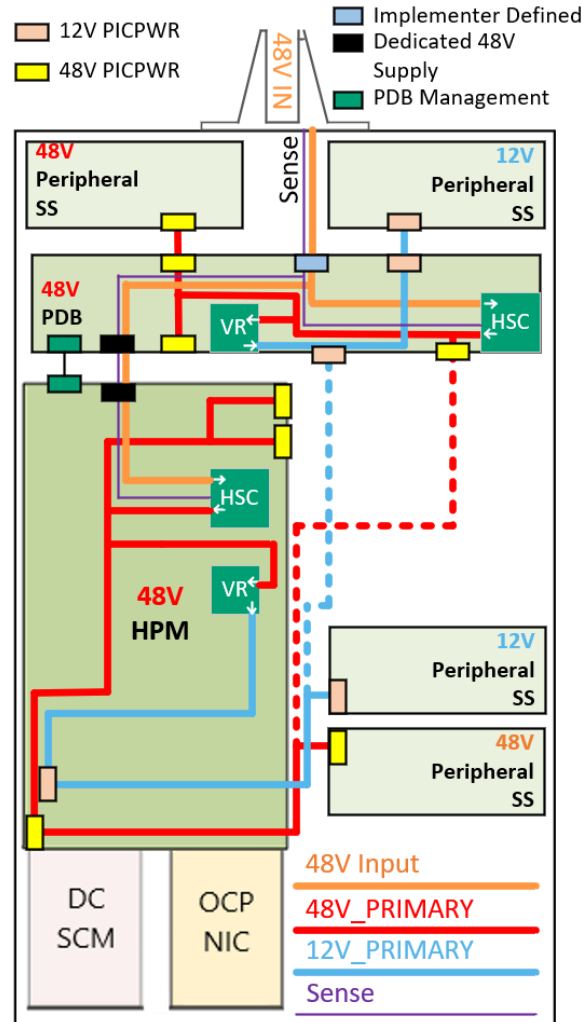


Figure 29: Remote 48V Rack Source Powering a 48V HPM and an optional PDB.

Notes:

- The example includes an optional PDB as a pass-through to power the HPM. If the PDB is not included, then the power source for the HPM may be cabled from the clip to one or more dedicated supply connector on the HPM. Implementations that cable from a single clip to two 48V input loads (e.g., one HPM and one PDB, two HPMS) may also be used.
- The dashed lines from PDB to peripherals indicate options to connect from PDB instead of from HPM.
- +12VStby connectivity is not shown.

In addition to the remote power distribution attributes defined in section **10.1.5**, configurations with a 48V rack sourced remote power distribution architecture and a 48V HPM have the following attributes:

- The PDB and HPM shall each contain one or more HSC circuits to provide controlled ramp of 48V PRIMARY output to downstream devices (other than dedicated 48V supply connectors).

- Each HSC circuit shall be provided a 48V Power Sense signal from the 48V busbar clip or equivalent 48V source through a dedicated 48V supply connector or equivalent input connection.
- Each HSC circuit shall not be enabled before 48V is present on the 48V Power Sense signal from the associated input source.
- Each HSC circuit shall be disabled as soon as the system detects a loss of 48V on the Power Sense signal from the associated input source.
- If there is more than one 48V input source, the input control circuits shall include OR-ing or isolation to prevent current from passing between input sources.
- HPM shall include one or more dedicated 48V supply connectors.
- HPM may include one or more 48V PICPWR connectors.
- HPM shall be functional when powered through one or more dedicated 48 supply connectors.
- If the PDB is used as a pass-through to power the HPM, then the PDB shall include one or more dedicated 48V supply connectors to supply power to the HPM.
- PDB shall provide +12VStby to the HPM to enable management in power states when one or more HSC is enabled, and 12V PRIMARY is not powered.
- Individual 12V peripheral subsystems shall not be connected to more than one 12V PRIMARY domain.

10.2.9. 48V M-CRPS Remote Power Distribution Architecture with a 48V HPM

This section describes requirements of a Remote Power Distribution implementation where a 48V M-CRPS or power subsystem is docking into the Remote Power Distribution or PDB/PIB and powers a 48V HPM and 12V peripherals via the 12V PICPWR connector(s) on the PDB or HPM, and 48V peripherals via the 48V PICPWR connector(s) on the PDB or HPM as shown in *Figure 30*.

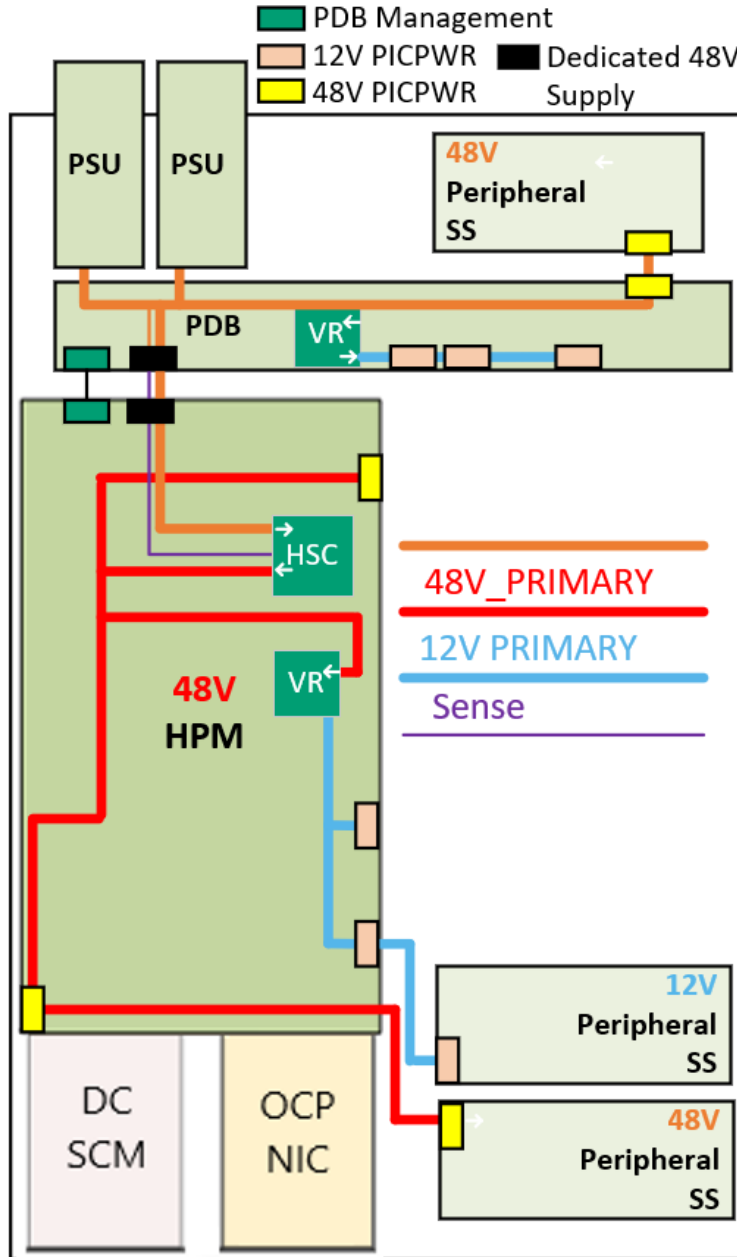


Figure 30: Remote 48V M-CRPS Source Powering a PDB/PIB Variant with a 48V HPM.

Note: +12VStby connectivity is not shown.

In addition to the remote power distribution attributes defined in section **10.1.5**, configurations with 48V M-CRPS sourced remote power distribution architecture and a 48V HPM have the following attributes:

- The HPM shall meet all the HPM and peripheral requirements defined in section 10.2.8.
- The PDB shall include one or more dedicated 48V supply connector to supply power to the HPM.

- Any +48V source for 48V PRIMARY and +12VStby source shall have OR-ing circuits or hot swap circuits on +48V and +12VStby to prevent reverse current going into the sources.

10.2.10. 48V Rack to SIF Remote Power Distribution Architecture with a 48V HPM

This section describes requirements for a Remote Power Distribution implementation where a 48V rack source (via a SIF PDB) powers multiple M-SIF components including a sled level Remote Power Distribution or PDB/PIB via a 48V SIF CONN and powers a sled level 48V HPM, 12V peripherals via the 12V PICPWR connector(s) on either PDB or HPM, and 48V peripherals via the 48V PICPWR connector(s) on the sled level PDB or HPM as shown in *Figure 31*.

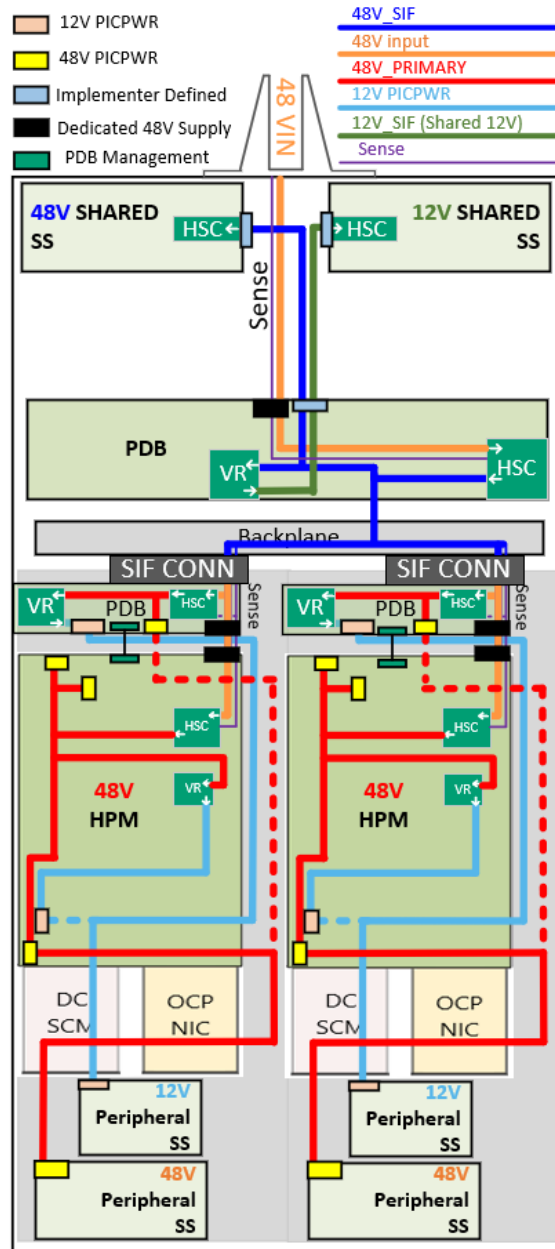


Figure 31: Remote M-SIF PDB Powering a PDB/PIB Variant with a 48V HPM.

Note: +12VStby connectivity is not shown.

In addition to the remote power distribution attributes defined in section **10.1.5**, configurations with M-SIF sourced remote power distribution architecture and a 12V HPM have the following attributes:

- The HPM, peripherals, and the sled level PDB shall meet all the requirements defined in section **10.2.8**.

10.2.11. 48V Peripheral Subsystem Power Distribution Architecture

This section describes additional requirements for 48V peripheral subsystems.

Refer to section **10.1.6** for the attributes of 12V peripherals subsystems.

The 48V peripheral subsystem power architecture has the following attributes:

- 48V Peripheral subsystems can attach to any 48V PICPWR connector on the HPM or PDB that has the power capability to support loads of the peripheral subsystem.
- Individual 12V or 48V peripheral subsystems shall not be connected to more than one 48V PRIMARY or 12V PRIMARY domain.
- 48V PICPWR connectivity methods are dependent on system needs and connection type(s) supported at each 48V PICPWR location (e.g., card edge or a compatible cable).
- For cable applications with 48V PICPWR connectors, the PICPWR pinouts shall meet M-PIC pinout requirements.
- A 48V peripheral subsystem consists of a management subsystem, a power gating subsystem, and a power load.
- The 48V peripheral subsystem shall assume that the power rail supplied from the HPM will be operational in the ACPI-S5 power state. If the load on the peripheral subsystem is not intended to operate in the S5 domain, then the peripheral subsystem shall implement appropriate power gating for the load.
- Loads shall not be directly attached to 48V PICPWR connectors [e.g., PCIe AUX power cable attaching from 48V PICPWR to PCIe AIC (Add-In Card) is NOT supported]. Minimally, a power delivery management subsystem shall be implemented on the peripheral subsystem or the load that it is compatible with the 48V PICPWR sidebands and architecture.
- Peripherals may consume a small amount of power for inventory and sideband initialization prior to being transitioned to higher power states by the HPM. It is strongly recommended that peripheral designs minimize the initial power consumed. It is also recommended that system designers verify that the total system power consumed is within the total initial power available.
- Power gating can be implemented in a variety of forms including, but not limited to, load switches, hot-swap controller, voltage regulators. Peripherals shall include soft-start functionality to prevent inrush current greater than the connector DC current rating and 0.1A/us as peripherals are enabled and are powering up. Management of the Inrush current due to electrical shorts is optional.
- If any peripherals are powered by 48V PICPWR and 12V PICPWR connectors, inputs shall be isolated to prevent leakage from one voltage domain to the other.
- Per 48V PICPWR sideband set (composed of an SMBus interface, 2 required sidebands, 2 optional sidebands), the SMBus and the 2 required sidebands shall be provided to the peripheral subsystem enabling the HPM to perform status, control, and inventory.
- It is strongly recommended that peripheral designs balance current flow through PICPWR connectors in applications that source power through more than one 48V PICPWR connector (on HPM or on the peripheral) to prevent overloading one of the current paths.

- To avoid damage resulting from high currents in 48V PICPWR connectors during partial-mate conditions, it is recommended that HPM, PDB, and peripheral implementations use last to mate/1st to break SB pins to detect partial-mate conditions. HPMs (and PDB by extension) or Peripherals should also take the necessary actions to prevent high currents through PICPWR connectors (including per channel if a dual channel PICPWR connects to different loads) when a partial-mate condition exists.
- To avoid PICPWR connector damage resulting from high currents in partial-mate conditions, it is recommended that peripherals be designed to ensure they do not draw high currents by default if SB pins are not connected when 48V_PRIMARY is powered up.

Figure 32 shows additional details of the power architecture of a peripheral subsystem.

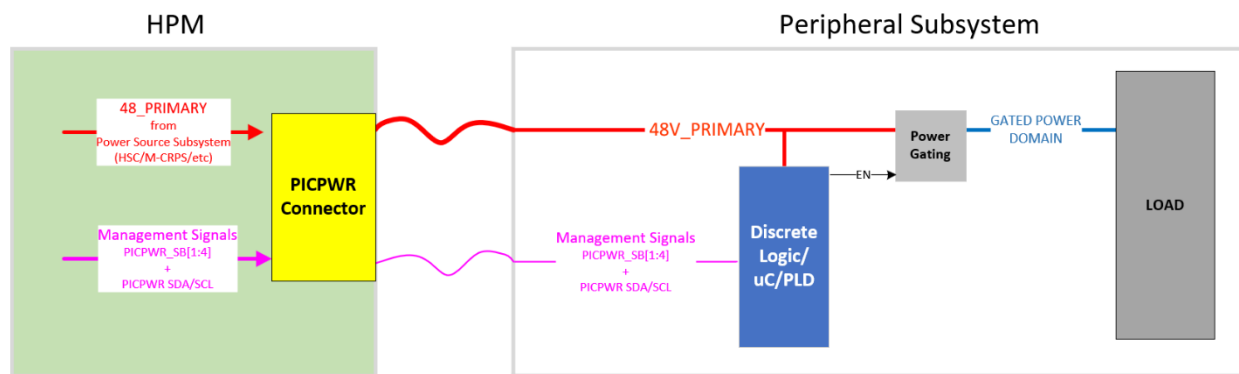


Figure 32: Peripheral Subsystem 48V Power Distribution Architecture Details

10.2.12. Dedicated 48V Supply Connector Pin Definition

Table 10: Dedicated 48V Supply Connector Pin Definition

Pin(s)	Signal Name	Signal Requirements
PWR	48V_SUPPLY	Input power rail from the power source subsystem used to power input control circuits that provide 48V_PRIMARY for downstream loads & logic on peripheral subsystem. <u>48V_SUPPLY shall be sourced by a 48V rack busbar (or equivalent), by the output of a 48V M-CRPS, or an upstream PDB sourced by the previous 2 sources. When 48V_SUPPLY is sourced by one or more 48V M-CRPS, +48V shall be powered in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).</u> <u>Connected circuits shall support up to 60V.</u> Implementation Notes: The maximum allowed voltage drop from the dedicated 48V supply connector to 48V PICPWR egress connectors

		is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in HPM design specification(s) for system configurations supported per HPM design. Refer to <i>Figure 8</i> for an example configuration showing voltage drop, measurement and set point. 48V_SUPPLY tolerance is based on the voltage source setpoint.
PWR	GND	Ground return for 48V_SUPPLY
Sense	Power Sense	This is a dual-purpose connection defined within the ORv3 base specification. <u>The connection shall be used to control the on and off behavior of the power entry circuitry (i.e., HSCs or switches) to ensure that 48V_SUPPLY load is not enabled until after the sense connection is detected and is un-loaded as soon as the sense connection is lost.</u> This connection can optionally be used with the power sense return to differentially measure the voltage at the source end of the input power cable (or interconnect) assembly. <u>Maximum current shall be limited to 1.5A continuous. Connected circuits shall support up to 60V.</u>
sense	Power Sense Return	Power Sense return path that can be used with the Power Sense to differentially measure the voltage at the source end of the input power cable (or interconnect) assembly. <u>Maximum current shall be limited to 1.5A continuous.</u>

ORv3 Implementation Notes:

- The chassis input voltage range may vary from either 46V to 52V or 52V to 56V.
- Nominal voltage supplied from an ORv3 48V busbar may be fixed at either 51V or 54V under no load and while in normal operation.

ORv2 Implementation Notes:

- The chassis input voltage range may vary from 40V to 59.5V.
- Nominal voltage supplied from an ORv2 48V busbar may be fixed at 54.5V under no load and while in normal operation.
- If the source is an ORv2 clip and cable assembly, the Power Sense Return shall be connected from the dedicated 48V supply connector to the power return in the cable assembly or at the busbar clip.

Peripheral and HPM compatibility Implementation Notes:

- Designers should consider creating HPMs and peripherals with lower minimum operating voltages, ideally around 40V, because of the 40V lower threshold's compatibility with a broader range of 48V rack sources. When deciding to design for 40V designers should weigh trade-offs (such as cost or performance per watt) against the benefits of broader compatibility.
- Refer to *Figure 33* for a comparison of three typical 48V rack voltage output voltage ranges to IT Gear (HPM, PDB, and peripherals) input voltage ranges.

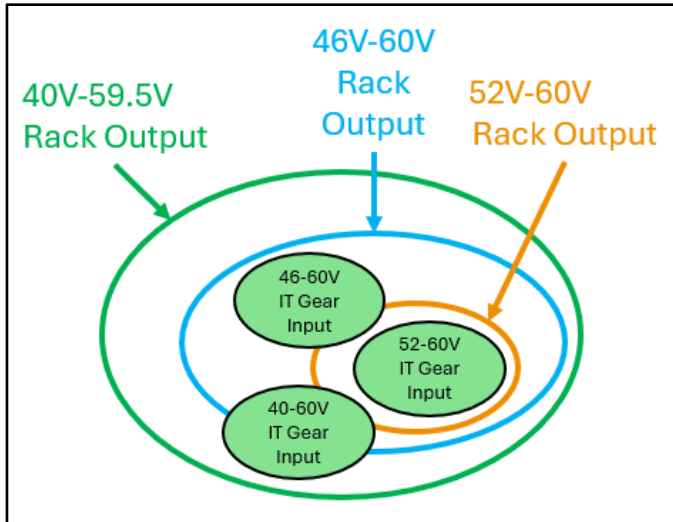


Figure 33: Input Voltage vs Rack Voltage Compatibility

10.2.12.1. Dedicated 48V Supply Connector 2x6+2 Vertical Header Pinout

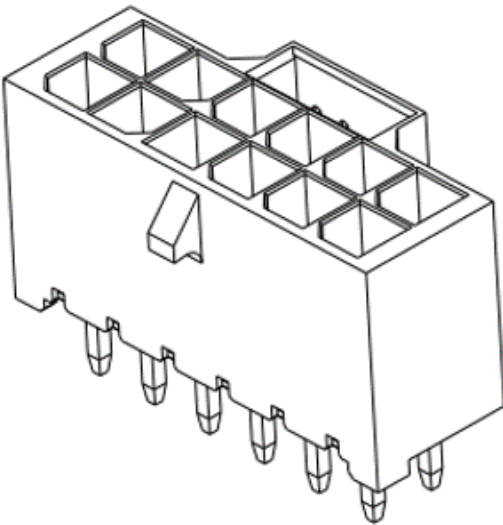


Figure 34: Dedicated 48V Supply Connector 2x6+2 Vertical Header Pinout

Notes:

- Connector power rating shall be: 3312W (12A per power pin) at 46V.
- Sense circuits shall support 1.5A continuous.
- Connector shall be pinned out per Table 11.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 11: Dedicated 48V Supply Connector 2x6+2 Pinout

Pin(s)	Signal Name
Circuits [1:6]	GND
Circuits [7:12]	48V_SUPPLY
Sense1	POWER_SENSE
Sense2	POWER_SENSE_RETURN

Dedicated 48V supply connector 2x6+2 physical pin numbering shall be implemented per *Figure 32*.

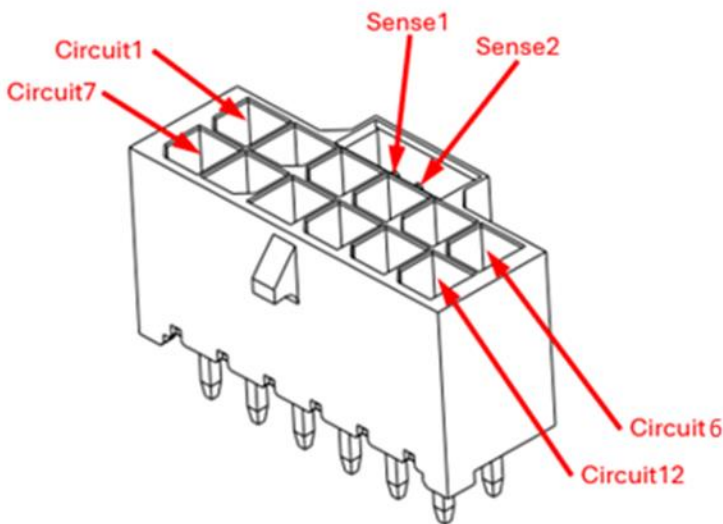


Figure 35: Dedicated 48V Supply Connector 2x6+2 Physical Pin Numbering

10.2.13. 48V PICPWR Connector Pin Definition

Table 12: 48V PICPWR Connector Pin Definition

Pin(s)	Signal Name	Signal Requirements
PWR	48V_PRIMARY	Primary power rail from the power source subsystem used to power downstream loads & logic on peripheral subsystem. <u>48V_PRIMARY shall be sourced by a ramp-controlled 48V source. 48V_PRIMARY and powered in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).</u> <u>Circuits shall support up to 60V.</u>

		Implementation Notes: The maximum allowed voltage drop from the dedicated 48V supply connector to 48V PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading, and maximum allowed voltage drop are expected to be defined in HPM design specification(s) for system configurations supported per HPM design. Refer to <i>Figure 8</i> for an example configuration showing voltage drop, measurement and set point. <u>48V_PRIMARY tolerance is based on the voltage source setpoint.</u>
PWR	GND	Ground return for 48V_PRIMARY and side-band signals
SB1:4	PICPWR _n _SB[4:1]	<u>Sideband GPIOs for status, control, and inventory of peripheral subsystem; shall be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages.</u> For electrical requirements see sections 12 and 12.1 as well as <i>Table 3</i> and <i>Figure 9</i>. The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use PICPWR_SB1 for PRES_N or PESTI functionality and use PICPWR_SB2 as active high power enable or for PWREN (power enable) functionality. PICPWR_SB[4:3] terminations and connections are optional and may be omitted if not used.
SB5	PICPWR _n _SCL	See sections 12 and 12.2. for SMBus and I3C electrical requirements.
SB6	PICPWR _n _SDA	

10.2.13.1. 48V 2x6+12SB PICPWR Right-angle Header Pinout

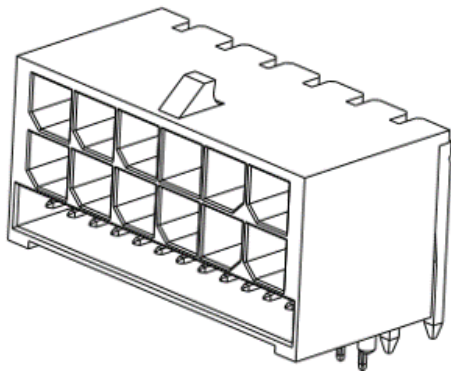


Figure 36: 48V 2x6+12SB Right-angle Header

Notes:

- Connector power rating shall be: 3312W (12A per power pin) at 46V.
- Connector shall support current excursions shorter than 1 second where the maximum currents for all excursion windows are less than 5 times the nominal connector current rating, provided the RMS current over all periods of 1 second or more do not exceed the nominal current rating.
- This connector shall have two independent channels of PICPWR sideband management signals.
- Connector shall be pinned out per *Table 13*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 13: 48V 2x6+12SB PICPWR Right-angle Header Pinout

Pin(s)	Signal Name
Circuits [1:6]	GND
Circuits [7:12]	48V_PRIMARY
SB1	PICPWR[n+1]_SB1
SB2	PICPWR[n+1]_SB2
SB3	PICPWR[n+1]_SB3
SB4	PICPWR[n+1]_SB4
SB5	PICPWR[n+1]_SCL
SB6	PICPWR[n+1]_SDA
SB7	PICPWR _n _SB1
SB8	PICPWR _n _SB2
SB9	PICPWR _n _SB3
SB10	PICPWR _n _SB4
SB11	PICPWR _n _SCL
SB12	PICPWR _n _SDA

2x6+12SB physical connector pin numbering shall be implemented per *Figure 37*.

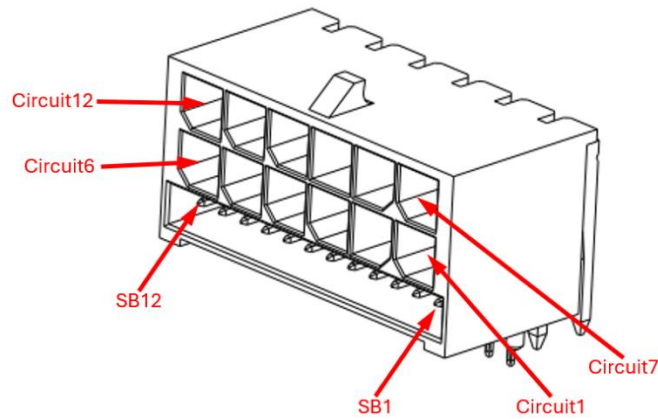


Figure 37: 48V 2x6+12SB Physical Pin Numbering

10.2.13.2. 48V 2x6+12SB PICPWR Vertical Header Pinout

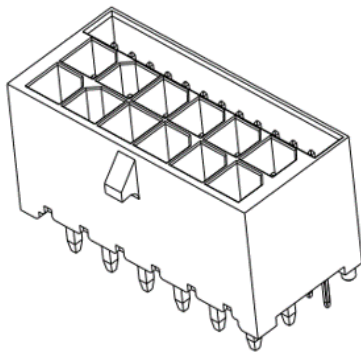


Figure 38: 48V 2x6+12SB Vertical Header

Notes:

- Connector power rating shall be: 3312W (12A per power pin) at 46V.
- Connector shall support current excursions shorter than 1 second where the maximum currents for all excursion windows are less than 5 times the nominal connector current rating, provided the RMS current over all periods of 1 second or more do not exceed the nominal current rating.
- This connector shall have two independent channels of PICPWR sideband management signals.
- Connector shall be pinned out per *Table 14*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 14: 48V 2x6+12SB PICPWR Vertical Header Pinout

Pin(s)	Signal Name
Circuits [1:6]	GND
Circuits [7:12]	48V_PRIMARY
SB1	PICPWR[n+1]_SB1
SB2	PICPWR[n+1]_SB2
SB3	PICPWR[n+1]_SB3
SB4	PICPWR[n+1]_SB4
SB5	PICPWR[n+1]_SCL
SB6	PICPWR[n+1]_SDA
SB7	PICPWR _n _SB1
SB8	PICPWR _n _SB2
SB9	PICPWR _n _SB3
SB10	PICPWR _n _SB4
SB11	PICPWR _n _SCL
SB12	PICPWR _n _SDA

2x6+12SB physical connector pin numbering shall be implemented per Figure 37.

10.2.13.3. 48V 2x3+6SB PICPWR Right-angle Header Pinout

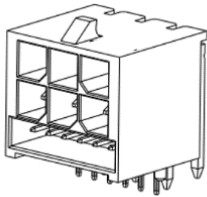


Figure 39: 48V 2x3+6SB Right Angle Header

Notes:

- Connector power rating shall be: 1863W (13.5A per power pin) at 46V.
- Connector shall support current excursions shorter than 1 second where the maximum currents for all excursion windows are less than 5 times the nominal connector current rating, provided the RMS current over all periods of 1 second or more do not exceed the nominal current rating.
- This connector shall have one channel of PICPWR sideband management signals.
- Connector shall be pinned out per Table 15.

- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 15: 48V 2x3+6SB Right-angle Header Pinout.

Pin(s)	Signal Name
Circuits [1:3]	GND
Circuits [4:6]	48V_PRIMARY
SB1	PICPWR _n _SB1
SB2	PICPWR _n _SB2
SB3	PICPWR _n _SB3
SB4	PICPWR _n _SB4
SB5	PICPWR _n _SCL
SB6	PICPWR _n _SDA

48V 2x3+6SB physical connector pin numbering shall be implemented per *Figure 40*.

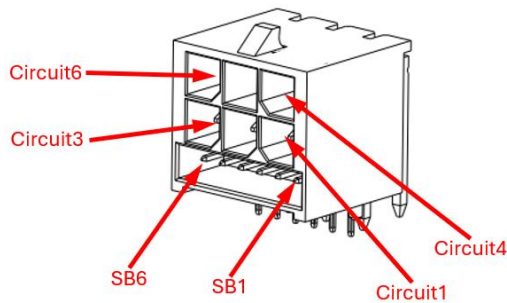


Figure 40: 48V 2x3+6SB Physical Pin Numbering

10.2.13.4. 48V 2x3+6SB PICPWR Vertical Header Pinout

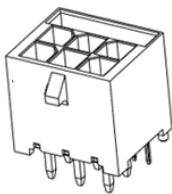


Figure 41: 48V 2x3+6SB Vertical Header

Notes:

- Connector power rating shall be: 1863W (13.5A per power pin) at 46V.
- Connector shall support current excursions shorter than 1 second where the maximum currents for all excursion windows are less than 5 times the nominal connector current rating, provided the RMS current over all periods of 1 second or more do not exceed the nominal current rating.
- This connector shall have one channel of PICPWR sideband management signals.

- Connector shall be pinned out per *Table 16*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 16: 48V 2x3+6SB PICPWR Vertical Header Pinout

Pin(s)	Signal Name
Circuits [1:3]	GND
Circuits [4:6]	48V_PRIMARY
SB1	PICPWR _n _SB1
SB2	PICPWR _n _SB2
SB3	PICPWR _n _SB3
SB4	PICPWR _n _SB4
SB5	PICPWR _n _SCL
SB6	PICPWR _n _SDA

48V 2x3+6SB physical connector pin numbering shall be implemented per *Figure 40*.

10.2.14. PDB Management Connectors

This section defines connections for HPMs used with a PDB. The connectors provide +12VStby, analog connections (used to monitor current and voltage from the M-CRPS modules on the PDB), and management signals for PDB. This section defines the minimum standard set of signals required for PDB management for the two standardized configurations (i.e., Type 1 and Type 2). If needed, additional signals may be added in an adapted HPM.

Even though M-PIC does not dictate cable construction, it is expected that PDB management cable constructions will connect from source side A to destination side A to ensure interoperability among HPMs and PDBs.

10.2.14.1. PDB Management Connector Type 1

The PDB Management Connector described in this section shall be used for HPM to PDB connections that use the PICPWR sideband management signals along with the PDB management cable to manage the PDB. If PDB designers intend to support HPMs with Type 1 and Type 2 PDB management cables, PDB Type 2 may be implemented, as it is the superset.

Type1 PDB management connector signals shall be implemented per *Table 17*.

Table 17: PDB Management Connector Type1 Pin Definition

Signal Name	Description	Spec	Notes
12V_STBY	12V Standby management power	12V +/-5% Up to 6 Amps	
IMON	Shared current monitor signal that represents the total output current for all shared power supplies.	Refer to <i>Table 28</i>	
VMON	Voltage-monitor output signal from PDB circuit.		
GND	Ground return for 12V_STBY and side-band signals	Up to 6 Amps	
SLoad	SGPIO load signal to PDB	Refer to sections 12 and 12.6 for SGPIO electrical requirements and protocol.	The SGPIO interface provides a low latency path from HPM to PDB for IO expansion on PDB.
SDataOut	SGPIO data signal from HPM to PDB		
SDataIn	SGPIO data signal from PDB to HPM		
SClock	SGPIO clock to PDB		
PMBUS_SCL	PMBus from DC-SCM BMC for PSU management/updates.	See sections 12 and 12.3 for PMBus electrical requirements.	The PMBus interface does not support I3C.
PMBUS_SDA			
FULL_PWR_CYCLE_N /FLEXIO	<u>Default signal usage on the HPM shall be an active low, open drain signal that is only pulled down to initiate a power cycle of PDB logic and all downstream 12V_STBY logic.</u> If the default signal usage is not needed (i.e., default usage circuits not implemented) on the PDB and HPM, only after negotiation between the HPM and PDB, the signal may be used as an alternate function (FLEXIO).	See section 12.1 for electrical requirements. It is recommended that HPM logic ensure 12V_PRIMARY is fully drained before asserting FULL_PWR_CYCLE_N. <u>A pullup circuit (equivalent to 10k ohms) on FULL_PWR_CYCLE_N /FLEXIO to 12V_STBY_PDB shall be on the PDB.</u>	

Refer to *Figure 42* for an example FULL_PWR_CYCLE_N architecture diagram.

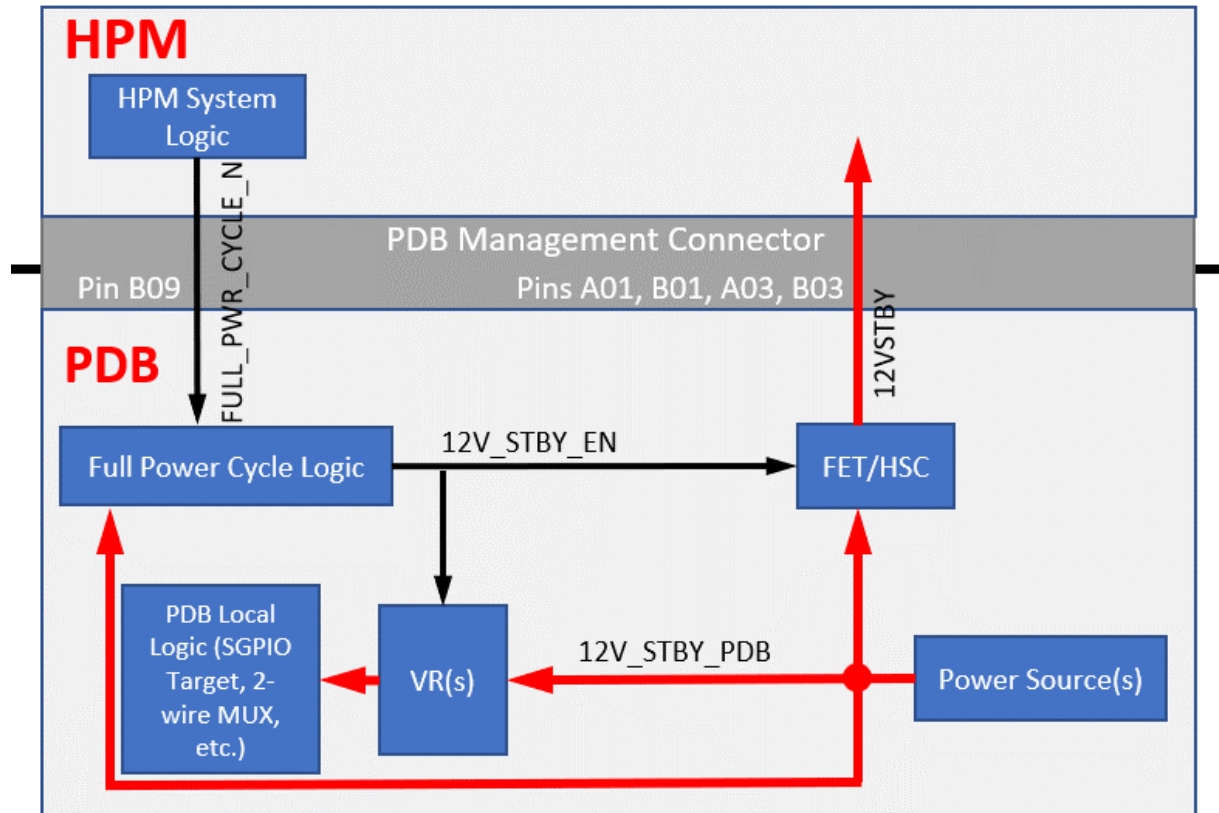


Figure 42: Example FULL_PWR_CYCLE_N Architecture Diagram

The following is an example of Full Power Cycle Logic:

On power up, a reset monitor holds 12V_STBY_EN low until:

- 12V_STBY_PDB Input voltage is in regulation AND
- FULL_PWR_CYCLE_N is de-asserted AND
- $\geq 600\text{ms}$ has passed for bleed off.

If FULL_PWR_CYCLE_N is asserted at any point in time, the reset monitor should get reset (12V_STBY_EN goes low, and delay starts at 0).

The following are examples of additional features implementers may add:

- PDB Logic to sequence; drainage of 12V_Primary, drainage of 12V_STBY and locally derived rails, then re-asserting 12V_STBY_EN).
- PMBUS accessed I/O to override PSU enable controls.
- Logic to limit assertion of FULL_PWR_CYCLE_N to times when system logic knows that the 12V_PRIMARY source has been removed for a sufficient period.

Table 18: HPM PDB Management Connector Type1HPM Pinout

Pin	Signal Name	Signal Name	Pin
A01	+12V_STBY	+12V_STBY	B01
A02	IMON	VMON	B02
A03	+12V_STBY	+12V_STBY	B03
A04	GND	GND	B04
A05	SLoad	SClock	B05
A06	SDataOut	GND	B06
A07	GND	SDataIn	B07
A08	PMBUS_SCL	GND	B08
A09	PMBUS_SDA	FULL_PWR_CYCLE_N/FLEXIO	B09

Vertical Type1 PDB management connector physical pinout shall be implemented per *Figure 43*.

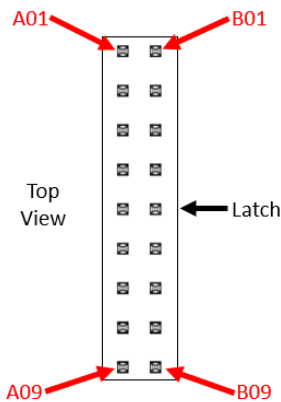


Figure 43: 2x9 Vertical Type1 PDB Management Connector Physical Pinout

2x9 Vertical Header

Notes:

- Connector current rating shall be: 2A per contact.
- Connector shall be pinned out per *Table 18*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

10.2.14.2. PDB Management Connector Type 2

The PDB Management Connector described in this section shall be used for HPM to PDB connections that do not power the HPM and manage the PDB using PICPWR connections (i.e., use a dedicated supply connector that does not include sideband management signals). The HPM PDB management connector type 2 includes additional management signals to account

for the management signals that were present in the Type1 PICPWR cables but are not present in dedicated supply connectors.

The Type2 PDB management connector signals shall be implemented per [Table 19](#).

Table 19: PDB Management Connector Type2 Pin Definition

Signal Name	Description	Spec	Notes
12V_STBY	12V Standby management power	12V +/-5% Up to 6 Amps	
IMON	Shared current monitor signal that represents the total output current for all shared power supplies.	Refer to <i>Table 28</i>	
VMON	Voltage-monitor output signal from PDB circuit.		
GND	Ground return for 12V_STBY and side-band signals		
SLoad	SGPIO load signal to PDB	Refer to sections 12 and 12.6 for SGPIO electrical requirements and protocol.	The SGPIO interface provides a low latency path from HPM to PDB for IO expansion on PDB.
SDataOut	SGPIO data signal from HPM to PDB		
SDataIn	SGPIO data signal from PDB to HPM		
SClock	SGPIO clock to PDB		
PMBUS_SCL	PMBus from DC-SCM BMC for PSU management/updates.	See sections 12 and 12.3 for PMBus electrical requirements.	The PMBus interface does not support I3C.
PMBUS_SDA			
FULL_PWR_CYCLE_N/FLEXIO	<u>Default signal usage on the HPM shall be an active low, open drain signal that is only pulled low to initiate a power cycle of PDB and all downstream 12V_STBY logic.</u> If the default signal usage is not needed on the PDB and HPM (i.e., default usage circuits not implemented), only after negotiation between the HPM and PDB, the signal may be used as a FLEXIO.	See sections 12.1 for electrical requirements. It is recommended that HPM logic ensure 48V_PRIMARY and 12V_PRIMARY rails are fully drained before asserting FULL_PWR_CYCLE_N. <u>A pullup circuit (equivalent to 10k ohms) on FULL_PWR_CYCLE_N/FLEXIO to 12V_STBY PDB shall be on the PDB.</u>	<u>In configurations requiring a full power cycle where both HPM and PDB provide +12VStby, HPM shall initiate a power cycle of its 12V_STBY supply when HPM asserts FULL_PWR_CYCLE_N to PDB.</u>
PDB_MGMT_[2:1]_SCL	SMB/I3C interfaces for PDB and/or downstream PICPWR connector management.	See section 12 and 12.2 for SMBus and I3C electrical requirements.	
PDB_MGMT_[2:1]_SDA			
PDB_MGMT_[2:1]_SB1	SB interfaces for PDB or downstream PICPWR connector management.	Sideband GPIOs for status, control, and inventory of PDB and/or	

		down-stream peripheral subsystems; <u>shall be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages.</u> For electrical requirements see sections 12 and 12.1 as well as <i>Table 3</i>, and <i>Figure 9</i>. The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between PDBs, it is recommended to use PDB MGMT_[2:1]_SB1 if PESTI functionality is desired for PDB or peripherals down-stream of PDB.	
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Table 20: HPM PDB Management Connector Type2 Pinout

Pin	Signal Name	Signal Name	Pin
A01	+12V_STBY	+12V_STBY	B01
A02	IMON	VMON	B02
A03	+12V_STBY	+12V_STBY	B03
A04	GND	GND	B04
A05	SLoad	SClock	B05
A06	SDataOut	GND	B06
A07	GND	SDataIn	B07
A08	PMBUS_SCL	GND	B08
A09	PMBUS_SDA	FULL_PWR_CYCLE_N/FLEXIO	B09
A10	PDB_MGMT_1_SB1	PDB_MGMT_2_SB1	B10
A11	PDB_MGMT_1_SDA	PDB_MGMT_2_SDA	B11
A12	PDB_MGMT_1_SCL	PDB_MGMT_2_SCL	B12

Vertical Type2 PDB management connector physical pinout shall be implemented per *Figure 44*.

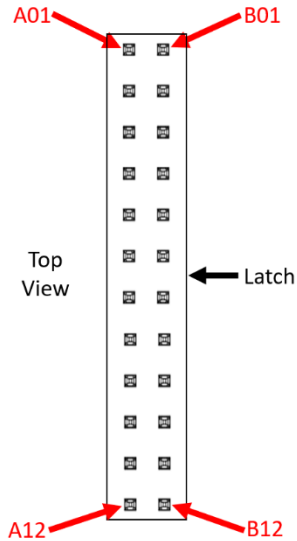


Figure 44: 2x12 Vertical Type2 PDB Management Connector Physical Pinout

2x12 Vertical Header

Notes:

- Connector current rating shall be: 2A per contact.
- Connector shall be pinned out per Table 20.
- The following link contains documentation of connector vendors and part numbers:

[Current Connector List](#)

10.3. Coin Cell Battery

HPM shall implement battery backed voltage interface per DC-SCM R2.x “Battery Voltage” requirement.

11. IO System

11.1. Boot Storage

This section defines an optional cable optimized interface for a boot/storage peripheral and two options for direct attach boot storage. This subsystem is typically implemented as 1 or 2 M.2 media devices (or similar) and may include a RAID 1 controller. However, with potential changes in the storage ecosystem, M-PIC also provides the option to use E1 storage devices. PCIe generational/speed requirements are not provided by this specification.

11.1.1. Cable Optimized Boot Peripheral

If present, the cable optimized peripheral interface is comprised of a SFF-TA-1036 connector with optimized power, signals, and connector form factor to work in FLW and DNO form factors.

Cable optimized boot peripheral implementations shall be either the power control method in section 11.1.1.1 or 11.1.1.2. PICPWR sideband signals are not part of the pinout because 12V boot power is managed using a switch on the HPM or using the PWRDIS signal to the device. Multiple HPMs sharing a single boot storage peripheral is outside the scope of this specification.

11.1.1.1. Power Control Switch on the HPM

This implementation was required for cable optimized boot peripherals defined up through M-PIC V1.02. If implementing the power control switch on the HPM:

- 12V power provided to the connector “12V” shall be sourced from 12V PRIMARY through a power switch.
- HPM shall control the power to the cable optimized boot peripheral using the switch on the HPM. The use of the PWRDIS signal is optional.

Because this configuration implements the switch on the HPM, it is forward compatible cable optimized boot peripherals that meet the requirements in section 11.1.1.2.

11.1.1.2. Power Control Using the PWRDIS Signal

Because SFF-TA-1009 compliant devices are required to support the ability to enable/disable their loads using the PWRDIS functionality, when using a SFF-TA-1009 compliant device, the switch on the HPM is a duplicate. To avoid requiring duplicate switches and to follow the “pay as you go” model for feature costs, this option allows designers to move the gating from the HPM to the cable optimized boot peripheral. If implementing power control using the PWRDIS signal:

- 12V power to the cable optimized boot peripheral connector shall be powered by 12V PRIMARY.
- HPM shall implement the PWRDIS signal to control the 12V power loading on the cable optimized peripheral.
- Cable optimized boot peripherals shall support controlling its primary 12V loads using the PWRDIS signal input from HPM.
- Management 12V loads may remain powered when PWRDIS is enabled.
- **Because cable optimized boot peripherals designed per section 11.1.1.1 are not compatible with HPMs without the power switch, it is recommended system designers consider the compatibility implications and ensure that implementations using PWRDIS are available at the same time.**

11.1.1.3. Cable Optimized Boot Peripheral Connector

The SFF-TA-1036 connector pin definition shall be implemented per Table 21.

Table 21: SFF-TA-1036 Connector Pin Definition

Signal Name	Description	Spec	Notes
12V or 12V_PRIMARY	12V power	12V +/-5% Up to 48W	12V (sourced from 12V_PRIMARY though a switch on HPM) or 12V_PRIMARY (when S0 power is controlled using PWRDIS)
GND	Ground return for 12V power and signals		
3p3_AUX_MGMT	3p3_AUX_MGMT is derived from 12VStby (if available).	Up to 200 mA (if provided)	This connection is optional. EDSFF devices are limited to 25 mA.
PETp0, PETn0 PETp1, PETn1 PETp2, PETn2 PETp3, PETn3	Root Port TX signals	Defined by the PCI Express Card Electromechanical Specification.	Support x1, x2, or x4 configurations
PERp0, PERn0 PERp1, PERn1 PERp2, PERn2 PERp3, PERn3	Root Port RX signals	Defined by the PCI Express Card Electromechanical Specification.	Support x1, x2, or x4 configurations
REFCLK_Dp0, REFCLK_Dn0	100 MHz PCIe reference clock	Defined by PCIe Base Specification.	
PERST0_N	PCIe fundamental reset to the device.	Defined as PERST# by the PCI Express Base Specification.	
REFCLK_Dp1, REFCLK_Dn1	100 MHz PCIe reference clock	Defined by PCIe Base Specification.	Used only if DUALPORTEN_N IS LOW
PERST1_N	PCIe fundamental reset to the device.	Defined as PERST# by the PCI Express Base Specification.	Used only if DUALPORTEN_N IS LOW
PESTI_PRES_N / PRSNT0_N	Peripheral Presence detection signal with the option for PESTI communication with the peripheral.	<u>This signal shall be connected to HPM FPGA with the prescribed terminations for PICPWR_SB1. For electrical requirements. See sections 12 and 12.1 as well as Table 3 and Figure 9.</u>	

SMB_SCL, SMB_SDA	SMBus management interface	See sections 12 and 12.2. for SMBus electrical requirements.	This interface does not support I3C.
SMBRST_N	SMBus reset	Defined by the SFF-TA-1009 Rev 3.0 Specification.	Reset for the management interface.
DUALPORTEN_N	Dual port enable signal	Defined by the SFF-TA-1009 Rev 3.0 Specification.	
LED	LED signal	Defined by the SFF-TA-1009 Rev 3.0 Specification.	
PWRDIS (Power Disable)	Power Disable Signal	Defined by the SFF-TA-1009 Rev 3.0 Specification.	
FLEXIO	Non-EDSFF device flexible use signal	<u>Shall be connected to HPM FPGA. Shall not include external pull up, pull down, or HPM intentionally applying a bias until after discovery and negotiation complete.</u> See section 12 for electrical requirements. WARNING: Recommend to <i>not</i> wire this signal directly to an EDSFF device signal MFG, pin #B7. See SFF TA-1009 Rev 3.0 Specification for Device's MFG use.	Instead of making this pin a "No Connect," it is connected to the HPM FPGA for proprietary use as desired by implementor. Discovery and the mechanism of negotiation is out of the scope of this specification but could be done by either 2 wire management bus or 1 wire management bus.
RFU	Reserved for Future Use	Defined by the SFF-TA-1009 Rev 3.0 Specification.	



Figure 45: Rendering of the SFF-TA-1036 Connector

Notes:

- Mated connector 12V current rating shall be 4A. Refer to *Figure 46*.
- Rated signal pin current shall be 0.65A per differential pair contact and 0.30A per single ended contact.
- The SFF-TA-1036 connector on HPM shall be pinned out per *Table 22*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

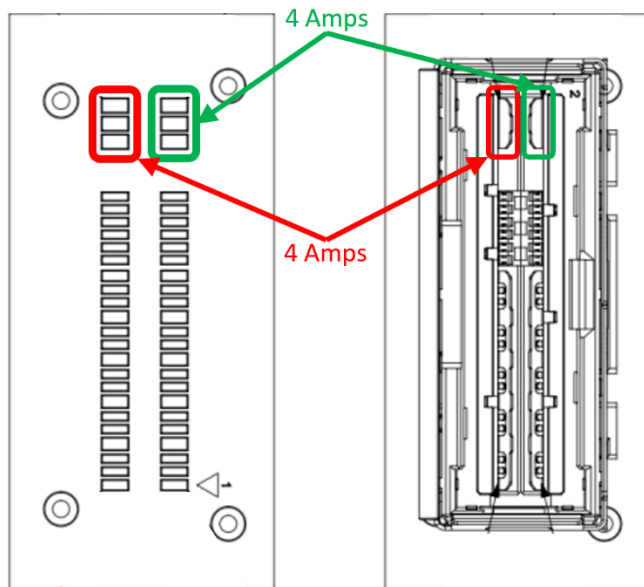


Figure 46: SFF-TA-136 Connector Current Rating

Table 22: SFF-TA-1036 Connector Pinout

Pin	Signal Name	Signal Name	Pin
26	12V	GND	25
27	12V	GND	24
28	12V	GND	23
29	FLEXIO	SMB_SCL	22
30	RFU	SMB_SDA	21
31	DUALPORTEN_N	SMBRST_N	20
32	PERST0_N	LED	19
33	3.3V AUX	PERST1_N	18
34	PWRDIS	PESTI_PRES_N / PRSENT0_N	17
35	GND	GND	16
36	REFCLKn0	REFCLKn1	15
37	REFCLKp0	REFCLKp1	14
38	GND	GND	13
39	PETn0	PERn0	12
40	PETp0	PERp0	11
41	GND	GND	10
42	PETn1	PERn1	9
43	PETp1	PERp1	8
44	GND	GND	7
45	PETn2	PERn2	6
46	PETp2	PERp2	5
47	GND	GND	4
48	PETn3	PERn3	3
49	PETp3	PERp3	2
50	GND	GND	1

The pinout in *Table 22* is for the HPM fixed side connector footprint only. It is recommended that system implementers pay special attention to the cable construction and the connector at the far end of the mated cable assembly since both affect the pinout at the far end of the mated cable assembly.

The SFF-TA-1036 physical pin numbering on HPM shall be implemented per *Figure 47*.

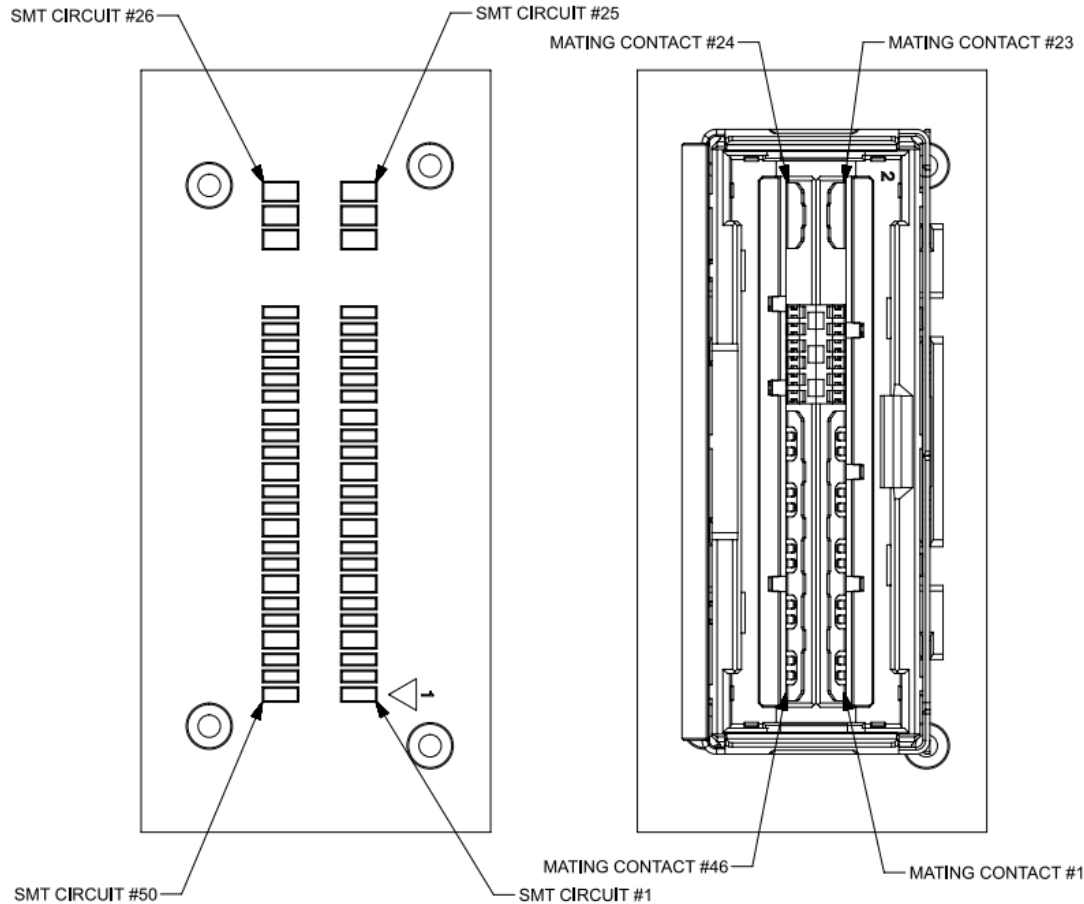


Figure 47: SFF-TA-1036 Connector Physical Pin Numbering

11.1.2. Direct Attach Boot Storage

HPMs may implement an integrated boot storage subsystem directly on the HPM.

11.1.2.1. M.2 Direct Attach Boot Storage

If M.2 direct connect storage media is implemented on HPM, it shall be a right-angle Socket 3 (Mechanical Key M) connector following the PCI Express M.2 Specification Revision 4.0, Version 1.0 pinout. HPMs have the option to connect from HPM FPGA to M.2 connector pin 1 with a pullup to 3.3V Aux (Available from S5) for M.2 device presence detection.

11.1.2.2. E1.S Direct Attach Boot Storage

If E1.S direct connect storage media is implemented on HPM, it shall be a right-angle SFF-TA-1002 connector following SFF-TA-1009 Rev 3.1 pinout.

11.2. Intrusion Switch

HPM form factors supporting an intrusion switch shall be implemented as follows:

- 1x3 Vertical header
 - The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)
- The signal HPM_SCM_INTRUSION_N is routed directly between header and DC-SCM without other circuit connectivity. Polarity of the HPM_SCM_INTRUSION_N has an active low indicating intrusion.
- Presence-detect signal routed to HPM's FPGA and called Intrusion_Cable_Pres_N
- Electrical details of HPM_SCM_INTRUSION_N are defined in the DC-SCM 2.x specifications.

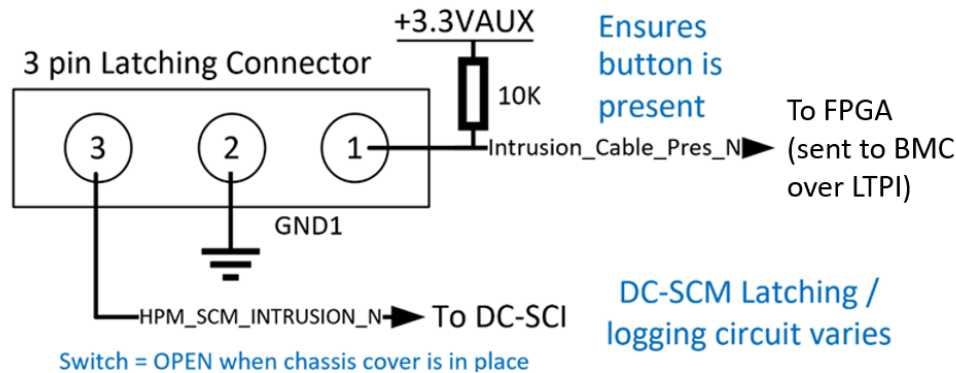


Figure 48: Intrusion Switch Pinout and Connectivity

Intrusion switch header physical header pin numbering shall be implemented per *Figure 49*.

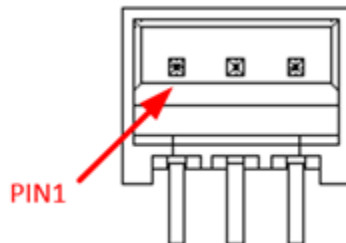


Figure 49: Intrusion Switch Header Physical Pin Numbering

11.3. Internal Host USB3 Connector

If the HPM includes only one internal host USB3.1 connector (internal port), it shall be either a vertical type A or vertical type C connector. Type A is recommended to achieve maximum modularity. Refer to *Figure 50* for an example of USB connectivity.

Usage examples include control panel expansion, debug, or an internal key. Physical presence, location, and envelope / keep out of the attached device or cable exit are to be defined by individual HPM form factor specifications. The location (HPM or DC-SCM) for the USB3 source and additional USB connectors located on the HPM are outside the scope of this specification.

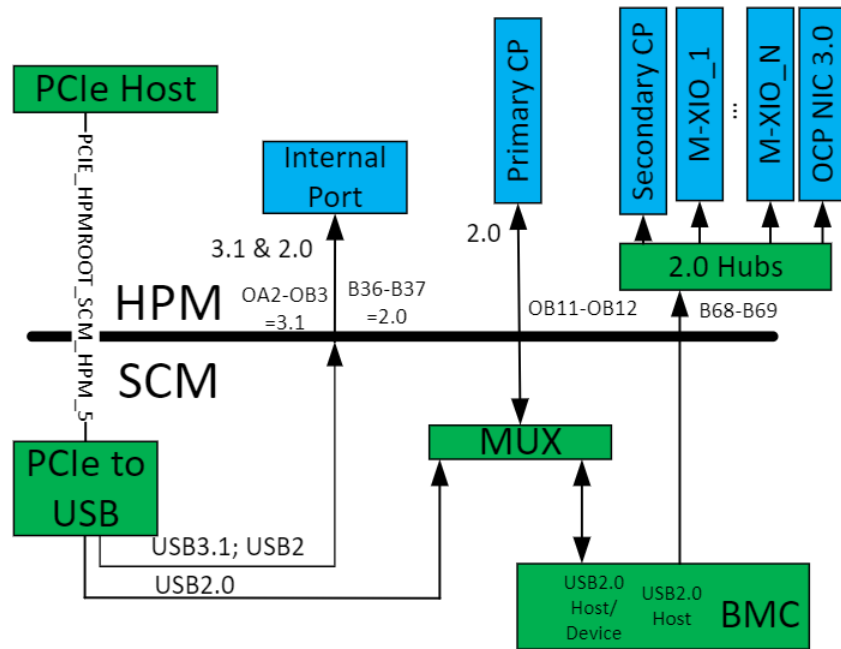


Figure 50: Example of a High-Level USB Diagram

11.4. Control Panel Interfacing

The primary function of a control panel is to enable users to interact with the system while they are physically present in front of the chassis. If the HPM form factor includes a single control, then it shall be the Primary Control Panel (PCP) connector. If an HPM form factor includes two control panels, the additional control panel shall be the Secondary Control Panel (SCP) connector. Connecting multiple HPMS to a single control panel is outside the scope of this specification.

To ensure the control panel is powered as early as possible, the power shall be sourced by the output of the 12V management switching circuit.

Due to the increased management complexity possible on the primary control panel, SB[4:3] are not optional on PCP but are optional on SCP. If SCP SB[4:3] are not used, components and connections may be omitted.

If a separate USB3 connection is required in one or more control panels, the USB connections may be cabled from the Internal USB3 connector on the HPM described in section **11.3**.

Even though M-PIC does not dictate cable construction, it is expected that the control panel cable construction will connect from source side A to destination side A to ensure interoperability among HPMs and control panels.

11.4.1. Primary HPM to Control Panel Connector

Primary HPM control panel connector shall be implemented per *Table 23*.

Table 23: Primary HPM Control Panel Pin Definition

Signal Name	Description	Spec	Notes
12V_CP GND	Control panel power.	12V +/-8%, Up to 200mA before 12V_PRIMARY is sourced by +12V. Up to 1.4A after 12V_PRIMARY is sourced by +12V.	<u>12V_CP shall be derived from raw CRPS +12VStby (if available) but switched to 12V_PRIMARY when it is available.</u> Overcurrent protection for 12V_CP is recommended to prevent shorts from being passed to +12VStby and management subsystems.
[SMB/I3C]_BMC_SDA/SCL	From DC-SCM BMC	May be biased any time +3.3Vaux is present. See sections 12 and 12.2 for SMBus and I3C electrical requirements.	Used for temperature sensor, and/or other SMBus/I3C devices.
PCP_SB[4:1]	From HPM FPGA for GPIO expansion on control panel	May be biased any time +3.3Vaux is present. Use the same HPM topology, termination, and values as PCPWRn_SB[4:1] See sections 12 and 12.1 for electrical requirements. See <i>Figure 9</i> for topology. <u>SB[4:3] shall be implemented on HPM.</u>	<u>Sideband GPIOs for status, control, inventory, and/or other control panel functions shall be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages.</u> The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use PCP_SB1 for PRES_N or PESTI functionality and use PCP_SB2 as active high PWREN (power enable) functionality.
USB_PCP_DP/DN	<u>This connection is optional. If connected, it shall be a High Speed capable USB 2.0 interface.</u>	See sections 12 and 12.4 for electrical requirements. Refer to <i>Figure 50</i> for an example of PCP USB 2.0 connectivity.	Potential use cases: boot key, service port, keyboard, or mouse.

SPI	SPI bus from DC-SCM	HPM should be designed to support SPI operation at ≥ 33 MHz, but the system may operate at lower frequencies because of cable and control panel loading. See sections 12 and 12.1 for electrical requirements. 3.3V_VAUX signaling (in S5)	Higher speed bus for devices such as SPI flash. Use cases for a generic single I/O SPI from the control panel connector include control panel interfacing or interfacing to other subsystems via cable splitting. Example uses include but are not limited to attestation, update and recovery, service action setting restoration storage, smart bezels, etc. <u>HPM shall be the SPI controller source where:</u> <u>MOSI is an output from HPM.</u> <u>MISO is an input to HPM.</u>
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2x10 Vertical Header Notes:

- Connector current rating shall be: 1A per contact.
- Connector shall be pinned out per Table 24.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 24: Primary HPM Control Panel Pinout

Pin	Signal Name	Signal Name	PIN
1	12V_CP	GND	2
3	12V_CP	[SMB/I3C]_BMC_SDA	4
5	NC	[SMB/I3C]_BMC_SCL	6
7	GND	GND	8
9	USB2_PCP_DP	PCP_SB4	10
11	USB2_PCP_DN	PCP_SB3	12
13	GND	PCP_SB2	14
15	MISO	PCP_SB1	16
17	CS	GND	18
19	MOSI	CK	20

Physical pin numbering shall be implemented per Figure 51.

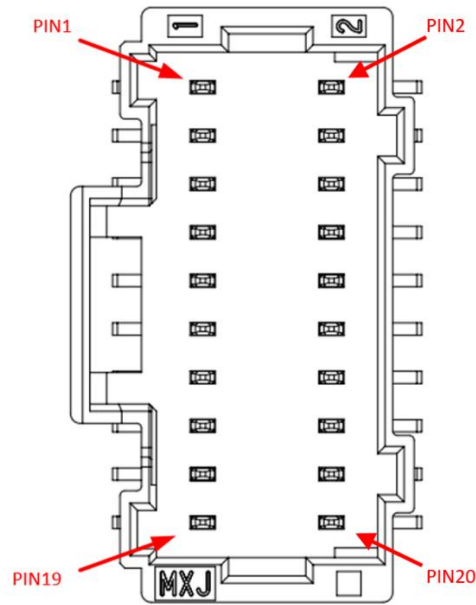


Figure 51: Control Panel Header Physical Pin Numbering

11.4.2. Secondary HPM to Control Panel Connector

Secondary HPM control panel connector shall be implemented per *Table 25*.

Table 25: Secondary HPM Control Panel Pin Definition

Signal Name	Description	Spec	Notes
12V_CP GND	Control panel power.	12V +/-8%, Up to 200mA before 12V_PRIMARY is sourced by +12V. Up to 1.4A after 12V_PRIMARY is sourced by +12V.	<u>12V_CP shall be derived from raw CRPS +12VStby (if available) but switched to 12V_PRIMARY when it is available.</u> Overcurrent protection for 12V_CP is recommended to prevent shorts from being passed to +12VStby and management subsystems.
[SMB/I3C]_BMC_SCP_SDA/SCL	From DC-SCM BMC	May be biased any time +3.3Vaux is present. See sections 12 and 12.2 for SMBus and I3C electrical requirements.	Used for temperature sensor, and/or other SMBus/I3C devices
SCP_SB[4:1]	From HPM FPGA for GPIO expansion on control panel	May be biased any time +3.3Vaux is present. Use the same HPM topology, termination, and	<u>Sideband GPIOs for status, control, inventory, and/or other control panel functions shall be connected to HPM FPGA with prescribed</u>

		values as P1CPWRn_SB[4:1]. SCP_SB[4:3] terminations and connections are optional and may be omitted if not used. See sections 12 and 12.1 for electrical requirements. See <i>Figure 9</i> for topology.	<u>terminations for “Plug-N-Code” specific usages.</u> The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use SCP_SB1 for PRES_N or PESTI functionality and use SCP_SB2 as active high PWREN (power enable) functionality. SB[4:3] terminations and connections are optional and may be omitted if not used.
USB_SCP_DP/DN	This connection is optional. <u>If connected, it shall be a High Speed capable USB 2.0 interface.</u>	See sections 12 and 12.4 for electrical requirements. Refer to <i>Figure 50</i> for an example of SCP USB 2.0 connectivity.	Potential use cases: boot key, service port, keyboard, or mouse.
RFU_[4:1]	RFU pins	<u>Shall not be Connected</u>	Reserved for Future Use

2x10 Vertical Header

Notes:

- Connector current rating shall be: 1A per contact.
- Connector shall be pinned out per *Table 26*.
- The following link contains documentation of connector vendors and part numbers:
[Current Connector List](#)

Table 26: Secondary HPM Control Panel Pinout

Pin	Signal Name	Signal Name	Pin
1	12V_CP	GND	2
3	12V_CP	[SMB/I3C]_BMC_SDA	4
5	NC	[SMB/I3C]_BMC_SCL	6
7	GND	GND	8
9	USB2_SCP_DP	SCP_SB4	10
11	USB2_SCP_DN	SCP_SB3	12
13	GND	SCP_SB2	14
15	RFU_1	SCP_SB1	16
17	RFU_2	GND	18
19	RFU_3	RFU_4	20

Physical pin numbering shall be implemented per *Figure 51*.

11.5. OCP NIC 3.0

See HPM form factor specifications for guidance on explicit OCP NIC variations supported (SFF, LFF, hot plug supported, etc.).

11.6. Smart NIC Management Interface

DC-MHS supports a method to interface with DPU/Smart NIC/IPU devices using required BMC domain USB 2.0 host controller signals through M-XIO connectors. See *Figure 50* for an example of USB high-level DC-SCM to M-XIO USB connectivity. Refer to the M-XIO base specification for details and usage.

11.7. DC-SCM Revision

DC-MHS is defined using the features and the form factor of DC-SCM revision 2.x. HPMs Shall implement DC-SCM Revision 2.x. Use of DC-SCM revision 1.0 is outside the scope of this specification.

Note: Even though DC-SCM does not require a new interface for HPM discovery, it is important for HPM designers to consult the DC-SCM revision 2.x specification for HPM discovery logic requirements.

12. Electrical Requirements

The destination subsystem shall be responsible for 1) electrical protection of local circuitry if the peripheral/subsystem is unpowered, 2) any cross-power domain isolation [such as when connecting MAIN powered only targets to the upstream AUX powered bus] and 3) any necessary voltage level translation in SMBus mode.

12.1. 3.3V Signaling Requirements

The 3.3V single-ended digital signals (PICPWRn_SB[4:1], [P/S]CP_SB[4:1], INTRUSION_CABLE_PRES_N, PESTI_PRES_N / PRSNT0_N, FLEXIO_FULL_PWR_CYCLE_N/FLEXIO, PDB_MGMT [2:1] SB1, and SPI) shall meet the electrical requirements in *Table 27*.

Table 27: 3.3V Logic Signal Requirements

Parameter	Symbol	Min	Max	Unit	Notes
High level input voltage	V _{IH}	2.0	3.465	V	
Low level input voltage	V _{IL}	-0.3	0.8	V	
High level output voltage	V _{OH}	2.3	3.465	V	
Low level output voltage	V _{OL}		0.2	V	
SPI High level input voltage	SPI V _{IH}	0.7 x VCC	VCC + 0.4	V	Care must be taken because SPI device VCC will have different sources.
SPI Low level input voltage	SPI V _{IL}	-0.3	0.8	V	
SPI High level output voltage	SPI V _{OH}	VCC – 0.2		V	
SPI Low level output voltage	SPI V _{OL}		0.4	V	Care must be taken because SPI device VCC will have different sources.

12.2. SMBus and I3C Signaling Requirements

SMBus, 3.3V, up to 400KHz or I3C Basic 1.1.1 mode, 1.8V, at higher speeds (I3C speeds vary based on overall topology and loading).

SMBus signals (named with SCL or SDA) logic levels shall be implemented per the System Management Bus (SMBus) Specification, Version 3.1.

For SMBus operation, a pullup to 3.3V upstream of the M-PIC defined connector shall be enabled. For I3C mode, the pullup shall be integrated in the I3C device upstream of the M-PIC defined connector, be configurable (start at 3.3V then go to 1.8V), and be transaction based.

For I3C basic recommended features, discovery, and a SMBus to I3C basic transition flow, refer to the informative “I3C Basic Implementation” section in the SFF-TA-1009 Specification Rev 3.1.

I3C signals (named with SCL or SDA) logic levels shall be implemented per the I3C Basic 1.1.1 Specification.

12.3. PMBus Signaling Requirements

PMBus, 3.3V, up to 400KHz.

PMBus signals (named with SCL or SDA) logic levels shall be implemented per the System Management Bus (SMBus) Specification, Version 3.2.

For PMBus operation, a pullup to 3.3V shall be provided.

PMBus does not support I3C mode.

12.4. USB Signaling Requirements

USB shall be implemented per the Universal Serial Bus Specification. Inputs and outputs shall be referenced from the signal destination's standpoint.

12.5. Imon and Vmon Signaling Requirements

Imon and Vmon analog signals shall meet the analog signaling requirements in Table 28.

Table 28: Imon and Vmon Voltage Signaling Requirements

Parameter	Min	Max (compliance mode)	Max (open circuit)	Unit	Notes
Analog Voltage Range	0	10.5	12.6	V	

12.6. SGPIO Requirements

This section describes signaling requirements for the low latency SGPIO interface between the HPM FPGA (initiator) and the PDB FPGA (target) if the HPM supports a PDB. The SGPIO interface is used for IO expansion on PDB.

12.6.1. SGPIO Protocol

The SGPIO interface has dedicated push-pull data signals going to (SDataOut) and from (SDataIn) the PDB. Both data paths transmit data at the same time.

Optionally, SDataIn may be used for physical PDB presence. If enabling PDB presence detection using the SDataIn signal, a 100k ohm 1% pullup to +3.3Vaux shall be located on the HPM (ensures the signal is high when PDB is not present) and a 10k ohm 1% pulldown shall be located on the PDB (ensures the signal is low when a PDB is present and SLoad is not low).

SLoad shall be a push-pull signal used to select the SGPIO target device and signal the start of the data transfer (starting with the first bit). When this signal is low, the SGPIO initiator and target shall clock out data. If the SLoad signal goes high before the data transfer is completed, then the transfer shall be aborted. When SLoad is high, the target data output shall be high impedance. If there is a mismatch between payload sizes (to HPM vs from HPM), it is recommended that the data sent be “0b” after the transfer is complete and while the SLoad signal is still low. To maximize commonality, the minimum SLOAD de-assertion is recommended to be a minimum of 3 clock cycles.

SClock shall be a push-pull signal used as the reference clock for the SGPIO interface. Data shall be clocked in on the falling edges of SClock. Because the latency between transactions (i.e., the time from SLOAD going low to the next time SLOAD can go low) depends on the total number of bits per transaction and the clock frequency, the SClock frequency supported by the HPM should be up to 25 MHz to provide flexibility for PDB designs.

Refer to *Figure 52* for an example of a SGPIO transaction waveform.

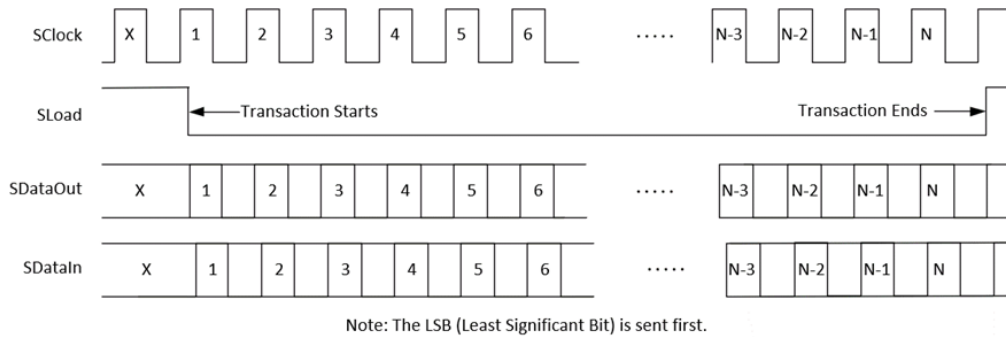


Figure 52: Example of a SGPIO Transaction Waveform

12.6.2. SGPIO Timing Requirements

The passive HPM interconnect shall be implemented per *Table 29*.

Table 29: HPM Passive Interconnect Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Skew between SClock and SLoad, SDataOut, and SDataIn signal lines on HPM	T_{SKEW}	-	10	ps	

The HPM SGPIO initiator device shall meet the timing requirements in *Table 30*.

Table 30: HPM SGPIO Initiator Device Timing Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
SClock Frequency	f_{CK}	5	25	MHz	HPM should be designed to support up to $f_{CK\ MAX}$, but the system may operate at lower frequencies because of cable and PDB implementations.
SClock Duty Cycle	t_{DUTY}	45	55	%	Measured at the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ of SClock
Rise time	t_R	-	6	ns	Measured from $V_{IL\ MAX}$ to $V_{IH\ MIN}$.
Fall time	t_F	-	6	ns	Measured from $V_{IH\ MIN}$ to $V_{IL\ MAX}$.
Setup time	t_{SU}	0	-	ns	Measured from $V_{IL\ MAX}$ for SLoad, SDataOut, and SDataIn to the midpoint between $V_{IH\ MIN}$ and

					$V_{IL\ MAX}$ (on the falling edge) of SClock
Hold time	t_H	2	-	ns	Measured from the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ (on the falling edge) of SClock to $V_{IL\ MAX}$ for SLoad, SDataOut, and SDataIn

12.6.3. SGPIO Voltage Requirements

The SGPIO signaling levels shall be compatible with 3.3V LVCMOS technology and meet the transmitter and receiver electrical requirements in *Table 31*.

Table 31: Transmitter and Receiver Electrical Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
IO Voltage	$V_{CC\ IO}$	3.135	3.465	V	
High level input voltage	V_{IH}	1.7	3.465	V	
Low level input voltage	V_{IL}	-0.3	0.8	V	
High level output voltage	V_{OH}	$V_{CC\ IO} - 0.4$	-	V	
Low level output voltage	V_{OL}	-	0.4	V	
IO Capacitance	$C_{I/O}$	-	8	pF	

13. References

This specification relies on the following specifications:

- OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
[OCP NIC Wiki](#)
- OCP Datacenter Secure Control Module (DC-SCM) Revision 2.x – Specifies a DC-SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
[DC-SCM Specs and Designs Wiki](#)
- Open Rack/Specs and Designs – Specifies ORv3 and ORv2 requirements as well as provides designs and reference files.
[Open Rack/SpecsAndDesigns](#)
- SMBus Management Interface Forum. System Management Bus (SMBus) Specification. System. Management Interface Forum, Inc, Version 3.1, 19 Mar 2018.
- USB Implementers Forum. Universal Serial Bus Specification, Revision 2.0, April 27th, 2000
- MIPI alliance Specification for I3C BasicSM v1.1.1 (9-Jun-2021)

- PCI-SIG®. PCI Express® Base Specification, Revision 5.0 May 28th, 2019
- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 4.0, September 2nd, 2019
- SFF-TA-1009 specification for Enterprise and Datacenter Standard Form Factor Pin and Signal Specification Rev 3.0, March 19th, 2021.
- SFF-TA-1009 specification for Enterprise and Datacenter Standard Form Factor Pin and Signal Specification Rev 3.1, January 6, 2023.
- The following link contains the DC-MHS Connector List:
https://drive.google.com/drive/folders/1sURGb6UQ7pZr48_0RnXanBGqgC2a4EA4
- The following link contains M-PIC specific reference material (including Errata documentation):
<https://drive.google.com/drive/folders/1A6qxOa1ma-Fk2mZSyQUENDScYKtS2sns>

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