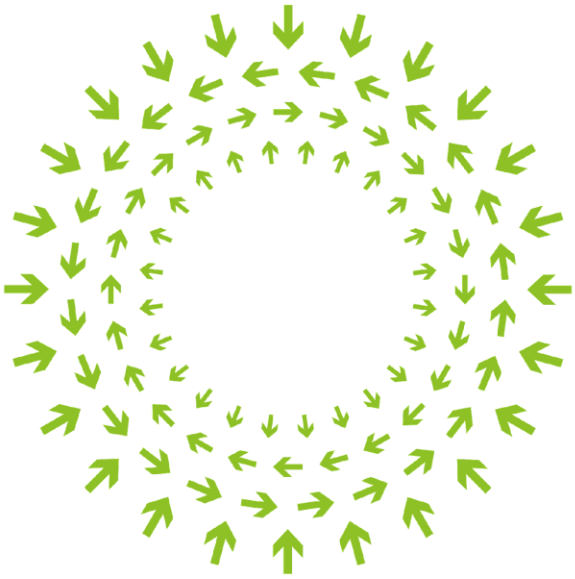


OPEN

Compute Project

Full Width HPM Form Factor (M-FLW) Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 1.2 RC3

09/26/2024

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1.2. Acknowledgements

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback of various individuals and companies that participated in DC-MHS.

2. Version Table

Date	Ver #	Description
4/22/2022	0.70	Initial Public Release
6/07/2022	0.75	• Added Spec Compliance Table Section 4 • Added 9.75mm to board under PSU Connectors • Moved OCP NIC Connector 6mm to left. (from 204.29mm to 210.29mm) • Moved IO Riser Connector #3 to left 5mm. Moved KOZ and Mount hole accordingly (From 136.02mm to 141.02mm) • Rotated PIC Power Connectors 180° • Defined Pins S1 & S12 on Pic Power Connectors and Rear Power Connectors and revised dimensioning scheme to Pin S1 • Figure 18, Defined IO Connectors Pin A1 & A77. • Defined Pins OB1 & B70 on NIC & DCSCM Connectors • Defined Pins OB1 & B70 and Pins B1 & B70 on Alternate NIC Connectors • Defined Control Panel Connector Pins A1 & A10 • New location for USB connector Zone • Moved Retention Hardware Height Restriction Zone note to Detail L • Combined 1U & 2U PCIE Mount Holes to one sheet • Revised references to “KIZ” to “Height Restriction Zone” • Revised Bottom Side KOZ shape for Tempan to rectangle. Revised Y-dimensioning scheme to center of rectangle • Added KOZ to Bottom side Mount Holes. Preliminary size at 13.8mm x 13.8mm. • Changed Figure 3 to support OCP NIC move of 6mm • Changed Figure 4 to show pads and KOZs around mounting holes • Updated Figure 6 for clarity • Changed Figure 10 to move OCP NIC by 6mm. • Changed Figure 11, Control panel connector orientation, and primary/secondary designations. • Changed Figure 12, USB Zone moved. • Combined Figure 17 and 18 into a new Figure 17. Moved 1U PCIe Riser Mount holes down 7.5mm and left 4mm. Added Mount Hole detail with Ø8.0mm Pad size, Ø16mm Component KOZ. • Changed Figure 21 to update Secondary size KOZs for mounting holes and chassis hooks • Updated Figure 29 for UBB outline updates • Added Figure 32 for UBB connector locations • Changed description of Adapted HPM in Section 13 • Figure 26 changed, rotating PIC Power connectors 180 degrees • Relocated power plane fusing requirements to M-PIC spec in Section 11.2 • Clarified minimum power plane recommendation in Section 11.2

6/27/2022	0.80	• Modified Table 4 in Section 11.1 to describe zone power and range of supported power • Clarified minimum power plane recommendation in Section 11.2 • Renamed Figure 22 • Figure 19, Sec 10.13, Changed primary side height restriction zones • Sect 10.12, Figure 18 change KOZ around Riser retention holes • Sect 10.8, Figure 12, moved Intrusion connector to same zone as USB • Figure 21, updated MH KOZs on bottom / secondary side. • Updated UBB Adapted outline in Figure 29 to update cutout options for cabled HSIO at far edge. • Figure 33 updated, based on connector feature updates from vendors • Figure 35, updated text in drawing • Figure 25, updated title in drawing • Added Guide pin part number to Sect 13.1.6 • Added bullet 6 to section 10.10.1 • Figure 18, 19, updated KOZ around riser retention holes • Figure 22, updated Thermal solution Bracketry KOZ • Section 10.8, new section for PDB to HPM header • Moved section 12 into existing sections and deleted it • Moved section 13.1 into Section 12 “Adapted HPMs” for spec clarity.
8/22/2022	0.9	• Updated Mounting Hole drawing • Added New handle hole geometry required dimensions, • Updated OCP NIC and DC SCM positions, Figure 9 • Moved PDB Management conn zone, Figure 13 • Moved boot connection zone, and modified to accommodate new HPM retention hole location and its associated KOZ, Figure 15 • Figures for Near IO Riser connector locations and Riser Retention holes • Updated Sect 10.3, HPM Board and Assembly thickness section, to include details and tolerance allowance for the Secondary Side Exception Heights. • Updated locations of Near side PIC Power (decreased pitch); maintained 10mm gap between pins of Near side Power connectors. Far Side PIC Power connectors moved outward to increase usable Far Edge space for CPU IO and VRs., Figure 31 • Updated Primary side height restrictions, Figure 17, Changed 20mm zone to 22mm and added note that numbers indicate max tol condition. Fixed an unattached dimension. • Added Platform Custom Zone options of 2x OCP NIC SFF, or single LFF with recommended placements, or direct dock E1.S boot, Section 10.6 • Updated Figure 3 with updated Near side outline • Updated Section 10.11, rewrite of requirements. • Updated CRPS Connector location (near OCP NIC), Figure 29

		• Update location of HPM retention hole, Figure 6 • Updated image for latest outline • Updated Secondary side KOZ's for chassis hooks (board pan interfaces), to allow for more flexibility in DIMM socket placement. Reduced HPM-chassis retention KOZ from 29 to 21mm long. For an example of chassis hook concept, • DC SCM Y position adjusted by 0.18mm, to correct mistake. This correction aligns DC SCM with OCP NIC at rear wall. • Changed Power Zone E rating to 160W • Changed Power Rating Zone C to 250W per Near IO Connector instance • Added section to define Platform Custom zone and a couple standard options that could be utilized. These drawings were in the Supplemental Info section, previously. • Added E1.S enablement option, • Figure 11 • Fixed KOZ around chassis retention hole to 21x21mm, For an example of chassis hook concept, • Added implementors note about HPM handle hole and Mounting holes For an example of chassis hook concept, • Deleted chapter 12.2, which had old, adapted options that were pulled into the new Platform Custom Zone. • Added introduction paragraph including units and tolerances to Section 10, matching M-DNO content. • Changed 11.1 Zone B connector to Vertical only (removed R/A option) • Intrusion Switch and USB Conn zone updated, to ensure it does not overlap in the 11.3mm height restriction zone, Figure 14. • Created new chapter for Far Side Panel Mount HPM in Supplemental Section 14.8. Moved and renamed this content out of the Adapted HPM section. • Changed Zone B Section 11.2 to include ingress power option per M-PIC specification
9/26/2022	1.0	• Added Connector List to DC MHS documents, Section 6 • Section 10.1, Updated Outline wording to indicate base outline is Type 1, and future Types will be defined. • Clarifications made in Section 10.1.1 • Moved HPM Board Thickness Section to 10.14, and moved secondary side height restriction details into Section 10.13 • Changed Board Handle Hole geometry, Section 10.4 • Made primary OCP NIC location a reference dimension in example of 2 OCP NIC use case. • Updated naming labels in Boot Storage Connector Figure 15 • Clarified hole descriptions as "Riser Retention Holes" in Section 10.11

		• Clarified wording on Primary Side Component Height Restrictions, Section 10.12 • Updated format of Secondary Side Zones and Height Restrictions, Section 10.13 • Added new requirements for secondary side height zone restrictions, as part of restructuring of Section 10.14 • Removed HPM Power Plane Section, Changed Section 11 from Power Delivery to Power Zones. • Added Section 12, with simple reference to other DC-MHS specs. • Updated Figure 31, and provided optional placement for connector #6. • Removed Power Plane requirements from FSPM section in Supplemental Information, for consistency with base spec. • Tolerance removed from Near IO connector placement, Figure 16 • Added CAD import tip in Section 14.9 • Added Section 14.5, Liquid cooling example to Supplemental Section Clarified Example references in Supplemental Information Section • Added outline notches for 4C+ connectors to the board outline (all figures) • Added Statement to Section 10.1 that Platform Custom Zone outline may be modified based on connector choices. • Route KOZ added to HPM Retention hole, impacting Figure 17 and Figure 19 • Corrected Reference to SFF-TA-1002 • Added additional industry specifications to Section 13 References • Added requirement reference to battery backed voltage interface to DC SCM R2.x • Updated Centerline labeling drawings with 4C+ connector dimensioning
10/26/2022	1.0 RC5	• Updated pin naming on Control Panel connector drawing Figure 12 to match M-PIC naming convention. • Updated line 195 wording to match DNO, fix typo.
05/24/2023	1.01 RC1	• Added clarification on relation of height restrictions and internal USB connector to Section 10.9 and 10.13 • Added clarification on vias below Figure 4 (not in scope of spec) • Updated Figure 29 to reference a new defined datum for M-CRPS connector (M and N) for locating purposes. Updated image to show a recommended superset connector footprint. Deleted reference to M-PIC and M-CRPS, line 785 • Removed reference to M-PIC at line 990 • Removed vendor label on connector drawing • Changed Implementors Note on offset connectors Section 10.15 • Added Figure 36 to help map example 1U and 2U Riser usage to Near IO positions • Clarified spec compliance statement on line 196

		• Refreshed image with latest housing version of Near IO connectors in Figure 16 and Figure 38 • Updated image of SFF-TA-1033 connector to show latest design of housing in Figure 32 • Page 16 updated link to DC-MHS WIKI
6/1/2023	1.01 RC2	• Fixed date mismatches in footer • Re-exported PDF to fix Figure links
03/28/2024	1.1 RC2	• Updated company list and family of specification list • Updated board drawings that were missing Primary or Secondary side view labels • Changed DC-SCM R2.0 to R2.x to match S-DNO • Updated Implementor's Note for Offset Connector to match S-DNO • Removed Zone 3 requirement, updated section to match S-DNO • Added Negative Feature Allowance to match S-DNO • Added Implementor's Note to **Section 10.6.1,** reasons why OCP NIC pitch was chosen • Board Hole Section updated verbiage and figure to be consistent with M-SDNO • Moved SCM Battery requirement from Section 12 to 10.5 • Updated HSIO Connector chapter to match MSDNO • Update Primary Side HRZ chapter to include connector/cable information • Wording updated to clarify 'recommended in Boot Storage Connector • Section 10.11 re-written for consistency with M-SDNO spec approach • Figure 19 Updated for removal of KOZ/pad details (moved into Table 2) • Sections 10.13.1, 10.13.5, and 10.14 updated to indicate new allowable max HPM assumed height of 6.2mm (was 5.86mm) • HPM to Chassis Retention Figure 6 and Board Handle Hole Figure 8 updated to add Primary/Secondary side Pad and KOZ (as reference in some cases). • Changed PIC PWR locating scheme to Circuit 1 as locating datum for consistency with M-PIC Spec • Spec Compliance Table Reordered, with new items added, and some items deleted. • Formatting Errors fixed in RC1 to RC2
09/2/2024	1.2 RC1	• Clarified verbiage and compliance requirements to enable cabled OCP NIC as alternative to direct dock, **Section 10.5** • Corrected PICPWR Circuit 1 flag in drawing. Changed Requirements for PICPWR location requirements from fixed locations to zones with recommended locations. **Section 11.2** • Moved OCP NIC R3 LFF references to Supplemental Info Section 14.9 • Updated Platform Custom Zone examples to include OCP NIC R3 DSFF, **Section 10.6.1**

	1.2 RC2	• Added Implementor notes related to DSFF application

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3. Scope

This document defines technical specifications for the Full Width HPM Form Factors used in Open Compute Project, Data Center Modular Hardware Systems.

Any supplier seeking OCP recognition for a hardware product based on this specification shall be 100% compliant with all features or requirements listed in **Section 4** of this specification.

3.1. Items Not in Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

3.2. Typical OCP Sections Not Applicable

Open Compute documents are typically expected and desired to contain common document Sections. The DC-MHS specifications are comprised of Base Form Factor Specifications and Supporting Platform Connectivity specifications, and are structured such that the typical OCP document structure does not apply to this Base Form Factor Spec. This specification will not contain the following Sections.

- Rack Compatibility (See **Section 14.1 Rack and Chassis Depth Stackup Assumptions**)
- Physical Specifications
- Thermal Design Requirements
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

4. Specification Compliance Table

235 The following table is intended to summarize the list of attributes and requirements for a design to be DC-MHS M-FLW Base Specification compliant.

#	Technical Specification	Document Reference
1	PCB Tolerance Table	**Section 10**
2	HPM Outline(s) definition	**Section 10.1, Figure 3**
3	All negative PCB features shall comply to listed restrictions	**Section 10.1.1**
4	Board Datum, Mounting hole, and Riser Retention hole requirements	**Section 10.2,Figure 5**
5	Board Datum, Mounting hole, and Riser Retention Hole pad and KOZ requirements	**Section 10.2, Table 2**
6	Hole required for HPM to Chassis Retention locking feature	**Section 10.3, Figure 6**
7	HPM to chassis retention KOZs required on Primary (Detail L and Secondary sides Detail M) around HPM Retention hole	**Section 10.12, Figure 17 and Section 10.13, Figure 19. Reference in Section 10.3, Figure 6**
8	HPM Handle requires a hole at Far side w/ specified geometry	**Section 10.4, Figure 8**
9	Required Location of DC-SCM R2.x OCP NIC R3 connection. a) Required at specified location Or b) Negative feature cutout sized to enable cabled OCP NIC at specified location and enablement of required power/IO cables	**Section 10.5 Figure 9**
10	Battery Backed Voltage Interface per DC-SCM R2.x requirements	**Section 10.5**
11	2x required instances of Control Panel Interface connectors per defined locations	**Section 10.7, Figure 12**
12	PDB Management Connector requirement and placement zone	**Section 10.8, Figure 13**
13	Internal USB connector and Intrusion Switch connector requirements and placement zone	**Section 10.9, Figure 14**
14	All HSIO connectors shall be M-XIO compliant	**Section 10.11**
15	Near Side Fixed Riser connectors shall use defined Fixed Riser connectors, placed in defined locations (if populated)	**Section 10.11.2, Section 10.11.3, Figure 16**
16	Near Side Fixed riser connectors shall use a 21A power block version	**Section 10.11.3**
17	HSIO connectors shall be defined in M-XIO	**Section 10.11.4, and Table 3**
18	Primary side component height restriction zones	**Section 10.12, Figure 17**
19	Adherence to 11.3mm Primary Height Restriction zone	**Section 10.12, Figure 17**
20	Max Height Restriction of mated height plug and cable assembly	**Section 10.12**
21	Secondary side Zone and Height Restrictions, Zones 1-4	**Section 10.13**
22	Secondary Side Height Restriction Zone 1	**Section 10.13.1, Figure 19**
23	Secondary Side Height Restrictions Zone 1 Exception	**Section 10.13.2**
24	Secondary Side Zone 2 0-height KOZs required (8x) on Secondary side	**Section 10.13.3, Figure 19**
25	Max Length of connector's alignment post/barb is 3.2mm	**Section 10.13.3**
26	Zone 4 Board Thickness + Backplate Thickness <= maximum defined calculation/formula	**Section 10.13.5**
27	Maximum allowed HPM Board thickness is 3.18mm	**Section 10.14**
28	HPM shall implement KOZ's on Far side mounting holes for Thermal solution brackets	**Section 10.15, Figure 26**
29	Required Locations for M-CRPS connectors	**Section 11.1, Figure 29**
30	HPM 2x6+12s PICPWR connector placement zones	**Section 11.2, Figure 31**
31	Minimum HPM Power Supply Rail Requirements per PCIe CEM Slot	**Section 11.3, Table 6**
32	HPM shall be required to implement electrical interfaces that must follow the DC-MHS family of specifications	**Section 12**

5. Overview

The objective of this specification is to specify the requirements of a Full Width Host Processor Module (HPM). This is for use within products designed for minimum 19" rack, also known as compliant with EIA-310-E but can also accommodate larger 21" racks. This form factor enables a full width HPM usage for CPUs, DIMMs, and related features. This full width form factor generally allows for maximum IO of the CPUs to be offered and brought to accessible slots (although exceptions could occur in the future). This specification will NOT reference a specific CPU or memory technologies. The goals and success criteria of this specification is so that multiple generations of CPU/Memory (Compute Core) designs can be designed into this form factor specification, so that chassis and system designs can be reused as desired. This should have the benefits of reduced design investment, reduced validation investment, and faster development cycle time.

This specification will define attributes and design requirements that are common and critical to the use and deployment of Enterprise and Cloud solutions which may also apply to Edge optimized service provider products. Examples of these attributes are mechanical form factor, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections.

The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs, implemented to the specification, to enable reuse of chassis and system level components over multiple generations. Implementing to this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

Implementors Note:

As a Base Specification, M-FLW contains and allows for optionality in many areas. In addition to this base specification, it is recommended that HPM designers create and maintain an HPM Design Specification that further details the needs and requirements of their own unique design.

Examples of information that may be included in a Design Specification are:

- Quantity and location of fixed/hybrid risers
- Quantity and location of other HSIO connectors
- Power zone requirements
- Innovation zone use case
- Etc.

6. DC-MHS Family of Specifications

The **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**N**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments.
- **M-FLW** (**M**odular Hardware System **F**ul**l** **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (i.e., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-SDNO** (**M**odular Hardware System **S**calable **D**e**N**sity **O**ptimized Specification) – Builds upon M-DNO, defines partial and full width HPMs with variable board outlines covering 19” EIA-310 and 21” OpenRack v3 infrastructure.
- **M-SIF** (**M**odular Hardware System **S**hared **I**n**f**rastructure Specification) – Specifies data and management plane interfaces along with power and cooling connections that are expected to be present within a modular platform utilizing shared elements.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **Current Connector List** – Vendor and part number information for all connectors referenced by DC-MHS specifications, updated as needed. Full URL: https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/
- To access additional DC-MHS specifications please visit the DC-MHS Project Wiki: https://www.opencompute.org/wiki/Server/DC-MHS

7. Terminology

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for spec compliance	
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
PCB	Printed Circuit Board	
Datum	A plane, axis or point location from which dimensions and tolerances are referenced.	
DC-SCM	Datacenter Secure Control Module Rev 2.x as defined by OCP DC-SCM Rev 2.x spec	
CPU	Central Processing Unit	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link, open standard for CPU to device and CPU to Memory connections.	
Chassis-Board Bracket	Bracket that attaches to a HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan Sub-pan
Near	Board location or zone, related to section of board closer to the datum	Near Side
Far	Board location or zone, opposite of location of datum	Far Side
Platform	Complete system including HPM, power, peripherals, etc	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
Platform Infrastructure Connectivity Spec	A Specification that defines Platform Interconnect details for features that are common across many HPM Form Factors. Examples connectivity features include fans, backplanes, and control panels.	M-PIC spec
KOZ	Keepout Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
Compliant HPM	An HPM which meets every item listed in the base specification compliance table.	
Adapted HPM	An HPM which has strong correlation to base spec requirements but does not meet every item in the base specification compliance table.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements the HPM form factor specification.	
System Designer	The person or organization designing a system which incorporates HPMs (whether compliant or adapted) into the system design.	

8. Background and Assumptions

This Full Width HPM Form Factor specification is created to enable typical platform feature sets for both Front and Rear Management, in 1U and 2U chassis applications. Some of the platform features that are common in the industry, and influence the Form Factor constraints are:

- Chassis installation within minimum EIA-310-E racks (but not limited to).
- PCIe (Version 5.0 and future) Card configurations typically offered by Enterprise OEMs/Hyperscalers. See **Figure 34. Examples of Typical 1U / 2U PCIe Slot** and **Figure 35. Examples of Typical 1U / 2U PCIe Slot Configs for Front** Management System
- In the 1U PCIe offering, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would require more restrictive Compute Core placement (not defined).
- HPM enabled minimum 75W of power per PCIe slot, with ability to scale up to 600W for some slots (likely 3~4).
- The specification details support for the Open Compute peripherals directly connected to board
    - OCP NIC R3.0
    - DC-SCM R2.x
    - *Note: A s*ystem is not limited to one device of each type; configurations with >1 DC-SCM R2.x are possible, but outside the scope this specification will cover.
- Thermal Design Points considerations includes keepout zone to enable air cooling thermal solutions that extend beyond the CPU and Memory sockets. Memory TDPs under consideration are in the 20-25W range.
- Considerations for Liquid cooling solutions, including CPU cold plates and DIMM liquid cooling manifolds.
- Considerations for Power Delivery to important chassis subsystems.

8.1. Rear Management (ie, OEM) Architecture Assumptions

1. Chassis depth constraints in consideration of Power Distribution Units placed approximately 780mm from front EIA mounting flange.
2. Enterprise Storage and Fan subsystems requiring approximately 220mm. (See Figure 34. Rack Depth Constraints)
3. Sliding rack rails that require a max overall chassis width of 434mm, with interior chassis width/opening of minimum 427mm.
4. Considerations for power and High-Speed IO cabling
5. Considerations for ease of installation and removal of motherboard in a chassis.
6. Adequate delivery power through HPM to enable typical storage configuration power loads.

8.2. Front Management (ie, Hyperscale) Architecture Assumptions

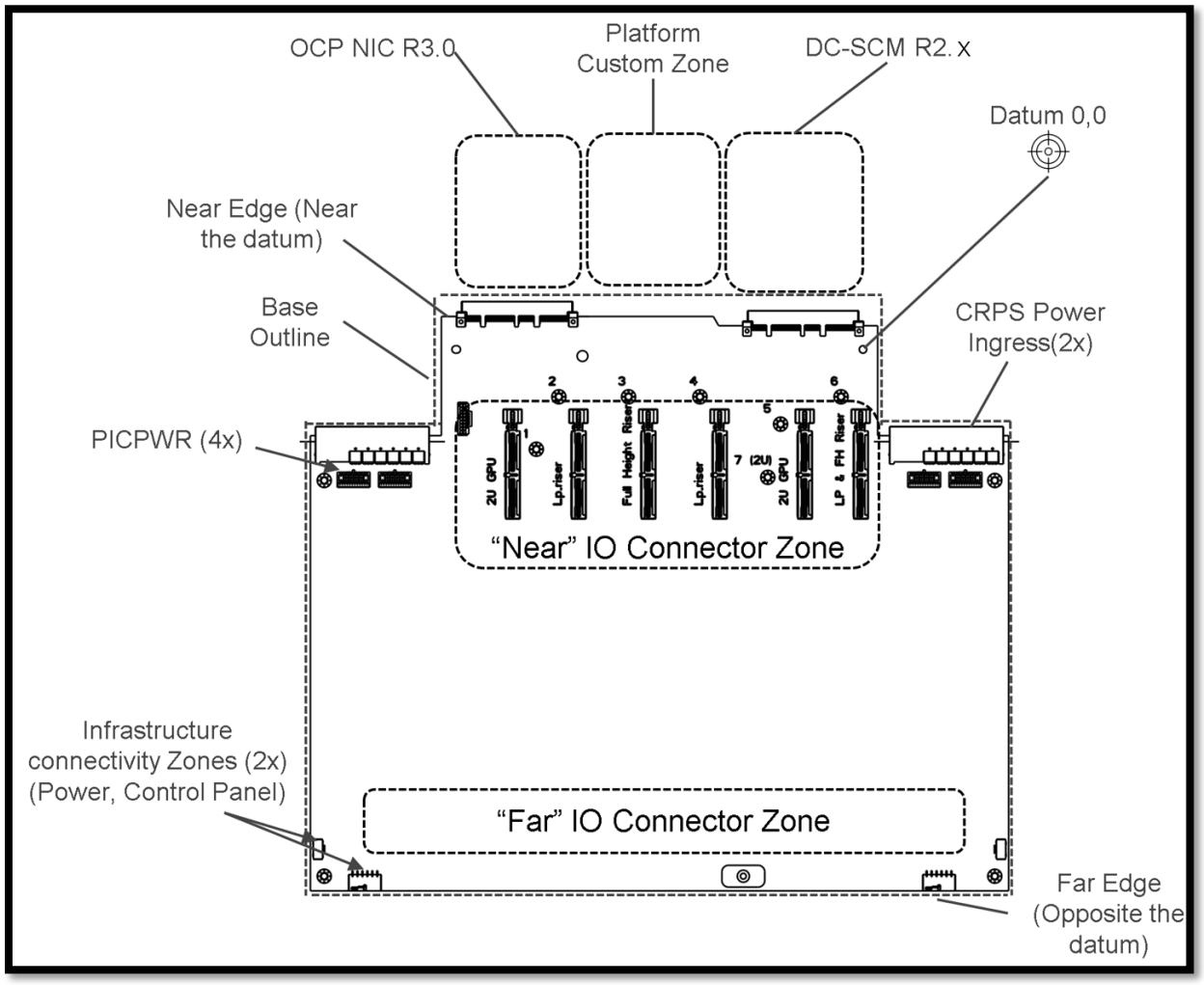
1. 1070mm rack depth
2. All IO generally on cold aisle but may also include some architectures with hot aisle IO. Assuming Front/Near end of system supports IO devices such as PCI CEM, OCP NIC R3.0, SSD’s, etc
3. PCIe also distributed at Far end, such as to backplane, OAI – Universal Baseboard, and other items.
4. AC or DC rack power supplied by rack from the hot aisle
5. If PSUs are used, they are not hot serviceable

9. HPM Layout

The following **Figure 1** shows the layout and approximate locations of major subsystems in the Enterprise and Hyperscale M-FLW HPM.

"Near" and "Far" are reference naming conventions to the side of the board and Compute Core, as to orient the reader as to which portion of the board and Compute Core is being referred to. This specification refers to the Near Side as where DC-SCM R2.x Management subsystem resides as a board peripheral. This is also typically referred to Rear IO location for Enterprise products, in which products are designed with IO in the hot aisle of a rack deployment (air exit). This is also typically referred to Front IO location for Hyperscale products, in which products are designed with IO in the cold aisle of a rack deployment (air inlet).

Figure 1. Full Width HPM Layout Diagram



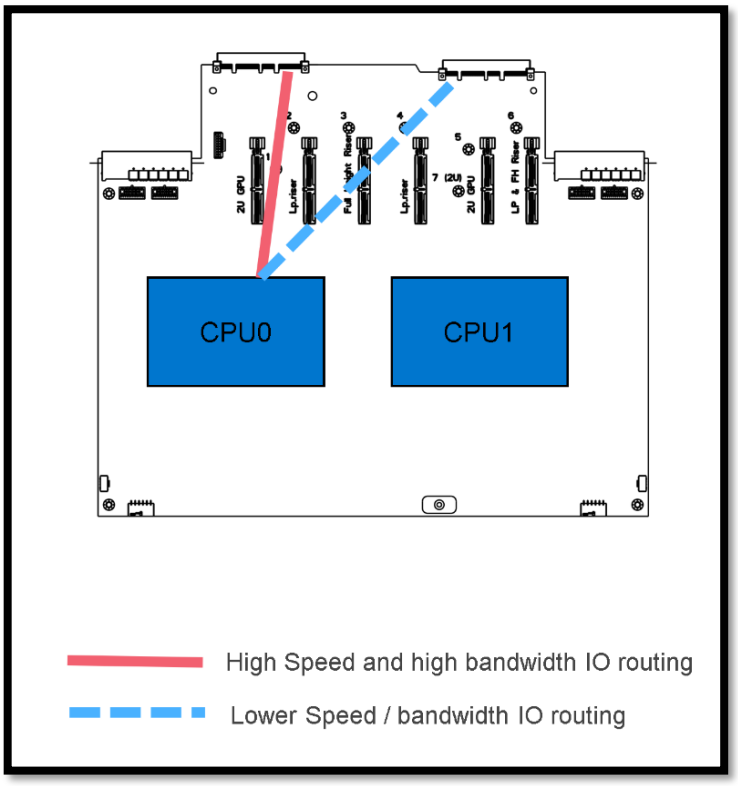
9.1. Two Socket (CPU) Assumptions

The OCP NIC R3.0 subsystem is positioned on the left based on two assumptions:

- In a 2S (CPU) system, the First/Boot CPU in a two CPU HPM is positioned on left.
- OCP NIC R3.0 is directly routed through the motherboard to the first/boot CPU.

The OCP NIC R3.0 is intended to be closer to this boot CPU to best enable the high-speed IO routing. The OCP NIC R3.0 will usually require higher bandwidth routing, and thus should be optimized for material selection and cost impacts. The routing from first/boot CPU to management subsystem (DC-SCM R2.x) has lower bandwidth requirements, and thus should not be the determining factor in board material selections and routing strategy. See **Figure 2**.

Figure 2. First CPU position relative to OCP NIC R3.0 and DC SCM R2.x



In this specification the CPU and Memory locations are intentionally not specified. This is for future flexibility in CPU/Memory quantities, locations, sizes, etc. The board area between DC-SCM R2.x and OCP NIC R3.0 is designated as a “Platform Custom Zone”, as shown in **Figure 1. Full Width HPM Layout Diagram**. The goal is to provide board area and system volume for individual platforms to provide system specific features.

9.2. One Socket Assumptions

In theory, for a one socket (CPU) platform, the OCP NIC R3.0 location does not have a strong affinity to either side. The OCP NIC R3.0 should remain in the specified HPM location (left) for chassis compatibility for all Full Width HPM products**.** The second OCP NIC shown in the Platform Custom Zone is optional, the OCP NIC on the left must always be populated.

10. Mechanical Requirements

In addition to the drawings and details within this document, DFX/CAD file link is provided in **Section 14.9**

All units are in millimeters, unless otherwise specified. The following standard tolerances apply to all drawings unless otherwise specified. PCB dimensions shown in this specification shall comply to the following tolerance table, unless otherwise specified.

Table 1. Tolerance Table

Dimension Type	Tolerance*
FROM Origin/Datum hole center TO round fiducial center	+/- 0.076mm (+/- 0.003 inch)
FROM Origin/Datum hole center) TO profiled card edge	+/- 0.254mm (+/- 0.010 inch)
FROM Origin/Datum hole center TO drilled hole center	+/- 0.127mm (+/- 0.005 inch)
FROM Profiled card edge TO profiled card edge	+/- 0.127mm (+/- 0.005 inch)
Feature of size (hole diameter, slot width, etc.)	+/- 0.100mm (+/- 0.004 inch)
PCB thickness	+/- 10% of nominal

*Unless Otherwise Specified

Route KOZ's referenced in this specification, at a minimum, refer to surface layers and microstrip routing. Further application of the Route KOZ to other layers is the choice of the HPM designer and/or Design specification.

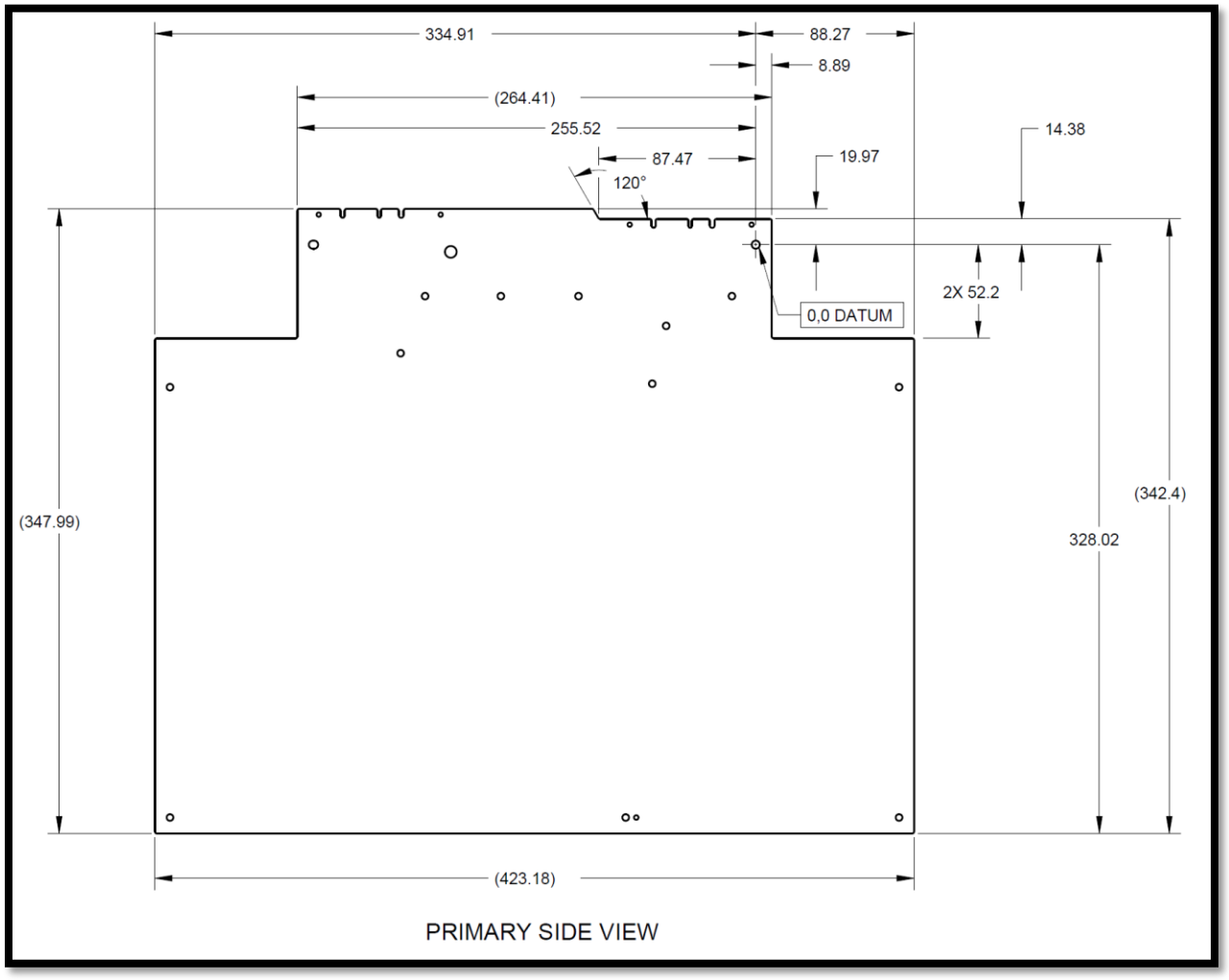
10.1. HPM Outline

The outlines defined in this section shall be followed for M-FLW Base spec compliant HPM. (Note for 1.0 release, there is only one Type defined.)

The Full Width Type 1 HPM (M-FLW) base outline is defined in **Figure 3** and shall be followed for a M-FLW Base Specification compliant HPM. This defines the outline and peripheral locations to fit compute core and IO elements in an FLW compliant chassis. This is intended to fit a wide variety of platform and chassis applications. The intent is to show overall dimensions of board outline.

DFX/CAD file link is provided in **Section 14.9**

Figure 3. Full Width Type 1 Outline

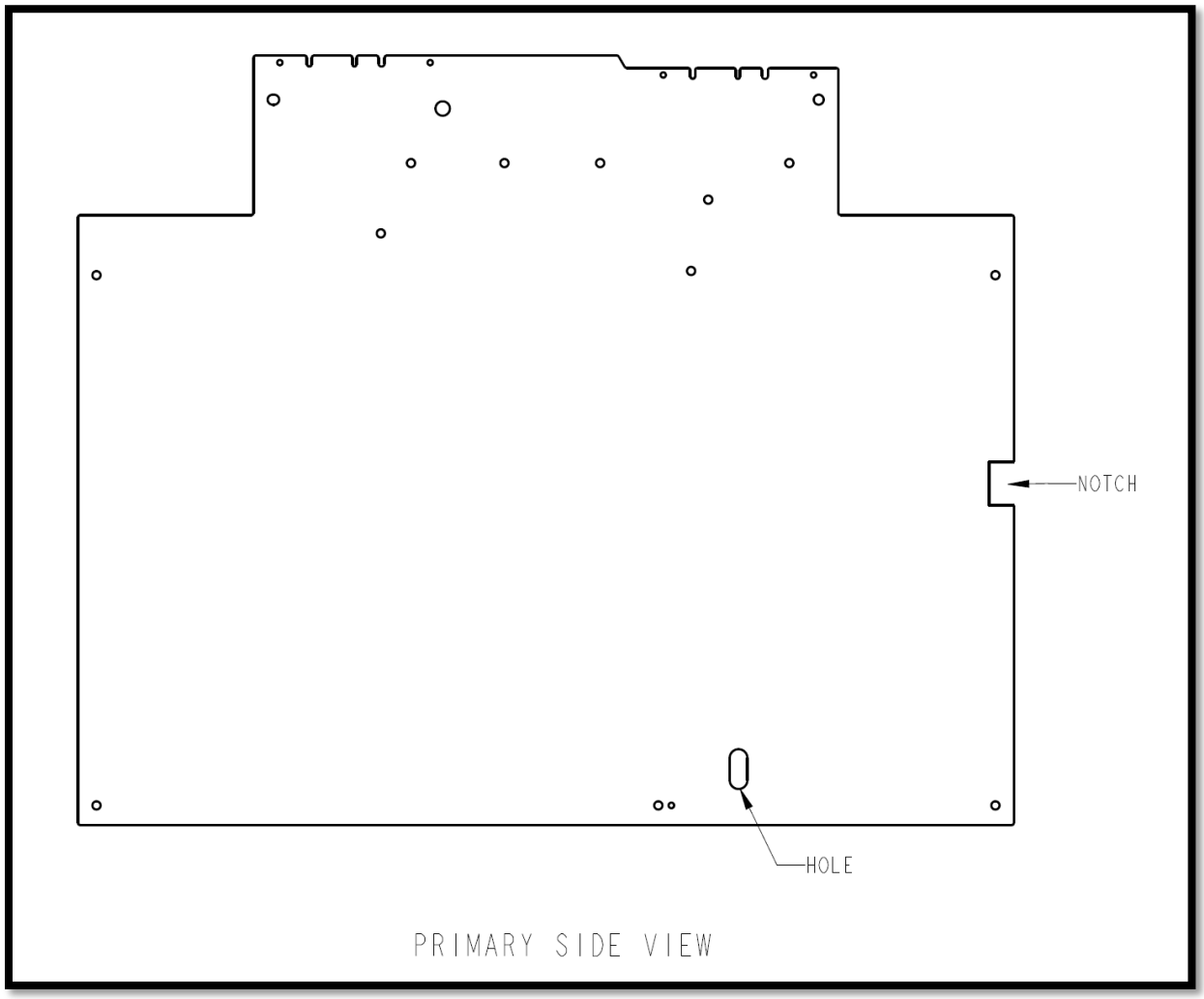


Note: The outline of the HPM near Platform Custom Zone (described in **Section 10.6**) may change for connector choice compatibility specific to the usage of the Platform Custom Zone.

10.1.1. Allowance for Negative PCB Features

All HPM types may include “negative PCB features” with the noted limitations. A negative PCB feature is defined as removal of PCB material in localized areas of the HPM outline. Examples of negative PCB features include notches along a board edge or openings of any geometric shape within the HPM outline. See **Figure 4** for illustrative example.

Figure 4: M-FLW HPM with Compliant Negative PCB Features



All negative PCB features implemented shall comply to the following restrictions:

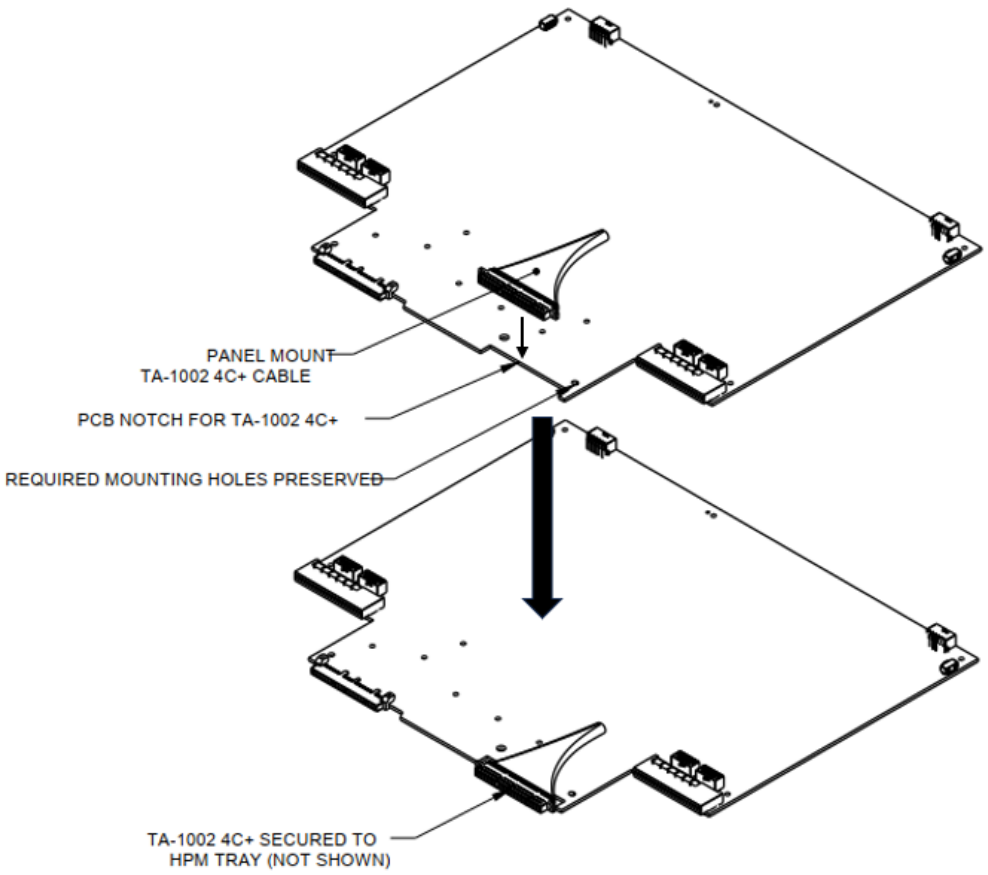
1. Negative PCB features shall not violate or conflict with any required features such as mounting holes and connector placement.
2. The negative PCB feature shall not extend the full length of the left or right edge of HPM (i.e., this feature shall not be used to essentially create a non-standard HPM width).

Implementors Notes:

HPM-level and system-level manufacturing, handling, shipping, and operational environments must be considered by the HPM designer. When implementing negative PCB features the HPM designer should consider the implications on HPM structural integrity.

The use of a negative PCB feature can afford the option of a chassis or HPM tray feature to reside within this evacuated area. However, it should be noted that if this chassis or HPM tray feature must always be present, then other specification compliant HPMs that do not have these negative PCB features may not be interoperable with this system. An ideal system implementation would not require these negative PCB features to be present on all supported HPMs.

An example application of a negative PCB feature is the use of a notch at the M-FLW reference OCP NIC3 connector location combined with the use of a cabled panel-mount TA-1002 4C+ connector. The shown notch preserves the option to position the NIC3 in the reference location, thereby mimicking a straddle-mount coplanar 4C+ on the HPM. The PCB notch geometry would be a function of the specific panel-mount 4C+ connector chosen for this application.



PRIMARY SIDE VIEW

10.2. Board Holes for Datum, Board Mounting, and Riser Retention

Board Datum, Mounting hole, and Riser Retention hole requirements shall be implemented per **Figure 5** and represent the minimum mounting hole requirements.

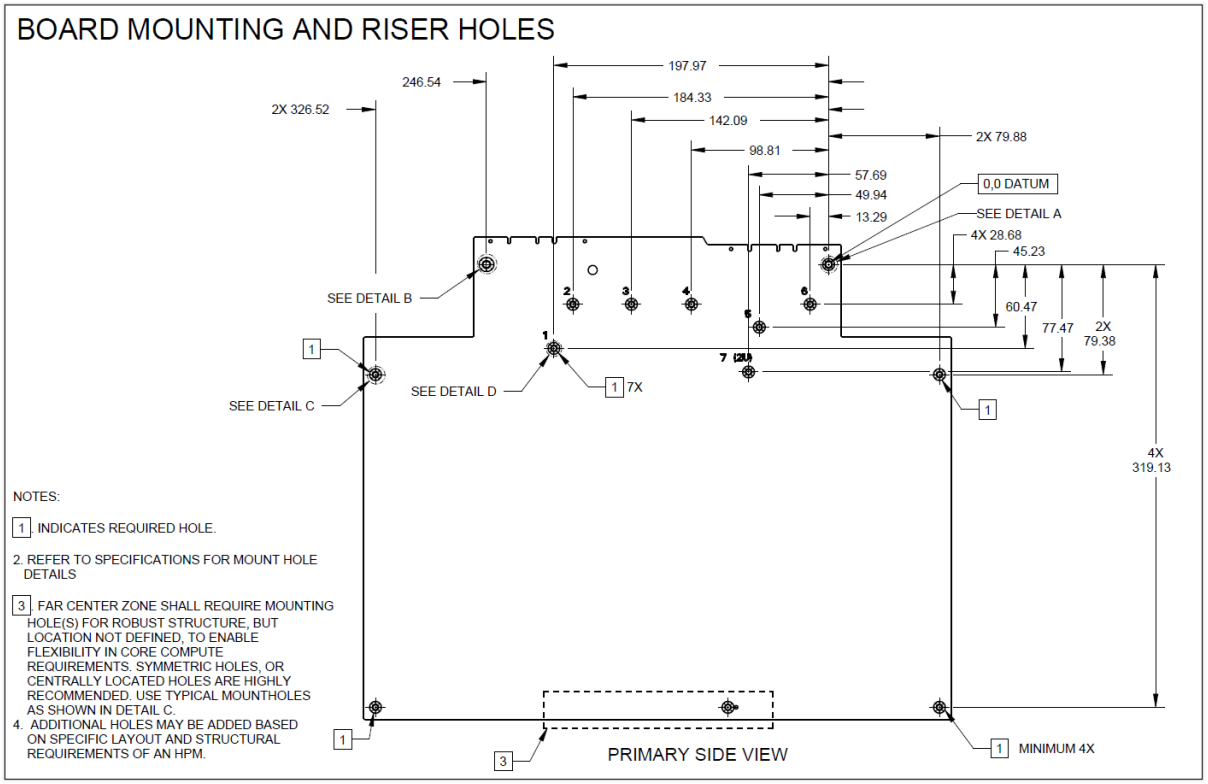
These six boards mounting holes on the perimeter may interface to the Chassis-to-Board Bracket (Board Pan) or a chassis base.

Additional mounting holes are allowed as needed, to ensure appropriate mechanical support of the Compute Core (not shown). Additional board holes are expected to interface to the board-chassis bracketry and should be designed in consideration of the bracket to chassis interface features, as defined in **Section 10.3 HPM to Chassis Retention.** A design should follow good engineering practices and in consideration of platform shock and vibration requirements. Shock and vibration requirements are not in scope of this specification.

The mounting holes shall have a pad and component KOZ as defined in **Table 2**.

The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension, it is considered adequately robust, and an exception will allow such component to encroach on the Component KOZ's in in **Table 2**.

Figure 5. Board Mounting Holes with Pads and Keepout Zones (Top / Primary side view)



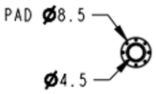
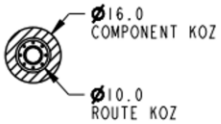
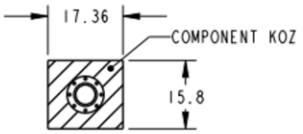
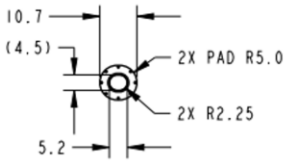
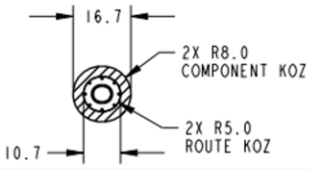
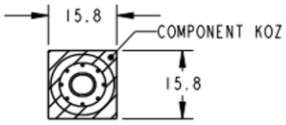
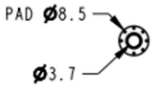
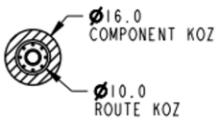
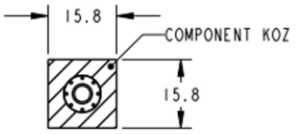
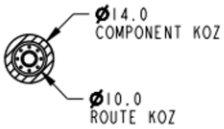
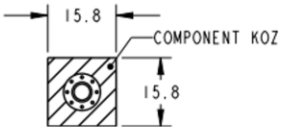
450

Implementors Note:

The PCB Datum hole (Detail A) is defined such that a collared standoff with tight tolerance fit can be used to control X-Y tolerances in HPM mounting. Additionally, a slotted hole (Detail B) is defined to control rotation around the datum, by allowing, as an example, a collared standoff to be used with tight fit to the top/bottom edge of the slot.

All other mounting holes follow standard mounting hole guidance (Detail C). These mounting holes are expected to have clearance fits to screw hardware.

Table 2. Board Hole Detail Views, with Pad and KOZ Details

	Hole and Pad Sizes	Top Side KOZ	Bottom Side KOZs
DETAIL A Unique Alignment Hole (0,0 DATUM)			
DETAIL B Unique Alignment Slot			
DETAIL C Standard Alignment Hole			
DETAIL D Riser Retention Hole			

The vias that are shown in Figures are for reference only. Via requirements are NOT in scope of this specification.

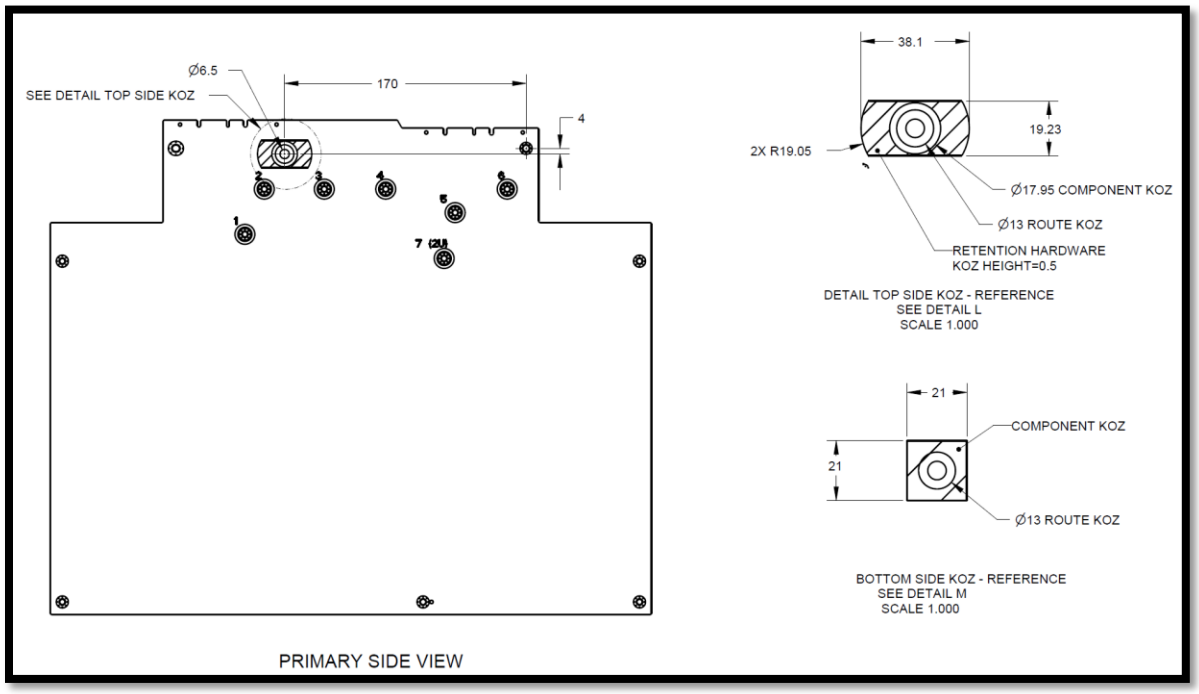
455 Additional Secondary side pad and KOZ requirements for mounting holes are shown in **Figure 19. HPM Secondary Side Height Keepout Zones, Pads, KOZ**

10.3. HPM to Chassis Retention

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required on HPM to be used for HPM retention to the chassis, located at the required location in **Figure 6**. The hole is sized for common retention methods such as plungers, thumbscrews, etc.

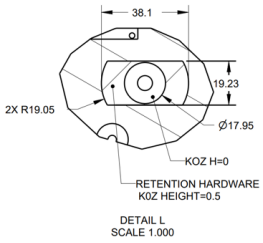
The KOZ's and Pad sizes in this view are shown as Reference. The controlling drawings are in **Sections 10.12 and 10.13.**

Figure 6. HPM Assembly to Chassis Retention Enablement



Implementors Note:

The wide shaped 0.5mm Height Restriction in **Figure 17. Zones for Primary Side Component Height Restrictions**, Detail L, is in place for finger grip allowances around the retention hardware (which could be a plunger, thumbscrew, wing screw, etc). Due to hardware and touchpoints being in this area, the goal is to minimize the size of components that could potentially be damaged by fingers coming in close contact to the board surface.

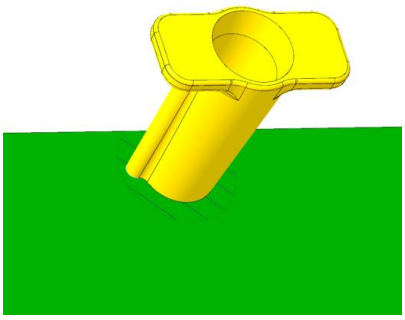




10.4. HPM Handle Hole

The HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with, but is not limited to, a plastic handle. An example is shown in **Figure 7**.

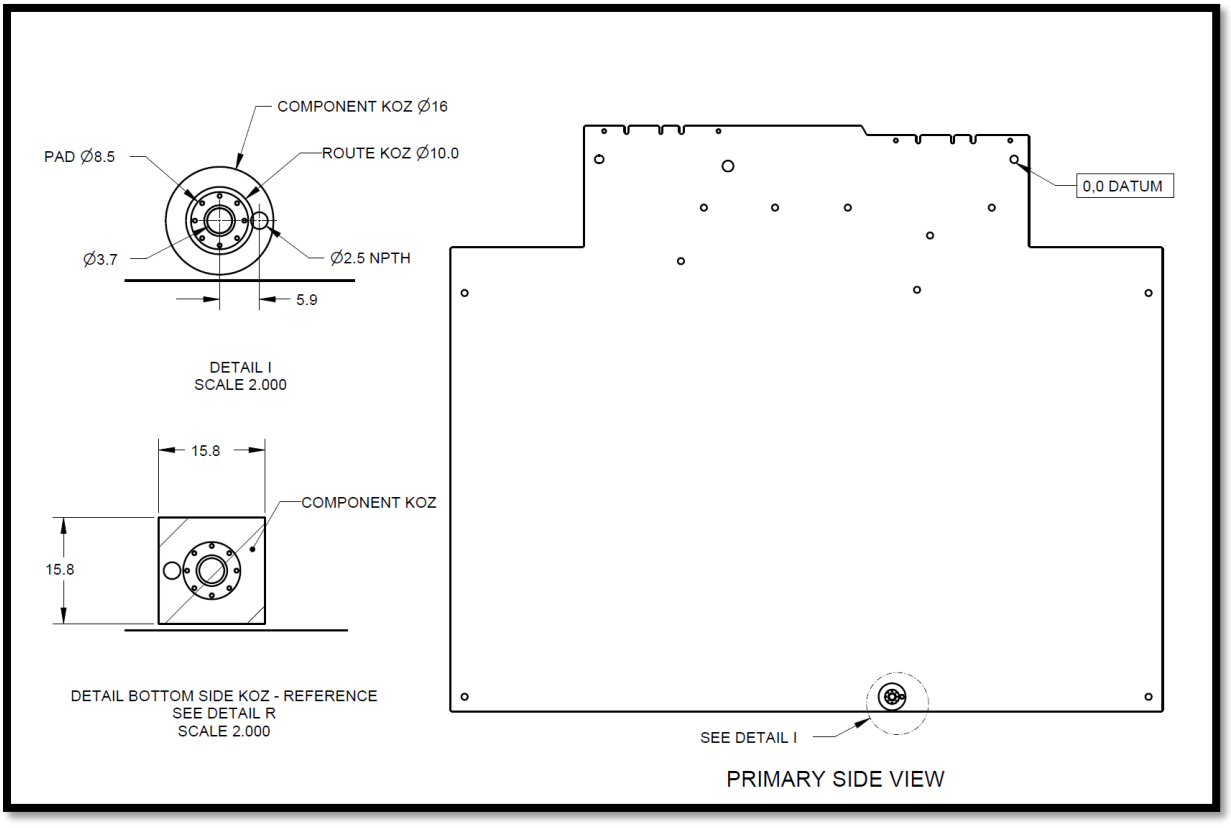
Figure 7. HPM Handling Feature



The hole location shall be near the Far side edge of the HPM. Designers may choose to either:

1. Replace a recommended mid-board mounting hole along the Far Side edge with the board handle hole. **Figure 8** demonstrates this.
2. Add an additional hole near the Far Side Edge with consideration for Compute Core Details such as cabling for HSIO.

Figure 8. HPM Handle Hole Detail



Implementors Note:

While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

The Board Handle hole may also be considered a mounting hole for structural purposes. For example, a designer does NOT need to place a board mounting hole in close proximity to the Board Handle Hole.

10.5. OCP NIC R3 and DC-SCM R2.x at Near Edge Locations

This specification defines fixed placement for certain peripheral connectors to maximize reuse across designs.

These fixed peripheral subsystem connectors are OCP NIC R3.0 and DC-SCM R2.x.

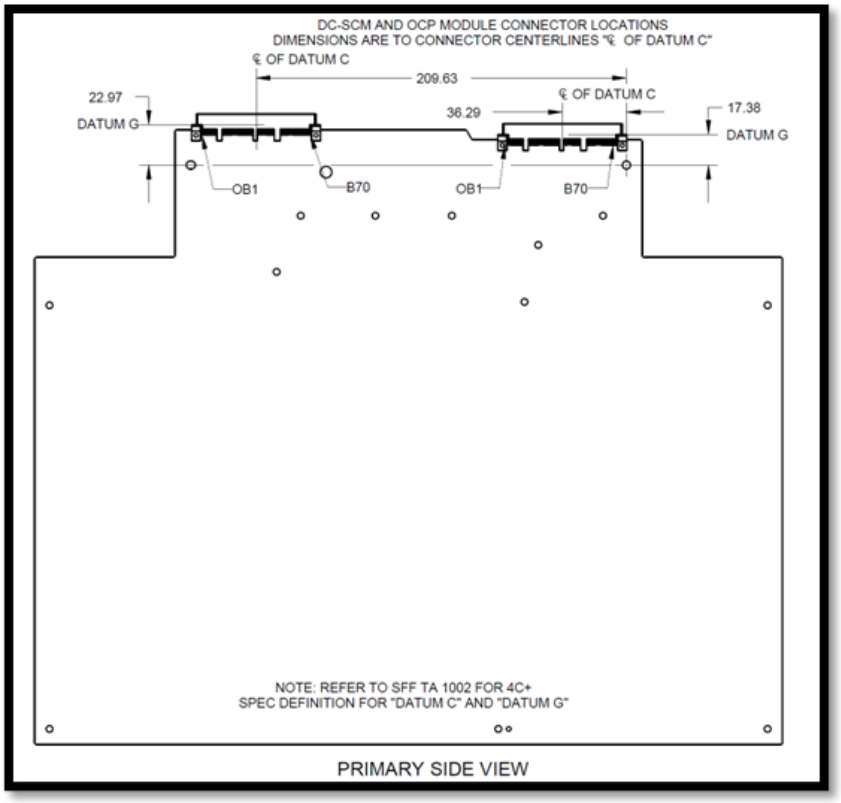
Each of these peripherals leverages connectors defined by SFF-TA-1002, including centerline definitions referenced in the Figures section of this specification. (Refer to the DC-MHS Connector List for vendor part number details).

The HPM shall place the OCP NIC R3 and DC-SCM R2.x at the locations defined by the centerline location of each of the connector subsystems in **Figure 9.**

Note, if a cabled OCP NIC HPM is preferred, a HPM design may omit placement of OCP NIC R3 connector, and instead, shall implement: a) negative feature (cutout) to create clearance for the cabled connector assembly, and b) appropriate connectors required for cabled OCP NIC enablement. Definition of the connectors needed on the HPM or on the cable assembly for enabling this cabled OCP NIC option are outside the scope of this specification. The negative feature (cutout) must be sufficiently sized as to allow the ability to place the cable OCP NIC 4C+ connector such that Datum C and G locations are maintained per **Figure 9.** Refer to Implementation note in **Section 10.1.1** for additional information.

HPM shall implement battery backed voltage interface per DC-SCM R2.x "Battery Voltage" requirement.

Figure 9. Centerline Locations of OCP NIC R3.0 and DC-SCM R2.x



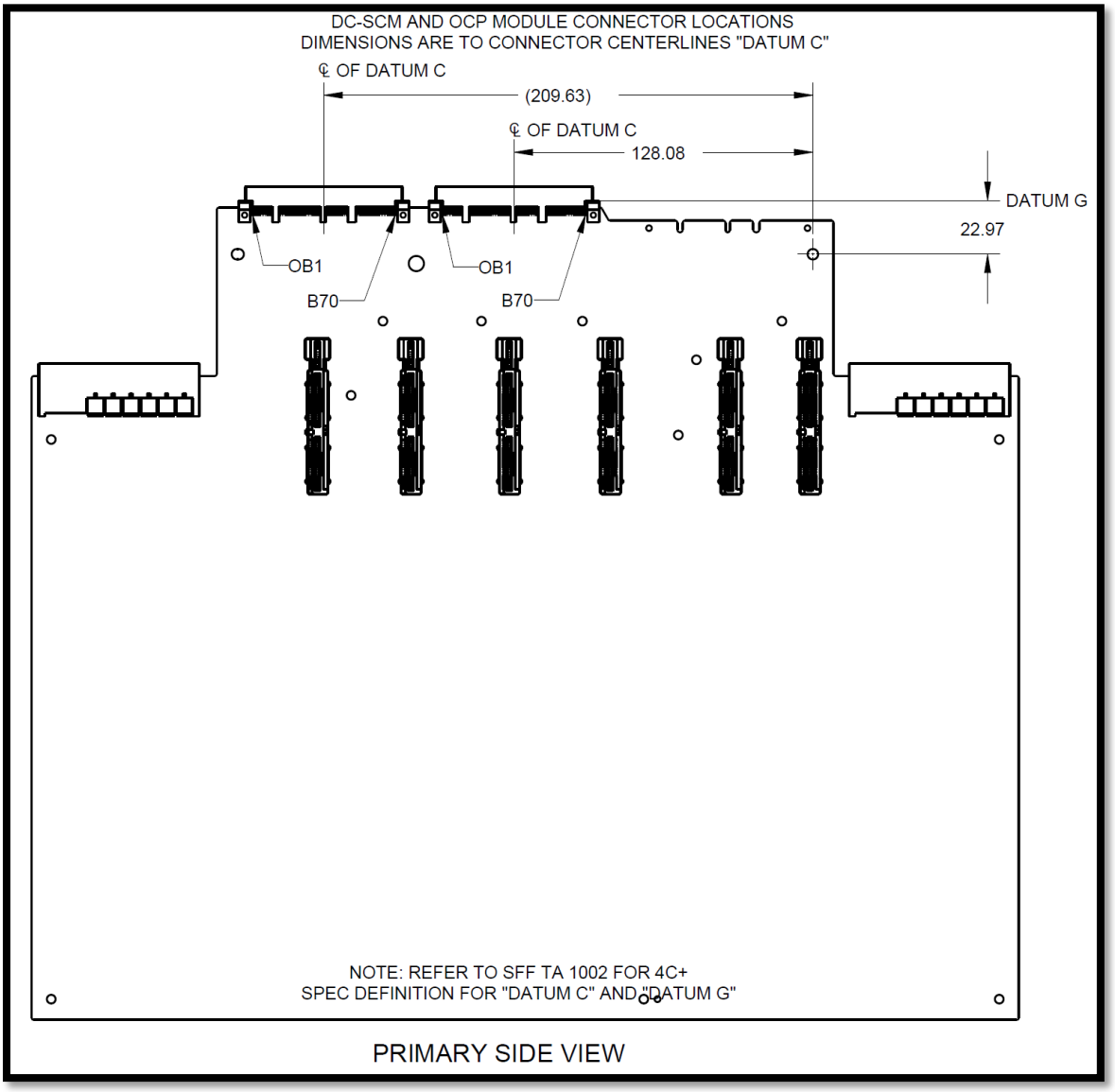
10.6. Platform Custom Zone

The Platform Custom Zone is defined as the Near Edge between the OCP NIC R3 and DC-SCM R2.x. (See **Section 9 HPM Layout**.) This area is intentionally undefined, so that System Designers may provide their desired features for the target platform. The Base Specification will define some options that are considered common use cases, to promote greater compatibility between future HPMs.

10.6.1. Second OCP NIC R3 Connector

A HPM may want to add a second OCP NIC R3 connector in the Platform Custom Zone. It is strongly recommended that HPM designs follow the recommended placement guidance in **Figure 10** for the second SFF-TA-1002 connector.

Figure 10. Location for Second OCP NIC R3 Connector in Platform Custom Zone

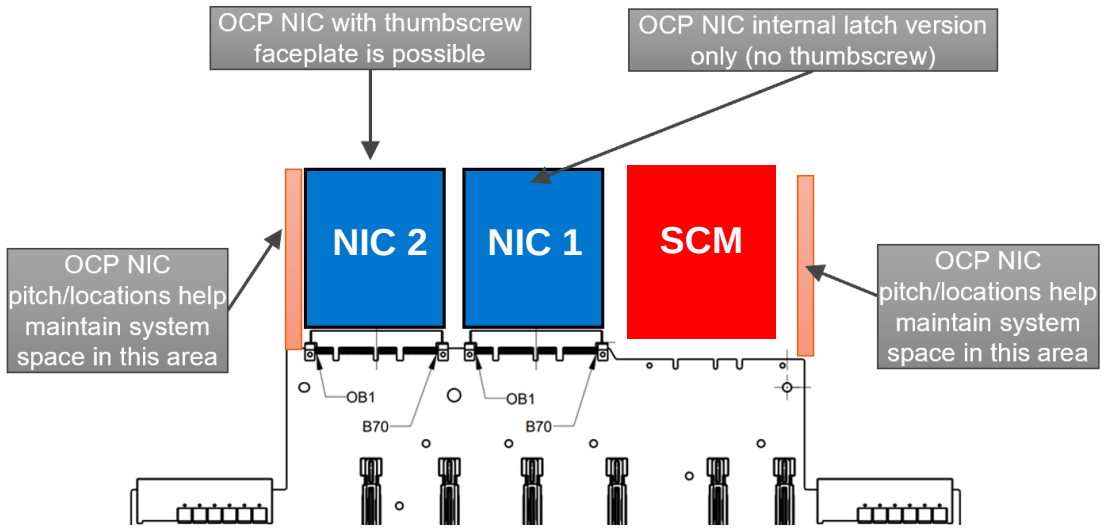


Implementors Note:

The pitch of the two OCP SFF NICs does NOT support the external thumbscrew for NIC 1 (a NIC 1 thumbscrew would trap NIC 2). It may be possible to support OCP NIC thumbscrew faceplate on NIC 2, but not in both locations.

The 2x OCP NIC connector locations were set to maximize space adjacent to M-CRPS. In a 1RU configuration with 3x LP CEM cards, the center LP CEM bracket traps NIC 1 from external hot plug, thus recommend using internal latch option for two SFF NICs.

All external devices on the user accessible face plate (as viewed from far side) are numbered starting with 1 and increment up left to right, top to bottom. When a second SFF NIC is added NIC 1 is now adjacent the DC-SCM and would be connected to CPU 1. In a dual NIC M-FLW system the primary OCP SFF NIC is numbered as NIC 2 which would still be attached to CPU 0.



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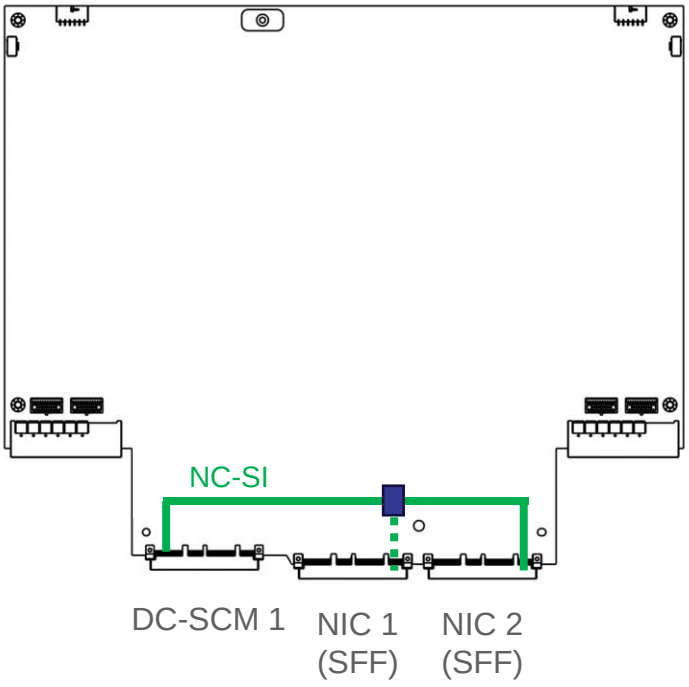
Implementors Note:

The DC-SCM DC-SCI is designed to support up to two RMII/NC-SI RMII-based transport interfaces, facilitating sideband communication between the DC-SCM to the NIC(s).

For DC-SCM applications utilizing a single NC-SI, it is advised to employ the first NC-SI interface instance (utilizing pins B43-B49). Upon integrating NIC 1 into the HPM, it is strongly recommended to establish an NC-SI RBT connection to NIC 1, rather than leaving it disconnected. The connection of NC-SI to NIC 1 can be achieved through one of the following methods:

1. A multidrop topology extending from the first NC-SI, or
2. An active MUX/Switch derived from the first NC-SI, or
3. A second NC-SI originating from the DC-SCM (illustration not provided).

The selection of the optimal topology is not covered within this specification; for further guidance, please consult the OCP NIC & DC-SCM Base Specifications. For additional information on NC-SI, refer to DMTF DSP0222.



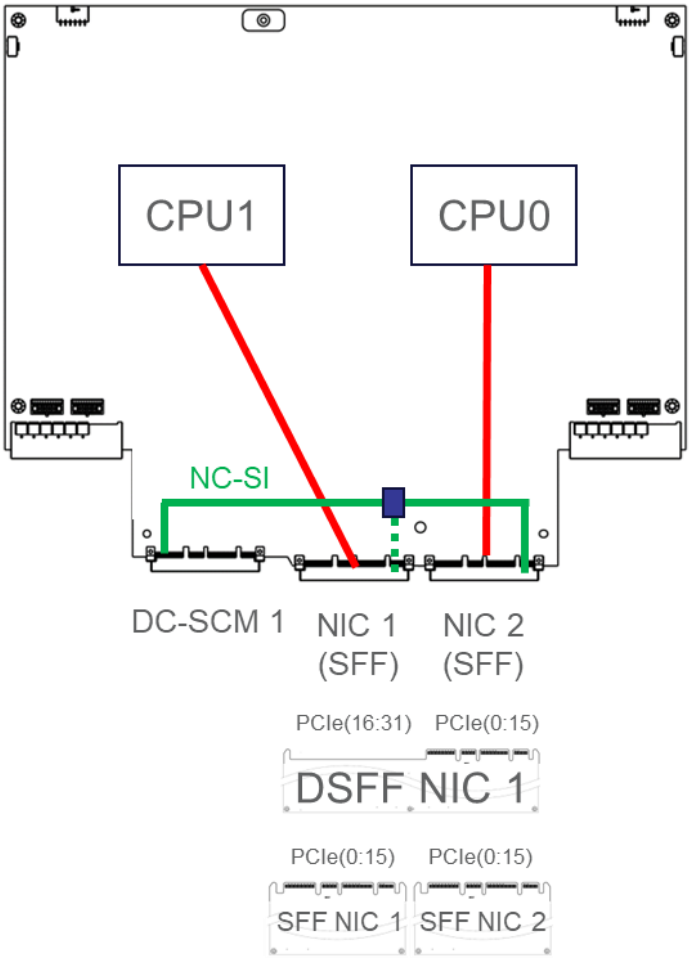
10.6.2. OCP NIC DSFF Enablement

The OCP DSFF NIC can be used in M-FLW. Guidance in Section 10.6.1 applies to DSFF Enablement as well. It is important to recognize caution when using the downshifted DSFF NIC with more than one CPU.

Implementors Note:

OCP DSFF NICs have the option to implement downshifting on the Secondary Connector card edge when operating with 16 or fewer lanes of PCIe and when the power consumption is 80W or less. It is important for HPM designers to recognize that NIC 2 (SFF) position is the DSFF's primary connector and shall always incorporate the sideband and power functionality.

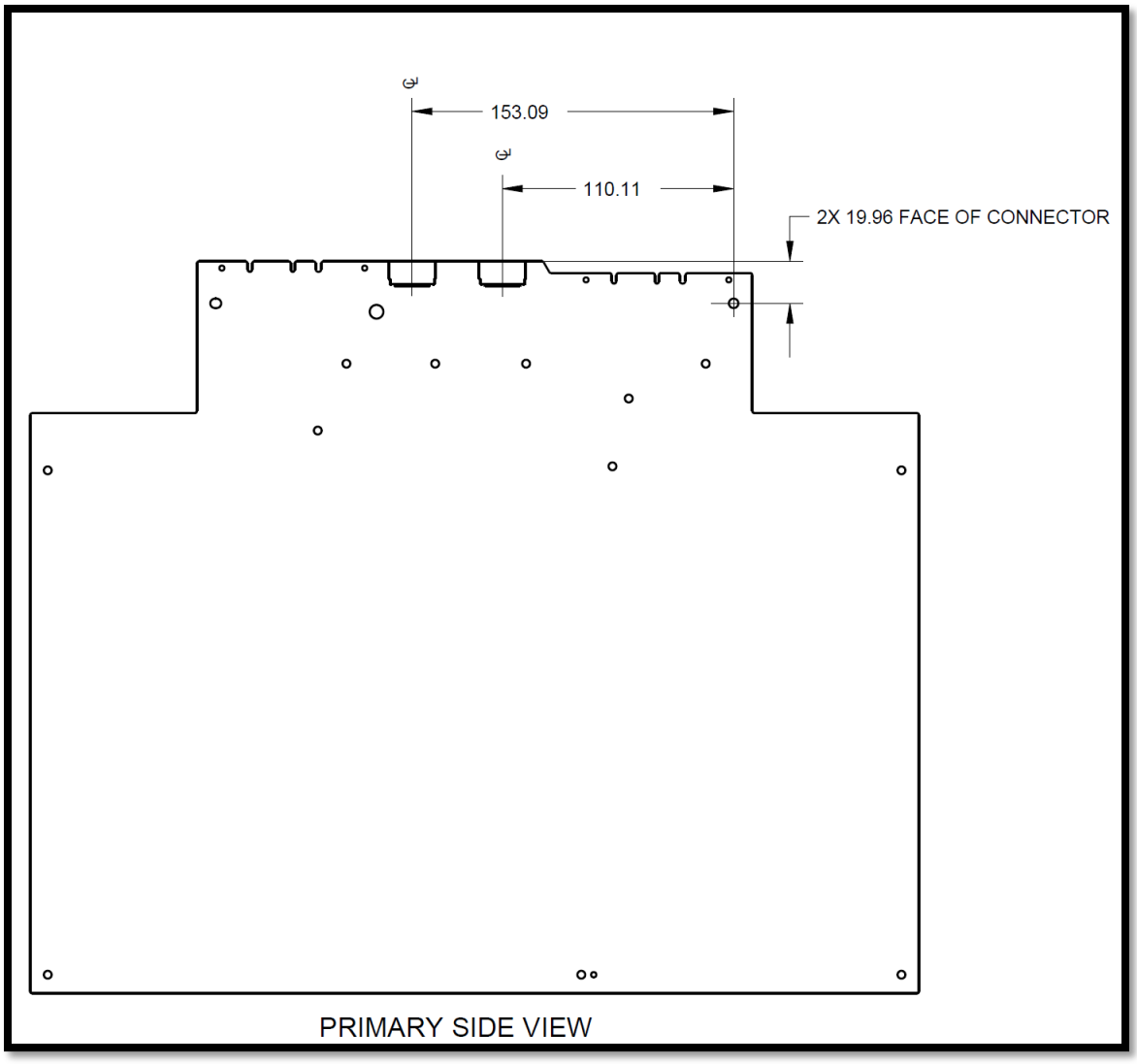
Given that the purpose of having two SFF-TA-1002 4C+ connectors is to accommodate either one DSFF NIC or two SFF NICs, the M-FLW Base Specification strongly advises HPM implementations to use a complete set of OCP NIC sideband functionalities on both the Primary and Secondary DSFF 4C+ connectors.



10.6.3. Direct Dock E1.S

An HPM design may want to support direct docking E1.S (EDSFF) in the Platform Custom Zone. These HPM designs should follow the following placement guidance for SFF-TA-1002, 1C connectors. See **Figure 11**. See M-PIC specification, chapter “E1.S Direct Attach Boot Storage” for complete connector and pinout guidance.

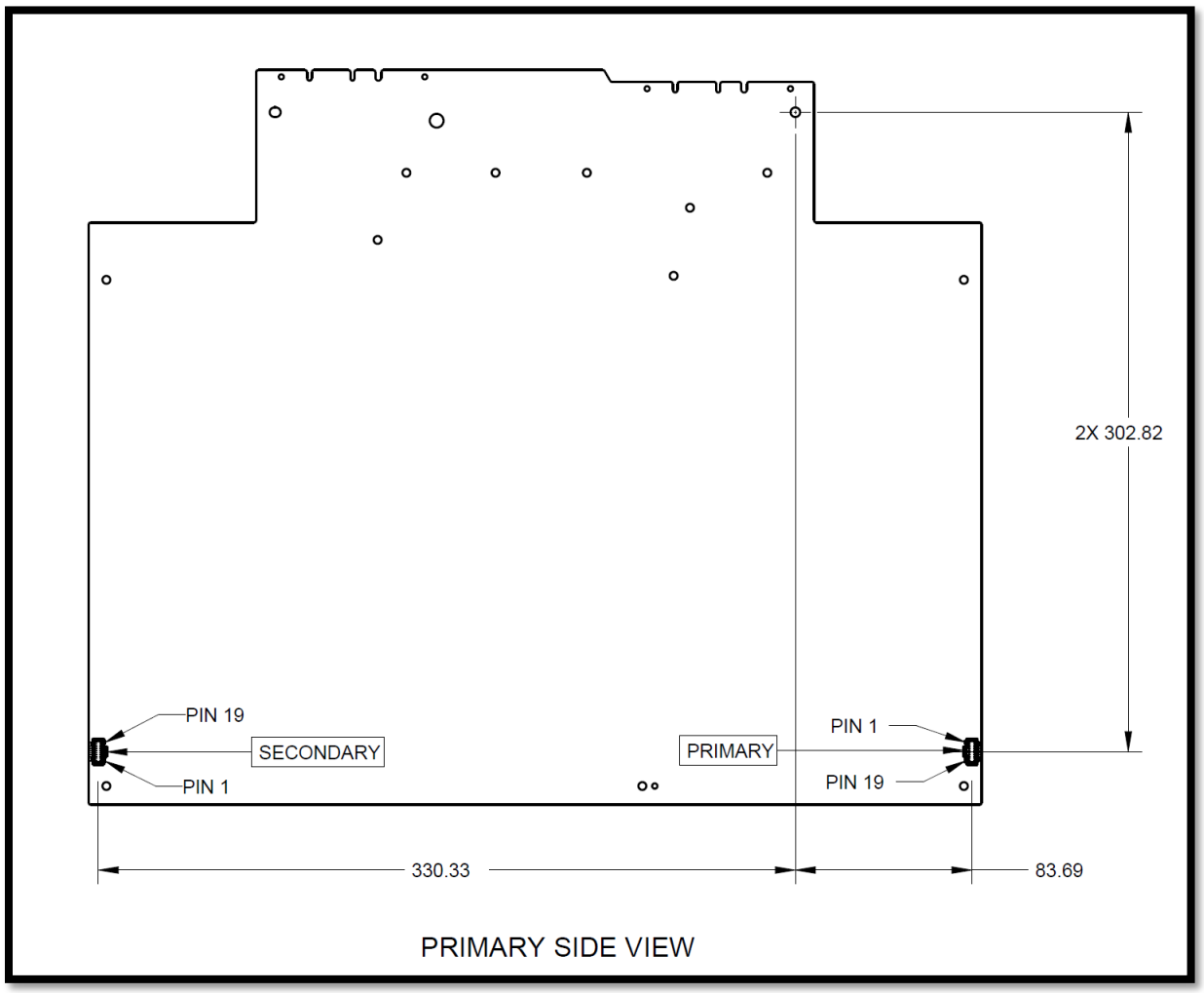
Figure 11. Direct Dock E1.S connector Enablement



10.7. Control Panel Connector Locations

The HPM shall implement two instances of the M-PIC defined Control Panel connections as shown in **Figure 12.** The Control Panel Connector details are further defined in M-PIC Section Reference: “Control Panel Interfacing”.

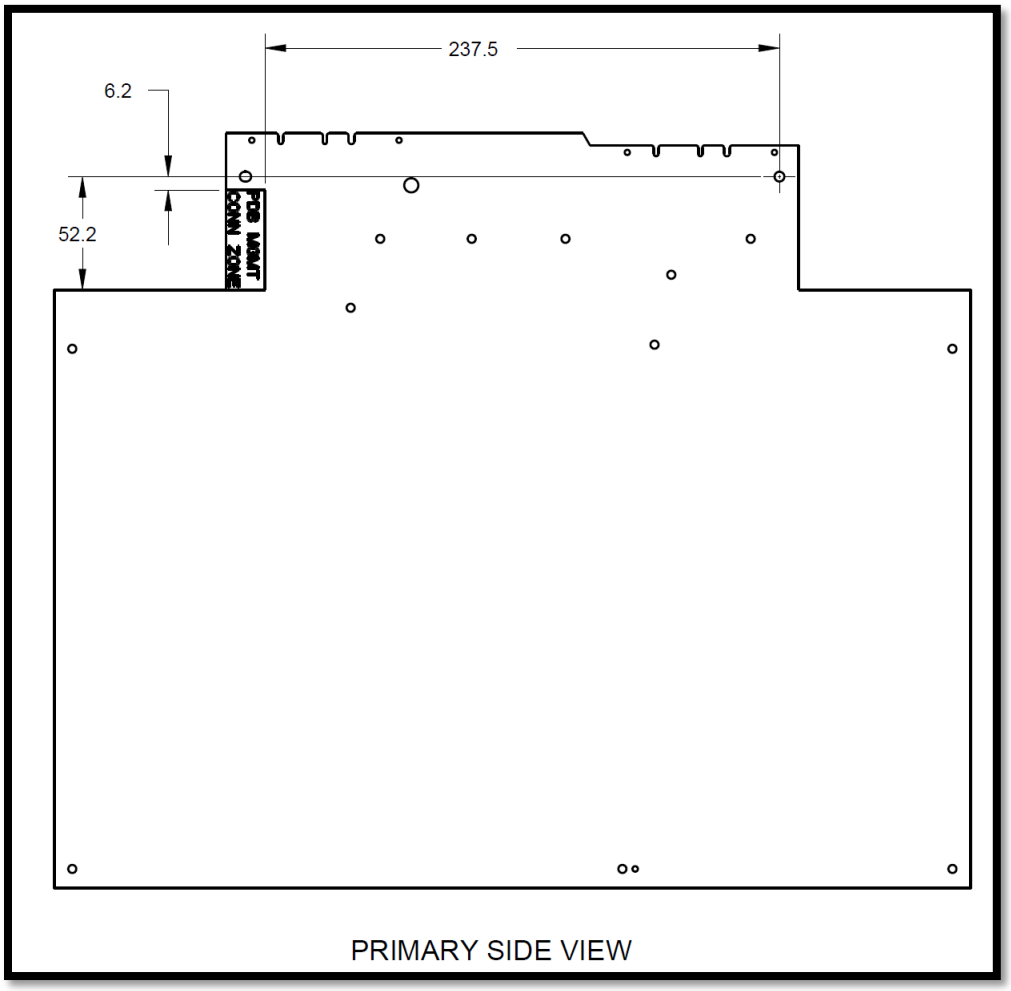
Figure 12. Control Panel Connection Locations



10.8. Zone for PDB Management Connector Header

The HPM shall implement a PDB Management Connector Header. The connector must be placed in the HPM within the zone defined by **Figure 13** (but can be depopulated in assembly BOM at a Design Specification level guidance). The PDB Management Connector details are further defined in M-PIC Section Reference: “PDB Management Connector Header”.

Figure 13. PDB Management Connector Header Location



10.9. Zone for Intrusion Switch and Internal Host USB3 Connection

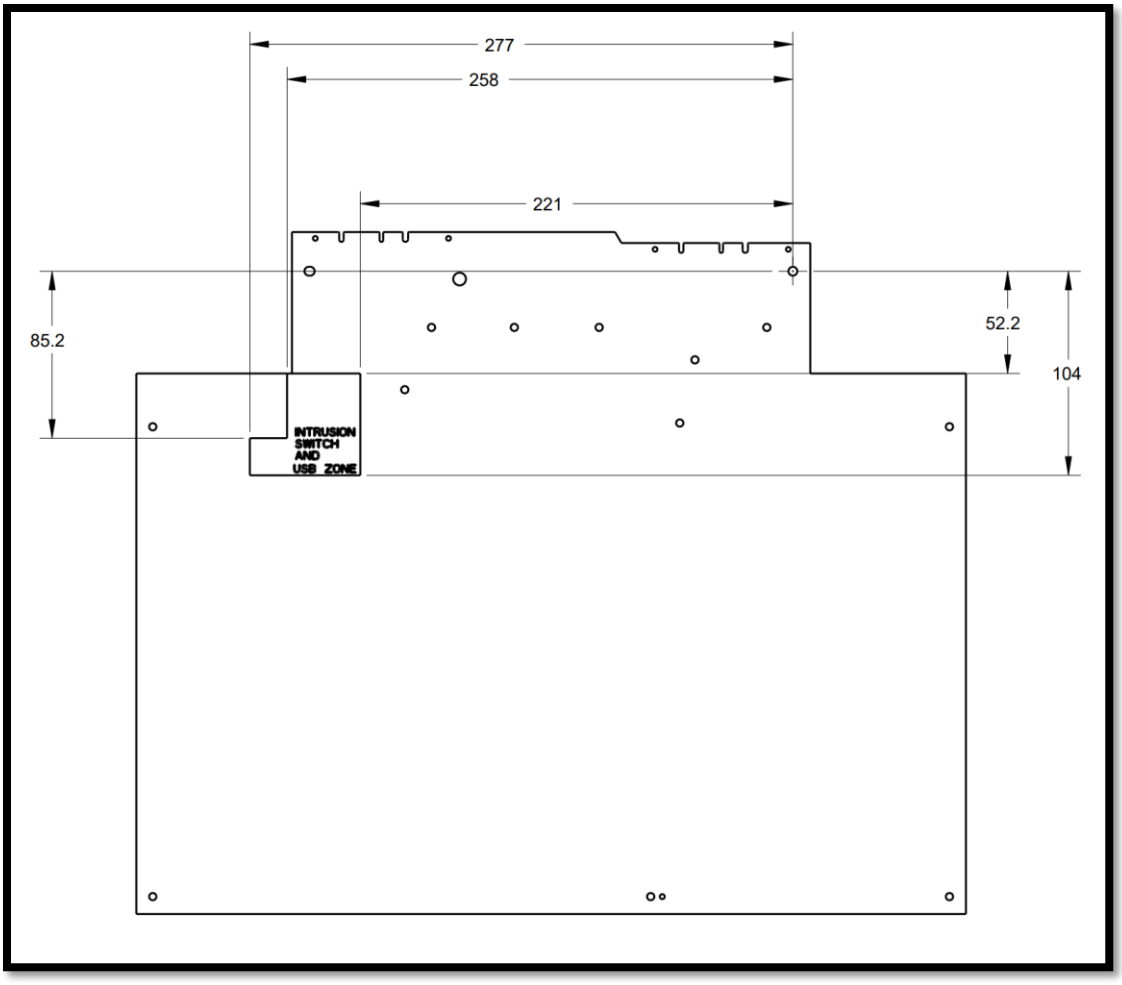
The HPM shall implement an internal USB3 connector. The connector must be placed on the HPM within the zone defined by **Figure 14**. The USB Connector details are further defined in M-PIC Section Reference: “Internal Host USB3 Connector”.

Implementors Note:

System and HPM designers should communicate on target devices for the internal USB connector and ensure heatsinks, add-in cards, or other system items are compatible with the devices or cables mated to the internal USB connector.

The HPM shall implement an intrusion switch connector. The connector must be placed on the HPM within the zone defined by **Figure 14**. The Intrusion Switch details are further defined in M-PIC Section Reference: “Intrusion Switch”.

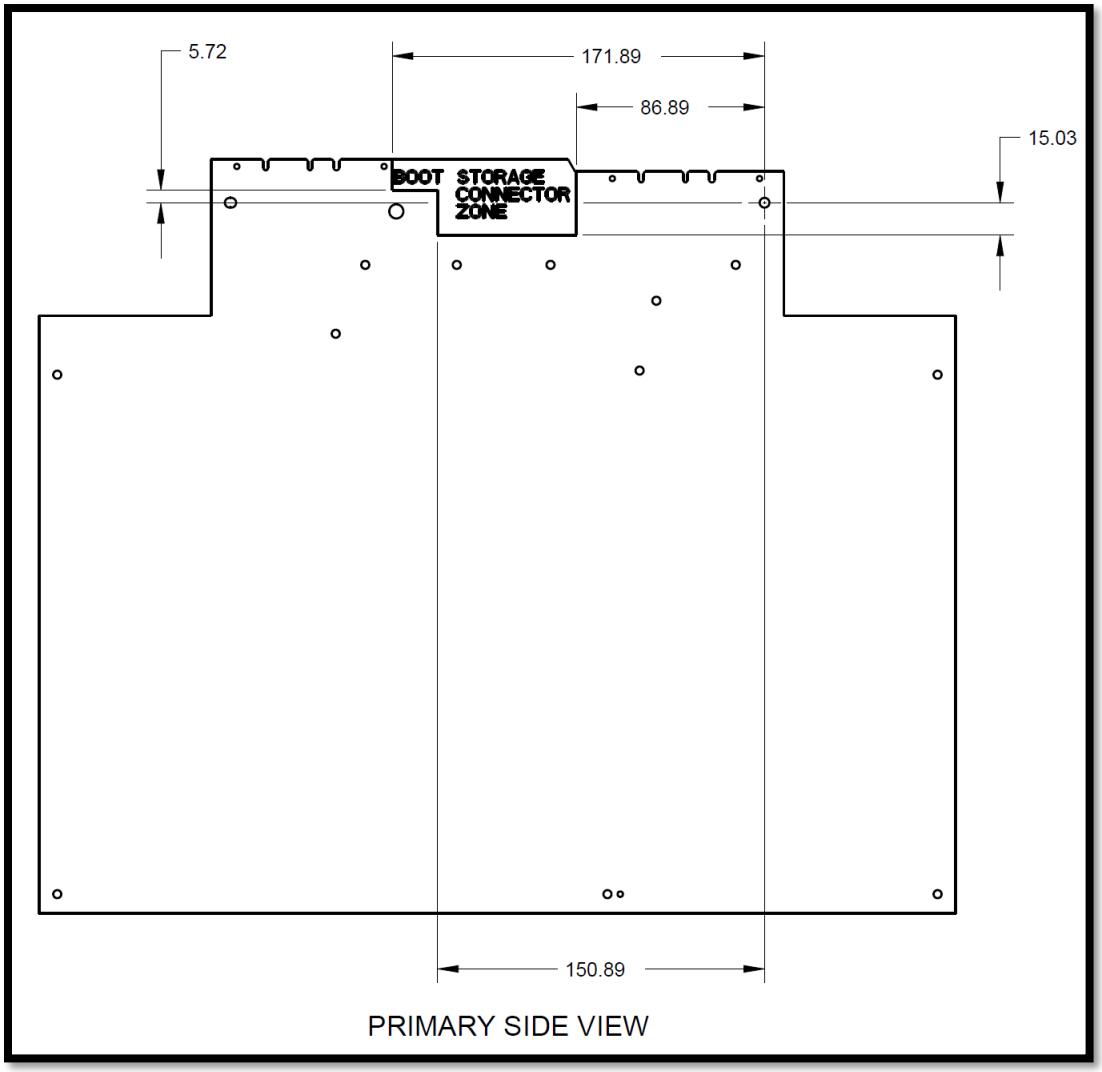
Figure 14. Intrusion and USB Connection Placement Zone



10.10. Boot Storage Connector Zone

The HPM is recommended to implement a Boot Storage Peripheral connector. The connector is recommended to be placed on the HPM within the zone defined by **Figure 15**. The Boot Storage Connector options and details are defined in M-PIC Section Reference: “Boot Storage”.

Figure 15. Boot Storage Connector Zone



10.11. High Speed I/O (HSIO) Connectors

This Base Specification seeks to allow for flexible high speed I/O (HSIO) routing options while also enabling HPM to system compatibility.

Board-to-Board (B2B) connections are defined as connections that mate two separate PCBs entirely without cabling. B2B connections are typically used to route HSIO from the HPM to a riser PCB or direct dock peripherals (i.e. DC-SCM R2.x, OCP-NIC R3).

Board-to-Cable (B2C) connections are defined as connections that mate two separate PCBs entirely with cabling. B2C connections are typically used to route HSIO from the HPM to a riser PCB or to other subsystems such as NVMe storage devices or backplanes.

Hybrid connections are defined as those which utilize both B2B and B2C elements to create a single mated interface between two PCBs. For example, if a Riser has a PCB with card edge fingers utilizing B2B to receive Power and Low Speed IO while also using a Twinax B2C connection for HSIO.

Implementors Note:

SFF-TA-1033 is an example of a connector supporting Hybrid connections, it can be used for B2B, B2C or Hybrid connections. While the HPM designer places the SFF-TA-1033, they do not necessarily know beforehand what style of connection the System designer will implement.

B2C

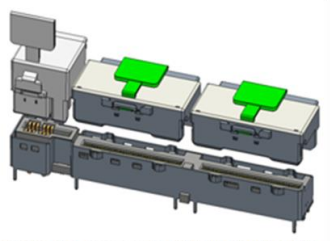


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

B2B

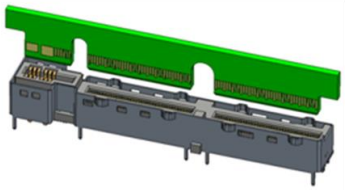


Figure 4-1 Combo x16+21A Power AIC Application

Hybrid

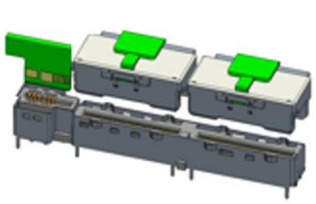


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

10.11.1. DC-MHS Compliant HSIO Connectors

All HSIO connectors shall be compliant with the M-XIO specification and are listed in **Table 3**. Refer to the **DC-MHS Connector List** for vendor part number details.

Table 3: M-FLW Specification Compliant HSIO Connectors

Use	Compliant Connectors
Near Side Fixed Risers Locations	SFF-TA-1033 (with 21A Power)
All Other HSIO	SFF-TA-1016 SFF-TA-1026 SFF-TA-1033

Note: Additional connectors may be added to future revisions of this specification *after* electrical definition by M-XIO.

DC-MHS HPMs allow for B2B, B2C or Hybrid risers. For best compatibility with many DC-MHS system designs, HPMs should implement riser connectors adhering to the guidance in **Section 10.11.2**

All other HSIO connectors adhere to common guidance in **Section 10.11.4**

Implementors Note:

HSIO cable choices are outside the scope of M-FLW. The SFF-TA-1016 and SFF-TA-1033 connectors can accept both cable types, but mixing cable/connector types may result in loss of the anti-tilt feature.

10.11.2. Near Side Fixed Riser Connectors

A DC-MHS riser may utilize B2B, B2C or Hybrid connectivity schemes. Riser and other endpoint device definition and implementation details are outside of the scope of this specification.

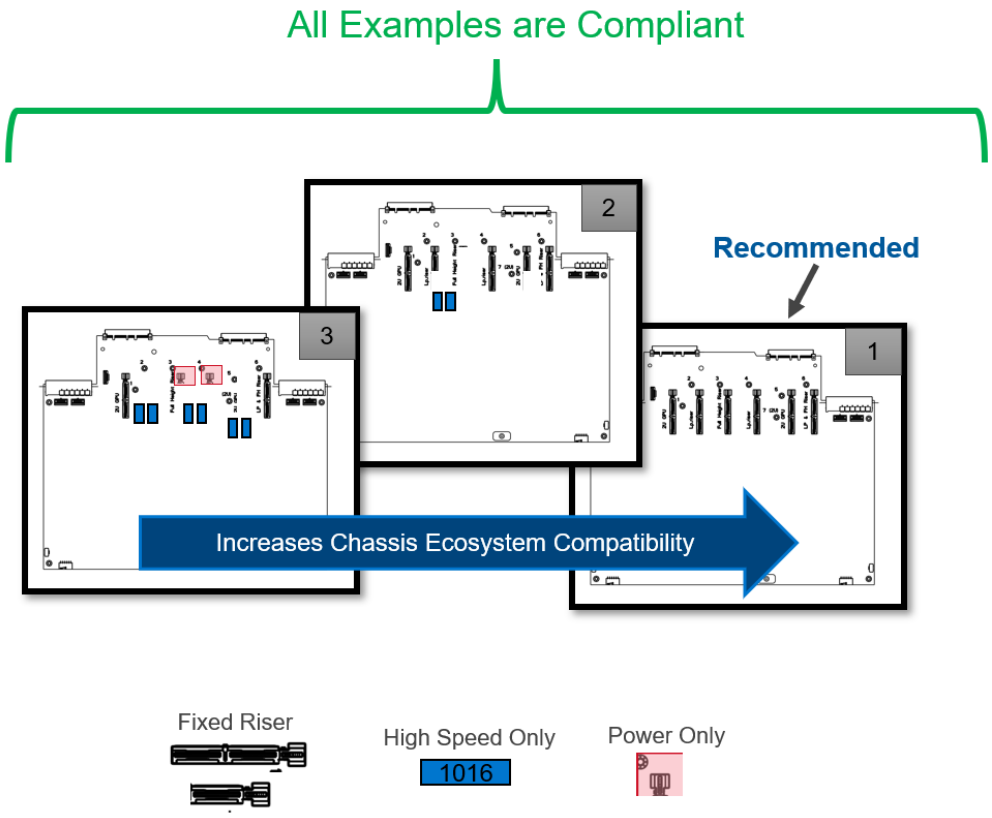
HPMs which implement near side fixed risers shall:

- Use a Fixed Riser connector defined in **Table 3**
- Place them in the location(s) defined in **Figure 16**

Full population of all Near Side Fixed Risers Locations is not required, as there may be technical or other reasons to exclude certain positions. It is recommended to implement as many fixed riser locations as possible.

Implementors Note:

For maximum ecosystem compatibility, designing an HPM to utilize as many Fixed Riser locations as possible is strongly encouraged. Utilizing these connectors in a fixed location allows System Designers to use B2B, B2C or Hybrid connections as best suits their use case. In the figure below, all three M-FLW examples are compliant, however, “Layout 1” is recommended because it implements all defined Fixed Riser connectors.

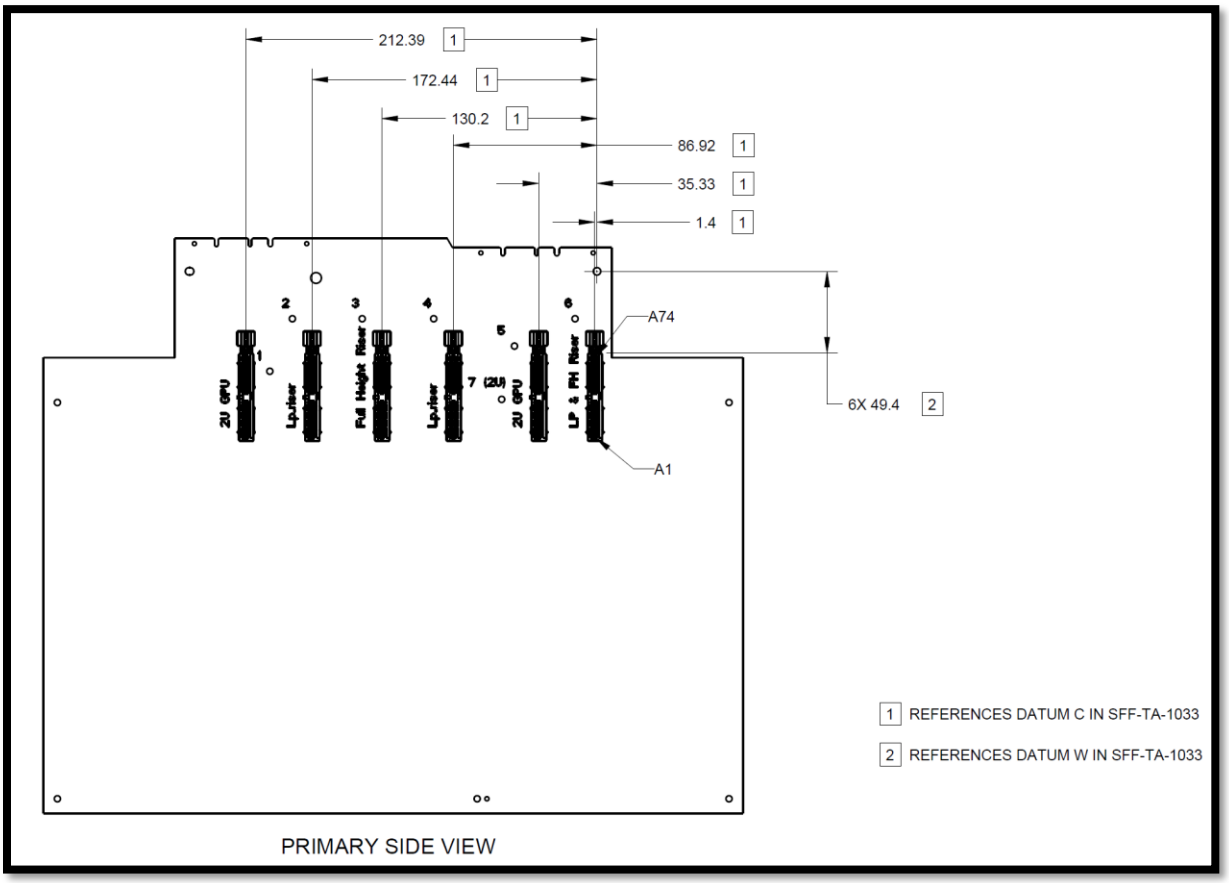


10.11.3. SFF-TA-1033 Fixed Riser Implementation Details

SFF-TA-1033 fixed riser connectors which are implemented shall follow **Figure 16** which define the required location of the SFF-TA-1033 connectors.

Note that SFF-TA-1033 has various versions. All SFF-TA-1033 Near Side Fixed riser connectors shall use a 21A power block version. Refer to the **DC-MHS Connector List** for vendor part number details.

Figure 16. Near IO Riser Connector Locations



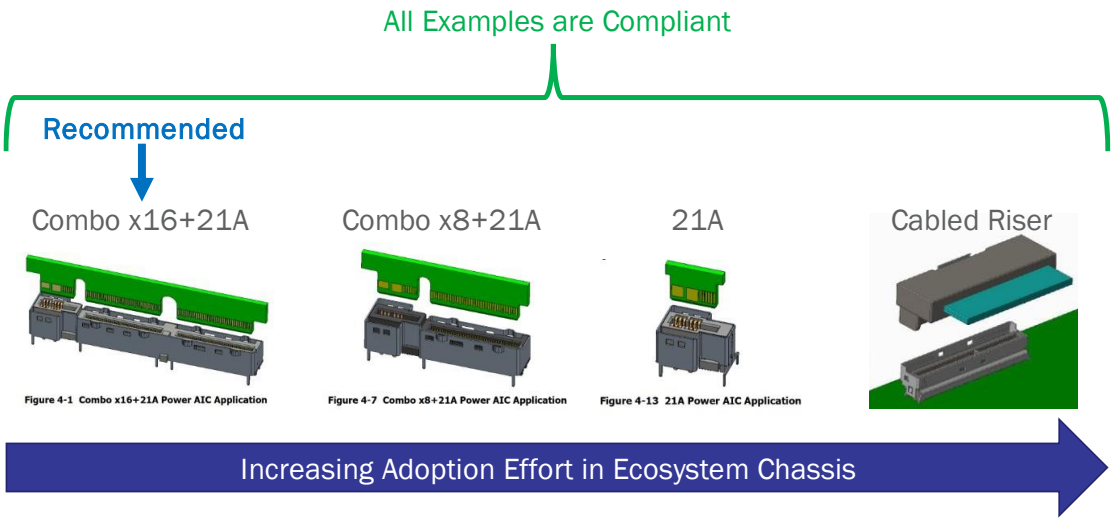
For further explanation on which mounting holes are associated with its Near IO connectors, see **Figure 38. Riser Retention Holes and Associated Near XIO Locations** in the Supplemental Information section.

Implementors Note:

Use of the Combo x16+21A connector, wired as a x16, is highly recommended for ecosystem compatibility. If HPMs are unable to support the maximum number of Fixed Riser connectors, it is recommended that the HPM designer consider reduced ecosystem compatibility in the following order:

1) Use the SFF-TA-1033 Combo x16+21A, wired as a x8 in compliance with M-XIO
2) Change the SFF-TA-1033 Combo x16+21A to the SFF-TA-1033 Combo x8+21A
3) Change the SFF-TA-1033 Combo x16+21A to the 21A Power only
4) Change to a B2C Riser with connectors adhering to **Section 10.11.4**

SFF-TA-1033 Fixed Riser Connector Options



10.11.4. Other HSIO Connectors

Except for the Fixed Riser Connectors described in **Section 10.11.3**, HSIO connector positions and quantity are not defined by this DC-MHS Base Specification. The HPM Designer is free to place them wherever they wish so long as they do not interfere with other required features (e.g. a required mounting hole) and while adhering to the component height restrictions in **Section 10.12.**

All implemented HSIO connectors shall be defined in M-XIO and listed in **Table 3.** Any combination of these connectors is allowed.

10.12. Primary Side Component Height Restriction Zones

A Component Height Restriction Zone shall be required, per **Figure 17. Zones for Primary Side Component Height Restrictions** which applies to all soldered components; exceptions noted below.

- The **12mm Zone** is intended to allow for extended heatsinks and other thermal solutions while not prohibiting cabling of HSIO. Adherence to the 12mm zone is strongly recommended. While deviations are allowed, HPM designers should limit component selections which exceed the restriction to reduce interference with system design elements which will expect to inhabit this space and may cause system compatibility issues.
- The **11.3mm Zone** is intended to avoid interference with PCIe CEM cards directly above the HPM and its peripherals. Adherence to the 11.3mm Zone is required.
- Cable routing channels along HPM edges

If a cable connection (power, High speed IO, etc) is placed in the component height restriction zone, the max height restriction shall apply to the mated height of the plug and cable assembly, including component and assembly tolerances; exception noted below.

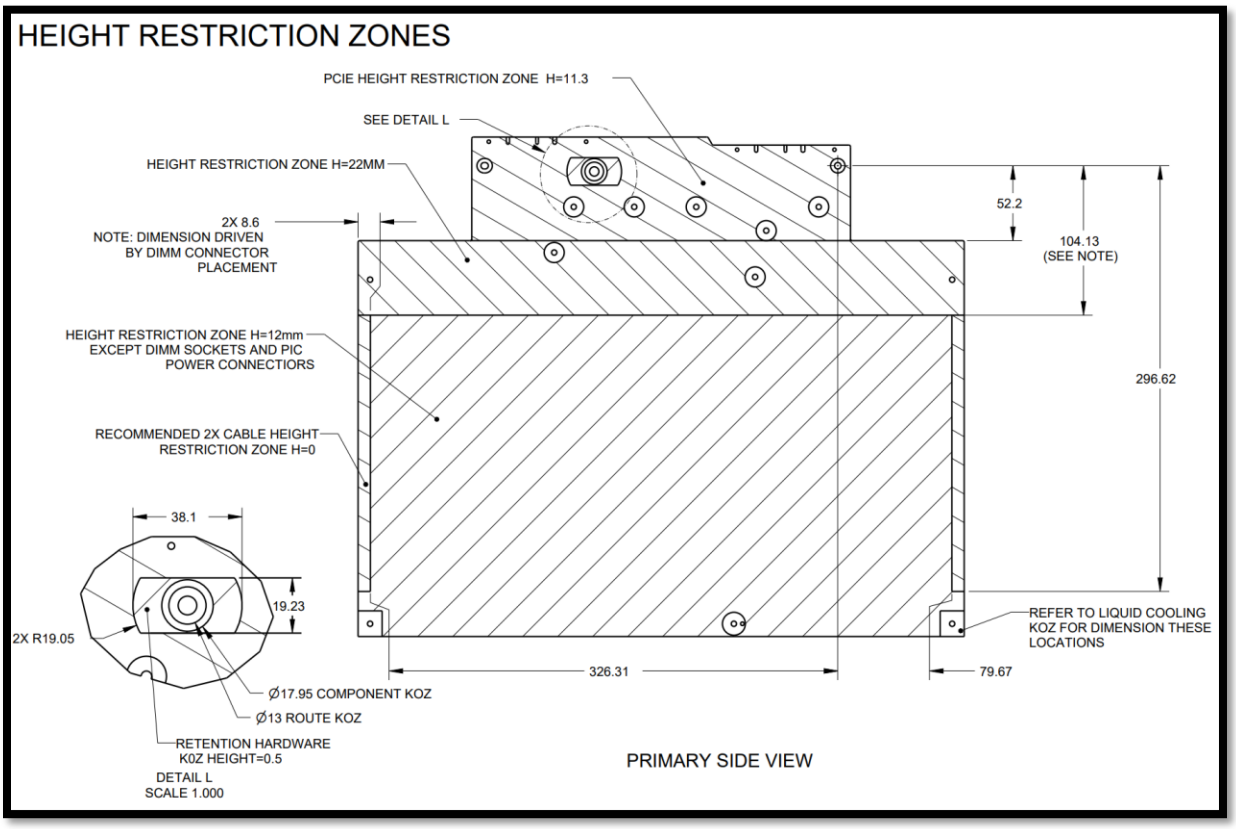
The exceptions allowed are:

- Special exceptions specified per zone in **Figure 17. Zones for Primary Side Component Height Restrictions**, such as DIMM sockets
- DIMM Connectors
- Zones that are classified as Recommended.
- The required Near IO connector (SFF-TA-1033 in **Section 10.11.1**) mated cabled height can exceed the 11.3mm height zone restriction.
- Internal USB connector interfaces (ie, cables, USB keys) may exceed either 11.3mm or 22mm height restriction zone.
- SFF-TA-1016 and SFF-TA-1026 connectors may be placed in the 11.3mm and 12.0mm Component Height Restriction Zones. The mating plugs for these connectors may exceed the HRZ depending on which connectors and plug types are chosen. As a result, an exception is allowed for these two connector types in the 11.3mm and 12.0mm HRZs. HPM designers should place these connectors with careful consideration of potential system use cases for their HPM.

The dimensions indicated in **Figure 17. Zones for Primary Side Component Height Restrictions** are maximum heights. Component and assembly (solder) tolerances must be chosen to stay within the maximum height.

For thermal solutions, one must consider the allowable variance in numbers, types, and location of Compute Core items. Thus, a fixed 12mm for component height restriction in the Compute Core area is intended to allow air cooling heatsinks or liquid cooling hardware of any variance. All other soldered board components must comply with exceptions noted in **Figure 17**

Figure 17. Zones for Primary Side Component Height Restrictions



Implementation Note:

The Height Restriction Zones defined in **Figure 17. Zones for Primary Side Component Height Restrictions** apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of solder components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

It is assumed that items such as CPU heatsinks, VR heatsinks, and shrouds are all designed by System Designers. And thus, the height and location tradeoff between these items are assumed responsibilities of the System Designer and not the HPM designer. The HPM Designer should consider best practices when making component placement choices. This makes no assumptions on the compatibility of Chassis, Peripherals or Thermal solutions. For future chassis and HPM compatibility, a System Designer is advised NOT design elements that intersect with the Height Restriction zone (Fans, Heatsinks, Risers, etc).

Recommended Cable Zero Height Restriction Zone: It is strongly recommended to implement a keepout zone to left and right of outermost DIMM sockets with a minimum dimension to HPM edge of 8.6mm, shown as Cable Height Restriction Zone in **Figure 17. Zones for Primary Side Component Height Restrictions**

This keepout is to enable HSIO cabling, power cabling and other platform infrastructure cabling to traverse from Near Side to Far Side zones, as needed by Platform Designers. (Designers should consider differences in DIMM socket widths from various vendors when determining DIMM placement.)

Implementation Note:

In some cases, a Compute Core design may only be able to deliver a desired capability by violating the cable keepout zone. By doing so, an HPM will cause issue with a platform's ability to cable High-Speed IO and Power delivery. In this case, a HPM Designer should make efforts to collaborate with Platform Designers on:

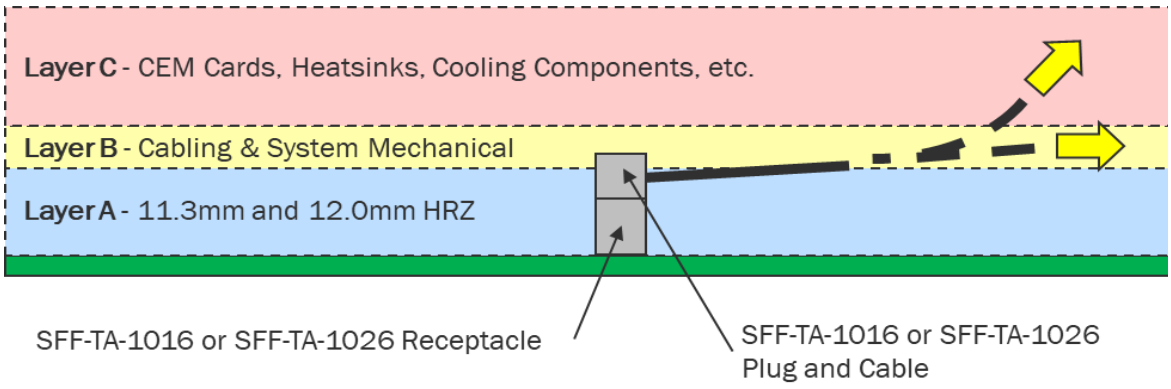
1. Increasing Near Side to Far Side power delivery and power egress capability to mitigate loss of power cabling

2. Identify available cabling space for High-Speed IO to meet a given platform configuration.

3. Adjusting DIMM pitch to enable cables should be considered.

Implementors Note:

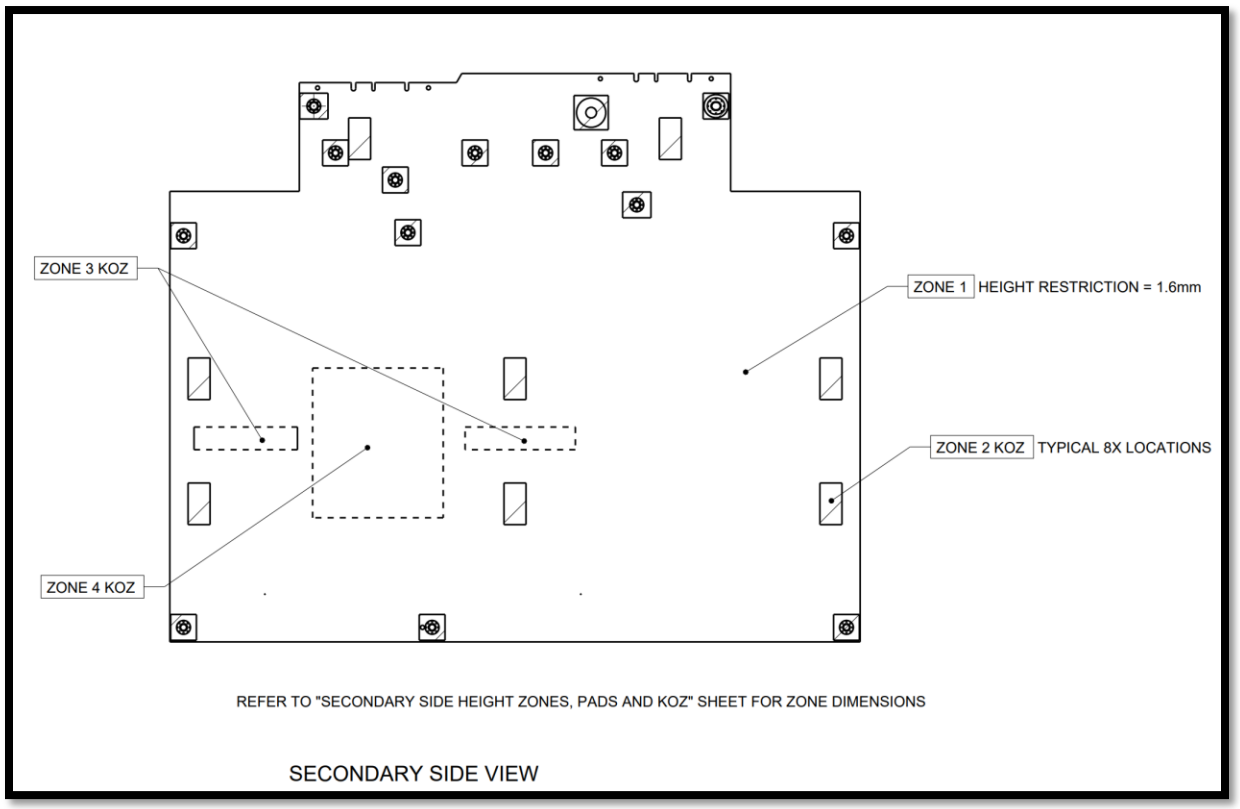
A height exception may be needed for the SFF-TA-1016 & SFF-TA-1026 connector + cable plug based on an understanding that a system design layer exists between the HPM HRZs (Layer A) and the Major Component Layer of a system (Layer C). Layer B is a mechanical design layer where cabling may route and sheet metal structures may be created in the system's chassis design. A system designer needs to understand the mated heights of plug + receptacle for the SFF-TA-1016 and SFF-TA-1026 connectors to be able to accommodate their occasional and purposeful intrusions into Layer B.



10.13. Secondary Side Zones and Height Restrictions

There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 18**. Each zone serves a unique purpose, defined in the following sections. Zones 1, 2, 3 and 4 are defined as requirements for compliance.

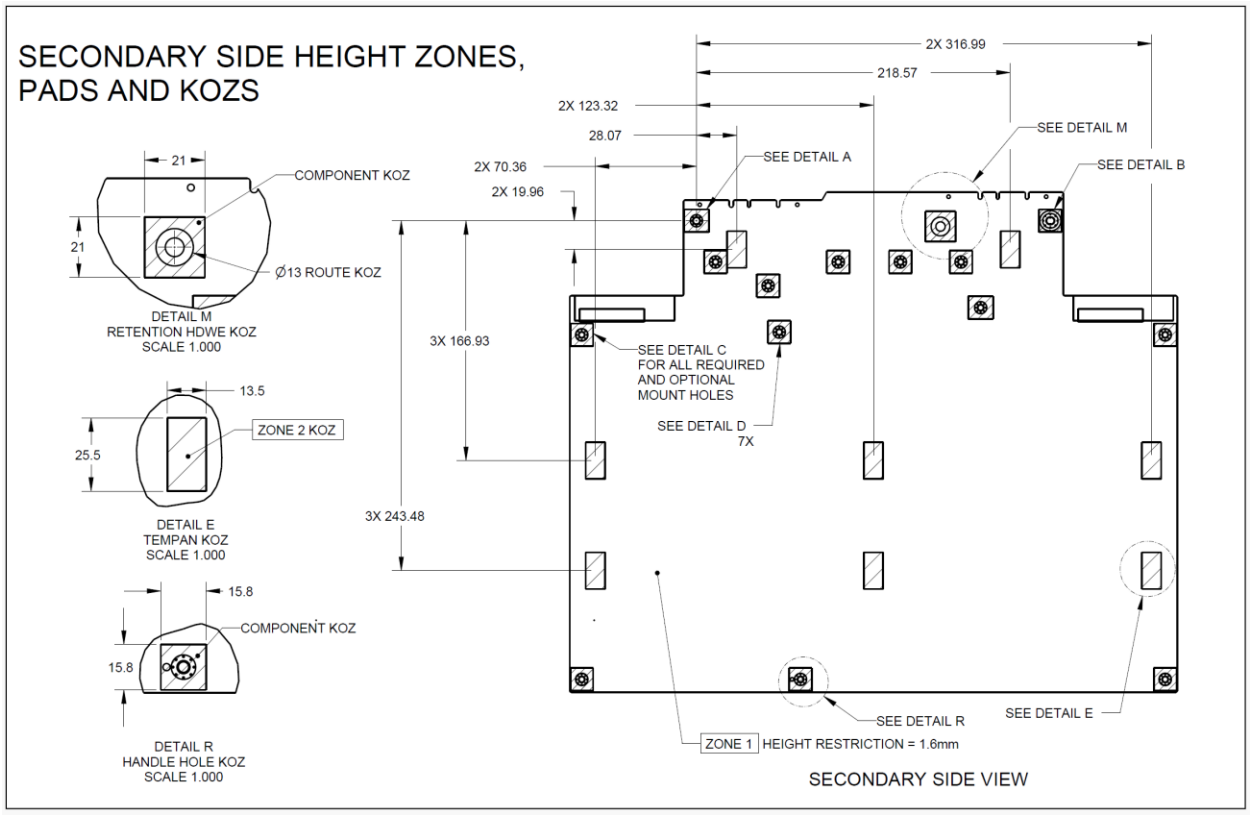
Figure 18: Secondary Side Height Restriction Zone and KOZ Definitions



10.13.1. Zone 1, Secondary Side Height Restriction

Zone 1 universally applies to the entire secondary side of the HPM, except for the defined Zones 2, 3, and 4. HPM electrical components are expected to utilize Zone 1. Zone 1 shall have a universal height restriction of 1.6 mm (exceptions noted in specification), per **Figure 19**. This is to ensure HPM component clearances to chassis base or board pan structure. This is especially important with a max allowable board thickness defined in **Section 10.14 HPM Board Thickness.**

Figure 19. HPM Secondary Side Height Keepout Zones, Pads, KOZ



Detail Views A – D that are referenced in this figure are in **Table 2. Board Hole Detail Views, with Pad and KOZ Details**

10.13.2. Zone 1 Exceptions for Secondary Side Tall Component

In some instances, an HPM Designer or System Designer, may desire tall secondary side components (such as special capacitors) that exceed the secondary side height restriction. Although this should be avoided, a HPM Designer may implement local exceptions if the following conditions can be met:

1. Exceptions are contained to small areas of the secondary side and shall not to exceed 400mm^2 area per instance.
2. No two instances of a secondary side exception shall be closer than 10mm, as to not drive excess cutouts in Chassis-to-HPM bracketry

It is recommended that (HPM Thickness + Height of Components) in Exception Areas never exceed 5.2mm. This total height enables common 2mm components on all compliant HPM thicknesses while mitigating potential system compatibility issues, for example:

- • 5.2mm – 2.36mm thick HPM = 2.84mm max component thickness
- • 5.2mm – 3.18mm thick HPM = 2.02mm max component thickness

Care should be taken to ensure that there is no risk if components in exception areas touch uninsulated chassis elements.

Implementors Note:

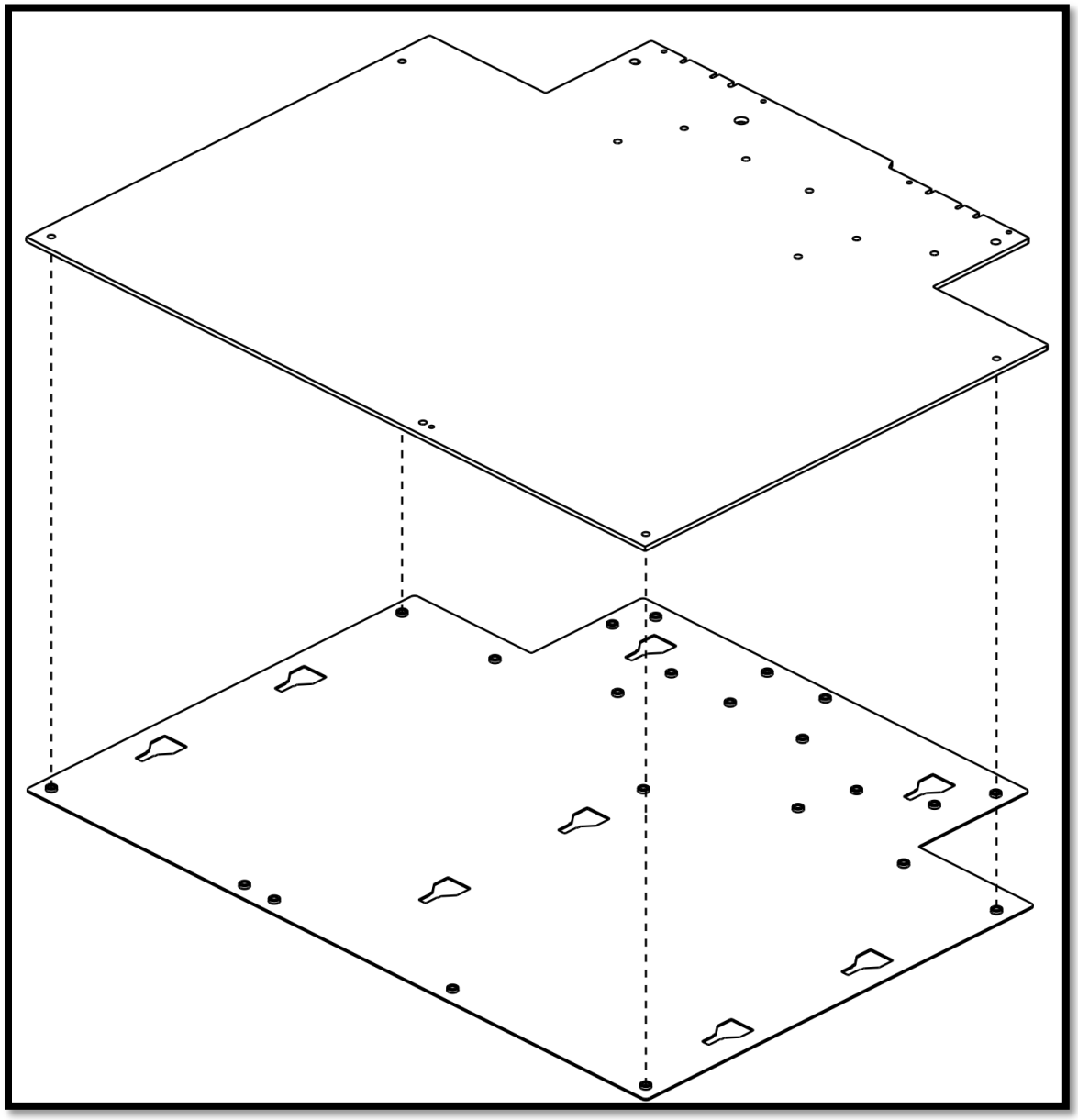
Secondary side exceptions for tall components may cause compatibility challenges between the HPM and System. HPM designers should work closely with the intended System Designers to ensure the exception locations and specific component heights are acceptable.

Numerous considerations outside the scope of this specification will determine the severity of compatibility issues. Examples include but are not limited to shock and vibration, chassis mechanical features, HPM uniformity, tolerancing, solder thickness, etc.

10.13.3. Zone 2, Chassis-to-HPM Bracket KOZ Requirements

The M-FLW HPM shall be designed to fit a Chassis-to-HPM Bracket (Board Pan) that enables different board layouts and mounting hole locations between different Compute Core designs while still maintaining compatibility to a common chassis design. Example shown in **Figure 20**.

Figure 20. Example of Chassis-to-HPM Bracket (Board Pan)



There will be fixed chassis hooks interfacing to the chassis-to-HPM bracket that require the Zone 2 zero height KOZ on HPM Secondary side. There shall be eight Zone 2 (0-height) KOZs implemented as defined in **Figure 19. HPM Secondary Side Height Keepout Zones, Pads, KOZ**. For an example of chassis hook concept, see **Section 14.7**.

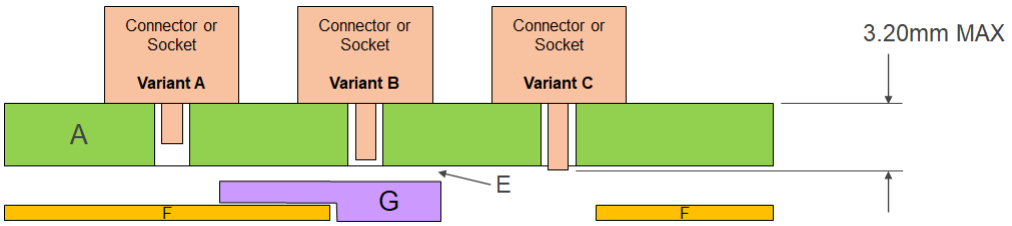
The geometry of the chassis hook is not specified and is a design choice for System Designer. Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb shall be 3.20mm MAX.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout.

Implementors Note:

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly. Refer to **Table 4. Example Z-Height Compliant Stack-Up, Per Zone** for definition of 'A', 'E', 'F' and 'G' the diagram.



10.13.4. Zone 3, HPM Secondary Support Requirements

HPMs may require secondary side support under the DIMMS and other semi-supported areas where HPM deflection is likely to occur during normal assembly processes. Two common design approaches to provide this support are:

1. HPMs can identify and provide areas for chassis designs to directly support the HPM PCB surface. These areas need to be clearly identified and free from any conductors or risk of shorting (no exposed vias, traces or components). Chassis designers may choose to support these areas with Board Pan formed features (metal) or bumpers/fillers (rubber or plastic).

2. HPMs can include bumpers or fillers in their design that are tuned in Z height (2.12mm +/- 0.10mm) to match with the Board Pan and exceed the height of all bottom side components.

Figure 21: Example Secondary Side Supports



10.13.5. Zone 4, CPU Backing Plate Requirement and Examples

The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by:

1. Backing Plate allowed Height = 6.2 – HPM thickness - 0.08mm standoff height tolerance – allowances for other backplate design requirements (insulators, deflections, etc)
2. See Implementors Note below for examples.

Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and/or HPM sled as represented by area 'C' in **Figure 25**.

Implementors Note:

HPM and CPU designers should consider these example Scenarios supported by DC-MHS HPM and Backing plate thickness requirements.

Board Thickness (Nominal, mm)	Maximum Allowable CPU Backing Plate Assembly Thickness (mm)
1.57	4.55
1.93	3.19
2.36	3.76
2.55	3.57
3.18	2.94

10.14. HPM Board Thickness

- The maximum allowed thickness and zone heights in the specification assume a minimum 6.2mm board mounting height.
    - Thickness and zone heights are established to ensure forward compatibility with 1U & 2U System Chassis assumptions.
    - Exceeding the thickness and zone height target values would result in system design impacts and incompatibilities.
    - The board mounting height for a given system is not within scope of HPM specification and is at discretion of the System designer.
- The maximum allowed HPM thickness is 3.18mm nominal and assume +/-10% tolerance is allowed.
    - Note that PCB Tolerances of +/- 10% are supported but are not a factor in determining the fit of the CPU Backing Plate when the HPMs are mounted to standoffs by their bottom surfaces.

Implementors Note:

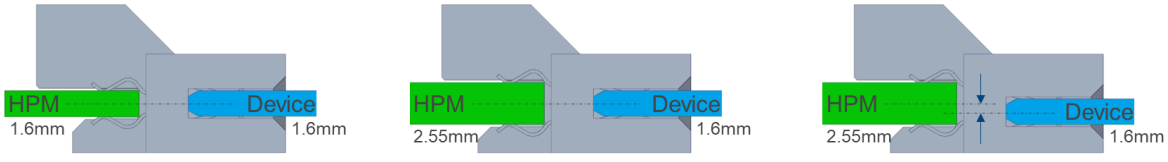
Offset connector choices and requirements may vary if a common chassis design needs to support varying HPM thicknesses. For the M-FLW specification, this could include connectors for OCP NIC R3 and DC SCM R2.x.

Failure to choose the proper offset could result in peripheral card not aligning to the chassis opening, demonstrated by card alignment in the figure below.

There is no recommendation for connector offset for MHS compliance. Connector offset is out of scope of DC-MHS HPM specifications.

Connector offset is a BOM (bill of material) choice by the system designer or HPM designer.

Refer to the latest OCP NIC R3.0 and DC-SCM R2.x specifications for a list of connector choices available at the time those specifications were published. Refer to connector vendors for the latest connector offset options.



0mm Offset, Top Surfaces and Centerlines Aligned

0mm Offset, Top Surfaces Not Aligned but Centerlines are Aligned

Negative Offset, Top Surfaces and Centerlines Not Aligned

Implementors Note:

HPM and Chassis designers should consider the height stack-up of each of the four zones identified in **Section 10.13**. **Table 4** and **Figure 22** through **Figure 25** demonstrate an example of a compliant stack-up for consideration. Note that the "total Z" value across the four zones must always be equivalent (maximum allowed value of 6.2mm shown for example only).

Table 4. Example Z-Height Compliant Stack-Up, Per Zone

		Zone 1	Zone 2	Zone 3	Zone 4	
Item	Description	Z Value (mm)	Z Value (mm)	Z Value (mm)	Z Value (mm)	Notes
A	HPM	3.18	3.18	3.18	3.18	MAX Thickness (w/o Added tolerance, Assumes bottom mounting)
B	Bottom Component Z	1.60	0			MAX Height
C	CPU Backing Plate				2.94	MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray
D	HPM Bottom Support			2.12		HPM Support Thickness +/- 0.10mm, must exceed Bottom Component Z
E(1)	Needed Gap	0.62	0.58			Gap is Larger, Requires Insulation and/or Clearance
E(2)	Resultant Gap			0.10	0.08	Gap is small, contact between parts is either Desired or Permissible
F	Board Pan	0.80		0.80		
G	Chassis Hook		2.44			MAX Height from Inside Surface of Chassis
	TOTAL	6.2	6.2	6.2	6.2	Example Solution Stack-up

Figure 22: Secondary Side Components (Zone 1)

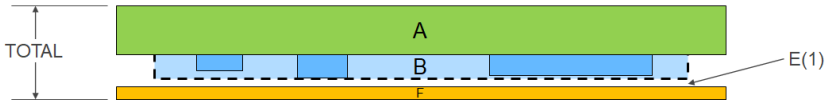


Figure 23: Chassis Hook Keepouts (Zone 2)



Figure 24: HPM Secondary Support (Zone 3)

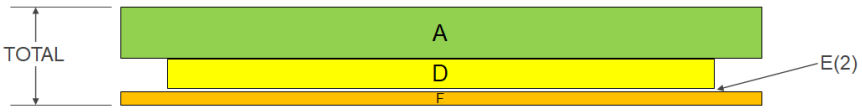
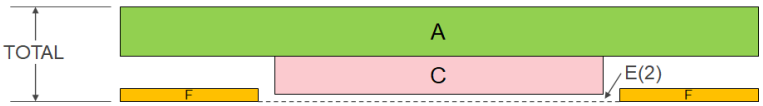


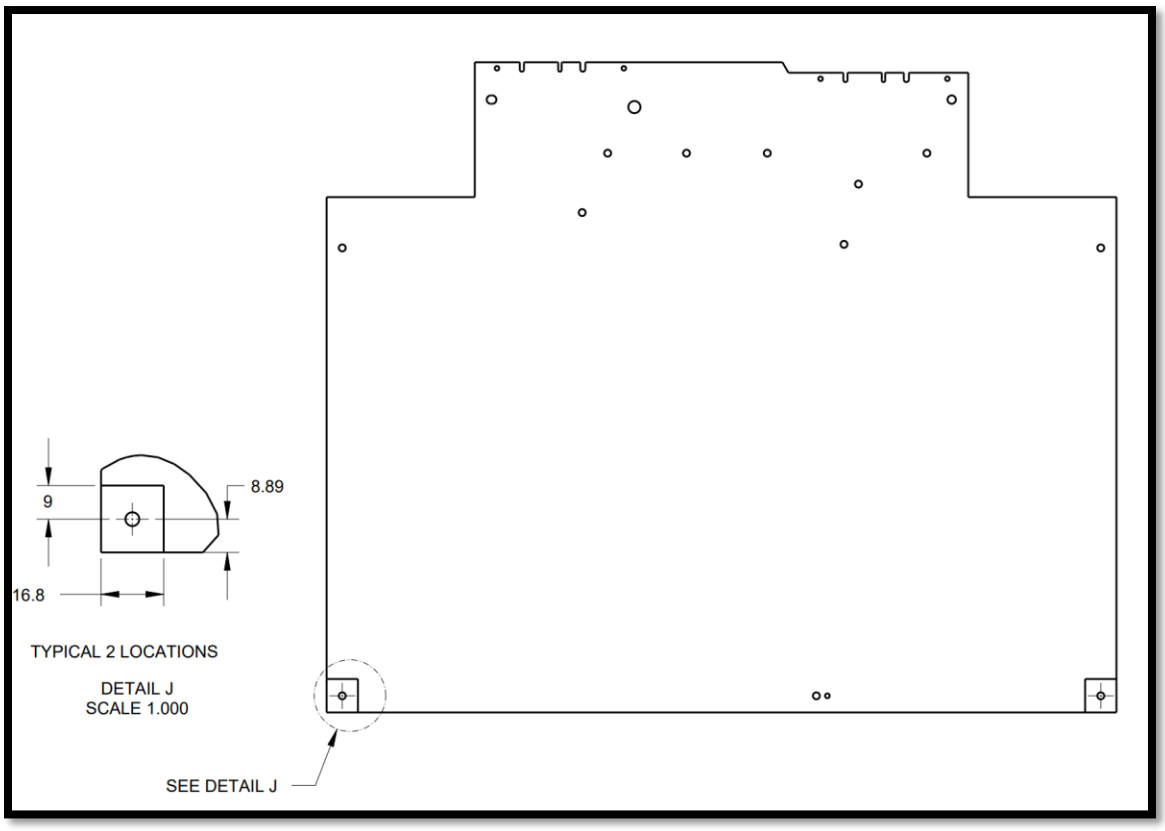
Figure 25: CPU Backing Plate (Zone 4)



10.15. Thermal Solution Bracketry Keepout Zones

There shall be keepouts around the Far Side HPM mounting holes to enable bracket mounting to the HPM, as detailed in **Figure 26**. These brackets may be needed for systems that wish to mount liquid cooling components, such as DIMM liquid manifolds, or large radiator assemblies.

Figure 26. Thermal Solution Bracket Keepouts



11. HPM Power Zones

The M-FLW HPM is powered from a 12V DC source. This Base Specification does not cover alternate PSU voltage sources (e.g., 48V DC). The HPM supports multiple power zones where significant power delivery and connectivity is expected. **Figure 27** illustrates locations of power zones on the HPM. Details of each zone are described below, some are ingress, some are egress from the HPM. Designers should use this guidance in design of HPM Power planes.

Implementors Note:

The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in private and/or public HPM design specification(s) for system configurations supported per HPM design

Figure 27. HPM Power Zone locations

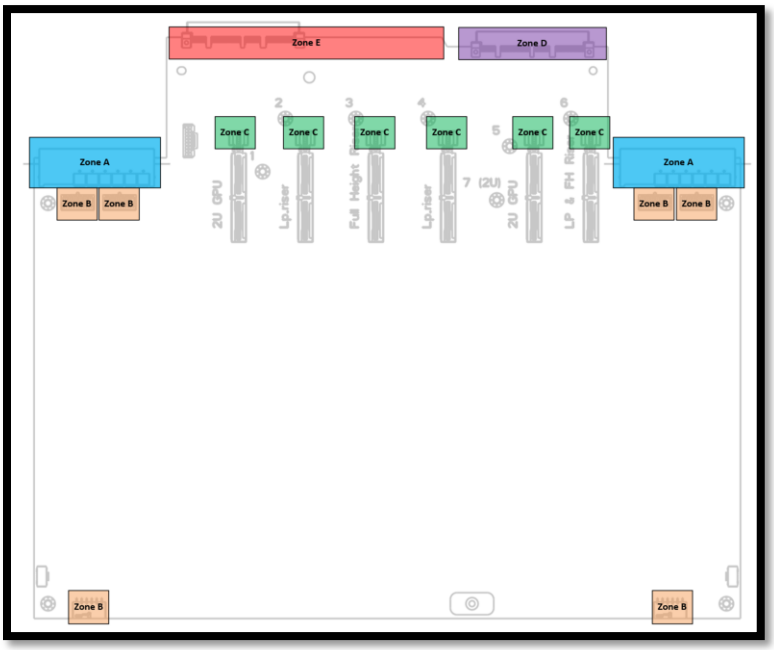


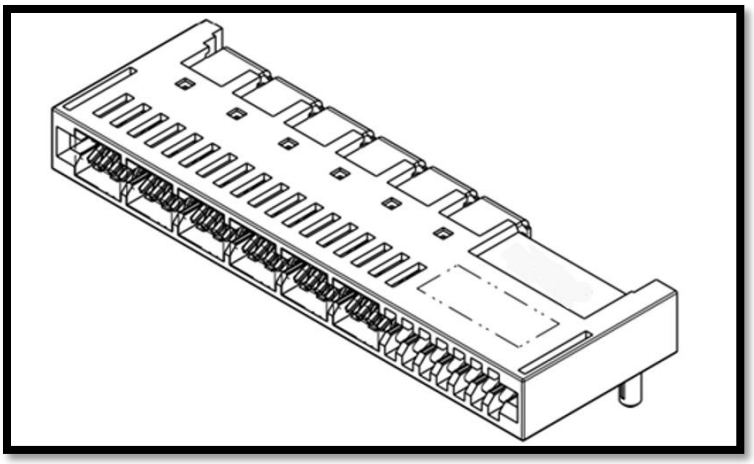
Table 5. Power Delivery Zones

Zone	Feature	Typical Usage	Zone Power Rating
Zone A	M-CRPS Connector	Ingress	up to 3200W
Zone B	2x6+12s PICPWR	Egress	up to 864W
Zone C	Near Side Riser PICPWR	Egress	up to 252W per Near IO Connector populated
Zone D	DC-SCM R2.x	Egress	up to 50W
Zone E	OCP NIC R3.0 + Platform Custom Zone	Egress	up to 160W

11.1. Zone A: M-CRPS Connector(s)

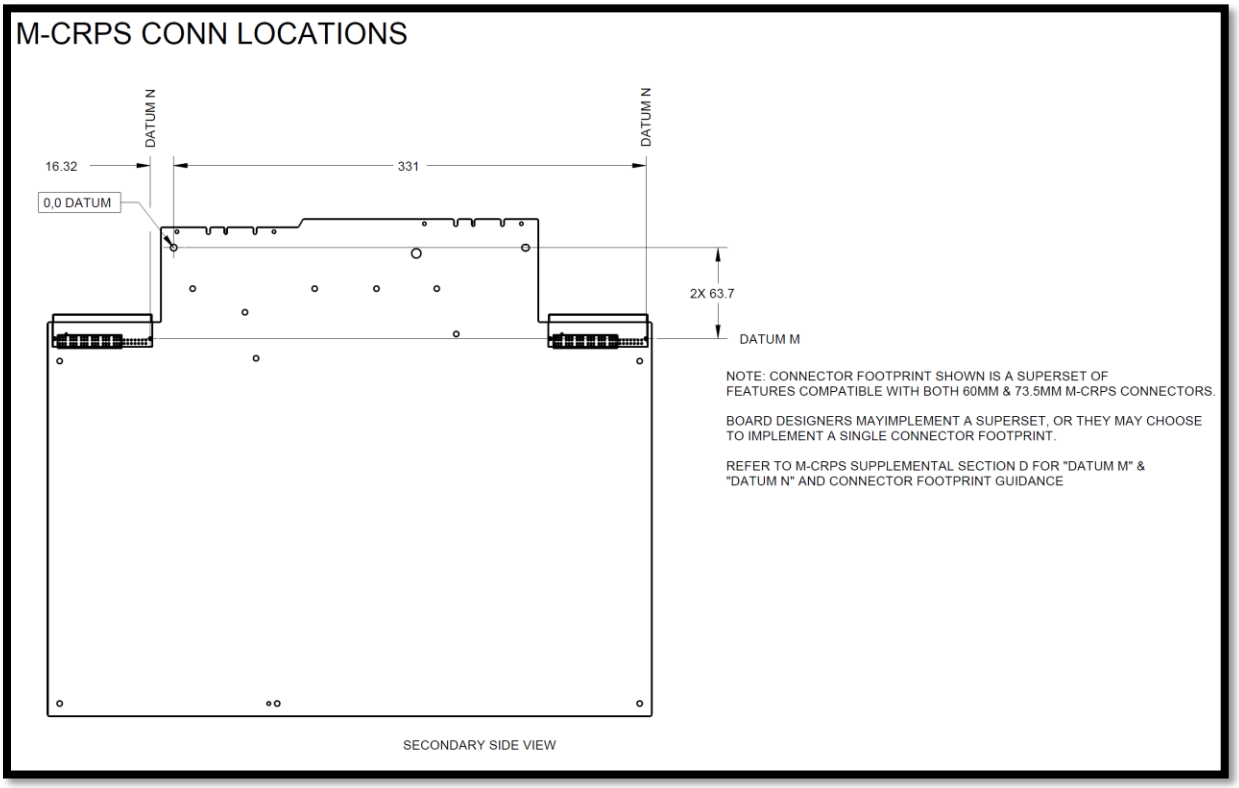
- Connector Power Rating: 3200W
- Typical usage: Power ingress

Figure 28. M-CRPS Power Connector



Locations of M-CRPS connectors shall be placed as defined in **Figure 29**

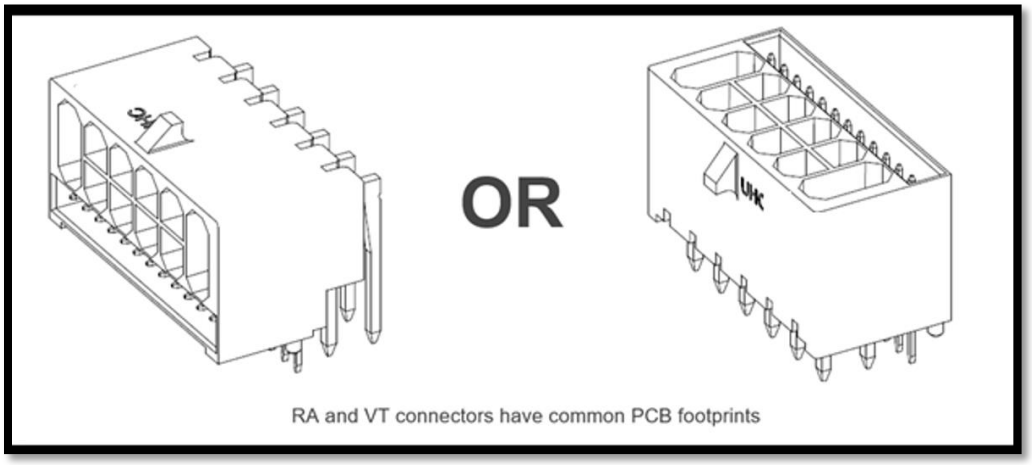
Figure 29. M-CRPS Connector Location Requirements



11.2. Zone B: PICPWR Connector(s)

- Connector Power Rating: 864W
- Typical usage: Power egress to peripherals, Power Ingress from PDB
- Refer to M-PIC Specification for additional details
- Far Side PICPWR may be either vertical or right angle, the connector has common footprints.
- Near Side PIC PWR should be vertical connector only

Figure 30. 2x6+12s PICPWR Power Connectors

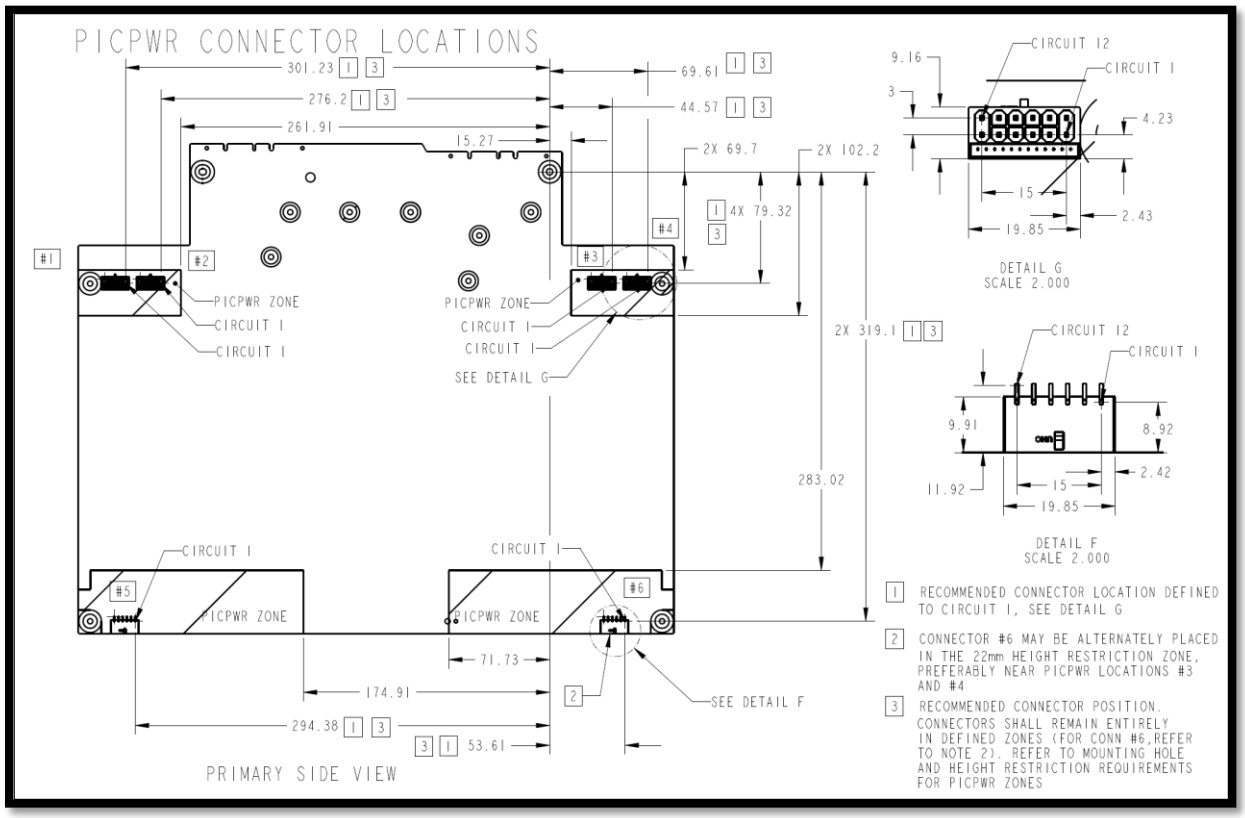


The HPM shall implement 6x PICPWR connectors matching the quantity per PICPWR zone shown in **Figure 31** The connectors are recommended to be placed at the indicated locations. The Figure notes that Connector #6 may be moved to the 22mm height restriction zone, and if so it is recommended to place that connector in or near the zone of PIC PWR connectors #3 and #4.

Note: HPM shall implement these connector footprints (but can be depopulated in assembly BOM with Design Spec guidance.) .

Note the location number is arbitrary and is not intended to be the same as M-PIC labeling/numbering requirements.

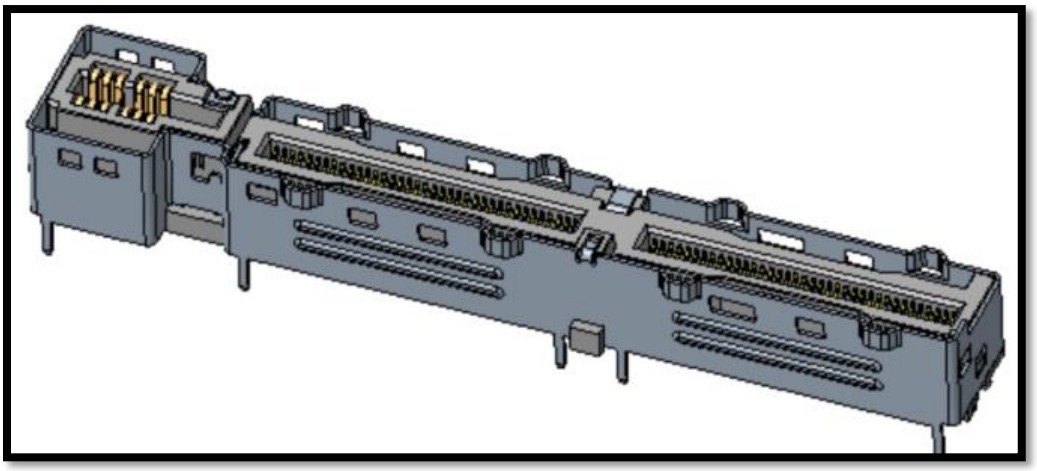
Figure 31 PICPWR connector (2x6+12s) Location Requirement (6 locations)



11.3. Zone C: SFF-TA-1033 Connectors w/ PICPWR

- Connector Power Rating: 252W
- Typical usage: Power egress for up to 3x 75W CEM PCIe devices
- Refer to M-PIC Specification for additional details.
- Refer to **Section 10.11** for additional details on Near Side connector and location.

Figure 32. SFF-TA-1033 Connector



The Egress Near Side Riser Power Zone provides power to PCIe devices on risers. This specification does not cover direct dock CEM implementation (non-riser approach). The HPM provides 12V_PRIMARY[1] to the Egress Near Riser Power Zone.

75W Slot power, detailed in **Table 6**, is provided for each PCIe CEM slot on all PCIe risers. The PCIe riser enables a +3.3Vaux and +3.3V (Vcc3_3) power sources derived from the 12V_PRIMARY source from the HPM

Table 6. Minimum HPM Power Supply Rail Requirements per PCIe CEM Slot

Power Rail	75 W Slot[2]
+3.3Vaux	Generated on PCIe riser. Derived from 12V_PRIMARY
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from 12V_PRIMARY
12V_PRIMARY Voltage Current	12V nominal 7.25A total: 5.5 A (CEM 5.0) + ~1.0A (VR conversion to V_{cc3_3}) + ~0.35A (VR conversion to +3.3Vaux) + ~0.40A (misc.)

Note 1: see M-PIC specification for definition of 12V_PRIMARY

Note 2: Additional power is provided to each CEM slot beyond PCIe CEM 5.0 specification to budget for miscellaneous logic on risers and VR conversion losses. Effective total 12V nominal power is 87W per slot (7.25Ax12V).

11.4. Zone D: DC-SCM R2.x Connector

- Connector Type: See OCP DC-SCM R2.x specification.
- Connector Power Rating: 50W (Refer to the OCP DC-SCM R2.x specification)

11.5. Zone E: NIC 3.0 and Platform Customization Zone Connector(s)

- Power Connector Type: See OCP NIC R3.0 specification and Platform Custom Zone
- Connector(s) Power Rating: 160W (combination OCP NIC R3 and Platform Custom Zone)
- This is a maximum number, the connectors OCP NIC R3 and Platform Custom Zone choice may not consume maximum power.

12. I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details, specifically M-PIC, M-XIO, M-CRPS, and M-PESTI specifications.

For information on connector placements, refer to **Section 10 Mechanical Requirements**.

13. References

Relevant Open Compute Specifications

This specification also relies on the following Open Compute Project specifications

1. OCP Server Network Interface Card (NIC) R3 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
    a. Mezz (NIC) » Open Compute Project

2. OCP Datacenter Secure Control Module (DC-SCM) R2.x – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
    a. Hardware Management/Hardware Management Module - OpenCompute

3. OCP Open Rack V3 - Class B and D were developed with Open Rack v3 use cases in mind, please refer to the Open Compute Project specifications for more information
    a. https://www.opencompute.org/wiki/Open_Rack/SpecsAndDesigns

Additional Industry References

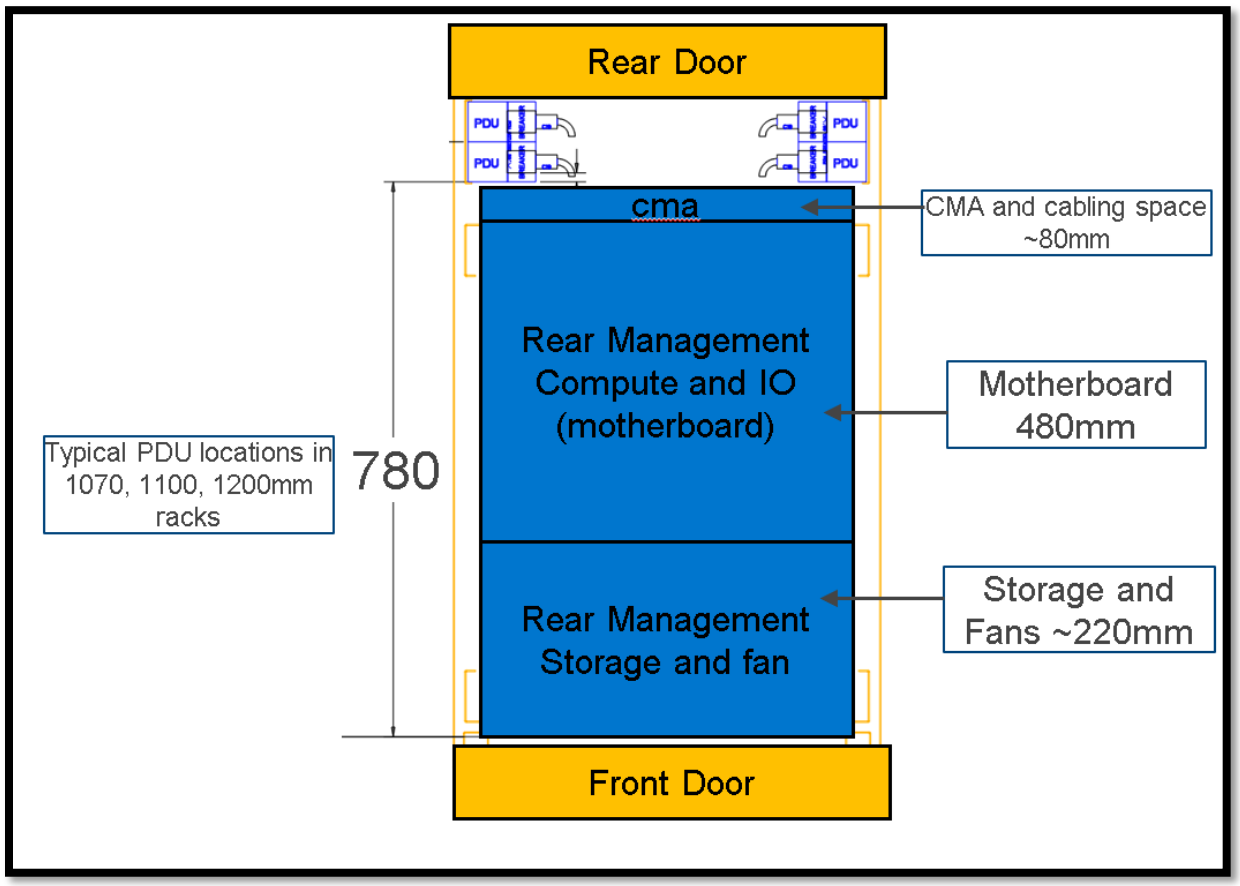
- ASMEY14.5 – 2018 Dimensioning and Tolerancing
- Open Rack V3
- SNIA SFF-TA-1002
- SNIA SFF-TA-1016
- SNIA SFF-TA-1026
- SNIA SFF-TA-1033
- Open19

14. Supplemental Information

14.1. Rack and Chassis Depth Stackup Assumptions

The M-FLW HPM Base Specification is constructed under the considerations that the installation environment has a Power Distribution Unit approximately 780mm from the front EIA flange. Although platforms may vary in depth, the board size constraint is chosen to enable typical chassis storage systems using this M-FLW HPM spec to fit with a Cable Management arm in less than the 780mm PDU constraint.

Figure 33. Rack Depth Constraints



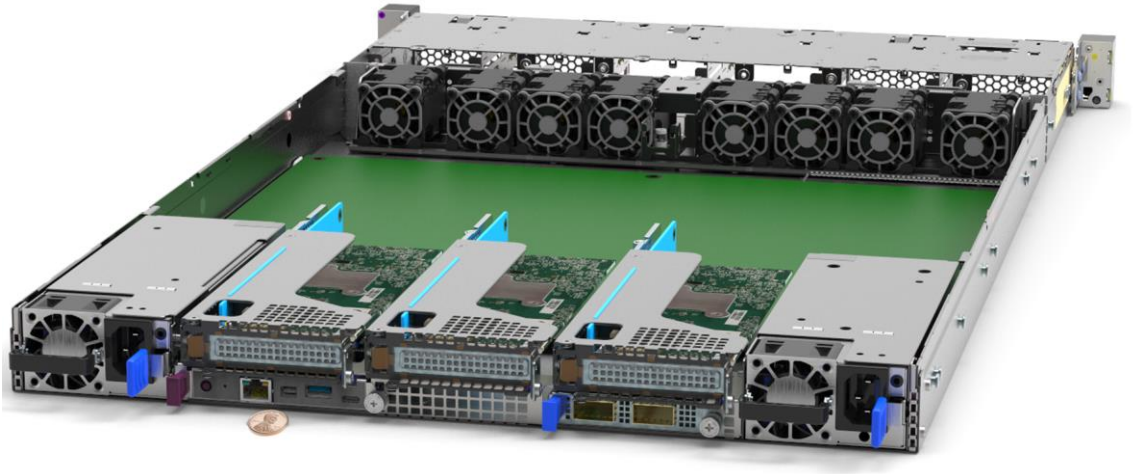
14.2. Example 1U and 2U PCIe Slot Typical Configurations

The following images in **Figure 34** are some example representations of typical Enterprise 1U and 2U PCIe Slot Configurations.

Figure 34. Examples of Typical 1U / 2U PCIe Slot Configs for Rear Management System

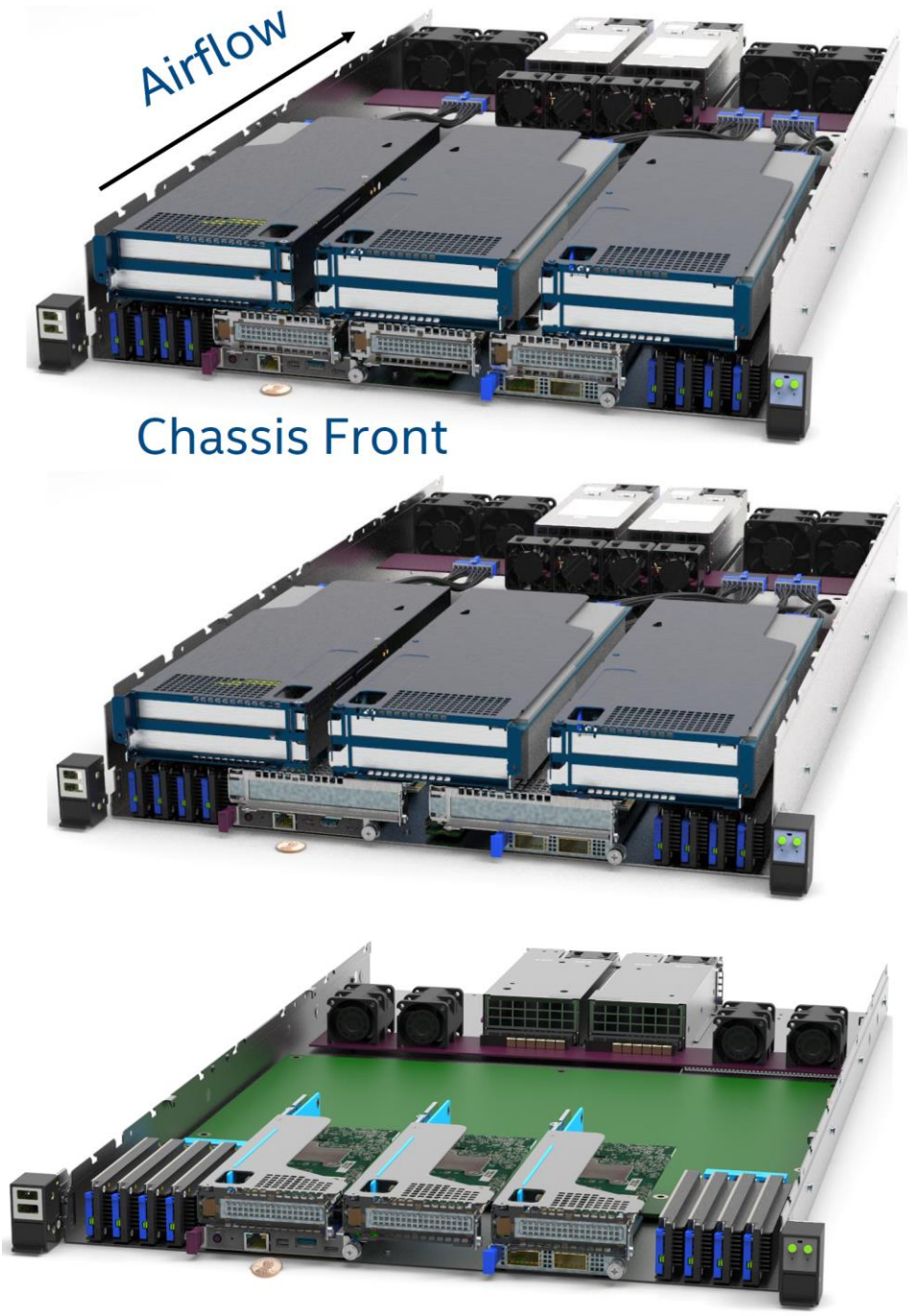


920



The following images in **Figure 35** are of typical Hyperscale 1U and 2U PCIe Slot Configurations. Note, these are 19” Front IO chassis like OCP Project Olympus. Also, the front can be shuffled around using an extra “adapter board” like **Figure 40. Base Outline HPM used in an Example 21"** Reference Chassis is not covered by the M-FLW HPM spec.

Figure 35. Examples of Typical 1U / 2U PCIe Slot Configs for Front Management System

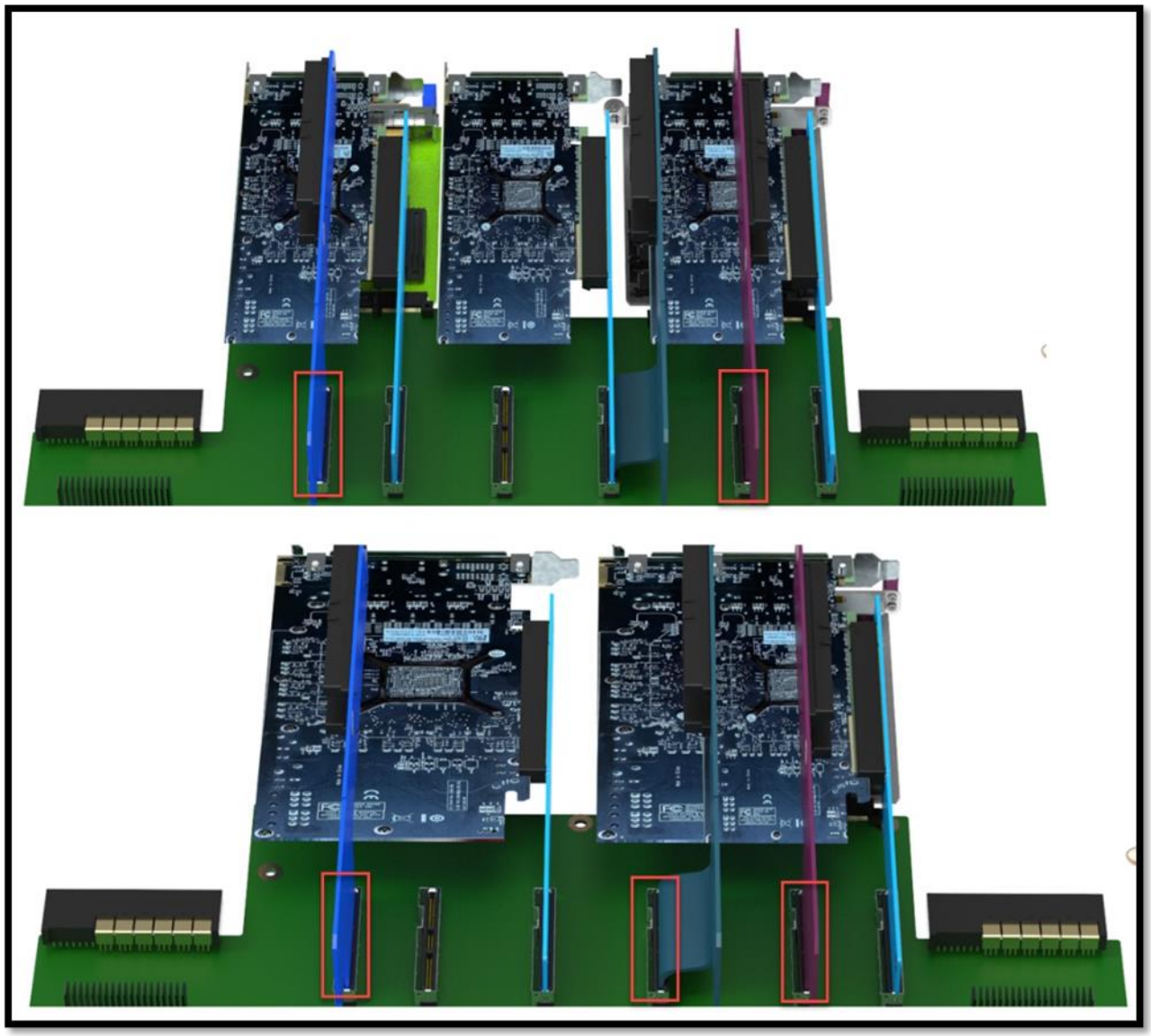


930

In the above example configurations, a system design may utilize risers assigned to Near IO positions, such as those shown in the example in **Figure 36**.

Note, that this also illustrates that the Y-position of Near IO cards is set so that cards in the lower 1U risers do not cover other Near IO positions; thus this enables blind mate access of 2U
935 riser assemblies.

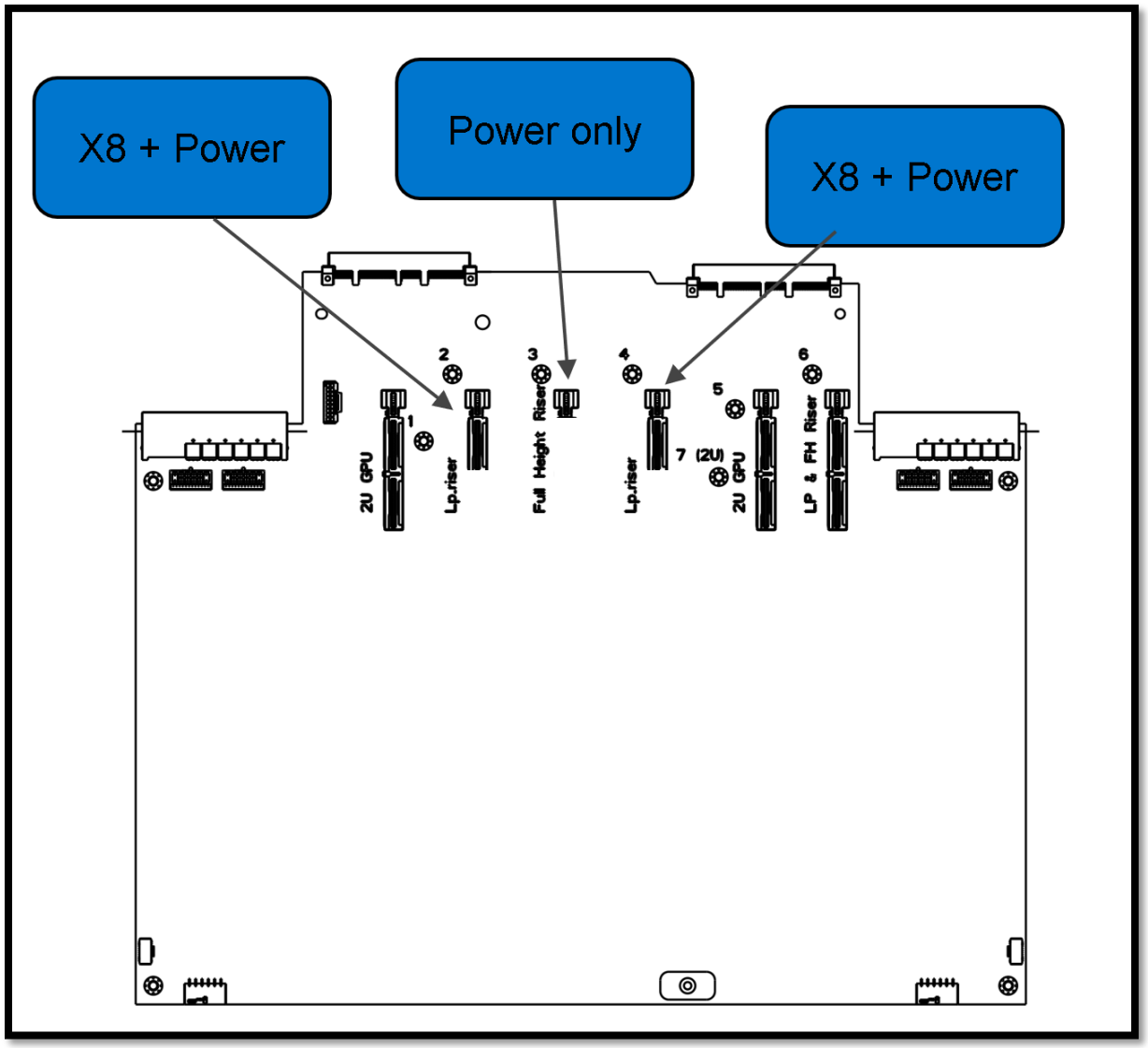
Figure 36. Riser assignment to Near IO positions for Assumed Configurations



14.3. Example Scenario for Near IO Population with < 6x16 ports

940 Certain Compute Cores may not have 6x16 ports to assign to all six Near IO positions. The HPM Designer may elect to follow the rules shown in **Section 10.11.2.** An example of this is shown below in **Figure 37**. HSIO might be cabled into the riser, but the riser still has the PICPWR portion of the connector for PCB applications. Refer to **Figure 37** which defines Datum M and Datum K position of all 3 connector variants.

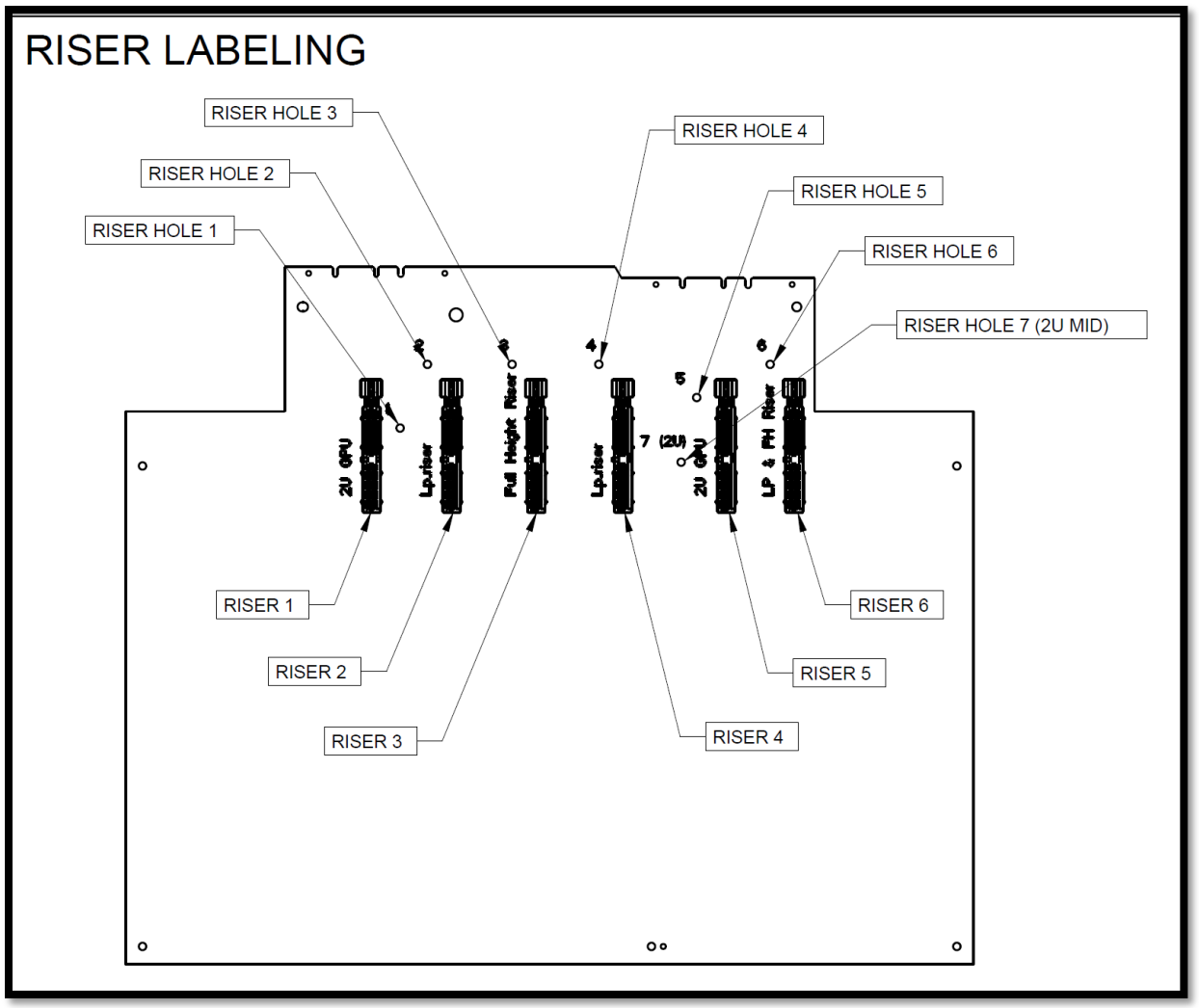
945 **Figure 37. Example Near IO Connector Population Scenario**



14.4. Additional Information on Near IO Riser Retention Holes

In a system configuration that uses riser cards in the Near IO, mechanical retention is enabled by holes in the HPM near each Near IO location. The following **Figure 38** demonstrates the riser retention holes and which Near IO position each hole is associated with.

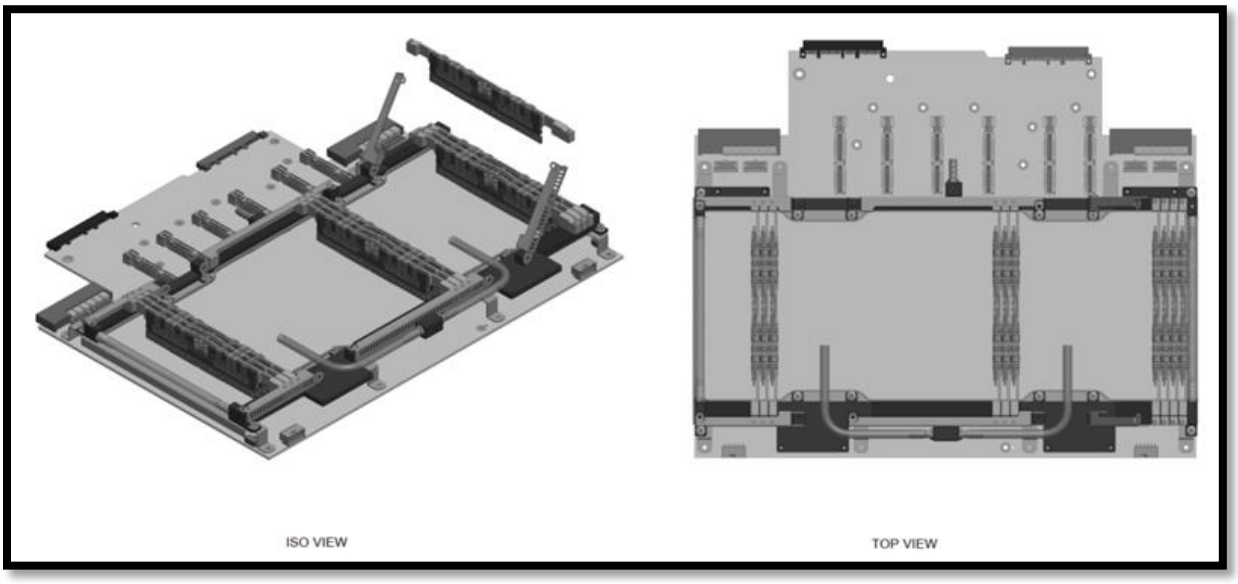
Figure 38. Riser Retention Holes and Associated Near XIO Locations



14.5. Example Liquid Cooling Implementation in 1U M-FLW

Figure 39 demonstrates an example implementation of a M-FLW Liquid Cooling solution w/ 10 DIMMs shown. Considerations should be made for CPU and DIMM locations not detailed in the M-FLW Base Specification. Example Liquid Cooling structure attaches to Far side mounting holes shown in **Figure 26. Thermal Solution Bracket Keepouts** and **Figure 19. HPM Secondary Side Height Keepout Zones, Pads, KOZ**. It also complies with **Figure 17. Zones for Primary Side Component Height Restrictions.**

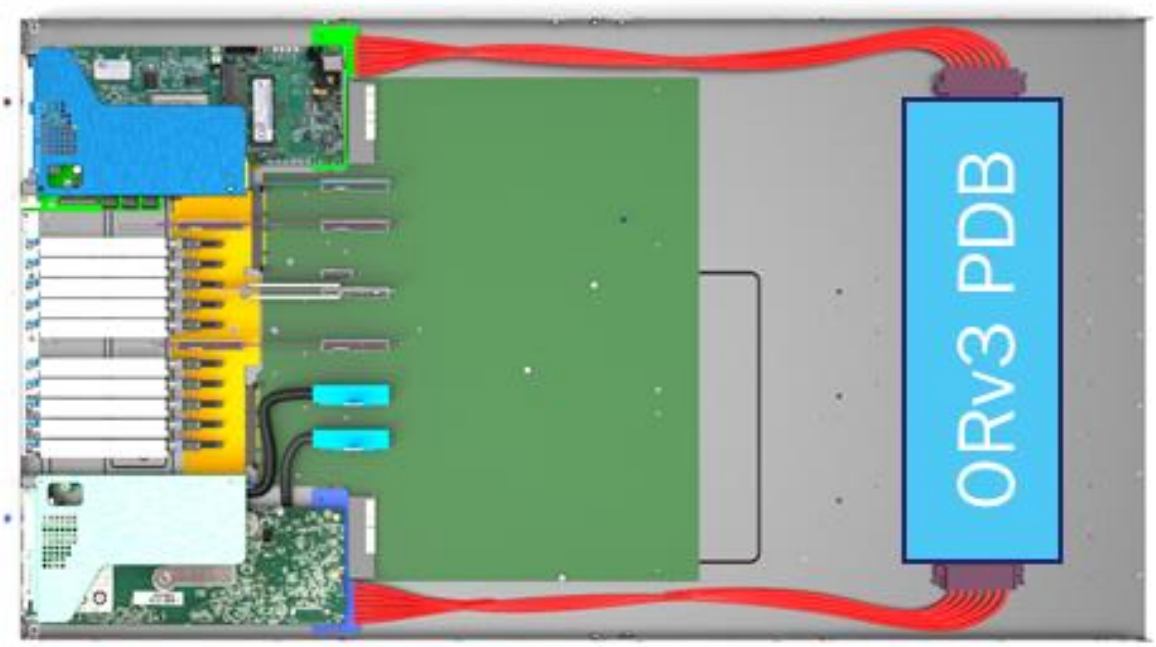
Figure 39. M-FLW 1U Liquid Cooling Example Implementation



14.6. Example/Reference System Architecture in 21” Chassis

Figure 40 shows how the Base Outline HPM can be utilized in a 21” chassis architecture, including if Power Supply Infrastructure is on the Far Side with cables to the near side power ingress.

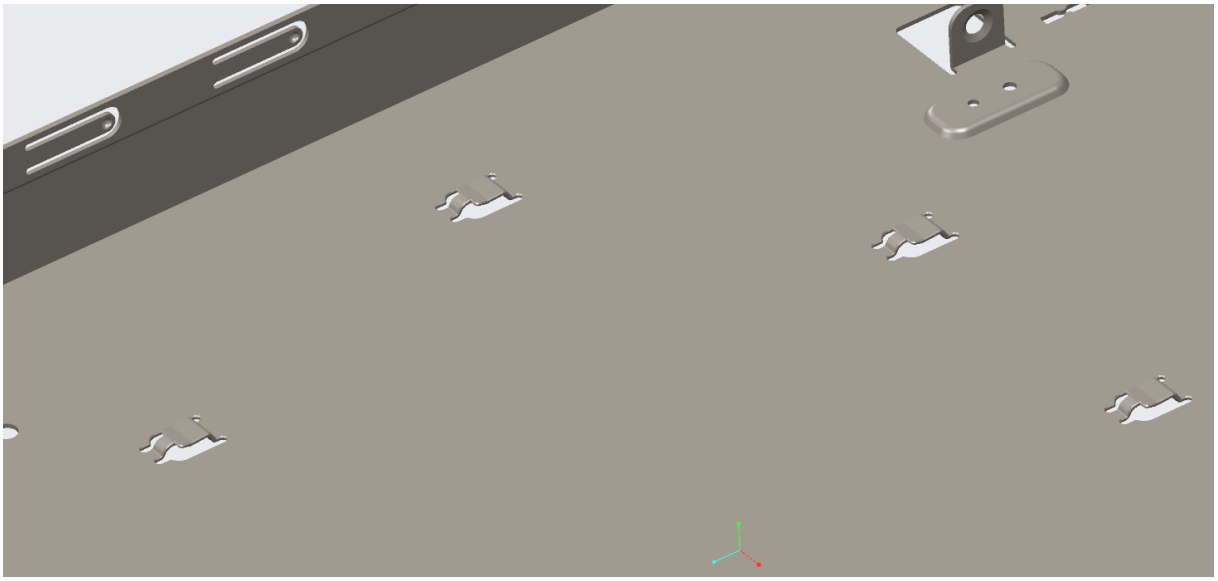
Figure 40. Base Outline HPM used in an Example 21" Reference Chassis



14.7. Example Chassis Base Geometry for Chassis-to-Board Bracket Interface

Figure 41 demonstrates example geometry required in the chassis base to interface to the Chassis-to-HPM bracketry in **Figure 20. Example of Chassis-to-HPM Bracket (Board Pan).** The exact geometry is not specified, but considerations must be made for maximum board thickness (see **Section 10.14 HPM Board Thickness**) and HPM Keepout Zone sizes (See **Section 10.13**).

Figure 41. Example Chassis Base Geometry to Interface Chassis-to-Board Bracketry



14.8. HPM with Far Side Panel Mount IO (FSPM) Requirements

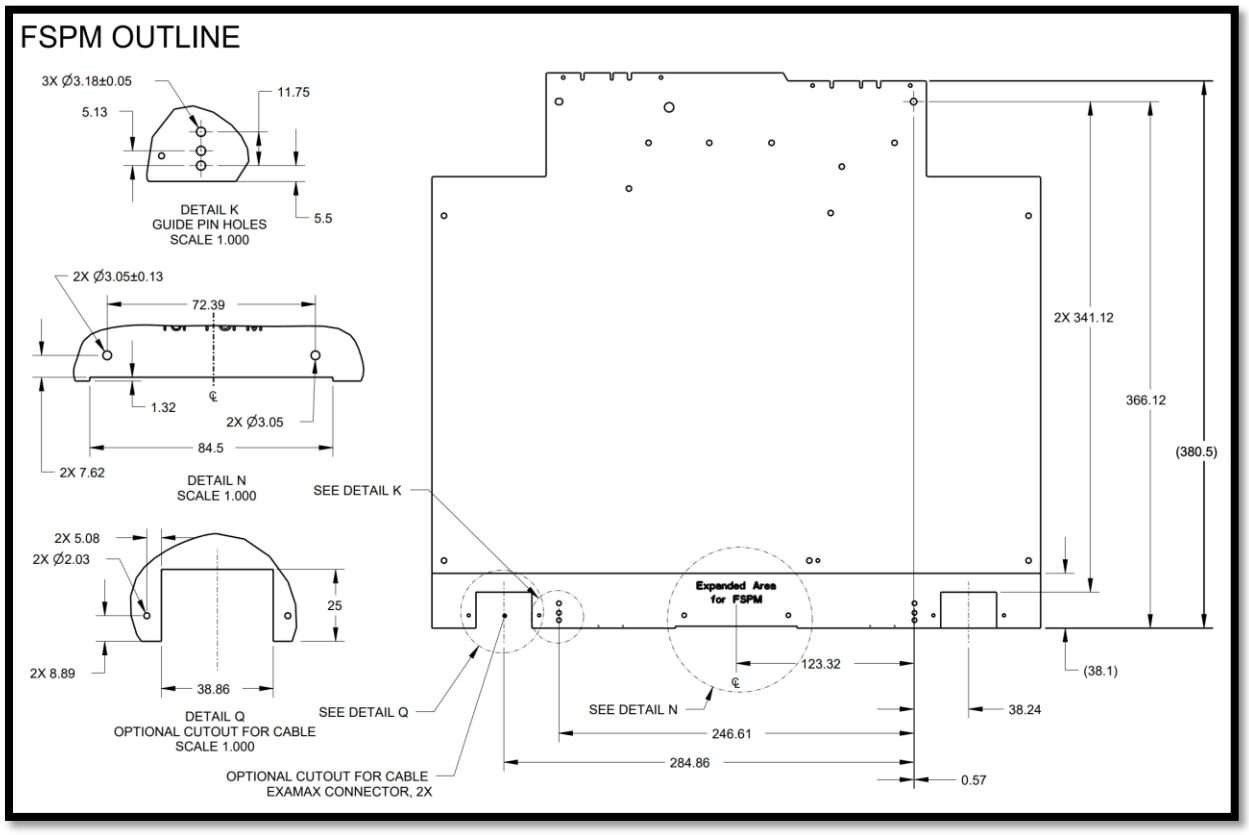
Readers Note: This Section represents a Future M-FLW Type. For this Version of M-FLW, we will abbreviate this HPM type as the FSPM (Far Side Panel Mount) HPM.

The FSPM architecture leverages the Base M-FLW Specification. FSPM Adaptation or Type has differences from the Type 1 Base M-FLW Spec, which are focused on the Far Side area to optimize Power Delivery and IO connections that are part of a Front Panel IO or Blade implementation. A FSPM implementation must implement blind-mate panel mountable connectors in the specified locations as described in **Figure 46. FSPM HPM Required Connector Locations**

14.8.1. FSPM HPM Outline

FSPM HPM outline is an extension of the M-FLW Base Spec outline listed in **Figure 3. Full Width Type 1 Outline** and must match the specified dimensions with exception of Far Side growth. The Far Side dimension of the base outline is extended by 38.11mm [1.5”] to accommodate blind mate IO connectors, power connector, and blind-mate guide pins to achieve reliable docking with panel-mount connections.

Figure 42. Full Width HPM Outline Modifications for Far Side Panel Mount



14.8.2. Blade High Speed IO connector

High Speed IO connector outlines shown in **Figure 42. Full Width HPM Outline Modifications for Far Side Panel Mount** are based on the Amphenol ExaMAX family (or equivalent) series.

There are seven 4x8 ExaMAX shown from left to right. In addition, there is one 6x8 ExaMAX in the far-right position that is intended to include extra clock and management signals.

The position of these connectors must align to the indicated positions, but any of the connectors may be depopulated if not used. However, both guide pin receptacles **must** always be included for mechanical robustness during blind-mate insertion. The pin-out for the connectors must adhere to the definitions defined in the M-XIO specification.

Table 7. Blade Far/South High-Speed IO Recommended Connectors

Connector family	Company	Configuration
ExaMAX / ExaMAX 2	Amphenol or Equivalent	4 pairs X 8 columns
ExaMAX / ExaMAX 2	Amphenol or Equivalent	6 pairs X 8 columns

Figure 43. ExaMAX 4x8 connector used in FSPM

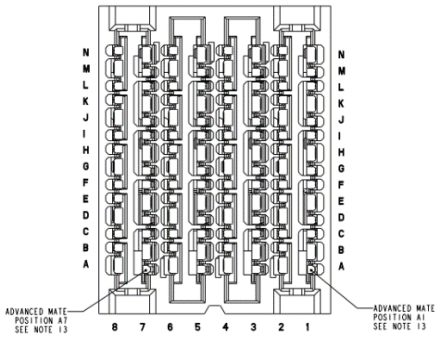
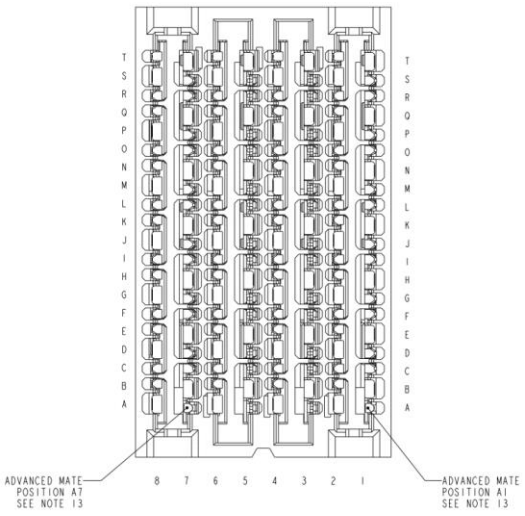


Figure 44. ExaMAX 6x8 connector used in FSPM



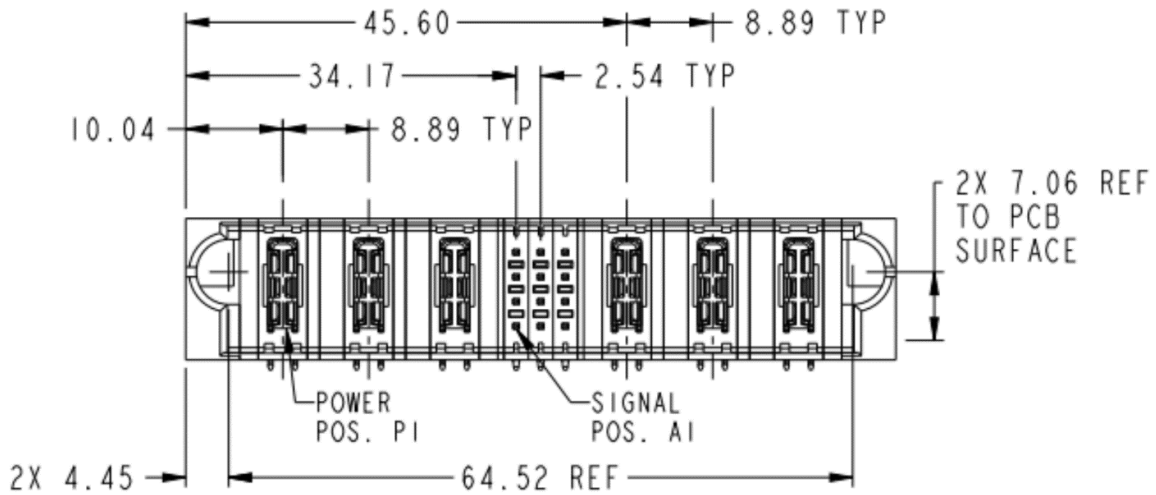
14.8.3. Ingress Power Connector

The Far Side power connector is shown **in Figure 45. PowerBlade+ Ingress Power Connector.** The connector must be based on Amphenol PowerBlade+ (or equivalent). The configuration is 3 high-power contacts on each side with 16 signal contacts in the middle. The pin-out and signal definitions must align with the definitions in the M-PIC and PICPWR specifications.

Table 8. Blade Far/South Ingress Power Recommended Connector

Connector Family	Company	Configuration
PowerBlade+	Amphenol 10106263-6003003LF or equivalent	3 High Power + 16 Signals + 3 High Power

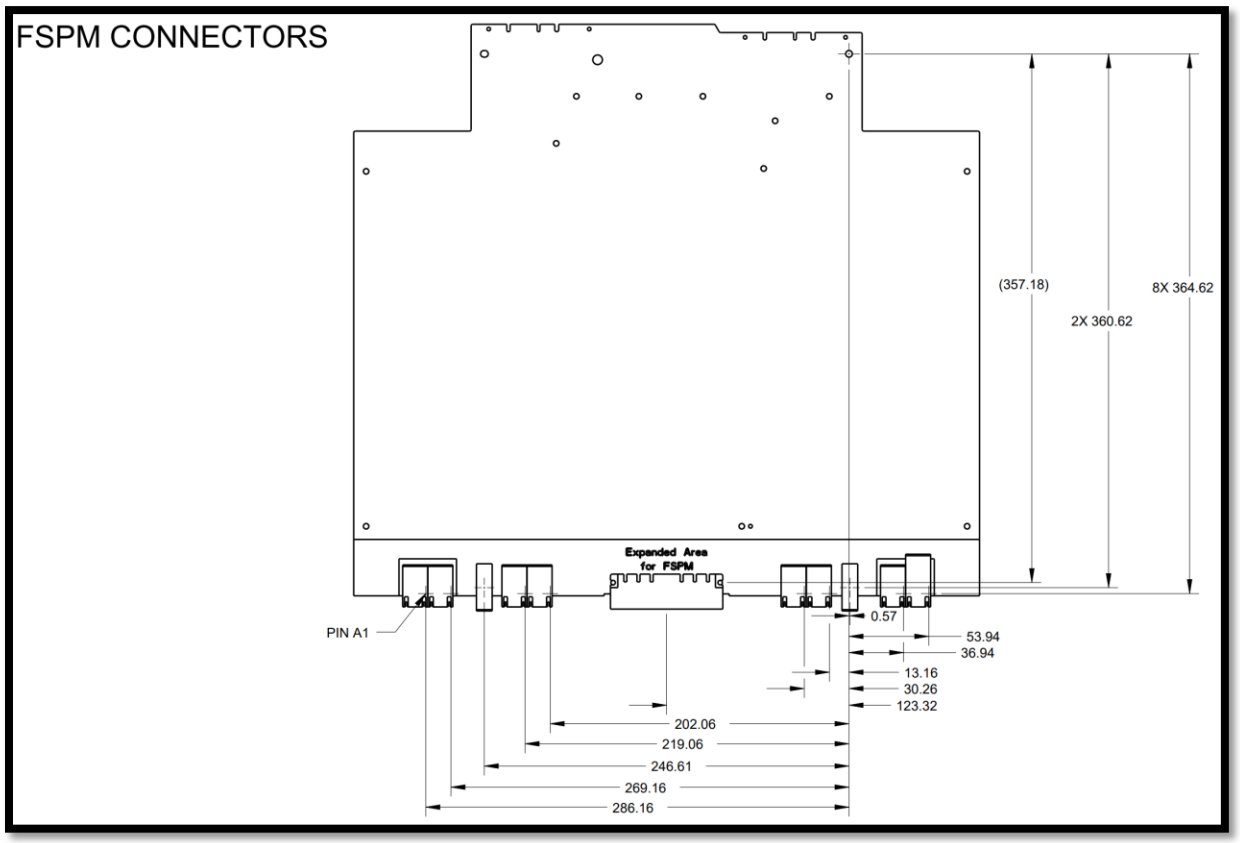
Figure 45. PowerBlade+ Ingress Power Connector



14.8.4. FSPM HPM Locations for Power and High-Speed IO

The connector locations for the FSPM HPM are specified in **Figure 46** . The FSPM HPM must comply with these connector locations.

Figure 46. FSPM HPM Required Connector Locations



14.8.5. Blade Mechanical Guide Pin

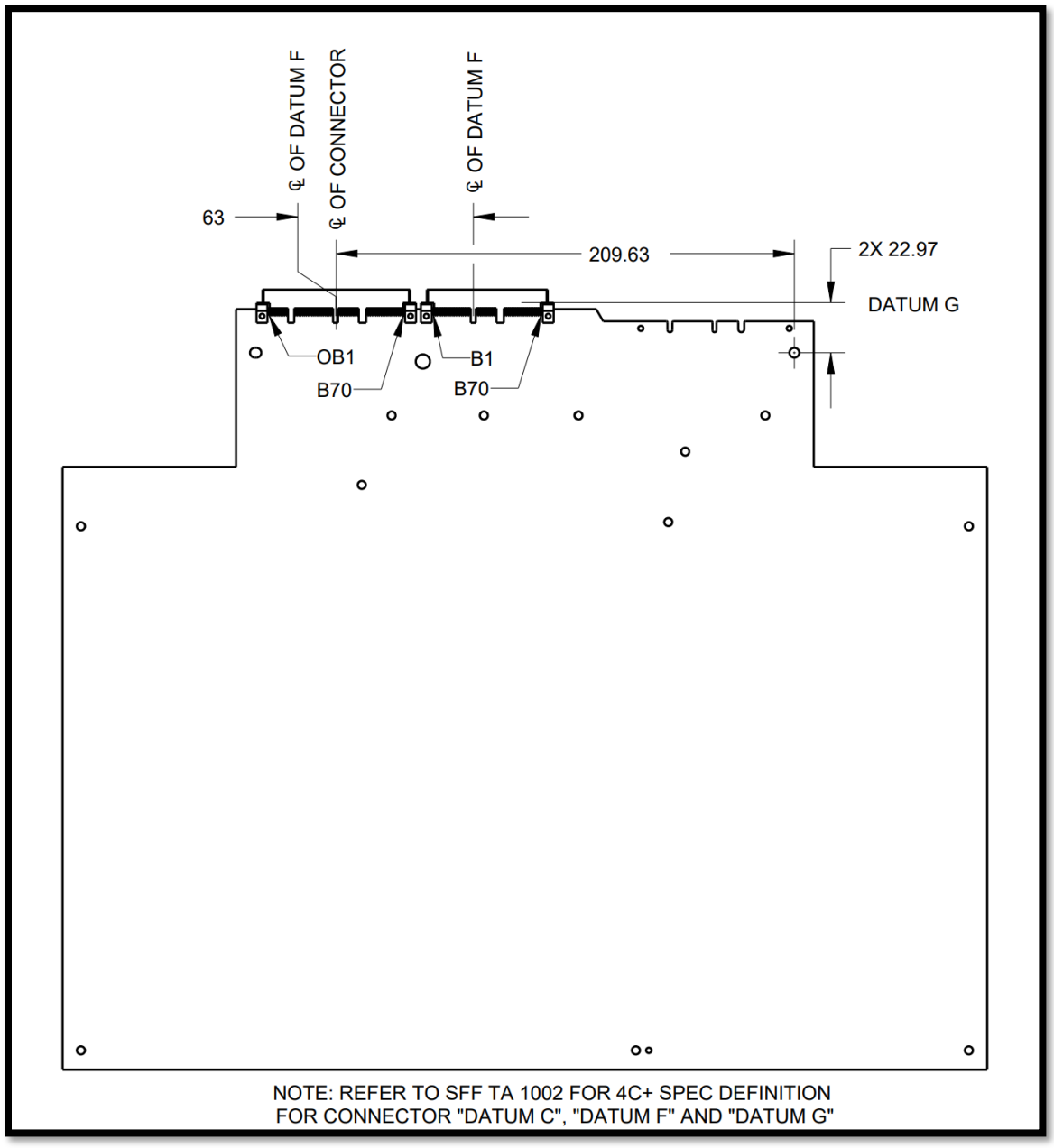
The outline shown in **Figure 46** also includes a position identified for a mechanical guide pin for blind mate alignment. The HPM must implement these features for safe blind mate implementation. The part number to use for the guide pin should be Amphenol 10037912-101LF (or equivalent).

14.9. Archived Platform Custom Zone OCP NIC R3 LFF

Note, this content is archived to Supplemental Information section as the M-FLW spec no longer promotes OCP NIC R3 LFF implementation, since this form factor was deprecated from the OCP NIC R3 spec. We are recording this info for reference.

An HPM design may want to support an OCP NIC R3 LFF, instead of a single SFF. These HPM designs should follow the following placement guidance in for the LFF connectors.

Figure 47. OCP NIC R3 LFF Implementation for Platform Custom Zone



14.10. CAD files

CAD files for M-FLW are at the following link:

https://drive.google.com/drive/folders/1tSvFScjQ2P3_OUIPfpOrrpsSBydVpDE2?usp=sharing

Note: For import into Solidworks, choose “free curves” as an import option to see KOZs below.

Figure 48. STP CAD model picture

