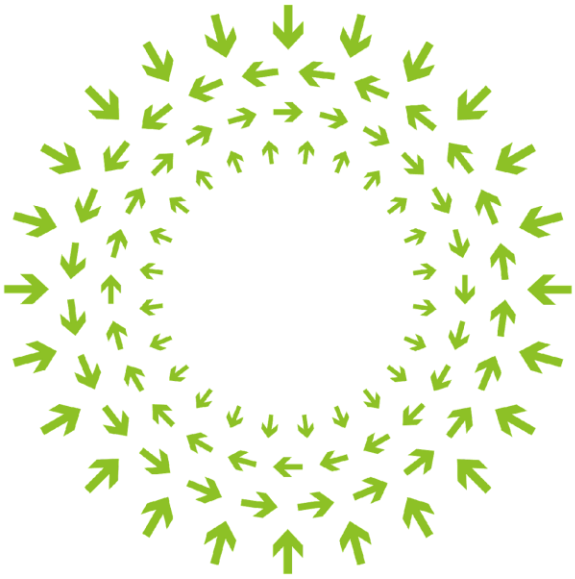


OPEN

Compute Project

Full Width HPM Form Factor (M-FLW) Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 1.0 Release Candidate 5

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1.2. Acknowledgements

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback from various individuals and companies that participated in DC-MHS.

2. Version Table

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Date	Ver #	Description
4/22/2022	0.70	Initial Public Release
6/07/2022	0.75	• Added Spec Compliance Table Section 4 • Added 9.75mm to board under PSU Connectors • Moved OCP NIC Connector 6mm to left. (from 204.29mm to 210.29mm) • Moved IO Riser Connector #3 to left 5mm. Moved KOZ and Mount hole accordingly (From 136.02mm to 141.02mm) • Rotated PIC Power Connectors 180° • Defined Pins S1 & S12 on Pic Power Connectors and Rear Power Connectors and revised dimensioning scheme to Pin S1 • Figure 18, Defined IO Connectors Pin A1 & A77. • Defined Pins OB1 & B70 on NIC & DCSCM Connectors • Defined Pins OB1 & B70 and Pins B1 & B70 on Alternate NIC Connectors • Defined Control Panel Connector Pins A1 & A10 • New location for USB connector Zone • Moved Retention Hardware Height Restriction Zone note to Detail L • Combined 1U & 2U PCIE Mount Holes to one sheet • Revised references to “KIZ” to “Height Restriction Zone” • Revised Bottom Side KOZ shape for Tempan to rectangle. Revised Y-dimensioning scheme to center of rectangle • Added KOZ to Bottom side Mount Holes. Preliminary size at 13.8mm x 13.8mm. • Changed Figure 3 to support OCP NIC move of 6mm • Changed Figure 4 to show pads and KOZs around mounting holes • Updated Figure 6 for clarity • Changed Figure 10 to move OCP NIC by 6mm. • Changed Figure 11, Control panel connector orientation, and primary/secondary designations. • Changed Figure 12, USB Zone moved. • Combined Figure 17 and 18 into a new Figure 17. Moved 1U PCIe Riser Mount holes down 7.5mm and left 4mm. Added Mount Hole detail with Ø8.0mm Pad size, Ø16mm Component KOZ. • Changed Figure 21 to update Secondary size KOZs for mounting holes and chassis hooks • Updated Figure 29 for UBB outline updates • Added Figure 32 for UBB connector locations • Changed description of Adapted HPM in Section 13 • Figure 26 changed, rotating PIC Power connectors 180 degrees • Relocated power plane fusing requirements to M-PIC spec in Section 11.2 • Clarified minimum power plane recommendation in Section 11.2

6/27/2022	0.80	• Modified Table 4 in Section 11.1 to describe zone power and range of supported power • Clarified minimum power plane recommendation in Section 11.2 • Renamed Figure 22 • Figure 19, Sec 10.13, Changed primary side height restriction zones • Sect 10.12, Figure 18 change KOZ around Riser retention holes • Sect 10.8, Figure 12, moved Intrusion connector to same zone as USB • Figure 21, updated MH KOZs on bottom / secondary side. • Updated UBB Adapted outline in Figure 29 to update cutout options for cabled HSIO at far edge. • Figure 33 updated, based on connector feature updates from vendors • Figure 35, updated text in drawing • Figure 25, updated title in drawing • Added Guide pin part number to Sect 13.1.6 • Added bullet 6 to section 10.10.1 • Figure 18, 19, updated KOZ around riser retention holes • Figure 22, updated Thermal solution Bracketry KOZ • Section 10.8, new section for PDB to HPM header • Moved section 12 into existing sections and deleted it • Moved section 13.1 into Section 12 “Adapted HPMs” for spec clarity.
8/22/2022	0.9	• Updated MH drawing • Added New handle hole geometry required dimensions, • Updated OCP NIC and DC SCM positions, Figure 8 • Moved PDB Management conn zone, Figure 13 • Moved boot connection zone, and modified to accommodate new HPM retention hole location and its associated KOZ, Figure 15 • Near IO connector and associated retention holes moved in • Figure 16 and Figure 17 • Updated Sect 10.3, HPM Board and Assembly thickness section, to include details and tolerance allowance for the Secondary Side Exception Heights. • Updated locations of Near side PIC Power (decreased pitch); maintained 10mm gap between pins of Near side Power connectors. Far Side PIC Power connectors moved outward to increase usable Far Edge space for CPU IO and VRs., Figure 32 • Updated Primary side height restrictions, Figure 18, Changed 20mm zone to 22mm and added note that numbers indicate max tol condition. Fixed an unattached dimension. • Added Platform Custom Zone options of 2x OCP NIC SFF, or single LFF with recommended placements, or direct dock E1.S boot, Section 10.6 • Updated Figure 3 with updated Near side outline • Updated Section Near Side IO Connectors 10.11, rewrite of requirements.

		• Updated CRPS Connector location (near OCP NIC), Figure 30 • Update location of HPM retention hole, Figure 5 • Updated image for latest outline, • Updated Secondary side KOZ's for chassis hooks (board pan interfaces), to allow for more flexibility in DIMM socket placement. Reduced HPM-chassis retention KOZ from 29 to 21mm long. For an example of chassis hook concept, • DC SCM Y position adjusted by 0.18mm, to correct mistake. This correction aligns DC SCM with OCP NIC at rear wall. • Changed Power Zone E rating to 160W • Changed Power Rating Zone C to 250W per Near IO Connector instance • Added Section 10.6 to define Platform Custom zone and a couple standard options that could be utilized. These drawings were in the Supplemental Info section, previously. • Added E1.S enablement option, • Figure 11 • Fixed KOZ around chassis retention hole to 21x21mm, For an example of chassis hook concept, • Added implementors note about HPM handle hole and Mounting holes For an example of chassis hook concept, • Deleted chapter 12.2, which had old, adapted options that were pulled into the new Platform Custom Zone. • Added introduction paragraph including units and tolerances to Section 10, matching M-DNO content. • Changed 11.1 Zone B connector to Vertical only (removed R/A option) • Intrusion Switch and USB Conn zone updated, to ensure it does not overlap in the 11.3mm height restriction zone, Figure 14. • Created new chapter for Far Side Panel Mount HPM in Supplemental Section 14.8. Moved and renamed this content out of the Adapted HPM section. • Changed Zone B Section 11.2 to include ingress power option per M-PIC specification
9/26/2022	1.0	• Added Connector List to DC MHS documents, Section 6 • Section 10.1, Updated Outline wording to indicate base outline is Type 1, and future Types will be defined. • Clarifications made in Section 10.2 • Moved HPM Board Thickness Section to 10.15, and moved secondary side height restriction details into Section 10.14 • Changed Board Handle Hole geometry, Section 10.4 • Made primary OCP NIC location a reference dimension in example of 2 OCP NIC use case. • Updated naming labels in Boot Storage Connector Figure 15

		• Clarified hole descriptions as “Riser Retention Holes” in Section 10.11 • Clarified wording on Primary Side Component Height Restrictions, Section 10.13. • Updated format of Secondary Side Zones and Height Restrictions, Section 10.14 • Added new requirements for secondary side height zone restrictions, as part of restructuring of Section 10.14 • Removed HPM Power Plane Section, Changed Section 11 from Power Delivery to Power Zones. • Added Section 12, with simple reference to other DC-MHS specs. • Updated Figure 32, and provided optional placement for connector #6. • Removed Power Plane requirements from FSPM section in Supplemental Information, for consistency with base spec. • Tolerance removed from Near IO connector placement, Figure 16 • Added CAD import tip in Section 14.9 • Added Section 14.5, Liquid cooling example to Supplemental Section Clarified Example references in Supplemental Information Section • Added outline notches for 4C+ connectors to the board outline (all figures) • Added Statement to Section 10.1 that Platform Custom Zone outline may be modified based on connector choices. • Route KOZ added to HPM Retention hole, impacting Figure 18 and Figure 20 • Corrected Reference to SFF-TA-1002 • Added additional industry specifications to Section 13 References • Added requirement reference to battery backed voltage interface to DC SCM R2 • Updated Centerline labeling drawings with 4C+ connector dimensioning
10/26/2022	1.0 RC5	• Updated pin naming on Control Panel connector drawing Figure 12 to match M-PIC naming convention • Updated line 195 wording to match DNO, fix typo.

3. Scope

This document defines technical specifications for the Full Width HPM Form Factors used in Open Compute Project, Data Center Modular Hardware Systems.

Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with all features or requirements described in this specification.

3.1. Items Not in Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

3.2. Typical OCP Sections Not Applicable

Open Compute documents are typically expected and desired to contain common document Sections. The DC-MHS specifications are comprised of Base Form Factor Specifications and Supporting Platform Connectivity specifications, and are structured such that the typical OCP document structure does not apply to this Base Form Factor Spec. This specification will not contain the following Sections.

- Rack Compatibility (See **Section 14.1 Rack and Chassis Depth Stackup Assumptions**)
- Physical Specifications
- Thermal Design Requirements
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

4. Specification Compliance Table

230 The following table is intended to summarize the list of attributes and requirements for a design to be DC-MHS M-FLW Base Specification compliant.

#	Technical Specification	Document Reference
1	PCB Tolerance Table	Section 10
2	HPM Outline(s) definition	Section 10.1, Figure 3
3	Minimum of 6 board mounting holes implemented	Section 10.2, Figure 4
4	Mounting Hole pad and KOZ requirements	Section 10.2, Figure 4
5	Hole required for HPM to Chassis Retention locking feature	Section 10.3, Figure 5
6	HPM to chassis retention KOZs required on Primary (Detail L and Secondary sides Detail M) around HPM Retention hole	Section 10.3.1, Section 10.13, Figure 18 and Section 10.14.1, Figure 20
7	HPM Handle requires a hole at Far side w/ specified geometry	Section 10.4, Figure 7
8	Required Locations of OCP NIC R3 and DC-SCM R2	Section 10.5, Figure 8
9	2x required instances of Control Panel Interface connectors per defined locations	Section 10.7, Figure 12
10	PDB Management Connector requirement and placement zone	Section 10.8, Figure 13
11	Internal USB connector and Intrusion Switch connector requirements and placement zone	Section 10.9, Figure 14
12	The Required connector for Near IO positions shall be SFF-TA-1033.	Section 10.11.1, Figure 16
13	Implemented Near IO Connector placement requirements	Section 10.11.1, Figure 16
14	7x riser retention hole requirements, locations, pads, KOZ's.	Section 10.11.2, Figure 17
15	Far Side HSIO connector choice height requirements	Section 10.12
16	Primary side component height restriction zones	Section 10.13, Figure 18
17	Secondary Side Zone 1 Exceptions shall not exceed combined nominal, max area per instance, and minimum spacing between instances	Section 10.14.2
18	Secondary Side Zone 2 0-height KOZs required (8x) on Secondary side	Section 10.14.3, Figure 20
19	Max Length of connector's alignment post/barb is 3.2mm	Section 10.14.3
20	Secondary Side Zone 3 KOZ's required under or near DIMM sockets	Section 10.14.4
21	HPM shall provide Secondary supports that attach in Zone 3	Section 10.14.4
22	Zone 4 Board Thickness + Backplate Thickness <= maximum defined calculation/formula	Section 10.14.5
23	Maximum allowed HPM Board thickness is 3.18mm	Section 10.15
24	HPM shall implement KOZ's on Far side mounting holes for Thermal solution brackets	Section 10.16, Figure 27
25	Required Locations for M-CRPS connectors	Section 11.1, Figure 30
26	HPM 2x6+12s PICPWR connector placement	Section 11.2, Figure 32
27	Minimum HPM Power Supply Rail Requirements per PCIe CEM Slot	Section 11.3, Table 6
28	HPM shall be required to implement electrical interfaces that must follow the DC-MHS family of specifications	Section 12
29	HPM shall implement battery backed voltage interface per DC-SCM R2.0 "Battery Voltage" requirement.	Section 12

5. Overview

The objective of this specification is to specify the requirements of a Full Width Host Processor Module (HPM). This is for use within products designed for minimum 19” rack, also known as compliant with EIA-310-E but can also accommodate larger 21” racks. This form factor enables a full width HPM usage for CPUs, DIMMs, and related features. This full width form factor generally allows for maximum IO of the CPUs to be offered and brought to accessible slots (although exceptions could occur in the future). This specification will NOT reference a specific CPU or memory technologies. The goals and success criteria of this specification is so that multiple generations of CPU/Memory (Compute Core) designs can be designed into this form factor specification, so that chassis and system designs can be reused as desired. This should have the benefits of reduced design investment, reduced validation investment, and faster development cycle time.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of customers and vendors of Enterprise and Cloud Full Width Server rack products. Examples include mechanical form factor, placement guidance of common subsystems and placement guidance of motherboard Input-Output (IO) connections.

6. DC-MHS Family of Specifications

The **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**ul**L** **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310-E Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**n**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310-E Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- **Current Connector List** – Vendor and part number information for all connectors referenced by DC-MHS specifications, updated as needed. Full URL: https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/

To access additional DC-MHS specifications please visit the OCP Server Project Wiki - Working

7. Terminology

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for spec compliance	
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
PCB	Printed Circuit Board	
Datum	A plane, axis or point location from which dimensions and tolerances are referenced.	
DC-SCM	Datacenter Secure Control Module Rev 2.0 as defined by OCP DC-SCM Rev 2.0 spec	
CPU	Central Processing Unit	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link, open standard for CPU to device and CPU to Memory connections.	
Chassis-Board Bracket	Bracket that attaches to a HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan Sub-pan
Near	Board location or zone, related to section of board containing DC-SCM Rev 2.0, Management subsystem	
Far	Board location or zone, opposite of location of Management Subsystem	
Platform	Complete system including HPM, power, peripherals, etc	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
Platform Infrastructure Connectivity Spec	A Specification that defines Platform Interconnect details for features that are common across many HPM Form Factors. Examples connectivity features include fans, backplanes, and control panels.	M-PIC spec
KOZ	Keepout Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
Compliant HPM	An HPM which meets every item listed in the base specification compliance table.	
Adapted HPM	An HPM which has strong correlation to base spec requirements but does not meet every item in the base specification compliance table.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements the HPM form factor specification.	
System Designer	The person or organization designing a system which incorporates HPMs (whether compliant or adapted) into the system design.	

8. Background and Assumptions

This Full Width HPM Form Factor specification is created to enable typical platform feature sets for both Front and Rear Management, in 1U and 2U chassis applications. Some of the platform features that are common in the industry, and influence the Form Factor constraints are:

- Chassis installation within minimum EIA-310-E racks (but not limited to).
- PCIe (Version 5.0 and future) Card configurations typically offered by Enterprise OEMs/Hyperscalers. See **Figure 35. Examples of Typical 1U / 2U PCIe Slot** and **Figure 36. Examples of Typical 1U / 2U PCIe Slot Configs for Front** Management System
- In the 1U PCIe offering, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would require more restrictive Compute Core placement (not defined).
- HPM enabled minimum 75W of power per PCIe slot, with ability to scale up to 600W for some slots (likely 3~4).
- The specification details support for the Open Compute peripherals directly connected to board
    - OCP NIC R3.0
    - DC-SCM R2.0
    - *Note: A s*ystem is not limited to one device of each type; configurations with >1 DC-SCM R2.0 are possible, but outside the scope this specification will cover.
- Thermal Design Points considerations includes keepout zone to enable air cooling thermal solutions that extend beyond the CPU and Memory sockets. Memory TDPs under consideration are in the 20-25W range.
- Considerations for Liquid cooling solutions, including CPU cold plates and DIMM liquid cooling manifolds.
- Considerations for Power Delivery to important chassis subsystems.

8.1. Rear Management (ie, OEM) Architecture Assumptions

a. Chassis depth constraints in consideration of Power Distribution Units placed approximately 780mm from front EIA mounting flange.

b. Enterprise Storage and Fan subsystems requiring approximately 220mm. (See **Figure 34. Rack Depth Constraints)**

c. Sliding rack rails that require a max overall chassis width of 434mm, with interior chassis width/opening of minimum 427mm.

d. Considerations for power and High-Speed IO cabling

e. Considerations for ease of installation and removal of motherboard in a chassis.

f. Adequate delivery power through HPM to enable typical storage configuration power loads.

8.2. Front Management (ie, Hyperscale) Architecture Assumptions:

a. 1070mm rack depth

b. All IO generally on cold aisle but may also include some architectures with hot aisle IO. Assuming Front/Near end of system supports IO devices such as PCI CEM, OCP NIC R3.0, SSD's, etc

c. PCIe also distributed at Far end, such as to backplane, OAI – Universal Baseboard, and other items.

d. AC or DC rack power supplied by rack from the hot aisle

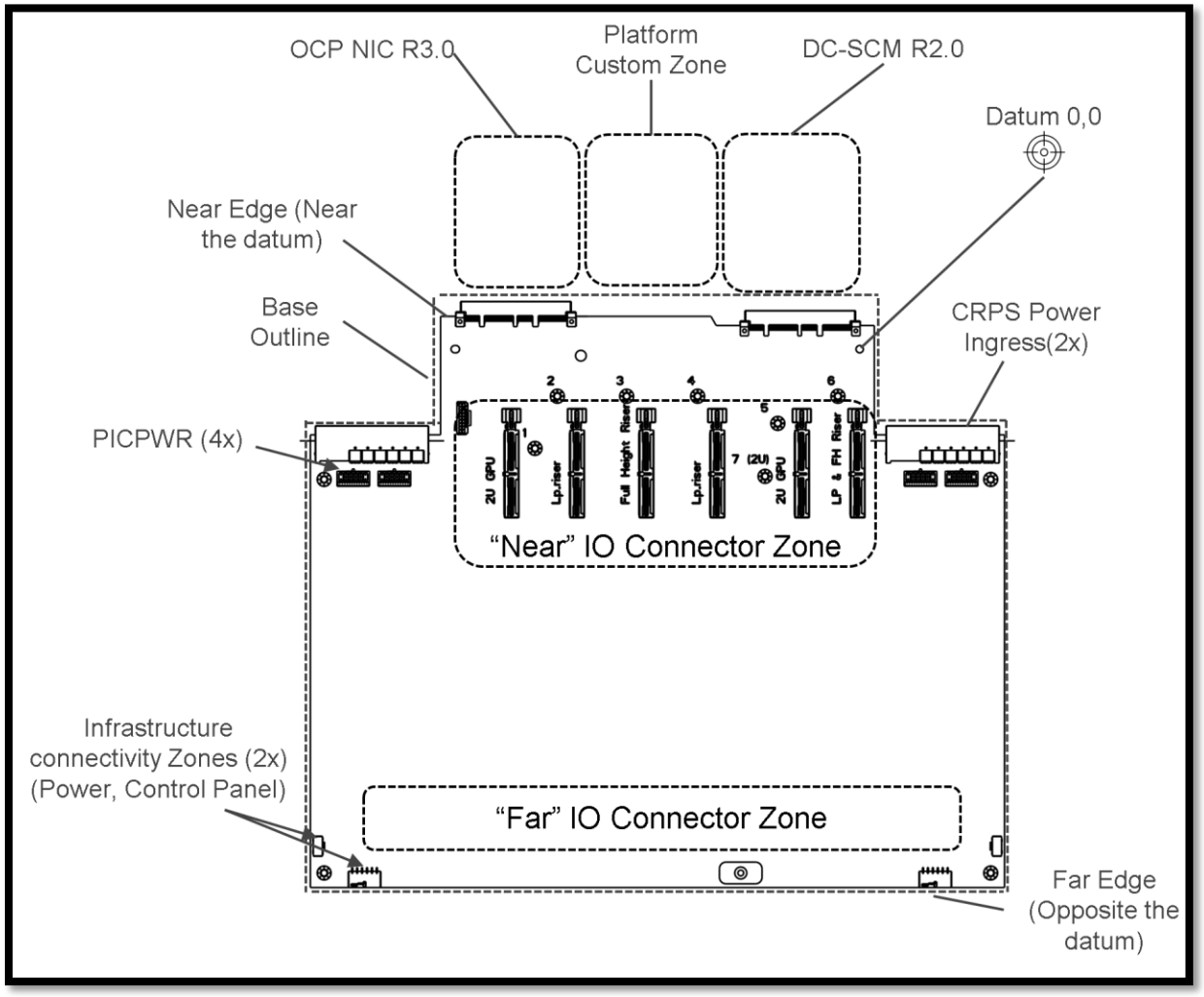
e. If PSUs are used, they are not hot serviceable

9. HPM Layout

The following **Figure 1** shows the layout and approximate locations of major subsystems in the Enterprise and Hyperscale M-FLW HPM.

"Near" and "Far" are reference naming conventions to the side of the board and Compute Core, as to orient the reader as to which portion of the board and Compute Core is being referred to. This specification refers to the Near Side as where DC-SCM R2.0 Management subsystem resides as a board peripheral. This is also typically referred to Rear IO location for Enterprise products, in which products are designed with IO in the hot aisle of a rack deployment (air exit). This is also typically referred to Front IO location for Hyperscale products, in which products are designed with IO in the cold aisle of a rack deployment (air inlet).

Figure 1. Full Width HPM Layout Diagram



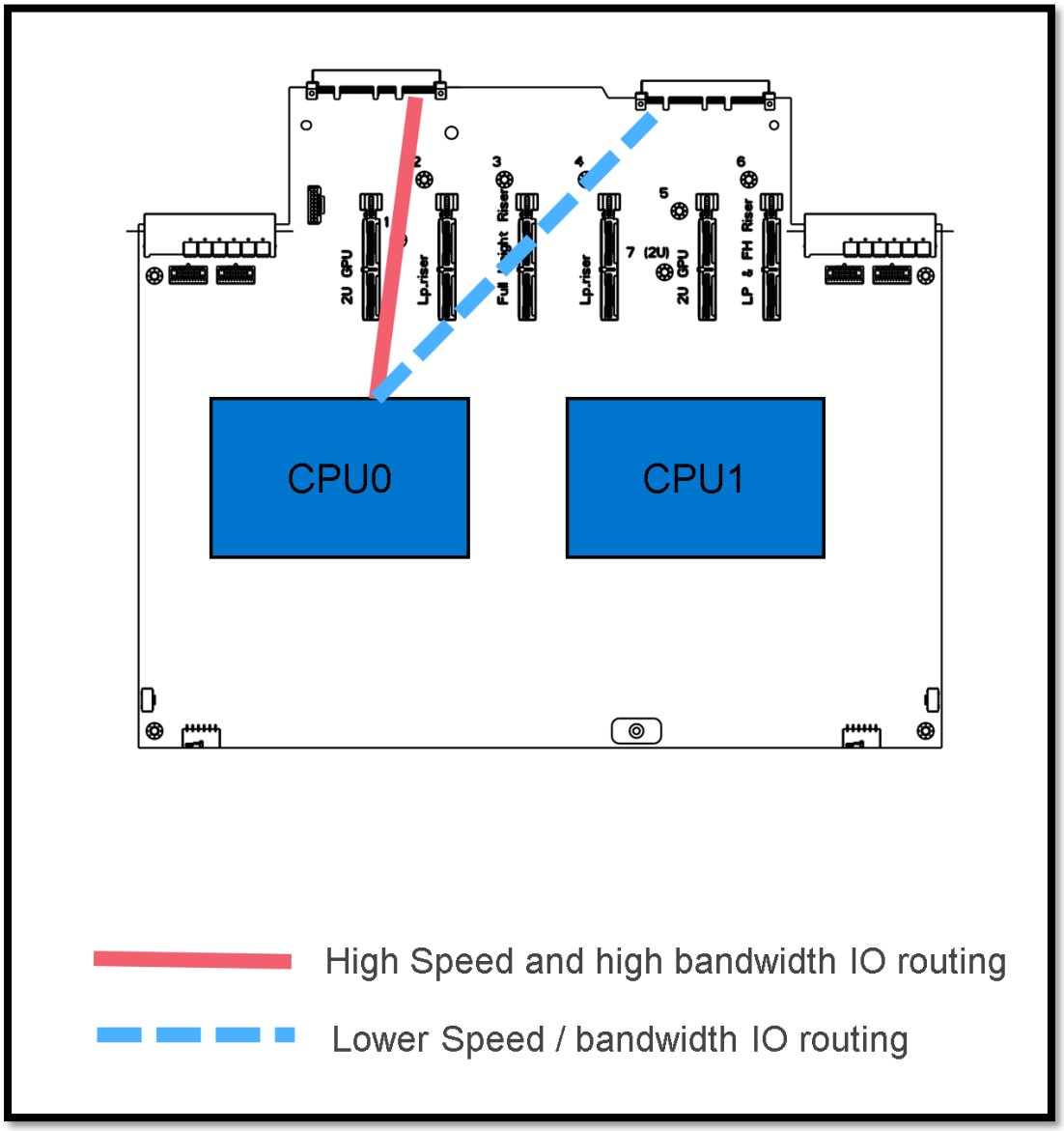
9.1. Two Socket (CPU) Assumptions

The OCP NIC R3.0 subsystem is positioned on the left based on two assumptions:

- In a 2S (CPU) system, the First/Boot CPU in a two CPU HPM is positioned on left.
- OCP NIC R3.0 is directly routed through the motherboard to the first/boot CPU.

The OCP NIC R3.0 is intended to be closer to this boot CPU to best enable the high-speed IO routing. The OCP NIC R3.0 will usually require higher bandwidth routing, and thus should be optimized for material selection and cost impacts. The routing from first/boot CPU to management subsystem (DC-SCM R2.0) has lower bandwidth requirements, and thus should not be the determining factor in board material selections and routing strategy. See **Figure 2**.

Figure 2. First CPU position relative to OCP NIC R3.0 and DC SCM R2.0



In this specification the CPU and Memory locations are intentionally not specified. This is for future flexibility in CPU/Memory quantities, locations, sizes, etc. The board area between DC-SCM R2.0 and OCP NIC R3.0 is designated as a “Platform Custom Zone”, as shown in **Figure 1. Full Width HPM Layout Diagram**. The goal is to provide board area and system volume for individual platforms to provide system specific features.

9.2. One Socket Assumptions

In theory, for a one socket (CPU) platform, the OCP NIC R3.0 location does not have a strong affinity to either side. The OCP NIC R3.0 should remain in the specified HPM location (left) for chassis compatibility for all Full Width HPM products**.** The second OCP NIC shown in the Platform Custom Zone is optional, the OCP NIC on the left must always be populated.

10. Mechanical Requirements

In addition to the drawings and details within this document, DFX/CAD file link is provided in **Section 14.9 CAD files**.

All units are in millimeters, unless otherwise specified. The following standard tolerances apply to all drawings unless otherwise specified. PCB dimensions shown in this specification shall comply to the following tolerance table, unless otherwise specified.

Table 1. Tolerance Table

Dimension Type	**Tolerance***
FROM Origin/Datum hole center TO round fiducial center	+/- 0.076mm (+/- 0.003 inch)
FROM Origin/Datum hole center) TO profiled card edge	+/- 0.254mm (+/- 0.010 inch)
FROM Origin/Datum hole center TO drilled hole center	+/- 0.127mm (+/- 0.005 inch)
FROM Profiled card edge TO profiled card edge	+/- 0.127mm (+/- 0.005 inch)
Feature of size (hole diameter, slot width, etc.)	+/- 0.100mm (+/- 0.004 inch)
PCB thickness	+/- 10% of nominal

*Unless Otherwise Specified

Route KOZ's referenced in this specification, at a minimum, refer to surface layers and microstrip routing. Further application of the Route KOZ to other layers is the choice of the HPM designer and/or Design specification.

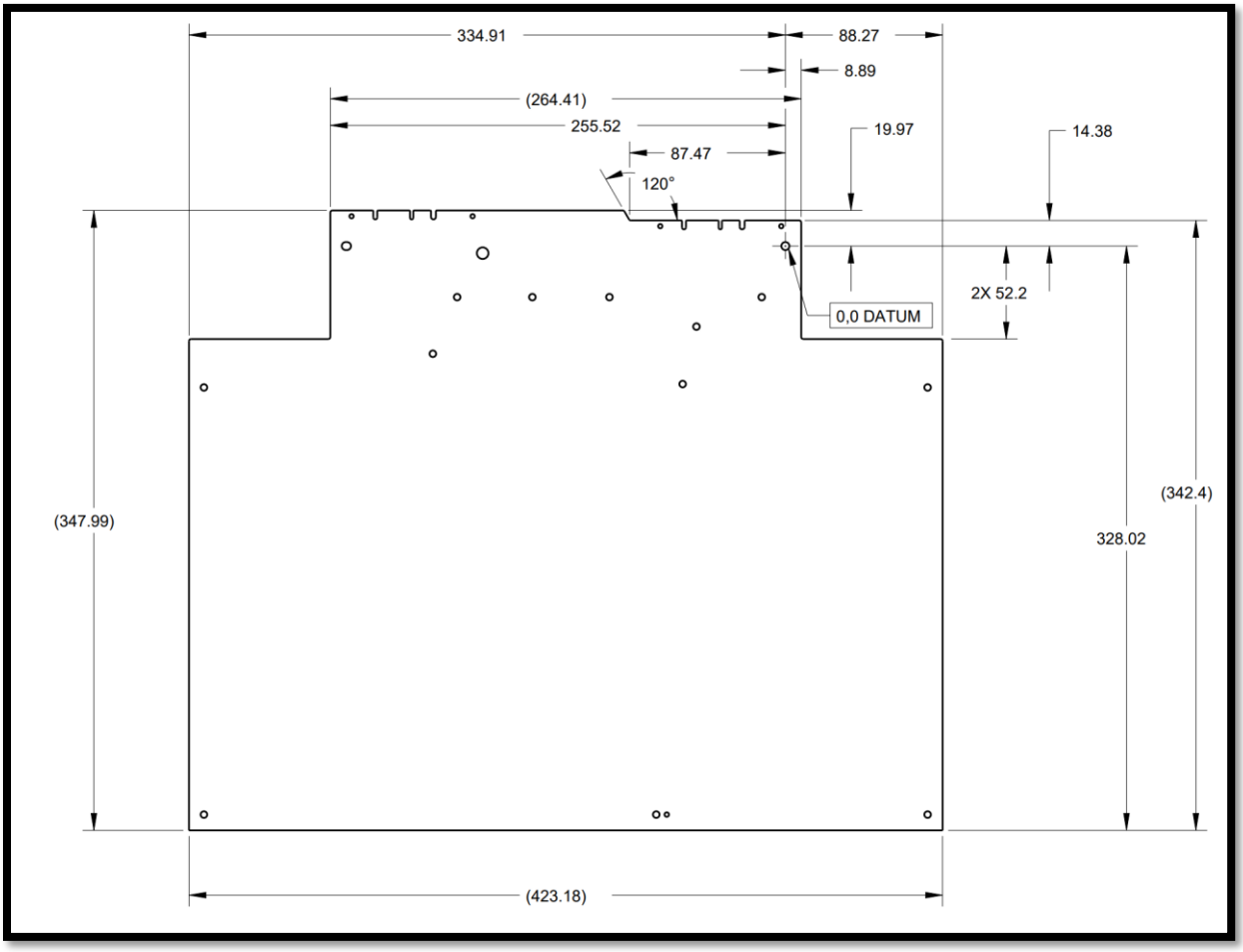
10.1. HPM Outline

The outlines defined in this section shall be followed for M-FLW Base spec compliant HPM.
(Note for 1.0 release, there is only one Type defined.)

The Full Width Type 1 HPM (M-FLW) base outline is defined in **Figure 3** and shall be followed for a M-FLW Base Specification compliant HPM. This defines the outline and peripheral locations to fit compute core and IO elements in an FLW compliant chassis. This is intended to fit a wide variety of platform and chassis applications. The intent is to show overall dimensions of board outline.

DFX/CAD file link is provided in **Section 14.9 CAD files**.

Figure 3. Full Width Type 1 Outline



Note: The outline of the HPM near Platform Custom Zone (described in Section 10.6) may change for connector choice compatibility specific to the usage of the Platform Custom Zone.

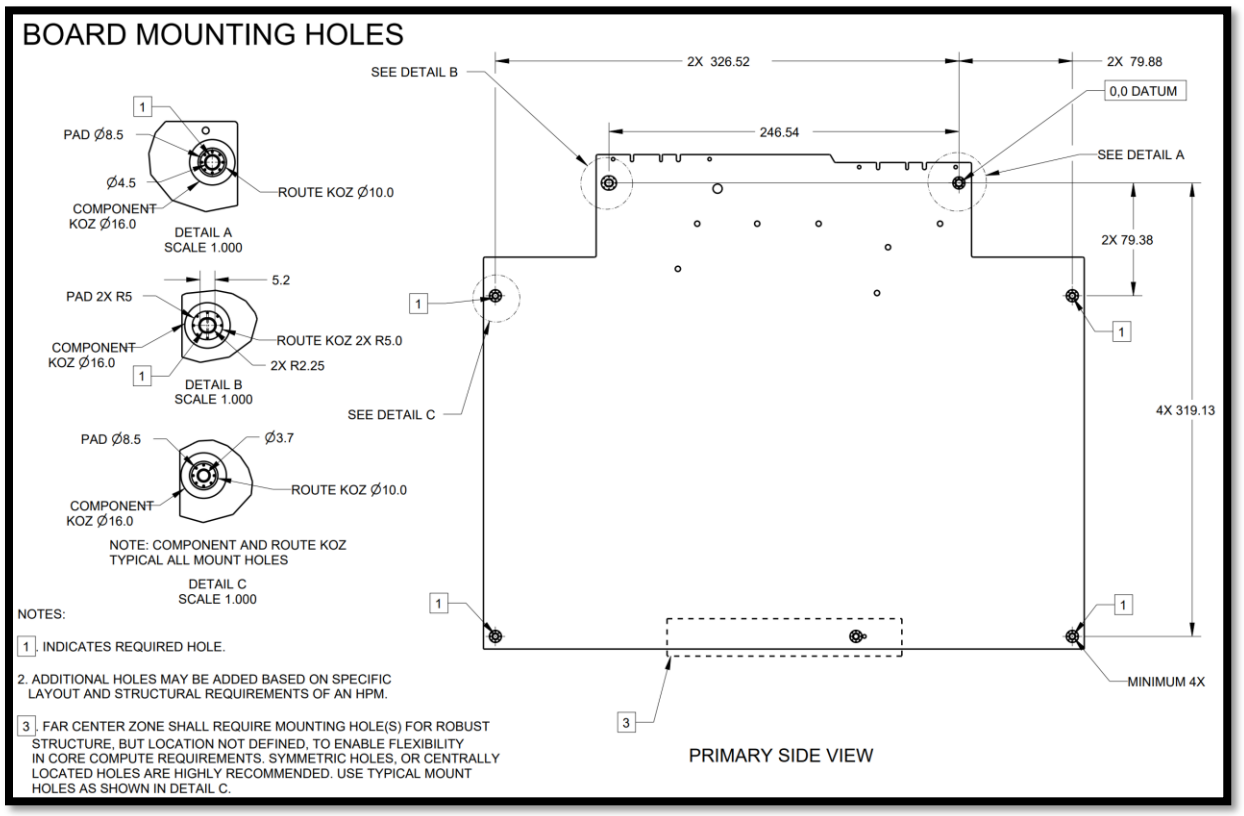
10.2. Board Datum and Mounting holes

A set of six required board mounting holes specified shall be implemented around the board perimeter per **Figure 4** and represent the minimum mounting hole requirements. These six boards mounting holes may interface to the Chassis-to-Board Bracket (Board Pan) or a chassis base.

Additional mounting holes are allowed as needed, to ensure appropriate mechanical support of the Compute Core (not shown). Additional board holes are expected to interface to the board-chassis bracketry and should be designed in consideration of the bracket to chassis interface features, as defined in **Section 10.3 HPM to Chassis Retention.** A design should follow good engineering practices and in consideration of platform shock and vibration requirements. Shock and vibration requirements are not in scope of this specification.

The mounting holes shall have a pad and component KOZ as defined in **Figure 4** . The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension, it is considered adequately robust, and an exception will allow such component to encroach on the Component KOZ's in **Figure 4**.

Figure 4. Board Mounting Holes with Pads and Keepout Zones (Top / Primary side view)



Additional References:

- The Secondary side pad and KOZ requirements for mounting holes are shown in **Figure 20. HPM Secondary Side Height Keepout Zones, Pads, KOZ**
- There are seven additional required holes shown in **Figure 17. 1U and 2U Near Side Riser Retention Enablement Holes**, which are the holes intended to be used for Riser hardware retention.

Implementors Note:

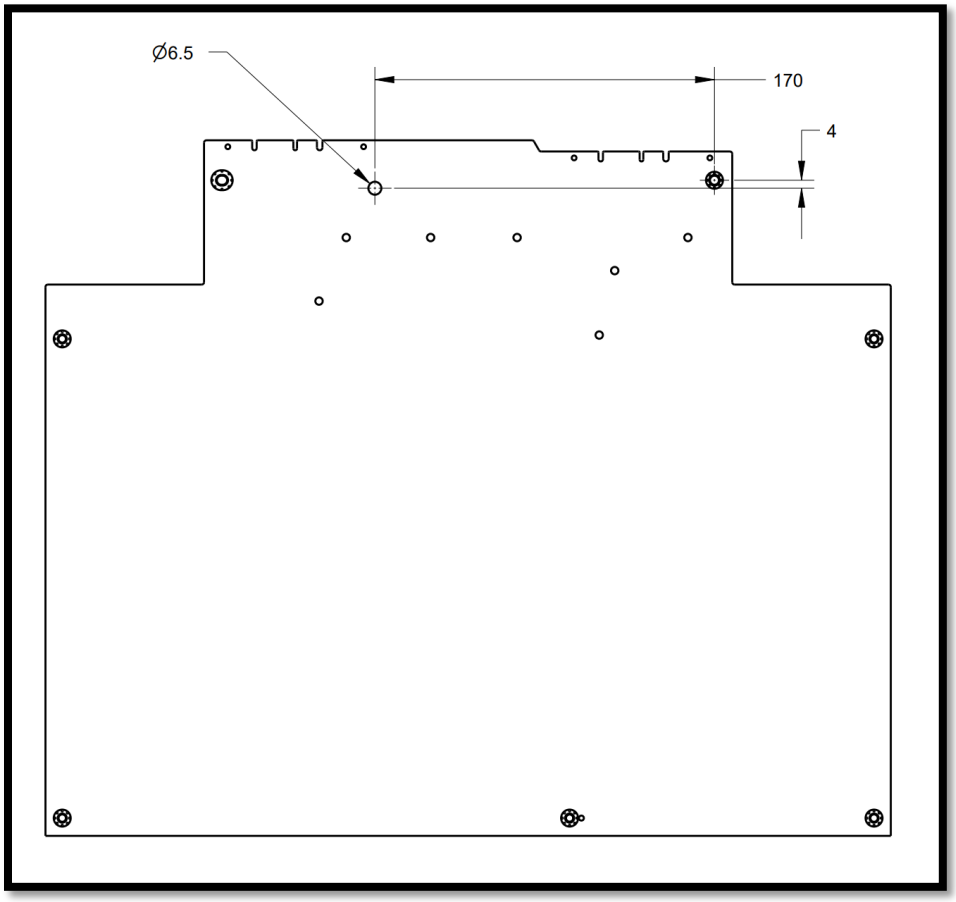
The PCB Datum hole (Detail A) is defined such that a collared standoff with tight tolerance fit can be used to control X-Y tolerances in HPM mounting. Additionally, a slotted hole (Detail B) is defined to control rotation around the datum, by allowing, as an example, a collared standoff to be used with tight fit to the top/bottom edge of the slot.

All other mounting holes follow standard mounting hole guidance (Detail C). These mounting holes are expected to have clearance fits to screw hardware.

10.3. HPM to Chassis Retention

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required on HPM to be used for HPM retention to the chassis, located at the required location in **Figure 5**. The hole is sized for common retention methods such as plungers, thumbscrews, etc.

Figure 5. HPM Assembly to Chassis Retention Enablement



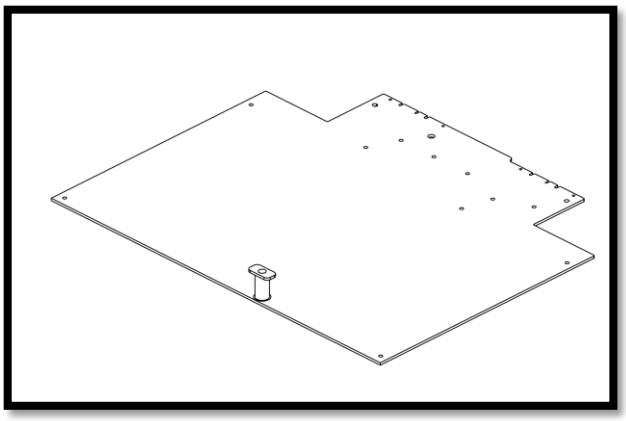
10.3.1. Keepout Zone for Retention Hardware

A keepout zone shall be implemented on both topside and bottom side around the Retention Hardware hole. The Primary (or Topside) KOZ is defined in **Section 10.13**, **Figure 18. Zones for Primary Side Component Height Restrictions.** For Secondary side KOZ, refer to **Section 10.14, Figure 20** (Detail M)**.**

10.4. HPM Handle Hole

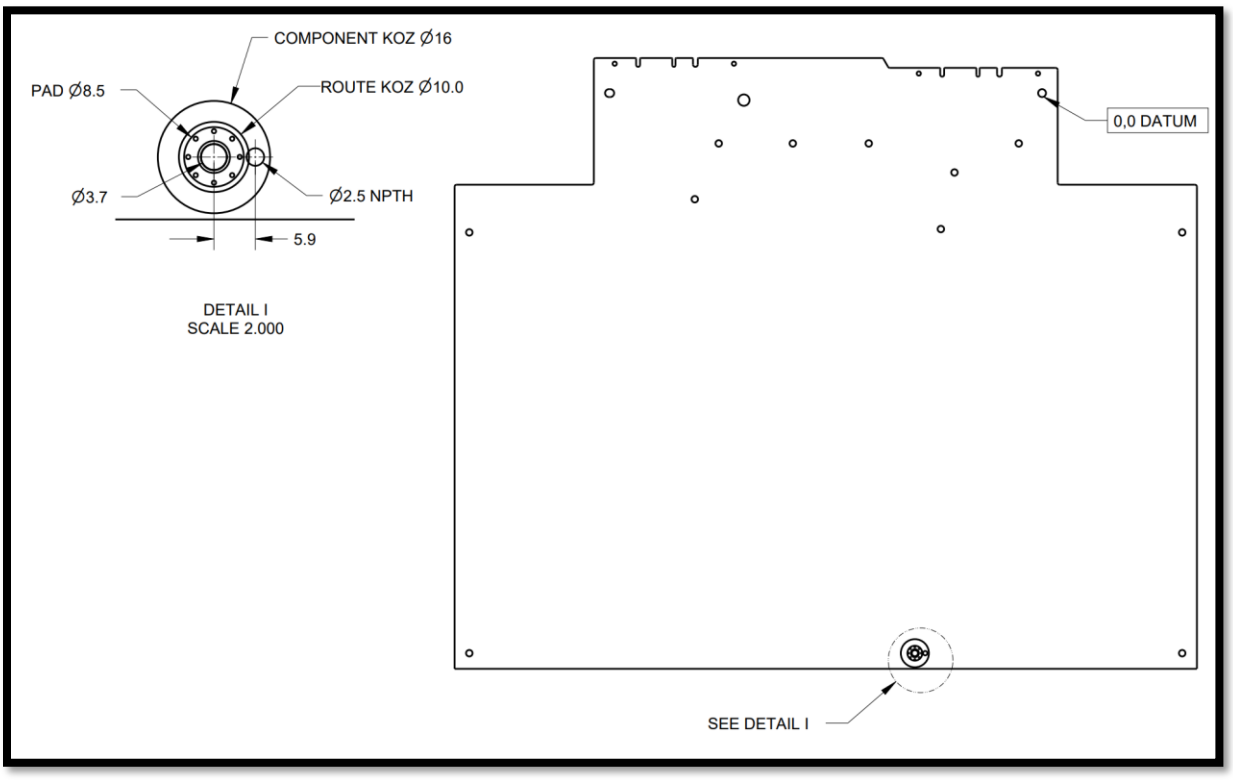
The FLW HPM shall require a hole interface to a mechanical handle near the Far Side Edge, with required geometry, pad and KOZ's specified in **Figure 7**. This handle solution may be implemented with, but not limited to, a plastic handle. Example is shown in **Figure 6**.

Figure 6. HPM Handling Feature



The location of the hole on the Far side is not specified but should be placed considering Compute Core details, such as Far High-Speed IO cabling, and Thermal solution keepout. To balance handling of board with chassis retention feature (near DC-SCM R2.0), it is preferred to place the handle feature to right half of the HPM.

Figure 7. HPM Handle Hole Detail



Implementors Note:

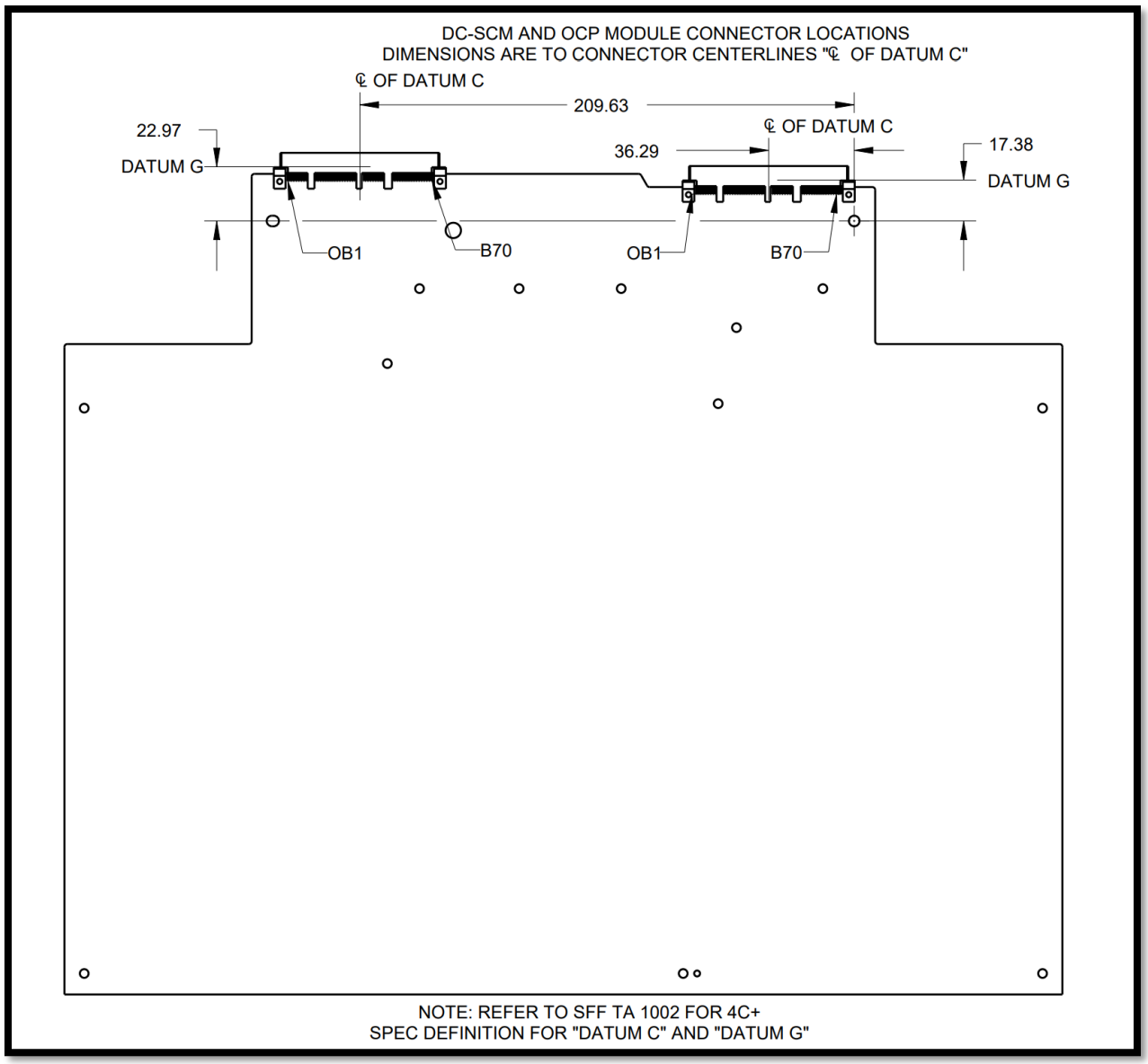
The HPM Handle Hole may also be considered a mounting hole for structural purposes. Platform designers should ensure their handle design supports the HPM. For example, a designer does NOT need to place a board mounting hole near the HPM Handle Hole.

10.5. OCP NIC R3 and DC-SCM R2 at Near Edge Locations

The HPM shall place the OCP NIC R3 and DC-SCM R2 at the locations defined by the centerline location of each of the connector subsystems in **Figure 8.**

Each of these peripherals leverages connectors defined by SFF-TA-1002, including centerline definitions referenced in the Figures of this specification. (Refer to the DC-MHS Connector List for vendor part number details).

Figure 8. Centerline Locations of OCP NIC R3.0 and DC-SCM R2.0



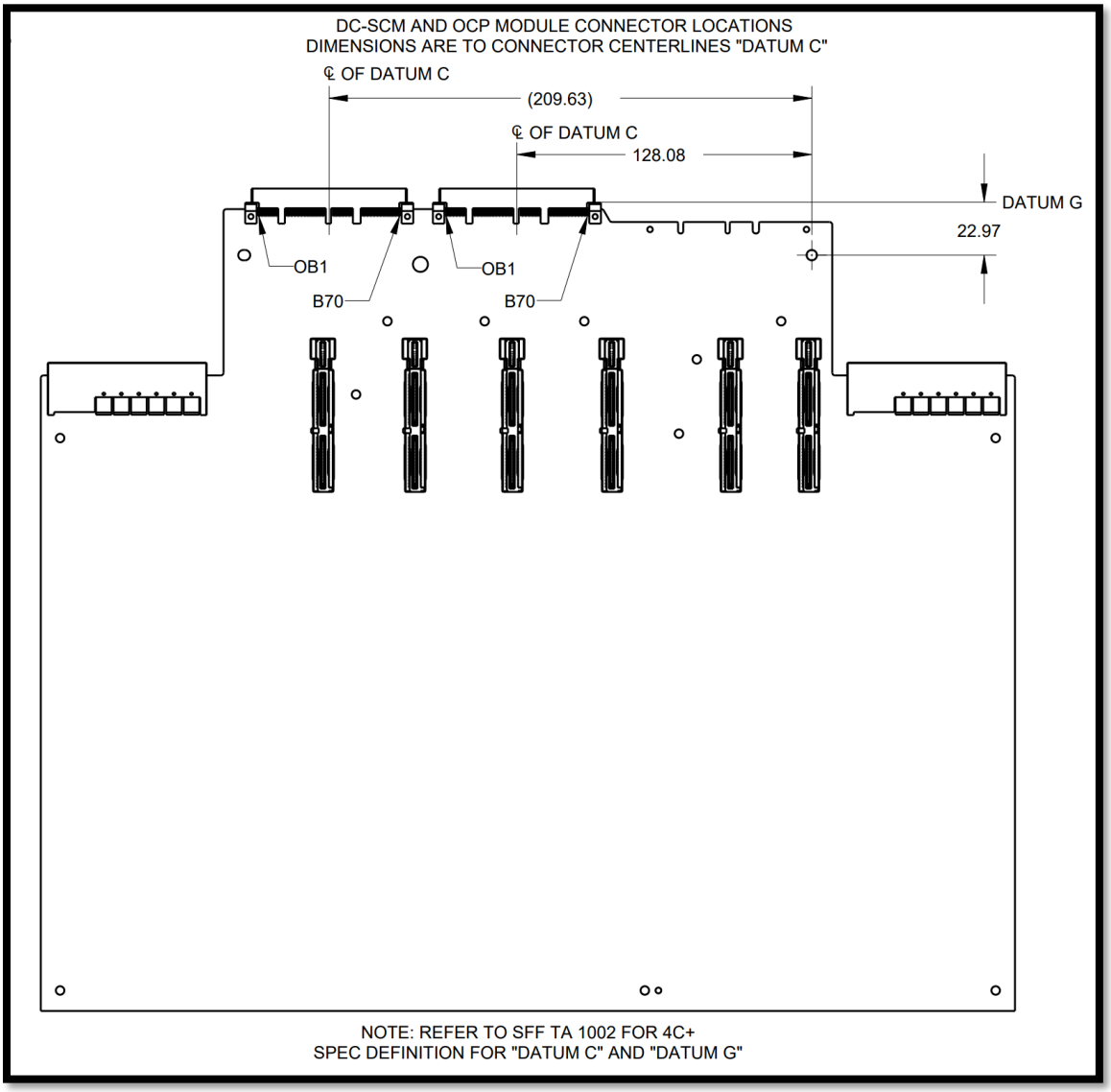
10.6. Platform Custom Zone

The Platform Custom Zone is defined as the Near Edge between the OCP NIC R3 and DC-SCM R2. (See **Section 9 HPM Layout**.) This area is intentionally undefined, so that System Designers may provide their desired features for the target platform. The specification will define some options that are considered common use cases, to promote greater compatibility between future HPMs.

10.6.1. Second OCP NIC R3

An HPM design may want to support a second OCP NIC R3. These HPM designs should follow the placement guidance in **Figure 9** for the second connector.

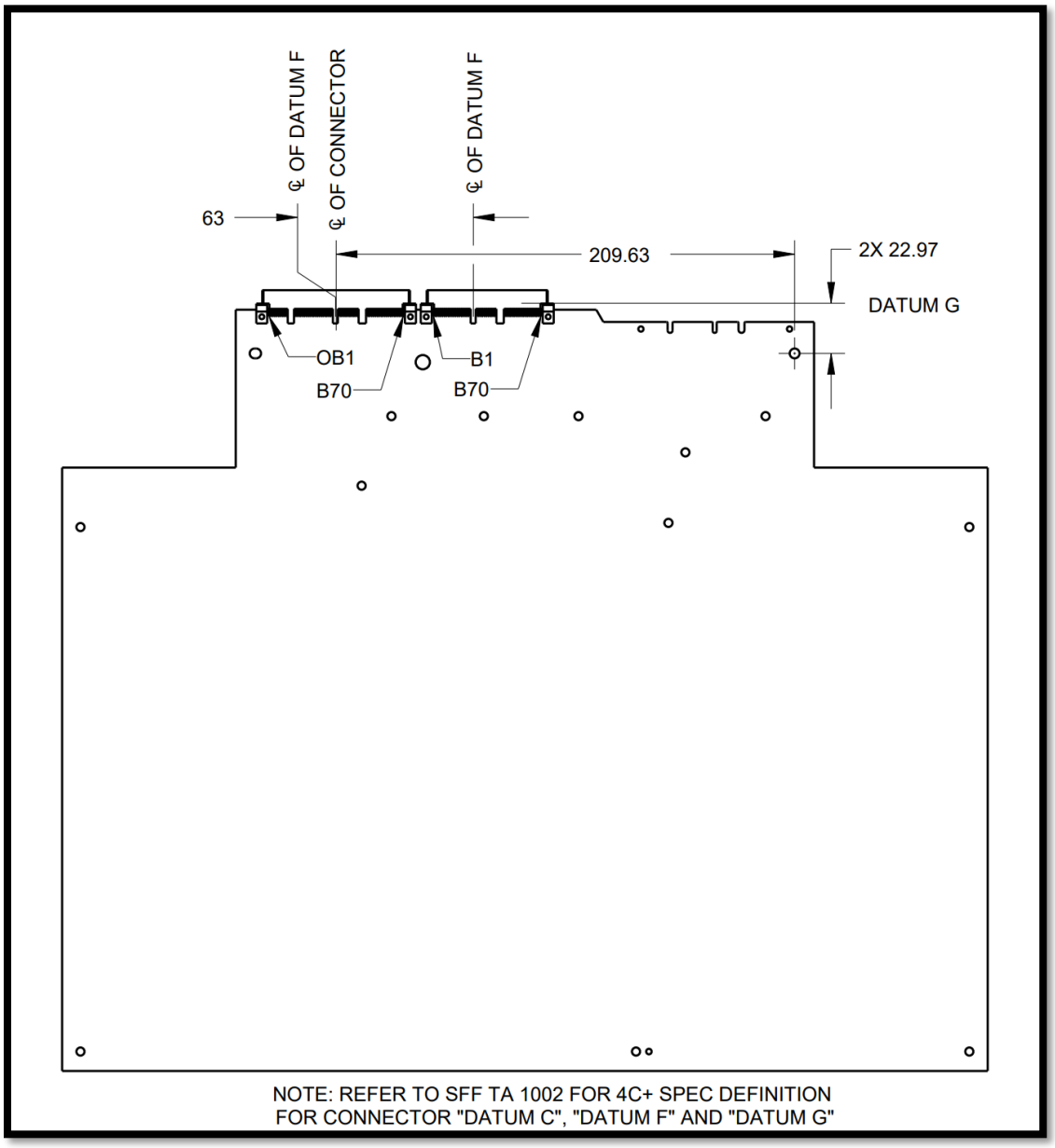
Figure 9. Location for Second OCP NIC R3 in Platform Custom zone



10.6.2. OCP NIC R3 LFF

An HPM design may want to support an OCP NIC R3 LFF, instead of a single SFF. These HPM designs should follow the following placement guidance in **Figure 10** for the LFF connectors.

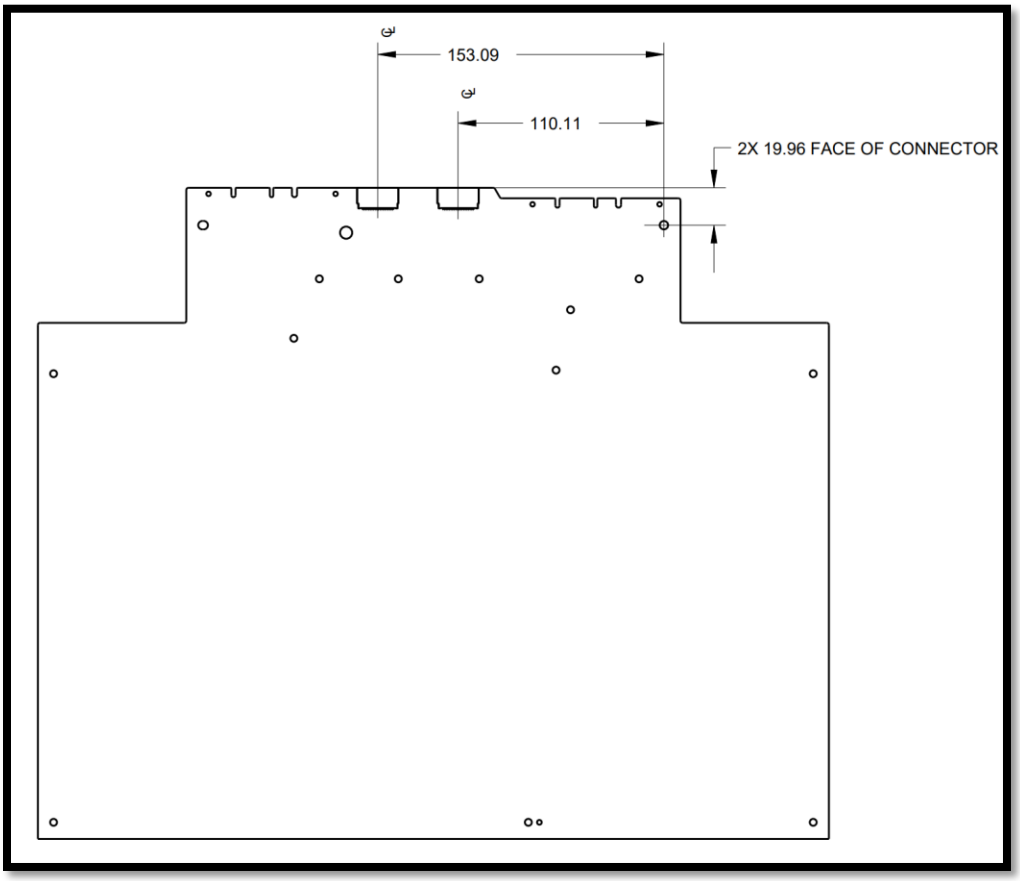
Figure 10. OCP NIC R3 LFF support



10.6.3. Direct Dock E1.S

An HPM design may want to support direct docking E1.S (EDSFF) in the Platform Custom Zone. These HPM designs should follow the following placement guidance for SFF-TA-1002, 1C connectors. See **Figure 11**. See M-PIC specification, chapter “E1.S Direct Attach Boot Storage” for complete connector and pinout guidance.

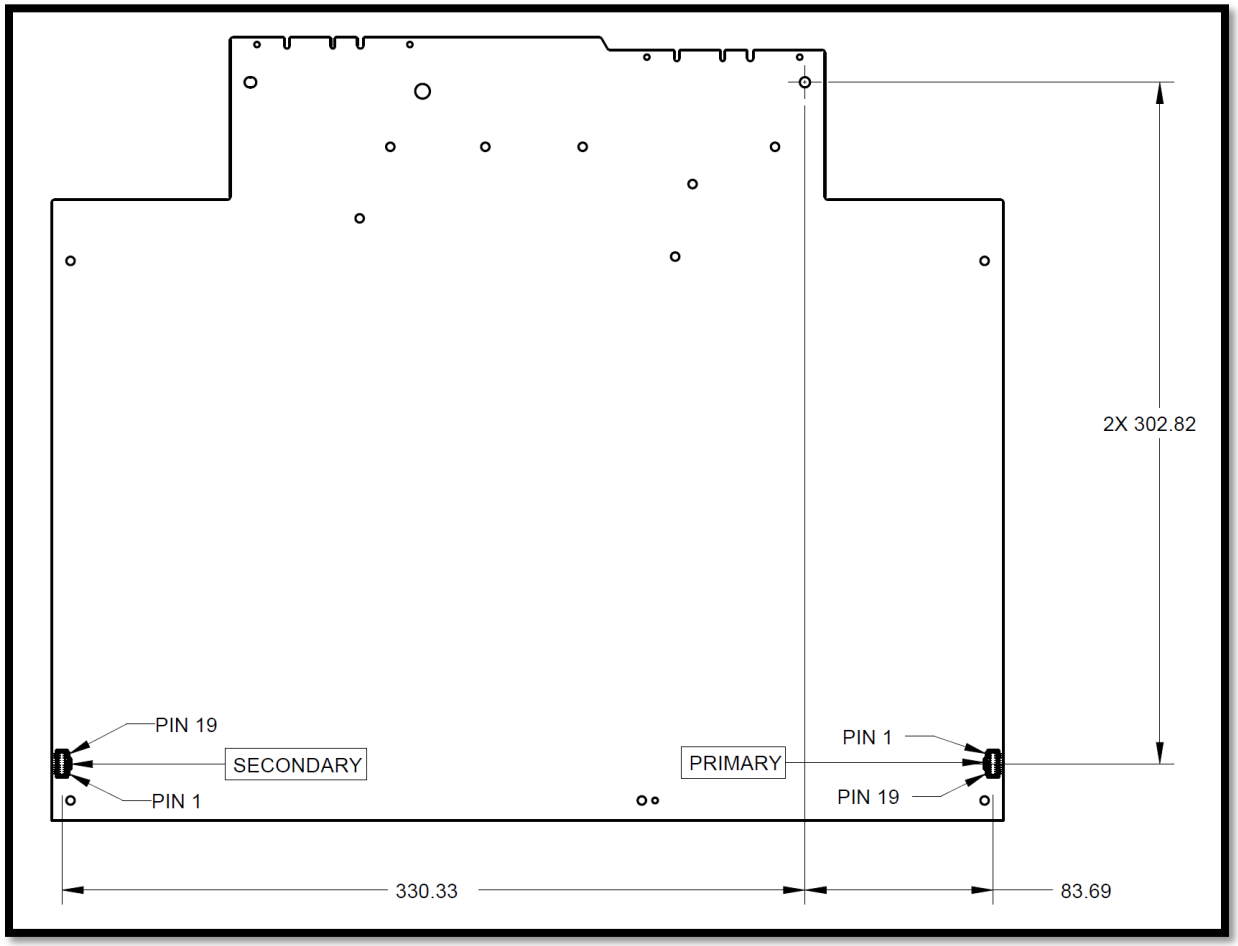
Figure 11. Direct Dock E1.S connector Enablement



10.7. Control Panel Connector Locations

The HPM shall implement two instances of the M-PIC defined Control Panel connections as shown in **Figure 12.** The Control Panel Connector details are further defined in M-PIC Section Reference: “Control Panel Interfacing”.

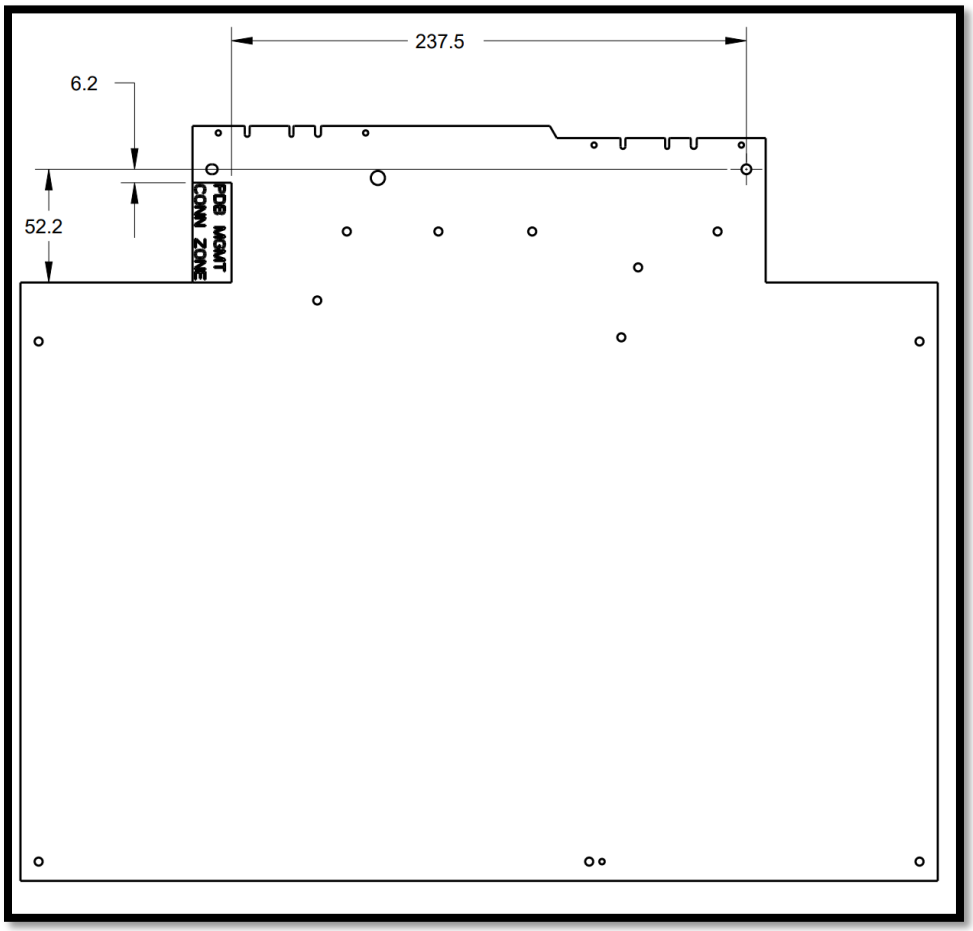
Figure 12. Control Panel Connection Locations



10.8. Zone for PDB Management Connector Header

The HPM shall implement a PDB Management Connector Header. The connector must be placed in the HPM within the zone defined by **Figure 13** (but can be depopulated in assembly BOM at a Design Specification level guidance). The PDB Management Connector details are further defined in M-PIC Section Reference: “PDB Management Connector Header”.

Figure 13. PDB Management Connector Header Location

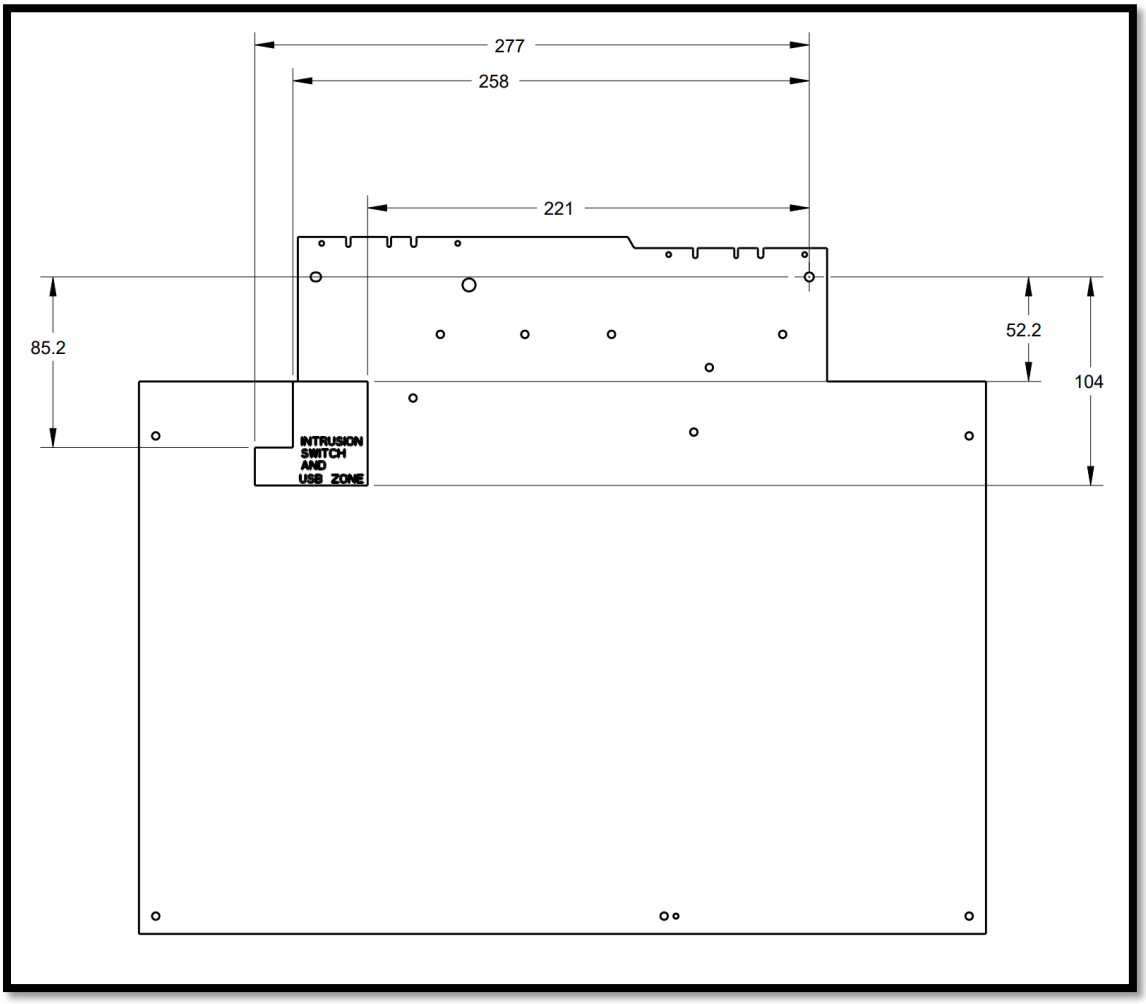


10.9. Zone for Intrusion Switch and Internal Host USB3 Connection

The HPM shall implement an internal USB3 connector. The connector must be placed on the HPM within the zone defined by **Figure 14**. The USB Connector details are further defined in M-PIC Section Reference: “Internal Host USB3 Connector”.

The HPM shall implement an intrusion switch connector. The connector must be placed on the HPM within the zone defined by **Figure 14**. The Intrusion Switch details are further defined in M-PIC Section Reference: “Intrusion Switch”.

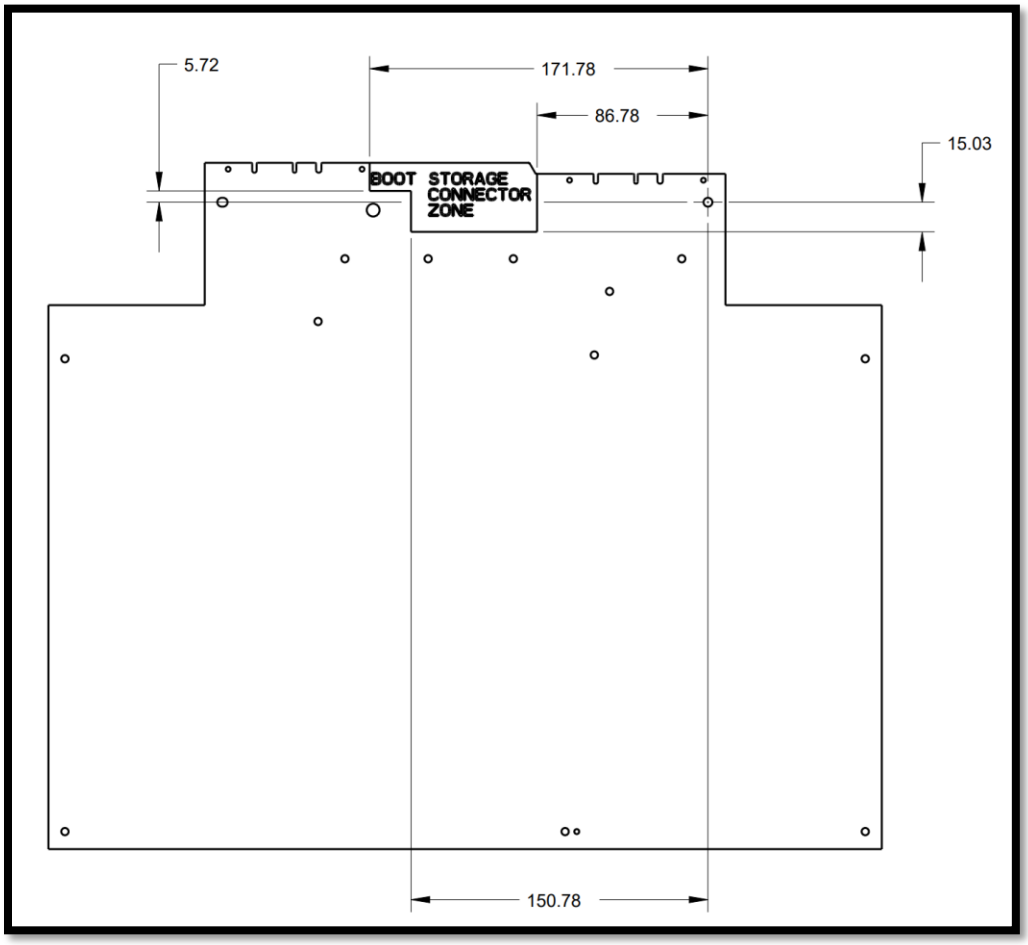
Figure 14. Intrusion and USB Connection Placement Zone



10.10. Boot Storage Connector Zone

The HPM is recommended to implement a Boot Storage Peripheral connector. The connector should be placed on the HPM within the zone defined by **Figure 15**. The Boot Storage Connector options and details are defined in M-PIC Section Reference: “Boot Storage”.

Figure 15. Boot Storage Connector Zone



10.11. Near Side IO Connectors

10.11.1. Location of Near Side M-XIO Connectors

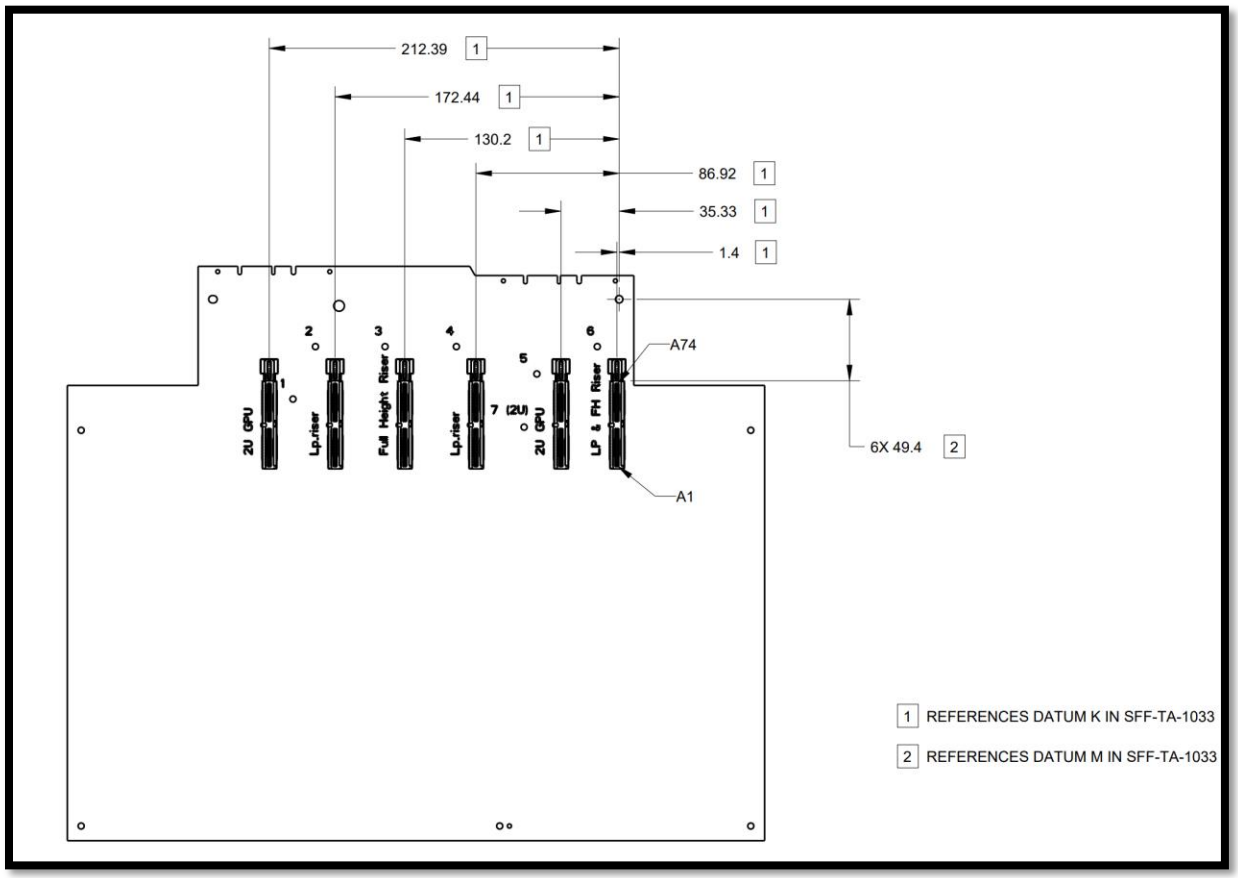
Note, that Near IO Requirements are mechanically focused to enable reuse of chassis and IO subsystems.

1. The required connector for the Near IO Riser positions shall be SFF-TA-1033
    a. Note, this Near IO connector can support either rigid or cabled riser connections.
2. An HPM might not use all six Near IO positions, but designers are recommended to use maximum number of possible positions. For Near IO implemented positions, the Near IO Connector shall be placed at locations defined in **Figure 16. Near IO Riser Connector Locations.**
3. Additional and/or Alternate connectors used within the Near IO zone are allowed. Alternate connector types, location and use cases are outside the scope of this specification.
4. Adoption of the following allocation priority in **Table 2** is recommended. Following this recommendation may result in increased applicability and interoperability of the HPM.

Table 2. Table of IO Allocation and Connector Population Priority for Near IO connector SFF-TA-1033

Recommended Priority	High Speed Connector Housing	High Speed Routing	Power Bay
1	X16	X16	power
2	X16	X8	power
3	X8	X8	Power
4	None	None	Power
5	Depopulate all connectors		

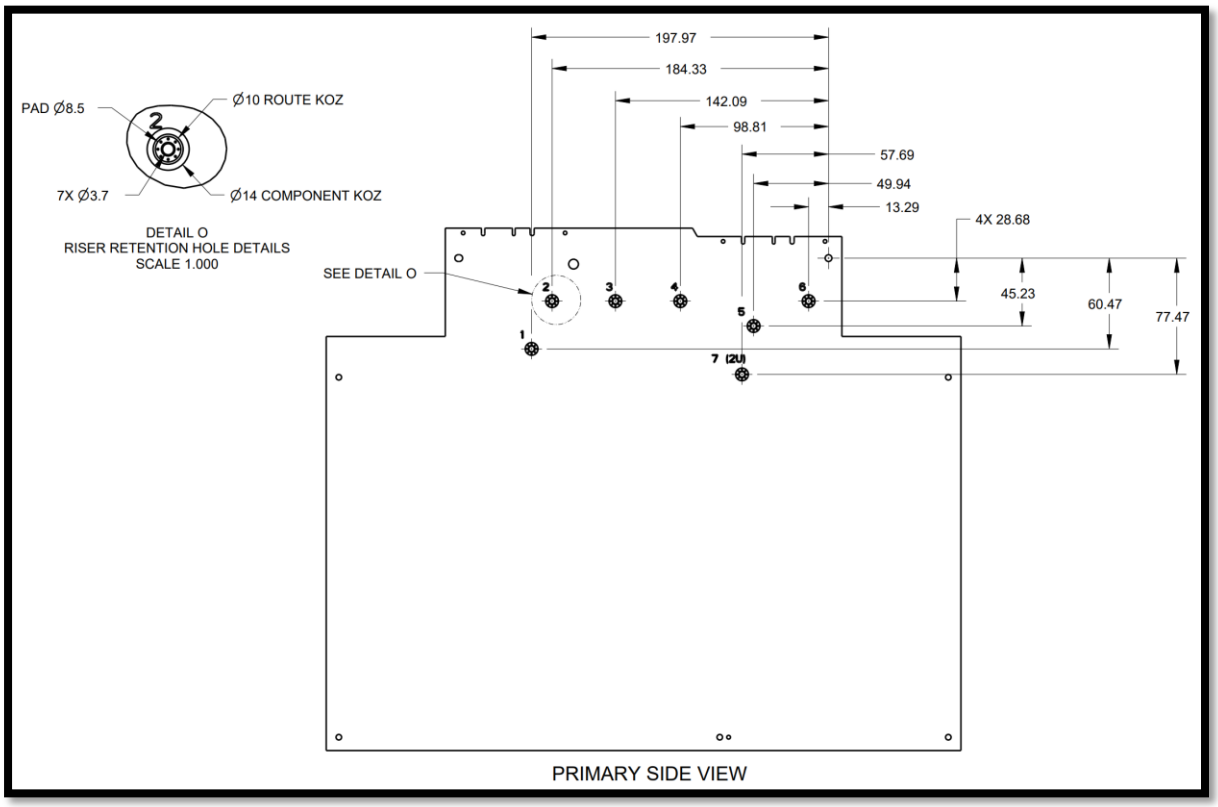
Figure 16. Near IO Riser Connector Locations



10.11.2. Riser Retention Hole Requirements for Near Side

The HPM shall implement seven riser retention holes associated with each Near IO connector position, as defined in **Figure 17** (including hole size, pad, and KOZ's). These are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). There is a total of seven holes associated with the six IO connectors. The riser retention holes are associated with both 1U and 2U PCIe Riser configurations. The riser retention holes are defined as a 3.7mm diameter hole, as shown in **Figure 17**, along with associated pads and component KOZs. Chassis Designers may choose the hardware and utilization method for riser retention.

Figure 17. 1U and 2U Near Side Riser Retention Enablement Holes



For further explanation on which mounting holes are associated with its Near IO connectors, see **Figure 38. Riser Retention Holes and Associated Near XIO Locations** in the Supplemental Information section.

10.12. Far Side IO Connectors

The Far Side IO connector locations referenced in **Figure 1. Full Width HPM Layout Diagram** are not specified because they are all assumed to be cable-only connections and will not have major dependencies to chassis or subsystem reuse compatibility.

High Speed IO connector choices for the Far Side shall be M-XIO compliant, and meet the Height Restriction requirements defined in **Section 10.13** . The recommended connectors for use in the Far Side are in **Table 3.**

Table 3. Far Side HSIO Recommended Connectors

Recommended Connector	Note
SFF-TA-1016	Must choose low profile variant
SFF-TA-1026	Appropriate due to low profile and ability to fit under thermal solutions

Implementors Note on SFF-TA -1016 Connectors

SFF-TA-1016 Connectors have mated height options above and below 12mm. System Designers should take these options into account with respect to the height restriction zones, if selecting SFF-TA-1016 connectors for an HPM.

10.13. Primary Side Component Height Restriction Zones

A Component Height Restriction Zone shall be required, per **Figure 18. Zones for Primary Side Component Height Restrictions** which applies to all soldered components; exceptions noted below.

If a cable connection (power, High speed IO, etc) is placed in the component height restriction zone, the max height restriction shall apply to the mated height of the plug and cable assembly, including component and assembly tolerances; exception noted below.

The exceptions allowed are:

- Special exceptions specified per zone in **Figure 18. Zones for Primary Side Component Height Restrictions**, such as DIMM sockets
- Zones that are classified as Recommended.
- The required Near IO connector (SFF-TA-1033 in **Section 10.11.1**) mated cabled height can exceed the 11.3mm height zone restriction

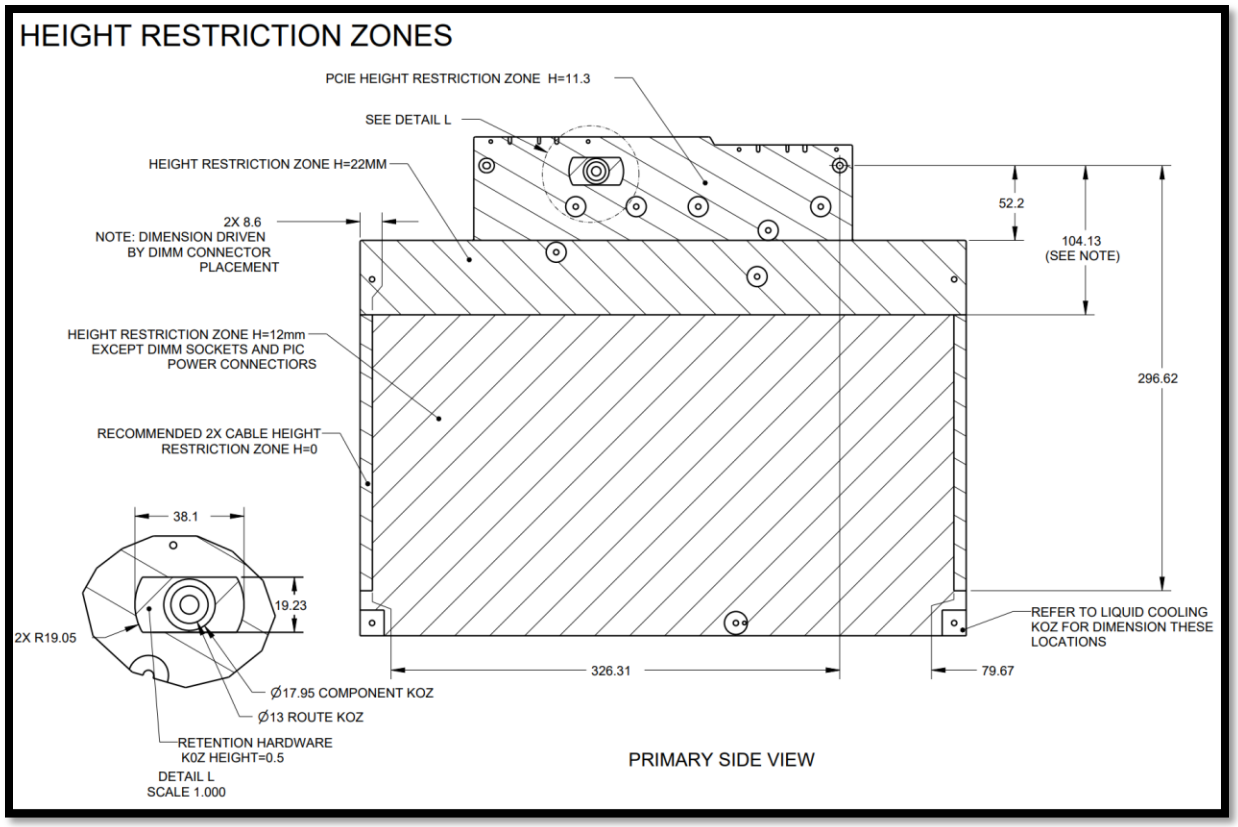
The dimensions indicated in **Figure 18. Zones for Primary Side Component Height Restrictions** are maximum heights. Component and assembly (solder) tolerances must be chosen to stay within the maximum height.

The purpose for these height restrictions is to enable:

- Thermal solutions to interface to Compute Core items such as CPU and DIMMs (not shown). Thermal solutions in scope include extended air heatsinks and liquid cooling solutions.
- Cable routing channels along HPM edges
- PCIe CEM cards on 1U risers

For thermal solutions, one must consider the allowable variance in numbers, types, and location of Compute Core items. Thus, a fixed 12mm for component height restriction in the Compute Core area is intended to allow air cooling heatsinks or liquid cooling hardware of any variance. DIMM sockets are exempt from the 12mm component height restriction. All other soldered board components must comply with exceptions noted in **Figure 18**

Figure 18. Zones for Primary Side Component Height Restrictions



Implementation Note:

The Height Restriction Zones defined in **Figure 18. Zones for Primary Side Component Height Restrictions** apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of solder components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

It is assumed that items such as CPU heatsinks, VR heatsinks, and shrouds are all designed by System Designers. And thus, the height and location tradeoff between these items are assumed responsibilities of the System Designer and not the HPM designer. The HPM Designer should consider best practices when making component placement choices. This makes no assumptions on the compatibility of Chassis, Peripherals or Thermal solutions. For future chassis and HPM compatibility, a System Designer is advised NOT design elements that intersect with the Height Restriction zone (Fans, Heatsinks, Risers, etc).

Recommended Cable Zero Height Restriction Zone: It is strongly recommended to implement a keepout zone to left and right of outermost DIMM sockets with a minimum dimension to HPM edge of 8.6mm, shown as Cable Height Restriction Zone in **Figure 18. Zones for Primary Side Component Height Restrictions**

This keepout is to enable HSIO cabling, power cabling and other platform infrastructure cabling to traverse from Near Side to Far Side zones, as needed by Platform Designers. (Designers should consider differences in DIMM socket widths from various vendors when determining DIMM placement.)

Implementation Note:

In some cases, a Compute Core design may only be able to deliver a desired capability by violating the cable keepout zone. By doing so, an HPM will cause issue with a platform's ability to cable High-Speed IO and Power delivery. In this case, a HPM Designer should make efforts to collaborate with Platform Designers on:

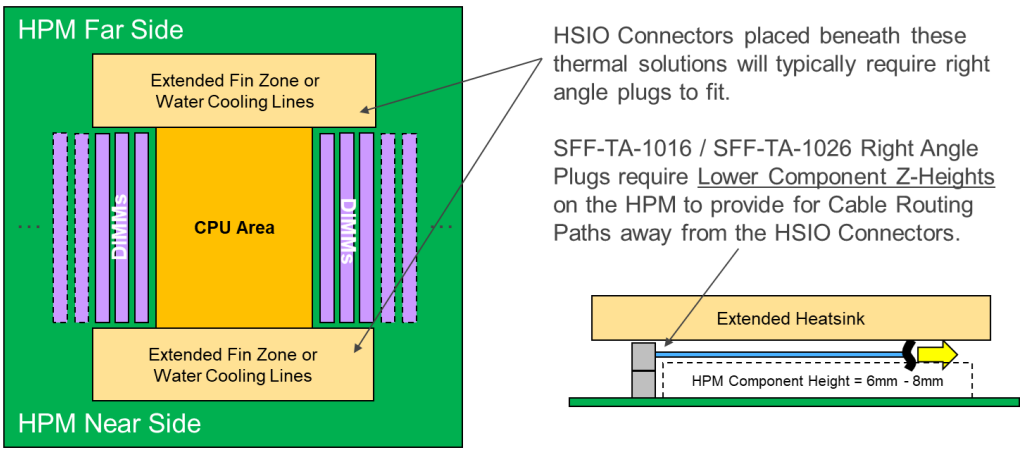
1. Increasing Near Side to Far Side power delivery and power egress capability to mitigate loss of power cabling

2. Identify available cabling space for High-Speed IO to meet a given platform configuration.

3. Adjusting DIMM pitch to enable cables should be considered.

Implementation Note:

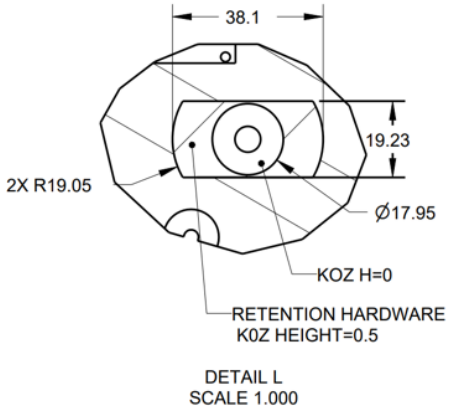
HPM designers must take care with component placements relative to cabled HSIO Connectors. Placements should allow for cable routing strategies beneath the defined 12mm maximum component height. Failure to do so will limit potential system intercepts for the HPM.



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Implementors Note:

The wide shaped 0.5mm Height Restriction in **Figure 18. Zones for Primary Side Component Height Restrictions**, Detail L, is in place for finger grip allowances around the retention hardware (which could be a plunger, thumbscrew, wing screw, etc). Due to hardware and touchpoints being in this area, the goal is to minimize the size of components that could potentially be damaged by fingers coming in close contact to the board surface.

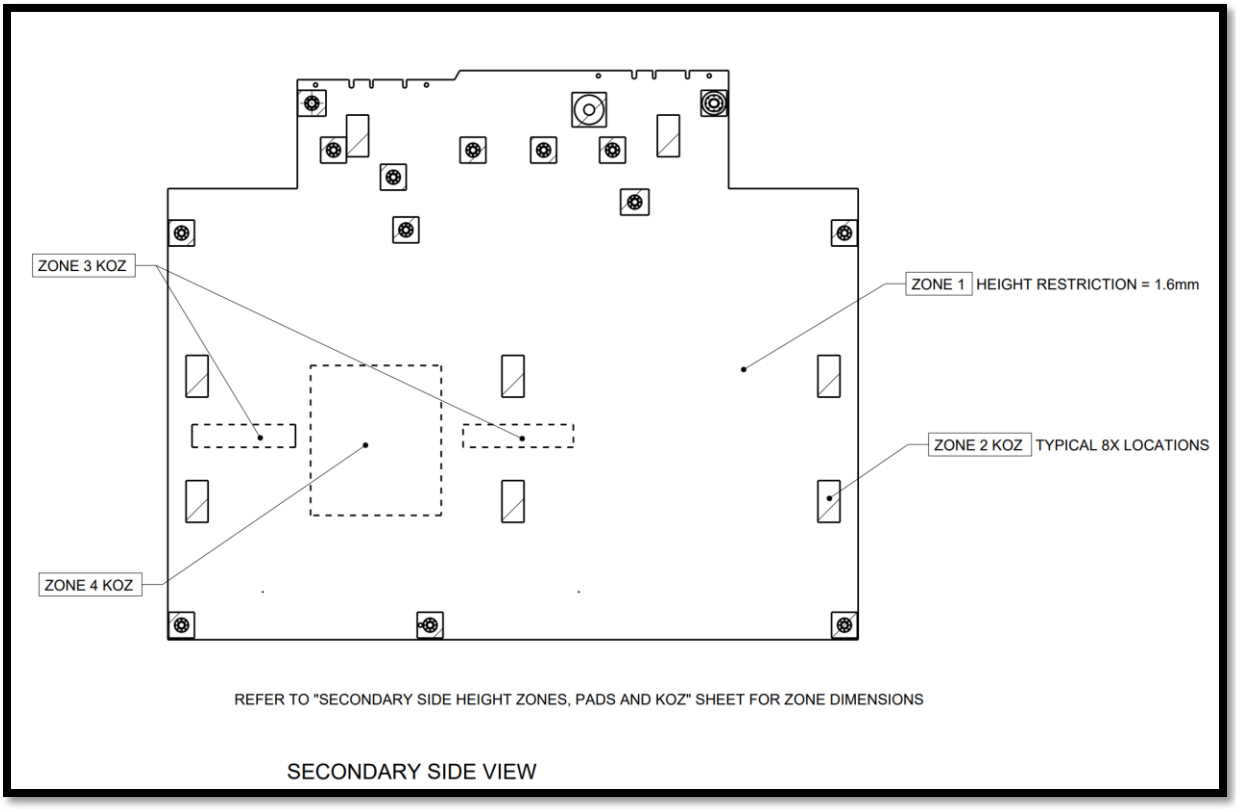




10.14. Secondary Side Zones and Height Restrictions

There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 19**. Each zone serves a unique purpose, defined in the following sections. Zones 1, 2, 3 and 4 are defined as requirements for compliance.

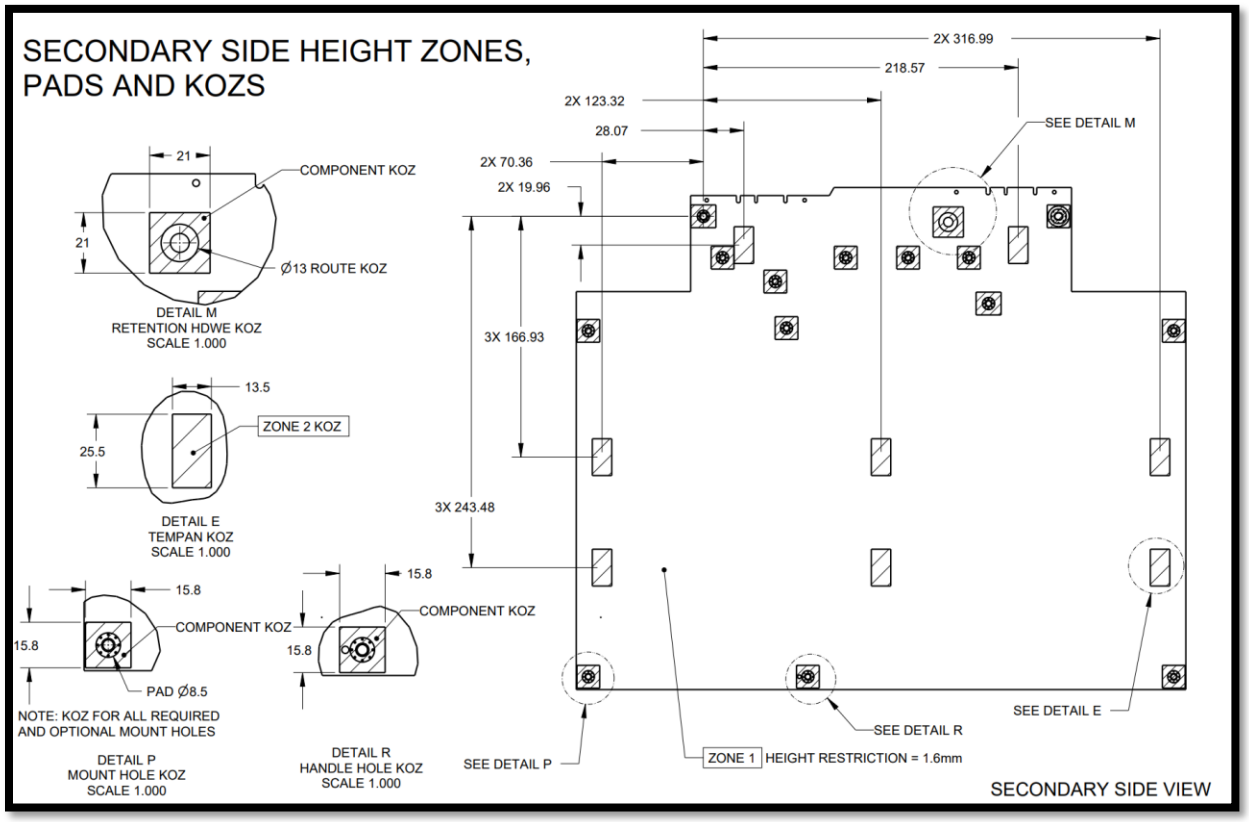
Figure 19: Secondary Side Height Restriction Zone and KOZ Definitions



10.14.1. Zone 1, Secondary Side Height Restriction

Zone 1 universally applies to the entire secondary side of the HPM, except for the defined Zones 2, 3, and 4. HPM electrical components are expected to utilize Zone 1. Zone 1 shall have a universal height restriction of 1.6 mm (exceptions noted in specification), per **Figure 20**. This is to ensure HPM component clearances to chassis base or board pan structure. This is especially important with a max allowable board thickness defined in **Section 10.15 HPM Board Thickness.**

Figure 20. HPM Secondary Side Height Keepout Zones, Pads, KOZ



10.14.2. Zone 1 Exceptions for Secondary Side Tall Component

In some instances, an HPM Designer or System Designer, may desire tall secondary side components (such as special capacitors) that exceed the secondary side height restriction. Although this should be avoided, a HPM Designer may implement local exceptions if the following conditions can be met:

1. For the Zone 1 Exceptions (to Secondary Side Tall Components), HPM thickness + Secondary side components shall not exceed 5.66mm nominal.

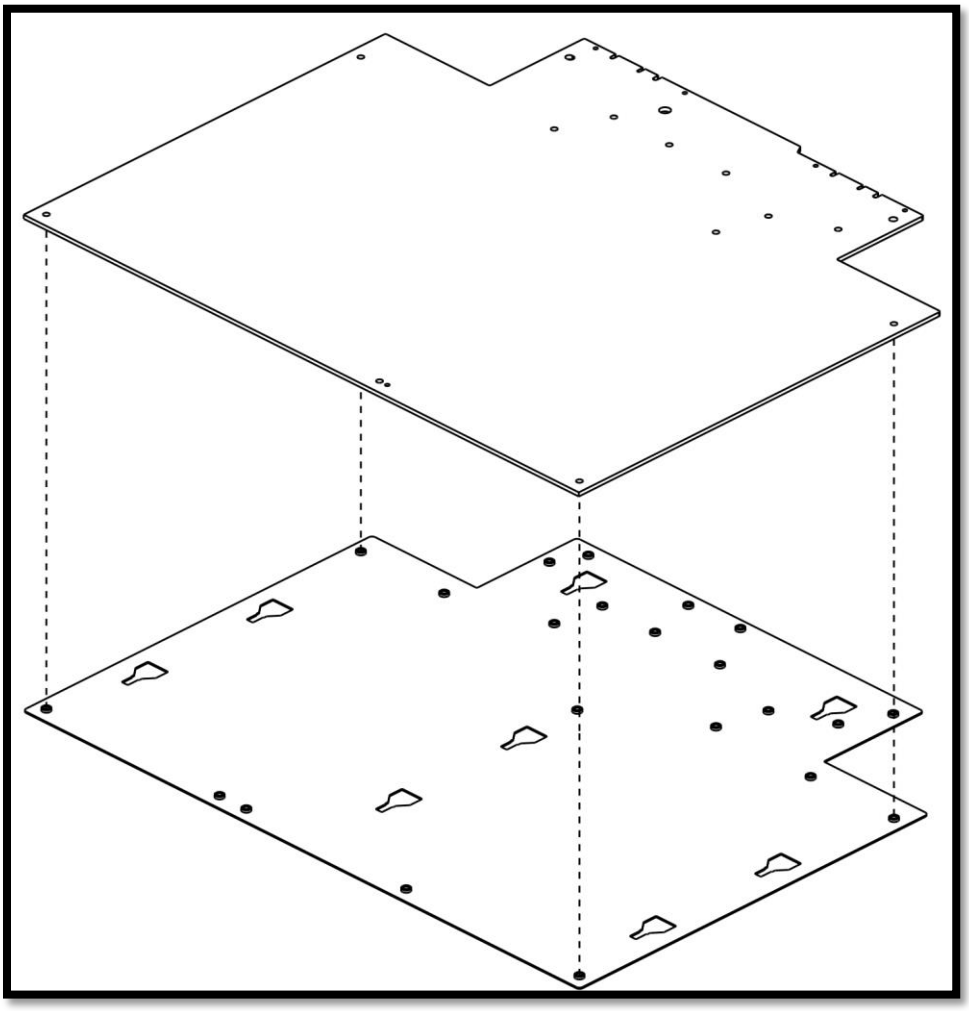
- Allowing for +/- 0.2 mm HPM mounting height tolerance in an assumed 5.86 HPM mounting height).

2. Exceptions are contained to small areas of the secondary side and shall not to exceed 400mm^2 area per instance.
3. No two instances of a secondary side exception shall be closer than 10mm, as to not drive excess cutouts in Chassis-to-HPM bracketry
4. The Chassis-to-HPM bracketry can be cutout to accommodate these exceptions.

10.14.3. Zone 2, Chassis-to-HPM Bracket (Board Pan) KOZ Requirements

The M-FLW HPM shall be designed to fit a Chassis-to-HPM Bracket (Board Pan) that enables different board layouts and mounting hole locations between different Compute Core designs while still maintaining compatibility to a common chassis design. Example shown in **Figure 21**.

Figure 21. Example of Chassis-to-HPM Bracket (Board Pan)



There will be fixed chassis hooks interfacing to the chassis-to-HPM bracket that require the Zone 2 zero height KOZ on HPM Secondary side. There shall be eight Zone 2 (0-height) KOZs implemented as defined in **Figure 20. HPM Secondary Side Height Keepout Zones, Pads, KOZ.**

For an example of chassis hook concept, see **Section 14.7**. The geometry of the chassis hook is not specified and is a design choice for System Designer.

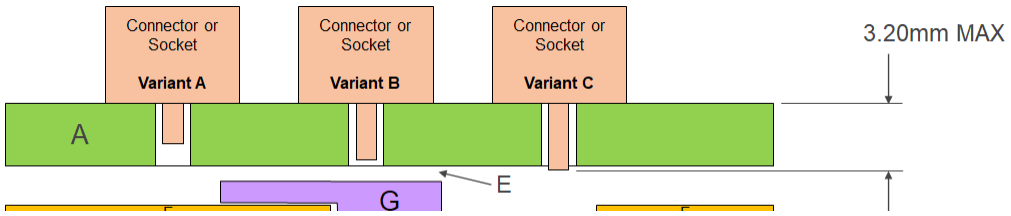
Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb shall be 3.20mm MAX.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout

Implementors Note:

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly. Refer to **Table 4. Example Z-Height Compliant Stack-Up, Per Zone** for definition of 'A', 'E', 'F' and 'G' the diagram.



10.14.4. Zone 3, HPM Secondary Support Requirements

To ensure maximum flexibility of HPM primary side layouts, secondary supports need to be incorporated under the DIMM Sockets and / or any other area of the HPM needing extra vertical compression support. These supports help prevent the board from flexing during assembly, when downward forces are applied to the HPM from the primary side.

The HPM shall Implement Zone 3 KOZs near or under DIMM sockets. The size, location and quantity is not defined and left to HPM designer.

The HPM shall provide Secondary Supports that attach in Zone 3, which are 1.78mm +/- 0.10mm thick. They are designed to be close to the board pan or chassis, and provide a vertical deflection stop for the HPM. The materials used and methods for support are the choice of the HPM Designer. This support height creates a common reference surface that Chassis Designers can rely on that is taller than the Secondary Component Z-Height MAX of 1.6mm.

Implementors Note:

If an HPM Designer and a Chassis Designer agree to transfer this responsibility for HPM support, and the HPM Designer provides all the appropriate PCB keepouts and guidance necessary to relocate these supports into the chassis design, then it will be permissible to remove these supplemental supports from the finished HPM PCB assembly.

10.14.5. Zone 4, CPU Backing Plate Requirement and Examples

The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by:

1. Backing Plate allowed Height = 5.86mm – HPM thickness - 0.08mm standoff height tolerance – allowances for other backplate design requirements (insulators, deflections, etc)
2. See Implementors Note below for examples.

Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and/or HPM sled as represented by area ‘C’ in **Figure 25 CPU Backing Plate (Zone 4).**

Implementors Note:

HPM and CPU designers should consider these example Scenarios supported by DC-MHS HPM and Backing plate thickness requirements.

Board Thickness (Nominal, mm)	Maximum Allowable CPU Backing Plate Assembly Thickness (mm)
1.57	4.21
1.93	3.85
2.36	3.42
2.55	3.23
3.18	2.60

10.15. HPM Board Thickness

- The maximum allowed thickness and zone heights in the specification assume a minimum 5.86mm board mounting height.
    - Thickness and zone heights are established to ensure forward compatibility with 1U & 2U System Chassis assumptions.
    - Exceeding the thickness and zone height target values would result in system design impacts and incompatibilities
    - The board mounting height for a given system is not within scope of HPM specification and is at discretion of the System designer.
- The maximum allowed HPM thickness is 3.18mm nominal and assume +/-10% tolerance is allowed.
    - Note that PCB Tolerances of +/- 10% are supported but are not a factor in determining the fit of the CPU Backing Plate when the HPMs are mounted to standoffs by their bottom surfaces.

Implementors Note:

HPM and Chassis designers should consider the height stack-up of each of the four zones identified in **Section 10.14**. **Table 4** and **Figure 22 - Figure 25** demonstrate an example of a compliant stack-up for consideration. Note that the "total Z" value across the four zones must always be equivalent (5.86mm shown for example only).

Table 4. Example Z-Height Compliant Stack-Up, Per Zone

		Zone 1	Zone 2	Zone 3	Zone 4	
Item	Description	Z Value (mm)	Z Value (mm)	Z Value (mm)	Z Value (mm)	Notes
A	HPM	3.18	3.18	3.18	3.18	MAX Thickness (w/o Added tolerance, Assumes bottom mounting)
B	Bottom Component Z	1.60	0			MAX Height
C	CPU Backing Plate				2.60	MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray
D	HPM Bottom Support			1.78		HPM Support Thickness +/- 0.10mm, must exceed Bottom Component Z
E(1)	Needed Gap	0.28	0.58			Gap is Larger, Requires Insulation and/or Clearance
E(2)	Resultant Gap			0.10	0.08	Gap is Small, Contact between Parts is either Desired or Permissible
F	Board Pan	0.80		0.80		
G	Chassis Hook		2.10			MAX Height from Inside Surface of Chassis
	TOTAL	5.86	5.86	5.86	5.86	Example Solution Stack-up

Figure 22: Secondary Side Components (Zone 1)

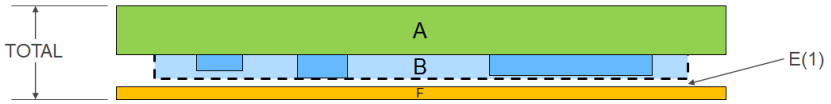


Figure 23: Chassis Hook Keepouts (Zone 2)



Figure 24: HPM Secondary Support (Zone 3)

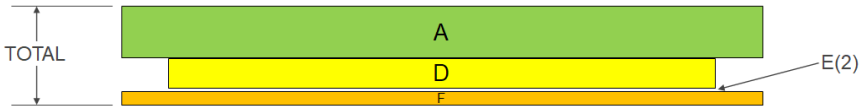
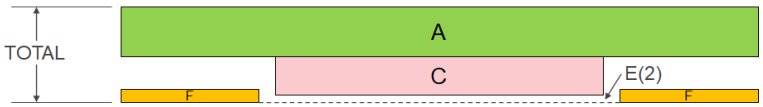


Figure 25: CPU Backing Plate (Zone 4)



Implementors Note:

Designers should consider that variations in HPM thickness can result in variation of the offset locations of OCP NIC R3.0 and DC-SCM R2.0 peripherals (relative to fixed chassis openings).

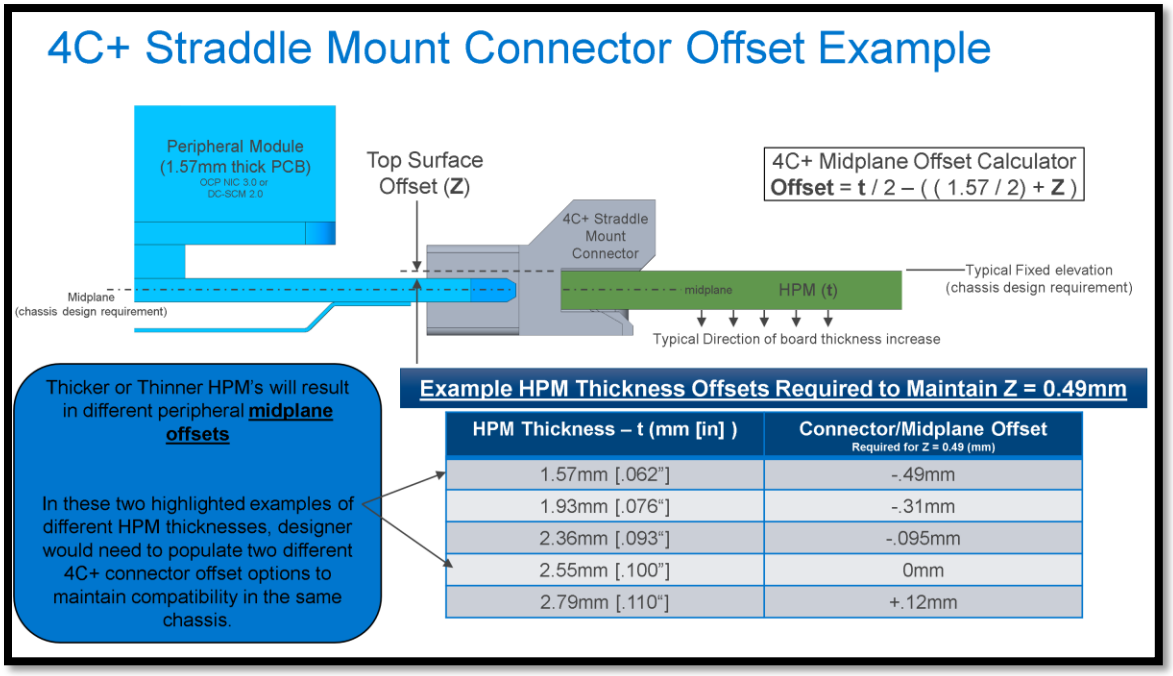
A common chassis design intended to support two different thickness HPMs may have to populate different 4C+ connector offsets.

Designers may consult with vendors of SFF-TA-1002 4c+ to determine best options for their chassis application. See

Figure 26. HPM thickness and Straddle Mount Peripheral Offsets below.

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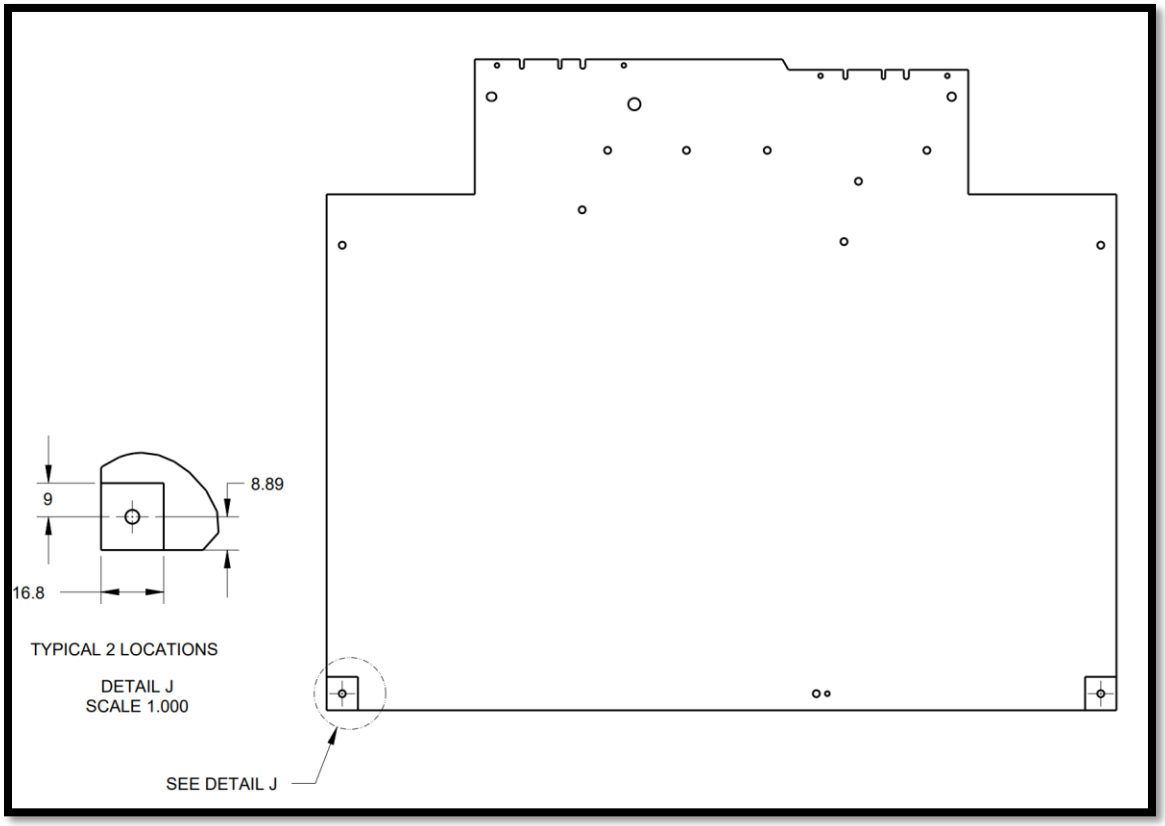
Figure 26. HPM thickness and Straddle Mount Peripheral Offsets



10.16. Thermal Solution Bracketry Keepout Zones

There shall be keepouts around the Far Side HPM mounting holes to enable bracket mounting to the HPM, as detailed in **Figure 27**. These brackets may be needed for systems that wish to mount liquid cooling components, such as DIMM liquid manifolds, or large radiator assemblies.

Figure 27. Thermal Solution Bracket Keepouts



11. HPM Power Zones

The M-FLW HPM is powered from a 12V DC source. This Base Specification does not cover alternate PSU voltage sources (e.g., 48V DC). The HPM supports multiple power zones where significant power delivery and connectivity is expected. **Figure 28** illustrates locations of power zones on the HPM. Details of each zone are described below, some are ingress, some are egress from the HPM. Designers should use this guidance in design of HPM Power planes.

Implementors Note:

The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in private and/or public HPM design specification(s) for system configurations supported per HPM design

Figure 28. HPM Power Zone locations

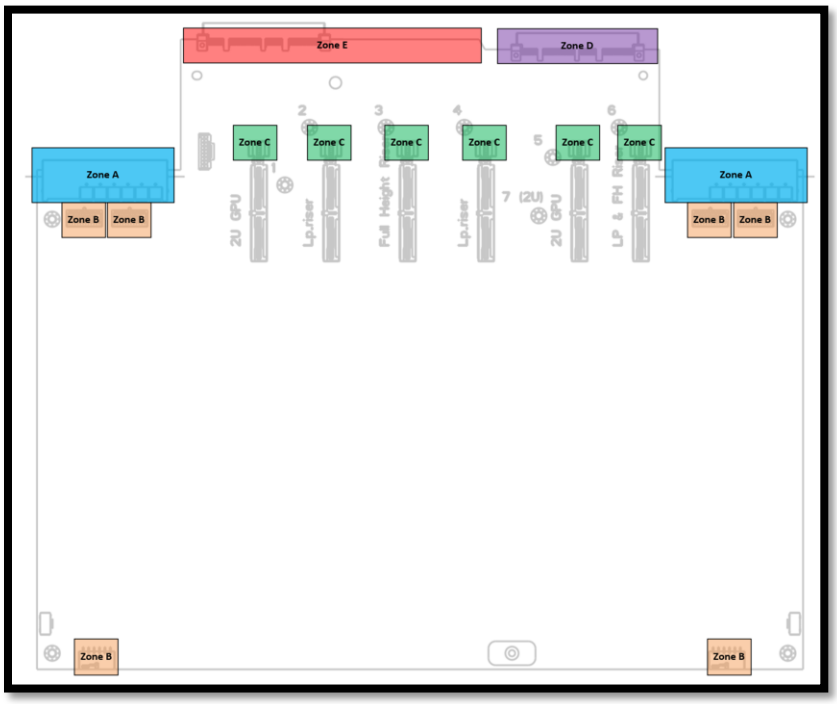


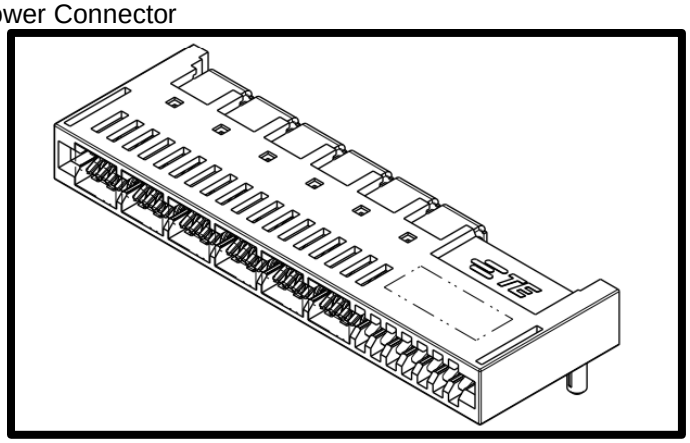
Table 5. Power Delivery Zones

Zone	Feature	Typical Usage	Zone Power Rating
Zone A	M-CRPS Connector	Ingress	up to 3200W
Zone B	2x6+12s PICPWR	Egress	up to 864W
Zone C	Near Side Riser PICPWR	Egress	up to 252W per Near IO Connector populated
Zone D	DC-SCM R2.0	Egress	up to 50W
Zone E	OCP NIC R3.0 + Platform Custom Zone	Egress	up to 160W

11.1. Zone A: M-CRPS Connector(s)

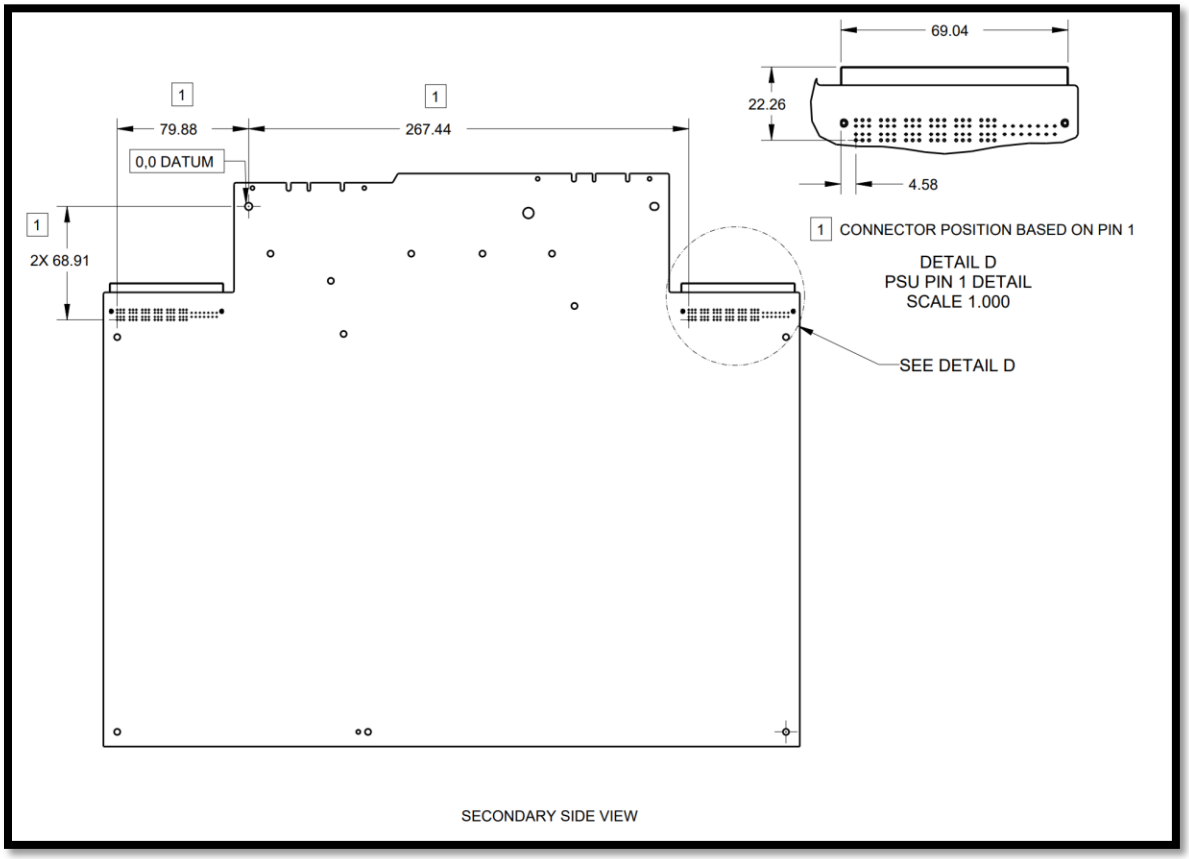
- Connector Power Rating: 3200W
- Typical usage: Power ingress
- Refer to M-PIC and M-CRPS Specification(s) for additional implementation details.

Figure 29. M-CRPS Power Connector



Locations of M-CRPS connectors shall be placed as defined in **Figure 30**

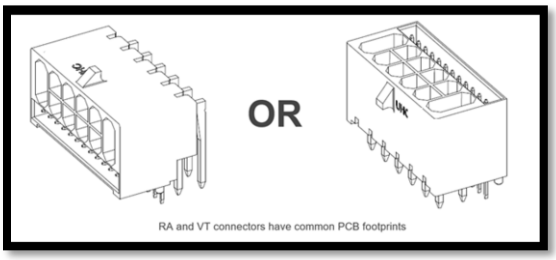
Figure 30. M-CRPS Connector Location Requirements



11.2. Zone B: PICPWR Connector(s)

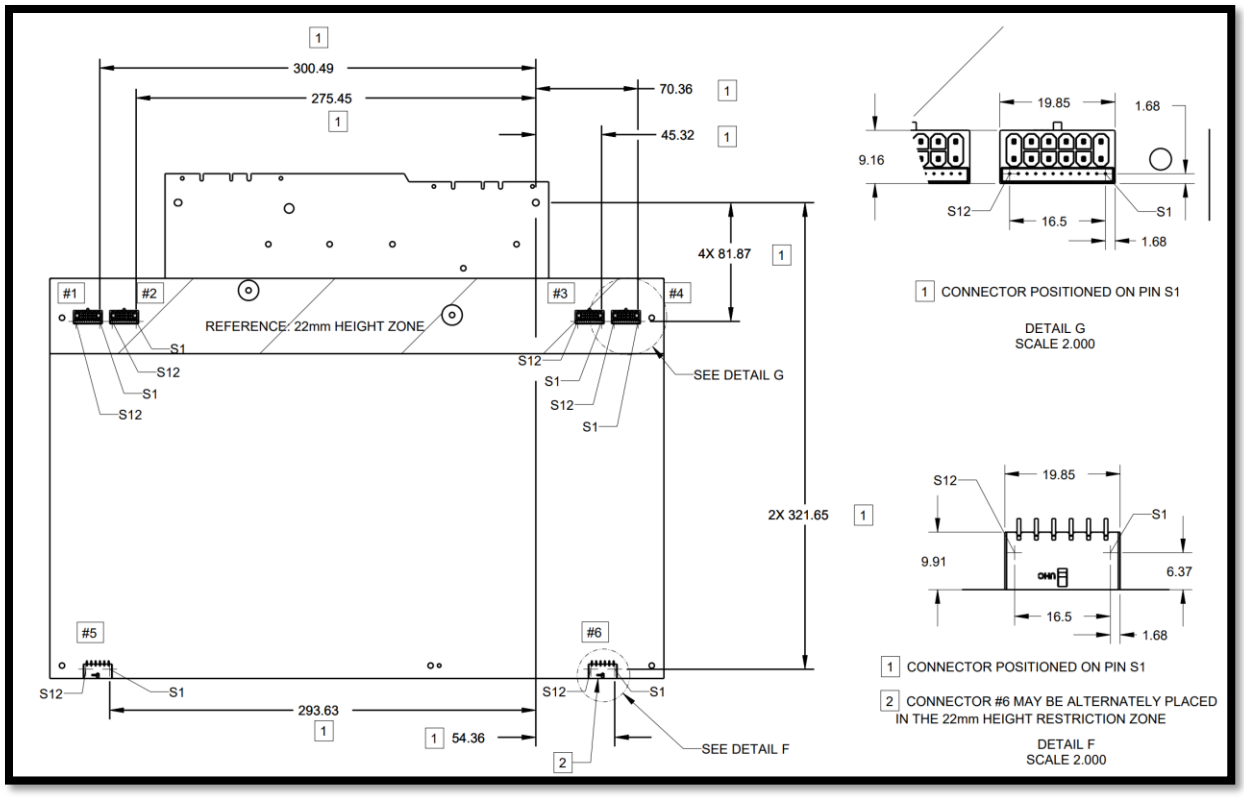
- Connector Power Rating: 864W
- Typical usage: Power egress to peripherals, Power Ingress from PDB
- Refer to M-PIC Specification for additional details
- Far Side PIC PWR may be either Vertical or Right Angle, the connector has common footprints.
- Note, Near Side PIC PWR should be vertical connector only

Figure 31. 2x6+12s PICPWR Power Connectors



<u>The HPM shall implement 6x PICPWR connectors at locations defined in **Figure 32**.</u> Note: HPM shall implement these connector footprints (but can be depopulated in assembly BOM with Design Spec guidance.) Note that connector #6 location may optionally be changed to reside in the 22mm Height restriction zone.

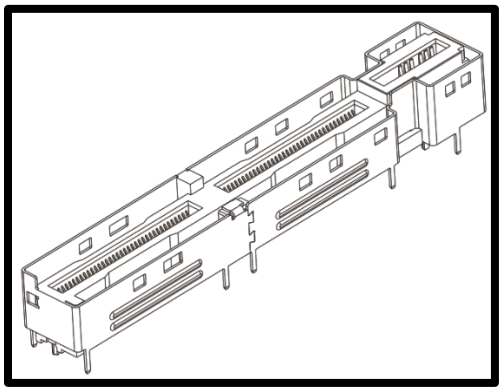
Figure 32 PICPWR connector (2x6+12s) Location Requirement (6 locations)



11.3. Zone C: SFF-TA-1033 Connectors w/ PICPWR

- Connector Power Rating: 252W
- Typical usage: Power egress for up to 3x 75W CEM PCIe devices
- Refer to M-PIC Specification for additional details.
- Refer to **Section 10.11 Near Side IO Connectors** for additional details on Near Side connector and location.

Figure 33. SFF-TA-1033 Connector



The Egress Near Side Riser Power Zone provides power to PCIe devices on risers. This specification does not cover direct dock CEM implementation (non-riser approach). The HPM provides 12V_PRIMARY[1] to the Egress Near Riser Power Zone.

75W Slot power, detailed in **Table 6**, is provided for each PCIe CEM slot on all PCIe risers. The PCIe riser enables a +3.3Vaux and +3.3V (Vcc3_3) power sources derived from the 12V_PRIMARY source from the HPM

Table 6. Minimum HPM Power Supply Rail Requirements per PCIe CEM Slot

Power Rail	75 W Slot[2]
+3.3Vaux	Generated on PCIe riser. Derived from 12V_PRIMARY
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from 12V_PRIMARY
12V_PRIMARY Voltage Current	12V nominal 7.25A total: 5.5 A (CEM 5.0) + ~1.0A (VR conversion to V_{cc3_3}) + ~0.35A (VR conversion to +3.3Vaux) + ~0.40A (misc.)

Note 1: see M-PIC specification for definition of 12V_PRIMARY

Note 2: Additional power is provided to each CEM slot beyond PCIe CEM 5.0 specification to budget for miscellaneous logic on risers and VR conversion losses. Effective total power is 87W per slot.

11.4. Zone D: DC-SCM R2.0 Connector

- Connector Type: See OCP DC-SCM R2.0 specification
- Connector Power Rating: 50W (Refer to the OCP DC-SCM R2.0 specification)

11.5. Zone E: NIC 3.0 and Platform Customization Zone Connector(s)

- Power Connector Type: See OCP NIC R3.0 specification and Platform Custom Zone
- Connector(s) Power Rating: 160W (combination OCP NIC R3 and Platform Custom Zone)
- This is a maximum number, the connectors OCP NIC R3 and Platform Custom Zone choice may not consume maximum power.

12. I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces (connectors) that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details, specifically M-PIC, M-XIO, M-CRPS, and M-PESTI specifications.

HPM shall implement battery backed voltage interface per DC-SCM R2.0 "Battery Voltage" requirement.

13. References

Relevant Open Compute Specifications

This specification also relies on the following Open Compute Project specifications

OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
Mezz (NIC) » Open Compute Project

OCP Datacenter Secure Control Module (DC-SCM) 2.0 – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
Hardware Management/Hardware Management Module - OpenCompute

Additional Industry References

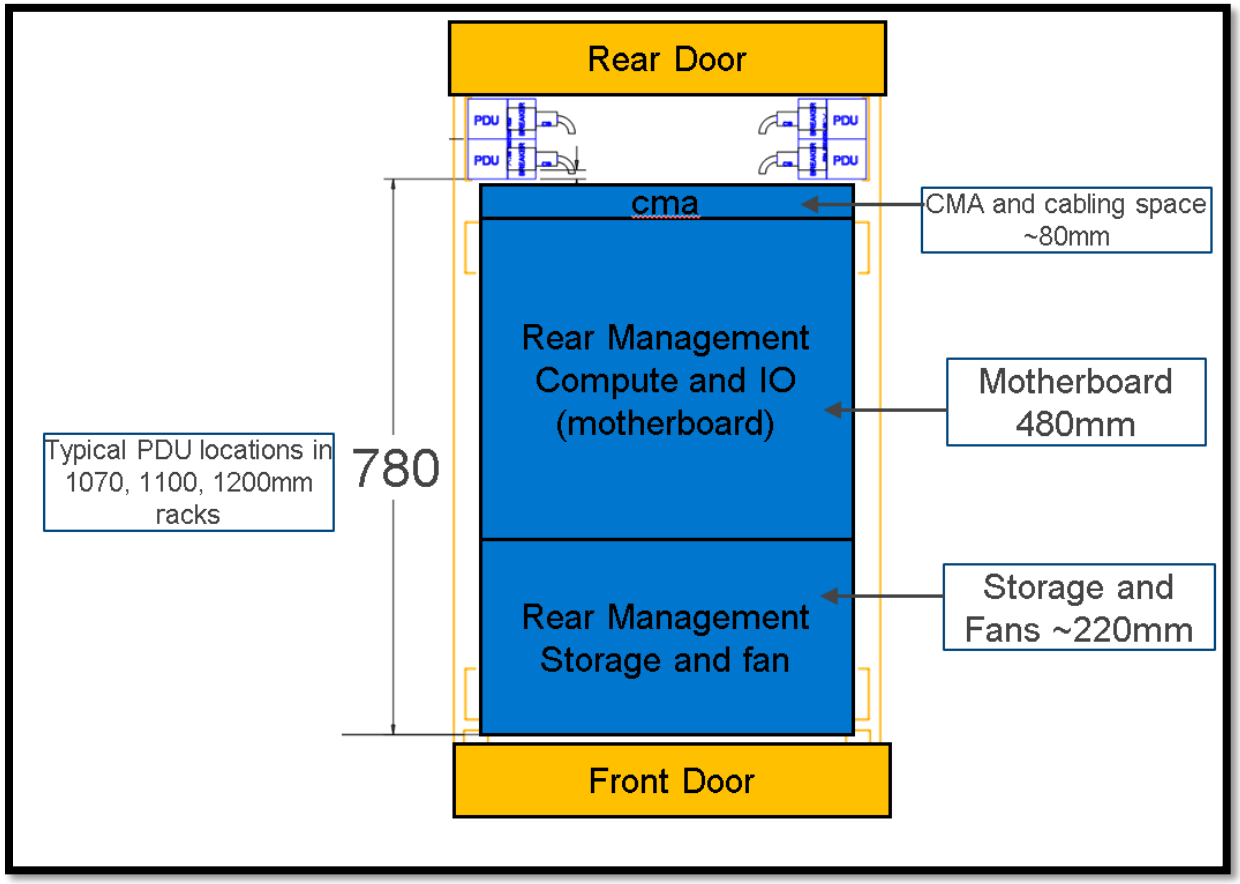
- ASMEY14.5 – 2018 Dimensioning and Tolerancing
- Open Rack V3 (Base Specification)
- SNIA SFF-TA-1002
- SNIA SFF-TA-1016
- SNIA SFF-TA-1026

14. Supplemental Information

14.1. Rack and Chassis Depth Stackup Assumptions

The M-FLW HPM Base Specification is constructed under the considerations that the installation environment has a Power Distribution Unit approximately 780mm from the front EIA flange. Although platforms may vary in depth, the board size constraint is chosen to enable typical chassis storage systems using this M-FLW HPM spec to fit with a Cable Management arm in less than the 780mm PDU constraint.

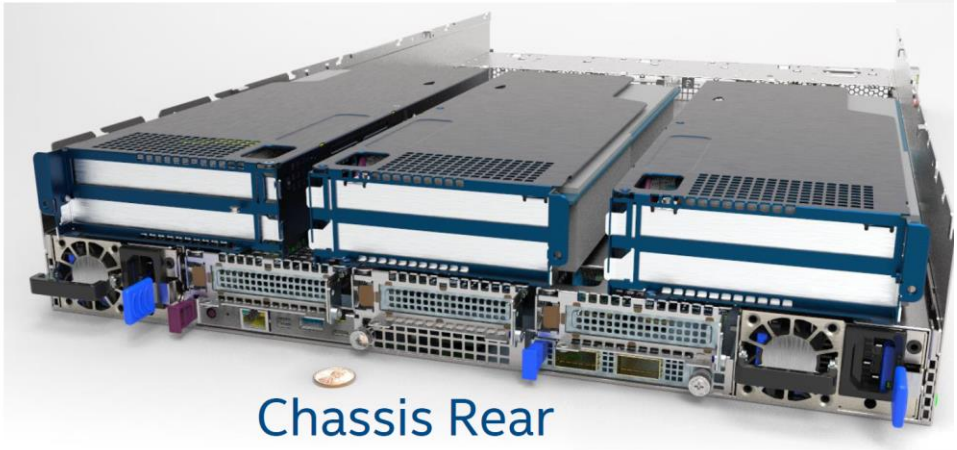
Figure 34. Rack Depth Constraints

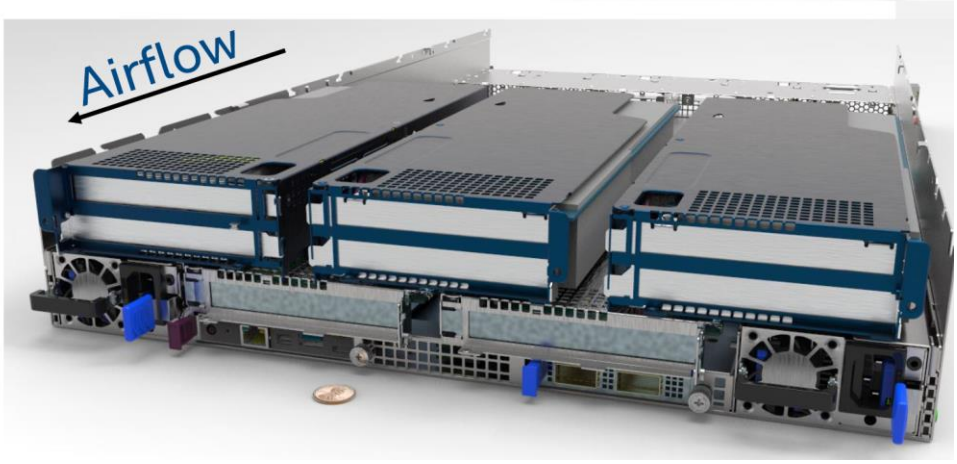


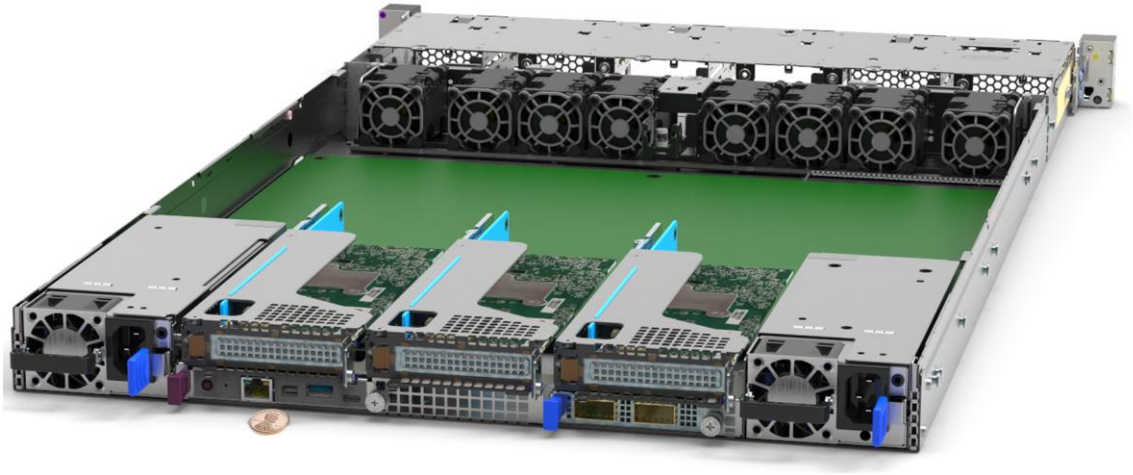
14.2. Example 1U and 2U PCIe Slot Typical Configurations

The following images in **Figure 35** are some example representations of typical Enterprise 1U and 2U PCIe Slot Configurations.

Figure 35. Examples of Typical 1U / 2U PCIe Slot Configs for Rear Management System

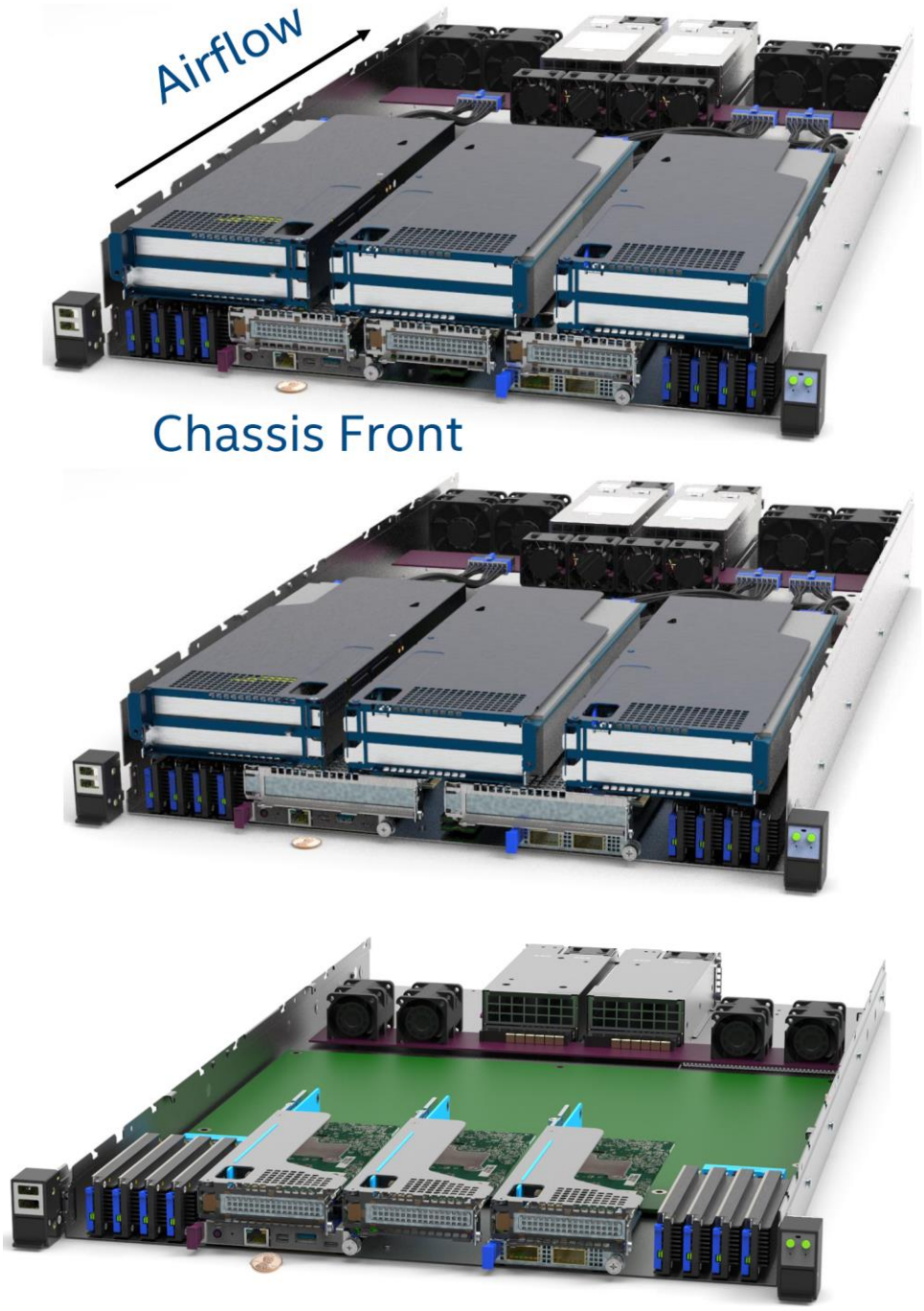






The following images in **Figure 36** are of typical Hyperscale 1U and 2U PCIe Slot Configurations. Note, these are 19" FrontIO chassis like OCP Project Olympus. Also, the front can be shuffled around using an extra "adapter board" like **Figure 40. Base Outline HPM used in an Example 21"** Reference Chassis is not covered by the M-FLW HPM spec.

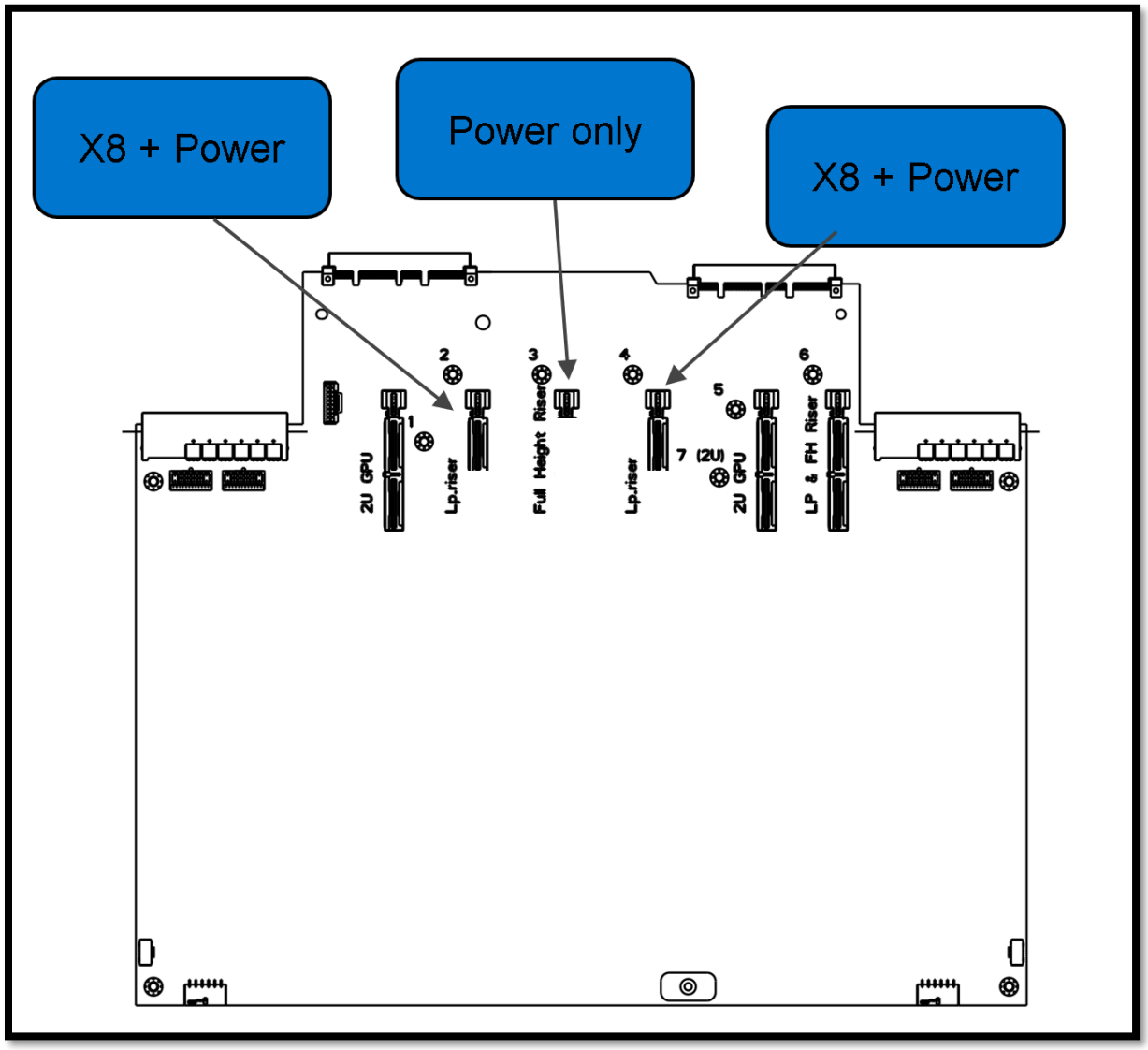
Figure 36. Examples of Typical 1U / 2U PCIe Slot Configs for Front Management System



14.3. Example Scenario for Near IO Population with less than 6x16 ports

Certain Compute Cores may not have 6x16 ports to assign to all six Near IO positions. The HPM Designer may elect to follow the rules shown in **Section 10.11.1 Location of Near Side M-XIO Connectors.** An example of this is shown below in **Figure 37**. HSIO might be cabled into the riser, but the riser still has the PICPWR portion of the connector for PCB applications. Refer to **Figure 37** which defines Datum M and Datum K position of all 3 connector variants.

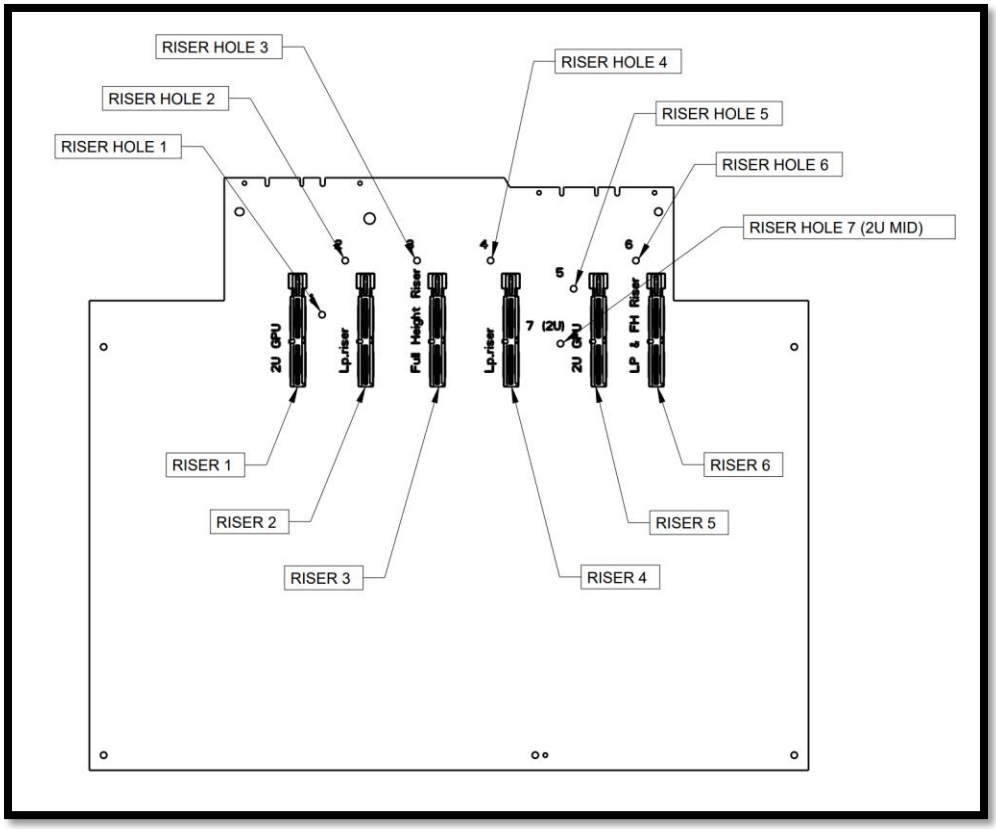
Figure 37. Example Near IO Connector Population Scenario



14.4. Additional Information on Near IO Riser Retention Holes

920 In a system configuration that uses riser cards in the Near IO, mechanical retention is enabled by holes in the HPM near each Near IO location. The following **Figure 38** demonstrates the riser retention holes and which Near IO position each hole is associated with.

Figure 38. Riser Retention Holes and Associated Near XIO Locations

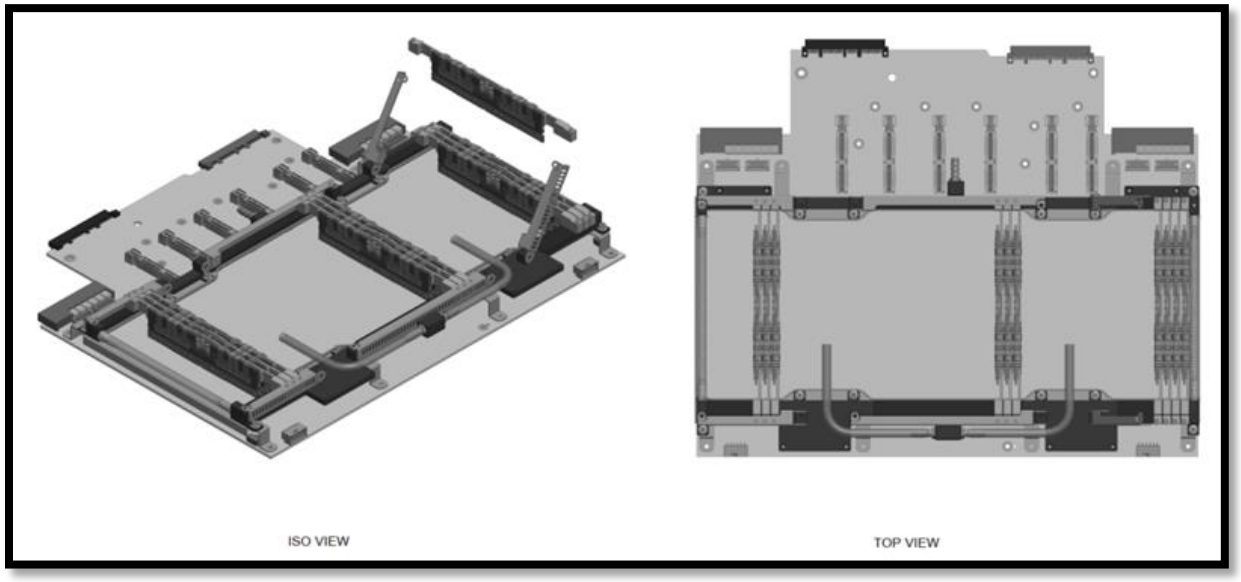


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14.5. Example Liquid Cooling Implementation in 1U M-FLW application

Figure 39 demonstrates an example implementation of a M-FLW Liquid Cooling solution w/ 10 DIMMs shown. Considerations should be made for CPU and DIMM locations not detailed in the M-FLW Base Specification. Example Liquid Cooling structure attaches to Far side mounting holes shown in **Figure 27. Thermal Solution Bracket Keepouts** and **Figure 20. HPM Secondary Side Height Keepout Zones, Pads, KOZ**. It also complies with **Figure 18. Zones for Primary Side Component Height Restrictions.**

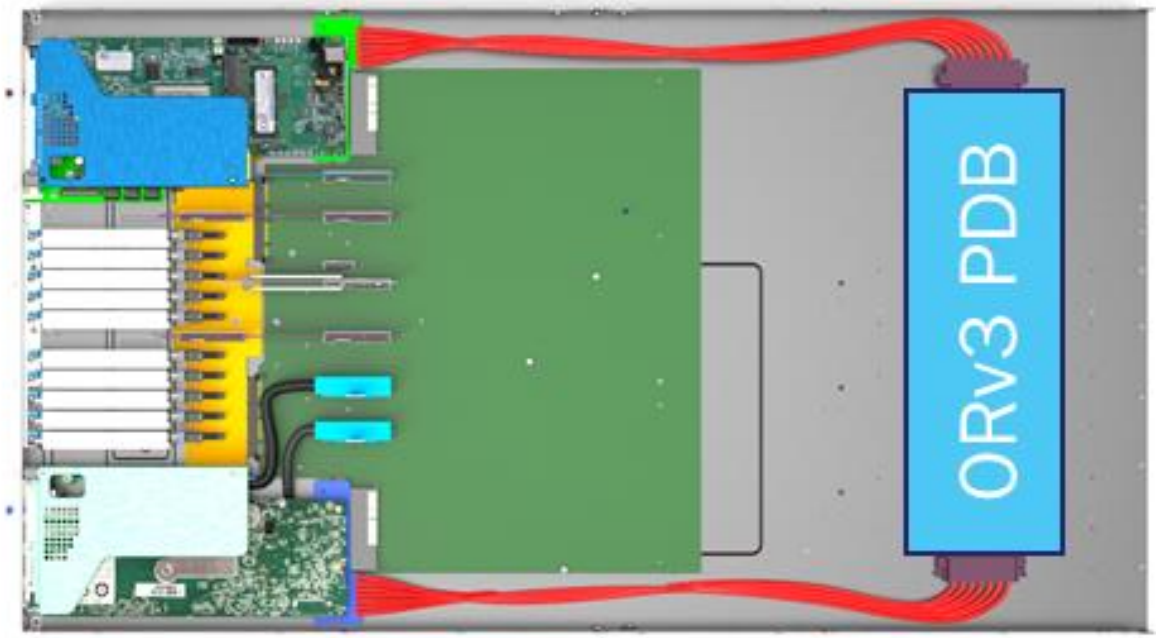
Figure 39. M-FLW 1U Liquid Cooling Example Implementation



14.6. Example/Reference System Architecture in 21” Chassis

Figure 40 shows how the Base Outline HPM can be utilized in a 21” chassis architecture, including if Power Supply Infrastructure is on the Far Side with cables to the near side power ingress.

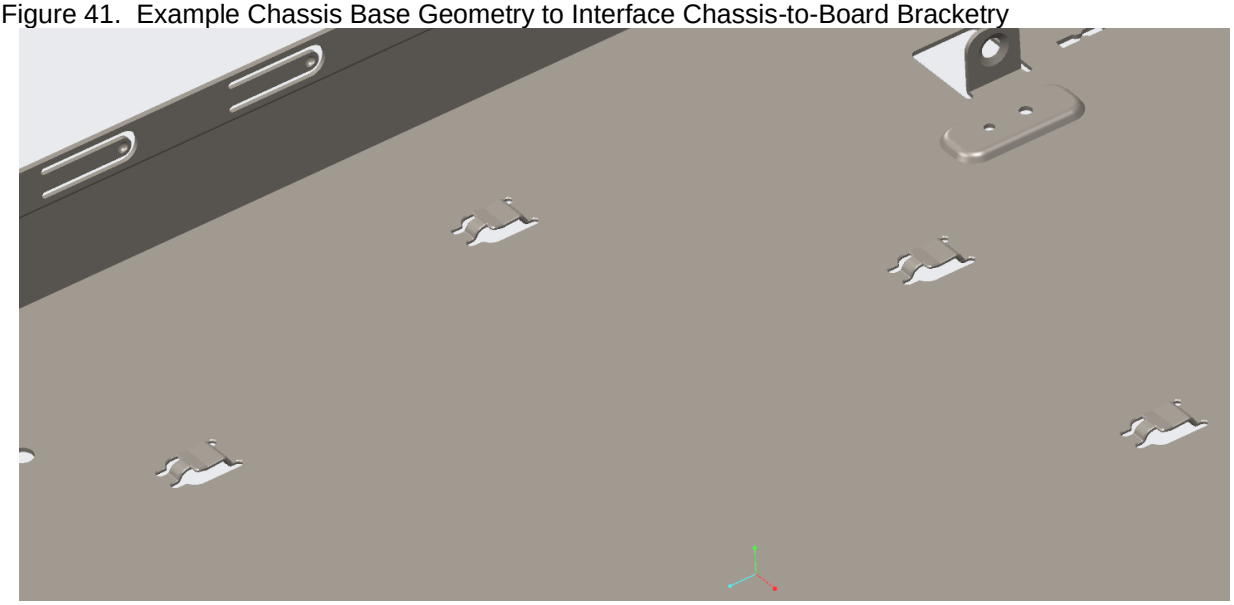
Figure 40. Base Outline HPM used in an Example 21" Reference Chassis



14.7. Example Chassis Base Geometry for Chassis-to-Board Bracket interface

Figure 41 demonstrates example geometry required in the chassis base to interface to the Chassis-to-HPM bracketry in **Figure 21. Example of Chassis-to-HPM Bracket (Board Pan).** The exact geometry is not specified, but considerations must be made for maximum board thickness (see **Section 10.15 HPM Board Thickness**) and HPM Keepout Zone sizes (See **Section 10.3.1 Keepout Zone for Retention Hardware**).

Figure 41. Example Chassis Base Geometry to Interface Chassis-to-Board Bracketry



14.8. HPM with Far Side Panel Mount IO (FSPM) Requirements

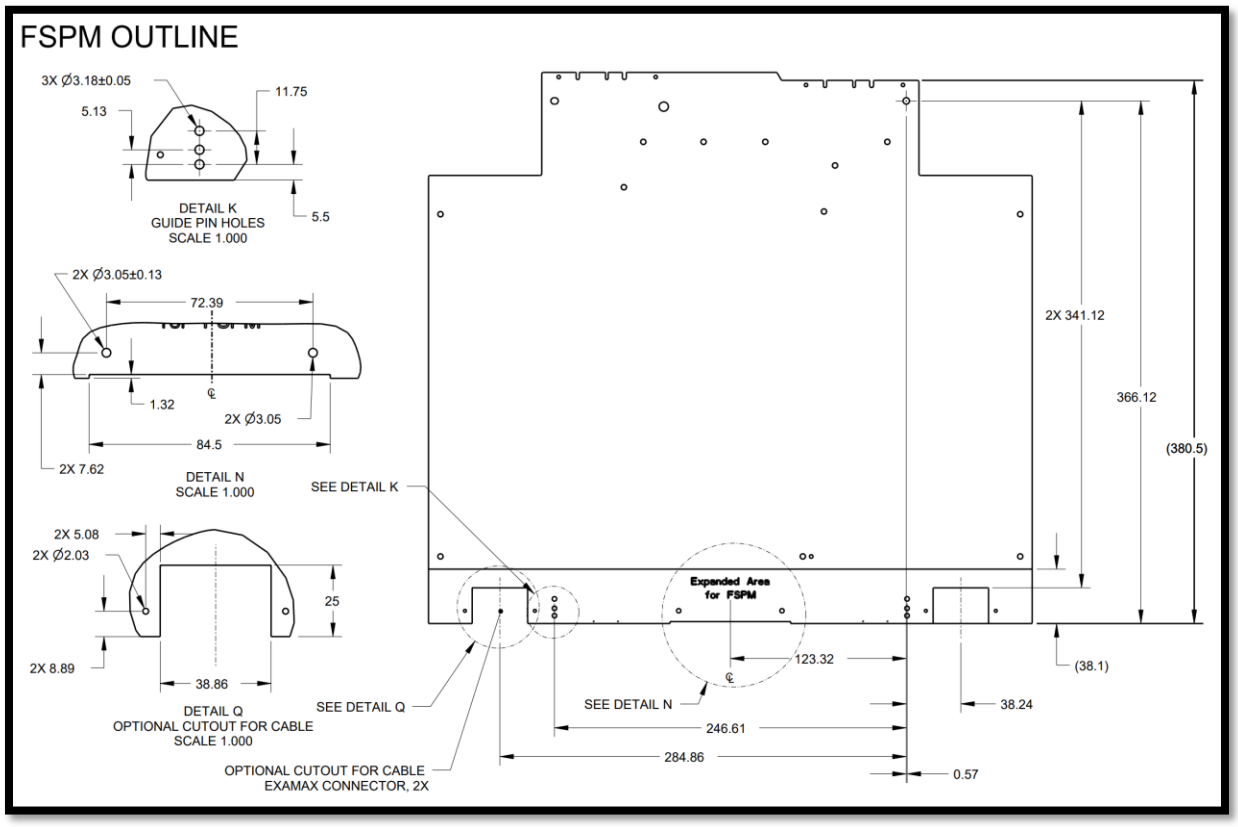
Readers Note: This Section represents a Future M-FLW Type. For this Version of M-FLW, we will abbreviate this HPM type as the FSPM (Far Side Panel Mount) HPM. This informative section will go into the normative section of the M-FLW specification once the FSPM target interfaces are released.

The FSPM HPM architecture leverages the base HPM specifications. FSPM Adaptation or Type has differences from the Type 1 Base Spec, which are focused on the Far Side area to optimize Power Delivery and IO connections that are part of a Front Panel IO or Blade implementation. A FSPM implementation must implement blind-mate panel mountable connectors in the specified locations as described in **Figure 42**

14.8.1. FSPM HPM Outline

FSPM HPM Outline is an extension of the base outline listed in **Section 10 Mechanical Requirements** and must match the specified dimensions with exception of Far Side growth. The Far Side dimension of the base outline is extended by 38.11mm [1.5”] to accommodate blind mate IO connectors, power connector, and blind-mate guide pins to achieve reliable docking with panel-mount connections.

Figure 42. Full Width HPM Outline Modifications for Far Side Panel Mount



14.8.2. Blade High Speed IO connector

High Speed IO connector outlines shown in **Figure 42. Full Width HPM Outline Modifications for Far Side Panel Mount** are based on the Amphenol ExaMAX family (or equivalent) series.

There are seven 4x8 ExaMAX shown from left to right. In addition, there is one 6x8 ExaMAX in the far-right position that is intended to include extra clock and management signals.

The position of these connectors must align to the indicated positions, but any of the connectors may be depopulated if not used. However, both guide pin receptacles **must** always be included for mechanical robustness during blind-mate insertion. The pin-out for the connectors must adhere to the definitions defined in the M-XIO specification.

Table 7. Blade Far/South High-Speed IO Recommended Connectors

Connector family	**Company**	**Configuration**
ExaMAX / ExaMAX 2	Amphenol or Equivalent	4 pairs X 8 columns
ExaMAX / ExaMAX 2	Amphenol or Equivalent	6 pairs X 8 columns

Figure 43. ExaMAX 4x8 connector used in FSPM

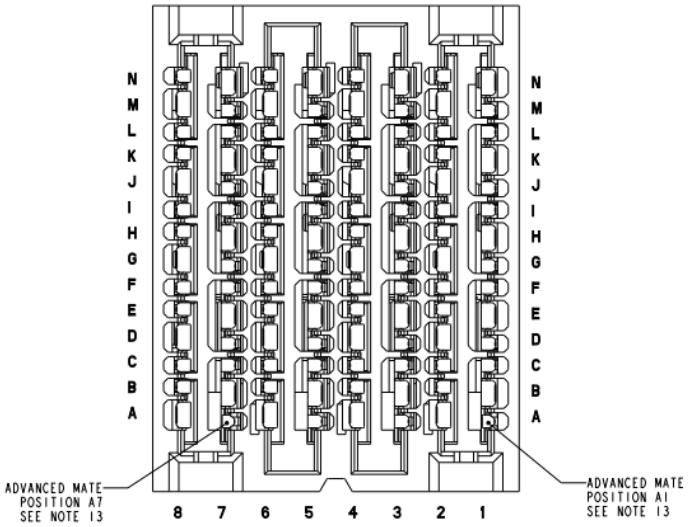
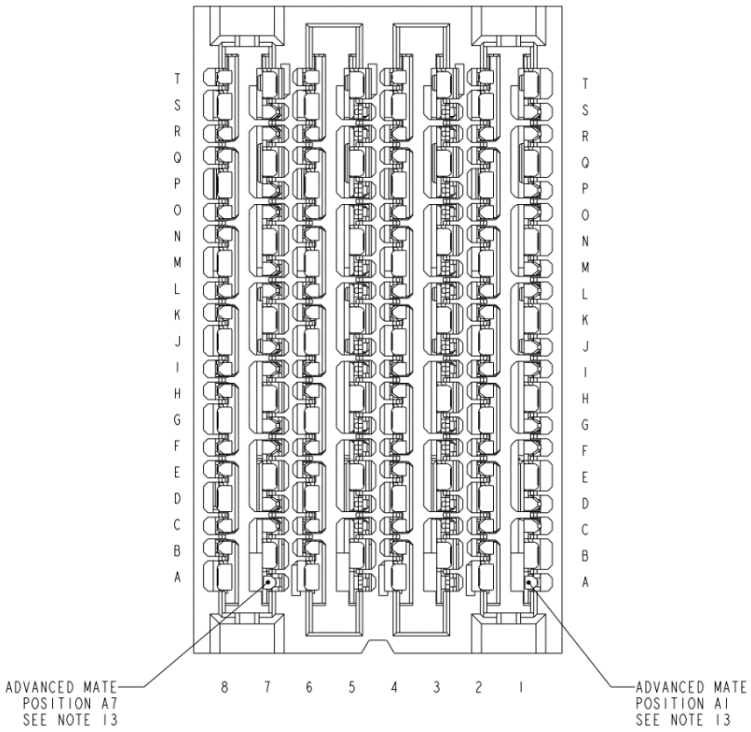


Figure 44. ExaMAX 6x8 connector used in FSPM



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Refer to M-PIC Specification for additional details.

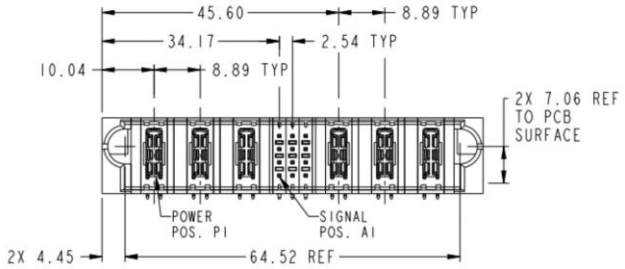
14.8.3. Ingress Power Connector

1000 The Far Side power connector is shown **in Figure 32 PICPWR connector (2x6+12s) Location Requirement (6 locations).** The connector must be based on Amphenol PowerBlade+ (or equivalent). The configuration is 3 high-power contacts on each side with 16 signal contacts in the middle. The pin-out and signal definitions must align with the definitions in the M-PIC and PICPWR specifications.

1005 Table 8. Blade Far/South Ingress Power Recommended Connector

Connector Family	**Company**	**Configuration**
PowerBlade+	Amphenol 10106263-6003003LF or equivalent	3 High Power + 16 Signals + 3 High Power

Figure 45. PowerBlade+ Ingress Power Connector

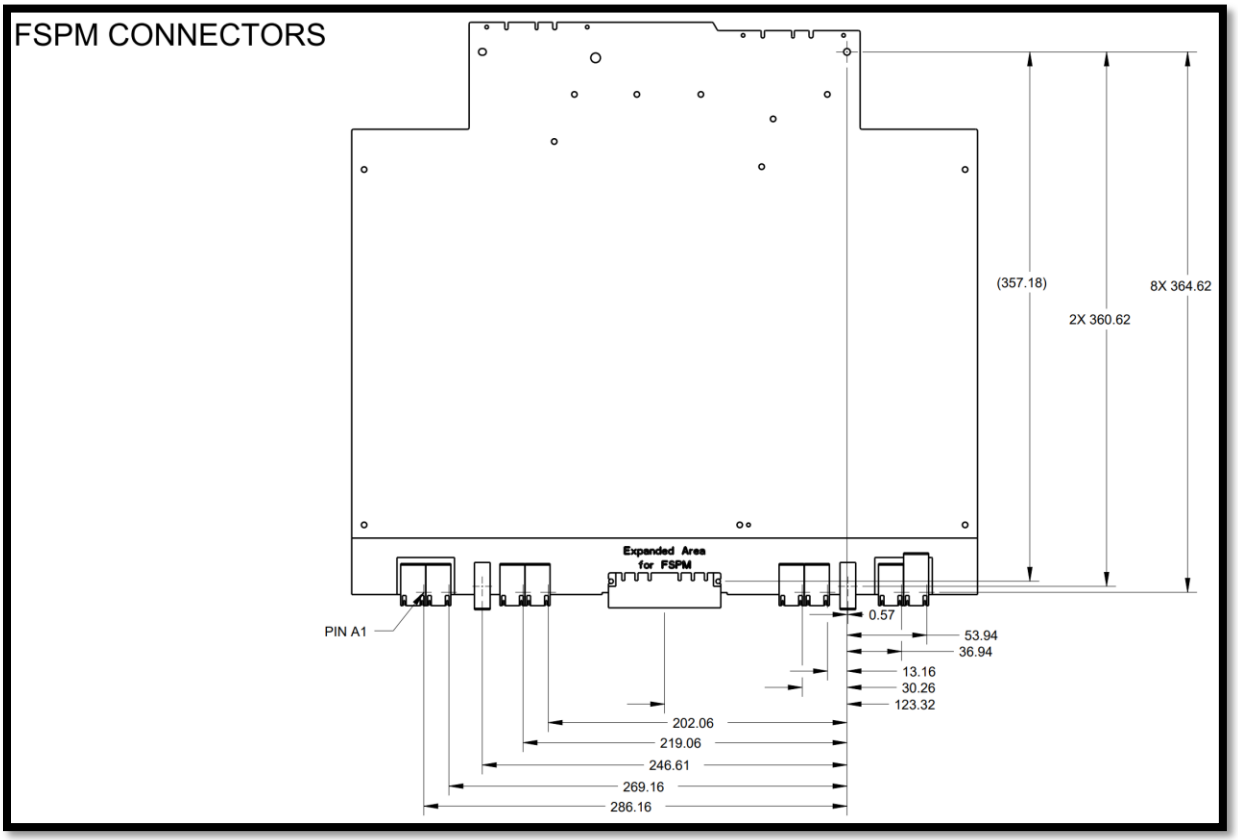


14.8.4. FSPM HPM Locations for Power and High-Speed IO

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The connector locations for the FSPM HPM are specified in **Figure 46** . The FSPM HPM must comply with these connector locations.

Figure 46. FSPM HPM Required Connector Locations



14.8.5. Blade Mechanical Guide Pin

The outline shown in **Figure 46** also includes a position identified for a mechanical guide pin for blind mate alignment. The HPM must implement these features for safe blind mate
1020 implementation. The part number to use for the guide pin should be Amphenol 10037912-101LF (or equivalent).

14.9. CAD files

CAD files for M-FLW are at the following link:

https://drive.google.com/drive/folders/1tSvFScjQ2P3_OUIPfpOrrpsSBydVpDE2?usp=sharing

Note: For import into Solidworks, choose “free curves” as an import option to see KOZs below.

Figure 47. STP CAD model picture

