



OPEN
Compute Project

Partial Width, Density Optimized HPM Form Factor (M-DNO) Base Specification

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Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

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M-DNO Authors / Contributors:

Dell, Inc: Michael Gregoire, James Utz, Corey Hartman, Sandor Farkas, Shawn Dube, Walt Carver, Owen Kidd

15 **Google LLC:** Jim Levins, Siamak Tavallaei

Intel Corporation: Dirk Blevins, Todd Langley, Leslie Fitch, Brian Aspnes, Michael Kasper, Susan Yost, Dan Surratt, Marc Milobinski

Hewlett Packard Enterprise Company: Rachid Kadri, Minh Nguyen, Vincent Nguyen

Meta Platforms, Inc: Todd Westhauser

20 **Microsoft Corporation:** Shane Kavanagh, Priscilla Lam, Mark Shaw

Advanced Micro Devices, Inc: Andrew Junkins, Greg Sellman, Paul Artman, Ravi Bingi

Jabil Inc.: Anthony Anconetani, Patrick Hampton, Matt McGuff

Ampere Computing: Jayesh Shah

NVIDIA Corporation: David Herring, Ray Laning, Tim Lee

25 Note: For questions about this specification please contact Michael Gregoire (michael.gregoire@dell.com) and / or Dirk Blevins (dirk.blevins@intel.com).

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1.2. Acknowledgements

185 With the hope of making this specification useful for the entire OCP community, we
acknowledge and appreciate the contributions, review, and feedback of various individuals and
companies that participated in DC-MHS.

2. Version Table

Date	Version #	Description
4/21/2022	0.7	Initial Public Release
6/22/2022	0.8	- Added Specification Compliance Table - Separated hole dimensioning to separate drawings - Added required pad size and recommended KOZs for all holes throughout document - Adjusted fixed riser connector positioning - Updated approach in Primary Side Component Height section - Added start of "zone" approach to PIC connector placement - Various text clarifications / edits - Various drawing updates and fixes
8/24/2022	0.9	- Rewrite of secondary side stackup, board thickness, board pan etc. (10.3, 10.4) - Removed Type 1 (many) - Changed certain values for Type 3 to TBD (many) - Placed all mounting hole information in one place (10.2) - Changed "mid-board" mounting holes from required to HPM Designer preference for all board types (10.2) - Removed secondary side keep out features for other board type hole locations (10.4) - Modified type 4 board outline in custom zone area (10.1) - Shifted HPM retention hole location (10.5) - Updated dimension scheme for recommended riser connectors, simplified verbiage for riser requirements (10.9) - Updated dimension scheme for PICPWR connectors (10.1.6) - Aligned PICPWR location optional / required characteristics across all board types (11.1) - Added PDB Management Connector (10.8) - Miscellaneous image and text cleanup throughout document (see change bars) - Added updated approach to primary side component height restrictions (10.12) - Added 1016 as a recommended option on far side (12.1) - Updated bottom side KOZ for board retention hole to align with FLW update (10.5) - Removed cable enablement section (added note to primary side KOZ section) - Added 2x3 PICPWR option, additional cleanup in power section (11.x) - Added adapted HPM chapter, moved note from power chapter to new chapter (13.x) - Simplified Ch 9 (removed board type goals) - Added tolerance table and custom tolerance for type 2/3 width (10,10.1) - Increased resolution of all figures - Additional Tweaks to NearIO verbiage to try and clarify intent (10.9) - Added required handle hole geometry (10.6) - Added Platform Custom Zone section with content TBD (10.13) - Added SFF number for riser connectors (12.1) - Scrubbed compliance table, added note not final until 1.0 (4) - Updated PIC connector locations (10.8) - Added example of re-purposing required mounting hole for Handle hole geometry
9/26/2022	1.0	1.0 Contains many clarifications and fixes. The most impactful changes for in flight designs based on 0.9 are denoted by '<' at the end of the line item - Updated document for consistent formatting of <u>requirements</u> and references - Added 'datum' and cleaned up the terminology table (7) - Small tweaks to compliance table (4) - Added reference and links to DC-MHS Current Connector List (6) (12) - Added reference to peripheral connector SFF-TA-1002 (10.7) - Removed adapted HPM chapter - Updated riser recommended connector name and power capability (11.1)

		- Added clarification that tolerance enables Open19 compatibility (10.1) - Reorganized supplemental material, added link to CAD (14) - Reorganized and clarified Sections 10.3 and 10.4 <- - Removed Power Plane section, added note on voltage drop (11) - Renamed and renumbered Power Zone chapter (11) - Updated tolerance table (10) - Updated top side component 6mm and 11.3mm zone shapes (10.12) <- - Updated Platform Infrastructure connector drawing (10.8) - Changed shape of board handle feature (10.6) <- - Added location numbering for PICPWR connectors (11.7) - Added example uses of Platform Custom Zone (10.13) - Moved recommended intrusion switch location (10.8) <- - Added separate image for Type 4 boot location zone (10.8) - Added route KOZ to HPM retention hole (10.5) <- - Added reference to battery voltage requirement from DCSCM (12) <- - Added additional industry references in separate section (13) - Corrected location of Detail B in Figure 11 (10/2) <- - Misc. text / drawing tweaks for clarity not impacting technical content
10/27/2022	1.0 RC5	- Added clarifying note to Figure 2 and Figure 4 (9) - Removed '2x' from Figure 9-11 as the second hole states is "not dimensioned" (10.2) - Updated CAD snapshot (14.3)
7/20/2023	1.01	RC1 - M-DNO ECN 1: Corrected location of E1.S in Type 4 Platform Custom Zone (Figure 35, Section 10.13.2) <- - Changed OCP NIC to strongly recommended (Section 10.7, Section 4) <- - Added 1016 / 1026 exception note to 11.3 and 12.0 component height zones, updated implementor note explaining cabling / system mechanical layer (Section 10.12) <- - Updated 1033 drawings with new connector (Figure 29, Section 10.9.2) - Updated Wiki Pointer to DC-MHS Wiki (Section 6) - Updated Terms table to link to Section 6 for DC-MHS family specifications (Section 7) - Updated compliance note with new language to mention compliance table (Section 3) - Added clarity that boot storage zone shown in Figure 27 and 28 is for the cabled boot connector option (Section 10.8) - Removed second OCP NIC from Figure 28 (Section 10.8) - Removed cabled boot connector from Figure 35 (Section 10.13.2) - Updated M-DNO, M-PESTI descriptions (Section 6) - Updated implementation note for offset connector selection (Section 10.4) - Updated note on board types to explain new DC-MHS strategy for "Type" (Section 9) - Added clarification that vias depicted are representative not prescriptive (Section 10.2) - Removed vendor name from PICPWR in Figure 37 (Section 11.2) - Ensured "shall" statements are always underlined and that all underline statements feature "shall" (Various) - Added M-SIF to Family of specifications (Section 6) - Added example of chassis base to support an HPM bracket or "board pan" (Section 14.4, 10.3.2) - Inclusion of new member companies RC2 - Updated table of contents and figures - Additional cleanup of "shall" requirements and underlining
3/14/2024	1.1	RC1 - Completed Type 3 definition (length changed from TBD to 550mm) (Various) - Corrected Typo for Type 4 Dimension H in Figure 26 (Section 10.8) - Updated connector offset implementors note (Section 10.4) - Changed references to DC-SCM 2.0 to DC-SCM 2.x (Various) - Added implementors note explaining anti-tilt feature of 1016/1033 cables (Section 10.9)

		• Added allowance for negative PCB features (Section 10.1.1) • Updated Zone 3 language and requirements (Section 10.3.3) • Corrected datum references for SFF-TA-1033 risers (Section 10.9.2.1) • Changed max HPM assembly thickness from 5.86mm to 6.2mm (Section 10.3 / 10.4) • Moved riser retention hole information to common drawings with other mounting hole information (Section 10.2) • Changed some previously required mounting holes to recommended (Section 10.2) • Re-Wrote HSIO connector section for clarity (placement rules for SFF-TA-1033 risers remain consistent with previous revisions) (Section 10.9) • Simplified compliance table references (Section 4) • Various language updates for clarity and alignment with other DC-MHS HPM specifications RC2 • Moved connector placement requirements from Chapter 12 to Section 10.8 where the relevant Figures are located
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3. Scope

This document defines technical specifications for the Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.

Any supplier seeking OCP recognition for a hardware product based on this specification must be 100% compliant with all features or requirements listed in Section 4 this specification.

3.1. Items Not In Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

3.2. Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

- Rack Compatibility (Discussed in Section 8)
- Physical Spec
- Thermal Design
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management (Leverages OCP DC-SCM R2.x)
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

4. Specification Compliance Table

The following table is meant to point the reader to sections containing Base Spec compliance required items. The table should not be used as a checklist as each row could contain multiple requirements. Base Spec compliance items are underlined and use the word “shall”.

Note: gaps in item numbering are intentional to avoid confusion related to requirements removed between V1.0 and this release.

Item	Requirement	Document Reference
1	PCB Tolerance Table	Section 10 (multiple items)
2	Follow the defined board Outline	Section 10.1 (multiple items)
3	All required mounting holes, including riser retention holes, with associated pads and KOZs	Section 10.2 (multiple items)
4	Unique alignment hole and slot with associated pad and KOZs	Section 10.2 (multiple items)
5	HPM Board thickness <= maximum defined	Section 10.4
6	Board Thickness + Backplate Thickness <= maximum defined (Backplate max thickness calculated as specified)	Section 10.4 & 10.3.4
7	Secondary side chassis hook keep out zones	Section 10.3.2 (multiple items)
8	Secondary side universal component height restriction	Section 10.3.1
10	Maximum length of a connector's Alignment Post or Retention Barb in Zone 2	Section 10.3.2
11	HPM to Chassis Retention hole and associated KOZs	Section 10.5 (multiple items)
12	Far Side hole for board handle with defined geometry and KOZs	Section 10.6 (multiple items)
13	Specified Location for OCP NIC 3.0 Co-Planar Connector, if implemented	Section 10.7
14	Specified Location for DC-SCM Co-Planar Connector	Section 10.7
15	Primary control panel connector placed within specified zone	Section 10.8
16	Intrusion switch header placed within specified zone	Section 10.8
17	Host USB connector placed within specified zone	Section 10.8
18	PDB Management connector placed within specified zone	Section 10.8
19	Any implemented board to board riser connectors placed in specific defined location	Section 10.9.2 (multiple items)
21	All non-exempt soldered components adhere to required Primary Side component height restrictions	Section 10.10 (multiple items)
22	If negative PCB features are implemented, follow section rules	Section 10.1.1 (multiple items)
23	Far side Ingress / Egress Power Zone with at least one 2x6 + 12SB PICPWR connector in specified location(s)	Section 11.2, Section 11.7 (multiple items)
24	If implemented, Near side Ingress / Egress Power Zone with 2x3+6S or 2x6+12S PICPWR connector(s) in specified zone	Section 11.2, Section 11.7 (multiple items)
25	Each implemented riser location connector is PICPWR compliant	Section 11.3, M-PIC
26	HPM delivers at least 87W to each implemented riser location	Section 11.3
27	All HSIO connectors (near and far) are M-XIO compliant	Section 10.9.1, M-XIO (multiple items)
28	Internal USB follows M-PIC specification	Section 10.8, M-PIC
29	Intrusion Switch follows M-PIC specification	Section 10.8, M-PIC
30	If implemented, boot storage follows M-PIC specification	Section 10.8, M-PIC
31	Primary control panel follows M-PIC specification	Section 10.8, M-PIC
32	If implemented, secondary control panel follows M-PIC specification	Section 10.8, M-PIC
33	PDB Management Connector follows M-PIC specification	Section 10.8, M-PIC
34	HPM shall implement battery backed voltage interface per DC-SCM R2.x “Battery Voltage” requirement	Section 10.7, DC-SCM 2.x

5. Overview

The objective of this specification is to outline the requirements of a family of partial width, **DeNsity Optimized Host Processor Module (HPM)** form factors within the OCP **Modular** hardware system group of specifications (**M-DNO** for short). This M-DNO specification embodies design considerations for CPU, DIMMs, and other server processor related features commonly used by the industry today but is not limited to only those functions. For instance, an FPGA array being placed within the Compute Area of the HPM is allowable per this specification. The HPM is designed with standard 19" rack, also known as compliant with EIA - 310-E and larger 21" racks in mind but is not limited to only those solutions. This specification considers both monolithic and multi-node / "blade" based system architectures in its definition.

The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs implemented to the specification to enable reuse of chassis and system level components over multiple generations and HPMs. Implementing to this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of Enterprise and Cloud solutions and may also apply to Edge optimized service provider products. Examples of these attributes are mechanical form factor, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections.

6. DC-MHS Family of Specifications

265 The **Data Center – Modular Hardware System (DC-MHS)** family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specifications:

- 270 • **M-CRPS (Modular Hardware System Common Redundant Power Supply Specification)** – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- 275 • **M-DNO (Modular Hardware System Partial Width Density Optimized Specification)** – Host Processor Module (HPM) specification targeted to partial width (i.e. $\frac{1}{2}$ width or $\frac{3}{4}$ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments.
- **M-FLW (Modular Hardware System Full Width Specification)** – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- 280 • **M-PESTI (Modular Hardware System Peripheral Sideband Tunneling Interface)** – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (i.e., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- 285 • **M-PIC (Modular Hardware System Platform Infrastructure Connectivity Specification)** – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- 290 • **M-SDNO (Modular Hardware System Scalable DeNsity Optimized Specification)** – Builds upon M-DNO, defines partial and full width HPMs with variable board outlines covering 19" EIA-310 and 21" OpenRack v3 infrastructure.
- **M-SIF (Modular Hardware System Shared Infrastructure Specification)** – Specifies data and management plane interfaces along with power and cooling connections that are expected to be present within a modular platform utilizing shared elements.
- 295 • **M-XIO (Modular Hardware System Extensible I/O)** – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- 300 • **Current Connector List** – Vendor and part number information for all connectors referenced by DC-MHS specifications, updated as needed. Full URL:
https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/

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To access additional DC-MHS specifications please visit the DC-MHS Project Wiki:
<https://www.opencompute.org/wiki/Server/DC-MHS>

7. Terminology

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for spec compliance	Must
DC-SCM	Datacenter Secure Control Module v2 as defined by OCP DC-SCM 2.x spec	SCM
PCB	Printed Circuit Board	PCBA
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
Chassis-Board Bracket	Bracket that attaches to an HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan Sub Pan
Datum	A plane, axis or point location from which dimensions and tolerances are referenced.	
Near	Board location or zone, related to section of board closer to the datum	
Far	Board location or zone, opposite of location of datum	
Platform	Complete system including HPM, power, peripherals, etc	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
CSP	Cloud Service Provider	
½ Width HPM	210mm wide HPM, enables systems with 2 HPMs side by side in 19" Rack	
¾ Width HPM	295mm wide HPM, enables systems with HPM adjacent to 2xM-CRPS PSUs	

Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	
Platform Infrastructure Connectivity Specification	Refer to Section 6	M-PIC
Full Width Specification	Refer to Section 6	M-FLW
Common Redundant Power Supply Specification	Refer to Section 6	M-CRPS, CRPS PSU
Extensible I/O Specification	Refer to Section 6	M-XIO
KOZ	Keep Out Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
Compliant HPM	An HPM which meets every item listed in this base specification compliance table.	
Adapted HPM	An HPM that utilizes a Compliant HPM as a construct, with a specific set of repeatable modifications which form the adaptation.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements this base specification.	
System Designer	The person or organization designing a system which incorporates HPMS (whether compliant or adapted) into the system design.	

8. Background & Assumptions

M-DNO targets a wide variety of 1 and 2 socket platforms including multi-node and monolithic (one HPM per chassis) systems for use in Enterprise, Cloud, and Edge applications. In these applications the range of targeted chassis can be extremely varied, as can the location of the HPM within the chassis. Monolithic systems are typically, but not limited to, 1RU or 2RU designs. Multi-node systems on the other hand are expected to have a broad application set from 2U (e.g. 4 ½ Width HPMs) to 5U (e.g. 8-12 ½ Width HPMs in vertical orientation) chassis and beyond. Rear and Front service models (including articulating chassis with removable cover) are also considered.

When considering representative system depth targets, the most common environments were distilled into the following categories:

1. Standard Depth Rack / Solution

- ~1070mm+ deep with a single ½ width (210mm) or ¾ width (295mm) HPM
- ~1070mm+ deep with two ½ width (210mm) HPMs

2. Mid Depth Rack / Solution

- ~430mm to 570mm deep with a single ½ width (210mm) or ¾ width (295mm) HPM

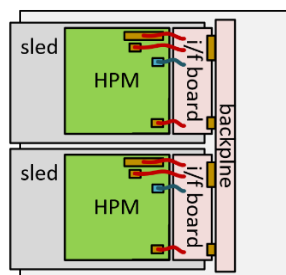
3. Short Depth Rack / Solution

- ~350mm to ~430mm deep with a single ½ width (210mm) HPM

This specification focuses on products targeted to these primary environments. **Section 14.1** illustrates design scenarios for each of these solutions providing the reader a clearer understanding of each category. This specification does not in any way prohibit alternate environments.

V1.1 of this specification does not address native “direct plug” or “blind mate” options for HPMs, these scenarios may be added in a future release. It is assumed that HPMs compliant with V1.1 will leverage an interface board to enable these use cases as demonstrated in **Figure 1**.

Figure 1: M-DNO HPM with multi-node interface board



8.1. Common Industry Platform Features Considered

340 Mechanical

- Chassis installation within minimum EIA-310-E racks (but not limited to)
- PCIe Riser Connector fixed placement
- PCIe Cable route considerations
- Any additional fixed connector placement

345

I/O

- PCIe (Version 3.0, 4.0, 5.0, and future) Card configurations typically offered by Enterprise OEMs/CSPs/CoSPs.
- In 1U offerings with PCIe CEM based I/O, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would restrict Compute Core placement (not defined).
- Use of Open Compute peripherals connectors on the HPM
 - OCP NIC R3.0
 - HFF DC-SCM R2.x
 - *Note: While each HPM outline depicts 1 connector of each type, a system is not limited to 1 device of each type; configurations with 0 or >1 OCP NIC R3 / DC-SCM R2.x are possible, but outside the scope of this specification*

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Power

- HPM supplied power to each fixed riser locations
- HPM Power Ingress and Egress connector placement for a variety of power layouts (PSUs with Cabled PDB, blind mate to bus bar, multi-node backplane, etc.)
- Considerations for Power Delivery to important chassis subsystems.

360

Thermal

- Thermal Design considerations including keep-out zone to enable thermal solutions that extend beyond the CPU and Memory sockets.

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8.2. Architecture Specific Assumptions

Mechanical / Systems

- 370 • M-DNO based systems
 - Do not direct plug PSUs into the HPM but instead leverage Power Distribution Boards (PDB) or other system / rack level power infrastructure
 - Use remote fan designs in air cooled platforms (there is no HPM spec provision for Fan connectors on the HPM)
- 375 • Support riser based I/O cards, cable based I/O cards or a mix of both
- Leverage a variety of front and rear service models of I/O, PSU, HPM, etc.
- Systems designed for larger HPM Types may support use of smaller Types in a common chassis or sled with minimal changes (e.g. cables, riser quantities, standoff locations)
- Multi-node chassis designs leverage static rails with overall inner chassis opening width of 443mm (in 19" rack)
- 380 • Monolithic chassis designs leverage slide rails with overall inner chassis width of 431mm (in 19" rack)
- $\frac{3}{4}$ Width HPM must accommodate 2x 60mm M-CRPS PSUs within chassis opening described above (431mm)

385

I/O

- All M-DNO HPM Types enable (but do not require systems to utilize) use of "off the shelf" OCP NIC V3.0
- Mid / Standard Depth systems will *typically* leverage Coplanar OCP NIC layouts
- 390 • Short Depth systems will often require alternate implementation such as "floating" the OCP NIC (or no-pop)
- PCIe CEM based I/O will be the predominant use case for consideration but alternate form factors are not prohibited

395 DC-SCM

- All M-DNO HPM Types enable (but do not require systems to utilize) use of "off the shelf" HFF DC-SCM 2.x
- Mid / Standard Depth systems will *typically* leverage Coplanar DC-SCM
- Short Depth systems will often require alternate implementation such as "floating" DC-SCM

400

9. HPM Layout

A Note on Board Types:

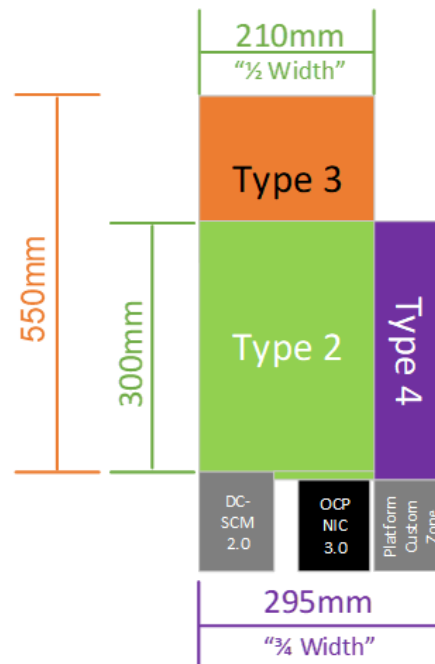
DC-MHS M-FLW and M-DNO HPM specifications (M-FLW 1.x, M-DNO 1.x) leverage a common set of Types which represent HPMs across both specifications

As of this M-DNO v1.1 release,

- Type 1 is defined in the M-FLW specification
- Type 2 and 4 continue to be defined in this M-DNO specification (since V1.0)
- Type 3 is newly completed in the v1.1 release of this M-DNO specification
- The DC-MHS M-SDNO specification does not define Types, but instead defines HPM “Classes”

To achieve the goals outlined in **Section 8**, this M-DNO specification defines three different HPM board “Types”. Note that the M-DNO specification does NOT mandate CPU / DIMM quantities or define a specific area for CPU and Memory.

Figure 2: M-DNO Board Type Layout Overview



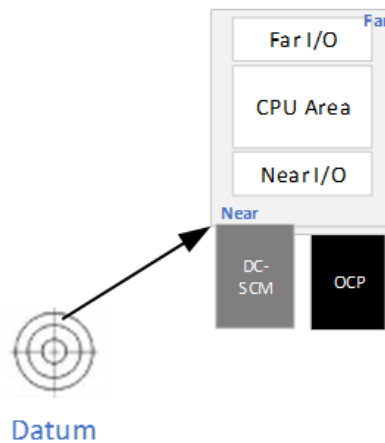
Note: Length dimensions shown represent DC-SCM side board edge

Figure 2 provides a dimensional overview of the three board types, additional definitions and concepts are described below:

1. Due to the wide array of potential HPM and Chassis configurations, this specification defines a **Near** <<Element>> as the <<Element>> closer to the Datum (0,0 reference) and **Far** <<Element>> as the <<Element>> further from the Datum, examples for <<Element>> include:
 - a. Corner
 - b. Edge
 - c. I/O Zone

An example of Near and Far terminology usage is shown in **Figure 3**.

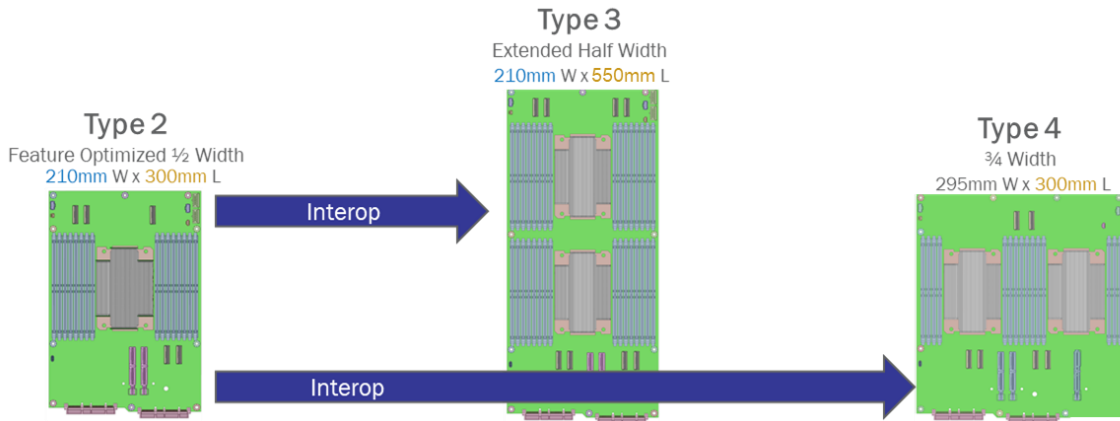
Figure 3: Near and Far Terminology Example



2. The location of the DC-SCM and OCP NIC connector on the HPM shall be common across all types relative to the Datum point (0,0)
3. "½ Width" refers to the common 210mm HPM width shared by Type 2 and 3
4. "¾ Width" refers to the 295mm HPM width used in Type 4
5. "Full Width" HPMs are outside the scope of this specification and are defined by the M-FLW specification
6. HPMs narrower than ½ Width are also outside the scope of this specification due to the inability of supporting common DCSCM 2.0 and OCP NIC 3.0 connector locations as described in #2. The DC-MHS workgroup may consider narrower HPM designs in the future.
7. The goal of this specification is to provide HPM Interoperability of smaller M-DNO HPM Types in systems designed for larger M-DNO HPM Types with minimal modifications (e.g. board pan or I/O cable changes), as depicted in **Figure 4**:
 - a. Type 2 HPMs can be easily leveraged into systems which support Type 3 HPMs
 - b. Type 2 HPMs can be easily leveraged into systems which support Type 4 HPMs
 - c. These goals do NOT apply between M-DNO and M-FLW HPMs

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Figure 4: M-DNO Type Interop Goals



Note: Length dimensions shown represent DC-SCM side board edge. HPM layouts depicted are **EXAMPLES ONLY**, many of the details are not specified by the M-DNO specification (DIMM count, connector locations and quantities, exact CPU Placement, etc.)

10. Mechanical Requirements

In addition to the drawings and details within this document, DFX/CAD files will be provided for further detail (**Section 14.3**).

Unless otherwise specified all units are in mm.

Unless otherwise specified, PCB dimensions shown in this specification shall comply to **Table 1**.

Table 1: Standard Tolerances

Dimension Type	Tolerance, unless otherwise specified
FROM Origin/Datum hole center TO round fiducial center	+/- 0.076mm (+/- 0.003 inch)
FROM Origin/Datum hole center TO profiled card edge	+/- 0.254mm (+/- 0.010 inch)
FROM Origin/Datum hole center TO drilled hole center	+/- 0.127mm (+/- 0.005 inch)
FROM Profiled card edge TO profiled card edge	+/- 0.127mm (+/- 0.005 inch)
Feature of size (hole diameter, slot width, etc.)	+/- 0.100mm (+/- 0.004 inch)
PCB thickness	+/- 10% of nominal

Route KOZ's referenced in this specification, at a minimum, refer to surface layers and microstrip routing. Further application of the Route KOZ to other layers is the choice of the HPM designer and/or Design specification.

10.1. HPM Outlines

There are 3 M-DNO HPM Type Outlines defined as described in **Section 9**.

The required M-DNO Type 2,3 and 4 Outlines shall adhere to **Figure 5 – Figure 7** below.

Note that **Figure 5** and **Figure 6** contain unique tolerances when dimensioning the HPM width. These asymmetric width tolerances allow the HPM designer to optionally choose to set the nominal total width to 209.55 if desired for use within a single-height half-width (SHHW) Open19 “brick”.

Note that the Type 4 outline near the Platform Custom Zone (described in **Section 10.11**) shown in **Figure 7** may change for connector choice compatibility specific to the usage of the Platform Custom Zone.

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Figure 5: Type 2 HPM Outline

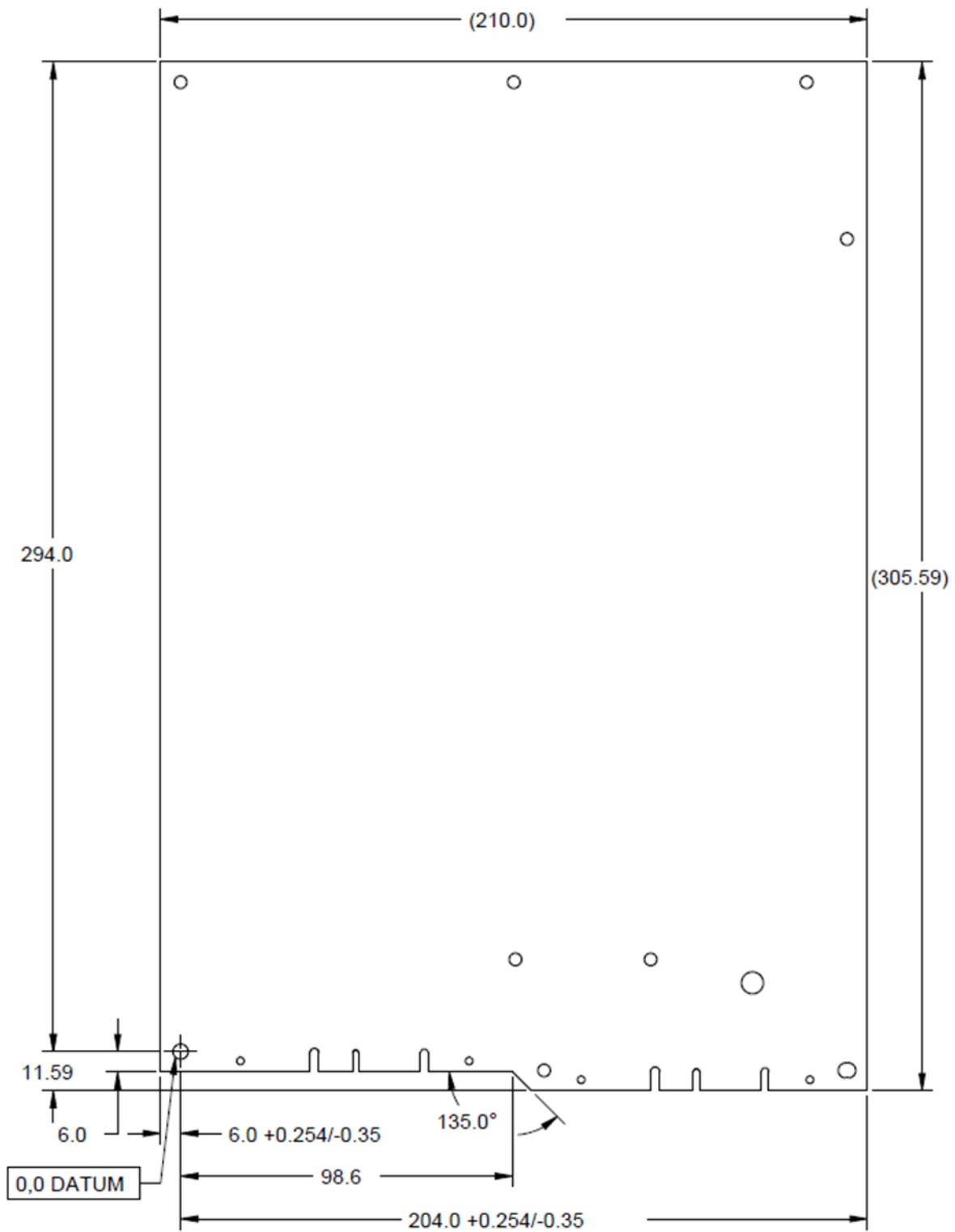


Figure 6: Type 3 HPM Outline

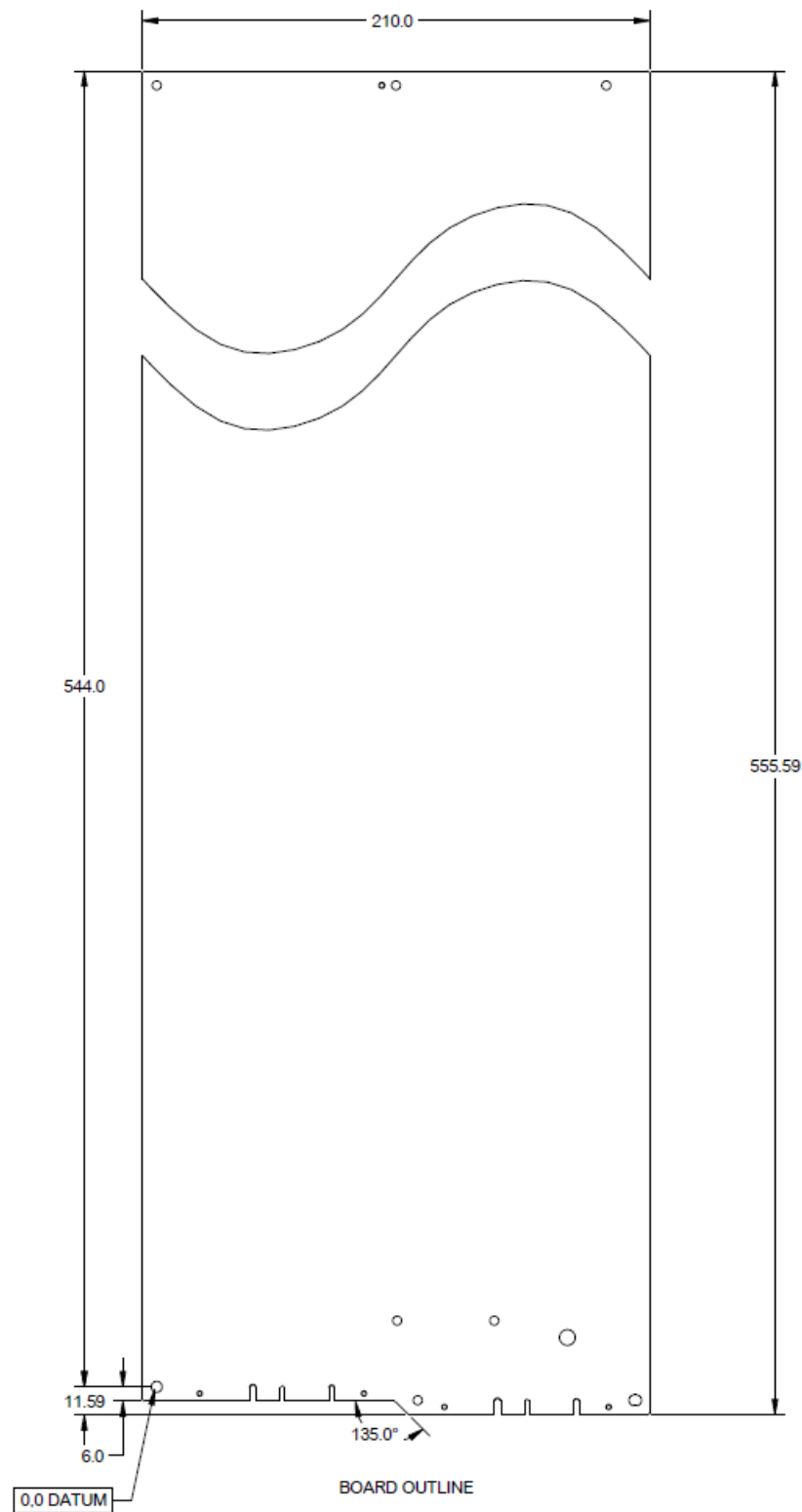
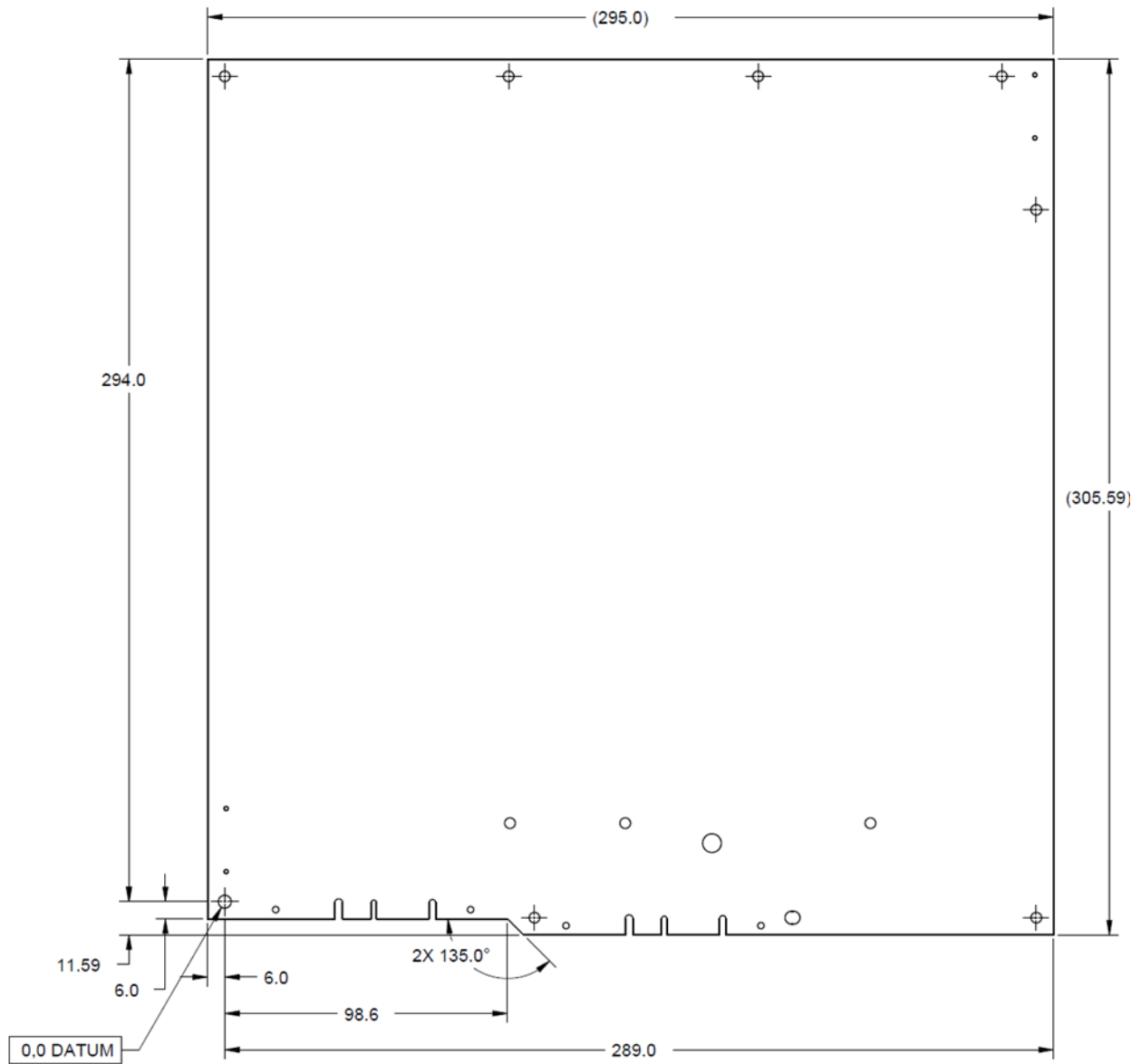


Figure 7: Type 4 HPM Outline

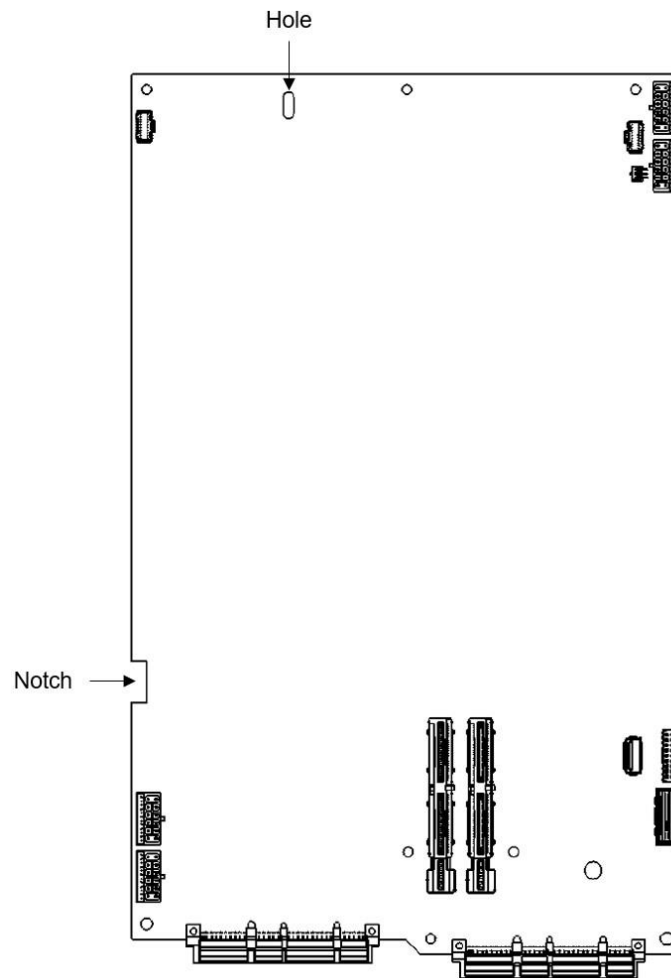


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10.1.1. Allowance for Negative PCB Features

All HPM types may include “negative PCB features” with the noted limitations. A negative PCB feature is defined as removal of PCB material in localized areas of the HPM outline. Examples of negative PCB features include notches along a board edge or openings of any geometric shape within the HPM outline. See **Figure 8** for illustrative example.

Figure 8: Negative PCB Feature Example



All negative PCB features implemented shall comply to the following restrictions:

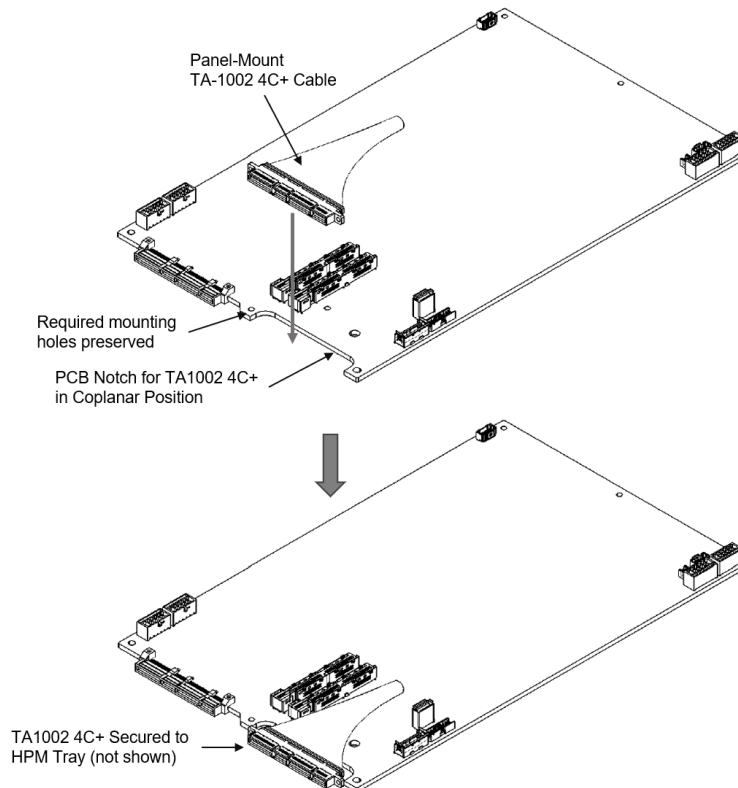
1. Negative PCB features shall not violate or conflict with any required features such as mounting holes and connector placement.
2. The negative PCB feature shall not extend the full length of the left or right edge of an HPM (i.e., this feature shall not be used to essentially create a non-standard HPM width).

Implementors Notes:

HPM-level and system-level manufacturing, handling, shipping, and operational environments must be considered by the HPM designer. When implementing negative PCB features the HPM designer should consider the implications on HPM structural integrity.

The use of a negative PCB feature can afford the option of a chassis or HPM tray feature to reside within this evacuated area. However, it should be noted that if this chassis or HPM tray feature must always be present, then other specification compliant HPMs that do not have these negative PCB features may not be interoperable with this system. An ideal system implementation would not require these negative PCB features to be present on all supported HPMs.

An example application of a negative PCB feature is the use of a notch at the M-DNO reference OCP NIC3 connector location combined with the use of a cabled panel-mount TA-1002 4C+ connector. The use of the cabled NIC3 connector enables flexible NIC3 location within the system. The shown notch preserves the option to position the NIC3 in the reference location, thereby mimicking a straddle-mount coplanar 4C+ on the HPM. The PCB notch geometry would be a function of the specific panel-mount 4C+ connector chosen for this application.



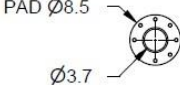
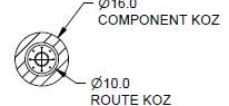
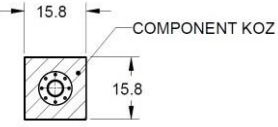
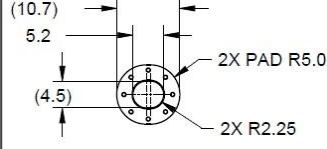
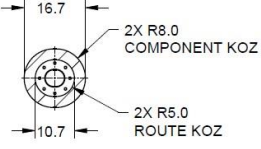
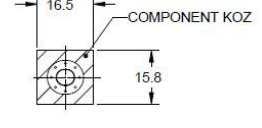
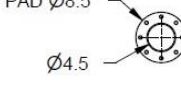
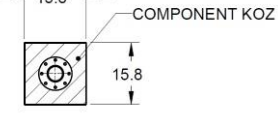
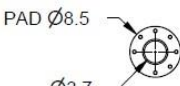
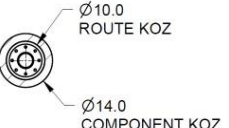
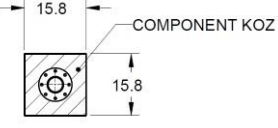
10.2. Board Datum and Mounting Hole Information

All M-DNO board types leverage a common datum location at the center of the mounting hole in the near corner of the board where the DC-SCM 2.x connector resides. This allows for fixed elements (riser connectors, peripheral connectors, ...) to have a common reference across all board types.

Detailed hole information common to all board types is provided in **Figure 9**. The vias that are shown in Figures are for reference only. Via requirements are NOT in scope of this specification. All holes shall adhere to the specified size, ground pad dimensions, component KOZ and route KOZ.

The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension (i.e. a DIMM connector), it is considered more robust, and may encroach on the Component KOZ's.

Figure 9: Hole Detail Reference

	Hole and Pad Sizes	Top Side KOZs	Bottom Side KOZs
DETAIL A Standard Mounting Hole			
DETAIL B Unique Alignment Slot			
DETAIL C Unique Alignment Hole			
DETAIL D Riser Retention Holes			

It is expected that HPM designers will add additional mounting holes based on their HPM layout. All additional holes shall adhere to Standard Mounting Hole requirements (Detail A in Figure 9).

505 A design should follow good engineering practices in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

There are required holes associated with each Near IO fixed riser location (Detail D in **Figure 9**) that shall be implemented regardless of whether the riser connector is implemented. The intent of requiring these holes is to always make retention holes available to system designers
510 (including systems with cable based I/O).

Riser retention holes are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). System designers may choose the hardware and utilization method for riser retention.

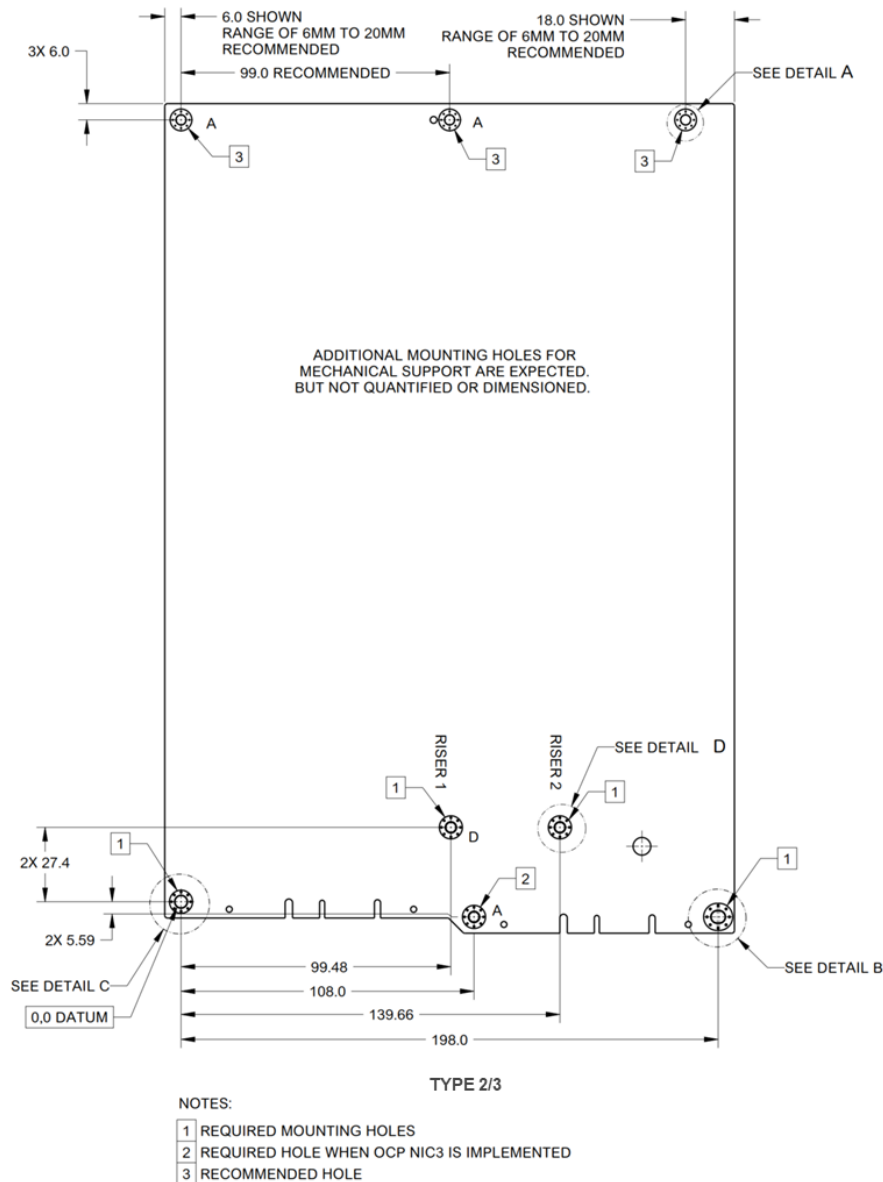
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10.2.1. Type 2 and 3 Mounting Holes

There are four required mounting holes on the Type 2 and 3 near side that shall be implemented. There is one additional required near side hole if the OCP NIC3 is implemented.

There are three recommended mounting holes on the Far Side. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm with a recommended span of 99mm. **Figure 10** shows the recommended placement for three of these holes. Note that **Figure 10** shows a Type 2 HPM, however it is accurate for Type 3 with holes dimensioned to the HPM edges.

Figure 10: Type 2 and 3 Mounting Holes

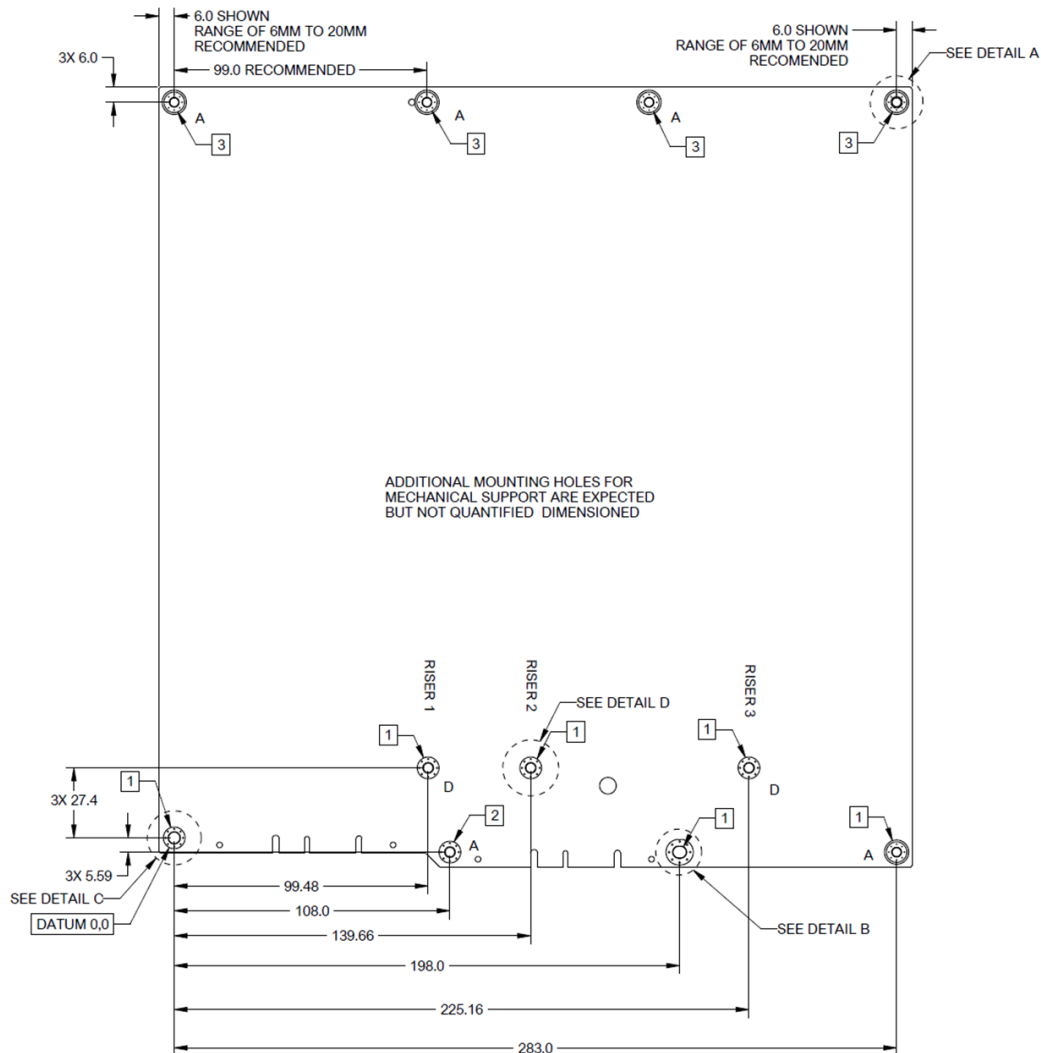


10.2.2. Type 4 Mounting Holes

There are six required mounting holes on the Type 4 near side that shall be implemented.
There is one additional required near side hole if the OCP NIC3 is implemented.

There are four recommended mounting holes on the Far Side. It is further recommended that the x-direction span between any two adjacent Far Side edge mounting holes is no larger than 140mm with a recommended span of 99mm. **Figure 11** shows the recommended placement for four of these holes.

Figure 11: Type 4 Mounting Holes



NOTES:

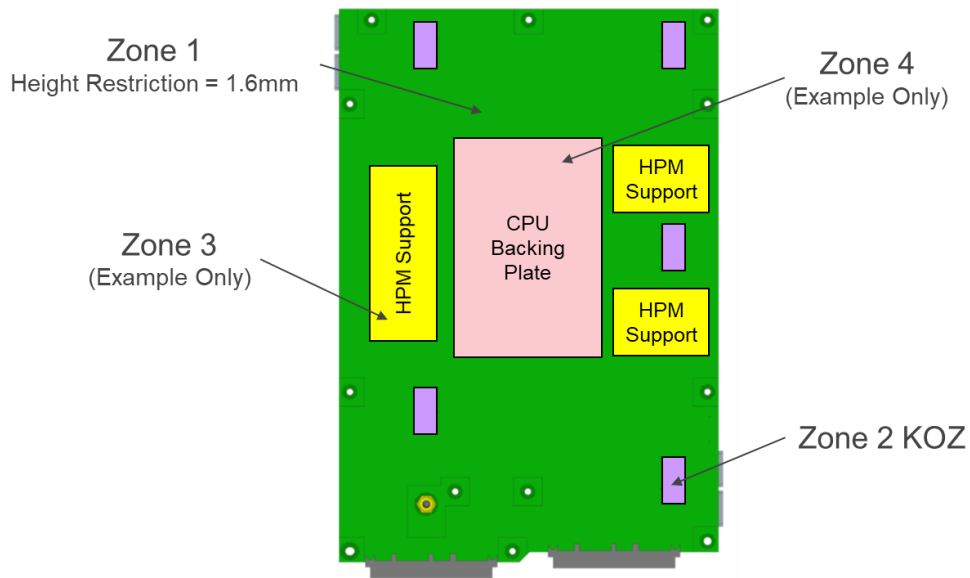
- 1 REQUIRED MOUNTING HOLES
- 2 REQUIRED HOLE WHEN OCP NIC3 IS IMPLEMENTED
- 3 RECOMMENDED HOLE

10.3. Secondary Side Zones and Height Restrictions

There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 12**. Each zone serves a unique purpose.

540 Zone 1, 2, 3 and 4 define different Requirements for Compliance.

Figure 12: Secondary Side Zone Definitions



10.3.1. Zone 1: Secondary Side Height Restriction

545 Zone 1 universally applies to the entire secondary side of the HPM, except for the defined Zones 2, 3, and 4. HPM electrical components are expected to utilize Zone 1.

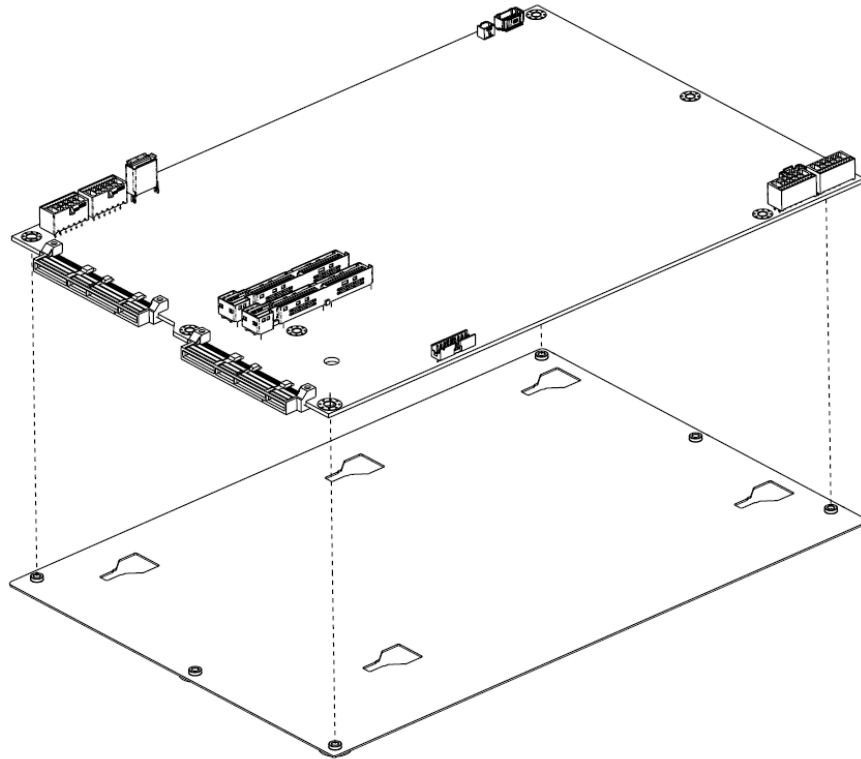
There shall be a required Zone 1 universal secondary side component height restriction of 1.6mm for all board types. This requirement ensures HPM component clearances to chassis base or board pan structures. This is especially important with a max allowable board thickness as defined in **Section 10.4**.

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10.3.2. Zone 2: Chassis to HPM Bracket (Board Pan) KOZ Requirements

M-DNO HPMs shall allow for a Chassis-to-Board Bracket (Board Pan) which enables different board layouts (and mounting hole locations) between HPM Types and Compute Core designs, while maintaining compatibility to a common chassis. An example Board Pan is shown in **Figure 13**.

Figure 13: Example of Chassis-to-Board Bracket (Board Pan)



Implementors Note:

While most monolithic server designs benefit from a Board Pan, it is NOT expected that all systems supporting M-DNO HPMs will require a Board Pan. Specifically, sled-based designs common in multi-node systems typically do not require a board pan. An example sled based secondary side zone stack-up can be derived by referring to **Table 2: Example Z-Height Compliant Stack-Up, Per Zone**, and replacing the space allocated to item 'F' and 'G' with the sled mechanicals.

M-DNO HPMs shall support required zero height KOZ locations for chassis hook features that interface between the chassis base and the Chassis-to-Board Bracket as defined in **Figure 14 – Figure 16**.

A supporting chassis base must provide hook geometry to interface the cutouts on the Chassis to Board Bracket.

For an example of a chassis hook concept, see **Section 14.4**. The geometry of the Board Bracket is not specified and is a design choice for the System Designer.

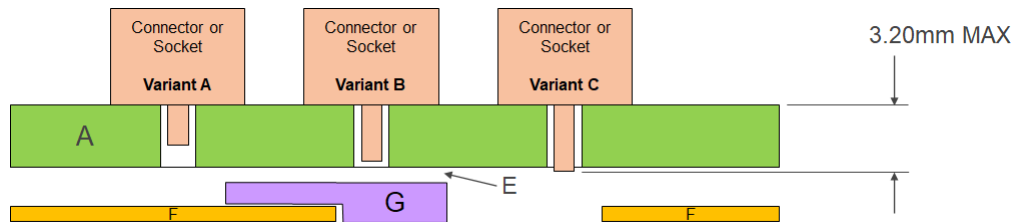
Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb shall be 3.20mm MAX such that it will not interfere with chassis hook features.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout.

Implementors Note:

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly. Refer to **Table 2: Example Z-Height Compliant Stack-Up, Per Zone** for details on 'A', 'E', 'F' and 'G'.



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Figure 14: Type 2 HPM Secondary Side Chassis Hook Locations

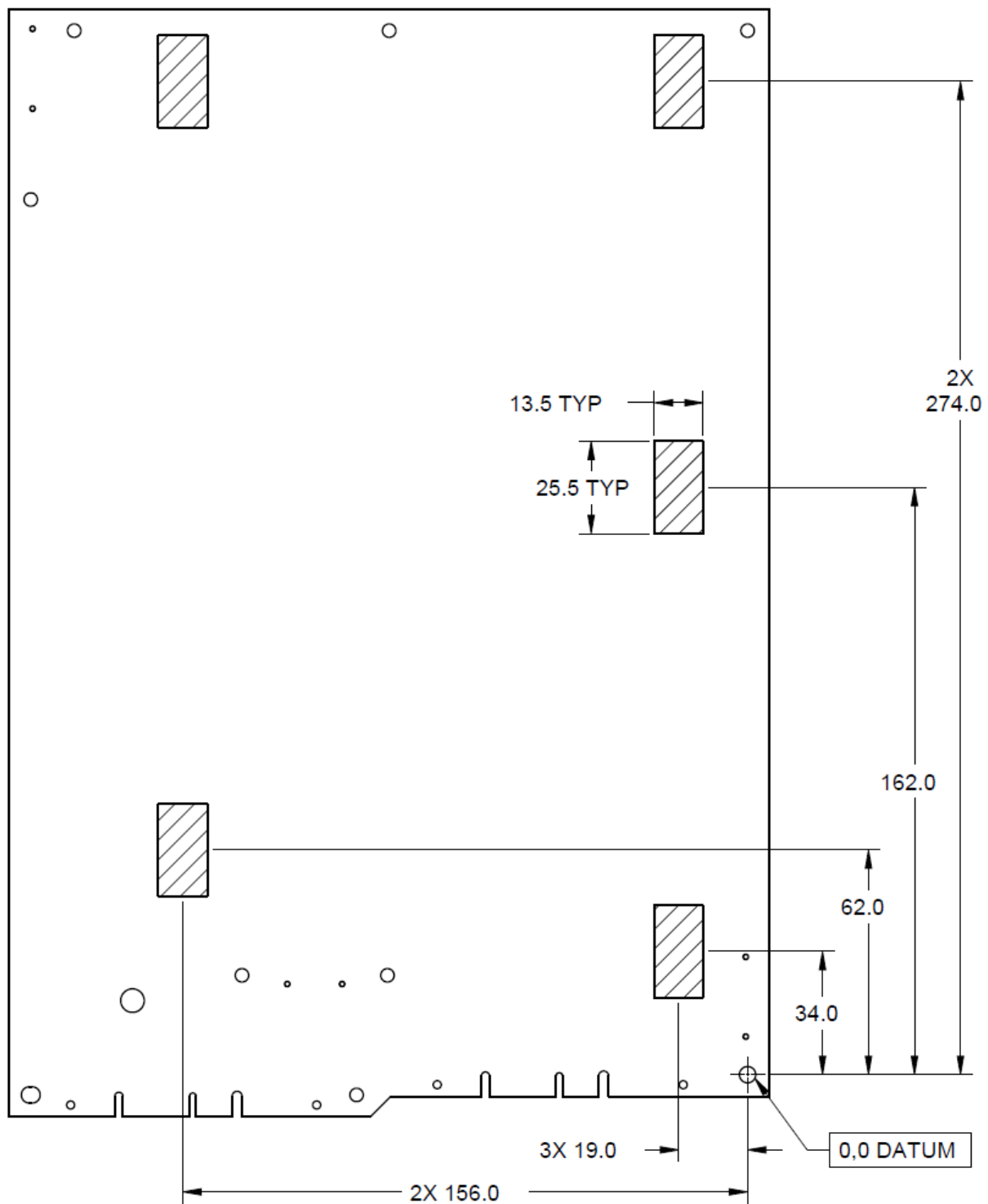


Figure 15: Type 3 HPM Secondary Side Chassis Hook Locations

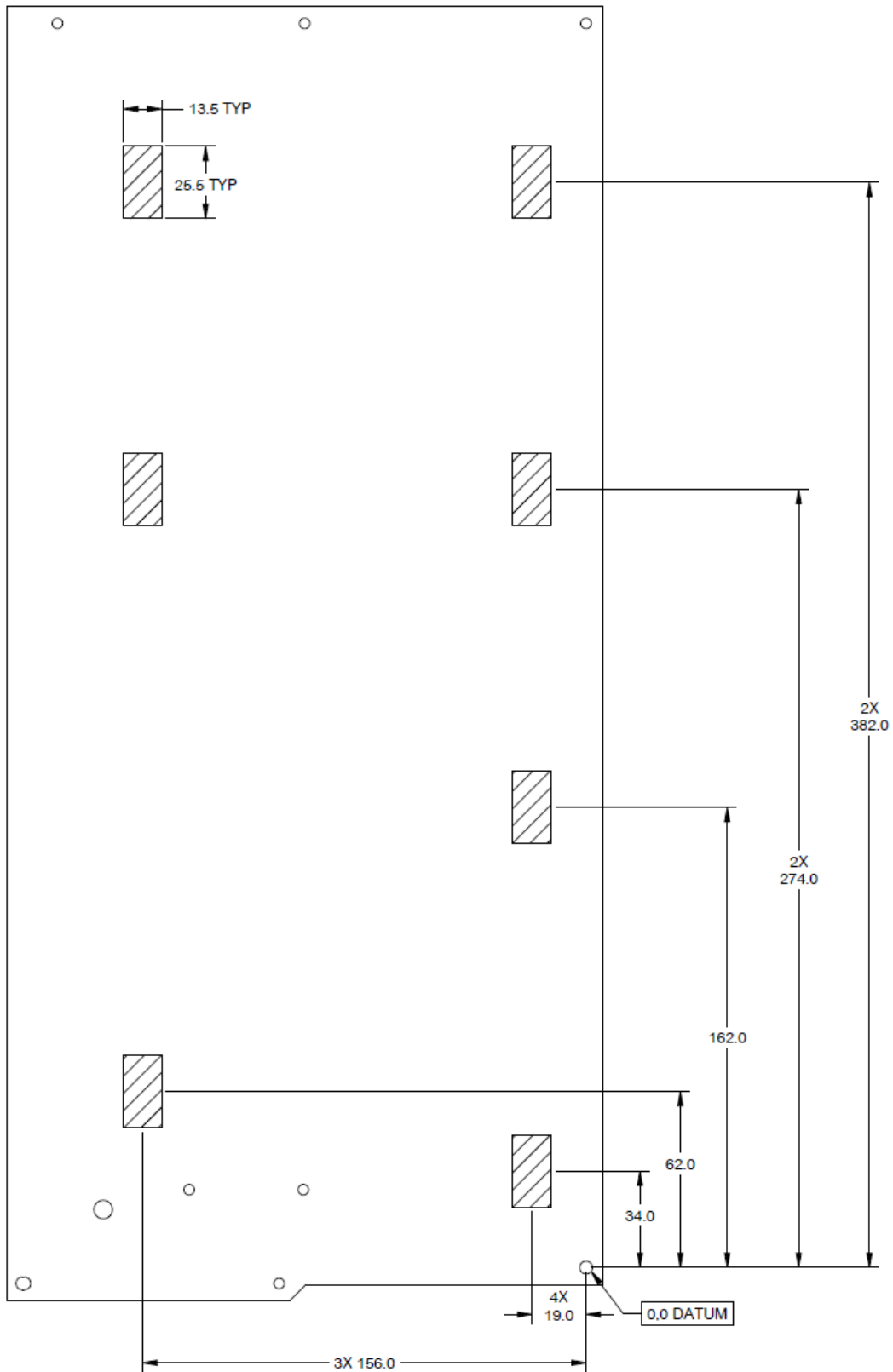
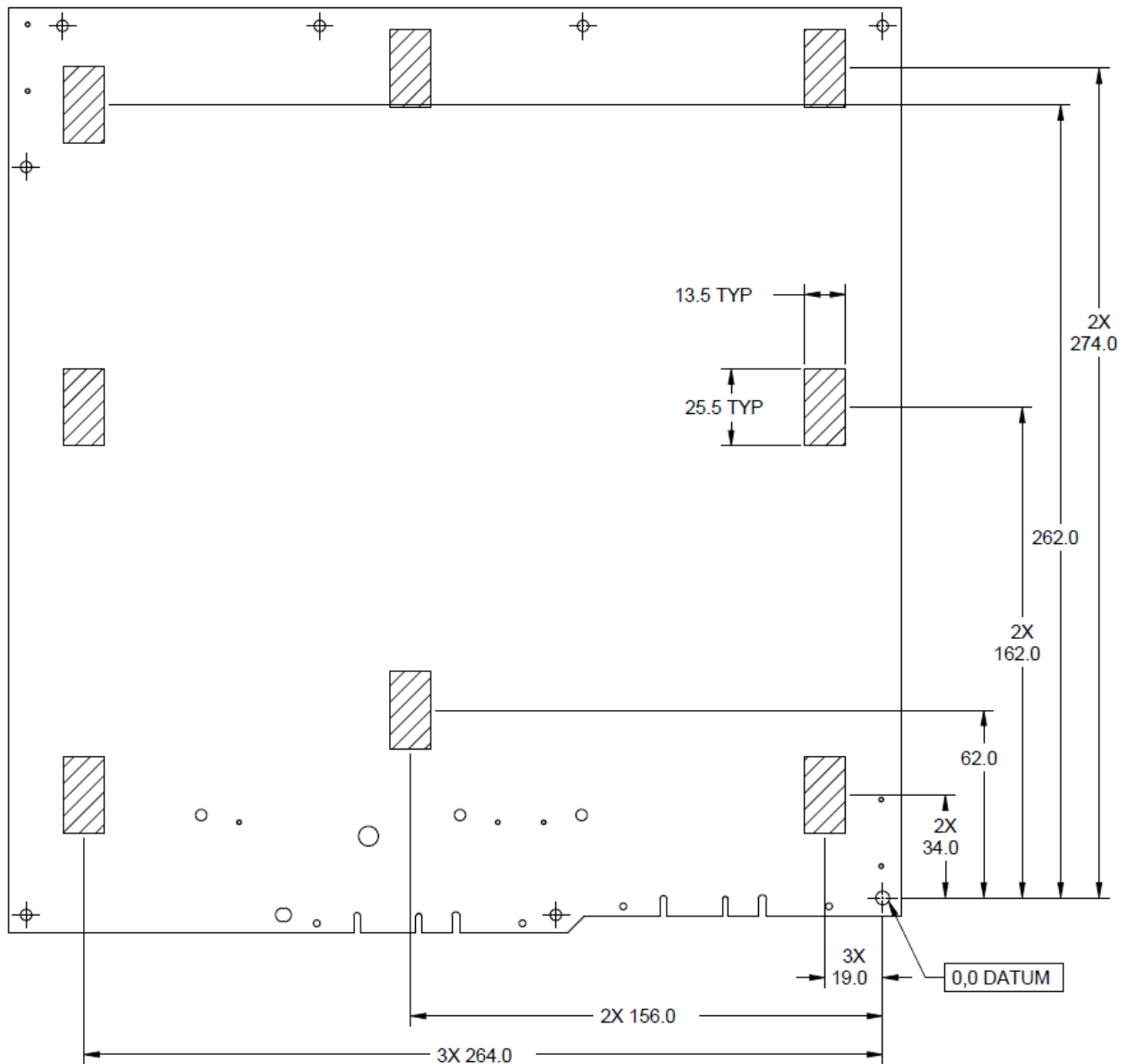


Figure 16: Type 4 HPM Secondary Side Chassis Hook Locations



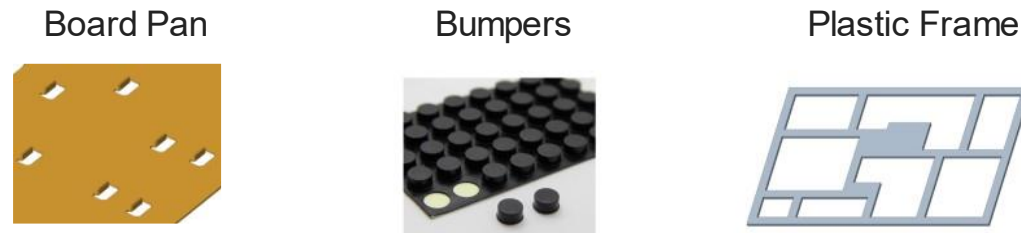
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10.3.3. Zone 3: HPM Secondary Support Requirements

HPMs may require secondary side support under the DIMMS and other semi-supported areas where HPM deflection is likely to occur during normal assembly processes. Two common design approaches to provide this support are:

1. HPMs can identify and provide areas for chassis designs to directly support the HPM PCB surface. These areas need to be clearly identified and free from any conductors or risk of shorting (no exposed vias, traces or components). Chassis designers may choose to support these areas with Board Pan formed features (metal) or bumpers/fillers (rubber or plastic).
2. HPMs can include bumpers or fillers in their design that are tuned in Z height (2.12mm +/- 0.10mm) to match with the Board Pan and exceed the height of all bottom side components.

Figure 17: Example Secondary Side Supports



10.3.4. Zone 4: CPU Backing Plate Requirements

Most server HPM designs need to support CPU backing plates or stiffeners placed under the CPU as part of the CPU Socket design.

The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by:

- Backing Plate allowed Height = 6.2mm – HPM thickness – 0.08mm standoff height tolerance – allowances for other backplate design req's (insulators, deflections, etc)
- See Implementors Note below for examples.

Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and / or HPM sled as shown in **Figure 21: CPU Backing Plate (Zone 4)**.

Implementors Note:

HPM and CPU designers should consider these example Scenarios supported by DC-MHS HPM board and Backing plate thickness requirements.

Board Thickness (Nominal, mm)	Maximum Allowable CPU Backing Plate Thickness (mm)
1.57	4.55
1.93	4.19
2.36	3.76
2.55	3.57
3.18	2.94

10.4. HPM Board and Assembly Thickness

- 610 • The maximum allowed thickness and zone heights in the specification assume a minimum 6.2mm board mounting height.
 - Thickness and zone heights are established to ensure forward compatibility with 1U & 2U System Chassis assumptions.
 - Exceeding the thickness and zone height target values would result in system design impacts and incompatibilities
- 615 • The board mounting height for a given system is not within scope of the HPM specification, and is at discretion of the System designer.
- The maximum allowed HPM thickness shall be 3.18mm nominal and assumes +/-10% tolerance is allowed.
 - 620 • Note that PCB Tolerances of +/- 10% are supported but are not a factor in determining the fit of the CPU Backing Plate when the HPMs are mounted to standoffs by their bottom surfaces.

Implementors Note:

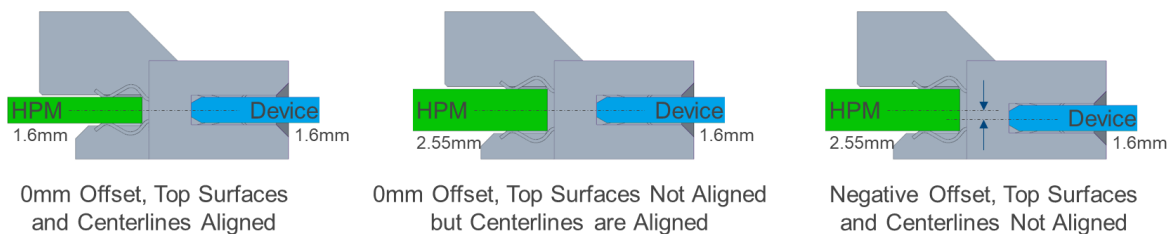
Offset connector choices and requirements may vary if a common chassis design needs to support varying HPM thicknesses. For the M-DNO specification, this could include connectors for OCP NIC R3 and DC SCM R2.

Failure to choose the proper offset could result in peripheral card not aligning to the chassis opening, demonstrated by card alignment in the Figure below.

There is no recommendation for connector offset for MHS compliance. Connector offset is out of scope of DC-MHS HPM specifications.

Connector offset is a BOM (bill of material) choice by the system designer or HPM designer.

Refer to the latest OCP NIC 3.0 and DC-SCM 2.x specifications for a list of connector choices available at the time those specifications were published. Refer to connector vendors for the latest connector offset options.

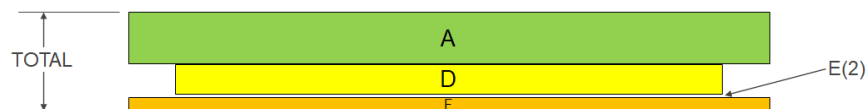
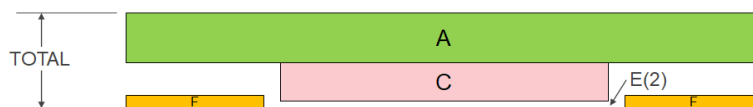


Implementors Note:

HPM and Chassis designers should consider the height stack-up of each of the 4 zones identified in **Section 10.3. Table 2** and **Figure 18 - Figure 21** demonstrate an example of a compliant stack-up for consideration. Note that the “total Z” value across the 4 zones must always be equivalent (maximum allowed value of 6.2mm shown for example only).

Table 2: Example Z-Height Compliant Stack-Up, Per Zone

		Zone 1	Zone 2	Zone 3	Zone 4	
Item	Description	Z Value (mm)	Z Value (mm)	Z Value (mm)	Z Value (mm)	Notes
A	HPM	3.18	3.18	3.18	3.18	MAX Thickness (w/o Added tolerance, Assumes bottom mounting)
B	Bottom Component Z	1.60	0			MAX Height
C	CPU Backing Plate				2.94	MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray
D	HPM Bottom Support			2.12		HPM Support Thickness +/- 0.10mm, must exceed Bottom Component Z
E(1)	Needed Gap	0.62	0.58			Gap is Larger, Requires Insulation and/or Clearance
E(2)	Resultant Gap			0.10	0.08	Gap is Small, Contact between Parts is either Desired or Permissible
F	Board Pan	0.80		0.80		
G	Chassis Hook		2.44			MAX Height from Inside Surface of Chassis
	TOTAL	6.2	6.2	6.2	6.2	Example Solution Stack-up

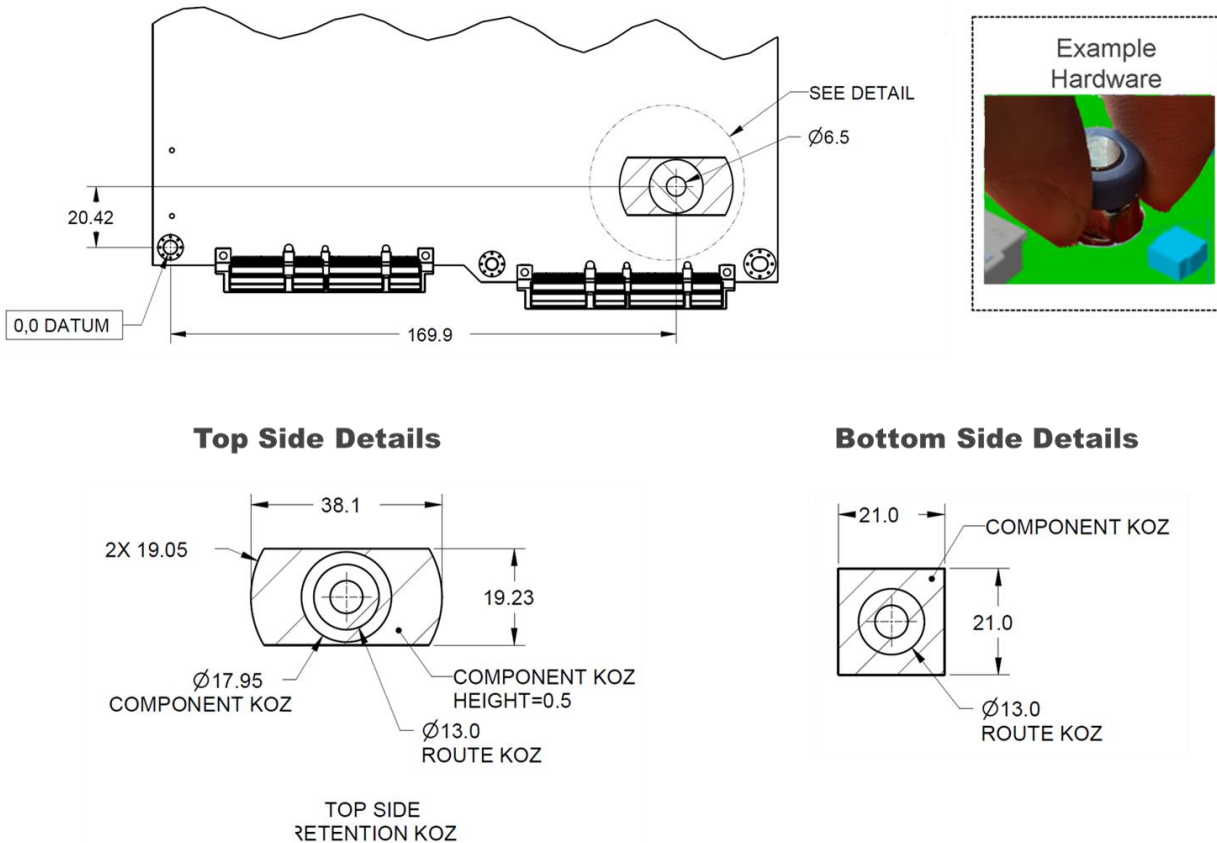
Figure 18: Secondary Side Components (Zone 1)**Figure 19: Chassis Hook Keepouts (Zone 2)****Figure 20: HPM Secondary Support (Zone 3)****Figure 21: CPU Backing Plate (Zone 4)**

10.5. HPM to Chassis Retention Mounting

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base.

There shall be a hole required for motherboard retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc. Hole Size, required Primary / Secondary side KOZs and height restrictions around this hole are defined in **Figure 22**.

Figure 22: HPM Assembly to Chassis Retention Enablement



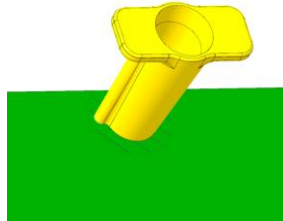
Implementors Note:

The wide shaped top side 0.5mm Height Restriction in **Figure 22** is in place for finger grip allowances around the retention hardware (which could be a plunger, thumbscrew, wing screw, etc.). Due to hardware and touchpoints being in this area, the goal is to minimize the size of components that could potentially be damaged by fingers coming in close contact to the board surface.

10.6. HPM Handle Hole

The HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with, but is not limited to, a plastic handle. An example is shown in **Figure 23**.

Figure 23: Example Board Handling Feature



Implementors Note:

While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

The hole location shall be near the Far side edge of the HPM. HPM Designers may choose to either:

1. Replace a required mid-board mounting hole along the Far Side edge (1 hole choice on Type 2 / Type 3, 2 hole choices on Type 4) with the board handle hole. **Figure 24** demonstrates this using a Type 2/3 board for example purposes.

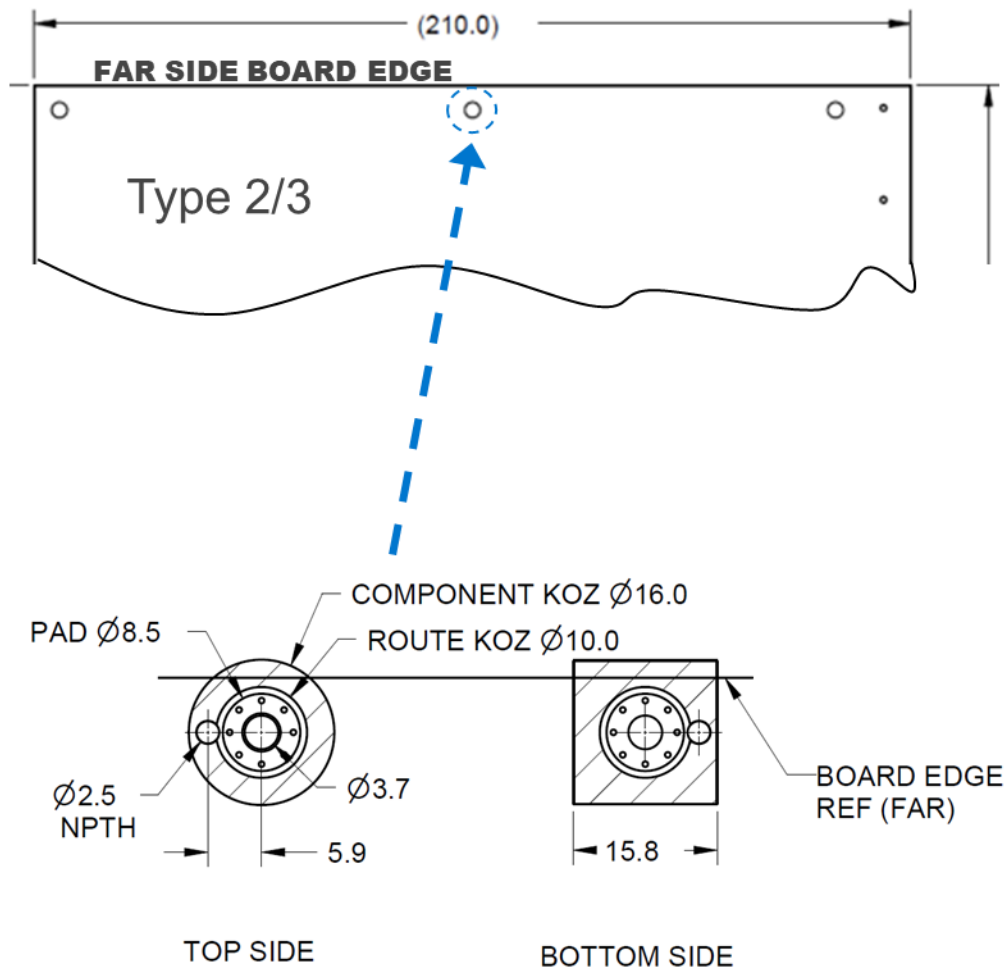
OR

2. Add an additional hole near the Far Side Edge with consideration for Compute Core Details such as cabling for HSIO.

The Board Handle hole may also be considered a mounting hole for structural purposes. For example, a designer does NOT need to place a board mounting hole in close proximity to the Board Handle Hole.

The board handle hole shall follow the required dimensions and KOZ in **Figure 24**.

Figure 24: Geometry and KOZ for HPM Handle Hole and Optional Placement Location



10.7. OCP NIC R3 and DC-SCM R2 at Near Edge Locations

665 This specification defines fixed placement for certain peripheral connectors to maximize reuse across designs.

These fixed peripheral subsystem connectors are OCP NIC R3.0 and DC-SCM R2.x.

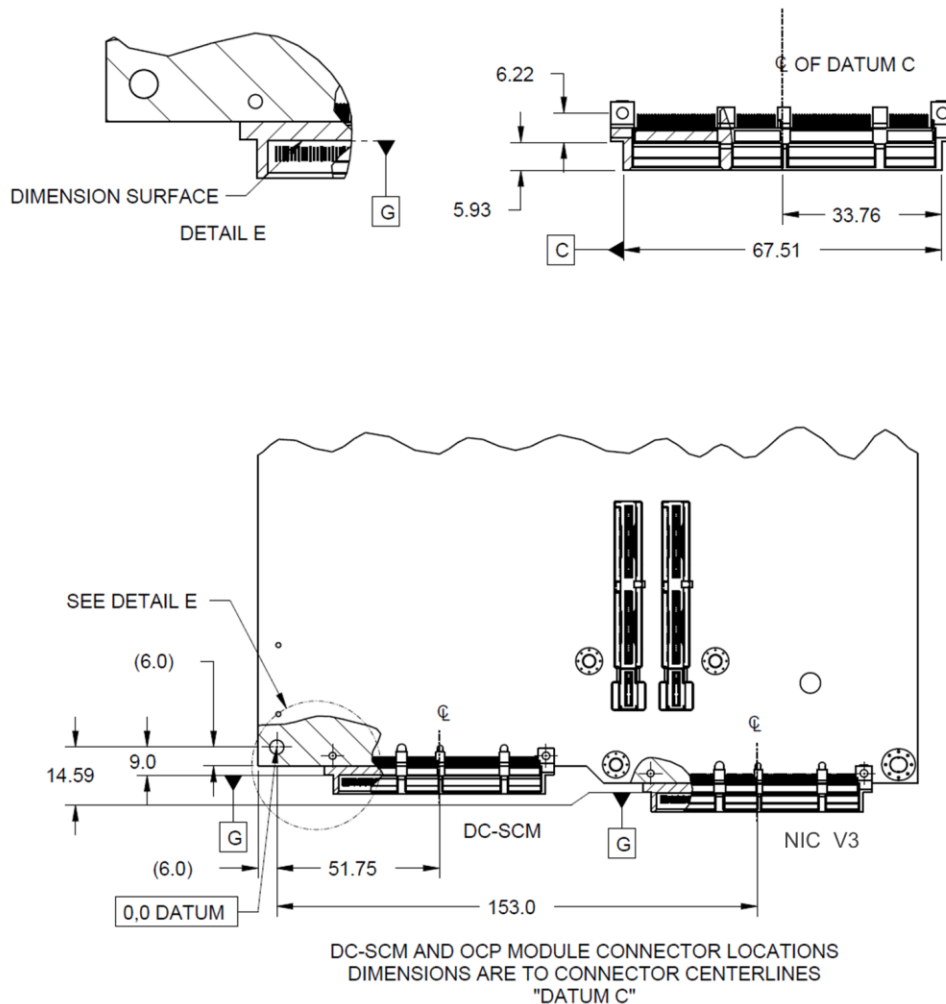
Each of these peripherals leverages connectors defined by SFF-TA-1002, including centerline definitions referenced in the Figures of this specification (Refer to the DC-MHS Connector List for vendor part number details).

The DC-SCM R2.x connector is required and shall be placed as defined in **Figure 25**.

The HPM shall implement battery backed voltage interface per DC-SCM R2.x “Battery Voltage” requirement.

675 The OCP NIC R3.0 connector is strongly recommended, if implemented, it shall be placed as defined in Figure 25.

Figure 25: Locations of OCP NIC 3.0 and DC-SCM 2.x



680 10.8. Platform Infrastructure Connector Placement

10.8.1. Connector Requirements

The electrical implementation for each connector shall follow the M-PIC specification.

Internal USB

- **M-PIC Section Reference:** “Internal USB3 Connector”
- 685 • **Connector Requirement:** Shall be Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Type A or C USB Compliant. It is strongly recommended that HPMS implement a Type A connector.

Intrusion Switch

- 690 • **M-PIC Section Reference:** “Intrusion Switch”
- **Connector Requirement:** Shall be Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

Boot Storage

- 695 • **M-PIC Section Reference:** “Boot Storage”
- **Connector Requirement:** Recommended
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

700 Due to HPM layout density it is expected that the Cable Optimized connector will be more prevalent in M-DNO designs. Type 4 M-DNO HPMS may choose to utilize the platform custom zone to enable the Direct Attach Boot Storage option.

Control Panels

- **M-PIC Section Reference:** “Control Panel Interfacing”
- **Connector Requirement:** Primary Shall Be Required (may de-pop), Secondary Optional
- 705 • **Connector Placement:** Recommended fixed location provided, expanded zone allowed
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

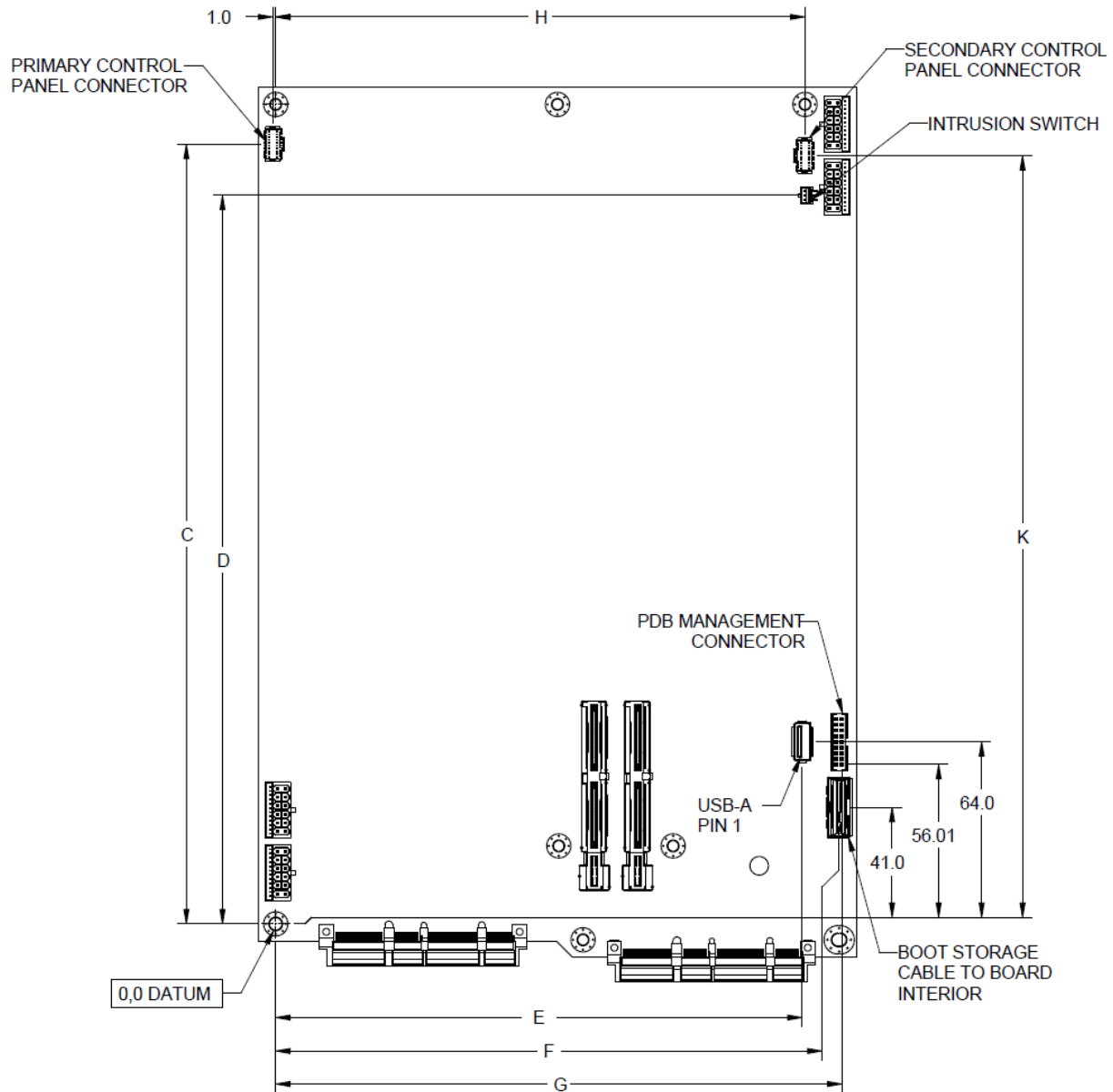
PDB Management Connector

- **M-PIC Section Reference:** “PDB Management Connector”
- **Connector Requirement:** Shall Be Required (may be de-populated)
- 710 • **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and DC-MHS Connector List

10.8.2. Connector Placement Zones and Recommended Placements

715

Figure 26: Platform Infrastructure Connector Recommended Placements



MISCELLANEOUS CONNECTORS							
	DIMENSION						
	C	D	E	F	G	H	K
TYPE	MID	MID	MID	MID	PIN 1	MID	MID
2	274	256	185	198	200	186	270
3	524	506	185	198	200	186	520
4	274	256	270	283	285	271	270

Figure 26 depicts the recommended location of the miscellaneous connectors defined in the M-PIC specification which are relevant to M-DNO HPMs. Additional information on these connectors is available in **Section 10.8.1**.

Note that a Type 2 board is represented but applicable dimensions are provided for all board types. These dimensions are intended to provide recommended connector locations that are consistent relative to the closest board corner across all board types.

To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 27 – Figure 29** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone. Note that the intrusion switch can share either the primary or secondary control panel zone.

Figure 27: Intrusion, Control Panel, USB and PDB Management Placement Zones

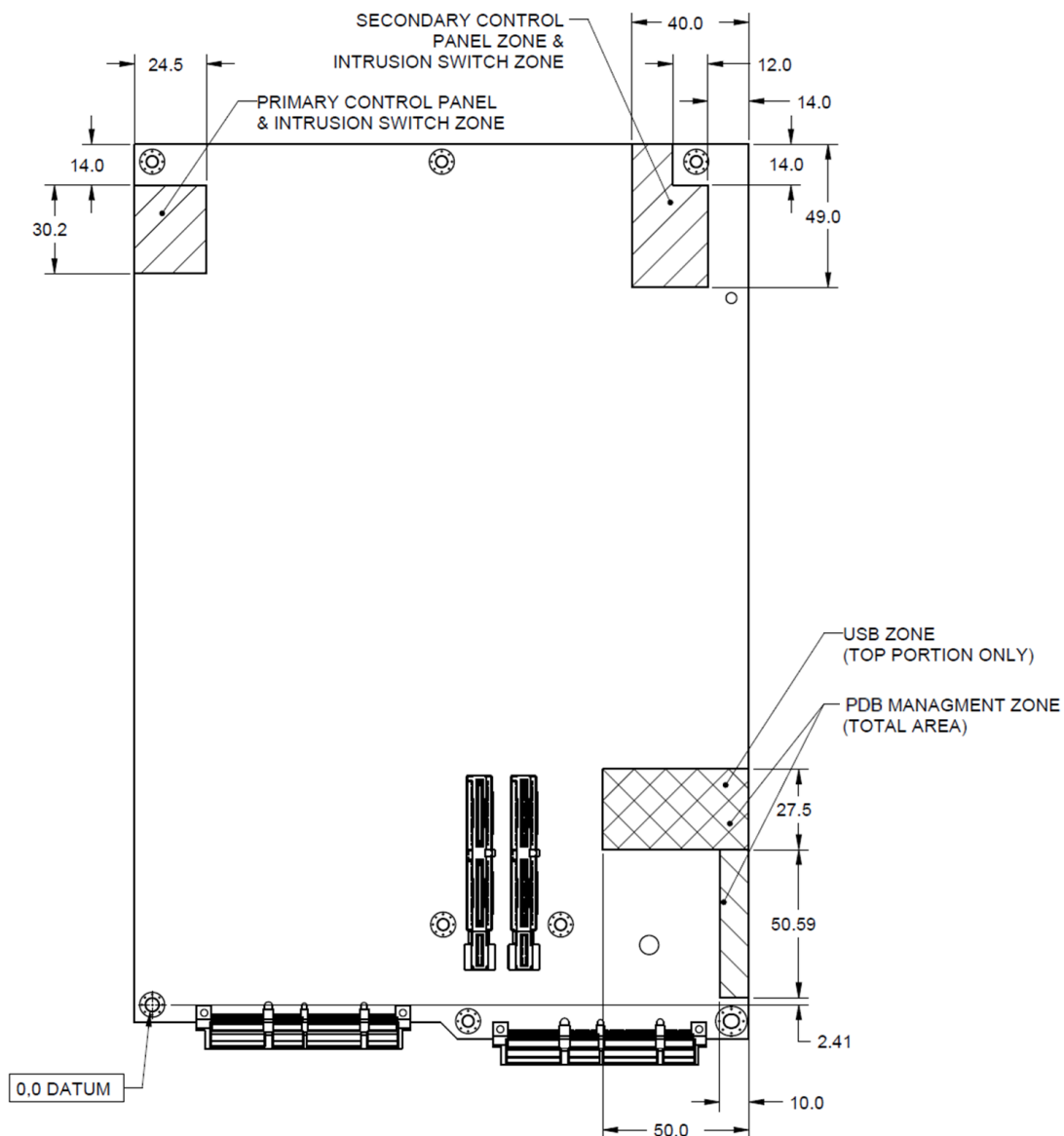


Figure 28: Cabled Boot Storage Placement Zone Type 2/3

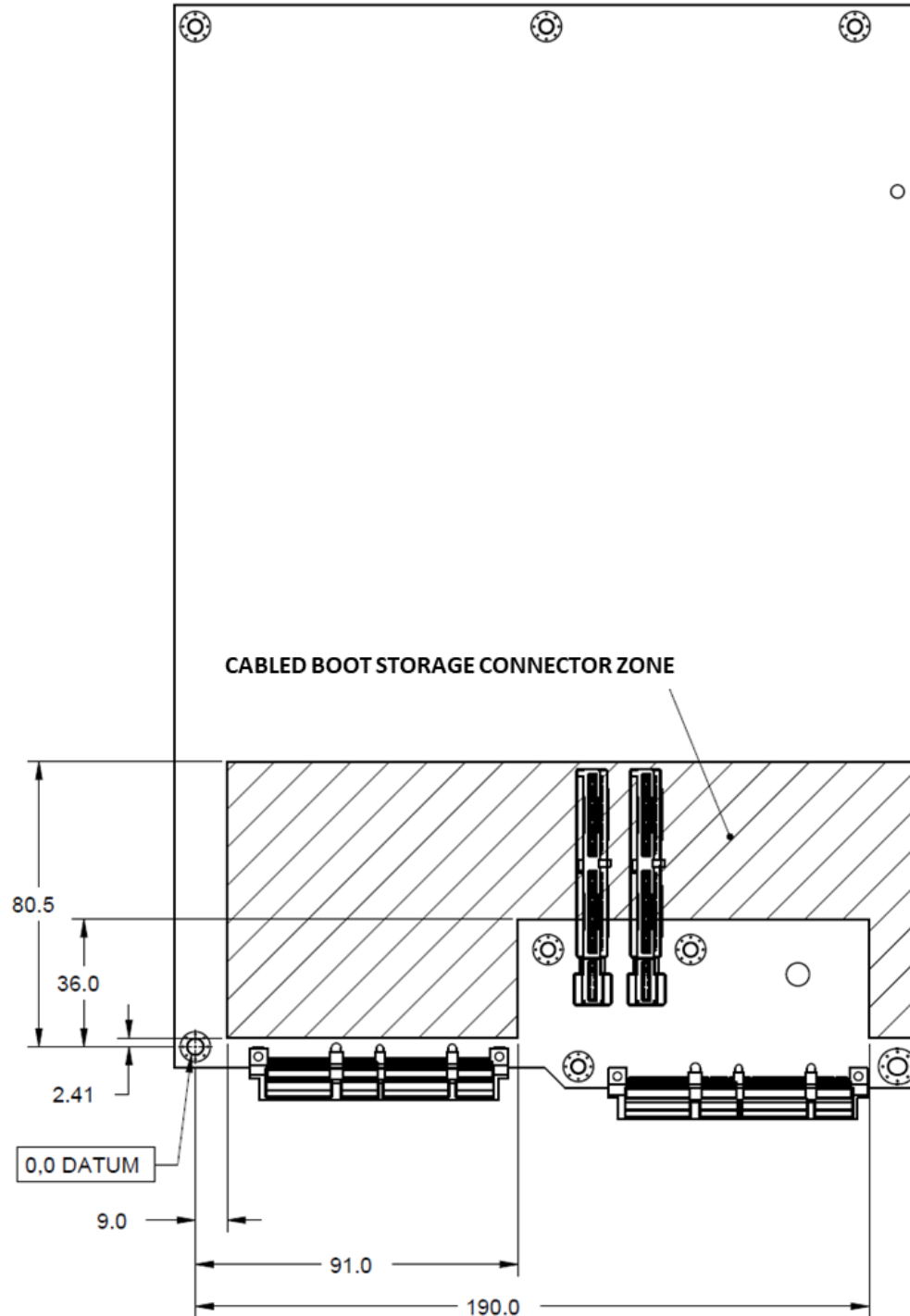
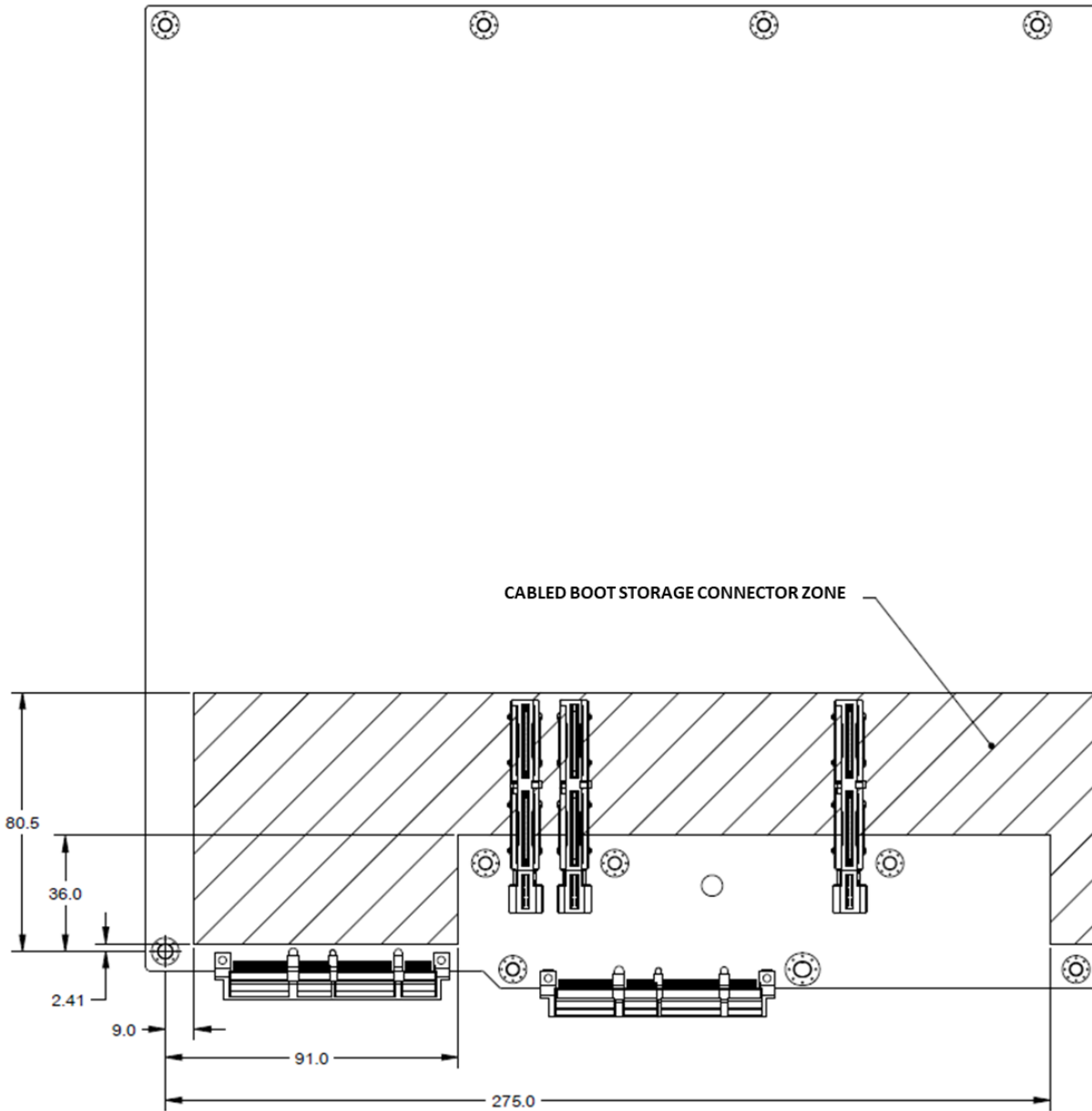


Figure 29: Cabled Boot Storage Placement Zone Type 4



735

10.9. High Speed I/O (HSIO) Connectors

This base specification seeks to allow for flexible high speed I/O (HSIO) routing options while also enabling HPM to system compatibility.

740 Board-to-Board (B2B) connections are defined as connections that mate two separate PCBs entirely without cabling. B2B connections are typically used to route HSIO from the HPM to a riser PCB or direct dock peripherals (i.e. DC-SCM R2.x, OCP-NIC R3).

Board-to-Cable (B2C) connections are defined as connections that mate two separate PCBs entirely with cabling. B2C connections are typically used to route HSIO from the HPM to a riser PCB or to other subsystems such as NVMe storage devices or backplanes.

745 Hybrid connections are defined as those which utilize both B2B and B2C elements to create a single mated interface between two PCBs. For example, if a Riser has a PCB with card edge fingers utilizing B2B to receive Power and Low Speed IO while also using a Twinax B2C connection for HSIO.

Implementors Note:

SFF-TA-1033 is an example of a connector supporting Hybrid connections, it can be used for B2B, B2C or Hybrid connections. While the HPM designer places the SFF-TA-1033, they do not necessarily know beforehand what style of connection the System designer will implement.

B2C

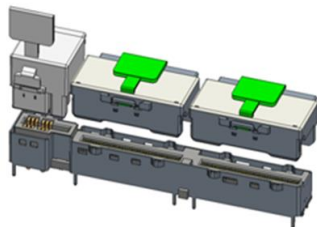


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

B2B

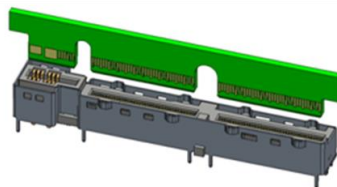


Figure 4-1 Combo x16+21A Power AIC Application

Hybrid

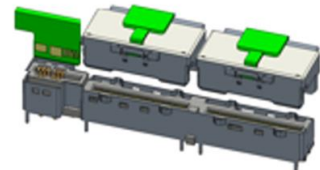


Figure 4-5 Separate RA 74 Pin Cables and a RA 21A Power Cable Application

750 10.9.1. DC-MHS Compliant HSIO Connectors

All HSIO connectors shall be compliant with the M-XIO specification and be listed in **Table 3**. Refer to the **DC-MHS Connector List** for vendor part number details.

755

Table 3: M-SDNO Specification Compliant HSIO Connectors

760

Use	Compliant Connectors
Near Side Fixed Risers Locations	SFF-TA-1033 (with 21A Power)
All Other HSIO	SFF-TA-1016 SFF-TA-1026 SFF-TA-1033

765

Note: Additional connectors may be added to future revisions of this specification *after* electrical definition by M-XIO.

DC-MHS HPMs allow for B2B, B2C or Hybrid risers. For best compatibility with many DC-MHS system designs, HPMs should implement riser connectors adhering to the guidance in **Section 10.9.2**.

770

All other HSIO connectors adhere to common guidance in **Section 10.9.3**.

Implementors Note:

HSIO cable choices are outside the scope of M-SDNO. The SFF-TA-1016 and SFF-TA-1033 connectors can accept both cable types but mixing cable/connector types may result in loss of the anti-tilt feature.

10.9.2. Near Side Fixed Riser Connectors

775 A DC-MHS riser may utilize B2B, B2C or Hybrid connectivity schemes. Riser and other endpoint device definition and implementation details are outside of the scope of this specification.

To enable chassis and I/O subsystem compatibility and reuse, fixed riser locations are defined with consistent locations across all M-DNO Types:

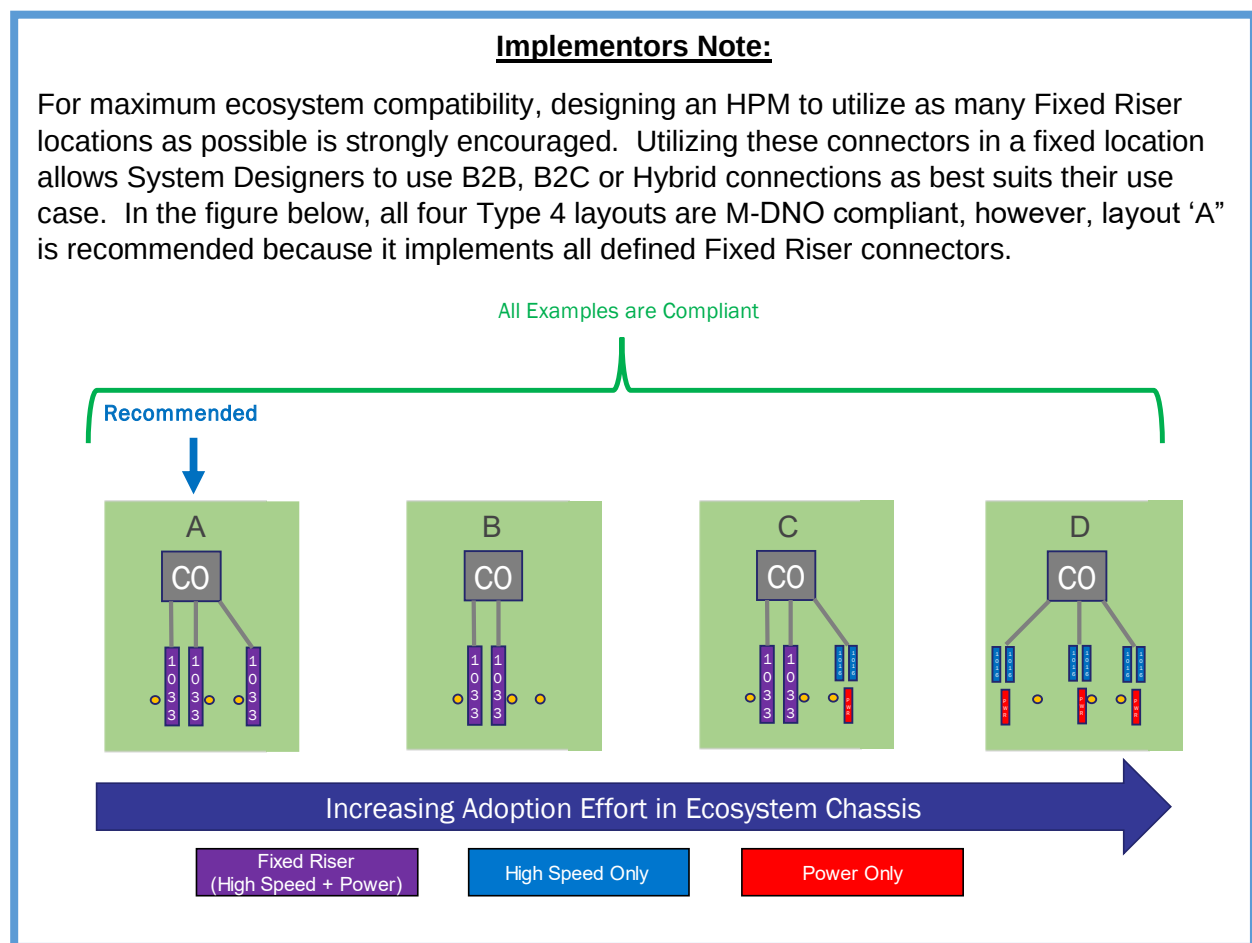
- 780
- Type 2 supports riser locations 1 and 2.
 - Type 3 supports riser locations 1 and 2.
 - Type 4 supports riser locations 1, 2 and 3.

HPMs which implement near side fixed risers shall:

- 785
- Use a Fixed Riser connector defined in **Section 10.9.1**
 - Place them in the location(s) defined in **Section 10.9.2.1**

Full population of all Near Side Fixed Risers Locations is not required, as there may be technical or other reasons to exclude certain positions. It is recommended to implement as many fixed riser locations as possible.

790

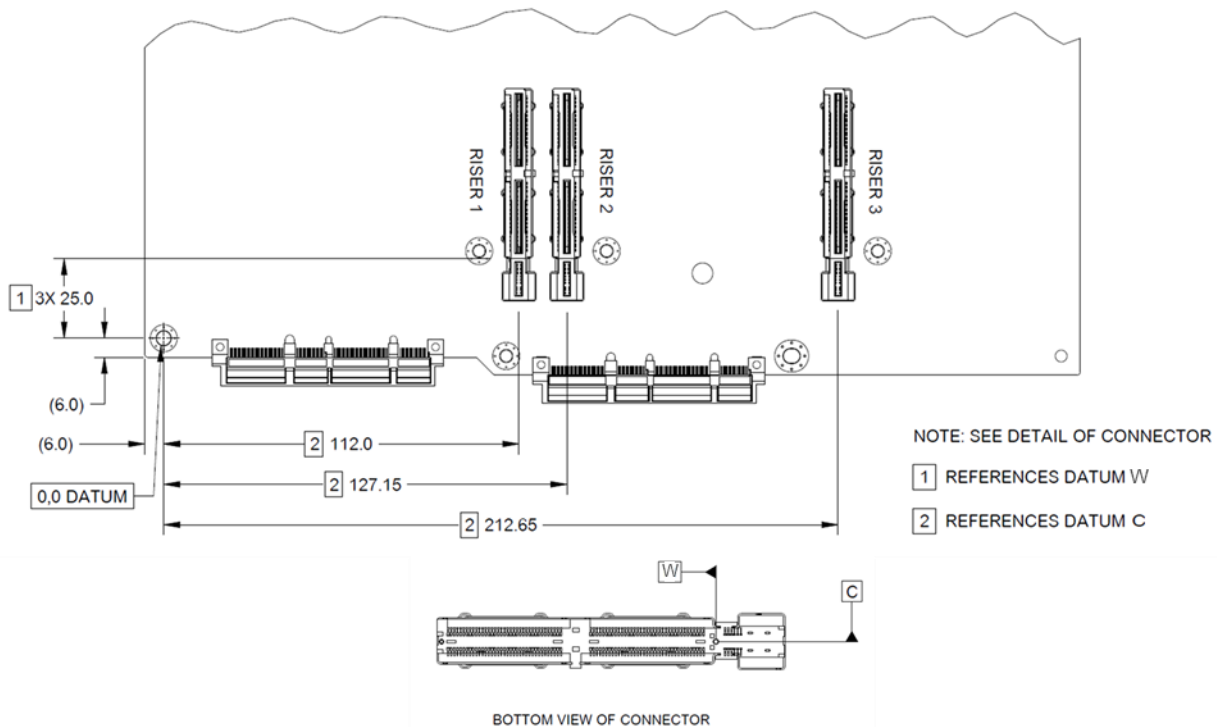


10.9.2.1 SFF-TA-1033 Fixed Riser Implementation Details

SFF-TA-1033 fixed riser connectors which are implemented shall follow **Figure 30** which define the required location of the SFF-TA-1033 connectors.

Note that SFF-TA-1033 has various versions. All SFF-TA-1033 Near Side Fixed riser connectors shall use a 21A power block version. Refer to the **DC-MHS Connector List** for vendor part number details.

Figure 30: Required Riser Locations with Recommended Connector



10.9.3. Other HSIO Connectors

Except for the Fixed Riser Connectors described in **Section 10.9.2**, HSIO connector positions and quantity are not defined by this DC-MHS base specification. The HPM Designer is free to place them wherever they wish so long as they do not interfere with other required features (e.g. a required mounting hole) and while adhering to the component height restrictions in **Section 10.10**.

All implemented HSIO connectors shall be defined in M-XIO and listed in **Table 3**. Any combination of these connectors is allowed.

10.10. Primary Side Component Height Restrictions and KOZs

All M-DNO board types shall adhere to a common approach of three different component height restriction zones as shown in **Figure 31 and Figure 32**.

- The **12mm Zone** is intended to allow for extended heatsinks and other thermal solutions while not prohibiting cabling of HSIO. Adherence to the 12mm zone is *strongly recommended*. While deviations are allowed, HPM designers should limit component selections which exceed the restriction to reduce interference with system design elements which will expect to inhabit this space and may cause system compatibility issues.
- The **11.3mm Zone** is intended to avoid interference with PCIe CEM cards directly above the HPM and its peripherals. Adherence to the 11.3mm Zone shall be required.
- The **6mm Zone** is the most restrictive and is intended to prevent interference with mechanical elements in support of the fixed riser locations and retention holes. Adherence to the 6mm Zone shall be required.

Zone height restrictions shall apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of soldered components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

Allowed exceptions to these zones are:

- DIMM connectors
- Connectors in specified Fixed Riser locations (**Section 10.9.2**)
- Plugs to connectors placed by this specification (e.g. vertical PICPWR or USB plugs)
- SFF-TA-1016 and SFF-TA-1026 connectors may be placed in the 11.3mm and 12.0mm Component Height Restriction Zones. The mating plugs for these connectors may exceed the HRZ depending on which connectors and plug types are chosen. As a result, an exception is allowed for these two connector types in the 11.3mm and 12.0mm HRZs. HPM designers should place these connectors with careful consideration of potential system use cases for their HPM

Note that Near IO connectors outside the specified Fixed Riser locations are NOT exempt and should adhere to the defined zone restrictions. This specification does not specify a specific Keep Out Zone for cable enablement.

Implementors Note:

The height exception for the SFF-TA-1016 & SFF-TA-1026 connectors based on an understanding that a system design layer exists between the HPM HRZs (Layer A) and the Major Component Layer of a system (Layer C). Layer B is a mechanical design layer where cabling may route and sheet metal structures may be created in the system's chassis design. A system designer needs to understand the mated heights of plug + receptacle for the SFF-TA-1016 and SFF-TA-1026 connectors to be able to accommodate their occasional and purposeful intrusions into Layer B.

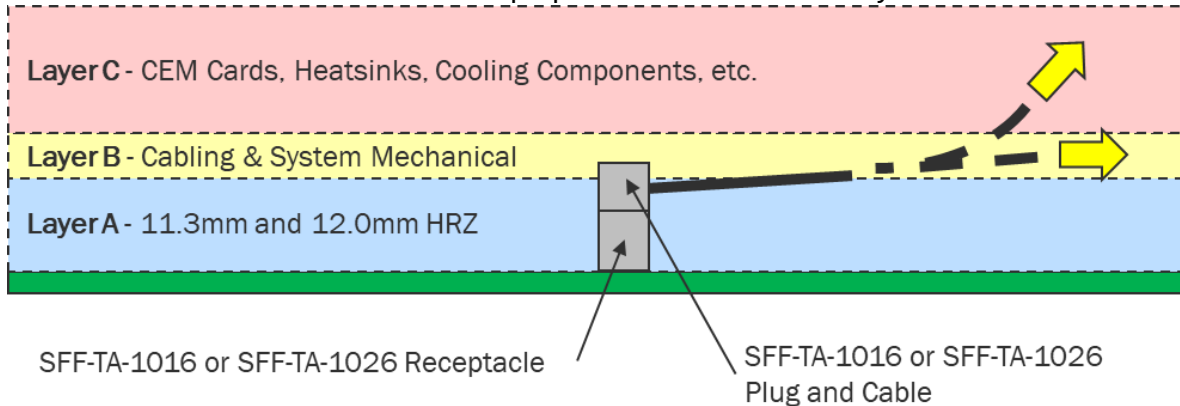
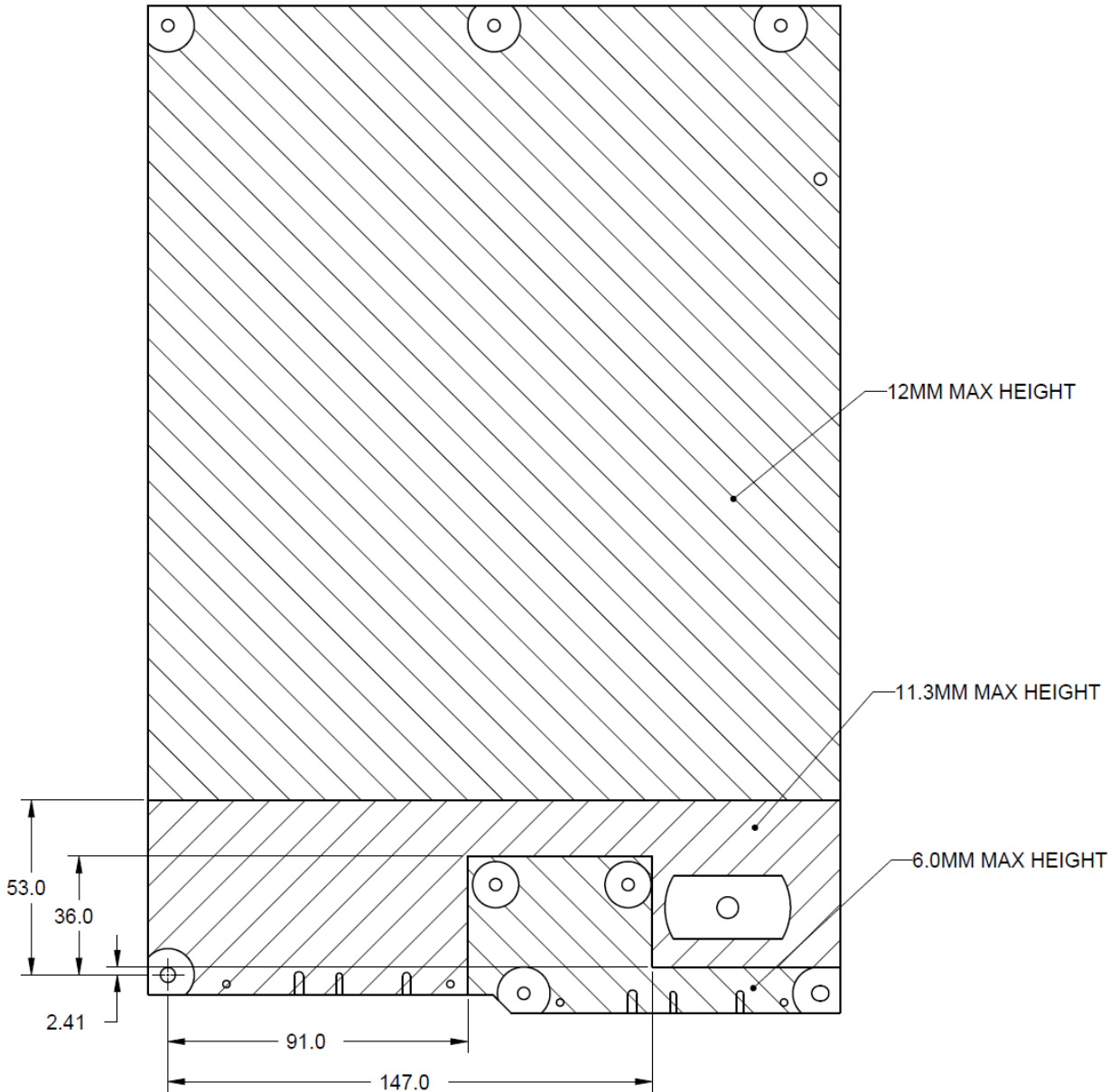
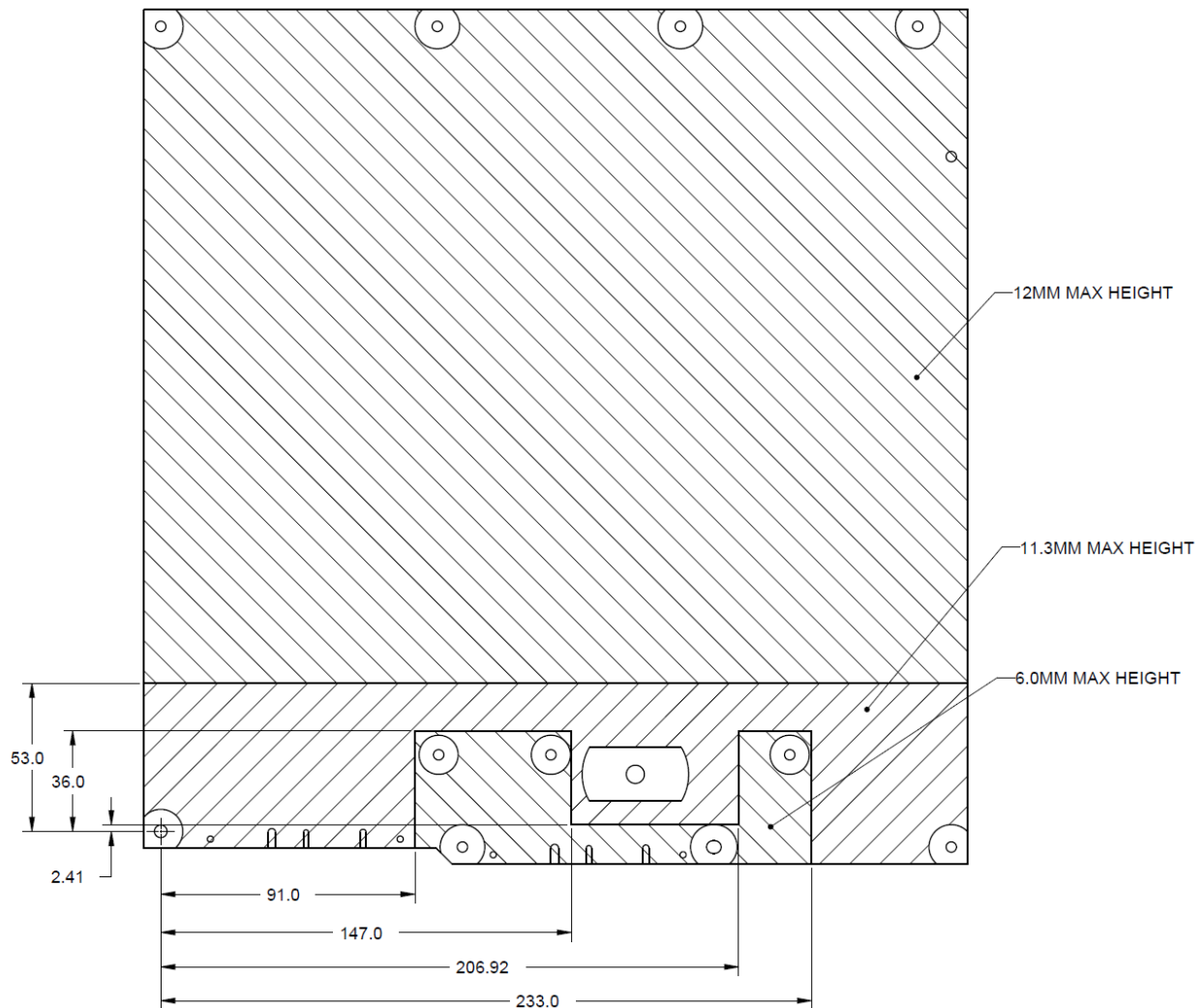


Figure 31: Type 2 and 3 Primary Side Component Height Restriction Zones



850

Figure 32: Type 4 Primary Side Component Height Restriction Zones



10.11. Platform Custom Zone (Type 4 Only)

855 The Platform Custom Zone (PCZ) is defined as the Near HPM Edge between the Far side of the OCP NIC R3 and the board edge. This area is intentionally undefined, so that System Designers may provide their desired features for the target platform.

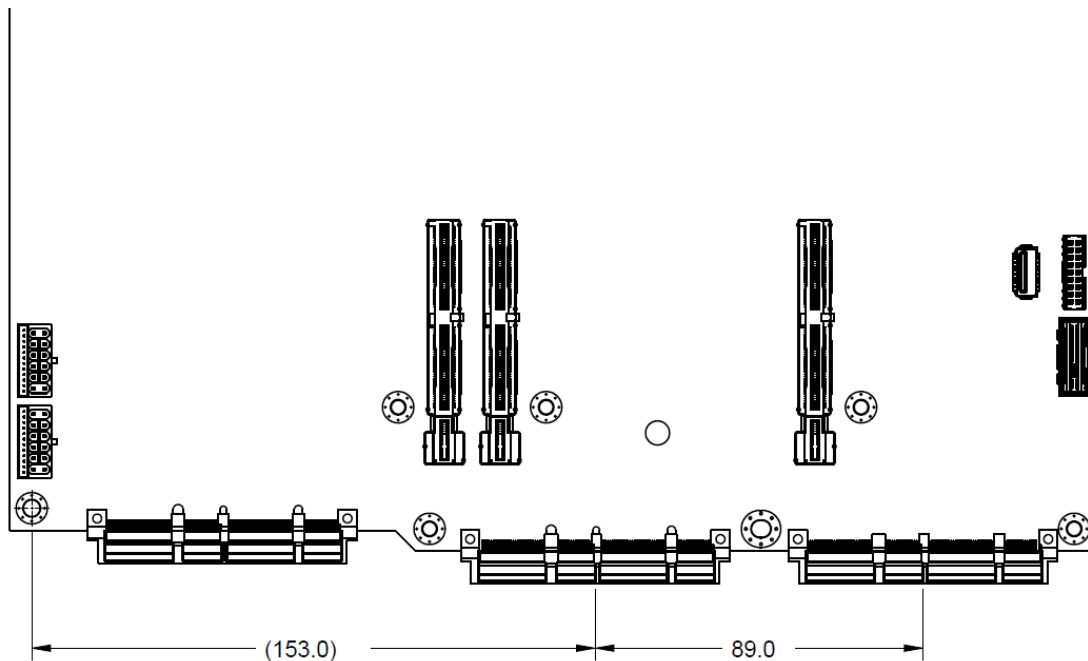
Only Type 4 HPMs support a PCZ (See **Figure 2: M-DNO Board Type Layout Overview**).

860 The specification defines some options that are considered common use cases, to promote greater compatibility between future HPMs.

10.11.1. Second OCP NIC R3

An HPM design may want to support a second OCP NIC R3. These HPM designs should follow the placement guidance in **Figure 33** for the second connector.

865 **Figure 33: Second OCP NIC in Custom Zone**

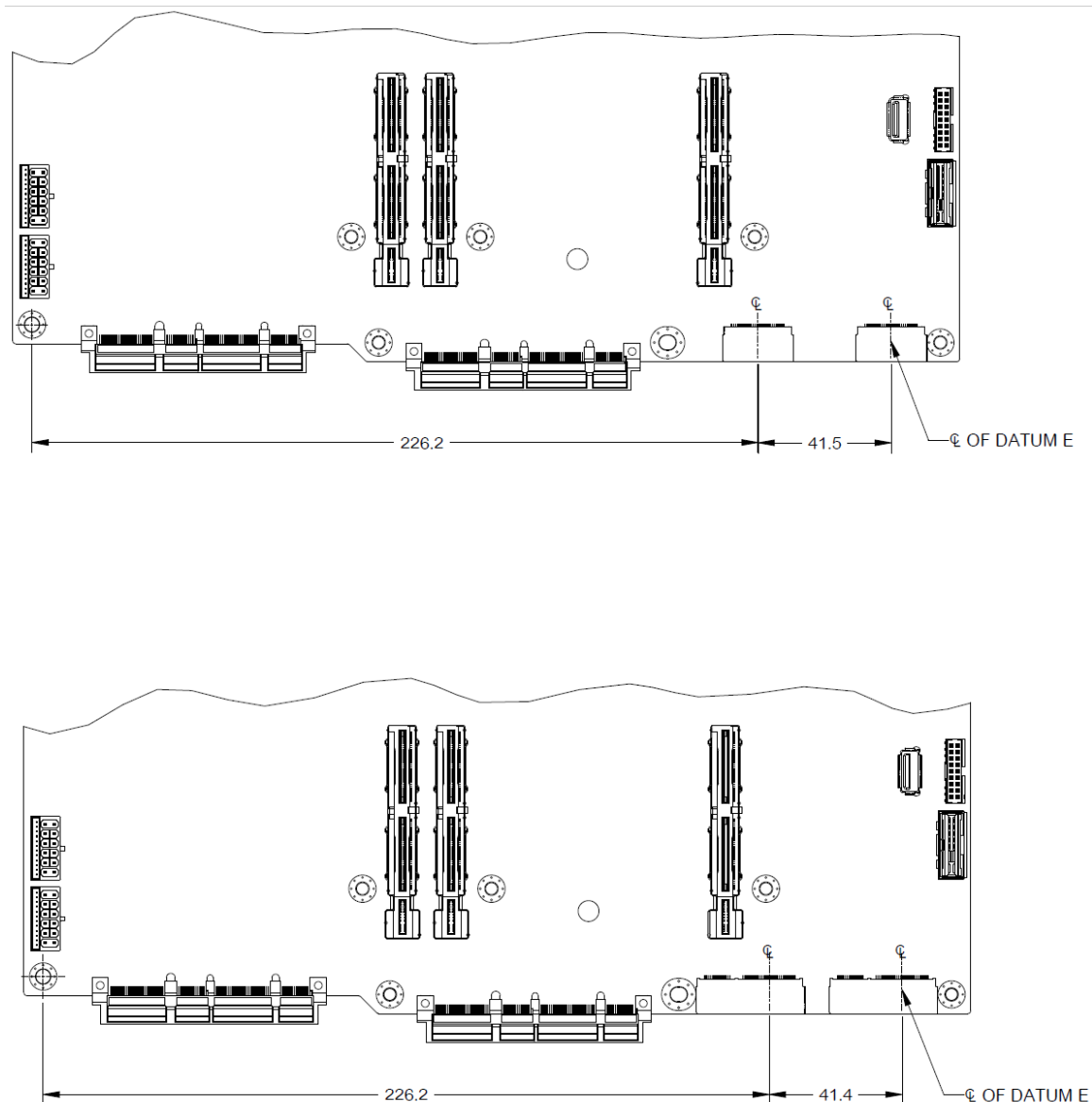


10.11.2. Direct Dock E1.S

870 An HPM design may want to support direct docking E1.S (EDSFF) in the Platform Custom Zone. These HPM designs should follow the placement guidance for SFF-TA-1002, 1C connectors in **Figure 34**. See M-PIC specification, chapter “E1.S Direct Attach Boot Storage” for complete connector and pinout guidance.

875 Note that dimensioning has been changed to reference the centerline of Datum E in the SFF-TA-1002 connector specification. Additionally, the defined location allows for either 1C or 2C connector variants to be placed.

Figure 34: Direct Dock E1.S in Custom Zone



11. Power Zones

880 M-DNO compliant HPMs are assumed to Ingress / Egress 12V DC. While alternate voltages are under consideration for future versions (e.g. 48V DC implementations), this version assumes the burden for alternate power sources is placed on the system power delivery infrastructure (PDB, bus bar, etc.). For information on Power Management (including Power Gating and use of sideband signals) refer to the M-PIC specification.

Implementors Note:

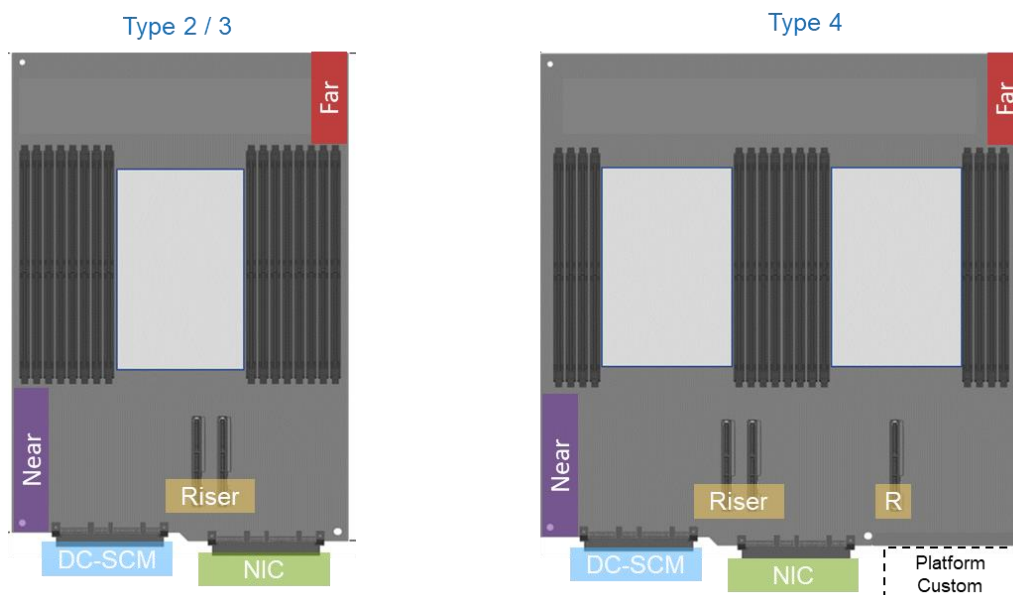
The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in private and/or public HPM design specification(s) for system configurations supported per HPM design.

885 11.1. HPM Power Zone Overview

To enable a variety of system power configurations (See **Section 14.2**) there are two defined bi-directional power zones for each HPM type referred to as the “Near” and “Far” Ingress / Egress zones as shown in **Figure 35**. These zones are intentionally placed in opposing corners of the HPM to maximize flexibility of system orientation.

890 Additional power zones include power egress to DC-SCM, OCP NIC and each fixed Riser location.

Figure 35: M-DNO Power Zone Overview (Type 2 and 4 Depicted)



895

11.2. Near and Far Bi-Directional (Ingress / Egress) Power Zones

Ingress / Egress Cabled Power Connector

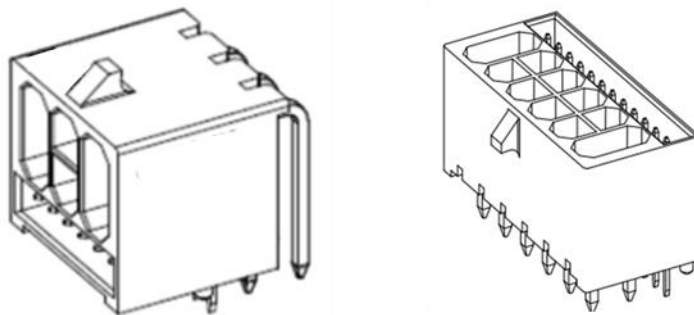
- **Power Connector Type:** 2x6+12SB and/or 2x3+6SB PICPWR .
Refer to M-PIC Specification and DC-MHS Connector List for additional details.
- **Connector Power Rating:** 864W (2x6) / 486W (2x3)
- **Typical usage:** Power ingress to HPM and / or egress to peripheral subsystems

It is assumed that most systems will provide power to M-DNO based HPMs via a cabled solution from a Power Distribution Board (PDB).

To maximize reuse of power delivery across all M-DNO HPMs, the required connectors for all Ingress / Egress power shall be the 2x6+12SB or 2x3+6SB PICPWR. An example of the 2x3+6 and 2x6+12SB is depicted in **Figure 36**.

Refer to the M-PIC specification for more information on PICPWR compliant connectors.

Figure 36: Example 2x3 + 6SB (Right Angle) and 2x6 + 12SB PICPWR Connector (Vertical)



Far Power Zone – Required

The Far Power Zone shall be required such that any system capable of providing power to the Far Zone of the HPM can provide ingress power to all M-DNO designs. While it is required for the HPM to implement this zone, the connector(s) may be depopulated.

- Two connector locations are defined for each board type in the Far Power Zone. Refer to **Section 11.7** for specific locations per board Type.
- One of the two defined locations (PICPWR-1 / PICPWR-2) is required and shall implement a 2x6+12SB PICPWR connector.
- The second location is optional and may implement either a 2x6+12SB or 2x3+6SB PICPWR connector if implemented.
- HPM designers electing to implement only a single connector may choose between either of the two specified locations.
- The far power zone connectors should be capable of meeting the full HPM power budget when used for ingress.

Implementors Note:

HPMs which implement the cabled PICPWR connectors may still be used in multi-node systems via an interposer or interface board to enable blind mate into system backplane / infrastructure. Refer to **Section 14.1** for an example of such a system.

Near Power Zone – Recommended

930 Due to the expected density of HPM designs in this area of the board, the Near Power Zone **may** be implemented at the discretion of the HPM designer. If Near zone power connectors are implemented, the connector(s) may be depopulated.

935 To increase the likelihood that this zone can be implemented, connectors may be placed anywhere within the designated zone area rather than having a fixed location. Refer to **Section 11.7** for this zone outline.

Within the defined zone any combination of 2x3+6SB and 2x6+12SB PICPWR connectors shall be allowed.

940 To maximize system use cases, it is recommended that HPM designers provide as much Ingress / Egress capability as feasible given HPM layout constraints. At a minimum, a single 2x3+6 (for egress to a peripheral subsystem) is recommended.

Implementors Note:

If providing Ingress power via the Near Power Zone is desired, it is recommended that the connector configuration matches the connector configuration of the Far Power zone in order to maximize flexibility for Power Ingress / Egress.

11.3. Fixed I/O Riser Location Power

- **Power Connector Type:** Integrated within SFF-TA-1033 Recommended Refer to M-PIC Specification and DC-MHS Connector List for additional details.
 - **Connector Power Rating:** 252W
 - **Minimum Power Delivered to Connector by HPM:** 87W
- Typical usage:** Power egress for 1 (required) or more (optional) 75W PCIe CEM Devices per Riser

For each **implemented** fixed riser location (up to three):

- HPMs shall deliver a minimum of 87W of power to the riser connector (See **Table 4** for calculation of 87W effective total power required *per slot*). This requirement is defined to guarantee each riser location can support a minimum of one 75W PCIe CEM card and reduce power cabling requirements in dense systems.
- HPMs may deliver additional power to the riser connector to enable additional cards at each riser location.
- Additional supplemental I/O power (e.g. auxiliary power for a GPU) is not defined and is assumed to be provided directly by system infrastructure (e.g. cable from PDB).
- I/O Risers shall comply with M-PIC PICPWR sideband signaling requirements.

Table 4: Minimum HPM Power Provided to Fixed Riser Locations

Power Rail	75 W Slot ¹
+3.3Vaux	Generated on PCIe riser. Derived from +12V
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from +12V
+12V Voltage Current	12V nominal 7.25A total: 5.5 A (CEM 5.0) + 1.0A (VR conversion to V_{cc3_3}) + 0.35A (VR conversion to +3.3Vaux) + 0.40A (misc.)

11.4. DC-SCM 2.x

- **Power Connector Type:** Refer to the OCP DC-SCM R2.x spec (Refer to **Section 13**)
- **Connector Power Rating:** 50W (Refer to the OCP DC-SCM R2.x spec)
- **Typical usage:** Power egress for DC-SCM 2.x

11.5. OCP NIC 3.0

- **Power Connector Type:** Refer to the OCP NIC R3.0 spec (Refer to **Section 13**)
- **Connector Power Rating:** 80W (Refer to the OCP NIC R3.0 spec)
- **Typical usage:** Power egress for OCP NIC 3.0

11.6. Platform Custom Zone (Type 4 Only)

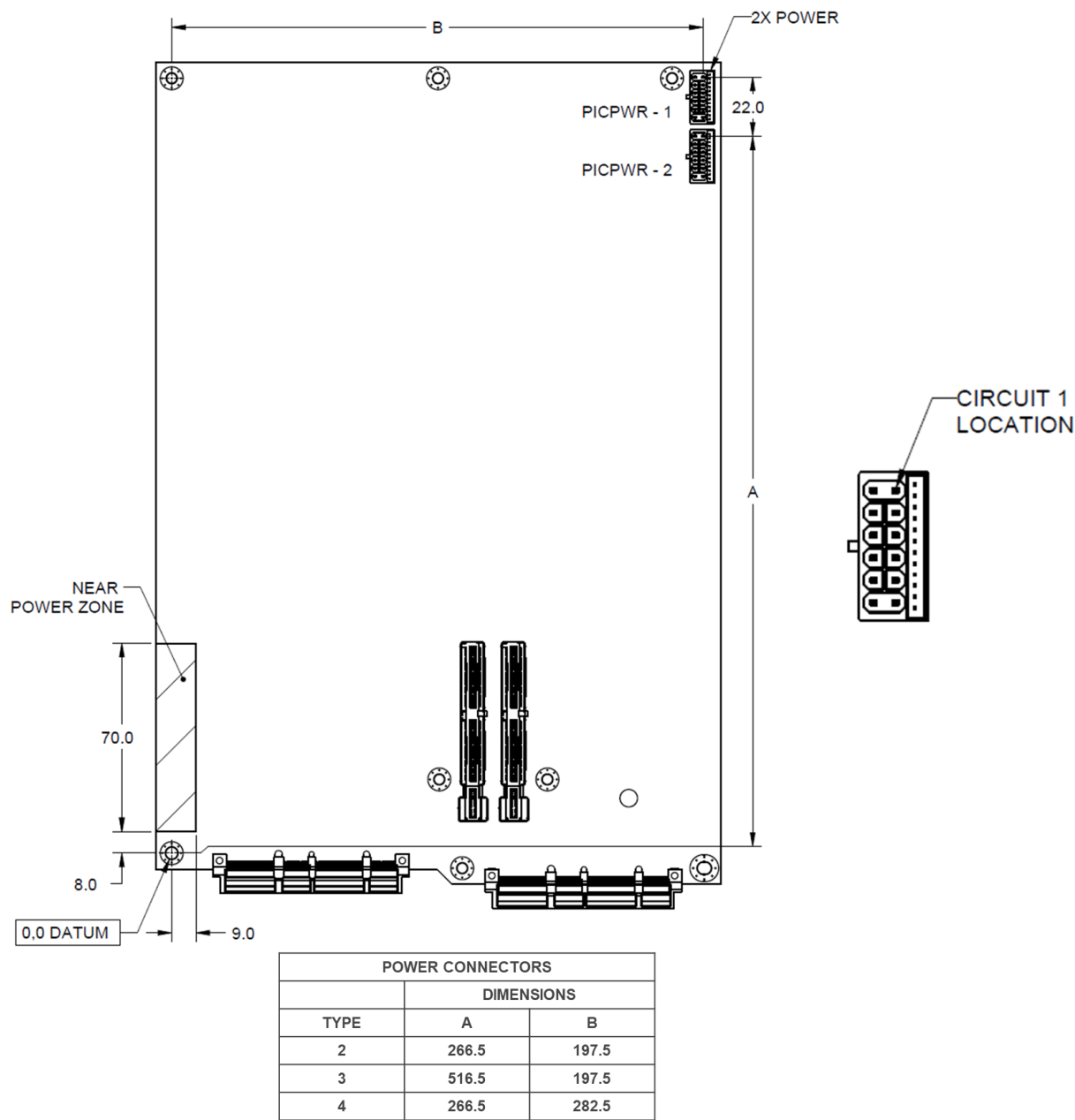
Power to the Platform Custom Zone is not defined as it is considered implementation specific.

11.7. Ingress / Egress Power Connector Locations

As described in **Section 11.1** the two Far power connector locations (PICPWR-1 and PICPWR-2) are fixed for each board type with common spacing between the two locations across all board types. Dimensioning is to Circuit 1 and is intended to be consistent for 2x6+12SB or 2x3+6SB selections.

The drawing and table within **Figure 37** shall define the required location(s) for each board type. Note that while for simplicity only a Type 2 board is depicted the dimensions listed are valid for other board types.

Figure 37: Near and Far Power Zone Connector Locations



11.7.1. **PICPWR Numbering**

It is recommended to number PICPWR connectors based on Circuit 1 location beginning at the Far Side board edge and moving towards the Near Side board edge.

For details on how to number each PICPWR connector, refer to the M-PIC specification.

12. I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details, specifically M-PIC, M-XIO, M-CRPS, and M-PESTI specifications.

1000

For information on connector placements, refer to **Section 10.8: Platform Infrastructure Connector Placement** and **Section 10.9: High Speed I/O (HSIO) Connectors**.

13. References

1005

Relevant Open Compute Specifications

This specification also relies on the following Open Compute Project specifications

1010

1. OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
Mezz (NIC) » Open Compute Project

1015

2. OCP Datacenter Secure Control Module (DC-SCM) 2.x – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
Hardware Management/Hardware Management Module – OpenCompute

Additional Industry References

1020

- ASMEY14.5 – 2018 Dimensioning and Tolerancing
- Open Rack V3
- SNIA SFF-TA-1002
- SNIA SFF-TA-1016
- SNIA SFF-TA-1026
- Open19

1025

14. Supplemental Material

14.1. M-DNO Conceptual Implementation Examples

1030 The M-DNO specification has multiple form factor types to address various product types and sizes. In this section some of the possible configurations and usages for the different Types will be shown.

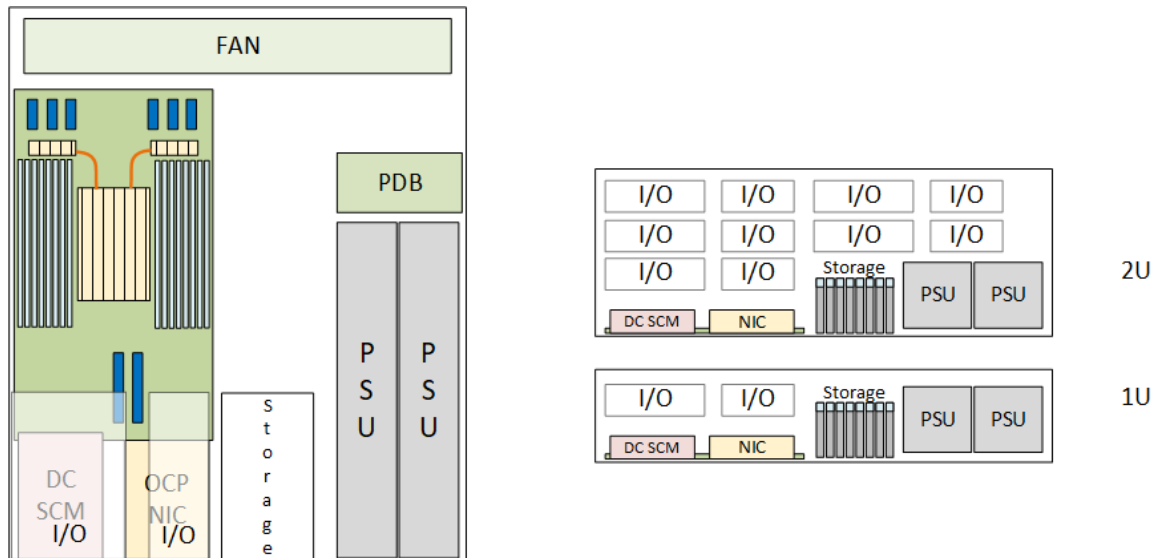
Note: Image representation of elements may not be to scale, and is subject to change

1035 It is understood that the configurations shown represents a small sample of what could be possible. This section also conveys the reasoning behind the different sizes of HPM associated with the three types.

Type 2

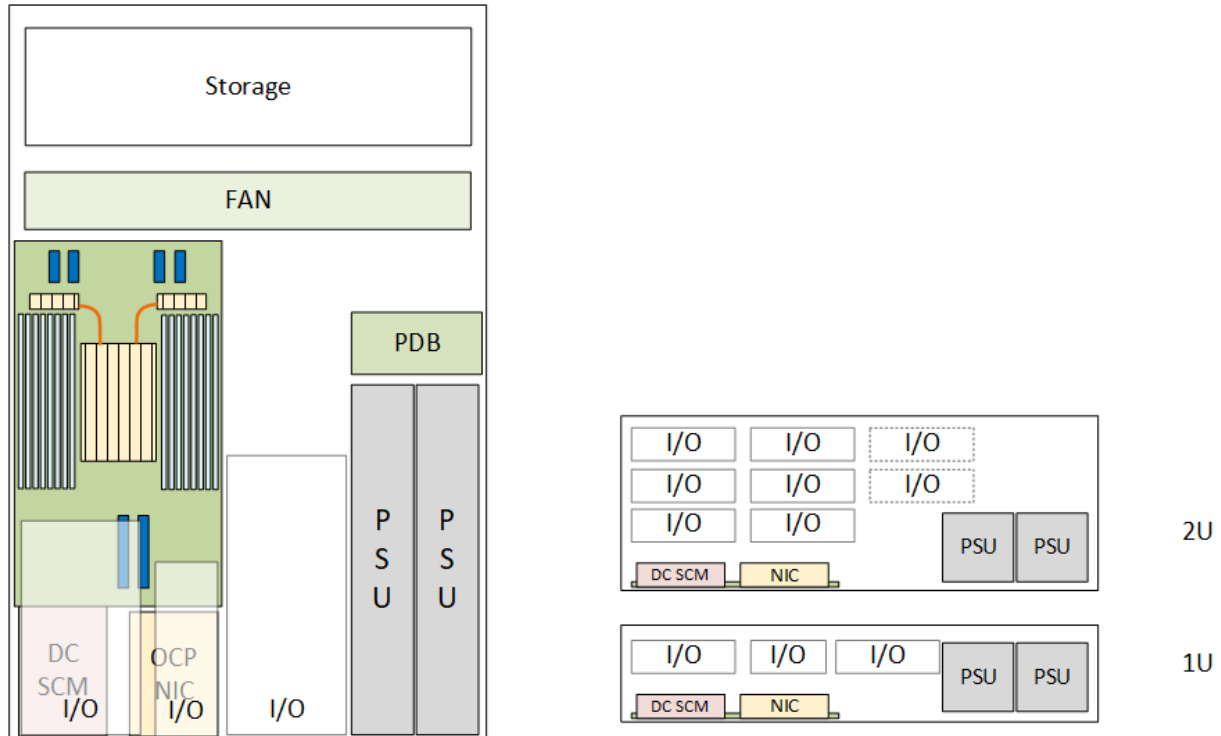
1040 The Type 2 HPM was optimized to provide an ideal solution for Dense (1/2 Width) 1 Socket designs. Type 2 is intended to support PCIe direct attach risers and EVAC thermal solutions as well as larger CPU sockets.

Type 2 Configuration Example – 1 Node Edge



- 1045 The Type 2 HPM would also be applicable for traditional enterprise server applications in or 1U or 2U heights. The variability of capabilities for I/O and Storage would be plentiful and facilitated by different riser, cable, and mid-plane configurations.

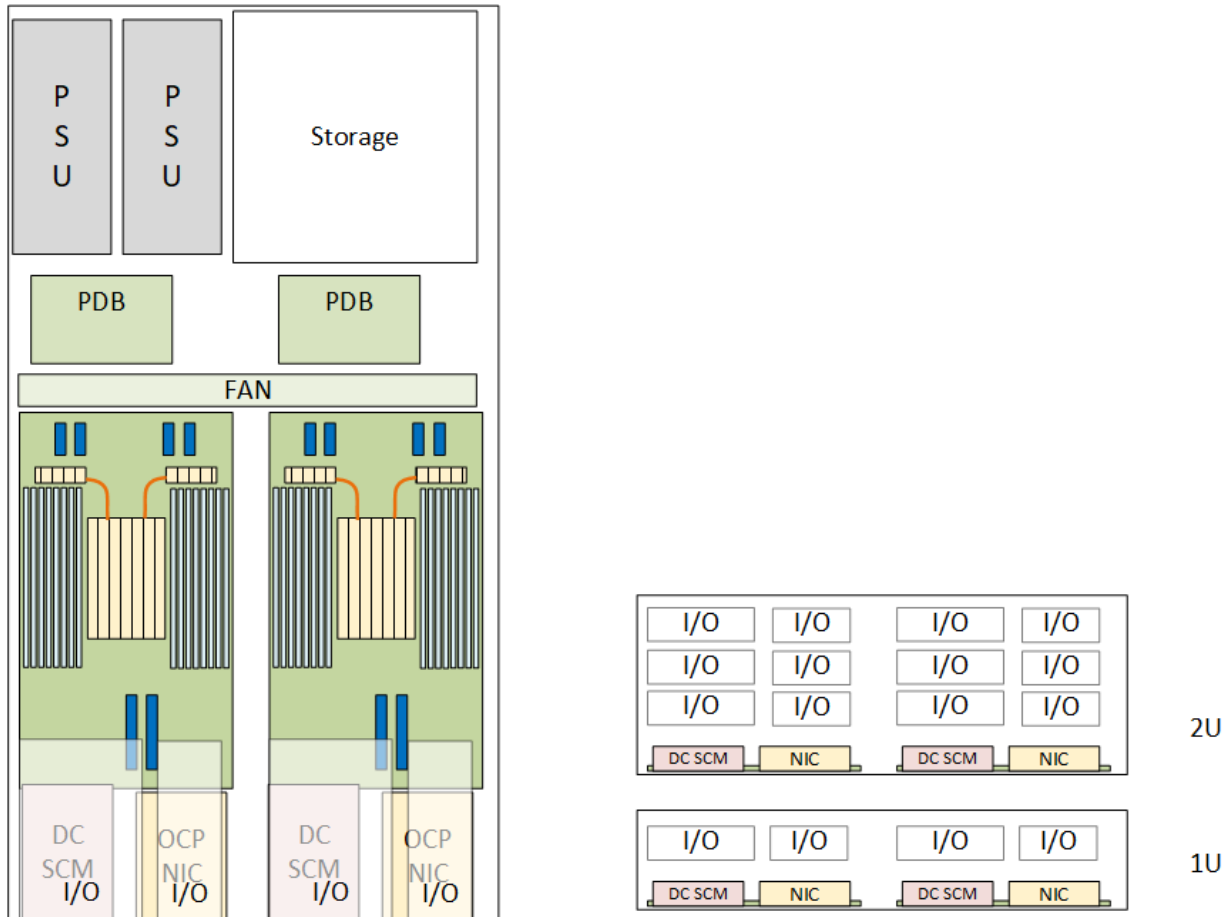
Type 2 Configuration Example – Enterprise Server



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The Type 2 HPM would also be suitable for 2 (or 4) Node products.

Type 2 Configuration Example – 2 Node

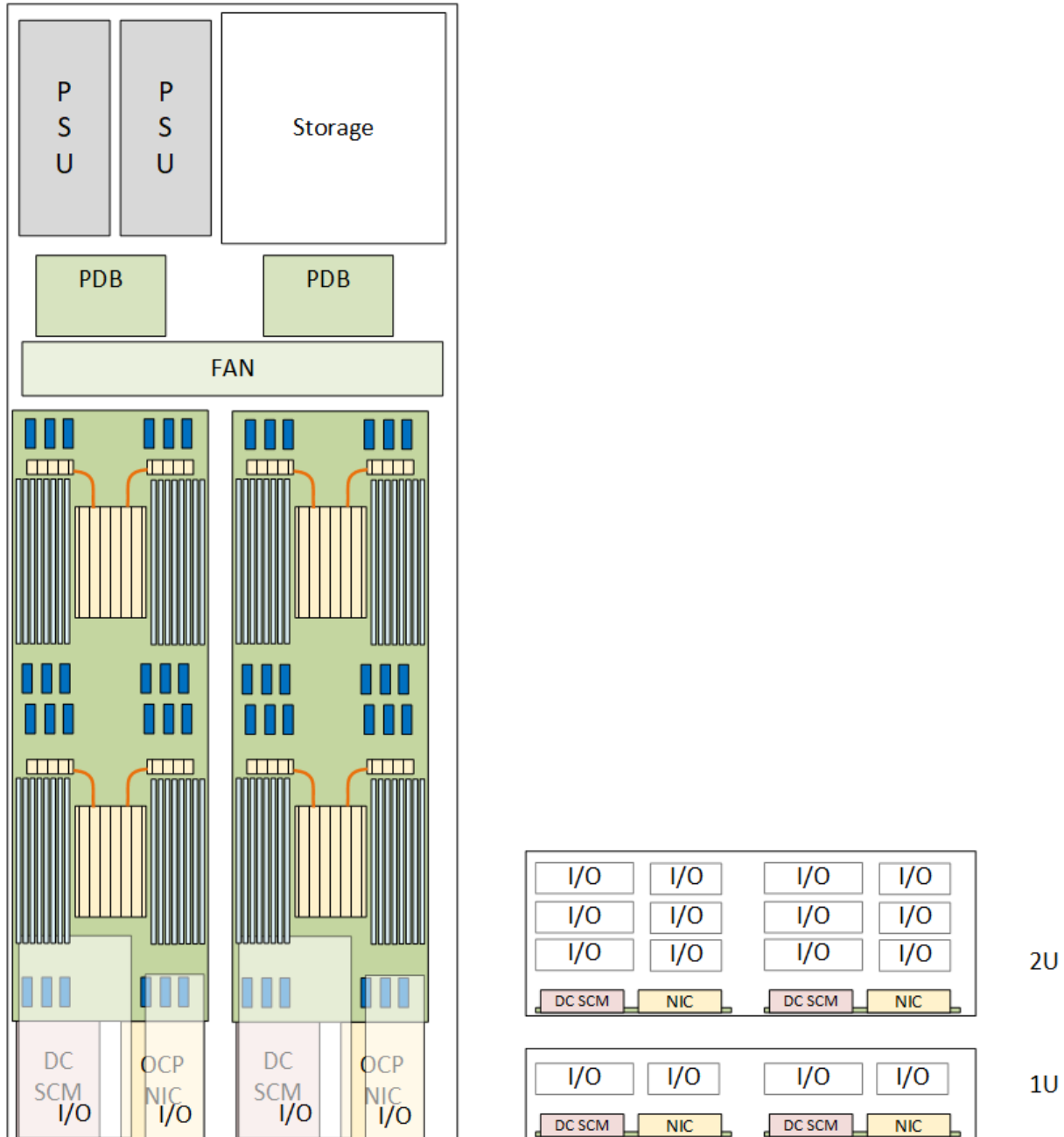


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Type 3

The Type 3 HPM grows in depth to allow 2 socket “shadow core” designs, specifically to support 2 Nodes across a chassis. In this configuration the ability to utilize the full PCIe resources is deprioritized. The ability to support EVAC thermal solutions would be applicable.

Type 3 Configuration Example – 4 Node

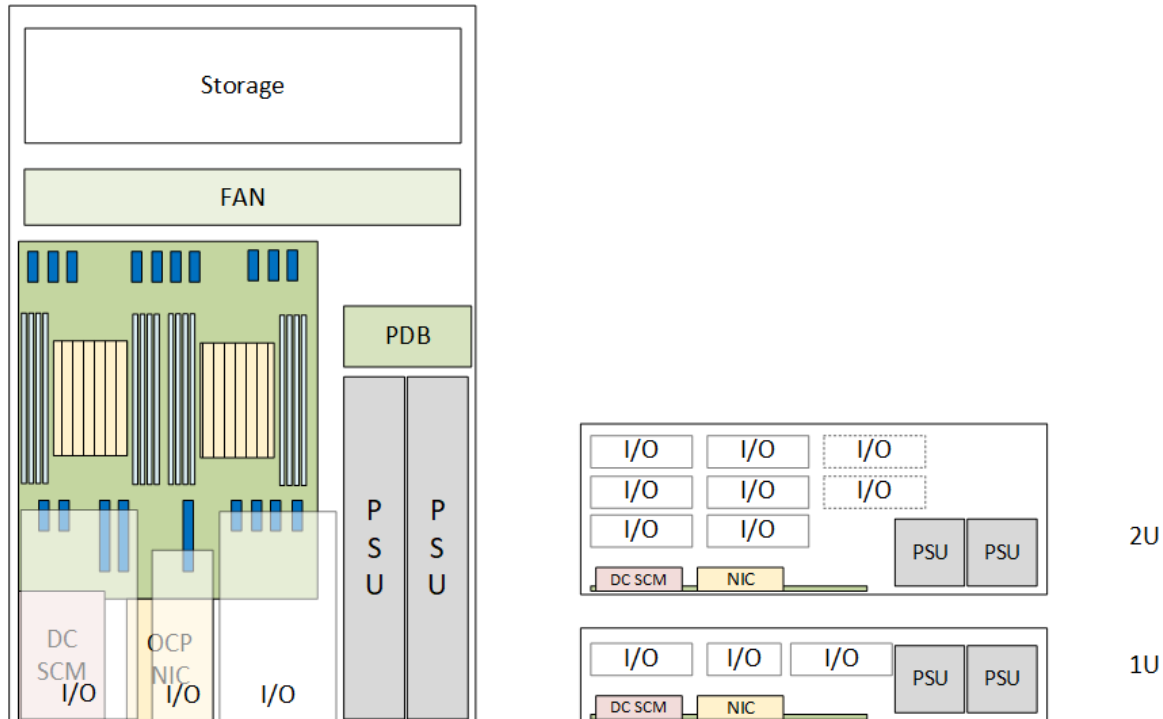


1065 Type 4

The Type 4 HPM is the only Type to grow in width. The primary driver for the Type 4 form factor is ability to support a dual socket “spread core” 2 Node product with adjacent PSUs in a 19” (or larger) rack. To achieve this 2 socket design a concession is made on memory socket support so that only one DIMM per channel is expected on an 8 channel per socket architecture. The other features intended to be supported on a Type 4 HPM would be full PCIe lane count, and EVAC thermal solutions.

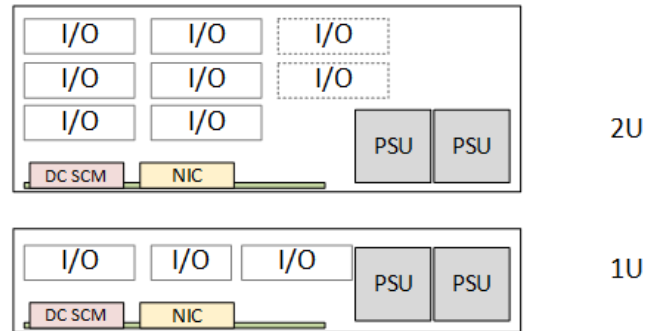
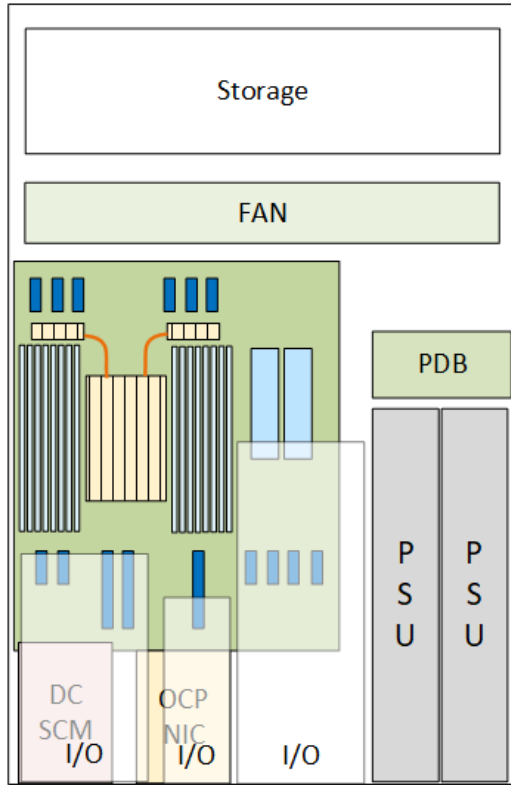
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Type 4 Configuration Example – 2 Socket Spread Core



- 1075 Another possible Type 4 HPM would be a 8 memory channel CPU with 2 DIMMS per channel as in Type 2, but with more on board peripherals than the other ½ width Types.

Type 4 Configuration Example – Expanded Features 1 Node



1080 Multi-Node Specific

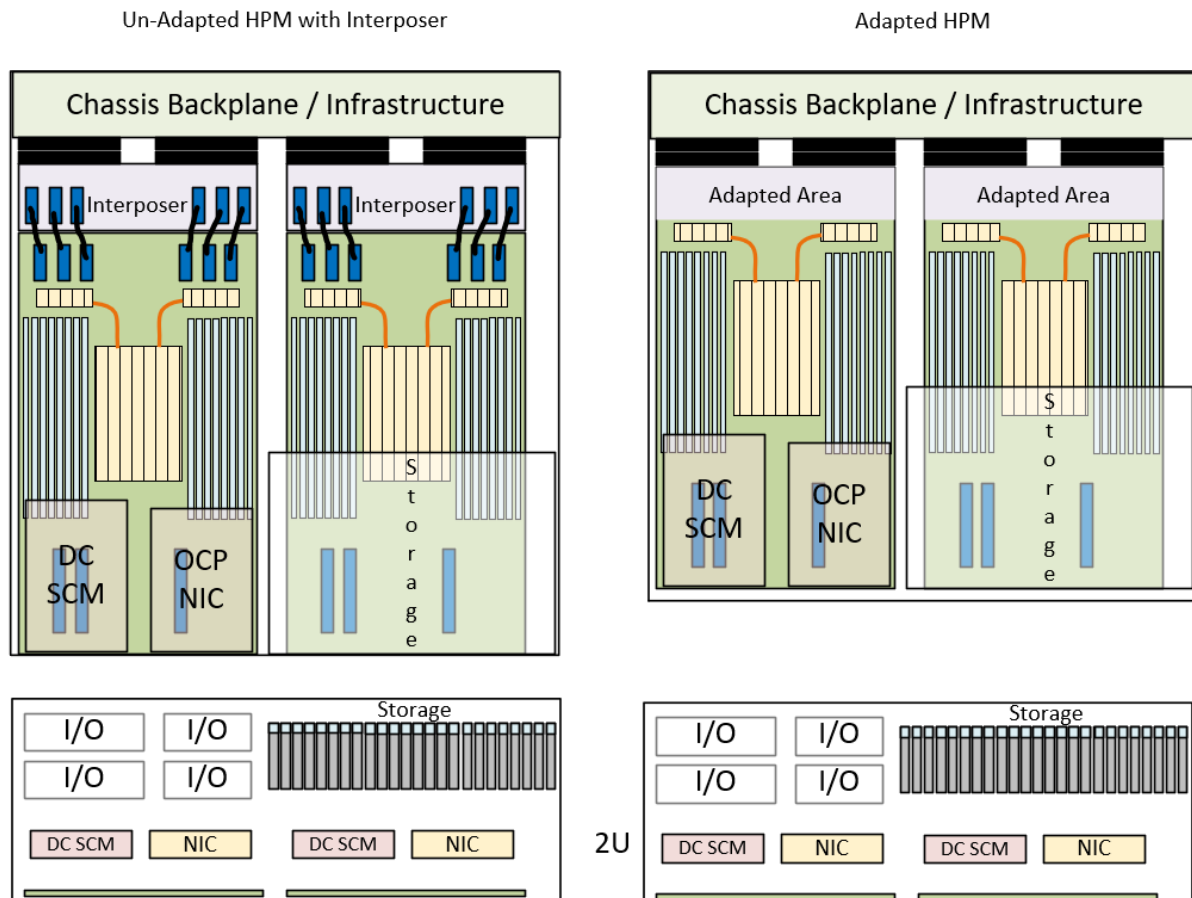
Multi-Node Adaptation

As described in the Power Zone **Section 11.1**, multi-node HPMs may choose to adapt the HPM to add board to board connectors on the Far board edge intended to directly mate into chassis power infrastructure (mid-plane, PDB, bus bar etc.).

1085 Un-adapted HPMs can also be leveraged with this type of chassis infrastructure by leveraging an interposer board between the HPM and the chassis infrastructure.

The example below depicts using an un-adapted HPM on the left and an adapted HPM on the right in a similar system. For this example, shown is a Type 2 node opting to “float” the DC-SCM and NIC cards as opposed to placing them Co-Planar. Additionally, a 21” chassis is depicted.

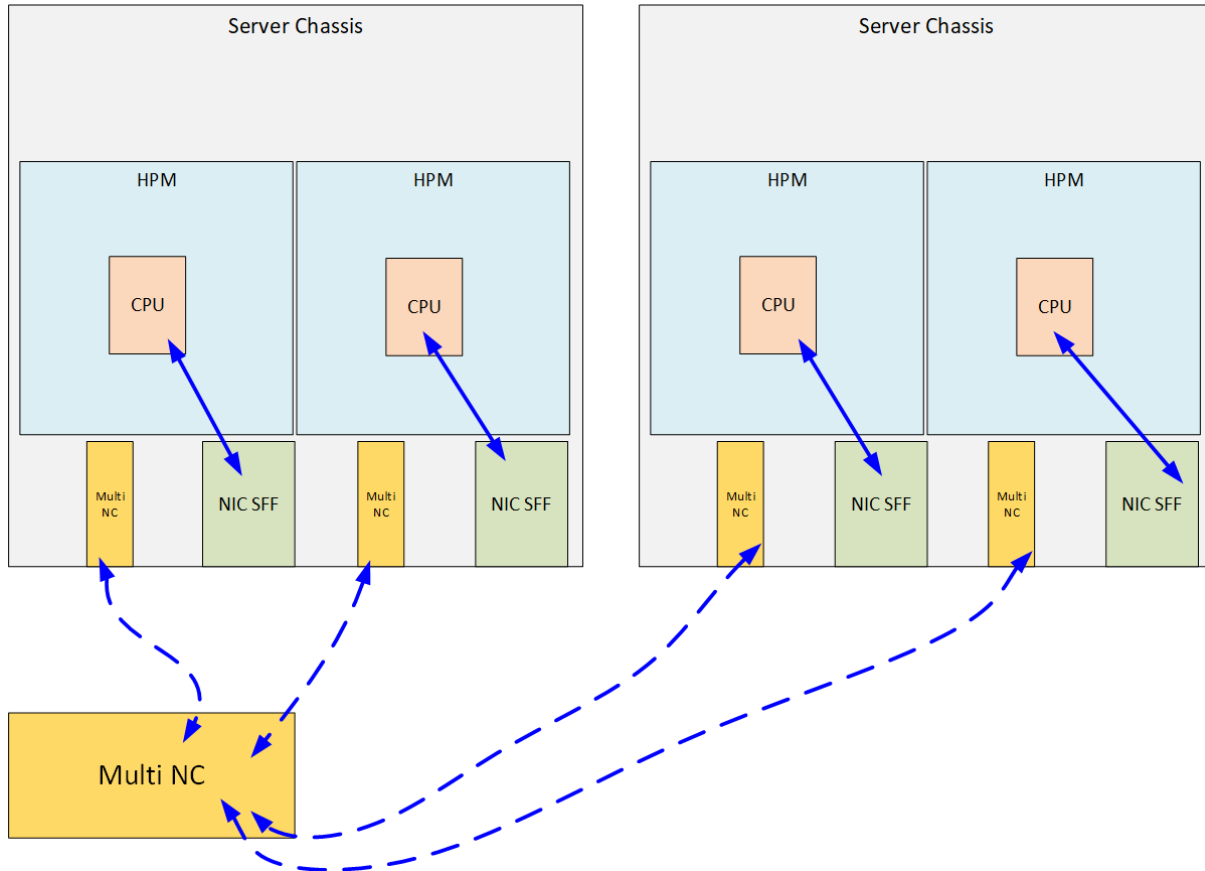
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Multi-Node Management

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How to deploy a multi-node management infrastructure using base specification compliant HPMs is outside of the scope of this specification. However, various common methodologies were evaluated to ensure that M-DNO compliant HPMs could be leveraged into these infrastructures. As an example, a small low-cost local node controller could be connected to the DC-SCM 4C+ connector and then connected to a chassis manager or multi-node controller.



1100 14.2. M-DNO Power Zone Usage

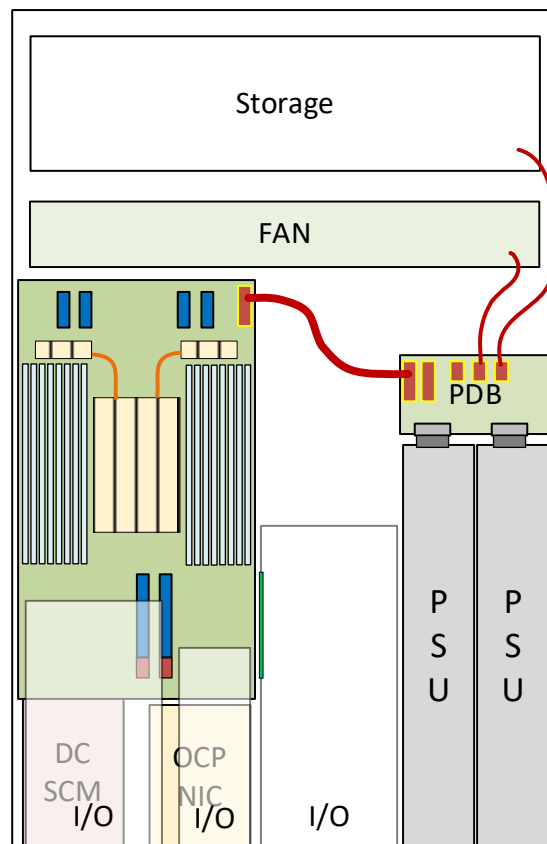
Examples

1105 The M-DNO specification provides some flexibility to HPM implementors and system designers when it comes to Power Zone Usage. In this section, demonstration of some expected configurations leveraging these various options are conveyed. For simplicity's sake, the different power flows are demonstrated using the same HPM board Type (Type 2), however the power zone use case flexibility is common across all board types.

The first example listed below shows a simple monolithic (one HPM) system where PSUs feed power to the system PDB, the HPM power zones are utilized in the minimum required model:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: None

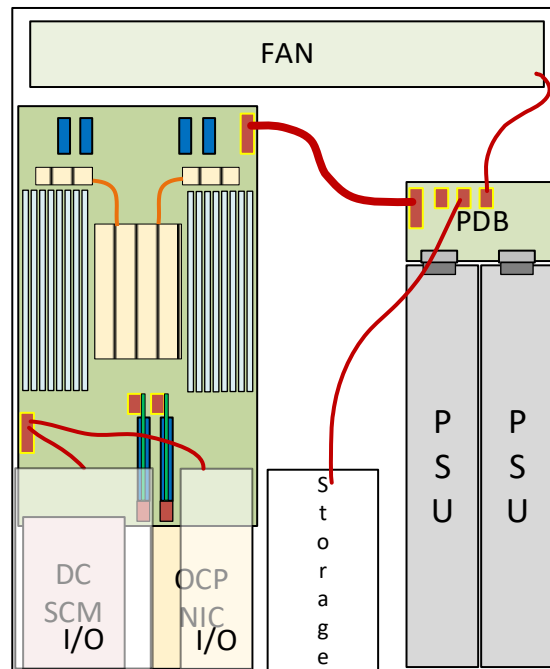
Example 1: Monolithic Basic One Zone Ingress



In the second example below, a monolithic (one HPM) system where PSUs feed power to the system PDB is shown. However, in this example, the optional Near Side power zone is leveraged:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: Supplemental power cable to CEM card aux (Note that the PICPWR definition requires a control an active cable to power gate these cables)
- Supplemental Power to I/O: From Near Zone (These cables could also be sourced from the PDB directly and would not require an active cable to power gate as control logic could be based on the PDB.)
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which leverage the far side for ingress power

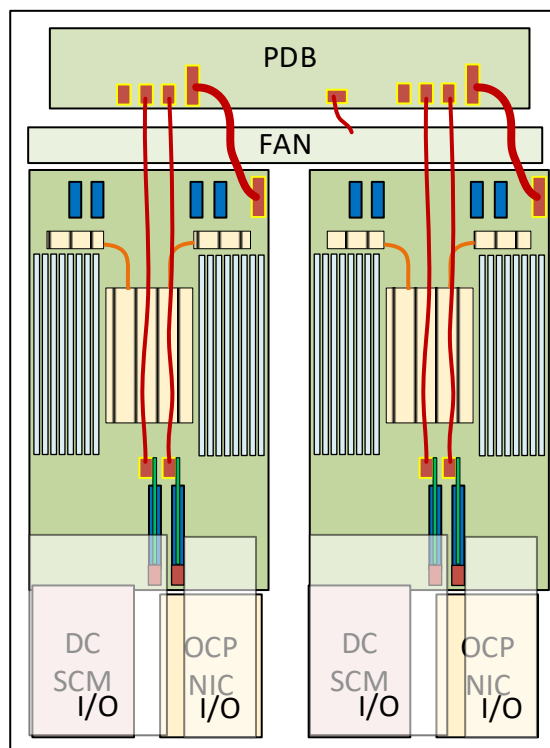
Example 2: Monolithic Leveraging Both Zones



The third example below illustrates a multi-node (>1 HPM) system with a Far Side PDB that could be supplied via PSUs, system level bus bars, or even rack level power distribution.

- 1140 • Far Side Ingress: Power from PDB to HPM (while these connections are depicted with cables the HPM could also be adapted to support a board-to-board connector to chassis power infrastructure like a PDB as noted in **Section 11.1**)
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- 1145 • Supplemental Power to I/O: From the PDB directly (do not require a “puck” as control logic could be based on the PDB)

Example 3: Multi-node with Far Side PDB

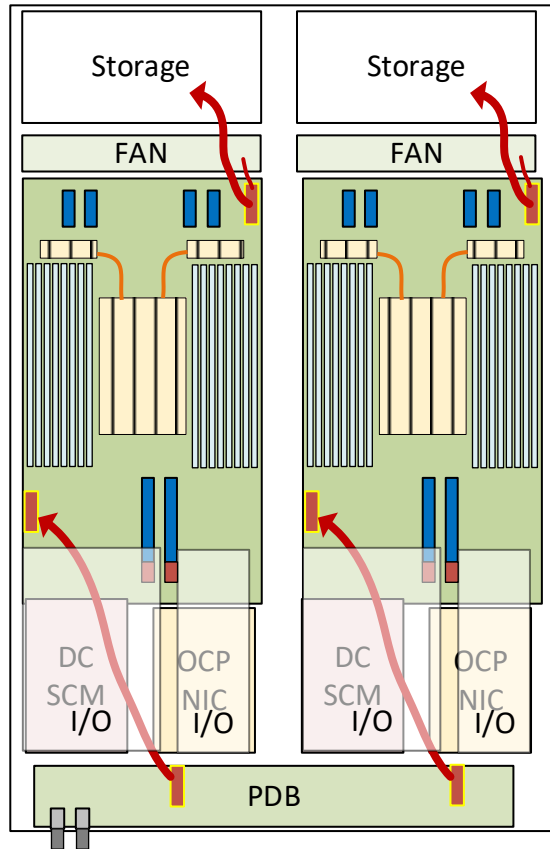


1150 The fourth example below demonstrates a multi-node (>1 HPM) system with a Near Side PDB that could be supplied via PSUs, system level bus bars or even rack level power distribution.

- Far Side Ingress: None
- Far Side Egress: Used to power Storage peripheral subsystem,
- Near Side Ingress: Power from PDB to HPM (cabled)
- Near Side Egress: None
- Supplemental Power to I/O: None
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which use to leverage the far side for ingress power

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Example 4 : Multi-node with Near Side PDB

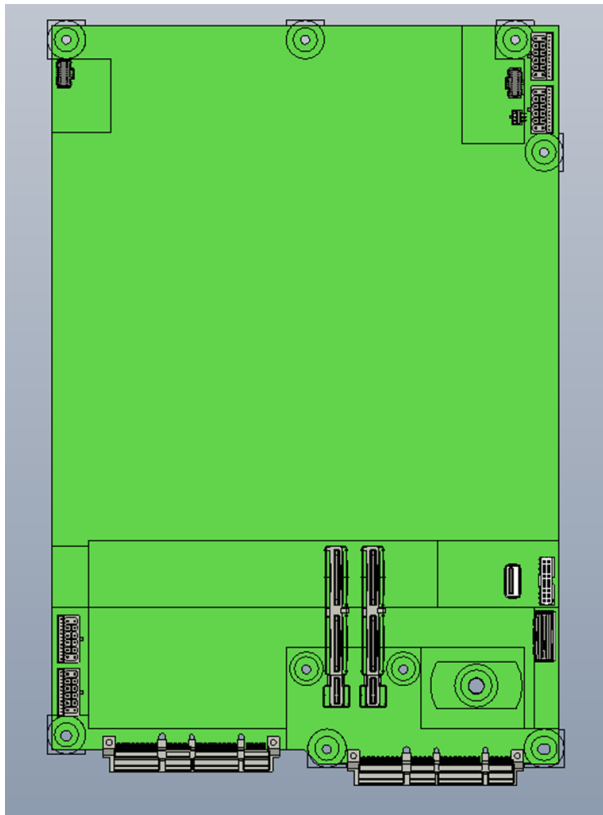


14.3. M-DNO CAD Files

1165 M-DNO CAD files are available at the following link:

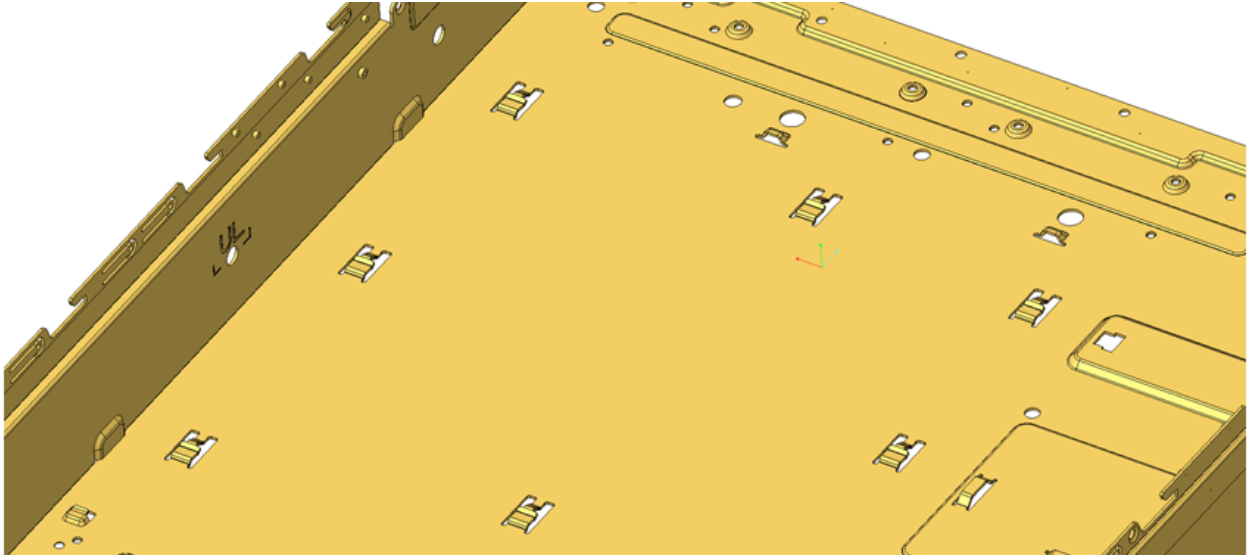
<https://drive.google.com/drive/folders/1YcDWJLH6FwTnaC7UJDD8jyS25bIJHp2Z>

CAD Snapshot (Type 2 Example)



1170 14.4. Example Chassis Base Geometry for Chassis-to-Board Bracket interface

Below is an example geometry required in the chassis base to interface to the Chassis-to-HPM bracketry in **Figure 13: Example of Chassis-to-Board Bracket (Board Pan)**. The exact geometry is not specified, but considerations must be made for maximum board thickness (see **Section 10.4**) and HPM Keepout Zone sizes (See **Section 10.3** and **10.5**).



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