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Project Junction City
Intel Whitley Common Cloud Platform Specification

Revision v1.0.0

Authors:

John Tell, System Architect, Intel Corporation
Wei Lu, Hardware Design Lead, Intel Corporation
Mark Sprenger, Mechanical Engineer, Intel Corporation
Juan Cevallos, Thermal/Mechanical Engineer, Intel Corporation
Jason Haines, Firmware Engineer, Intel Corporation
Gareth Ward, Hardware Engineer, Intel Corporation
Louis Luo, Hardware Design Lead, Wiwynn Corporation
Eason Chi, Hardware Engineer, Wiwynn Corporation
Amber Tsai, Mechanical Engineer, Wiwynn Corporation
Eric Tseng, Mechanical Engineer, Wiwynn Corporation
Jordan Su, Thermal Engineer, Wiwynn Corporation

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Revision History

Revision	Editor	Description
V0.1 (December 2020)	John Tell	First Draft
V0.2 (January 21, 2021)	John Tell	• pg. 9 – changed U.2 to Right Angle connector • pg. 11 (Fig 3.2) – moved “13” Pushbutton/LED location, deleted top “15” conn reference • Pg. 11 – corrected TDP support to 270W • Pg. 12 – corrected DIMM Overview section • Pg. 14 & 24 – corrected OCP3.0 and U.2 to Right Angle connectors • Pg. 26 – Updated System Fan connector • Pg. 28 – Changed settings for J4D4 jumper • Pg. 37 – Updated SSD Drive pitch to reference SSD Drive Connector pitch • Pg. 40 – Added note “Default – B25 Compatibility pin NOT

		monitored”
V0.9 (January 24, 2021)	John Tell	No Changes for submittal
V1.0 (April 28, 2021)	John Tell	No Changes for final submittal

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1. Scope & Overview

Scope:

Intel Junction City is designed based on Cloud Optimized Server concept to fulfill various Cloud computing requirements and use cases from multiple customer input during initial concept discussions.

Junction City is a dual-socket spreadcore server platform that supports the Whitley Platform Xeon-SP (Ice Lake) processors in combination with the Lewisburg-R PCH (PCH) to provide an optimized feature set intended to align to Cloud CSP technology requirements.

This specification defines the overall system concept, platform specifications, midplane sku options, riser options, PCIe configurations, power delivery, and user I/O details.

This specification does not intend to cover; system-level mechanical specifications (only basic concept and dimensions), BIOS and BMC firmware specifications, thermal design specifications, or any specifications related PSUs, storage devices, and networking devices.

Overview:

Junction City Cloud Compute Server features are listed below:

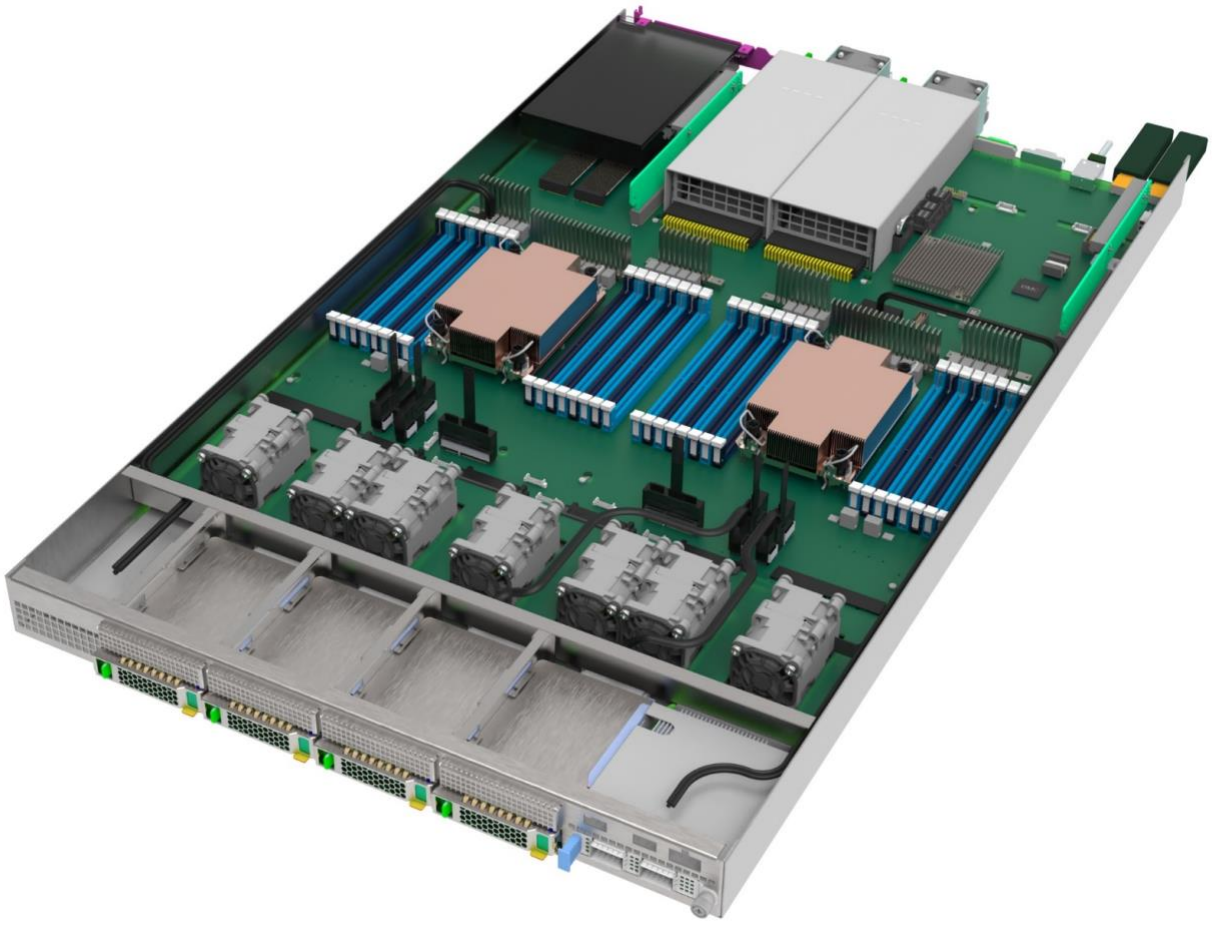

Figure 1.1 Junction City Common System – Mechanical ISO View

Table 1-1. Junction City System Feature List

Item Name	Specifications
Chassis	1U Rack Mount Form Factor – intended to provide design guidance for ODMs
Power Supplies	+12VDC 1U Common Redundant Power Supplies (CRPS)
System Fans	Dual Rotor 12V Fans (40x40x56mm)
Baseboard	12L Whitley Dual Socket Spread-Core (32DIMM) motherboard (17.2in x 20.0in)
Sys board - Midplane1	Direct attach to baseboard to support 2x OCP3.0 + 4x U.2 SSD pass-thru for front panel access, supports cut-out locations for up to 7 system fan locations
Sys board - Midplane2	Direct attach to baseboard to support 6x U.2 SSDs for front panel access, supports cut-out locations for up to 7 system fan locations
Sys board - Riser	2x Rear access locations up to PCIe x16 per Riser slot. Supports 1x FHHL PCIe AIC
Sys board - Front Panel	Front Panel module card to support: RJ45 - 1GbE Dedicated Management Power/Reset buttons ID locator button/led Status LEDs
System Cabling Kit	PCIe Gen4 SSD cables (SFF-TA-1009 to SFF-8639) Front Panel Kit: • Front I/O slimSAS cable (supports RGMII) • Serial COM + VGA cable • USB cable 12VDC Optional Cable for additional Front Power requirements (i.e. 40W System Fan support)

Table 1-2. Junction City Baseboard Feature List

	Descriptor
Processor	Dual socket P4 (LGA4189) ICX support TDP: 150W-205W (up to 270W power delivery supported) Supports 3 links per CPU, x20, speed: 11.2 GT/s
Platform Controller Hub	DMI Gen 3 x4 12x SATA 6 Gbps ports and 2x M.2 for boot 2x USB3.0 ports in rear porch 1x USB3.0 & 1x USB2.0 ports in front (cabled)
Processor Memory Configuration	DDR4 Registered, 3200 MTS(1DPC) & 2933 MTS 2DPC 2-2-2-2, 8x Channels/Socket Surface Mount DIMM Connectors, 310 mil DIMM pitch

	Barlow Pass DCPMM DIMM support
FPGA	Intel® MAX 10 FPGA 10M25 (25k LEs) 484pin package Used for Power Seq + PFR support
Management & Security	ASpeed AST2500 BMC with video Intel® Trusted Execution Technology Boot Guard using SPI TPM2.0 Intel PFR Platform Root-of-Trust
PCI Express Interface	2x x16 PCIe riser connectors 2x x16 OCP 3.0 (SFF-TA-1002) 4C+ Connectors 4x x4 Right Angle U.2 (SFF-8639) connectors 6x x8 EDSFF (SFF-TA-1009) connectors
Debug	CPU/PCH Merged XDP (MIPI60 connector) At Scale Debug Autonomous Crash Dump (ACD) Close Chassis Debug (DCI) over USB3.0 (Front or Rear access) Port80 (LED and/or connector) Dediprog BMC UART Debug header SMBus Debug header
Boot Device	U.2 NVMe SSD (Front Panel) 2x M.2 (PCIe x2 per conn)
Front Panel & Rear Panel IO options	2x USB 3.0 (Front supports 1x USB3 & 1x USB2), Video, Serial Port 1 GbE manageability port Power, Reset and ID buttons Status LEDs

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2. Physical Specifications

2.1 Block Diagram

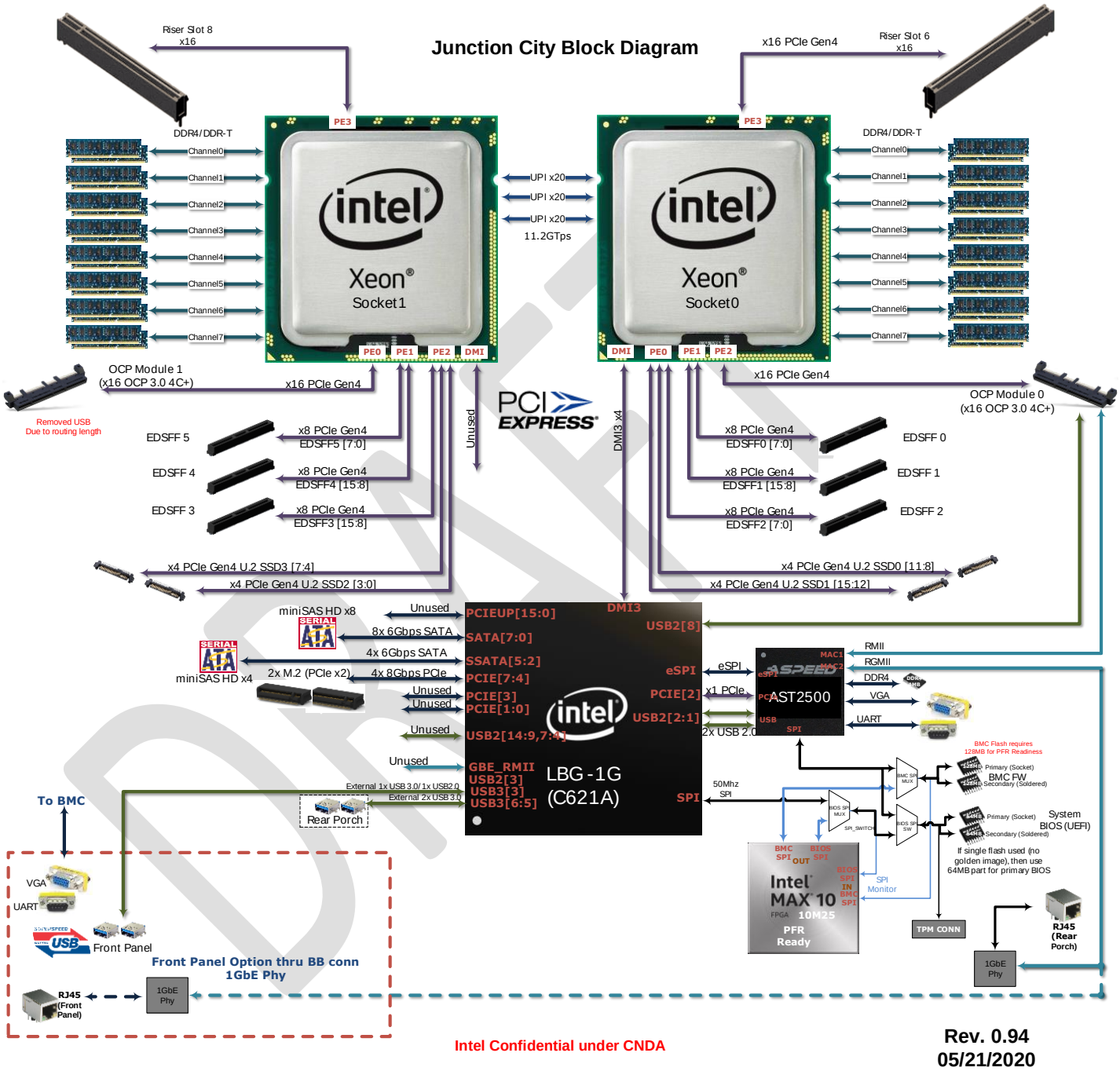

Figure 3.1 Functional block diagram of the Junction City motherboard

2.2 Placement and Form Factor

Board form factor is 17.2 inch by 20 inch (17.2""x20"). Figure 3-2 illustrates board placement. The placement is meant to show key components' relative positions. Following internal connectors should be placed as close as possible to front of the board in order to have easy front access:

- 7x System Fan connectors (Midplane Fan support)
- 1x RJ45
- 1x VGA
- 1x Serial COM port
- 2x USB

Figure 3.2 illustrates the actual placement of key parts of the Junction City motherboard.

2.3 CPU and Memory

2.1.1 CPU

The motherboard supports all Intel® Icelake-SP processors with TDP up to 270W. The features listed below must be supported by the motherboard

- Support two Icelake-SP XCC processors up to 270W TDP, and vendors should engage with Intel to ensure the design ready for future processors

- Three full-width (20 lanes per link) Intel UPI links up to 11.2 GT/s/direction for Icelake-SP XCC processor
- Up to 36 cores per CPU (up to 72 threads with Hyper-Threading Technology).
- Single Processor mode is supported on CPU0

2.1.2 DIMM Overview

The motherboard has DIMM subsystem designed as below:

- DDR4 direct attach memory support on CPU0 and CPU1.
- 8x channels DDR4 registered memory interface on each CPU
- Support DDR4 speeds up to 3200MT/s (1DPC) or 2933MT/s (2DPC)
- Support RDIMM, LRDIMM DDP, LRDIMM 3DS TSV-4H
- Support SR, DR, QR and 8R DIMM
- Up to maximum 4096 GB with 128 GB DRAM DIMM
- Follow updated JEDEC DDR4 specification with 288 pin DIMM socket
- Refer to Whitley Reference Design for supported DDR4 memory configurations

2.1.3 BPS (Barlow Pass DIMM)

Board and system design shall support Barlow Pass DIMM with 128G, 256G and 512G and allow all POR configurations and power levels.

Junction City shall support BPS ADR.

2.1.4 DIMM Nomenclature

DIMMs are organized into physical slots on DDR4 memory channels that belong to each processor sockets. Each Socket (CPU) will have alphabetical lettering to denote memory channels, for example, Channel A, B, C, D, E, F, G, H for each of the 8 channels of the ICX processor. The DIMM count within the channel will be denote by numbering. CPU{skt#}_DIMM_{CH letter]{dimm#}

The memory slots of DDR4 channels from the ICX processor should be populated on a farthest first fashion. This means that A1 cannot be populated if A0 is empty.

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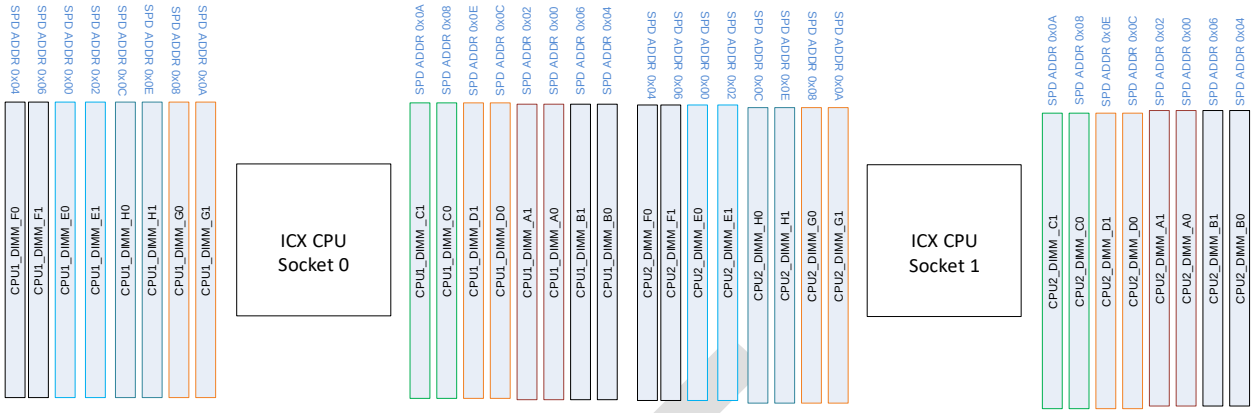

Figure 3.3 Whitley CPU and DIMM labeling and placement

2.4 Platform Controller Hub (PCH)

The motherboard uses Intel® Lewisburg-Refresh (C621A) chipset, which supports following features:

- 4x USB 3.0/2.0 ports: two for front panel connector, two for rear panel connector
- 2x M.2 connector (PCIe 3.0 x2 ports) from PCH
- 12x miniSAS HD ports
- SPI interface, connect to BMC to enable BMC the capability to perform BIOS upgrade and recovery
- SPI interface for TPM header
- SMBUS interface (master & slave)
- Intel® Server Platform Services (SPS) 4.0 Firmware with Intel® Node Manager
  - PECI access to CPU
  - SMLink0 connect to BMC
  - Intel® Manageability Engine (ME) obtain HSC PMBus related information through SMLink0 to BMC interface by default; BMC has direct connection to HSC PMBus to have flexibility of HSC PMBus related feature support
  - Intel® ME SMLink1 connect to Hotswap controller PMBus interface with resistor option, default is disconnect
  - Power capping capability
  - Temperature sensors reading from BMC
- PCH SKUs
  - Board design shall support Lewisburg-Refresh 1G (C621A) PCH SKU in terms of power delivery and thermal design

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2.5 PCIe

2.5.1 PCIe lane mapping

Junction City is designed to support 2x PCIe 1U Riser slots for Rear Panel access, with the remaining ICX direct PCIe interfaces (x48 per CPU) towards the Front Panel supporting:

2x OCP 3.0 Right Angle Connectors supporting PCIe Gen4 x16 per connector

4x U.2 SFF Right Angle Connectors for PCIe Gen4 (x4) Hotswap supported NVMe SSDs per connector

6x EDSFF Vertical Mount Connectors for PCIe Gen4 (x8) to either HSBP on Top Row Front Panel or additional PCIe bandwidth to Rear AIC

Junction City also supports 2x M.2 (80 or 110mm) PCIe Gen3 (x2) Boot locations from the LBG-R PCH.

Table 2-1 PCIe Lane Mapping

Device	Technology	Port	# of Lanes	Bifurcation supported
OCP0	Gen4	CPU0 PE2	16	x16, x8, x4
OCP1	Gen4	CPU1 PE0	16	x16, x8, x4
EDSFF0	Gen4	CPU0 PE1 [7:0]	8	x8, x4
EDSFF1	Gen4	CPU0 PE1 [15:8]	8	x8, x4
EDSFF2	Gen4	CPU0 PE0 [7:0]	8	x8, x4
EDSFF3	Gen4	CPU1 PE2 [15:8]	8	x8, x4
EDSFF4	Gen4	CPU1 PE1 [15:8]	8	x8, x4
EDSFF5	Gen4	CPU1 PE1 [7:0]	8	x8, x4
SSD0	Gen4	CPU0 PE0 [11:8]	4	x4
SSD1	Gen4	CPU0 PE0 [15:12]	4	x4
SSD2	Gen4	CPU1 PE2 [3:0]	4	x4
SSD3	Gen4	CPU1 PE2 [7:4]	4	x4
RISER0	Gen4	CPU0 PE3	16	x16, x8, x4
RISER1	Gen4	CPU1 PE3	16	x16, x8, x4
CPU Total			64 per CPU	
BMC	Gen2	PCH PCIE[2]	1	x1
M.2 A	Gen3	PCH PCIE[5:4]	2	x2, x1
M.2 B	Gen3	PCH PCIE[7:6]	2	x2, x1
PCH Total			5	

2.5.2 PCIe Hot Plug

PCIe Hot Plug is supported on SSD0-3 and EDSFF0-5 connector locations to support NVMe drive hot swap capabilities.

2.6 PCB Stack Up

Following PCB stack up should be followed for motherboard design. Please refer to Whitley PDG regarding Orion City Stack up for further details.

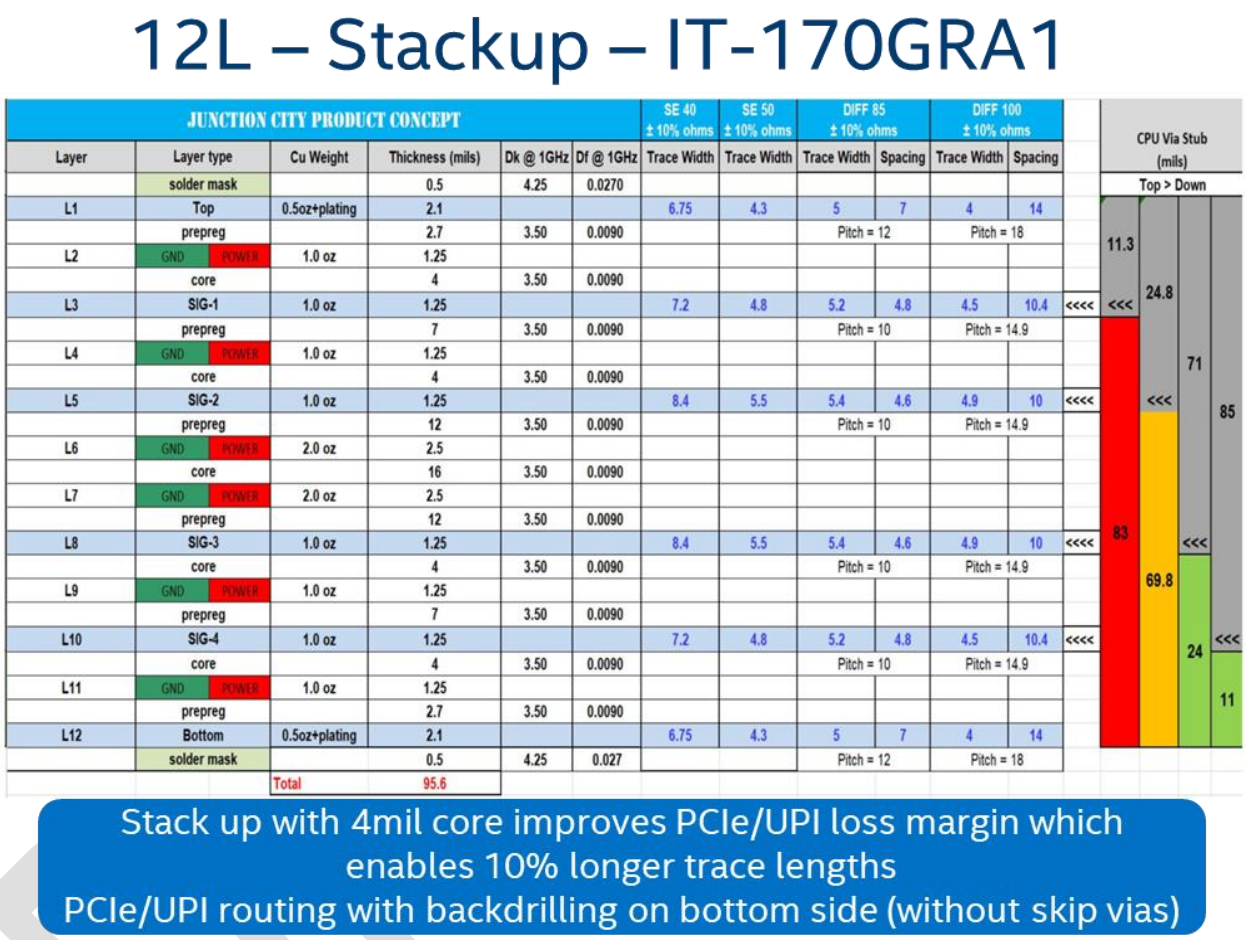

Figure 3.6 illustrates the actual placement of key parts of the Junction City motherboard.

3. Reference Design

Junction City is a derivative design based on Intel Orion City Cloud Reference Board (referenced as Orion City in this document).

Vendor shall use the latest Intel Whitley Orion City Design Database collateral Rev1.01 (Doc# 576577) as the base of RFP study, making proposal, and proposal discussion.

Vendor shall use the latest Junction City Design Collateral Rev1.1 (Doc# 630232), including the Intel Junction City Design Collateral Errata Rev2.0 (634174) as the base of EVT design. EVT design schematic, board file, CPLD code, Voltage Regulator firmware shall start from this collateral.

4. BIOS

4.1 BIOS Chip

In order to facilitate BIOS development, the SPI flash used by the BIOS, Junction City supports Dual ROM flash; socketed Flash (Primary) and soldered down Flash (Secondary), both devices will be soldered down versions for Production systems. It is recommended to support 64MB flash part for the board design. The recommended 16 pin SOIC SPI flash socket information is as follows: Vendor: LOTES. Vendor Part Number: ACA-SPI-006-T01 Intel Part Number: D91187-001.

4.2 BIOS HW Jumpers

See Headers and Jumpers section

4.3 BIOS Feature Requirements

For Junction City BIOS Feature Requirements see listing included in Intel Junction City Design Collateral.

5. BMC ASPEED AST2500 BMC

Embedded ARM1176JZF-S 32-bit RISC CPU microcontroller with max frequency of 800MHz, 4Gb SDRAM and dual serial NOR SPI flash each with a 64Gb capacity. Hardware capabilities of this microcontroller include the following and further details can be obtained in the AST2500 datasheet:

- VGA/2D controller with max resolution of 1920x1200 (32bpp@60Hz)
- Media/Storage Redirection (USB)
- Keyboard, video and mouse (KVM) Redirection
- LPC or eSPI bus interface support
- DDR3/4 16-bit interface with up to 800Mbs/1600Mbs operation, with ECC support
- USB
    - USB 2.0 Virtual Hub Controller (x1)
    - USB 2.0 Device Controller (x1)
    - USB 1.1 HID Controller (x1)
    - USB 2.0 Host Controller (x2)
    - USB 1.1 Host Ports (x2)
- Hash Engine (MD5/SHA/RSA)
- Crypto Engine (AES/RC4/DES/3DES)
- I2C/SMBus Controller (x14)
- PWM Outputs (x8)
- Fan Tach (x16)
- PECI 3.1 support with IO buffer
- GPIO (228 max)
- SGPIO Master (80 max)
- SGPIO Monitor (10 devices x2ch x2)
- UART (x5)
- Hardware UART debug
- Hardware Watchdog Timer

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- RTC
- Ethernet
    - MAC Module (x2)
    - 10/100/1000Mbps
    - Interfaces: RGMII (x2) or RMI/NC-SI (x2)
- Embedded SRAM (36KB)
- Battery Backed SRAM (64 bytes)
- Chip Unique ID (64 bits)
- System SPI Interface
- MCTP/PCIe
- DMA between System and BMC memory
- ADC (16 voltage channels)
- JTAG (boundary scan, master)
- SD/SDIO/eMMC Interface (x2)
- Mailbox registers for communication between the BMC and host
- IO port 80h snooping capability, with DMA support for autonomously moving port80 data to memory.

5.1 BMC Requirements

For Junction City BMC Feature Requirements see listing included in Intel Junction City Design Collateral.

5.2 BMC ROM Flash

In order to facilitate BMC FW development, the SPI flash used by the BMC, Junction City supports Dual ROM flash; socketed Flash (Primary) and soldered down Flash (Secondary), both devices will be soldered down versions for Production systems. It is recommended to support 64MB flash part for the board design (128MB part is required, if customers plan to support PFR FW). The recommended 16 pin SOIC SPI flash socket information is as follows: Vendor: LOTES. Vendor Part Number: ACA-SPI-006-T01 Intel Part Number: D91187-001.

5.3 Management Network Interface

The BMC supports options for front or rear panel access to a dedicated (not shared with host OS) 1GbE PHY. The BMC can also optionally support the use of an OCP NIC plugged into the first slot (OCP Module0), connected to CPU0 and is shared with the host OS.

5.4 Serial COM and SOL

1 host OS RS-232 serial COM port is suppported which can be configured to output BIOS MRC debug data during POST. This COM port can also be redirected over LAN using the IPMI 2.0 Serial Over LAN (SOL) feature and also with newer and more secure serial over SSH feature.

5.5 BMC Sensor Monitoring

The following table provides a description of the proposed HW sensor monitoring provided by the BMC on Junction City. This table is included since these have HW implications to the board design. Specific sensor support is dictated by customer requirements.

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Table 5-5 Sensor Monitoring Support for Junction City

MONITORING CAPABILITY	DESCRIPTION	FIRMWARE ACTIONS
Voltage	BMC monitors main voltages on system, including battery, using the BMC A/D inputs. Exposes readings via IPMI threshold sensors.	BMC logs SEL entry for threshold crossing. Criticality reflected in Front or Rear Panel Status LED.
Thermal	BMC monitors system thermal sensors, typically: Inlet and outlet ambient air temperature, CPU(s), DIMM(s) and other discrete board thermal sensors. May include Lewisburg PCH, PCIe or OCP add in cards, storage devices (SSDs), power supplies or other component thermal sensors depending on platform-specific thermal management requirements. Exposes readings via IPMI threshold sensors. Some IPMI thermal sensors may aggregate the readings of the underlying physical sensors.	BMC logs SEL entry for threshold crossing. Criticality reflected in Front or Rear Panel Status LED. BMC automated fan speed control algorithm can be configured to use various thermal sensors for control inputs.
Thermal Trip	BMC monitors CPU, Memory and PCH ThermTrip inputs. Exposes readings as digital discrete IPMI sensors.	BMC logs SEL entry upon detection of signal assertion. Criticality reflected in Front or Rear Panel Status LED. Note that system shutdown occurs via Hardware action, without BMC involvement.
VRD 13 VRHOT#	BMC monitors VRD 13 VRHOT# signals for each Processor VR and Memory VR solution. Exposes readings as discrete IPMI sensors	BMC logs SEL entry upon detection of signal assertion. Criticality reflected in Front or Rear Panel Status LED
VRD temp monitoring	BMC monitors CPU and memory VRD temperatures via PECI ***BMC FW support for this is TBD.***	BMC logs SEL entry for threshold crossing. Criticality reflected in Front or Rear Panel Status LED. Fan control algorithm uses thermal sensors for control inputs.
Fan Tach	BMC monitors its fan tachometer inputs and exposes readings via IPMI threshold sensors (1 Per Fan).	BMC logs SEL entry for threshold crossing. Criticality reflected in Front or Rear Panel Status LED and Fan Fault LEDs. Fan failure may result in boosting of one or more other fans.
Power and Current Monitoring for Power Supplies	BMC monitors the following on a per-power-supply basis (only supported on systems with PMBus-compliant Power Supplies): input power, output current (% of max rating). Exposes readings via IPMI threshold sensors. Node Manager 2.0 also exposes total input power (sum for all PSUs) via a NM-specific IPMI command.	BMC logs SEL entry for threshold crossing. Criticality reflected in Front or Rear Panel Status LED. If NM 2.0 policies are enabled, changes in input power readings can result in system throttling for power limiting.
Power Supply Presence & Status	BMC monitors each installed Power Supply Unit (PSU) for presence, failure, predictive failure (warnings), A/C lost, A/C present but out-of-range, and configuration errors (e.g. incompatible	BMC logs SEL entry for changes to presence state. Log SEL entries for warning/fault state changes.

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	manageability protocol). Exposes state as IPMI discrete sensor.	
Power Supply Redundancy	BMC monitors redundancy state of PSU sub-system (only supported on configurations that have redundant PSU capability). Exposes state as IPMI redundancy sensor.	BMC logs SEL entry for changes in redundancy state.
SMI# Timeout	BMC monitors SMI# signal to detect if it has remained asserted for > 90s. Events are logged against an IPMI discrete sensor. **This functionality relies on CATERR/MSMI signal routed to PCH.**	BMC logs SEL entry for SMI Timeout detected. BMC controller resets the system after a predetermined amount of time.
Processor Presence	The BMC monitors the presence of each Processor. Exposes state as IPMI discrete sensor (1 per CPU slot).	BMC logs SEL entry for state changes.
Processor IERR	The BMC monitors the CATERR# signal for held-low condition and queries the Processor via PECI to determine which Processor is the source and try to determine type (e.g. due to FIVR fault or CPU/VR mismatch). Exposes state as IPMI discrete sensor (1 per CPU slot).	BMC logs SEL entry for state changes. Criticality reflected in Front or Rear Panel Status LED
Processor ERR[2]#	The BMC monitors the ERR[2]# signal Exposes state as IPMI discrete sensor (1 per CPU slot).	BMC logs SEL entry for state changes. Criticality reflected in Front or Rear Panel Status LED. BMC controller resets the system after a predetermined amount of time.
Processor Population Fault	The BMC monitors the Processor slot population state for invalid configuration (e.g. no CPU in a slot that must be populated). Exposes state as IPMI discrete sensor (1 per system)	BMC logs SEL entry for state changes. Criticality reflected in Front or Rear Panel Status LED
VR Watchdog Timer	The BMC starts a timer upon system DC power-on and monitors for System PowerGood signal assertion before expiration of time. The BMC reports if timer expires.	BMC (or HW) powers down the system. BMC logs SEL entry for timer expiration. Criticality reflected in Front or Rear Panel Status LED
Processor Thermal Control (PROCHOT#)	The BMC reads/clears registers in Processor (via PECI) to monitor % of time that Processor is throttled due to internal thermal conditions over a given time window. Exposes readings via IPMI threshold sensors (1 per CPU).	BMC logs SEL entry for threshold crossing. Criticality reflected in Front or Rear Panel Status LED.

5.6 BMC Debug Header

BMC UART header is a 3-pin header provided on the baseboard, and is required for BMC Firmware development. During production this header can be removed. Typical application is to use a UART to USB cabled similar the this FTDI cable: TTL-232R-3V3

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Table 5-6 BMC Debug Header Pinout

Pin#	Description
1	BMC_UART_TX
2	GND
3	BMC_UART_RX

6. Thermal Design Requirements

6.1 Thermal Design Description

- System summary
- System boundary conditions
- High-level thermal requirements

6.1.1 Temperature projections for key components

Below are projections for key components when using a 1U Intel Reference thermal solution using System Fans @ 20W max power. For CPU guidance refer to the Thermal and Mechanical Specifications and Design Guide (TMSDG) document #574080

Table 7-1: Temperature Projections (elevation 900m) for 1U Intel Reference Thermal Solution

	Inlet Temperature (°C)	40		35	
Description	Tspec (°C)	TDP (W)	Margin(°C)	TDP (W)	Margin(°C)
CPU0 Ice Lake (165W/205W)	88/82 (case)	165.0	12	205.0	3
CPU1 Ice Lake (165W/205W)	88/82 (case)	165.0	11	205.0	2
DDR4 LRDIMM/Apache Pass	95/84 (case)	12	20	12/18	14/0
CPU VRs	105 (board)	8.3	19	10.3	20
DIMM VRs	105 (board)	3.4	31	8.4	32
BMC AST2500	106 (case)	1.5	29	1.5	31
PCH(LBG-1G)	86 (case)	15.0	14	15.0	15
Intel SSD DC D4800X SFF U.2 1.5TB	70 (case)	25.0	9	25.0	14
OCP 3.0 Network Interface Card					
ASIC	105 (junction)	35.0	28	35.0	33
QSFP	70 (case)	3.5	7	3.5	12
PCIe AIC	105 (junction)	-	-	75.0	-56
PSU1	55 (inlet)		6		7
PSU2	55 (inlet)		4		2

Below are are projections for key components when using a 1U Extended Volume Air Cooling (EVAC) thermal solution option.

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	Inlet Temperature (°C)	40		35	
Description	Tspec (°C)	TDP (W)	Margin(°C)	TDP (W)	Margin(°C)
CPU0 Ice Lake (165W/205W)	88/82	165.0	13	205.0	6
CPU1 Ice Lake (165W/205W)	88/82	165.0	12	205.0	5
DDR4 LRDIMM/Apache Pass	95/84	48.0	19	120.0	13/-1
CPU VRs	105	8.3	19	10.3	20
DIMM VRs	105	3.4	31	8.4	32
BMC AST2500	106	1.5	29	1.5	31
PCH(LBG-1G)	86	15.0	14	15.0	15
Intel SSD DC D4800X SFF U.2 1.5TB	70	25.0	9	25.0	14
OCP 3.0 Network Interface Card					
ASIC	105	35.0	28	35.0	33
QSFP	70	3.5	7	3.5	12
PCIe AIC	105			75.0	-56
PSU1	55		6		7
PSU2	55		4		2

6.2 Thermal Management

Refer to BMC Sensor Monitoring section

6.3 PROCHOT#

PROCHOT# is a bidirectional pin used to signal that a processor internal temperature has exceeded a predetermined limit and is self-throttling (rarely used), or as a method of throttling the processor by an external source (more frequently used).

The ICX Processor controller toggles PROCHOT# (OUTPUT mode on ICX Processors) when it goes into throttling mode. The duty cycle of PROCHOT# toggling over a period of time indicates the amount of throttling initiated by the ICX Processor cores. The BMC Firmware does not monitor PROCHOT# to determine CPU throttling percentage. Instead, it will obtain outbound ICX Processor throttling data via the PECI interface.

An external source can also toggle the PROCHOT# (Input mode on ICX Processor) to force the processor into throttling mode. This usually happens when the system reaches a certain thermal threshold. In the Whitley platform implementation, VRHOT# is an output of the ICX processor VR13 controller, which is capable of throttling the processor via PROCHOT#. Additionally, logic on the baseboard will assert PROCHOT# if a PMBUS Alert is asserted. The ME can also force a throttle event via the same logic block. Finally, a Power Supply can assert its PMBUS_ALERT_N signal due to an over current event, which will assert the PROCHOT# pin (also known as Fast PROCHOT#).

6.4 MEMHOT_IN#, MEMHOT_OUT#

ICX changed MEMHOT# from a bi-directional signal to 2 uni-directional signals MEMHOT_IN# and MEMHOT_OUT#. The ICX Uncore (Memory Controller) drives the MEMHOT_OUT# active LOW when it goes into throttling mode for external agent (i.e. BMC) monitoring. An external source toggles the MEMHOT_IN# to force the memory controller to go into throttling mode. This happens when the system reaches a certain power / thermal threshold. In the Whitley platform implementation, VRHOT# is an output from the memory subsystem VR13.0 controller, which is capable of throttling the ICX memory controller via MEMHOT_IN#.

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Logic on the baseboard will assert MEMHOT_IN# if a PMBUS Alert is asserted from the system PSU. The ME can also force a MEMHOT_IN# event via the same logic block. Management firmware monitors the memory subsystem VR13.0 VRHOT# and creates a SEL event if VRHOT# is asserted.

6.5 THERMTRIP# / MEMTRIP#

ICX also changed one THERMTRIP# signal to two signals THERMTRIP# and MEMTRIP#, used by the Processors to tell the system that a Thermal threshold has been achieved in either the Processors or Memory and that the system must be shut down immediately.

THERMTRIP# pin on ICX processor indicates a Core Catastrophic Thermal Event

MEMTRIP# pin on ICX processor indicates Memory Subsystem (DIMMs) Catastrophic Thermal Event

On the Junction City board the THERMTRIP# pin will be configured to signal Processor catastrophic thermal events to the PCH. The MEMTRIP# pin will be connected to the BMC for Memory catastrophic thermal events logging, the DIMM EVENT# pin connected to PCH THERMTRIP# input is used to shut down the system immediately.

6.6 Thermal Sensors

Thermal sensors and their integration with the thermal management implementation create the opportunity for optimization. However, because many of the component interactions will not be known until completion of the Junction City board layout, some of the optimal board sensor locations are to be determined, however onboard temperature sensors are needed to monitor air inlet and exhaust temperature. To accommodate this unknown aspect placeholders have been added for board sensors. The following table summarizes the list of thermal sensors to be used for thermal management. And, Figure 6-1 shows the approximate locations of on-board thermal sensors. The maximum allowable tolerance of thermal sensors in the motherboard is +/-2°C.

Table 7-2: Thermal Sensors

Component	Sensor Type	Location	Access	Quantity	Use
ICX Processor	DTS	On-processor die	PECI	1	Shutdown, Throttling
Processor VRD 13	Processor VRHOT#	Processor VRD 13	SVID	1	Throttling
Lewisburg-R 1G	DTS	Lewisburg Die	SMB	1	Shutdown
Board sensor	TMP75	Inlet & Exhaust	SMB	2	Throttling

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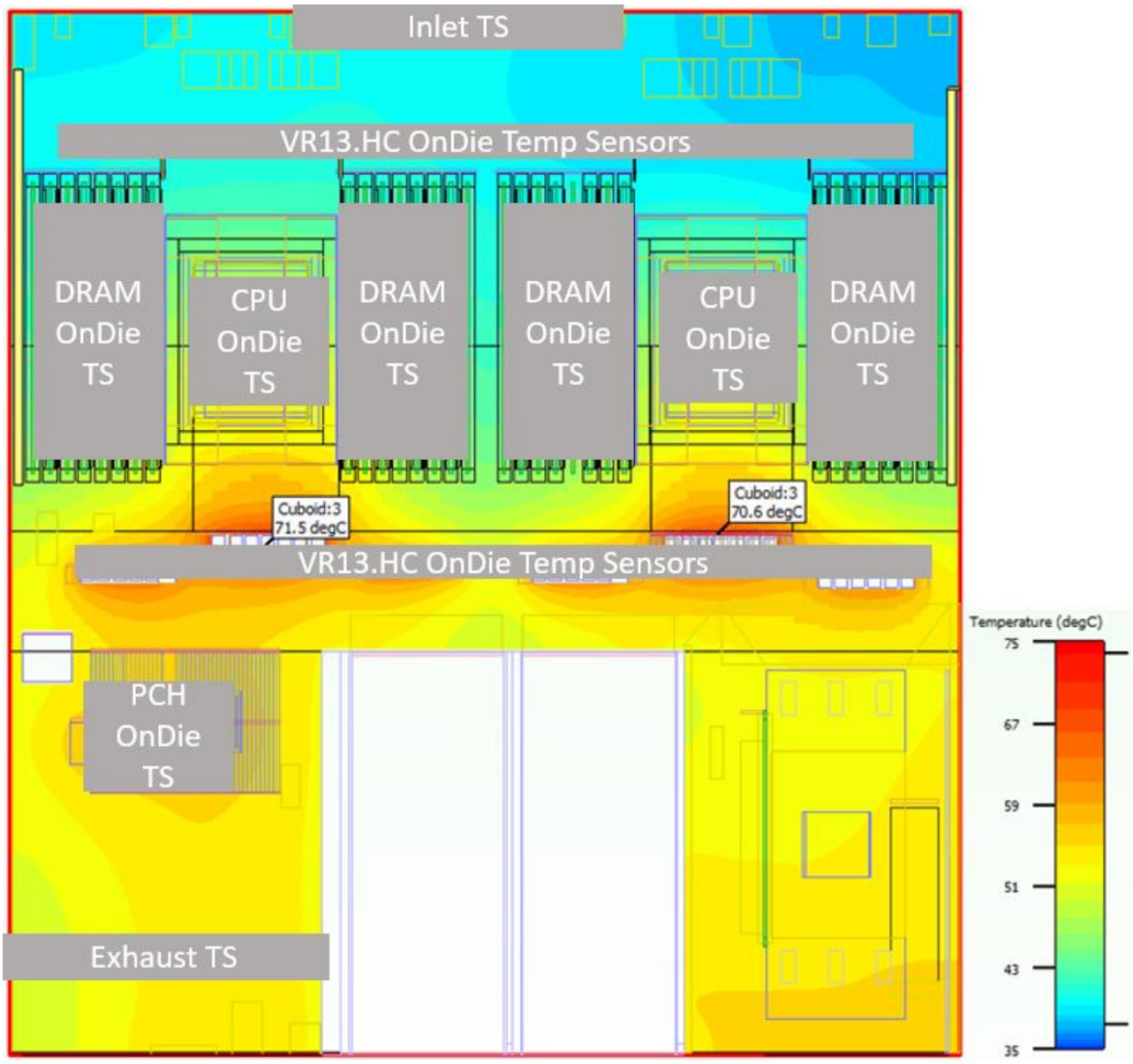

Figure 6-1 Board Temperature Sensor Placement

6.7 Environment Conditions

DC Environment conditions:

- 3,000 feet (950 m) above sea level
- Cool-Aisle Range between 10°C and 35°C (50°F to 95°F)
- Relative Humidity - Range between 20% and 80%

7. I/O System

7.1 PCIe Topologies

Junction City is designed to support 2x PCIe 1U Riser slots for Rear Panel access, with the remaining ICX direct PCIe interfaces (x48 per CPU) towards the Front Panel supporting:

- 2x OCP 3.0 Right Angle Connectors supporting PCIe Gen4 x16 per connector
- 4x U.2 SFF Right Angle Connectors for PCIe Gen4 (x4) Hotswap supported NVMe SSDs per connector
- 6x EDSFF Vertical Mount Connectors for PCIe Gen4 (x8) to either HSBP on Top Row Front Panel or additional PCIe bandwidth to Rear AIC
- Junction City also supports 2x M.2 (80 or 110mm) PCIe Gen3 (x2) Boot locations from the LBG-R PCH.

Table 7-1 PCIe Lane Mapping

Device	Technology	Port	# of Lanes	Bifurcation supported
OCP0	Gen4	CPU0 PE2	16	x16, x8, x4
OCP1	Gen4	CPU1 PE0	16	x16, x8, x4
EDSFF0	Gen4	CPU0 PE1 [7:0]	8	x8, x4
EDSFF1	Gen4	CPU0 PE1 [15:8]	8	x8, x4
EDSFF2	Gen4	CPU0 PE0 [7:0]	8	x8, x4
EDSFF3	Gen4	CPU1 PE2 [15:8]	8	x8, x4
EDSFF4	Gen4	CPU1 PE1 [15:8]	8	x8, x4
EDSFF5	Gen4	CPU1 PE1 [7:0]	8	x8, x4
SSD0	Gen4	CPU0 PE0 [11:8]	4	x4
SSD1	Gen4	CPU0 PE0 [15:12]	4	x4
SSD2	Gen4	CPU1 PE2 [3:0]	4	x4
SSD3	Gen4	CPU1 PE2 [7:4]	4	x4
RISER0	Gen4	CPU0 PE3	16	x16, x8, x4
RISER1	Gen4	CPU1 PE3	16	x16, x8, x4
CPU Total			64 per CPU	
BMC	Gen2	PCH PCIE[2]	1	x1
M.2 A	Gen3	PCH PCIE[5:4]	2	x2, x1
M.2 B	Gen3	PCH PCIE[7:6]	2	x2, x1
PCH Total			5	

7.2 USB

Junction City is designed to support redundant USB3.0 for Front and/or Rear panel access. Front panel will support 1x USB3.0 and 1x USB2.0, and Rear panel will support 2x USB3.0. USB power delivery is controlled by onboard TPS2557 USB power switch for each USB connector.

7.3 SATA

Junction City can support up to x12 sSATA miniSAS connection near the PCH section of the baseboard. Junction City will not support SATA boot option from PCH (see M.2 section for clarification)

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7.4 M.2

Junction City is designed to support dual M.2 locations on the baseboard next to the PSUs. M.2 supports PCIe x2 for each location. SATA interface is not supported on either M.2, due to limitation of routing length exceeding Whitley PDG recommendations. Junction City will support 80mm or 110mm length modules.

7.5 Fan Connectors

There are 7x 16pin fan connectors located on the baseboard located near the Midplane connector edge. Junction City can support either Single or Dual Rotor 40Wmax System Fans along the Midplane cut-out locations. There are also 3x CPU/System single rotor fan 4pin headers for open chassis debug purposes.

Table 7-1 4Pin CPU Fan Header Single Rotor Fan Pinout

	Fan Header		**Fan Cable**	
Fan Connector Spec	**Signal Description**	**Baseboard Connector Pin**	**Wire Color**	**Fan Connector Pin**
	GND	1	Black	1
	12V	2	Yellow	2
	Tach/Sense (NC)	3	Green	3
SSI	PWM (Control)	4	Blue	4
P/Ns		C74770-001 (White)		Molex 47054-1000(White)

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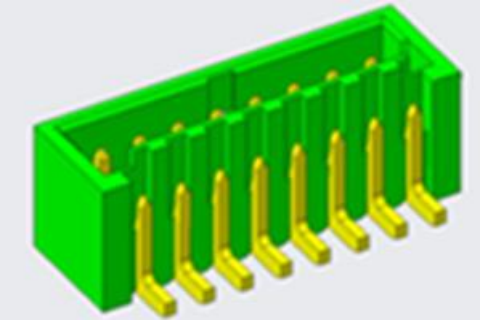

Figure 7-1 8pin 1U System Fan Connector

Table 7-2 8Pin 1U 40W Fan Pinout (**FAB2 Update**)

	Signal Description	Baseboard Connector Pin
	PWM (Control)	1
	Tachometer2 (Sense)	2
	+12V	3
	GND	4
	PWM (Control)	5
	Tachometer1 (Sense)	6
	+12V	7
	GND	8
P/N	**Foxconn HSM1080-L0000-9H**	

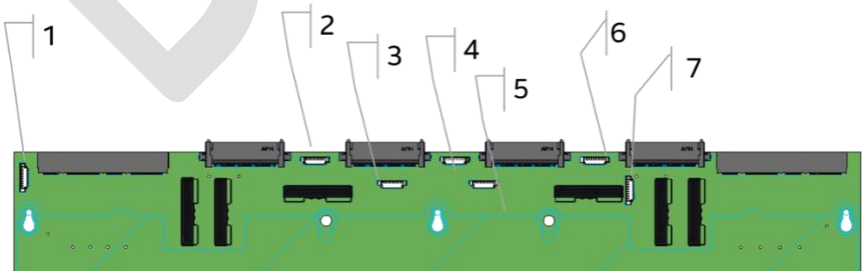

Figure 7-2 Front Midplane Fan Connector Locations (7x)

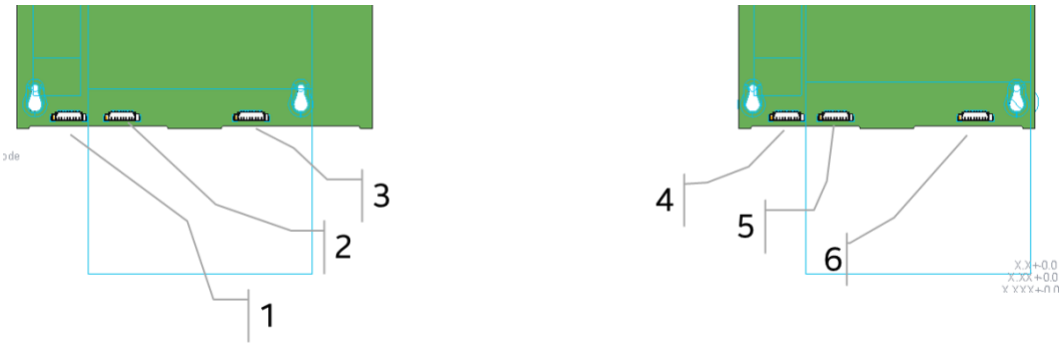

Figure 7-3 Rear Fan Connector Locations (6x) – No Longer Supported in FAB2

7.6 TPM Module

Junction City will support a 12pin TPM connector to support Intel TPM Module. TPM design collateral provided to customers for manufacturing module to support Junction City. See below schematic pinout figure for the 12pin connector (AFCI 20021221-00312C4LF or equivalent). Also, see below figure of TPM module dimensions and retention solution.

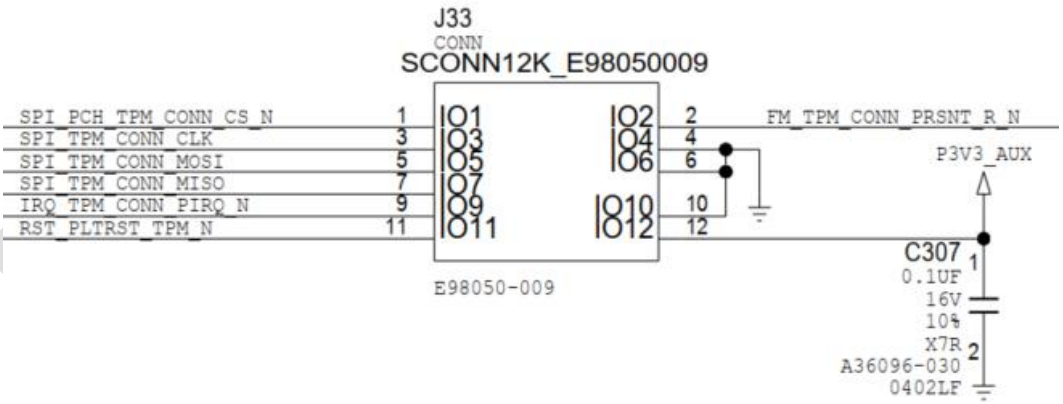

Figure 7-4 Intel TPM Module baseboard connector pinout

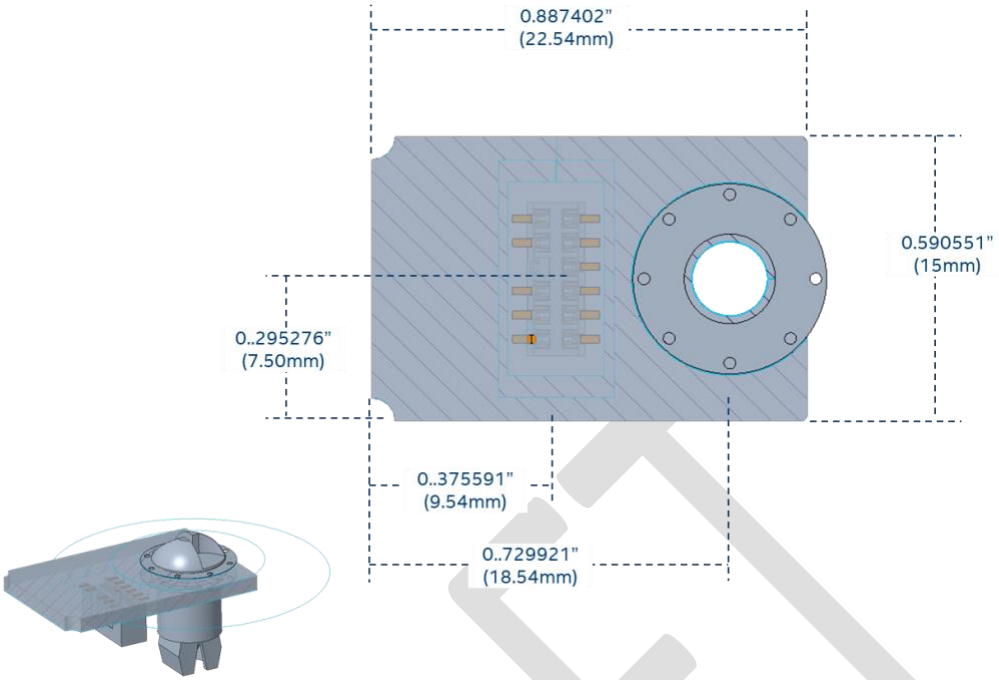

Figure 7-5 Intel TPM Module Dimensions & retention

7.7 Battery Connector (RTC)

Junction City RTC CR2032 Battery Holder.

Table 7-3 RTC Battery Holder

Device	Description	IPN	Comments
BT3A1	**BAT ACC, HOLDR, THM, CR2032**	C68619-006	CR2032 BATTERY HOLDER 3PIN THRU-HOLE BLACK, /HF, LOTES, AAA-BAT-043-Y14

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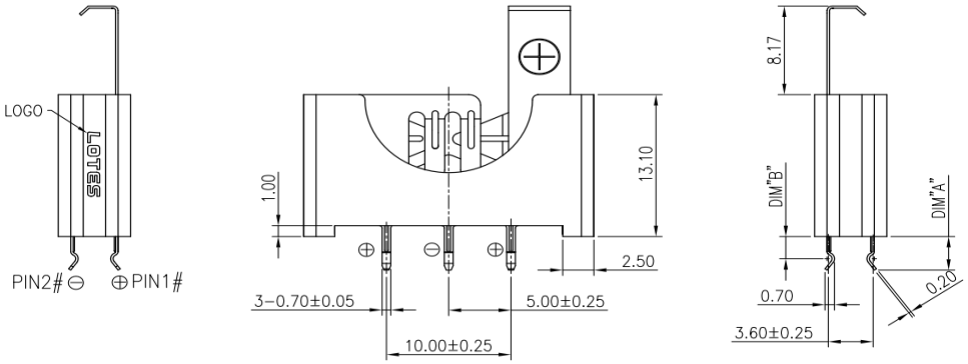

7.8 Headers and Jumpers

Below provides a summary and description of headers utilized by the baseboard.

Table 7-4 Summary of Headers and Jumpers

RefDes	Header type	IPN	Function	Settings
J4D4	2.54mm, 1x3, VT, SMT, Header	D14776-017	LT Key Downgrade Jumper	1 - 2 LT Key Downgrade Disabled When High (Prod) 2 - 3 LT Key Downgrade Enabled When Low (Debug)
J49	2.54mm, 1x3, VT, SMT, Header	D14776-017	ME FW Update Jumper	1 - 2 Normal (Default) 2 - 3 ME Force Update
J51	2.54mm, 1x3, VT, SMT, Header	D14776-017	BIOS USB Recovery Jumper	1 -2 Normal Operation (Default) 2 - 3 BIOS USB FLASH Recovery Mode
J48	2.54mm, 1x3, VT, SMT, Header	D14776-017	Password Clear Jumper	1 - 2 Normal (Default) 2 - 3 Password Clear
J50	2.54mm, 1x3, VT, SMT, Header	D14776-017	Top Swap Strap Jumper	1 - 2 Normal (Default) 2 - 3 Top Swap Enabled
J7E1	2.54mm, 1x3, VT, SMT, Header	D14776-017	BMC Force Update Jumper	1 - 2 Normal Operation (Default) 2 - 3 Force BMC Update
J36	2.54mm, 1X3, VT, PLG, Header	A91829-001	BMC Remote Debug Jumper	1 - 2 Enable BMC Remote Debug 2 - 3 Disable BMC Remote Debug (Default)

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J37	2.54mm, 1X3, VT, PLG, Header	A91829-001	ESPI Enable Jumper	1 - 2 ESPI Enabled (Default) 2 - 3 ESPI Disabled (LPC)
J46	2.54mm, 1X3, VT, PLG, Header	A91829-001	CMOS Clear	1-2 Normal RTC Reset (Default) 2-3 Clear RTC Registers

7.8.1 FORCE BMC UPDATE – J7E1

When this 3-pin jumper is set, it puts the BMC Firmware in update mode, which enables the user to update BMC Firmware code when necessary. BMC's GPIOE should be strapped LOW when BMC Firmware update is required.

Table 7-5 Force BMC Update Jumper

JUMPER POSITION	MODE OF OPERATION	NOTE
1-2	NORMAL	BMC GPIOE is pulled HIGH. **Default position.**
2-3	UPDATE	BMC GPIOE is pulled LOW.

7.8.2 BIOS RECOVERY MODE – J51

The Whitley platform utilizes BIOS recovery to repair the system BIOS from SPI flash corruption in the main BIOS application code and Boot Block code. This 3-pin jumper is used to reload BIOS when the image is suspected to be corrupted. Lewisburg PCH GPIO should be strapped LOW when BIOS recovery is required. See BIOS Supported Jumper section for more details on the functionality of this jumper.

Table 7-6 BIOS Recovery Mode Jumper

JUMPER POSITION	MODE OF OPERATION	NOTE
1-2	NORMAL	Lewisburg PCH GPIO is pulled HIGH. **Default position.**
2-3	RECOVERY	Lewisburg PCH GPIO is pulled LOW.

7.8.3 RESET BIOS CONFIGURATION – J46

This jumper used to be the CMOS Clear jumper. The BIOS DEFAULT jumper is tied to Lewisburg's RTCRST# pin. When this pin is asserted, the RTC_PWR_STS bit (D31:F0:A4h.2) in Lewisburg will be set, and the configuration bits in the RTC well will be set to their default state. BIOS inspects RTC_PWR_STS during boot to determine if the data in the NVRAM needs

to be set to default. See BIOS Supported Jumper section for more details on the functionality of this jumper.

Table 7-7 BIOS Default Jumper

JUMPER POSITION	MODE OF OPERATION	NOTE
1-2	NORMAL	Lewisburg PCH RTCRST_N pin is pulled HIGH. **Default position.**
2-3	RESET BIOS CONFIGURATION	Lewisburg PCH RTCRST_N pin is pulled LOW.

7.8.4 BIOS TOP SWAP - J50

The PCH supports a “Top-Block Swap” mode that has the PCH swap the top block in the FWH or SPI flash (the boot block) with another location. This allows for safe update of the Boot Block (even if a power failure occurs). When the “top-swap” enable bit is set, the PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines as selected in Boot Block Size (BOOT_BLOCK_SIZE) soft strap for SPI.

Table 7-8 BIOS Image Swap Jumper

JUMPER POSITION	MODE OF OPERATION	NOTE
1-2	NORMAL	**Default position.**
2-3	Top Swap	Top Swap enabled position.

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7.8.5 Postcode & LEDs

Junction City can support Postcode debug thru Port80 LED onboard or from a connector supporting 3rd party module (see figure below showing module).

Port80 LED's Porch Area

Junction City Port80 discretd LED's are located on the poarch area.

Table 7-8 Discrete Port 80 Postcode LEDs on Portch

Location	Type	IPN	Function	Comments
DS5D2	LED (Green)	K19857-001	POST_CODE_0	
DS5D3	LED (Green)	K19857-001	POST_CODE_1	
DS5D1	LED (Green)	K19857-001	POST_CODE_2	
DS6D3	LED (Green)	K19857-001	POST_CODE_3	
DS6D1	LED (Orange)	C97278-023	POST_CODE_4	
DS6D2	LED (Orange)	C97278-023	POST_CODE_5	
DS6D5	LED (Orange)	C97278-023	POST_CODE_6	
DS6D4	LED (Orange)	C97278-023	POST_CODE_7	

Junction City Porch Port80 Postcode Card Connector.

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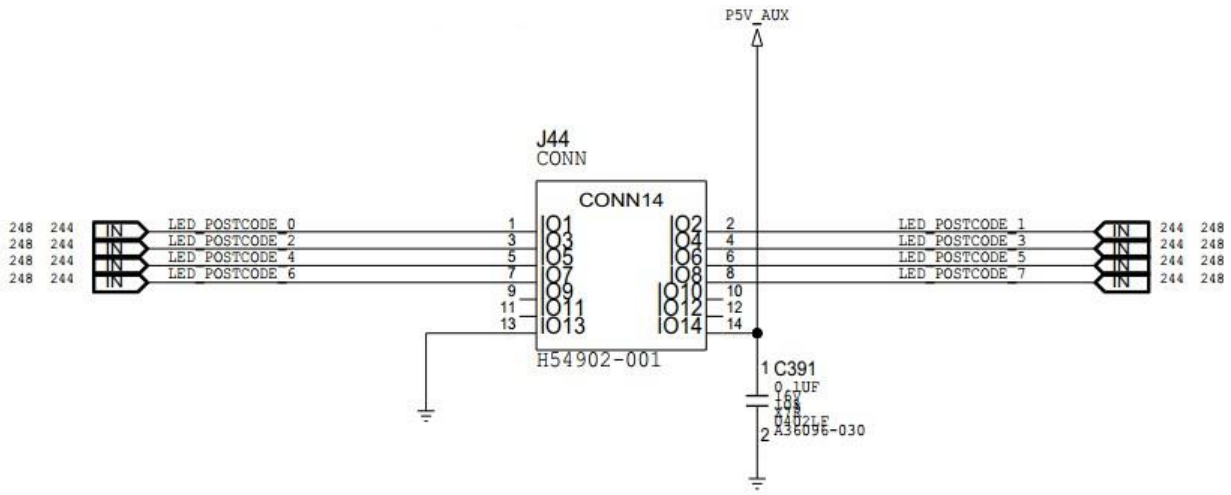

Figure 6 Port80 Postcode Debug Card Connector

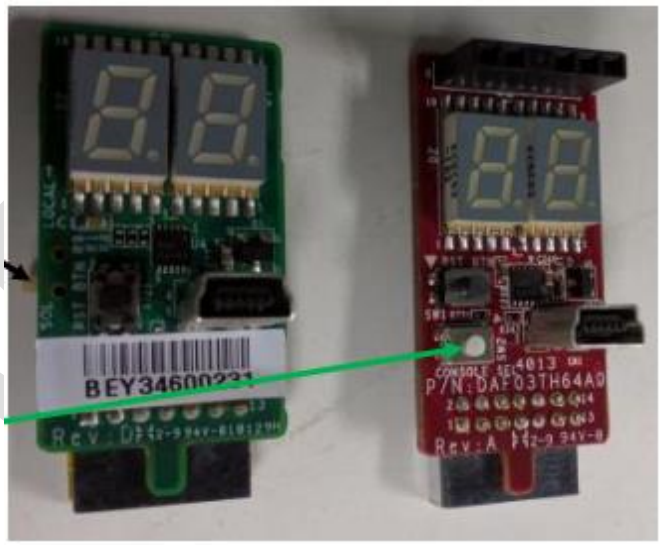

Figure 7 Example J44 Port80 POST Cards (used on Crescent City)

Junction City Porch Port80 Postcode SMT Dual Seven Segment Display.

Table 7-9 Port80 POST Seven Segment Display

Device	Description	IPN	Comments
DS8D5	LED DISP,8,2,8.00,MM,ORG,SM	K19852-001	

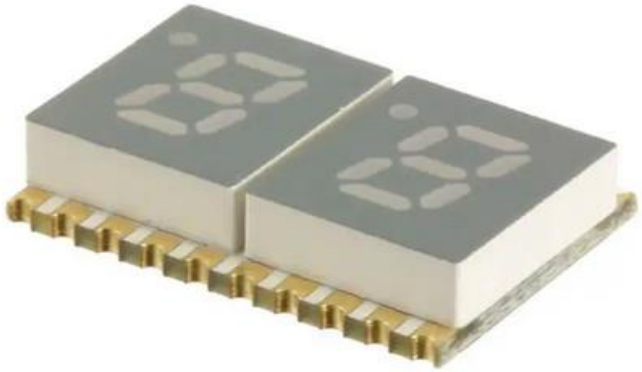

Figure 8 Example DS8D5 Port80 POST Seven Segment Dual Display

7.8.5.3 All other Onboard LEDs

Junction City baseboard and front/rear panel will support below LEDs for convenient identification of the board status.

Table 7-10 LEDs on Baseboard and Front & Rear Panel

Location	Type	IPN	Function	Comments
DS1C1	LED, SMT-GREEN	K19857-001	LED_PWRGD_P1V8_CPU0	
DS1C2	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCANA_CPU0	
DS1C3	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCIN_CPU0	
DS1C4	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCSA_CPU0	
DS1C5	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVPP_CPU0	
DS1C6	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVDDQ_CPU0	
DS1C7	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVTT_CPU0	
DS1C8	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCIO_CPU0	
DS2C1	LED, SMT-GREEN	K19857-001	PWRGD_P12V_STBY_LED	
DS2C2	LED, SMT-GREEN	K19857-001	PWRGD_P5V_STBY_LED	
DS2C3	LED, SMT-GREEN	K19857-001	PWRGD_P3V3_STBY_LED	
DS2C4	LED, SMT-GREEN	K19857-001	PWRGD_P1V2_BMC_STBY_LED	

DS2C5	LED, SMT-GREEN	K19857-001	LED_PWRGD_P12V_PCIE	
DS2C6	LED, SMT-GREEN	K19857-001	LED_PWRGD_P5V	
DS2C7	LED, SMT-GREEN	K19857-001	LED_PWRGD_P3V3	
DS2C8	LED, SMT-GREEN	K19857-001	LED_PWRGD_BMC_STBY_VRS	
DS2C9	LED, SMT-GREEN	K19857-001	LED_PWRGD_PCH_STBY_VRS	
DS2C10	LED, SMT-GREEN	K19857-001	LED_PWRGD_P12V_MAIN	
DS4A2	LED, 2NC-YELLOW	K44807-001	FM_SPEAKER_PCH_N	
DS4A2	LED, 2NC-YELLOW	K44807-001	FM_BEEP_LED_P	
DS5A3	LED, SMT-GREEN	K19857-001	LED_FPGA_HEARTBEAT_FET	
DS7C1	LED, SMT-GREEN	K19857-001	LED_BMC_HB_LED_D_N	
DS7C2	LED, SMT-RED	D14725-005	FM_RED_LED_ANODE	
DS7D1	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCIO_CPU1	
DS7D2	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVPP_CPU1	
DS7D3	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVDDQ_CPU1	
DS7D4	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVTT_CPU1	
DS8D1	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCIN_CPU1	
DS8D2	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCSA_CPU1	
DS8D3	LED, SMT-GREEN	K19857-001	LED_PWRGD_P1V8_CPU1	
DS8D4	LED, SMT-GREEN	K19857-001	LED_PWRGD_PVCCANA_CPU1	
DS9A1	LED, GREEN	C96565-011	LED_POWER_ANODE	
DS1	LED, DUAL, GREEN	C97900-011	FP_LED_STATUS_AMBER_R_N	
DS1	LED, DUAL, GREEN	C97900-011	FP_LED_STATUS_GREEN_R_N	
DS2	LED, SM-BLUE	D14725-016	FP_LED_ID_R_N	

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8. Mechanical (Chassis Concept ONLY)

8.1 System Chassis

Junction City chassis will feature a unique and highly configurable design. The chassis will be equipped with up to two high-efficiency 12VDC CRPS power supplies (hot-pluggable). High-performance dual rotor fans provide ample optimized cooling for the dual processor modules and up to twelve (12) hot-swappable drive bays for maximum storage capacity in a 1U form factor.

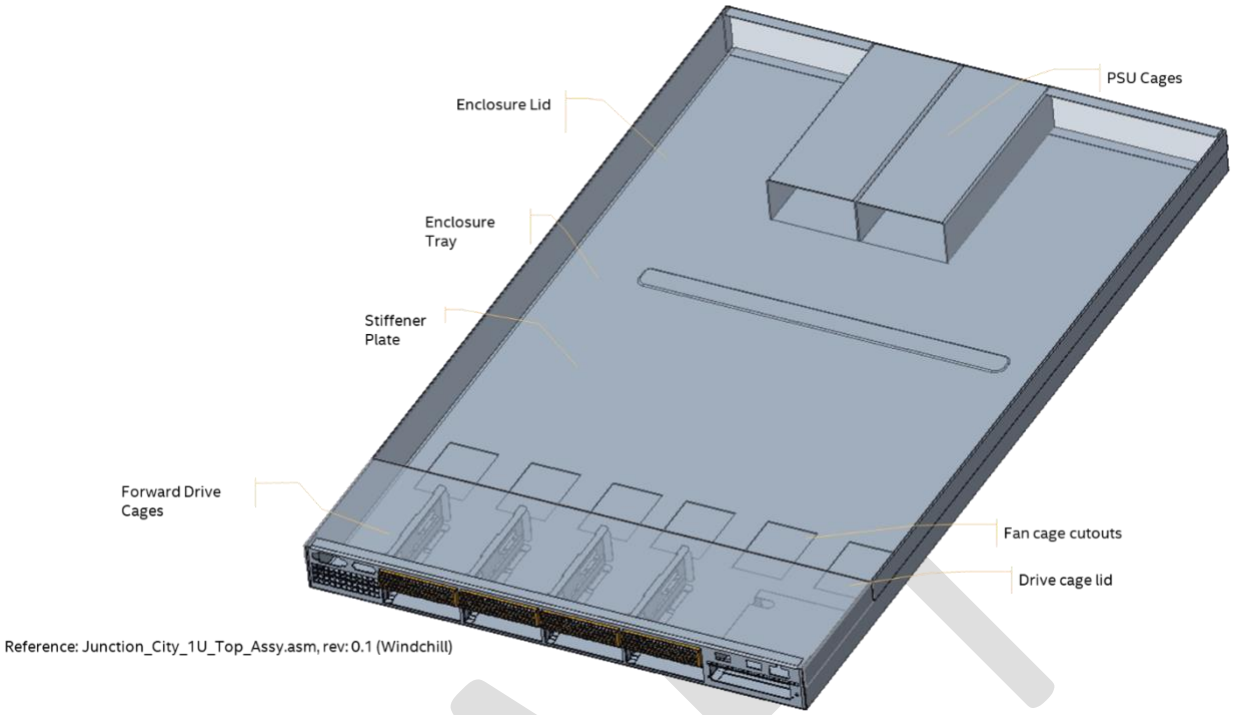

Figure 8-1 Junction City Chassis

Functional Area	Requirement	Comment
Chassis Dimensions	Chassis shall fit within a standard 1U 19” EIA rack.	See dimensions below
Materials	Chassis materials properties and strength shall meet or exceed the properties of SECC/SGCC electrogalvanized cold rolled steel	
Chassis Sag	Chassis sag shall not exceed 1.05mm	As measured by: Accounting for material thickness of the static rail, static rail deflection contribution, the tolerances associated with the material and assembly stack (flatness), residual rack dynamic shock and static sag, the chassis pan should not interfere with server chassis U space below.
Cable management	Chassis shall provide cable management features to keep cabling secure and away from critical elements	
Chassis Rack assembly	Chassis shall move freely on rack side support brackets	Does not support sliding rails.
Side support bracket	Shall be installed in standard 19” EIA rack mounting holes	

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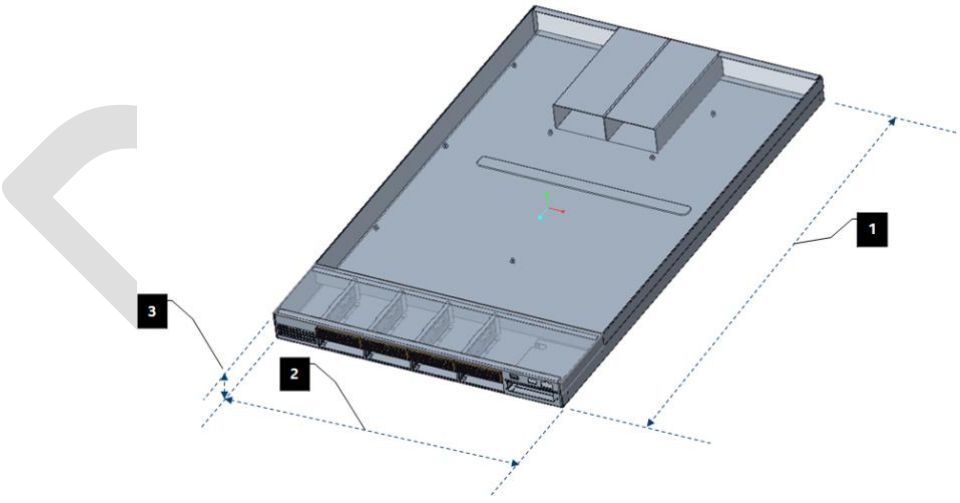
	Shall provide M6 mounting holes Vertical component of side bracket shall be outside the 450mm EIA Rack dimension	
Chassis Mount	M6 thumb screws at 465mm (±0.8) center to center	Mount to standard 19" EIA rack

8.1.1 Chassis Dimensions

Table 8-1. Chassis Dimensions

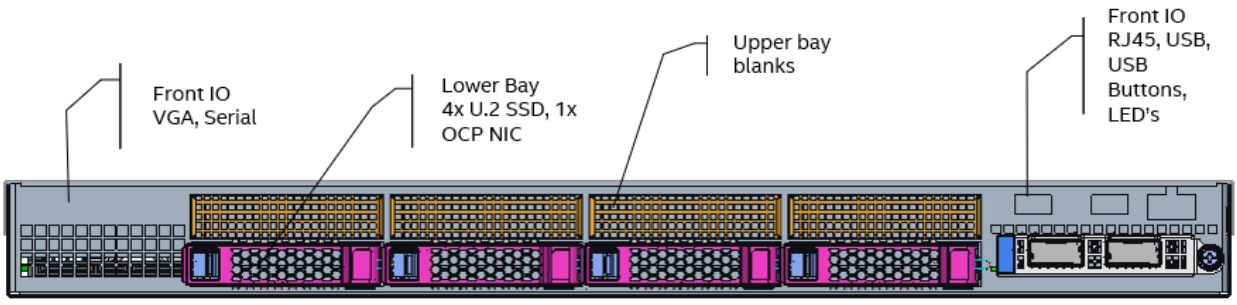
	Description	Dim	Tolerance
	Depth	752mm (29.61")	MAX
	Width	447mm (17.60")	MAX
	Height	43.4mm (1.71")	MAX

Figure 8-1 Junction City Chassis Dimension Key



8.1.2 Front Panel

Figure below shows a concept idea on how the Front Panel arrangement could be supported. Depending on the SKU and Midplane configuration for supporting OCPs and SSDs, as these locations are specific. Front panel supports access to OCP Module, U.2 NVMe SSDs, and Front IO option for Mgmt RJ45, Serial COM, VGA, USB, Pwr/Reset/ID buttons and status LEDs.



IO	U.2 SSD	U.2 SSD	U.2 SSD	U.2 SSD	IO
IO	U.2 SSD	U.2 SSD	U.2 SSD	U.2 SSD	OCP

Figure 8-2 Junction City Front Panel Concept

Horizontal SSD Drive Connector Pitch	72.17 mm (2.841”)
Vertical SSD Drive Connector Pitch	17.50 mm (.689”)

8.1.3 Rear Panel

Figure below shows a concept idea on how the Rear Panel arrangement could be supported. Rear panel will support access to PSUs, PCIe AICs on both the right and left side of PSU locations. Rear IO option for Mgmt RJ45, Serial COM, VGA, USB, Pwr/Reset buttons and status LEDs.

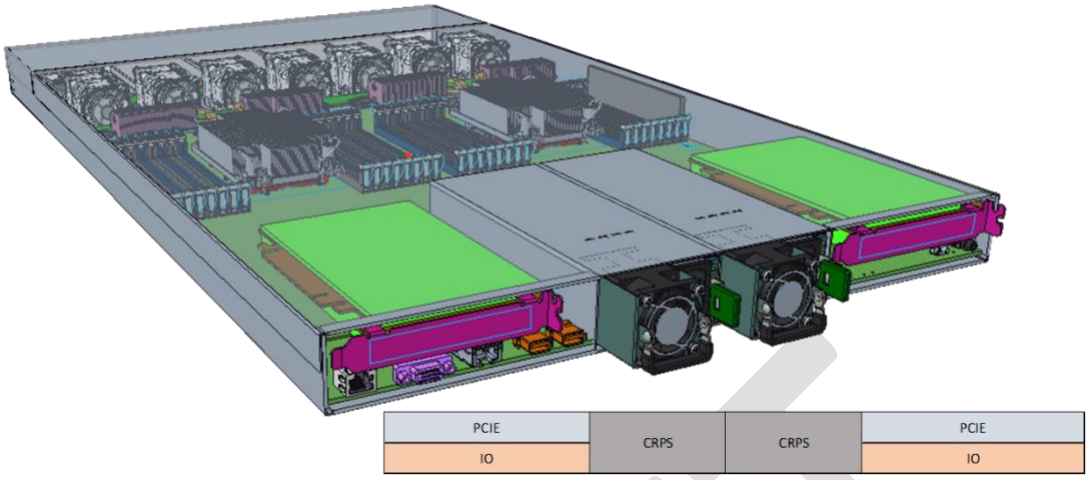


Figure 8-2 Junction City Rear Panel Concept

8.2 System Power Supplies

Junction City will support 1U Common Redundant Power Supplies (CRPS) +12VDC. The baseboard design will support 2x Power Edge Connectors for direct insertion of PSUs (No PDB required). Power Supply capacity will be dependent on configuration up to 1200W. Baseboard provides Hotplug support using MP5920 controller + 4 MP5991 EFUSEs in parallel. CRPS PSUs support 1+1, 2+0, and 1+0 redundancy configurations, with load sharing 1+1 as default, please refer to Intel Common Redundant Power Supply (CRPS) Design Guide for Servers (Doc ID# 573090) section 10.4 Cold Redundancy for details on CRPS redundancy. Junction City also supports Power Shelf +12VDC input, but recognizing analyzing the PS_ON state vs PS_PWRGD, P12V_PSU_Sensor resistor divider, and PSU Compatibility (B25 pin). If PS_ON state is Low, and PS_PWRGD, P12_PSU_Sensor are High the FPGA will determine the PSU source to be Power Shelf input, if and only if the B25 pin is 0V (in order to avoid faulty CRPS PS_ON signal to cause CRPS to power-ON as Power Shelf. If PS_ON, PS_PWRGD, P12V_PSU_Sensor are all Low, the FPGA will determine the PSU source to be CRPS and operate normally. See Figure below on connections and truth table on recognizing CRPS vs Power Shelf. B25 pin can also be defined as PS_KILL signal on certain CRPS PSUs, thus it is required to verify signal states prior to using this pin in the Power Sequencing FPGA logic. If PS_KILL or PSU holds signal low during AC power off, it can not be used for this purpose.

	PS_ON	PS_PWRGD	P12V_PSU_Sensor	B25 (Compatibility) GPIO	B25 (Compatibility) AN_IN
CRPS	0	0	0	1	Voltage Range Depending on CRPS
Power Shelf	0	1	1	0	0

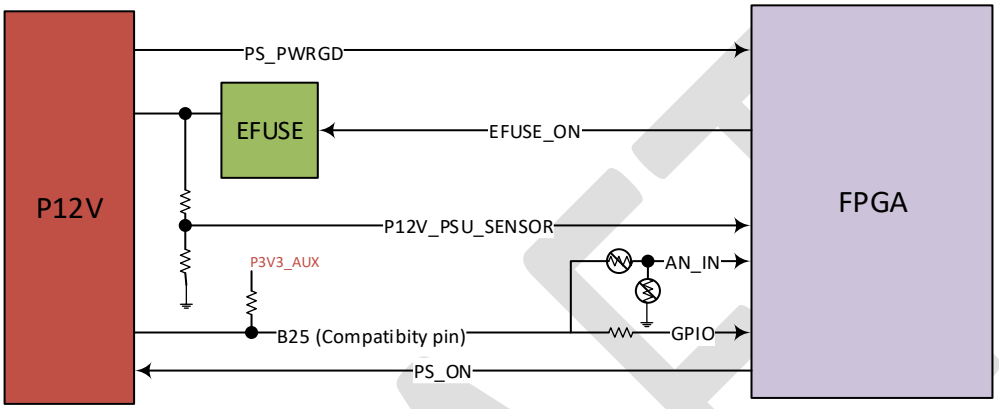


Figure 8-3 Power Shelf compatibility diagram and truth table during S5 (B25 is optional and can NOT be used if held low in AC power off state (Default – B25 Compatibility pin NOT monitored)

Figure 8-4 Intel CRPS 1U +12VDC Redundant Power Supply

8.3 System Fans

The system fan should have good relative power efficiency. The propagation of vibration

caused by fan rotation should be minimized and limited. The frame size of fan is 40x40mm.

The maximum thickness of fan should not be greater than 56mm. Fans will provide TACH output and PWM input. No fault or LED status is required. Junction City supports 7x 40x40x56mm Dual Rotor 12V Fans in the Midplane cutout locations. There are also 3x Debug CPU + System Fan locations to support benchtop testing of the baseboard. FAB2 design will replace all 7 fan connectors with higher power (40W max) capable fan power output, as opposed to the current 20W max fan connectors. Here a link to and example of the Dual Rotor fan for Junction City

- https://www.delta-fan.com/Download/Spec/GFC0412DS-DU49.pdf

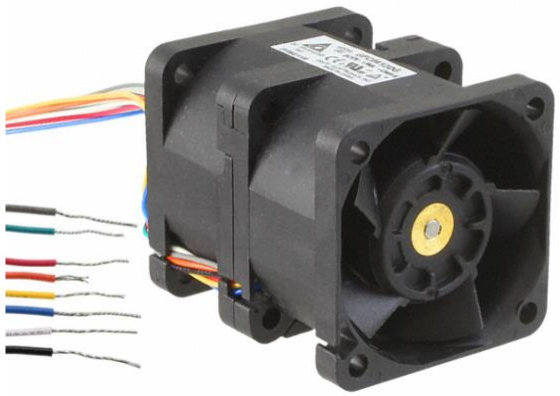


Figure 8-3 Example - Delta Dual Rotor Fan (GFC0412DS-DU49)

8.3.1 Fan Speed Control (FSC)

8.3.1.1 FSC Input

BMC needs to gather data as possible input of FSC. The data to be gathered includes:

Table 8-3 FSC Input Data Source

Type of Data	Data used for FSC input
Temperature	CPU0/1 core temperature from PECI
Temperature	TSOD of all DIMMs from PECI
Temperature	PCH temperature through SMLINK0
Temperature	Inlet and Exhaust air
Temperature	VR of CPU and DIMM
Temperature	Mezz card and PCIe card support thermal reporting interface
Temperature	U.2 & M.2 SSD through in-band and out-of-band interface (Depends on vendor support)
Fan Speed	All FAN tachometer inputs

8.3.1.2 FSC Requirements

- System design and fan speed control support N+1 redundancy for fan rotor failure
- A mix of PID control algorithm and step control is preferred. If only one control algorithm is used, PID is preferred.
- Hysteresis strategy needs to be considered to make sure FSC stable. FSC should try to avoid any fan speed oscillation.
- Step control based on the readings from all temperature sensors should be used before PID control is triggered. There should be fan PWM lookup tables for each critical thermal components such as CPU, DIMM, PCH, PCIe, and SSD.
- Once PID control is triggered, FSC should set fan PWM to the maximum PWM needed to maintain temperature at SP among all the critical thermal components.
- For PID control, K values should be fine-tuned in such a way that component temperature can be kept stable at SP during steady state and temperature oscillation is minimized

8.4 CPU Heat Sinks

Junction City can support both a Whitley Reference 1U Heatsink for low TDP ICX CPU's (≤165W) and an EVAC Remote Heatsink for higher TDP ICX CPUs (≥ 205W). However, certain configurations may allow for a Whitley Reference 1U Heatsink for TDP > 165W. Intel recommends performing thermal simulations and platform thermal stress testing based on customers' actual configuration. Whitley Reference 1U Heatsink is recommended for configurations that allow its use in order to reduce overall cost. EVAC heatsink would be a custom solution that would require customization with ODM. The heat sinks should be less than 26 mm to fit into 1RU space. The heat sink should have clear service guidance, such as screw installation sequence, torque requirement and air-flow direction provided by the ODM. See heatsink examples options below that were used in thermal simulations.

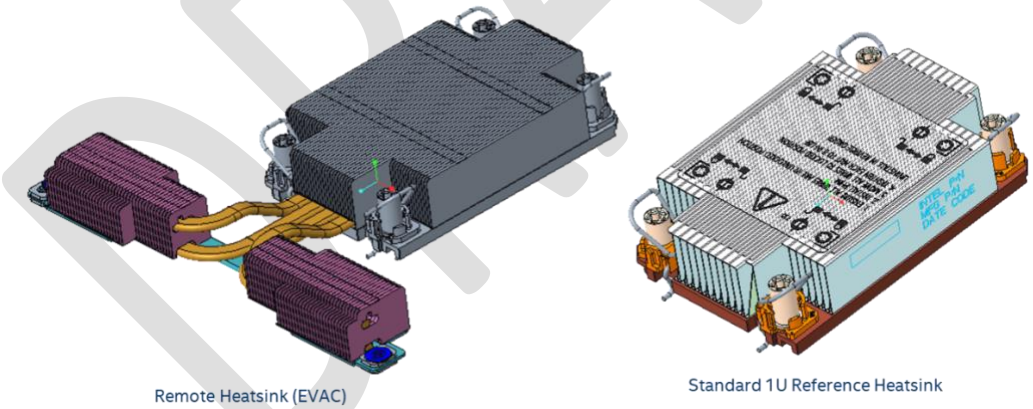


Figure 8-4 EVAC Remote Heat Sink Concept (only) and Standard 1U Reference Heat Sink (IPN K66289-001)

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8.5 System Cabling

Cables should be routed to minimize air flow blockage, secured in chassis, and have Keep Outs reserved for cable insertion/removal.

System Cabling includes:

- Front I/O slimSAS to Front Panel for supporting 1GbE Mgmt, Power/Reset Buttons, UID, and Status LEDs
- Front Panel access cables for USB3.0 (1x) and USB2.0 (1x)
- Front Panel access cable for Serial COM (DB9) & VGA (DB15)
- Up to 6x PCIe Gen4 cables from EDSFF (84pin SFF-TA-1009) to U.2 NVMe SSD (SFF-8639) panel mount for Hotswap capability of SSDs, cables include power delivery
- AC Power Cables (2x) for PSUs

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9. POWER

9.1 Board Power Budget

Board power budget (board circuitry capability) for Junction City baseboard is shown in Table 5-1 (below). The board hardware design is targeting maximum workload in hardware and VR design with adequate margin reserved, while target TDP for highest performance is 270W TDP per CPU (205W TDP limit for 1U Chassis support).

Table 9-1 Board Power Budget (Hardware Capability)

Junction City Max Power Budget	Quantity	Power per Item [W]	Utilization	Design Power [w]	Usage Power [w]
CPU (ICX-SP)	2	270	TDP	540	540
DDR4 LR-DIMM 3D4H 8Rx4 3200 16Gb (%80 Utilization) MAX Config of 24 DDR DIMMs + 8 BPS	24	12	80%	288	230.4
Barlow Pass (%80 Utilization) MAX Config of 24 DDR DIMMs + 8 BPS	8	18	80%	144	115.2
PCH (1G)	1	15	50%	15	7.5
PCIe Slots (1X75W Max allowed) (%80 Utilization)	1	75	80%	75	60
OCP 3.0 (2X 35W) (%80 Utilization)	2	35	80%	56	70
U.2 SSDs (%80 Utilization) Assumine 2x OCP, max 8 SSDs allowed)	8	25	80%	160	160
USB3.0 (4.5W) ; USB2.0 (2.5W) (%50 Utilization) Only 2xUSB allowed	2	5	50%	10	5
BMC, SPI, DDR and Clocks	1	10	80%	8	10
System Fans	7	40	100%	280	280
Miscellaneous (i.e. gate drive)	1	10	100%	10	10
VR Loss and PCB Loss	1	217	90%	217	195.3
Total Power for the Main Board				**1803**	**1683.4**

Junction City Max Power Budget is assume to consist 270W TDP, which is not POR for 1U Chassis (205W Max). Memory configuration is assumed to have 24 DDR4 LR-DIMMs + 8 BPS NVMe DIMMs for a Max power configuration. Storage solution will be limited to 8 SSDs, if 2x OCPs are installed, however up to 12x SSDs can be supported, if total power budget is understood. Remaining power consumption, such as Miscellaneous, VR Loss, PCB loss, and other small components on baseboard are rough estimates.

9.2 Power Delivery Architecture

9.2.1 Power Diagram

Power delivery diagram for Junction City (Figure 9-1) shows the architectural scheme for power distribution. Below key concerns and challenges in the baseboard power delivery design should be carefully taken care of:

- Power delivery scheme and VR solution is designed to support the maximum TDP design. Max current of each power rail is maximum numbers expected under the known target workload.
- Workload dependent core power rails of ICX (VCCIN, VDDQ) should share the same power source, so that maximum power budget sharing can be achieved and realized.

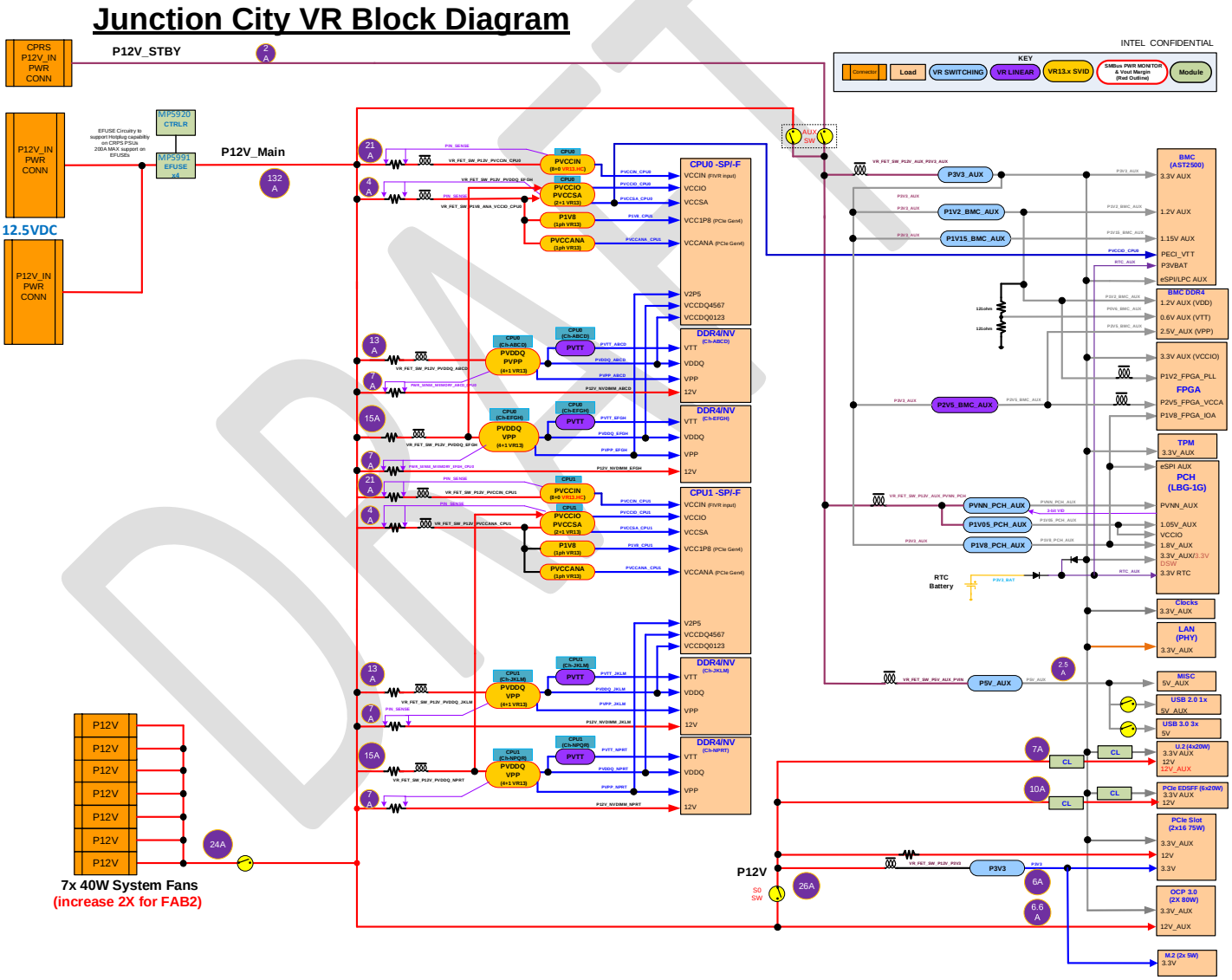

Figure 9-1 Junction City Power Delivery Block Diagram (FAB2 Update)Motherboard Power System

10. DEBUG FEATURES

Junction City should support below debug features to support product level debug requirements that align to customer requirements specific for Cloud Computing datacenter environments.

Debug hooks and features are listed below:

- At Scale Debug (ASD)
- Autonomous Crash Dump (ACD)
- Close Chassis Debug thru USB3.0 to support DCI (Front or Rear Panel access)
- XDP debug interface
- JTAG programming for MAX10 FPGA
- BIOS recovery
- USB connector for boot support (Front or Rear Panel access)
- M.2 PCIe x2 connector for boot support
- UART PCH connection (Serial console)
- BMC UART Debug Header
- Port80 Postcode (LED and Serial output)
- Optional Port80 (14pin) Debug Module

10.1 At Scale Debug (ASD) Support

Junction City supports BMC JTAG connections thru Level Shifters to connect into the JTAG chain for supporting ASD. ASD solution permits the BMC to act as a debug master to access the CPU and PCH remotely throught the BMC network management connection. Diagram below (reference Whitley PDG) shows the connections necessary on the platform to enable ASD. Please refer to the Whitley PDG for additional details to support ASD.

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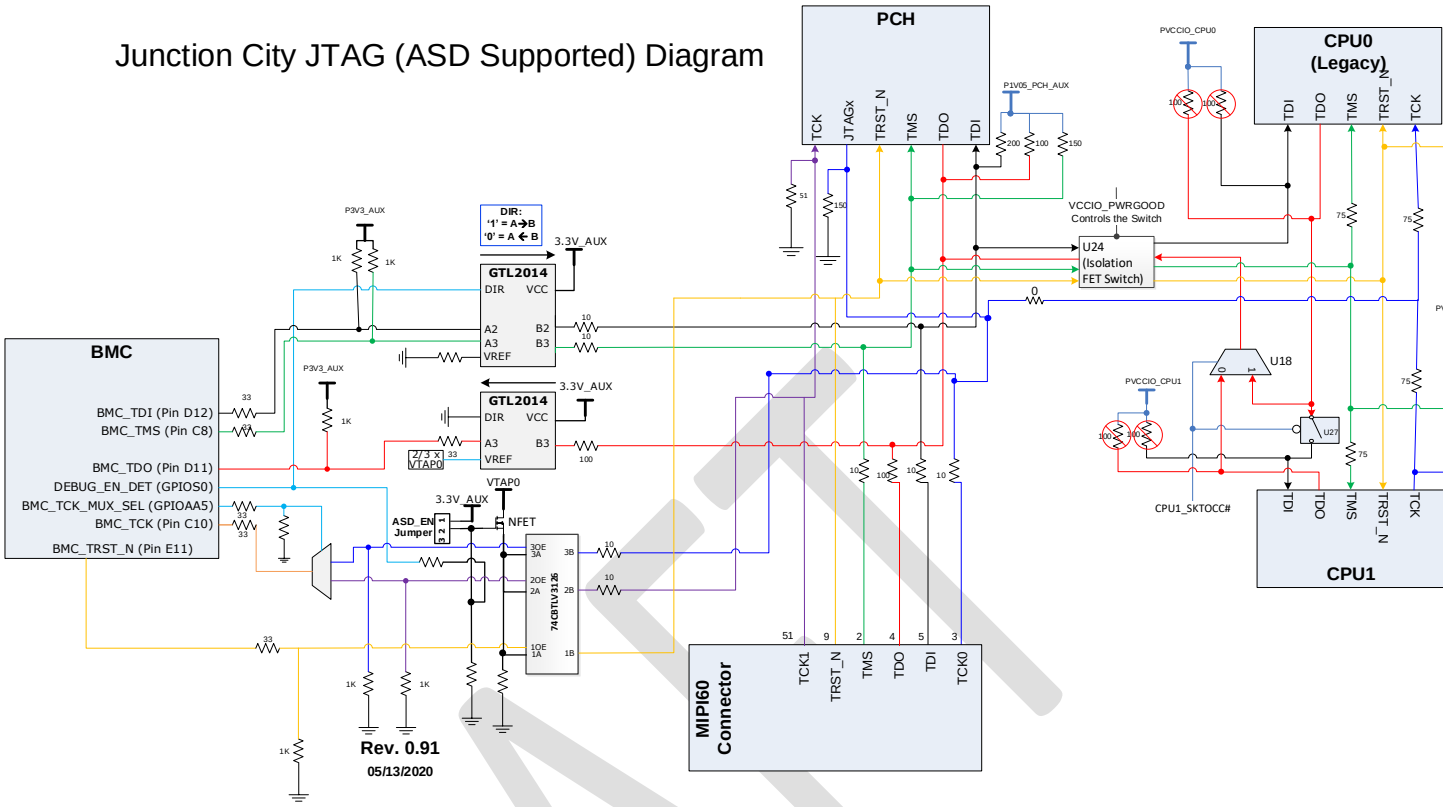

10.2 Autonomous Crash Dump Support (ACD)

Junction City will support ACD thru PECI interface to the BMC for logging crash dump in BMC DRAM for ICX platforms.

10.3 Intel® Direct Connect Interface (DCI)

Junction City will disable DCI by default. Datacenter's are encouraged to use ASD, rather than DCI due to Security risk of allowing external debug access at Front or Rear. However, customers do have the ability to enable this feature via onboard HW strap, with the understanding of such risks.

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