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Print name

Email address

Date 09/20/2018

Title Sr. Solutions Architect

Bound Entity Inespur Systems

Address
2: Scope

This document defines the technical specifications for the Open Compute Project Mission Bay 8 GPU

3: Overview

The Mission Bay will be contents 8 GPU base board that supports NVIDIA SXM2 GPU to provide a flexible feature set between technology leadership and cost.
Figure 1: System top view

Figure 2: System front view

Figure 3: System rear view
4: Feature Requirements

4.1: PCB/Switch/GPU

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td>Form Factor</td>
<td>No Standard</td>
</tr>
<tr>
<td></td>
<td>Layer</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>Color</td>
<td>Green</td>
</tr>
<tr>
<td></td>
<td>Board Size</td>
<td>450X590MM</td>
</tr>
<tr>
<td>Switch</td>
<td>Type</td>
<td>PLX9797</td>
</tr>
<tr>
<td></td>
<td>Vendor</td>
<td>Broadcom</td>
</tr>
<tr>
<td></td>
<td>PCIE</td>
<td>PCIE 3.0</td>
</tr>
<tr>
<td></td>
<td>Lane</td>
<td>97 lanes</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown</td>
<td>Yes</td>
</tr>
<tr>
<td>GPU</td>
<td>Type</td>
<td>SXM2 V100 、P100</td>
</tr>
<tr>
<td></td>
<td>Vendor</td>
<td>INVIDIA</td>
</tr>
<tr>
<td></td>
<td>Port</td>
<td>2个PCle3.0 x8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>P100： 4个NVLink1.0 x8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V100： 6个NVLink2.0 x8</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown</td>
<td>Yes</td>
</tr>
</tbody>
</table>

4.2 :Memory/Clock/Storage

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Generator</td>
<td>5P49V5901A750NLGI8</td>
<td></td>
</tr>
<tr>
<td>Clock Buffer</td>
<td>9ZX21901BKLFT 9DB834AGILFT</td>
<td></td>
</tr>
</tbody>
</table>
### 4.3: PCIE Slot

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIEX16</td>
<td>PCIE A0, PEXA&lt;16:31&gt;, UP Stream</td>
<td>J40</td>
</tr>
<tr>
<td>PCIEX16</td>
<td>PCIE A1, PEXA&lt;80:95&gt;, Down Stream</td>
<td>J29</td>
</tr>
<tr>
<td>PCIEX16</td>
<td>PCIE A2, PEXC&lt;80:95&gt;, Down Stream</td>
<td>J30</td>
</tr>
<tr>
<td>PCIEX16</td>
<td>PCIE B0, PEXA&lt;0:15&gt;, UP Stream</td>
<td>J41</td>
</tr>
<tr>
<td>PCIEX16</td>
<td>PCIE B1, PEXA&lt;64:79&gt;, Down Stream</td>
<td>J28</td>
</tr>
<tr>
<td>PCIEX16</td>
<td>PCIE B2, PEXB&lt;80:95&gt;, Down Stream</td>
<td>J26</td>
</tr>
<tr>
<td>PCIEX24</td>
<td>CPU Board connector, for fabric mode</td>
<td>J48</td>
</tr>
</tbody>
</table>

### 4.4: LAN

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAN1</td>
<td>Vendor</td>
<td>ASPEED</td>
</tr>
<tr>
<td></td>
<td>LAN Controller</td>
<td>AST2500</td>
</tr>
<tr>
<td></td>
<td>Transfers rate</td>
<td>10/100/1000Mb/s</td>
</tr>
</tbody>
</table>

### 4.5: External I/O

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>External I/O</td>
<td>1000M RJ45 with 1port</td>
<td>J56</td>
</tr>
<tr>
<td></td>
<td>Power Button</td>
<td>SW2</td>
</tr>
<tr>
<td></td>
<td>UID Button</td>
<td>SW1</td>
</tr>
<tr>
<td></td>
<td>BMC Reset</td>
<td>J123</td>
</tr>
</tbody>
</table>

### 4.6: Internal I/O

<table>
<thead>
<tr>
<th>Features</th>
<th>Description (type, Q'ty)</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEX9797 EEPROM Socket</td>
<td>For Switch FW, x3</td>
<td>J44/J22/J21</td>
</tr>
</tbody>
</table>
# 4.7: Onboard header

<table>
<thead>
<tr>
<th>Features</th>
<th>Description(Q’ty)</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-board header</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fabric select</td>
<td>X3</td>
<td>J37/J35/J32(x3)</td>
</tr>
<tr>
<td>VS/Base Mode select</td>
<td>X1</td>
<td>J51(x3)</td>
</tr>
<tr>
<td>MCU0/1 JTAG</td>
<td>Flash the MCU FW, x2</td>
<td>J50/J47(x5)</td>
</tr>
<tr>
<td>MCU0/1 UART</td>
<td>For MCU debug, x2</td>
<td>J46/J45(x3)</td>
</tr>
<tr>
<td>BMC Reload</td>
<td>X1</td>
<td>J98(x3)</td>
</tr>
<tr>
<td>Phy disable</td>
<td>X1</td>
<td>J125(x3)</td>
</tr>
<tr>
<td>Sharelink disable</td>
<td>X1</td>
<td>J126(x3)</td>
</tr>
<tr>
<td>Video disable</td>
<td>X1</td>
<td>J91(x3)</td>
</tr>
<tr>
<td>BMC Uart</td>
<td>X1</td>
<td>J104(x4)</td>
</tr>
<tr>
<td>SYS Uart</td>
<td>X1</td>
<td>J53(x4)</td>
</tr>
<tr>
<td>1278 I2C header</td>
<td>X1</td>
<td>J38(x3)</td>
</tr>
<tr>
<td>9797 VR I2C header</td>
<td>X1</td>
<td>J36(x3)</td>
</tr>
</tbody>
</table>

PEX9797 I2C Connector: For switch debug, x1
PEX8608 I2C Connector: For 8608 debug, x1
CPLD JTAG: For CPLD FW, x1
GPU Connector: Two connector for one GPU, x16
GPU JTAG: X8
BMC FLASH Socket: For BMC FLASH, x1
RTC Battery Socket: Battery, x1
IPMB Connector: For IPMB, x1
Power Connector: For Power, x9
5: Architecture Block Diagram

5.1: MB block diagram

The GPU board user 3 PEX9797s for PCIE fan out and PCIE management. It has 8 SXM2 GPUs mounted under the switch. It also use BMC for board management and PEX8608 for fabric usage. Its block diagram is as follows.

GPU Block Diagram
● PEX9797 x3, for PCIE fan out
● PEX8608 for PCIE management signal router
● SXM2 GPU is the PCIE device
● The MCU manages GPU power and sideband signals.
● The CPLD controls power on/off
● AST2500 for Box management
● 1 X24 GEN3 PCIE slot for management CPU board
● 2 x16 GEN3 PCIE slot for upstream to host
● 4 x16 GEN3 PCIE slot for downstream to endpoint
● 1 management LAN from BMC for box management
● 1 external uart for BMC debug
● 1 external uart for CPU debug

5.2: Chipset support

5.2.1 PEX9797 & GPU chipset:

PEX9797 is 96 lanes PCIE 3.0 PCIE switch. It has fanout mode and fabric mode. Fanout mode is the transparent bridge for host and endpoint. Fabric mode provide some advanced features such as PCIE management and Endpoint allocation etc,

In this GPU box, all of the three switches are configured as 6 x16 ports. The 9797_A port P0 and P4 are for upstream, others are for downstream.
The 8 GPUs are PCIe endpoints by PCIE x16 port. In the GPU box, the NVLink topology compatible with SXM2 V100 and P100.

5.2.2 PEX9797 fabric mode

Fabric mode is for advanced research, the mode could support such as dual hosts, management PCIe endpoint and allocate endpoints from one to another. PEX9797 use the PCIE lane96 to connect management CPU (Avaton C2350, CPU Board) for the feature. For example, we can decide which gpu belongs to host0, and then change it to host1. The Avaton CPU is the management CPU for PEX9797, the management signal is route to PEX8608 first.
5.3 Clocking

The system uses CFC clock generated locally. All PCIE switch and PCIE endpoint clocks come from the same clock buffer. The diagram as follows.

- 18X 100MHZ for PCIE
- 8X 156MHZ for GPU NVLink
5.4: On Board Slot

Refer to 1.5 for details.

5.5: BMC

- ASPEED AST2500 chip with 4Gb DRAM
- Embedded NIC dedicated for management, 100/1000 Mbps port
- 1 COM ports support
- Embedded video (VGA) with 16MB video memory
- SMBUS 2.0 specification compliant
- Thermal sensor

5.6: I/O connector or onboard header

- 1 x1000M RJ45 connector for dedicated LAN
- 2 of 6 PCIe x16 slots for upstream, 4 ports for device.
- 1 x24 PCIe 3.0 slot for management cpu.
- 1 x6pin I2C header for 9797 debug
- 1 x5pin JTAG header for MCU FW
- 1 x10pin JTAG header for CPLD FW
- 1 x30 pin IPMB connector for BMC communication, IPMB bus based on I2C interface

6: Environmental Requirements

This section provides regulatory and compliance information applicable to this system.

6.1 Product Regulatory Compliance

Markings

This product shall be certified with the following Product Certification Markings for any deployments for their respective regions.

6.2 Operating environment

- Operating temperature: 5°C to 40°C (41°F to 104°F)
- Non-operating temperature: -40°C to 70°C (-40°F to 158°F)
- Operating relative humidity: 20% to 85%RH
- Non-operating relative humidity: 10% to 95%RH