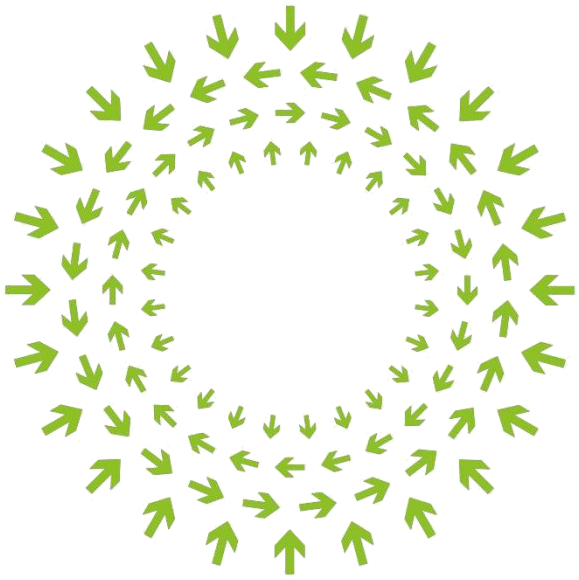


OPEN
Compute Project

Inspur 4 Socket Server Whistler System Design SPEC

Rev 0.1

Author:

Inspur Whistler Team

Table of Contents

1. License

"As of 6/21/2019, the following persons or entities have made this Specification available under the OCPHL-P, which is available at https://146a55aca6f00848c565-a7635525d40ac1c70300198708936b4e.ssl.cf1.rackcdn.com/files/bbcc4243e687a86e6e0e7c54afdada4350e2c294.pdf and by request to Inspur, Inc.

You can review the signed copies of the Contributor License for this Specification on the OCP website which may also include additional parties to those listed above.

Your use of this Specification may be subject to other third party rights. THIS SPECIFICATION IS PROVIDED "AS IS." The contributors expressly disclaim any warranties (express, implied, or otherwise), including implied warranties of merchantability, non-infringement, fitness for a particular purpose, or title, related to the Specification. The entire risk as to implementing or otherwise using the Specification is assumed by the Specification implementer and user. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE."

2. Revision History

Version	Date	Description
0.1	5/21/2019	Initial Release

Note: Because the product version upgrade or other reasons, the contents of this document will not be updated on a regular basis. Unless otherwise agreed, this document used only as a guide, in this document, all statements, information and advice does not constitute any express or

implied guarantees.

3. Scope

This specification describe a kind of 3U, 4 sockets server system. It is designed a flexible system architecture based on Intel Purley Platform. It can be expanded to GPU BOX, 32*M.2 SSD and maximum support 3*GPU cards. There are 2 kinds of different mechanical structure.

4. Overview

4.1 Overview

Whistler is based on Intel® Sky Lake-SP CPU architecture. The motherboard supports up to 48 DIMMs. Whistler was designed in the Q1 of 2018.

4.2 Product Overview

Whistler is a completely independent research and development of server products. Based on Intel® Sky lake-SP CPU architecture, using Lewisburg chipset. Support four mainstream Intel Xeon Sky Lake-SP 81xx/61xx/51xx series processors. Support 48 DIMMs DDR4 memory, the biggest support to 2666 MHZ. Support Lewisburg-1G PCH and AST2500 is managed chipset. There are 9 pcs PCIe Slots on board and maximum support 12 pcs slots. Supports 5 pcs M.2 SSD on board. Structure, storage, PCI extension, power supply, fan and other parts modular design. Centralized power supply design, to realize saving energy and reducing consumption.

4.3 Product standard

CPU	
CPU type	Supports four Intel® Sky Lake-SP 81xx/61xx/51xx series processors (TDP 205W)
Connecter	Four Socket-P0 slots
Chipset	

Chipset type	PCH LBG-1G
RAM	
RAM type	DDR4 RDIMM/LRDIMM/AEP/NVDIMM
RAM slot quantity	48
RAM total capacity	Total capacity 6144GB（single 128GB）
I/O Connecter	
USB	Two external USB 3.0 ports(Front), Internal USB 2.0 port
VGA	One external VGA (Front)
UID	One ID pilot lamp inlay
Manager chipset	
Manager chipset	Integrated one independent 1000 Mbps network interface, specifically for remote management of IPMI.
PCI Express slot	The motherboard supports 9 pcs PCI Express 3.0 slots
HDD	
HDD type	Support one 3.5-inch SAS/SATA HDDs and 32 M.2 SSD
Power supply	
PSU spec	The whole system adopts three specifications of PSU, the power is 1600W, and the maximum configuration is 4 power supplies. According to the system configuration, the appropriate PSU and PSU redundancy modes are selected to support 2+2 redundancy under certain configuration conditions.
Input power	The main specifications is 1600W PSU AC-- 180-264V, Typical 230V DC-- 164-300V, Typical 270V

Environmental Requirements	
Altitude (Motherboard)	1500m (operational) or 12192m(non - operational)
Altitude (Full system)	1500m (operational) or 12192m(non - operational)
Operating and storage relative humidity (Full system)	10% to 90% (non-condensing)
Operating temperature rang (Motherboard)	-5℃ to +45℃ ; Note: It is suggested to power on to work after standing for 1 hour in the data center, after long time transportation.
Operating temperature range(Full system)	-5℃ to +35℃; Note: It is suggested to power on to work after standing for 1 hour in the data center, after long time transportation.
Storage temperature range (Motherboard)	-40℃ to +70℃
Storage temperature range(Full system)	-40℃ to +70℃
Transportation temperature range(Motherboard)	-40℃ to +70℃ (short-term storage)
Transportation temperature range(Full system)	-40℃ to +70℃ (short-term storage)

5. Physical Specifications

5.1 Block Diagram

Figure 5-1 illustrates the functional block diagram of the Motherboard.

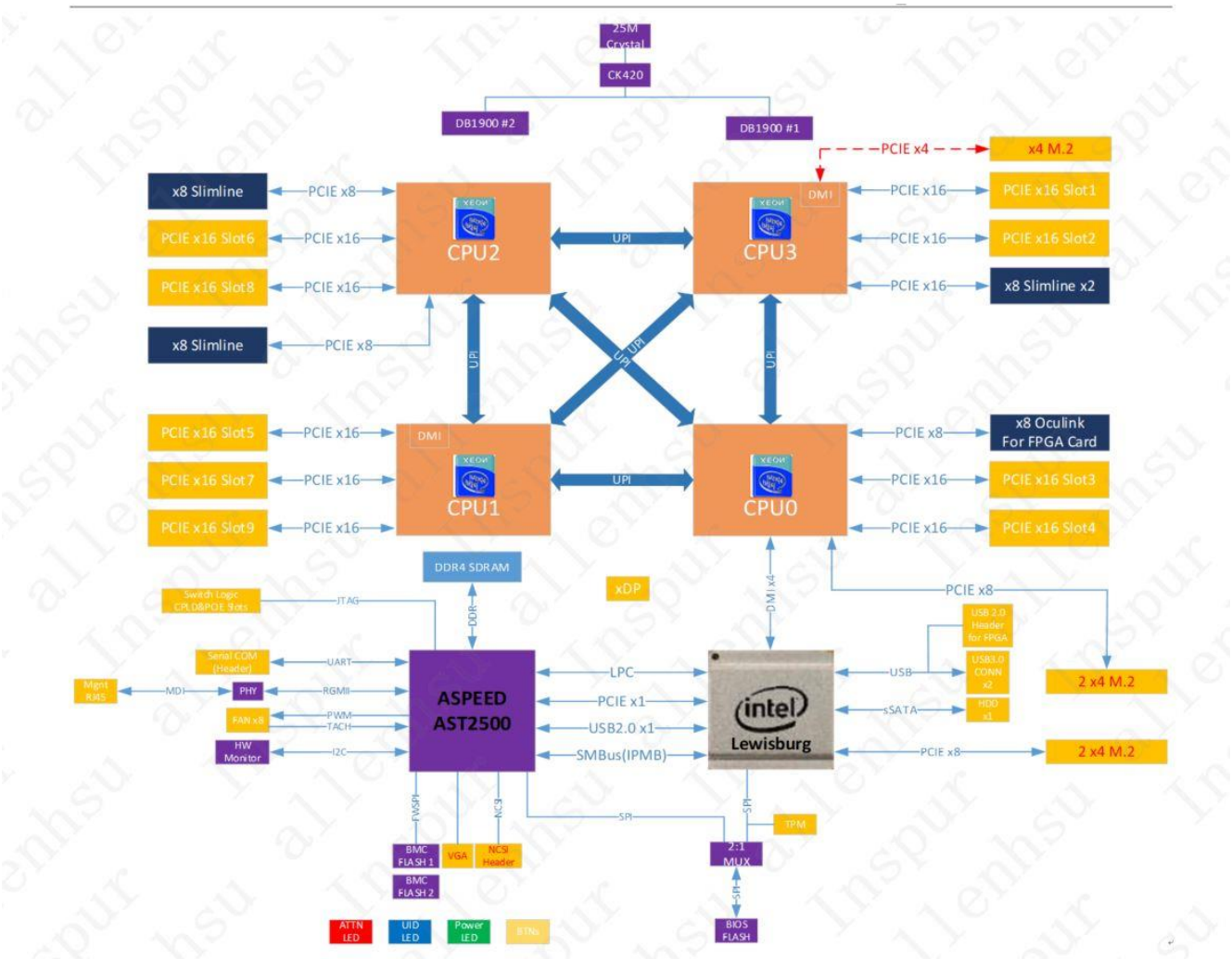


Figure 5-1 Block Diagram

5.2 Placement and Form Factor

Board form factor is 16.7 inch by 22.7 inch (16.7”x22.7”). Figure 5-2 is board placement. The placement is meant to show key components ’relative positions, exact dimension and position information would be exchanged by DXF format for layout and 3D model of mechanical.

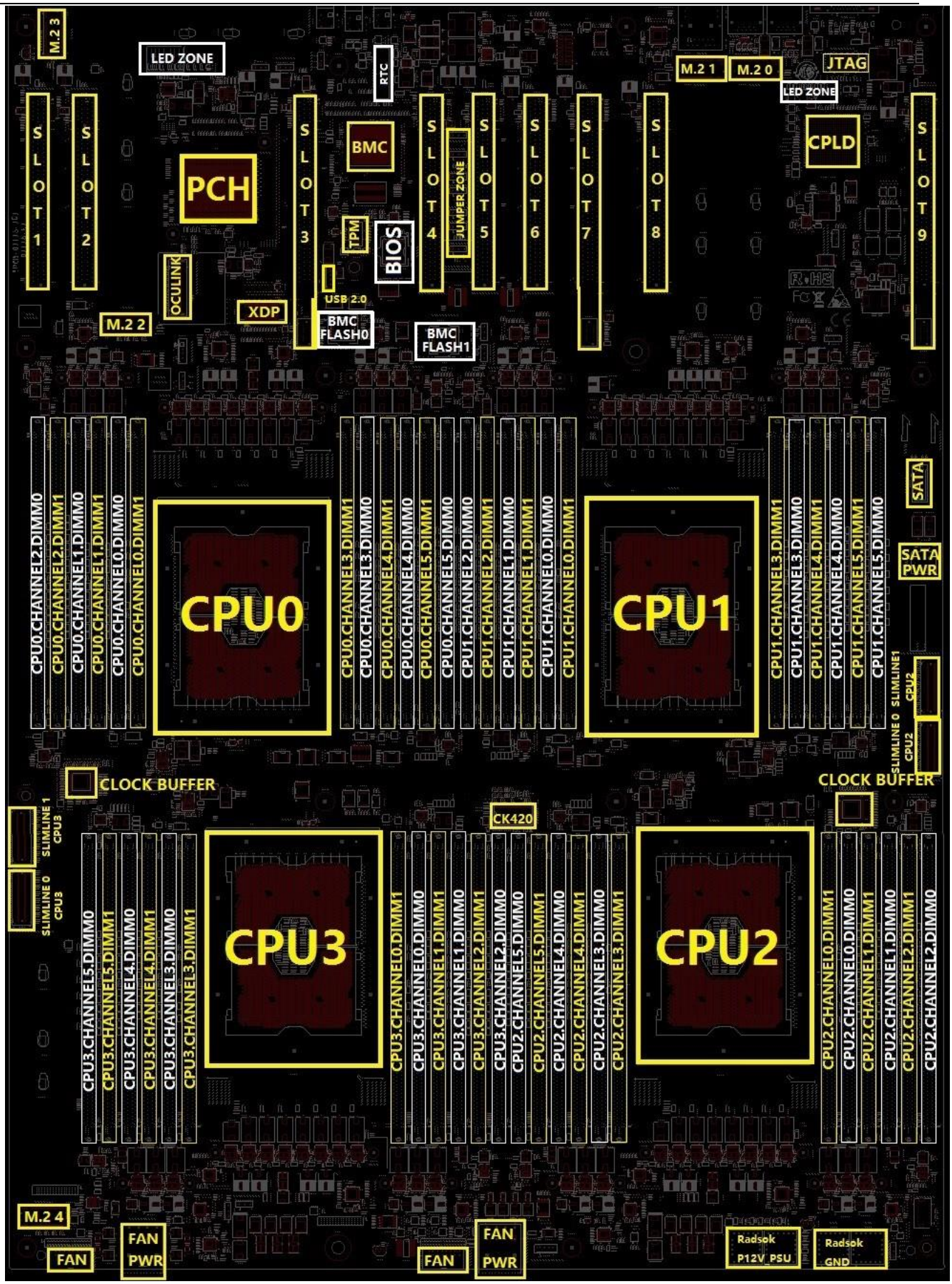

M.2 3
LED ZONE
RTC
M.2 1
M.2 0
JTAG
LED ZONE
SLOT 1
SLOT 2
PCH
BMC
SLOT 3
SLOT 4
JUMPER ZONE
SLOT 5
SLOT 6
SLOT 7
SLOT 8
CPLD
SLOT 9
TPM
BIOS
OCULINK
USB 2.0
XDP
M.2 2
BMC FLASH0
BMC FLASH1
CPU0.CHANNEL2.DIMM0
CPU0.CHANNEL2.DIMM1
CPU0.CHANNEL1.DIMM0
CPU0.CHANNEL1.DIMM1
CPU0.CHANNEL0.DIMM0
CPU0.CHANNEL0.DIMM1
CPU0
CPU0.CHANNEL3.DIMM1
CPU0.CHANNEL3.DIMM0
CPU0.CHANNEL4.DIMM1
CPU0.CHANNEL4.DIMM0
CPU0.CHANNEL5.DIMM1
CPU0.CHANNEL5.DIMM0
CPU1.CHANNEL2.DIMM1
CPU1.CHANNEL2.DIMM0
CPU1.CHANNEL1.DIMM1
CPU1.CHANNEL1.DIMM0
CPU1.CHANNEL0.DIMM1
CPU1.CHANNEL0.DIMM0
CPU1
CPU1.CHANNEL3.DIMM1
CPU1.CHANNEL3.DIMM0
CPU1.CHANNEL4.DIMM1
CPU1.CHANNEL4.DIMM0
CPU1.CHANNEL5.DIMM1
CPU1.CHANNEL5.DIMM0
SATA
SATA PWR
SLIMLINE 1 CPU2
SLIMLINE 0 CPU2
CLOCK BUFFER
CLOCK BUFFER
CK420
SLIMLINE 1 CPU3
SLIMLINE 0 CPU3
CPU3.CHANNEL5.DIMM0
CPU3.CHANNEL5.DIMM1
CPU3.CHANNEL4.DIMM0
CPU3.CHANNEL4.DIMM1
CPU3.CHANNEL3.DIMM0
CPU3.CHANNEL3.DIMM1
CPU3
CPU3.CHANNEL0.DIMM1
CPU3.CHANNEL0.DIMM0
CPU3.CHANNEL1.DIMM1
CPU3.CHANNEL1.DIMM0
CPU3.CHANNEL2.DIMM1
CPU3.CHANNEL2.DIMM0
CPU2.CHANNEL5.DIMM1
CPU2.CHANNEL5.DIMM0
CPU2.CHANNEL4.DIMM1
CPU2.CHANNEL4.DIMM0
CPU2.CHANNEL3.DIMM1
CPU2.CHANNEL3.DIMM0
CPU2
CPU2.CHANNEL0.DIMM1
CPU2.CHANNEL0.DIMM0
CPU2.CHANNEL1.DIMM1
CPU2.CHANNEL1.DIMM0
CPU2.CHANNEL2.DIMM1
CPU2.CHANNEL2.DIMM0
M.2 4
FAN
FAN PWR
FAN
FAN PWR
Radsok P12V_PSU
Radsok GND

Figure 5-2 Placement

5.3 CPU and Memory

5.3.1 CPU

The motherboard supports all Intel® Sky Lake -SP processors with TDP up to 205W.

- Support four Sky Lake-SP processors up to 205W TDP.
- Three full-width Intel UPI links up to 10.4 GT/s/direction for Sky Lake-SP processor.
- Up to 28 cores per CPU (up to 56 threads with Hyper-Threading Technology).
- Single Processor mode and Two-CPU mode are both supported

5.3.2 DIMM

The motherboard has DIMM subsystem designed as below:

- DDR4 direct attach memory support on CPU0, CPU1, CPU2 and CPU3.
- 6x channels DDR4 registered memory interface on each CPU
- 2x DDR4 slots on each Chanel (total 48x DIMMs)
- Support DDR4 speeds up to 2666MT/s 1DCP and 2DCP
- Support DDR4 RDIMM/LRDIMM/AEP/NVDIMM
- Support SR, DR, QR and 8R DIMMs
- Up to maximum 6144 GB with 128 GB DRAM DIMM
- Follow updated JEDEC DDR4 specification with 288 pin DIMM socket
- Memory support matrix for DDR4 is as Table 5-1

2 Slots Per Channel	
1 DIMM Per Channel	2 DIMM per Channel
2666 MT/s	2666 MT/s

Table 5-1

5.4 PCH

The motherboard uses Intel® Lewisburg chipset, which supports following features:

- Two external USB 3.0 port(Front), One internal USB 2.0 port;
- 4x slimline x8 connector use x16 PCIE riser card;

- 1x Oculink connector use FPGA card;
- LPC interface, mux with BMC to enable BMC the capability to perform BIOS upgrade and Recovery
- SPI interface for TPM header
- SMBUS interface (master & slave)
- Intel® Server Platform Services (SPS) 4.0 Firmware with Intel® Node Manager
- PECI access to CPU
- SMLink0 connect to BMC
- Intel® Manageability Engine (ME) obtain HSC PMBus related information directly.
- Intel® ME SMLink1 connects to Hot swap controller PMBus interface by default.
- BMC connected to HSC PMBus, so it masters HSC PMBus related feature flexibly.
- Temperature sensors reading from BMC
- PCH SKUs
- Board design shall support all PCH SKUs in terms of power delivery and thermal design.

5.5 PCIe Usage

PCIe lanes are configured according to Figure 5-3 and Table 5-2:

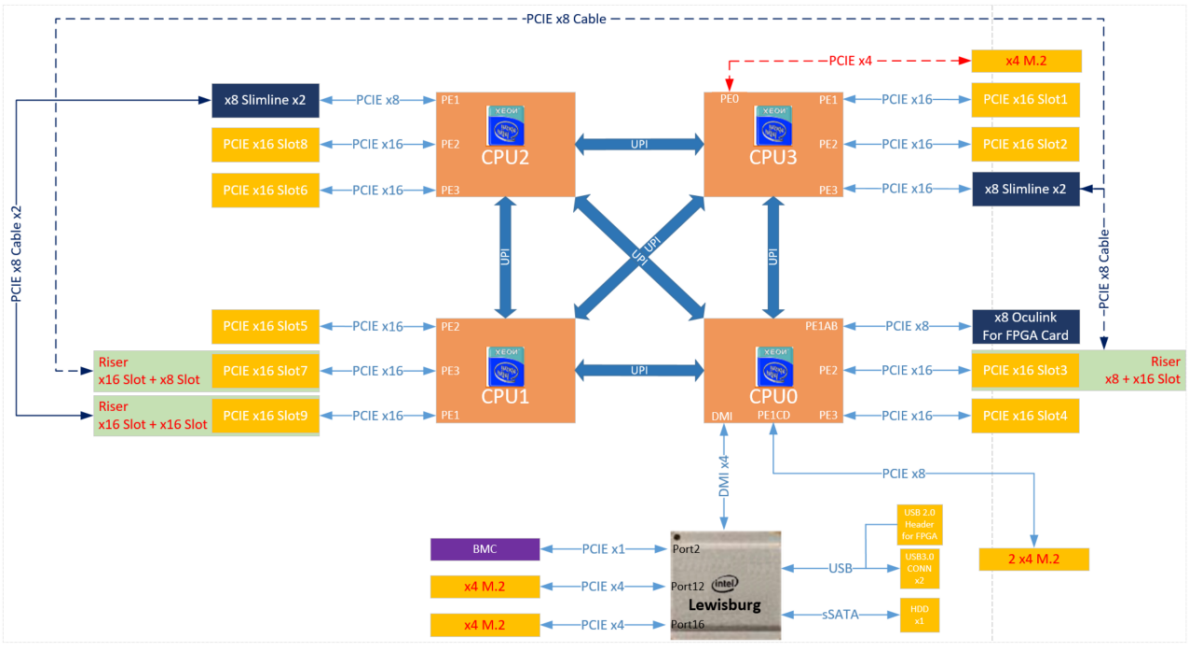


Figure 5-3 PCIe Usage

PCIE Resource Configuration			
CPU0	PE1(Lane0-7)	X8	Oculink for FPGA card
	PE1(Lane8-15)	2 X4	M.2
	PE2(Lane0-15)	X16	PCIe Slot 3
	PE3(Lane0-15)	X16	PCIe Slot 4
CPU1	PE1(Lane0-15)	x16	PCIe Slot 9
	PE2(Lane0-15)	X16	PCIe Slot 5
	PE3(Lane0-15)	X16	PCIe Slot 7
CPU2	PE1(Lane0-15)	2 x8	2 x8 Slimline
	PE2(Lane0-15)	x16	PCIe Slot 8
	PE3(Lane0-15)	X16	PCIe Slot 6
CPU3	PE0(Lane0-7)	2 X4	M.2
	PE1(Lane0-15)	x16	PCIe Slot 1
	PE2(Lane0-15)	X16	PCIe Slot 2
	PE3(Lane0-15)	2 x8	2 x8 Slimline

Table 5-2

5.6 MB PCB Stack Up

Layer Name	Plane Description	Layer Thickness (mil)	COPPER TYPE	Copper Weight (oz)	DK
	solder mask	0.4			
Signal1	SIGNAL	1.6	HTE	1	
PP	1080 RC65%*1	2.7			3.68
Plane 2	GND	1.2	RTF	1	
Core	3313 RC56%*1	4			3.86
Signal 3	SIGNAL	1.2	RTF	1	
PP	2116 RC60*1	4.4			3.78
Plane 4	GND	1.2	RTF	1	
Core	3313 RC56%*1	4			3.86
Signal 5	SIGNAL	1.2	RTF	1	
PP	2116 RC60*1	4.4			3.78
Plane 6	GND	1.2	RTF	1	
Core	1086 RC58%*1	3			3.78
Signal 7	SIGNAL	1.2	RTF	1	
PP	2113 RC60%*3	11			3.78
Plane 8	POWER	2.4	RTF	2	
Core	3313 RC56%*1	4			3.86
Plane 9	POWER	2.4	RTF	2	
PP	2113 RC60%*3	11			3.78
Signal 10	SIGNAL	1.2	RTF	1	
Core	1086 RC58%*1	3			3.78
Plane11	GND	1.2	RTF	1	
PP	2116 RC60*1	4.4			3.78
Signal 12	SIGNAL	1.2	RTF	1	
Core	3313 RC56%*1	4			3.86
Plane13	GND	1.2	RTF	1	
PP	2116 RC60*1	4.4			3.78
Signal 14	SIGNAL	1.2	RTF	1	
Core	3313 RC56%*1	4			3.86
Plane 15	GND	1.2	RTF	1	
PP	1080 RC65%*1	2.7			3.68
Signal 16	SIGNAL	1.6	HTE	1	
	solder mask	0.4			
Material	**IT170GRA with RTF** **Total**	**94.2**			

Figure 5-4 stack up

6. I/O System

This section describes the motherboard I/O system.

6.1 PCIe x 16 Slot

The motherboard has 9 pcs PCIe x16 slots used by four kinds of PCIe riser cards.

Figure 6-1 illustrates the source of PCIe x16 slots.

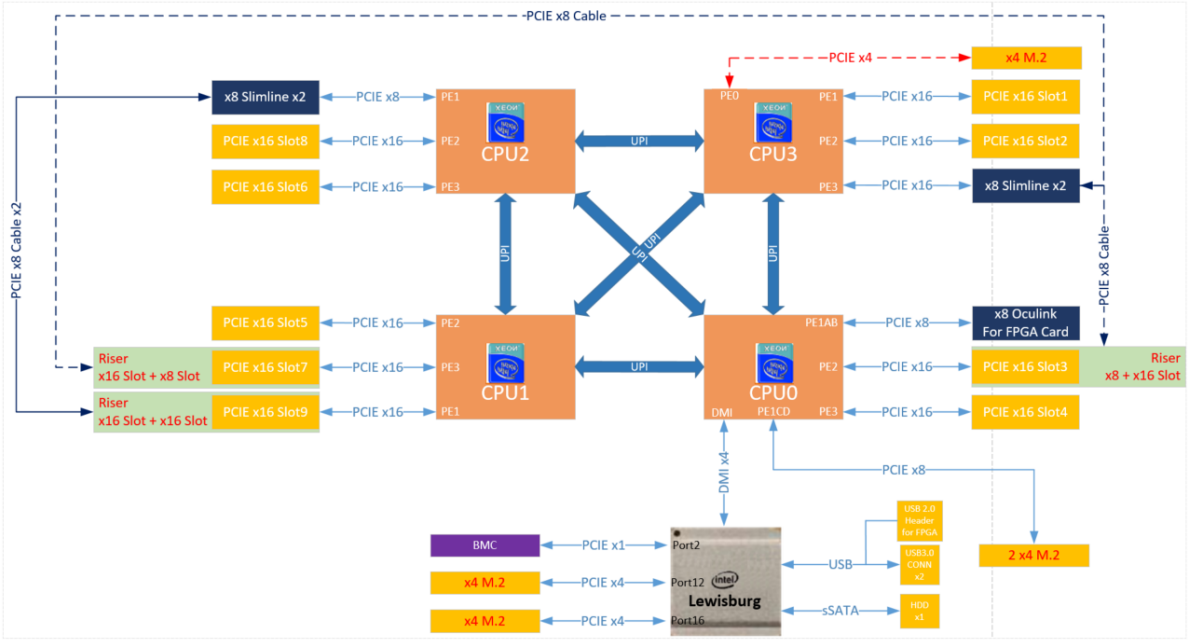
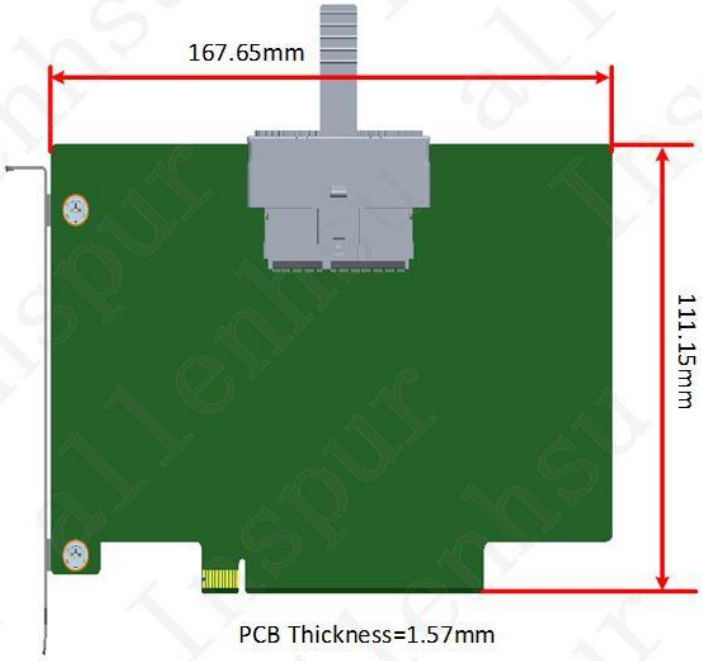


Figure 6-1 PCIe x16 slot

6.2 Riser Card Type

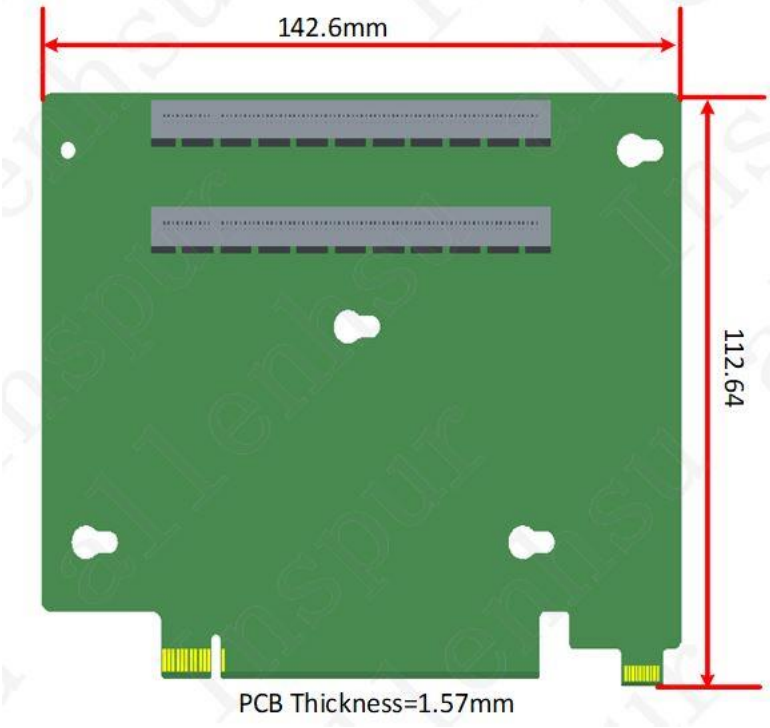
There are four kinds of PCIe riser cards as follow.

6.2.1 GPU BOX Sliver riser card



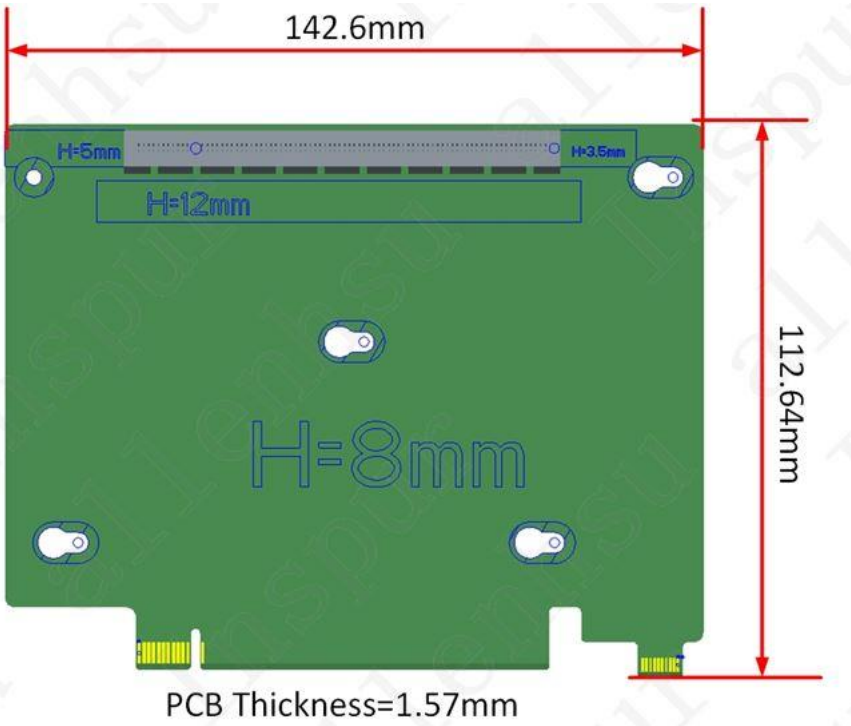
This riser card connect to HGX-1GPU BOX.

6.2.2 2x16 Slot riser card



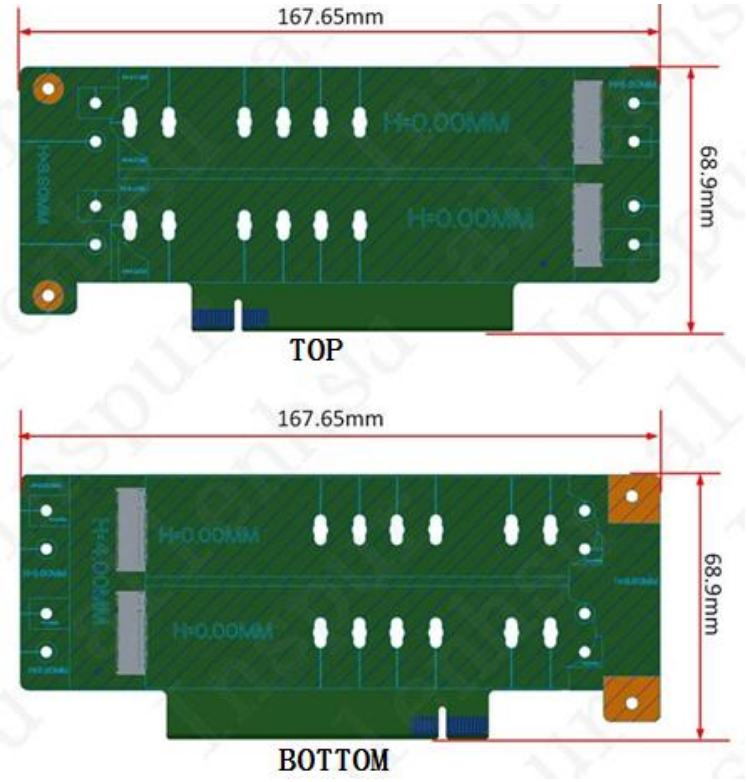
This riser card can support two standards PCIe x16. One connector is from PCIe slot, the other one is from 2*x8 Slimline connectors.

6.2.3 GPU 1x16 slot riser card



This riser card support GPU board.

6.2.4 4 M.2 carrier



This riser card support four M.2 cards.

6.3 DIMM Slot

Total 48 DIMMs, DIMM 1 is Black, DIMM0 is White.

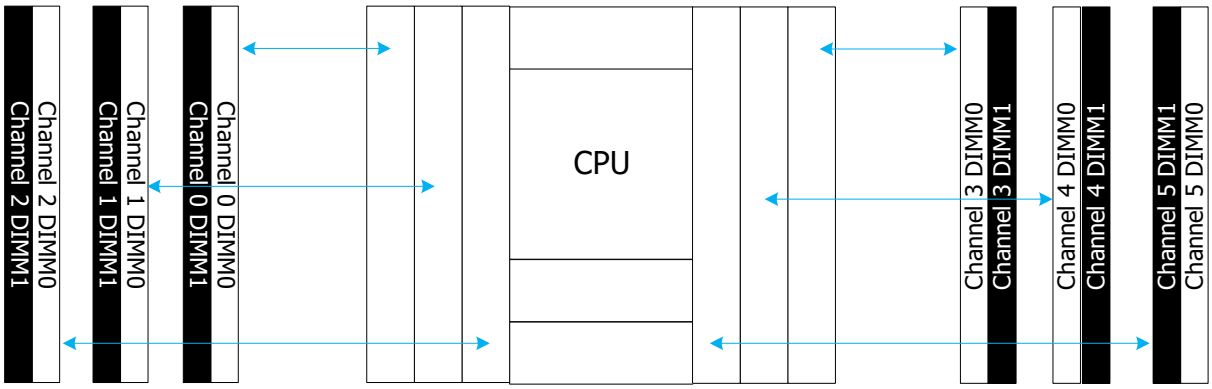


Figure 6-2 DIMM Topology

6.4 Network

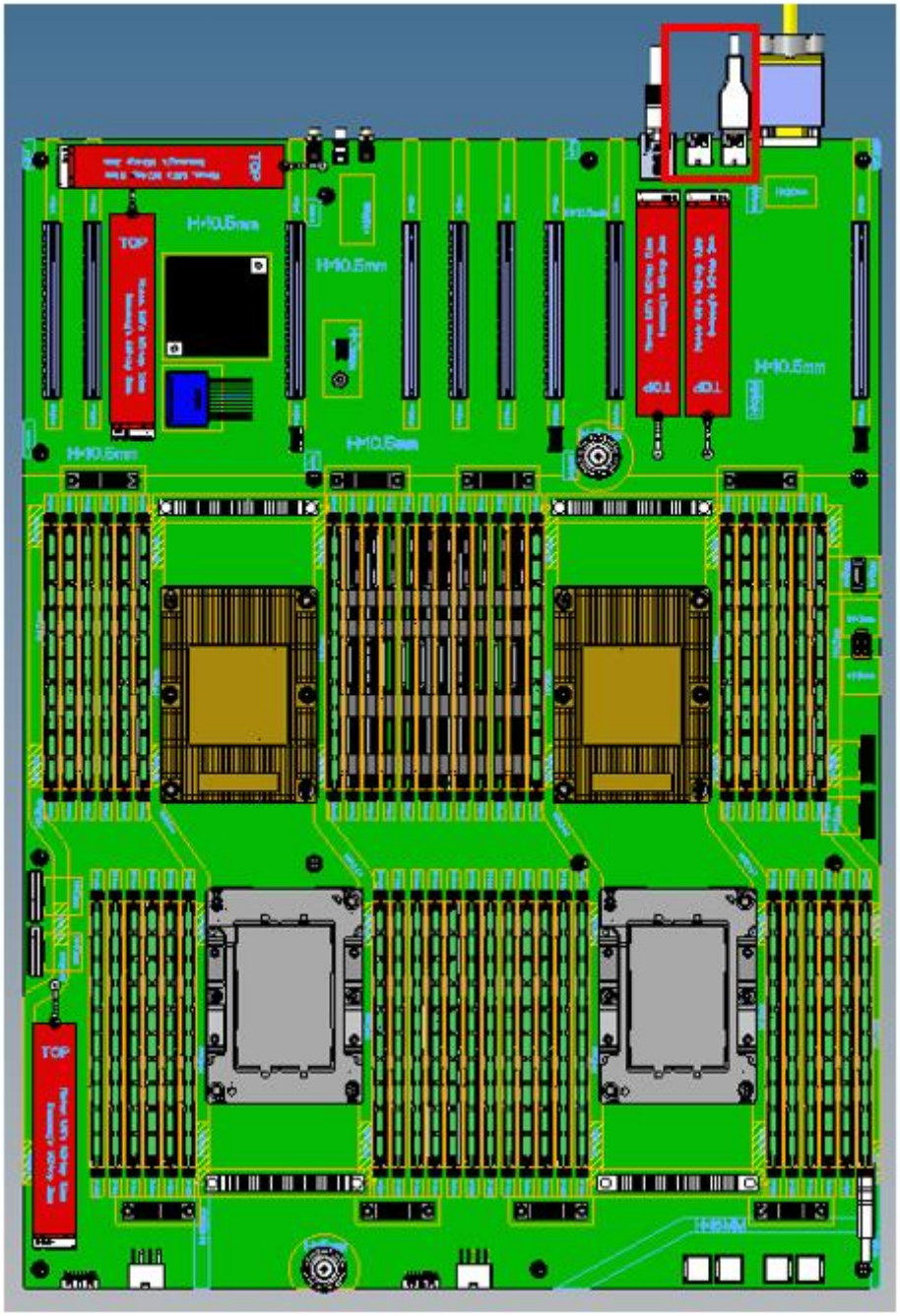
6.4.1 Management network

The motherboard has one management network interface for BMC's connection. Dedicated RJ45 port for Board management, driven by BMC through RMII/NC-SI.

6.5 USB

The Motherboard has two external USB2.0/3.0 connectors located in Front edge of Motherboard and one internal USB 2.0 header. BIOS should support follow devices on USB ports available on Motherboard:

- USB Keyboard and mouse
- USB flash drive (bootable)
- USB hard drive (bootable)
- USB optical drive (bootable)



6.6 sSATA

The motherboard can support 1x 3.5” hard disks.

6.6.1 1x sSATA

The motherboard has Intel® Lewisburg PCH on board, which has a sSATA controller.

It support 1x sSATA 3.0 port.

Figure 6-3 SATA Topology

6.7 M.2

The motherboard supports 5x PCIe M.2 devices on board and 8 pcs PCIe 4x M.2 carrier as chapter 6.2.4

6.8 Fan

The motherboard holds 2 pcs system FAN connectors. Each FAN has 8 pins, which includes two DC power pins, two GND pins, two TACH pins, one PRESENT pin and one PWM pin. They are used to support dual rotor FAN that share PWM control signal and PRESENT signal but it has separate TACH signal. FAN connector pin's definition is listed in Table 6-1, and FAN connector diagram is shown in Figure 6-5. Rated voltage of FAN is 12 VDC, and rated current is 5000 mA/Max, 5750 mA.

Pin	Definition
1	INFAN 12 VDC
2	OUTFAN 12 VDC
3	INFAN TACH
4	Present
5	OUTFAN GND
6	OUTFAN 12 VDC
7	OUTFAN TACH
8	INFAN & OUTFAN PWM

Table 6-1

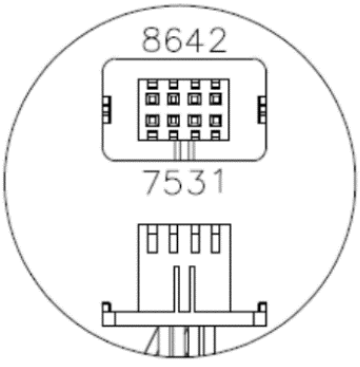


Figure 6-5 FAN connector

6.9 LED

► Power status LED, Green/Orange

--When power on, turn on green LED

--When Power off, turn on orange LED

► UID status LED, Blue

--When device is selected, turn on LED

--When device is not selected, turn off LED

► Attention status LED: RED

--When system is abnormal, turn on LED

--When system is normal or power off, turn off LED

6.10 TPM

The Motherboard supports one TPM with SPI interface.

6.11 Header

Signal	Description	Location	Default
FM_MFG_MODE	1-2:Enable Manufacture Mode 2-3:Disable Manufacture Mode	J70	Default 2-3
HDA_SDO	1-2:Disable Flash Override 2-3:Enable Flash Override	J72	Default 1-2
FM_ME_RECOVER_N	1-2:Normal 2-3:ME Force Update	J88	Default 1-2
RST_RTCRST_N	1-2:Normal Operation 2-3:Clear CMOS	J89	Default 1-2
FM_PASSWORD_CLEAR_N	1-2:Normal Operation 2-3:Clear Password	J103	Default 1-2
	1-2: Normal Operation Also Top Swap Disable 2-3: Recover BIOS Also Top Swap Enable	J120	Default 1-2
	1-2: Normal 2-3: BMC disable	J90	Default 1-2

7. Power system

7.1 System Power budget

Rail	Voltage(V)		CPU(205W)	DIMM	AEP	Lewisbug-T	SATA HDD	SYS Fan	M.2	USB	BMC	PCIE (75W)	CRT	BCM54612	CPLD	Total (A)
IC QTY	IC Qty		4.00	8.00	24.00	1.00	1.00	8.00	6.00	3.00	1.00	10.00	1.00	1.00	1.00	
PVCCIN CPUn	SVID	1.80	228.00													912.00
PVCCSA CPUn	SVID	0.85	16.00													64.00
PVCCIO CPUn	SVID	1.00	21.00													84.00
PVDDQ XXX	SVID	1.20	17.50	71.60	2.68											712.80
PVTT XXX	0.60	0.60		1.71	0.01											13.65
PVPP XXX	2.50	2.50	1.20	8.90	0.20											76.00
P3V3 STBY	3.30	3.30	0.08			1.30					0.40	0.38		0.50	1.00	7.36
P2V5 STBY	2.50	2.50									0.10					0.10
P1V8 STBY	1.80	1.80				1.00					0.10					1.10
P1V2 STBY	1.20	1.20									0.60					0.60
P1V15 STBY	1.15	1.15									0.80					0.80
PVNN STBY PCH	SVID	1.00				23.00										23.00
P1V05 STBY PCH	1.05	1.05				15.00										15.00
P12V	12.00	12.00			1.60		2.00	10.00				5.50				175.40
P12V STBY	12.00	12.00														-
P5V	5.00	5.00					1.50			0.90			0.50			4.70
P3V3 A	3.30	3.30							5.00			3.00				16.00
P3V3 B	3.30	3.30							5.00			3.00		0.00		44.00
Power (max)			205.00	13.40	18.00	29.00	17.00	69.00	14.00	4.50	2.00	75.00	2.50	1.65	2.00	
			820.00	643.20	432.00	29.00	17.00	552.00	84.00	13.50	2.00	750.00	2.50	1.65	2.00	2922.44

Table 7-1 System Power Budget

7.2 Power Simple Topology

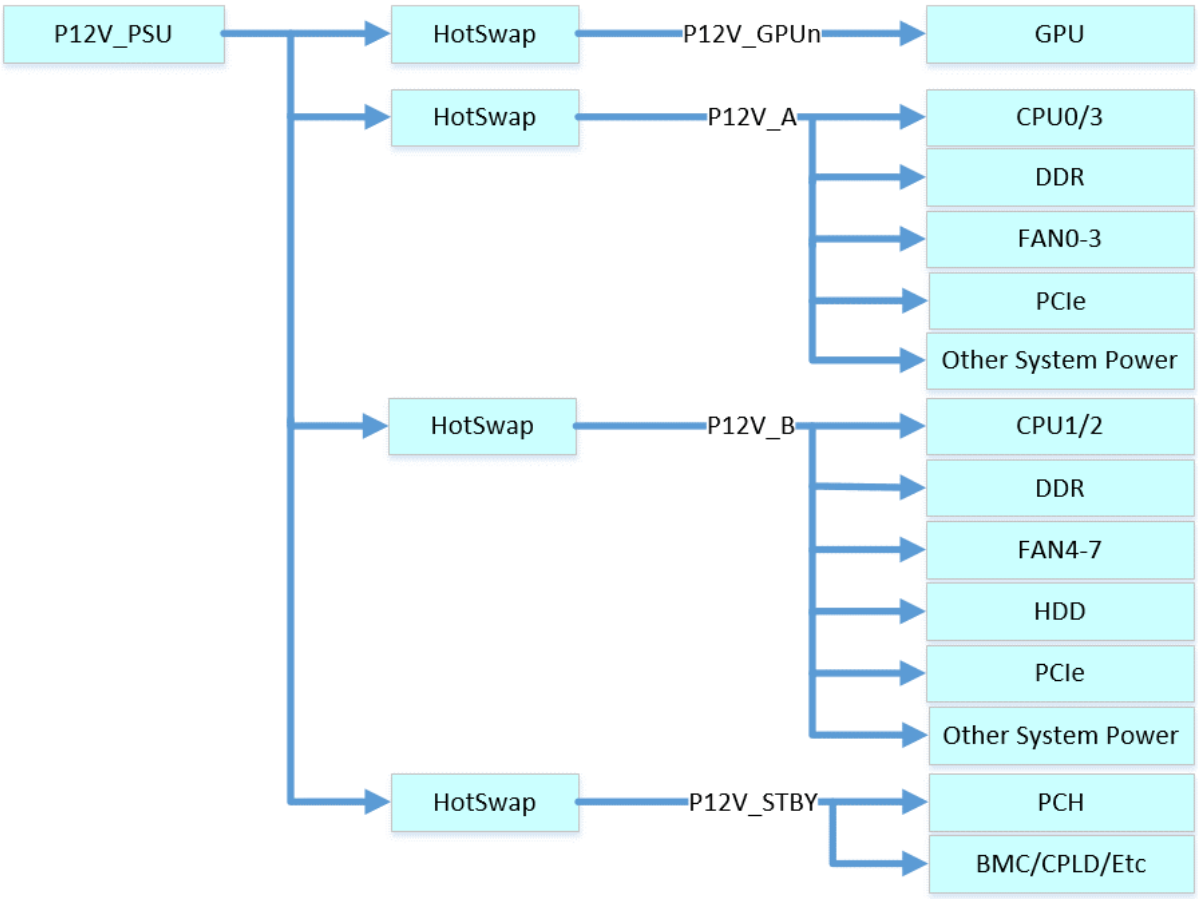


Figure 7-1 power topology

7.3 Input voltage Level

The nominal input voltage delivered by the power supply is 12.2V DC nominal at light loading with a range of 11.8V to 12.6V.

	Typical	Min	Max
AC Input	230V	180V	264V
DC Input	270V	164V	300V
Output Main	12.2V	11.8V	12.6V
Output STBY	12.0V	11.4V	12.6V

Table 7-2 PSU Output Characteristics

7.4 DC-DC Power Design

7.4.1 CPU VR

CPU VR follow latest VR13 SPEC. Using the minimum number of total phases to support the maximum CPU power. CPU VR have auto phase dropping feature, and run at optimized phase count among 1, 2, 3,…, and maximum phase count. CPU VR support all Power States to allow the VRM to operate at its peak efficiency at light loading.

7.4.2 DIMM VR

DIMM VR support auto phase dropping for high efficiency across loading. DIMM VR compliant to latest VR13 specification.

7.4.3 Detail design

Power Rail	VOUT	VIN	VR Type	VR QTY /BRD	VR Controller IC and FET	SMBus Address
PVCCIN_CPU0 PVCCIN_CPU3	SVID	P12V_A	Switcher	2	MPS MP2965+7Phase MP86956；	CPU0:0X40 CPU1:0X40 CPU2:0X40 CPU3:0X40 With I2C SW
PVCCIN_CPU1 PVCCIN_CPU2	SVID	P12V_B	Switcher	2		
PVCCSA_CPU0 PVCCSA_CPU3	SVID	P12V_A	Switcher	2	Infineon PXE1110C+1Phase TDA21470	CPU0:0XC8 CPU1:0XC8 CPU2:0XC8 CPU3:0XC8 With I2C SW
PVCCSA_CPU1 PVCCSA_CPU2	SVID	P12V_B	Switcher	2	Infineon PXE1110C+1Phase TDA21470	
PVCCIO_CPU0 PVCCIO_CPU3	SVID	P12V_A	Switcher	2	Infineon IR38163	CPU1:0X80 CPU2:0X80 CPU3:0X80

PVCCIO_CPU1 PVCCIO_CPU2	SVID	P12V_B	Switcher	2	Infineon IR38163	CPU4:0X80 With I2C SW
PVDDQ_ABC PVDDQ_DEF PVDDQ_UVW PVDDQ_XYZ	1.2V	P12V_A	Switcher	4	Infineon PXM1310C+3Phase TDA21470	PVDDQ_ABC:0XC0 PVDDQ_DEF:0XE4 PVDDQ_GHJ:0XC0 PVDDQ_KLM:0XE4 PVDDQ_NPQ:0XC0 PVDDQ_RST:0XE4 PVDDQ_UVW:0XC0 PVDDQ_XYZ:0XE4
PVDDQ_GHJ PVDDQ_KLM PVDDQ_NPQ PVDDQ_RST	1.2V	P12V_B	Switcher	4	Infineon PXM1310C+3Phase TDA21470	
PVTT_ABC PVTT_DEF PVTT_UVW PVTT_XYZ	0.6V	P12V_A	Switcher	4	IR3897MTRPBF	
PVTT_GHJ PVTT_KLM PVTT_NPQ PVTT_RST	0.6V	P12V_B	Switcher	4	IR3897MTRPBF	
PVPP_ABC PVPP_DEF PVPP_UVW PVPP_XYZ	2.5V	P12V_A	Switcher	4	TPS53515RVER	
PVPP_GHJ PVPP_KLM PVPP_NPQ PVPP_RST	2.5V	P12V_B	Switcher	4	TPS53515RVER	
PVNN_STBY_PCH	0.85V 0.9V 0.95V 1.0V	P12V_STBY	Switcher	1	IR38263MTRPBF	PVNN:0X86
P1V05_STBY_PCH	1.05V	P12V_STBY	Switcher	1	TPS53353DQPR	
P1V8_STBY	1.8V	P12V_STBY	Switcher	1	MPQ8632GLE-6-Z	
P3V3_STBY	3.3V	P12V_STBY	Switcher	1	TPS53515RVER	
P2V5_STBY	2.5V	P3V3_STBY	LDO	1	TPS7A7200RGTT	
P1V2_STBY	1.2V	P2V5_STBY	LDO	1	TPS7A7200RGTT	
P1V15_STBY	1.15V	P12V_STBY	Switcher	1	MPQ8636GLE-4-Z	
P5V	5.0V	P12V_B	Switcher	1	TPS53515RVER	
P3V3	3.3V	P12V_A	Switcher	1	MP2951+2Phase MP86945	

P3V3_B	3.3V	P12V_B	Switcher	1	TPS53355DQPR	
P12V_STBY	12V	P12V_PSU	Hot Swap	1	MP5023GV-000-Z	P12V_STBY:0X82
P12V_A	12V	P12V_PSU	Hot Swap	1	ADM1278	P12V_A:0X8C
P12V_B	12V	P12V_PSU	Hot Swap	1	ADM1278	P12V_B:0X8A

8. BIOS

8.1 BIOS Description

8.1.1 BIOS Chip

The BIOS chip uses PCH's SPI interface through BMC controlled MUX.

Item	Description
Code Base Vendor	AMI AptioV
BIOS Image Size	16MB
ROM Image Size	32MB

8.1.2 BIOS Source Code

BIOS Code based on AMI Purley LightningRidge CRB code, using Intel EDKII software architecture.

8.2 BIOS Features

8.2.1 BIOS Supported Specifications

- Multiprocessor Specification, Version 1.4.
- PCI BIOS Specification, Version 2.1.
- PCI-to-PCI Bridge Architecture Specification, Version 1.2.
- PCI Express Base Specification Version 4.0
- PCI Local Bus Specification Version 3.0
- PCI Firmware Specification Version 3.2
- Advanced Configuration and Power Interface Specification 5.0 or later
- System Management BIOS (SMBIOS) Specification 3.2.0 or later
- Plug and Play BIOS Specification, Revision 1.0A

- PC System Design Guide 2001 - Any conflict occurs between Windows Logo Program System and Device Requirements and, follows Windows Logo Program System and Device Requirements.
- Serial ATA Specification 3.0 or later
- AHCI Specification 1.3
- EDD (BIOS Enhanced Disk Drive) Specification V3.0 Revision 0.8
- Bootable CD-ROM Format Specification, Version 1.0
- TCG EFI Platform Specification
- Functionality and Interface Specification of Cryptographic Support Platform for Trusted Computing (Chinese TCM)
- UEFI Specification 2.3.1 or later
- UEFI PI Specification 1.7 or later
- UEFI SCT 2.3
- NIST 800-147 BIOS Protection Guidelines
- NIST 800-147B BIOS Protection Guidelines for Server
- Intelligent Platform Management Interface Specification V2.0

8.2.2 BIOS Error Handle

The BIOS should support reporting the following POST or error SEL log to BMC and standard RAS feature. From the SEL log, the user may know the specific location of device that the error happens with. And the system could be more reliable with the RAS feature.

- BIOS support IPMI SEL Log
- BIOS support machine check error
- BIOS support DDR4 command/Address parity check
- BIOS support memory mirroring
- BIOS support memory demand/patrol scrubbing
- BIOS support memory rank/multi rank sparing
- BIOS support Intel QPI Clock Fail over
- BIOS support PCI Express Advanced Error Reporting
- BIOS support PCI Express Enhanced Root Port Error Reporting
- BIOS support EMCA gen 2

8.2.3 BIOS Setup Screen

BIOS setup options are included but not limited to the following options:

- BIOS setup support modifying active core numbers

  The BIOS setup shall display the total core numbers and the active core numbers of every CPU. And the user shall be allowed to disable any number of cores supported.

- BIOS setup support enable/disable HT

  Hyper Thread option shall be enabled by default. Only one thread is active if HT is disabled.

- BIOS setup support enable/disable VT-X/VT-D/SR-IOV

  These items shall be enabled if virtualization function is need and could be disabled if not.

- BIOS setup support displaying the L1/L2/L3 cache of CPU

The L1/L2/L3 cache size of CPU should be displayed on the main page of BIOS Setup.

- BIOS setup support enable/disable Turbo Boost

  Turbo Mode opportunistically, and automatically, allows processor cores to run faster than the marked frequency if the physical processor is operating below power, temperature and current specification limits. Turbo Mode can be enabled or disabled by the BIOS and it will increase the performance of workloads.

- BIOS setup support enable/disable P-state (EIST)

  Enhanced Intel Speed Step Technology support shall be controlled by the BIOS. EIST, which offers the capability to support a multitude of processor performance states, allows the processor to dynamically adjust frequency and voltage based on power versus performance needs. EIST should be enabled by default.

- BIOS setup support enable/disable C-state

  Multiple low power idle states (C0/C1/C1E/C6) should be typically implemented by the BIOS. Enable C state could minimize the idle power consumption of the processor. C state may be set disabled by default for the system performance.

- BIOS setup support enable/disable PCIE ASPM

  ASPM operation may be controlled by the BIOS. Optimal power consumption could be obtained if ASPM is enabled, however, some instances of performance impact can be observed.

- BIOS setup support enable/disable PXE boot

  The BIOS should support UEFI and Legacy PXE boot by default and they may be disabled under BIOS setup. PXE will be booted directly if F12 is pressed during the POST process.

- BIOS setup support performance/efficient/custom

  The BIOS is set to performance mode by default. The user may change to efficient mode for power saving or to custom mode under BIOS setup if they want.

8.2.4 SMBIOS

The BIOS shall provide support for the System Management BIOS (SMBIOS) Reference Specification, Version 3.2.0 or later. The BIOS shall implement the following SMBIOS tables:

Type	Structure
0	BIOS Information
1	System Information
2	Base Board Information
3	System Enclosure or Chassis
4	Processor Information
7	Cache Information
8	Port Connector Information
9	System Slots
11	OEM Strings
13	BIOS Language Information
16	Physical Memory Array
17	Memory Device
19	Memory Array Mapped Address
38	IPMI Device Information
39	System Power Supply
41	Onboard Devices Extended Information
127	End-of-Table

8.2.5 Boot

- BIOS Support SAS, SATA and PXE boot.

  The BIOS shall support booting to SAS device, SATA disk or PXE boot option.

- BIOS Support Changing boot priority

Boot priority shall be changed under BIOS setup and boot option shall be allowed to be disabled or enabled.

- BIOS support modifying BOOT sequence via IPMI commands:

  The sequence of boot option shall be adjusted with IPMI raw or chassis command. This change should be one-time or persistent.

- BIOS support Boot Retry :

  Enable: If there is no bootable device found, BIOS should keep loop searching for bootable device.

  Disable: If there is no bootable device found, BIOS will stop boot and show" Reboot and Select proper Boot device or Insert Boot Media in selected Boot device and press a key".

  BIOS shall support UEFI and legacy boot mode options, and UEFI and legacy boot mode shall have independent boot loop.

8.2.6 BIOS Update

- BIOS support USB Storage Device Recovery

  The BIOS may supporting recovery via a USB storage with a BIOS image in it when the BIOS of the system is corrupted with incomplete functionality.

- BIOS support Update BIOS Image through BMC

  The BIOS shall support being flashed via BMC Web GUI. There may be two upgrade modes, "BIOS+ME" and "BIOS only". And there should be a checkbox of "Keep BIOS Setup Option" for users, so they can choose whether the NVRAM should be cleared.

- BIOS support Update BIOS in UEFI Shell, Windows OS & Linux OS

  The BIOS shall support for flashing BIOS under UEFI Shell, Windows and Linux with AMI AFU tools. And with different parameters, BIOS region, ME region or other region could be flashed separately.

9. BMC

BMC is an independent system of host server system. This independent system has its own

processor and memory; The host system can be managed by BMC system even if host hardware or OS hang or went down.

9.1 Main Feature

- Support IPMI 2.0, IPMI Interface include KCS, LAN, IPMB
- Management Protocol,IPMI2.0, HTTPS, SNMP, Smash CLI
- Web GUI
- Redfish
- Management Network Interface, Dedicated/NCSI
- Console Redirection(KVM) and Virtual Media
- Serial Over Lan(SOL)
- Diagnostic Logs, System Event Log (SEL), Blackbox Log, Audit Log
- Hardware watchdog timer, Fans will full speed when BMC no response in 4 mins
- Intel® Intelligent Power Node Manager 4.0 support
- Event Alert, SNMP Trap(v1/v2c/v3), Email Alert and Syslog
- Dual BMC firmware image support
- Storage, Monitor RAID Controller/HDD/Virtual HDD
- Firmware update, BMC/BIOS/CPLD
- Device State Monitor and Diagnostic

9.2 Integrated BMC Hardware

ASPEED AST2500 Baseboard Management Controller, at the center of the server management subsystem is the ASPEED AST2500 integrated Baseboard Management Controller. This device provides support for many platform functions including system video capabilities, legacy Super I/O functions, hardware monitoring functions, and incorporates an ARM1176JZF-S 32-bit RISC CPU microcontroller to host an IPMI 2.0 compliant server management firmware stack.

The following functionality is integrated into the component:

- Baseboard Management Controller (BMC) with peripherals
- Server class Super I/O (SIO)
- Graphics controller
- Remote KVM redirection, USB media redirection, and HW Encryption

The eSPI/LPC interface to the host is used for SIO and BMC communication. The eSPI/LPC Bus interface provides IPMI Compliant KCS and BT interfaces.

The PCI Express interface is mainly used for the graphics controller interface to communicate with the host. The graphics controller is a VGA-compliant controller with 2D hardware acceleration and full bus master support. The graphics controller can support up to 1920x1200

resolution at high refresh rates. The PCI Express interface is also used for BMC messaging to other system devices using MCTP protocol.

The USB 2.0 Hub interface is used for remote keyboard and mouse, and remote storage support. BMC supports various storage devices such as CDROM, DVDROM, CDROM (ISO image), floppy and USB flash disk. Any of the storage devices can be used as a boot device and the host can boot from this remote media via redirection over the USB interface.

For the main capabilities of the BMC AST2500.BMC provide the 10/100/1000M local RJ45 management connector through BCM54612 and enable the communication between BMC and OCP A/PCH with NCSI BUS.

10. Thermal Design Requirements

To meet thermal reliability requirement, the thermal and cooling solution should dissipate heat from the components when system operating at its maximum thermal power. The thermal solution should be found by setting a high power target for initial design in order to avoid redesign of cooling solution; however, the final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. Thermal solution should not allow any overheating issue for any components in system.

The heat dissipation system includes 8pcs 6056Fan & 4 CPU HS, which can support normal operation at 35 C without risk of over-temperature and device frequency reduction. According to the maximum configuration evaluation, the heat dissipation under 205W CPU*4+3 300W GPU configuration is risk-free. The proportion of heat dissipation power is less than 12% under the normal operation of the system.

10.1 Data Center Environmental Conditions

The thermal design needs to satisfy the data center operational conditions as described below.

10.1.1 Altitude

Data centers could be located up to 1500 meters above sea level.

In the simulation, the influence of altitude factor is considered. The simulation is carried out according to the air density at 1500 meters altitude. The PA test is carried out at high altitude and low pressure, and the test data do not exceed the temperature.

10.1.2 Cold-Aisle temperature

We adopt the most advanced PID control fan method in the industry. The fan speed is positively correlated with the device temperature. Within the maximum heat dissipation capacity of the system, it can ensure that all parts of the system are running in spec, so as to achieve the best point of system power consumption and heat dissipation reliability.

10.1.3 R.H

Most data centers will maintain the relative humidity to be between 20% and 80%. In the thermal design, the environmental condition changes due to the high altitude may not be considered when the thermal design can meet the requirement with maximum relative humidity, 80%.

PA test and heat dissipation test will be carried out in the most stringent test environment, 80% humidity or even higher humidity are tested.

10.2 Server operational condition

10.2.1 Inlet Temperature

Inlet sensor has an accuracy of (+1 C). We will test the heat dissipation at the temperature of 20, 25, 30 and 35 to verify our heat dissipation scheme. Heat dissipation test will grab as many temperatures as possible in the system to judge, all temperatures can be passed.

10.2.2 Fan Redundancy

The server fans at N+1 redundancy should be sufficient for cooling server components to temperatures below their maximum spec to prevent server shut down or to prevent either CPU or memory throttling. Fan redundancy function is designed as our heat dissipation index at the beginning of the design.

10.2.3 Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component on the card. Otherwise, the thermal margin for every component in the system is at least 7% for inlet temperature up to 30°C.

According to the test results, the heat dissipation of high-risk heat dissipation components in the system can meet the margin requirement of 2%. The CPU part of the maximum heat dissipation pressure component has a residual of about 5 °C ~35 °C, and the GPU part has a residual of about 4 °C.

10.3 Thermal kit requirements

10.3.1 Heat Sink

The heat sink design should choose to be most optimized design with lowest cost. The heat sink design should be reliable and the most energy efficient design that satisfies all the conditions described above.

The system uses 2U standard Purley platform radiator. In order to consider the power consumption and reliability of the system, under the CPU shadow layout, there is a differentiated design part to minimize the temperature difference of the CPU.

10.3.2 System Fan

The system fan must be highly power-efficient with dual bearing. The propagation of vibration cause by fan rotation should be minimized and limited. The frame size of fan is 60x60x56mm and the quantity of fan is 8PCS. The power supply for fan should use 2 pin P12V to avoid current over spec. Under the normal operation condition of the system, the fan efficiency reaches more than 40%. The maximum current of the fan is 5.7A/unit.

10.3.3 Air-Duct

The air duct needs to be part of the motherboard tray cover, and must be most energy efficient design. The air-duct design should be simple and easily serviceable. For

different config, system can change the air-duct to meet. Using highly green material or reusable material for the air duct is preferred.

The design of the wind guide hood takes into account the different configuration and collocation as well as the possible expansion in the future. On the basis of meeting the heat dissipation requirements, it is as simple and practical as possible.

10.3.4 Thermal sensor

The sensors we have used all high-precision sensors. Inlet sensor can guarantee the accuracy of ±1℃, and other sensors can guarantee the accuracy of ±2℃.

11. Environmental and Regulations

11.1 Motherboard high altitude

11.1.1 Operational at 1500 meters above sea level

11.1.2 Non-Operational at 12192 meters above sea level

11.2 Motherboard relative humidity

11.2.1 Operating and Storage relative humidity: 10% to 90% (non-condensing)

11.3 Motherboard Temperature

11.3.1 operating temperature range: -5°Cto +45°C

11.3.2 Storage temperature range: -40°C to +70°C

11.3.3 Transportation temperature range: -40°Cto +70°C(short-term storage)

11.4 Full system high altitude

11.4.1 Operational at 1500 meters above sea level

11.4.2 Non-Operational at 12192 meters above sea level

11.5 Full system relative humidity

11.5.1 Operating and Storage relative humidity: 10% to 90% (non-condensing)

11.6 Full system Temperature

11.6.1 operating temperature range: -5°C to +35°C

11.6.2 Storage temperature range: -40℃ to +70℃

11.6.3 Transportation temperature range: -40℃ to +70℃ (short-term storage)

11.7 Full system Vibration & Shock

11.7.1 Operating Vibration:

0.2g acceleration, 5 to 500 Hz, 15minutes per each of the three axes, Transportation temperature range: -40℃to +70℃ (short-term storage)

11.7.2 Non-Operating Vibration:

2.2g acceleration, 5 to 500 Hz, 10minutes per each of the three axes

11.7.3 Operating Shock: 2g, half-sine 11mS, 100 shocks per each of the three axes.

11.7.4 Non-Operating Shock: 25g, 2 shocks per face

12. Mechanical

12.1 External Chassis

3U Rack mount sever in 19-inch rack frame. Chassis form factor: 943mm(D)*441mm(W)*130mm(H).
There are 2 kinds of chassis. The 8*M.2/GPU-BOX and the GPU Chassis Form-Factor.

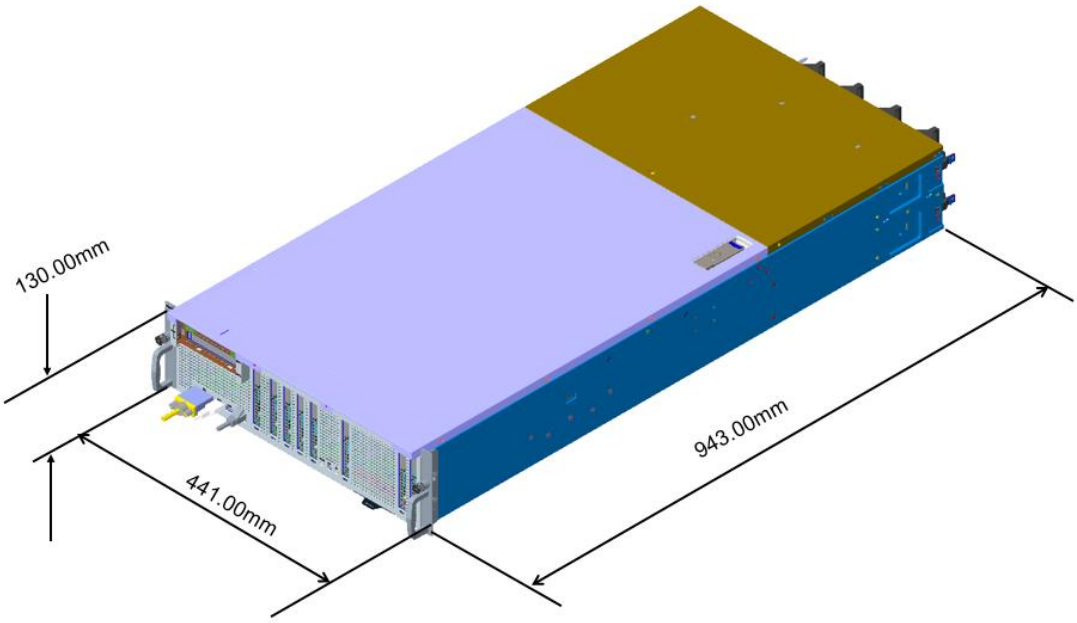


Figure12-1: Chassis Form-Factor（8*m.2/GPU-BOX）

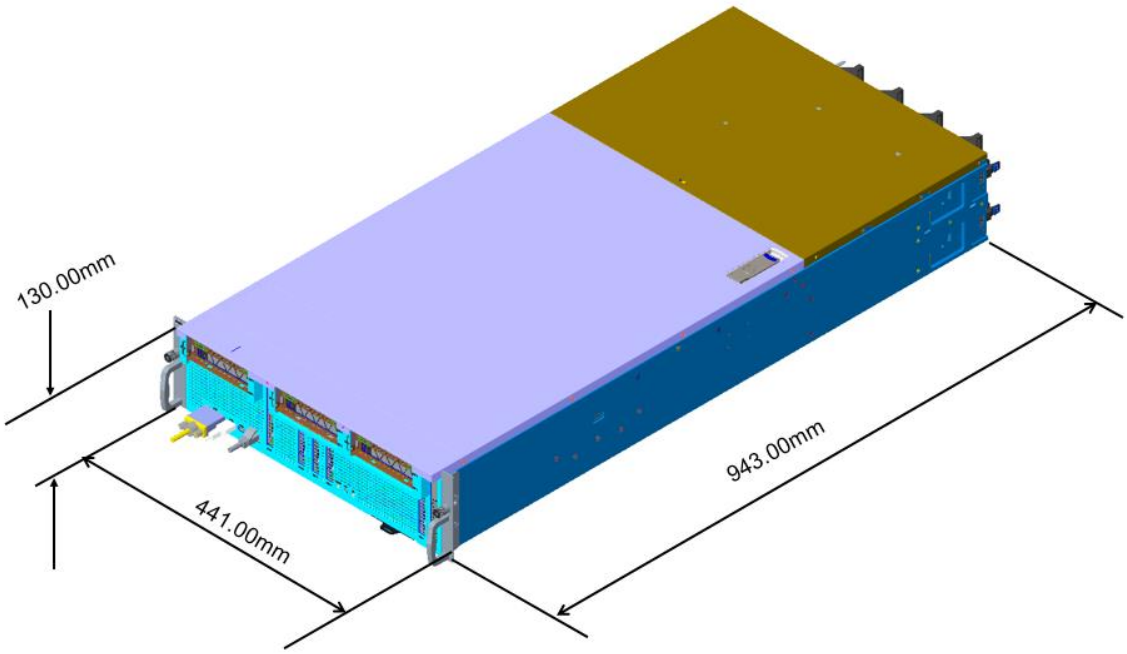


Figure12-2: Chassis Form-Factor（GPU）

12.2 HDD Carrier

1x3.5’’ HDD Carrier is supported， tool-less design is preferred.

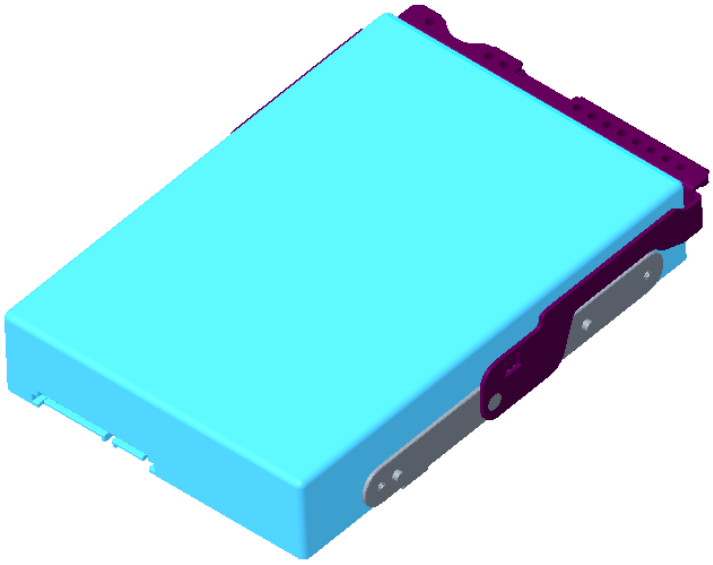


Figure12-3: 3.5’’ tool-less HDD Carrier

12.3 Fan Module

Fan module should be hot-plug and convenient for disassembly and assembly.

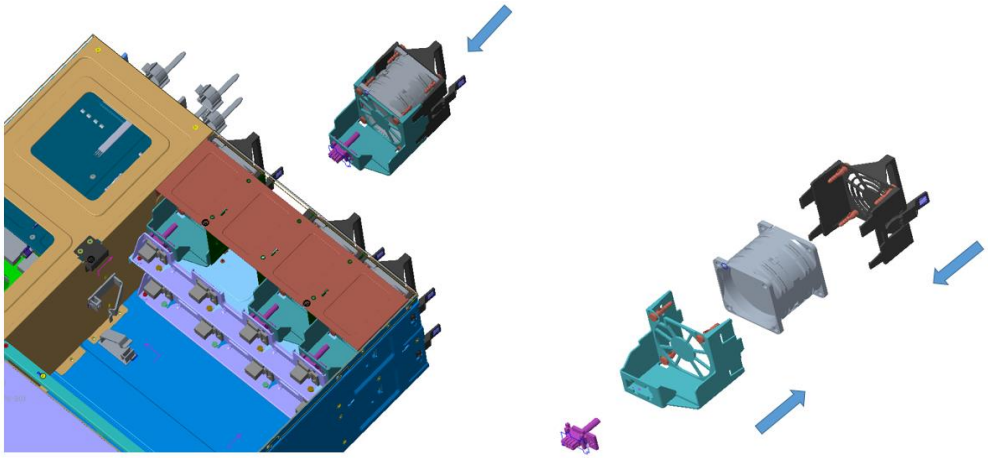


Figure12-4: Fan Module

12.4 PCIE Module

PCIe related designs should follow PCIe specification.
At first the PCIe device is needed to assembled into the PCIe bracket, then assemble into the chassis. The PCIe card’s assembled method is relatively simply. It is tool-less design.

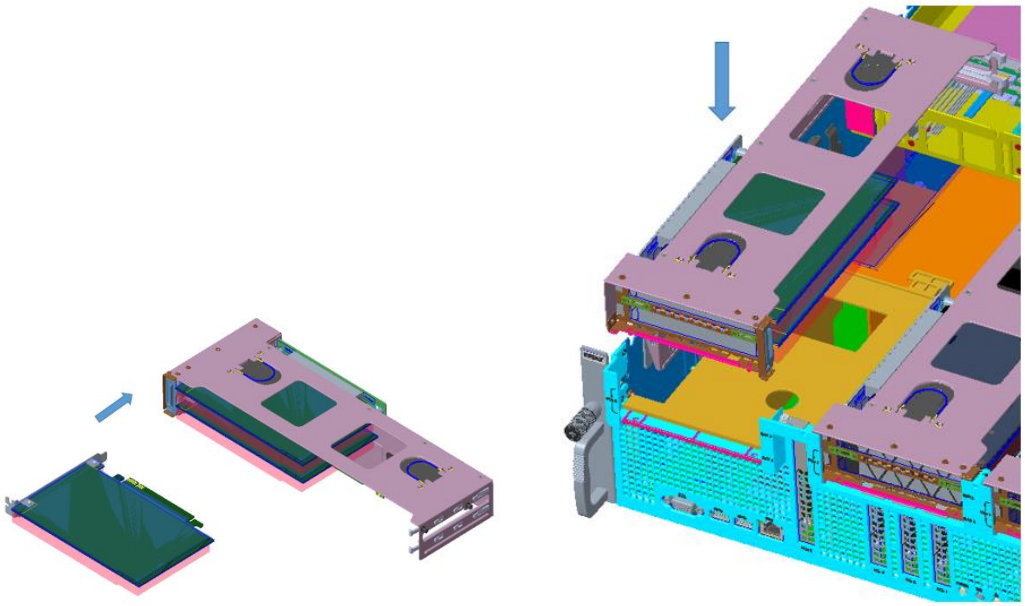


Figure12-5: PCIe Module

12.5 Front View

GPU-Box interconnection or up to 8Xm.2 or up to 3GPU is supported.

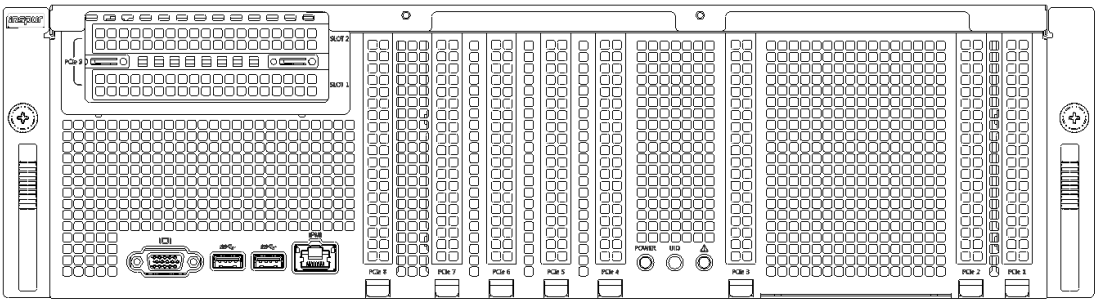


Figure12-6: Front View-GPU-Box/8*m.2

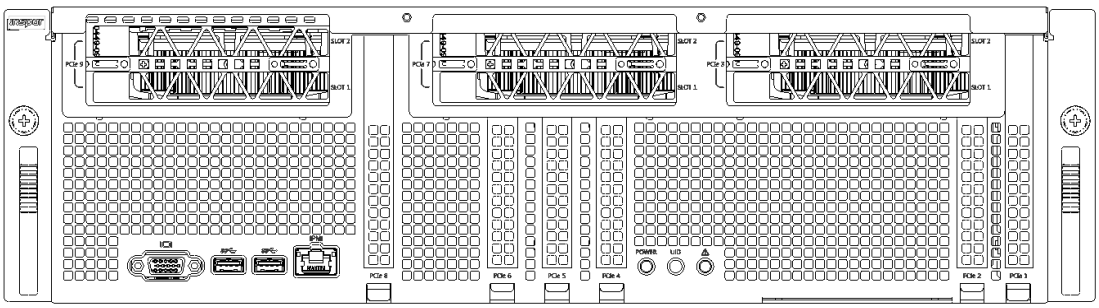


Figure12-7: Front View-GPU

12.6 Rear View

8 Fan and 4PSU is supported.

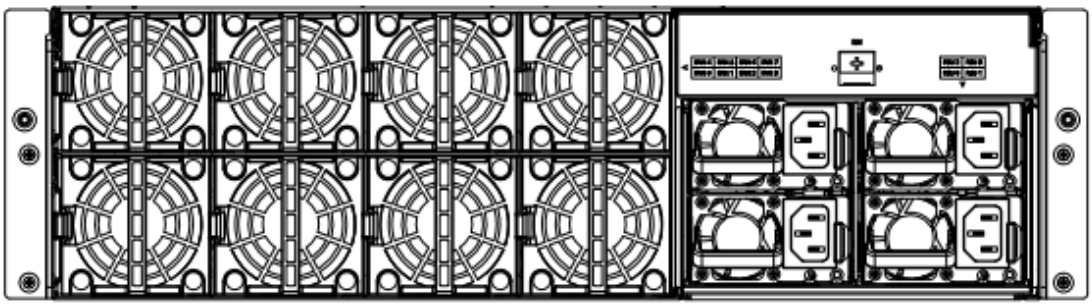


Figure12-8: Rear View

13. Labels and Markings

13.1 Labels

The motherboard shall include the labels such as adhesive and silk screen labels on the component side of the motherboard.

13.2 Markings

The motherboard shall include the markings such as adhesive and silk screen markings in accordance with required international certification.

The Whistler shall include the following labels on the component side of the motherboard. The labels shall not be placed in a way that may cause them to disrupt the functionality or the air flow path of system.

Open top panel stickers	Adhesive label	Yes
Component description stickers (rear panel view、motherboard view……)	Adhesive label	Yes
Host nameplate label	Adhesive label	Yes
Carton configuration label	Adhesive label	Yes
The serial number label	Adhesive label	Yes
Certification label (FCC)	Adhesive label	Yes
Remove the protective film label	Adhesive label	Yes
More power supply label	Adhesive label	Yes