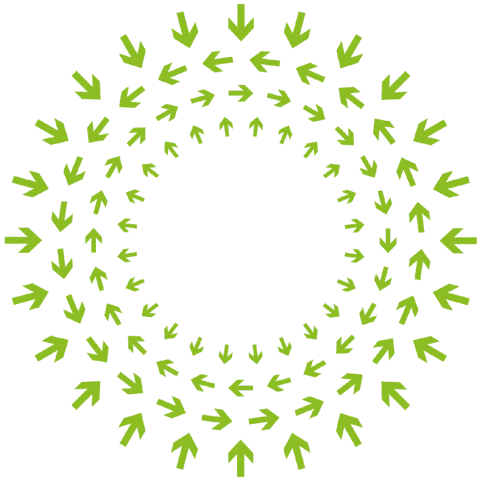


Open Rack V3 +/- 400V to 50V 18kW PSU Design Specification

Version: 1.0.0

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Table of Contents

Table of Contents 3
Revision History 6
1. Scope 7
1.1 Glossary of Acronyms 7
2. Overview 9
3. Electrical Requirements 9
3.1 DC Input Voltage & Frequency 9
3.2 Start-up Sequence 9
3.3 Turn on – Cold Start 10
3.4 Turn on – DC Failure / Recovery 10
3.5 Input Over Voltage Protection 10
3.6 Input Over-Current Protection 10
3.7 DC Inrush Current & Re-rush Current 11
3.8 Efficiency 12
3.9 DC Output voltage 12
3.10 DC Output set point voltage accuracy 12
3.11 DC Output droop voltage 12
3.12 DC Output Voltage Ripple & Noise 12
3.13 Dynamic Response 12
3.14 Overshoot at Turn on / Turn off 13
3.15 Hold-up Time 13
3.16 DC_Loss_L Signal (Reserved) 14
3.17 Pulse power requirements 15
3.18 Output Over Voltage Protection (OVP) 16
3.19 Over Power / Current protection 16
3.20 Over Power/Current Protection Limits 16
3.21 Output Short-circuit Protection 16
3.22 Over Temperature Protection 16
3.23 Active Current Sharing Accuracy through analog bus 17
3.24 power supplier physical addressing 17
3.25 LED 17
3.26 Grounding 18
3.27 Y-Cap 18
3.27.1 Start-up (0V to 50V) Transition procedure 19
3.28 Power system stability requirements 19
3.29 PSU connector pinout 19
3.30 Interoperability 22
4. Communication 22
4.1 Firmware Upgrade 23
4.2 Suggested implementation 23

4.3 Metering Accuracy 24
4.4 Blackbox Function 24
4.4.1 Fault Log History 25
5. Environment 25
5.1 Temperature 25
5.2 Humidity 25
5.3 Altitude 25
5.4 Acoustic Noise 26
5.5 Vibration and Shock (non-packaged) 26
5.6 Package Vibration, Drop and Compression 26
6. Thermal 26
6.1 Operational 26
6.1.1 Airflow direction 26
6.1.2 DeltaT 26
6.1.3 Thermal Margin 27
6.2 Thermal design requirements 27
6.2.1 Sensor accuracy 27
6.2.2 System fan(s) 27
6.2.3 Surface temperature 27
6.3 System Fan Failure 28
6.4 PSU Module Thermal Monitoring 28
6.5 Shelf output busbar clip temperature monitoring and protection (if selected) 28
7. Mechanical 28
7.1 PSU Physical Dimensions 29
7.2 Construction 29
7.3 Materials and Fasteners 30
7.4 Latch & Handle Requirements 30
7.5 EMI Gaskets 31
7.6 Chassis Interface 31
7.7 Rear Blind Mate Connector 31
7.8 Rear Blind Mate Connector Protection 32
7.9 Mechanical Drawings 33
8. Reliability and Quality 34
8.1 Component Derating Analysis (WCSA) 34
8.2 MTBF Requirements 35
8.3 Design Failure Mode and Effect Analysis (DFMEA) 35
8.4 High Accelerated Life Test (HALT) 35
8.5 NPI Reliability Tests 35
8.6 Disallowed Components 36
8.6.1 Capacitors 36
8.6.2 Sheet Metal Material and Zinc Whisker Implications 36
8.6.3 Mix-source Builds 37

9. Manufacturing Quality Control and Testing **37**
9.1 Manufacturing Testing 37
9.1.1 Incoming Quality Inspection 37
9.1.2 In-Circuit and Parametric Test 38
9.1.3 Burn-In (BI) and Ongoing Reliability Testing (ORT) 38
9.1.4 Hipot and Ground Continuity Test 38
9.2 Automation and Continuous Improvement 38
9.2.1 Conformal Coating 39
9.3 Quality Control Process 39
9.4 Warranty and Failure Analysis 39
9.5 Product Change Notification 39
10. Compliance requirements **40**
10.1 Safety Standards 40
10.1.1 Safety requirements 40
10.2 EMC Requirements 41
10.3 Environmental Compliance 42
10.4 Documentation 42

Revision History

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1. Scope

This document defines the technical specifications for Open Rack V3 HVDC IT Rack HVDC input power supply used in the Open Compute Project.

1.1 Glossary of Acronyms

The following acronyms and abbreviations are used throughout this specification:

Acronym	Definition
AC	Alternating Current
ASTM	American Society for Testing and Materials
AVL	Approved Vendor List
BBU	Battery Backup Unit
BI	Burn-In
BOM	Bill of Materials
CAD	Computer-Aided Design
CB	Certification Body
CE	Conformité Européenne (European Conformity)
CFM	Cubic Feet per Minute
CISPR	Comité International Spécial des Perturbations Radioélectriques (International Special Committee on Radio Interference)
CLA	Contributor License Agreement
COG	Ceramic of Glass (C0G capacitor dielectric)
CPK	Process Capability Index
CSA	Canadian Standards Association
DC	Direct Current
DFM	Design for Manufacturability
DFMEA	Design Failure Mode and Effect Analysis
DMTBF	Demonstrated Mean Time Between Failures
DVT	Design Verification Test
ECHA	European Chemicals Agency
EEE	Electrical and Electronic Equipment
EIA	Electronic Industries Alliance
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPA	Environmental Protection Agency
EU	European Union
EVT	Engineering Verification Test
FA	Failure Analysis
FAI	First Article Inspection
FCC	Federal Communications Commission
FET	Field-Effect Transistor
FW	Firmware
GPU	Graphics Processing Unit
GR&R	Gage Repeatability and Reproducibility
HALT	High Accelerated Life Test
HVDC	High Voltage Direct Current
HW	Hardware
I2C	Inter-Integrated Circuit

IEC	International Electrotechnical Commission
IPC	Institute for Printed Circuits (now Association Connecting Electronics Industries)
ISTA	International Safe Transit Association
LED	Light-Emitting Diode
MOS/MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean Time Between Failures
NPI	New Product Introduction
NPO	Negative-Positive-Zero (capacitor temperature coefficient)
NRTL	Nationally Recognized Testing Laboratory
OCP	Over-Current Protection / Open Compute Project (context-dependent)
ORT	Ongoing Reliability Testing
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
OWFa	Open Web Foundation Agreement
PC/ABS	Polycarbonate/Acrylonitrile Butadiene Styrene
PCBA	Printed Circuit Board Assembly
PCN	Product Change Notification
PCR	Post-Consumer-Recycled
PDU	Power Distribution Unit
PE	Protective Earth
PFAS	Per- and Polyfluoroalkyl Substances
PFMEA	Process Failure Mode and Effect Analysis
PMI	Power Management Interface
PMM	Power Management Module
PN	Part Number
PSU	Power Supply Unit
PVT	Production Verification Test
PWM	Pulse Width Modulation
RCCA	Root Cause Corrective Action
REACH	Registration, Evaluation, Authorisation and Restriction of Chemicals
RH	Relative Humidity
RMA	Return Merchandise Authorization
RoHS	Restriction of Hazardous Substances
ROM	Read-Only Memory
RPM	Revolutions Per Minute
SCP	Short-Circuit Protection
SEC	Securities and Exchange Commission
SELV	Safety Extra-Low Voltage
SGCC	Steel Galvanized Cold Commercial
SMT	Surface-Mount Technology
SN	Serial Number
SPC	Statistical Process Control
SW	Software
TOR	Top of Rack
UL	Underwriters Laboratories
UVP	Under-Voltage Protection
WCSA	Worst Case Stress Analysis
WEEE	Waste Electrical and Electronic Equipment

2. Overview

This specification defines the HVDC input power supply that fit into the 49V power shelf. The power supply is intended for use on a power shelf that is part of the rack, for supplying DC power to system loads. The power supply operates based on “narrow range 48V Architecture.” Based on this concept, power supply output voltage is 50V with an adjustable range. Benefits of this architecture compared to Orv2 with 40~60V dc voltage range are:

- Voltage range as low as possible to eliminate oversized voltage/current design
- Widely enable 4:1 fixed ratio converters and downstream conventional 12V PoL converters.
- Power to flow naturally, not with Software control and dependency.
- Enable simple fixed-voltage power supplier design.

3. Electrical Requirements

Requirements Brief Summary is given below:

- 18kW output power.
- Input rated nominal voltage +/- 400Vdc with +/- 5%
- Peak efficiency> 98.5%, and full load efficiency > 97.5% measured with fans @ 25°C inlet air temperature
- DC Output overvoltage and overcurrent protection
- DC Input overvoltage and undervoltage protection
- Over-temperature warning and protection
- Active current sharing on top of droop
- Hot insertion/removal (hot plug)
- Front to back air cooling
- Internally controlled variable-speed system fan
- Ability to field FW upgrade (with bootloader)

3.1 DC Input Voltage & Frequency

The power supplier shall be capable of supplying full rated output power

Parameter	Nominal	Min	Max	Output Power Rating (kW)
DC Input Voltage	+/- 400Vdc to +/- 410Vdc	+/-380V dc	+/-420 V	18kW

Table 1 : DC Input Voltage & Frequency Requirements.

Table above specifies the DC input voltage requirements for continuous operation. PSU minimum and maximum operating voltage can be limited further by software. If PSU input voltage goes out of the range while operating at any load value, PSU shall power relay within 6 ms.

3.2 Start-up Sequence

The power supply shall be able to start up under rated nominal power at the min DC input voltage as specified in Table 1 above. With DC present, within specified parameters, the power supply must always remain operational. The startup sequence shall be designed such that the power

supply is able to meet the overall system start-up time and inrush current requirements specified later.
After DC voltage is applied, the internal bias supply starts, the microcontroller boots and keeps the DC-DC converter off. Then the microcontroller closes the inrush relay and turns on all the converters.

3.3 Turn on – Cold Start

The output voltage of the power supplier shall be monotonic during turn on and turn off, there shall not have any reverse voltage during turn off.

- The DC output voltage rise time without external capacitors should be less than **200ms** with 120% constant-current limit. If after 10s the output voltage isn't at the required level, the PSU shall consider this event as OCP and restart once.
- The max capacitive loading on a single unit at power up is 60 mF.
- For any loads (from 'no-load' to 'max-load'), the output voltage will rise monotonically from $0V_{DC}$ to $50V_{DC}$, without overshoot or ringing, at any turn on following application of DC input voltage, and anytime when the PSU resumes functionalities after an automatic protection condition (including parallel operations). The output voltage will fall monotonically from $50V_{DC}$ to $0V_{DC}$, without undershoot or ringing.
- Output voltage shall never reverse polarity at the turn off (all conditions and converters).

3.4 Turn on – DC Failure / Recovery

The power supplier shall recover automatically after an DC power failure. The start-up time requirement shall be the same as that of a cold start specified in section above.
The PSU shall include a soft-start that promptly resets at any input DC loss > 2 ms, or after any automatic protection conditions.

3.5 Input Over Voltage Protection

The power supplier shall contain protection circuitry such that application of an input voltage below the minimum and above the maximum specified in Table 1 shall not cause any damage to the power supplier and shut down while operating. The power supplier shall shut down if the input voltage is over 450V for 20ms.

3.6 Input Over-Current Protection

The power supplier shall incorporate primary fusing on both input and return lines for input over-current protection to meet product safety requirements. Fuses shall be selected to prevent nuisance trips. Fuse may be internal to the unit and need not be user serviceable. DC inrush current shall not cause the fuse to blow under any conditions. No power supplier operating condition shall cause the fuse to blow unless a component in the power supplier has failed. This includes DC output overload and short-circuit conditions. Fuse shall be approved by UL for an interrupt rating of at least 20kA.

PSU fuse shall be in coordination with the HPRv4 DC PDU fuse curve as given below (subject to change)

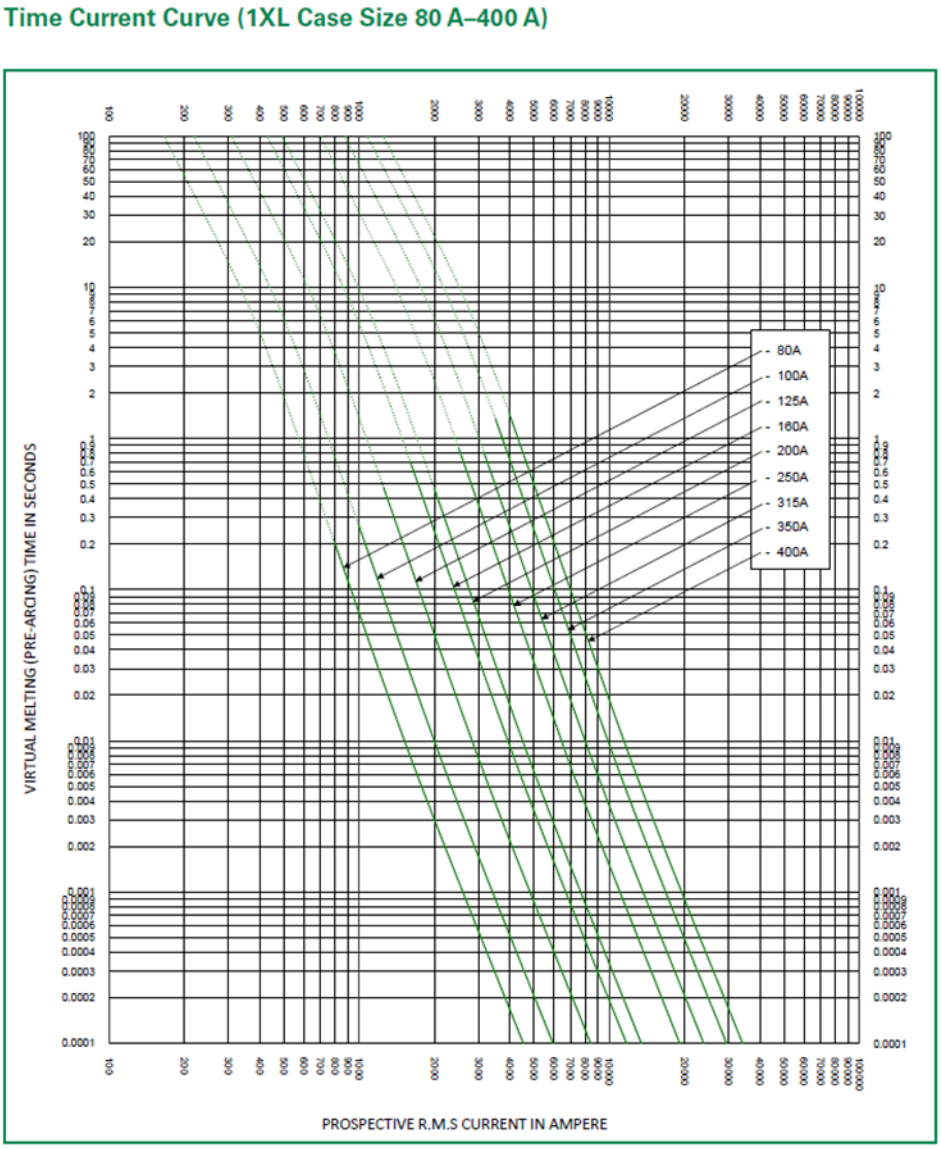


Figure 1: HVDC PDU PSX Fuse Curve

3.7 DC Inrush Current & Re-rush Current

1) DC Inrush Current
   Maximum DC inrush current from cold power-on shall be limited to no greater than 30A. This specified inrush current shall not include the X-Capacitors charging.

2) Re-rush Current
   Maximum DC re-rush current at DC recovery after dropout shall be less than 150% times of the steady-state current for less than 2ms. The steady-state current varies with the input DC voltage and loading levels.

This specified re-rush current shall not include the X-Capacitors charging.

3.8 Efficiency

The efficiency of the power suppliers when measured at an DC input voltage of +/-400V and with the cooling fans connected (with input and output voltage measured at corresponding connectors, at 25 C ambient and after 30 minutes running at full load) shall meet the requirements outlined in Table below.

Input voltage	Peak Efficiency (%)	full load Efficiency (%)
+/- 400V	98.5	97.5

Table 2: Efficiency Requirements

3.9 DC Output voltage

The DC output voltage of the power supplier shall be fixed at 50V @NL and 49V@FL while in normal operation. The power supplier output voltage set point shall be adjusted via Modbus by +/-1V.
The power supplier shall supply rated power for the entire range of DC output voltage.

3.10 DC Output set point voltage accuracy

The power supplier set point output voltage accuracy at 100% load shall be +/-0.2% or +/-0.1V for 49V. This can be accomplished by EoL calibration.

3.11 DC Output droop voltage

The power supplier droop voltage (0%-100%) shall be 1V by default (with the tolerance of +/-0.1V). That means output voltage is 49V at 100% load and 50V at no-load. The droop extends linearly to 150% (it means at 150%, the droop is 1.5V, and voltage is 48.5V).

3.12 DC Output Voltage Ripple & Noise

The DC output voltage ripple and noise shall not exceed 500 mV peak to peak. Ripple and noise are defined as periodic or random signals over a band of 5Hz to 100MHz measured across a steady-state resistive load. Measurements shall be made differentially using an oscilloscope with 100Mhz bandwidth limit enabled. Compliance will be verified using a 0.1uF capacitor connected locally to the oscilloscope probe tips during this measurement.

3.13 Dynamic Response

Under these testing conditions, the DC output voltage shall not vary by more than specified for undershoot and overshoot with 3ms settling time (with and without capacitive loading on a single unit of 60mF). The measurement shall be from the new steady state value (due to droop) to the voltage spike/dip peaks during a transient load.

Step load increase or decrease	Frequency	Transient load rate	Max undershoot and overshoot
50% step load (10% min. load)	Up to 10kHz	5 A/uSec	1.5V
90% step load (10% min. load)	Up to 6.5kHz	5 A/uSec	
140% step load (10% min. load)	Up to 4kHz	5 A/uSec	

Table 3. Dynamic load requirements.

Dynamic load profiles under test include but not limited to the ones shown in Table 4.

No.	Low load	High load	Duty cycle	Frequency
1	10%	60%	50%	20Hz, 100Hz, 500Hz, 1kHz
2	50%	100%	50%	
3	10%	100%	50%	
4	10%	150%	50%	
5	10%	60%	50%	10kHz
6	50%	100%	50%	10kHz
7	10%	100%	50%	6.5kHz
8	10%	150%	50%	4kHz

Table 4. Example dynamic load profiles.

3.14 Overshoot at Turn on / Turn off

The output voltage overshoot upon the application or removal of DC input voltage, under the specified input voltage defined before, not to exceed 1V.

3.15 Hold-up Time

Minimum 6ms holdup time requirements at full load condition. Holdup time is calculated from the time DC input is lost till the time the output voltage is out of acceptable 48V range.

3.16 DC_Loss_L Signal (Reserved)

(This signal is just reserved, the description in this section is for reference only, not required)

DC_Loss_L signals have been added to the PSU (Power Supply Unit) and BBU (Battery Backup Unit) to enable control during DC loss events. Each PSU now has an output DC_Loss_L signal, while each BBU has two input DC_Loss_L signals.

The following is the diagram of DC_loss_L signal connection.

Diagram of ORV3 PSU/BBU AC_LOSS & PULSE_MGMT Signals for AC to BBU Transition

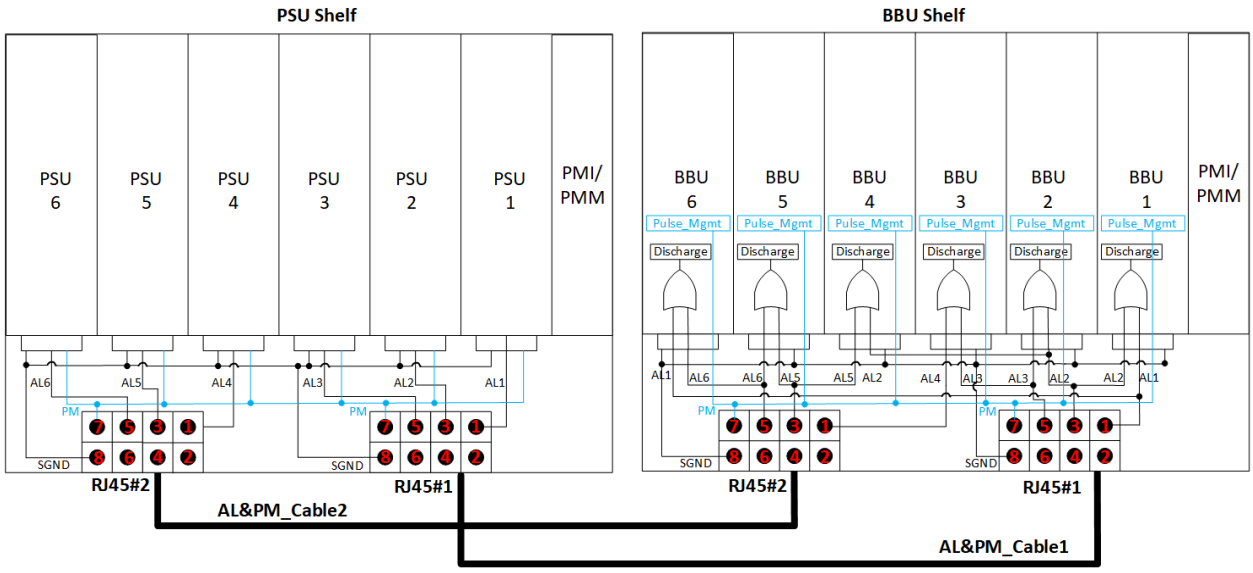


Figure 2: *DC_Loss_L Signal Connection Diagram*

The DC_Loss_L signal assertion shall be triggered by the following conditions using a logic "OR" operation to ensure proper backup operation under all conditions.

1) Upon detection of DC loss, the PSUs should assert the DC_Loss_L signal after a validation delay of 4-5ms.
2) The second condition for DC_Loss_L assertion will be based on the threshold of the remaining bulk capacitor energy, which should be kept at a minimum of > 5ms to allow sufficient time for the BBU to ramp up.
3) When other DC faults happen (input UVP/OVP/UFP/OFP), the PSUs should assert the DC_Loss_L signal after certain validation delays.

When a BBU receives the active DC_Loss_L signals, BBU will pull the Sync_Start_L signal low, allowing the BBU shelf to initiate immediate discharge.

After DC restores to normal condition, the PSU shall deassert the DC_Loss_L signal after a minimum of 500ms validation delay upon detecting the PSU main output is powered up. This ensures the safe transition from PSU to BBU and keeps the 50V bus voltage high.

The PSU DC_Loss_L signal can be toggled through Modbus for testing purposes, including cable connections, to ensure the proper battery backup operation.

To avoid BBU over-discharging due to single fault conditions like PSU input fuse open, the PSU shall deassert the DC_Loss_L signal after DC_Loss_L asserted for 300s.

3.17 Pulse power requirements

The power supply unit (PSU) should be capable of supporting the following repetitive peak pulse load while maintaining output within regulation and input power within the maximum limit.
≤140%, ≤50ms moving average
≤160%, 400us moving average
≤100%, ≥1s moving average.

BBU backup should not be triggered during the pulse loading operation.
Maximum output voltage under/overshoot should meet the requirement in Table 3.
The PSU input current waveform shall not be clamped during pulse loading operation.

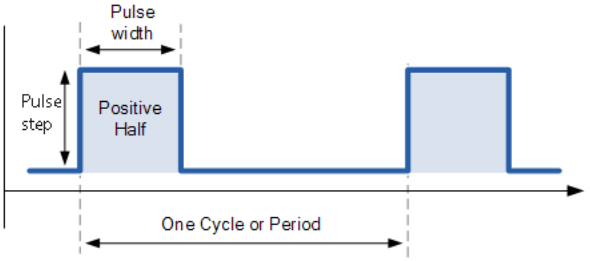


Figure 3: *Pulse Load Current Waveform*

Pulse load profiles under test include but not limited to the ones shown in Table 5.

No.	Low load	High load	T_low	T_high	Average load	Frequency	load current slew rate
1	70%	130%	0.05ms	0.05ms	100%	10kHz	5A/us
2	20%	140%	0.1ms	0.1ms	80%	5kHz	5A/us
3	40%	160%	0.1ms	0.1ms	100%	5kHz	5A/us
4	40%	160%	0.4ms	0.4ms	100%	1.25kHz	5A/us
5	0%	80%	1ms	1ms	40%	500Hz	0.3A/us
6	20%	140%	50ms	50ms	80%	10Hz	5A/us
7	60%	140%	50ms	50ms	100%	10Hz	5A/us

8	30%	140%	28.6ms	50ms	100%	12.7Hz	5A/us
9	30%	160%	0.34ms	0.4ms	100%	1.35kHz	5A/us
10	30%	160%	1.71ms	2ms	100%	269Hz	5A/us

Table 5 Example pulse load profiles.

3.18 Output Over Voltage Protection (OVP)

The power supplier shall shut down for DC output voltage exceeding 52.5V and the reacting time shall not exceed 200ms. For DC output voltage shall never exceed 54V (fast OVP).

3.19 Over Power / Current protection

If a PSU is overloaded higher than the values listed below in sections 3.20, it shall shut down. 5s after an overload shuts down, if detecting 50V bus voltage is alive, PSU shall retry once to sync turn on. Otherwise, PSU shall latch off. During the one-time retry with 50V bus, if the fault still presents, the PSU shall latch off.
No DC_loss_L signal shall be asserted during overload condition.
The latch off can be cleared by DC cycling, reseating or a Modbus command. The OCP retry counter shall be cleared 30 minutes after normal operation.

3.20 Over Power/Current Protection Limits

PSU shall be self-protected for any overcurrent and short circuit conditions.
PSU shall set multiple protection levels and delay time for over current and short circuit protection properly. The OCP settings should be reviewed by the design team. Below are the minimum limits required.

- Average power is more than 115% for 10s.
- Average power is more than 120% for 100ms.

3.21 Output Short-circuit Protection

The power supplier shall employ short-circuit protection to protect the power supplier and attached load in the case of an output short-circuit or other output overload condition.

If the PSU output voltage is lower than 10V (short circuit condition), the power supplier shuts off immediately. No component shall be damaged. PSU shall only retry once to sync start after 5s if detecting 50V bus voltage is still alive. Otherwise, PSU shall latch off.

No DC_loss_L signal (not used) shall be asserted during output short-circuit condition.
The latch off can be cleared by DC cycling, reseating or a Modbus command. The SCP retry counter shall be cleared 30 minutes after normal operation.

3.22 Over Temperature Protection

The power supplier shall employ over-temperature protection for both ambient over temperature and internal thermal temperature to protect the power supplier. The power supplier shall shut

down under over temperature condition and recover after a certain period after the over temperature condition is removed.
The OTP circuit shall incorporate built in hysteresis such that the power supply does not oscillate on and off due to temperature recovering condition. The OTP event shall be reported as a fault.

3.23 Active Current Sharing Accuracy through analog bus

The power suppliers shall have a dedicated analog bus with slow bandwidth for active current sharing.

- With the maximum number of power suppliers connected in the system, the current sharing accuracy shall be +/- 2% or better under load > 50% and +/- 5% or better under load >20%.
- Max setpoint increase (capture range) for the current regulation is 500mV.
- Current sharing bus (Ishare) voltage full scale shall linearly increase to 7V and scale up linearly up to 150% (10.5V).
- The PSU input impedance of the current sharing shall be 30kR & 100pF or better, and able to support at least 10x power shelves in parallel operation within one rack.
- Active current sharing and droop sharing response time should be minimized for cooperation with pulse power capacitor shelf. Active current sharing loop should meet the stability requirements.
    - The active current sharing total delay time, measured from the end of load current variation to the end of Ishare out variation should be less than 50us.
    - The active current sharing control bandwidth shall be less than 100Hz.

In the event of active current sharing gets broken, the PSU shall share the load through voltage drooping with accuracy up to 5 times the values above. The failure of a module inside the PSU should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to share load in parallel and be able to hot-swap.

3.24 power supplier physical addressing

Four power supplier signal pins are used for the slot physical addressing. There are digital signals that should have internal pull up resistors inside the power supplier. On the power shelf, these pins can be grounded (0) on left open (1) to determine power supplier location as below:
power supplier slot location 1: 0000
power supplier slot location 2: 0001
power supplier slot location 3: 0010
power supplier slot location 12: 1011

3.25 LED

The PSU will have a single blue and single amber LED mounted near the PSU handle for accessibility. Following are power supply LED States:

LED 1, Blue LED:

1) **Blinking Blue @ 4Hz frequency**: Sync Start State**,** PSU is ready to turn on its output and awaiting the sync Start signal
2) **Solid Blue**: 50V is ON and available
3) **No LED**: 50V output off

LED 2, Amber LED:

1) **Blinking Amber @ 4Hz frequency**: Bootloading

2) **Solid Amber**: Primary/Secondary/Fan/bootloading Failure and/or loss of DC output
    - (refer to PSU Modbus/Pmbus registers for specific failures)
3) **No LED**: fault NOT present/condition 1 and 2 are false.

- NOTE: toggling DC input power will reset the solid/blinking amber fault light but will come up again if faults re-occur.
- Only one of the 3 conditions per LED will be applied at ALL times.

Refer to the mechanical drawing for the suggested location of the LEDs.

3.26 Grounding

The protective earth ground pins shall be connected to the safety ground (power supply chassis). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

Power supply unit output voltage return shall not be connected to earth/safety ground.

PSU signal ground is directly connected to the output voltage return. A 10ohm resistor is reserved between the Shelf/PMI/PMM signal ground and PSU signal ground.

Signal ground coming from TOR shall be isolated from the PMI/PMM signal ground through a 10 ohm resistor.

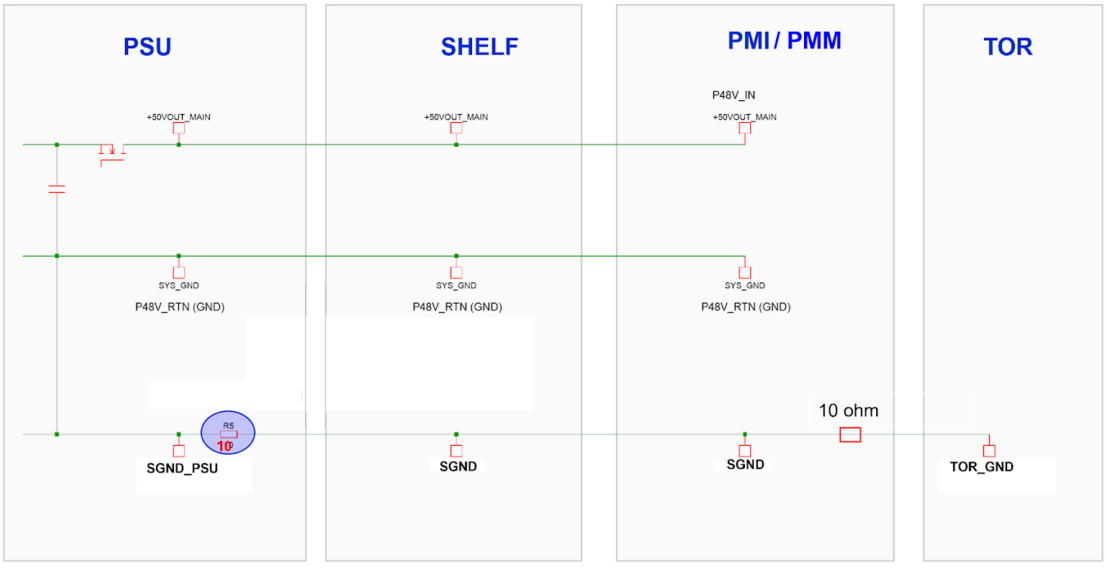


Figure 4: *PSU Grounding Diagram*

3.27 Y-Cap

There should be no Y-caps placed outside the Oring FET between 50V and chassis. This measure is taken to prevent single faults, hot plug inrush currents, and static state leakage currents.

3.27.1 Start-up (0V to 50V) Transition procedure

Each PSU has a small circuit to output a SYNC_START signal and all PSUs' SYNC_START signals are connected together on the power shelf backplane.

1) Each PSU sets its SYNC_START signal to high when the PSU is ready to turn on the output.
2) Only PSU in SLOT #1 generates a random timer and set SYNC_START to high when ready and the random timer is finished.
3) The PSUs will turn on the output when the SYNC_START signal is high.
4) If the SYNC_START signal is kept stuck low for 3s more than the max random timer limit, the PSU shall turn on immediately.
5) if PSU1 is not installed or its SYNC_START signal is stuck low, the other PSUs shall turn on within 10s. In this case a random timer doesn't exist.

Please refer to section 3.3 for the timing and constant current value requirements during the cold startup.

3.28 Power system stability requirements

Please see appendix A for power system stability requirements.

3.29 PSU connector pinout

Suggested PSU output connector: Amphenol 10169891-843202SLF

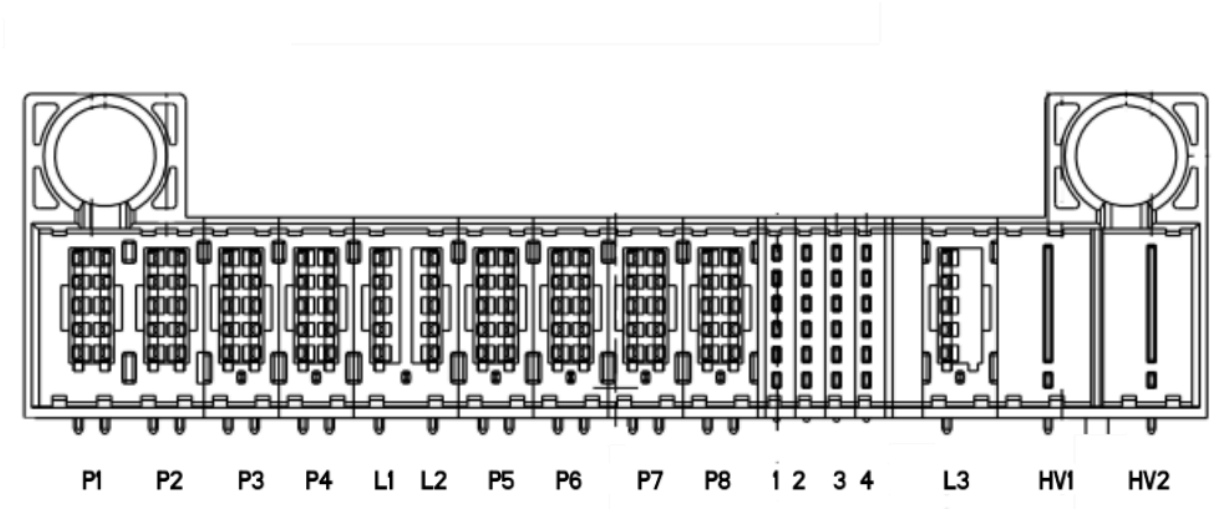
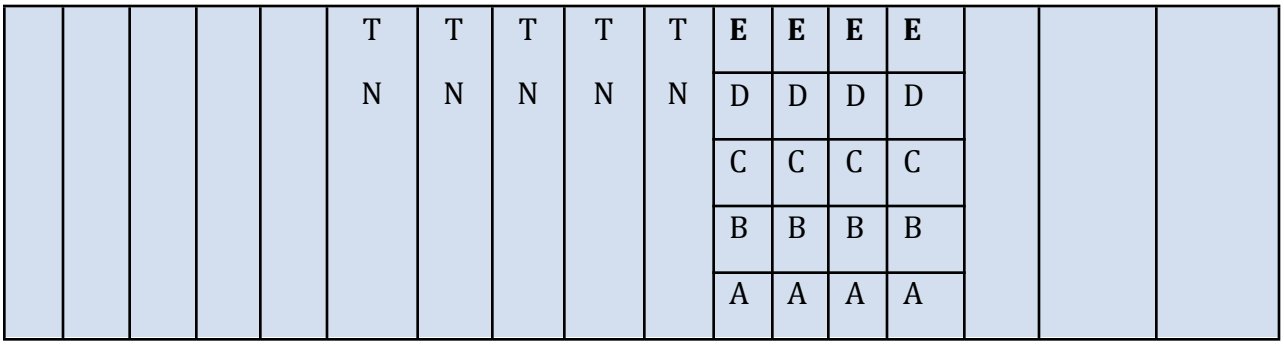


Figure 5: *PSU Output Connector*

Table 6: Pin mating sequence

P1	P2	P3	P4	L1	L2	P5	P6	P7	P8	1	2	3	4	L3	HV1	HV2
V1	V1	V1	V1	V1	R	R	R	R	R	**F**	**F**	**F**	**F**	PE	-400V	+400V



PSU Pinout	Signal Name	Type	Bus	Function	Comments
F1	PSU_A0	Input		Address 0 – PSU ID A0	Internal pull up 10k to 3.3V
F2	PSU_A1	Input		Address 1 – PSU ID A1	Internal pull up 10k to 3.3V
F3	PSU_A2	Input		Address 2 – PSU ID A2	Internal pull up 10k to 3.3V
F4	PSU_A3	Input		Address 3 – PSU ID A3	Internal pull up 10k to 3.3V
E1	Alert	Output/ Active Low	individual	Logic “Low ”= Fault or Waring Logic “High ”= OK	Open-collector/drain output, internal pull up 10k to 3.3V
E2	Reset_Latch_Fault	Input/ Active high	individual	high for 1-2s = clear faults and start PSU if not operating due to a fault	Should be enabled by SW. Internal pull down 10k resistor.
E3	Busbar_Clip+_Temp	Input		Busbar clip + contact temperature sensor	
E4	Busbar_Clip-_Temp	Input		Busbar clip – contact	

				temperature sensor	
D1	Input_Loss_L	output/ Active low			Open-collector/drain output, internal pull up 100k and a diode to 3.3V
D2	Ground	Ground	share bus	Signal ground	
D3	RS485A	BI	Share bus		
D4	RS485B	BI	Share bus		
C1	Input Sense1	Input	Active Low	Logic “Low ”= Output Turn on Logic “High ”= Output Turn off	Quick shut down Output, mitigate hot unplug arcing. Internal pull up to the Vcc refer to the PE.
C2	PSKILL (Short Pin)	Input	Active Low	Logic “Low ”= Output Turn on Logic “High ”= Output Turn off	Quick shut down Output, mitigate hot unplug arcing. Internal pull up 10k to 3.3V.
C3	Input Sense2	Input	Active Low	Logic “Low ”= Output Turn on Logic “High ”= Output Turn off	Quick shut down Output, mitigate hot unplug arcing. Internal pull up to the Vcc refer to the PE.
C4	Reserve				
B1	ISHARE	Analog	share bus	Main Output current share bus	
B2	I2C_SDA	BI	share bus	I2C Data	
B3	I2C_SCL	BI	share bus	I2C Clock	

B4	Ground	Ground	share bus	signal ground	
A1	Present_L	Output	Individual	Low: PSU present	1. 10Ω pull-down inside PSU~~/BBU~~ module. 2. 4.7k pull-up inside PMM. 3. Connecting to PMM2 edge connector pin A27/B27/A28/B28/A29/B29/B19/A20/B20/A21/B21/A22 respectively.
A2	DC_Fault_CLR/Sync_stop	BI	share bus	clear latch off flag after DC fault event	Open-collector/drain output; Internal pull up 100k and a diode to 3.3V
A3	Sync_Start	BI	share bus	Synchronizing turn-on main output	Open-collector/drain output, Internal pull up 100k and a diode to 3.3V
A4	PS_Off	reserved			

Note:

1. The pull up resistor of all the shared signals should be individually in series with a Schottky diode, so the problem in one PSU doesn't impact other PSUs.
2. Logic signals level (3.3V high and 0V low) measured on both PSU-level and shelf-level should meet the requirements of >=3V for high and <=0.3V for low in different operation conditions.

3.30 Interoperability

The PSU modules and PSU shelves (including the PMM module) from different suppliers shall be interoperable and interchangeable. All PSU modules on the same rack must be from the same supplier.

4. Communication

The power suppliers shall be able to communicate on ModBus (up to 115kbps). See related Appendices.

The software interface shall be operational when the DC input is present or when the DC output bus is powered up by other power sources. Refer to the register maps for fault/read/write registers that PSU should communicate.

4.1 Firmware Upgrade

The interface shall allow the user to re-flash firmware on the device. Firmware upgrade shall result in no power interruption on the shelf level (the unit being upgraded can go offline.) Upgrades can be done 1 power supplier at a time. PSU output voltage interruption due to FW upgrade shall be less than 5s.

The PSU FW shall maintain regulation on the output during Send, Install and verification of the new FW, and only require a soft reset (that may reset the output for a short period in a few seconds)

4.2 Suggested implementation

Traditional designs have the following implementation on it is micro flash at high level:

Upon micro boot, when FW update is not enabled, i.e., the unit is not being updated, the unit boots into the application mode and carries out the operation.

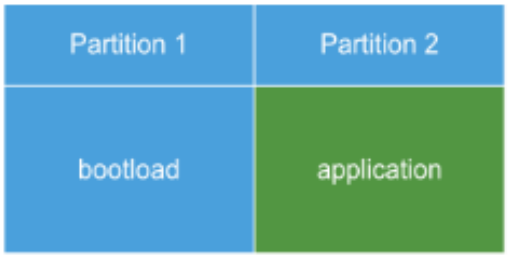


Figure 6: *Firmware Boot Process (Two Partitions)*

As an update is initiated, the bootloader partition is leveraged for the duration of the update, the new FW is then installed in the application partition, a soft reset occurs, and unit boots into the newly installed application

In the improved method, the micro flash can be split in 3 partitions.

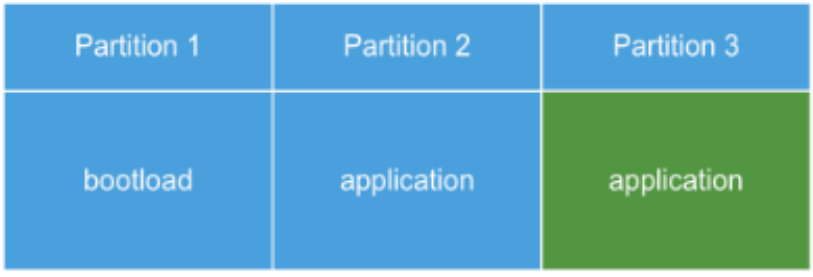


Figure 7: *Firmware Boot Process (Three Partitions)*

The application operations can carry as before. So will the FW update, however, the update will occur on the partition that is not currently running, once the FW install is complete, the unit resets and boots into the newly installed image. This has the benefit of having a last good copy of the FW on the PSU at all times as well.

Note that this implementation depends on the architecture of the microcontroller used, in some cases, 3 separate partitions are not required, and a similar process can take place with two partitions in the flash and the presence of a ROM.

4.3 Metering Accuracy

Accurate reporting of input power (power factor, input current, input current harmonics and voltage) and output power (output current and voltage) readings shall be reported via communication system at all rated voltage.
The accuracy shall be maintained across the operating temperature range and DC input range.

Metering accuracy specification:

Table 7: *Metering Accuracy Specifications*

Parameter	Load	Accuracy
DC input power	<10%	±7%
	10-<20%	± 5%
	20-100%	±3%
DC input current	<10%	±0.5A
	10-<20%	±2%
	20-100%	±1%
DC input voltage	0-100%	±1%
Output voltage	0-100%	±0.5%
Output current	10-20%	±10%
	20-40%	±2%
	40-100%	±1%
Output power	<10%	±5%
	10-<20%	±3%
	20-100%	±2%

4.4 Blackbox Function

For the following section please refer to the Communication Specification in Appendix A for detailed information.

The black box function shall store key important data to be used when a fault occurs.

- Shall store data in memory and be able to withstand several read/write cycles
- PSU shall be able to store failure data before the PSU turns off/fails even in catastrophic failure events both on primary and secondary side. Hold up time of the blackbox microcontroller must be able to store all the information and then shutdown.
- Last 4 events stored in memory.
- DC input current, DC input voltage, Input Power, DC output voltage, DC output current,
- Temperature readings, system fan speed, input voltage, output voltage, bulk voltage, various error codes from all the different converters (OTP, OVP, OCP,UVP), and warnings.
- Total run time of PSU
- Run time since last turn on
- Real time stamping
- Number of DC outages (can be determined by going into backup without counting the battery test conditions)

Power supply event data is saved to the Black Box for the following events:
Any events that caused the Main Output to shut down:

- Main Output over voltage fault
- Main Output under voltage fault
- Main Output over current fault
- Main Output short circuit fault
- System fan failure
- Over temperature fault

Any events that caused the DC input to be bad:

- DC Input under voltage fault
- DC Input over voltage fault
- DC Input out of range frequency fault

4.4.1 Fault Log History

The FAULT_LOG_HISTORY is used to read the event data of the unit. The fault log history data stores up to 4 event data sets. If the event data sets exceed 4, the oldest data set shall be removed to give way for the latest data set. Unused history data sets shall have a value of zero for all registers.

5. Environment

5.1 Temperature

- Operational or cold aisle (inlet) temperature: -5C to +45C
- Non-operational: -40C to +85C

5.2 Humidity

- Operational **:** 10-90% RH non-condensing
- Non-operational **:** 5-93% RH non-condensing

5.3 Altitude

- Operationa**l :** 0-3050m

- Non-operational **:** 0-12000m

5.4 Acoustic Noise

- Target sound pressure should not exceed 85dBA when system fan modules are running at full speed and operating within the defined environmental envelope

5.5 Vibration and Shock (non-packaged)

The PSU shall meet vibration and shock tests per EN 60068-2-6 and 60068-2-27, respectively, for both non-operating and operating conditions, with the specifications listed below. The test should be performed inside the power shelf with all 6 PSUs and PMI installed. During operating vibration and shock tests, the PSU shall exhibit full compliance to the specification without any electrical discontinuities.

During the non-operating tests, no damages of any kind (including physical damages) should occur and they should not corrupt the functionalities of the PSU per the specifications.

Shock and Vibration tests are to be performed on soft tooled and hard tooled parts.

5.6 Package Vibration, Drop and Compression

PSU units in their package shall meet the following requirements:

Table 8: *Package Vibration, Drop and Compression Requirements*

Package Vibration	1.146 G_{rms}, 2-200-2 Hz, all three axes, Random Vibe	ISTA 3E 06-06
Package Drop	8-inch drop	ISTA 3E 06-06
Package Compression	Maximum compression loading on a bulk pack	ASTM D 642-94

6. Thermal

6.1 Operational

6.1.1 Airflow direction

Front-to-back

6.1.2 DeltaT

This is the air-side temperature difference across the PSU module and represents airflow usage (CFM) in relation to heat loss in the device (W). Efficient use of airflow is critical to meeting facility-level requirements, and the following temperature difference targets are outlined.

- Air inlet and outlet temperature difference ≥ 22°F (or 12.2°C) across 30~85% load range and up to 35°C inlet/ambient and 3050m (10,000ft) above sea-level.

- Excessive air-side deltaT is also not preferred. It is strongly recommended to maintain the air inlet and outlet temperature difference ≤ 25°C at 35°C ambient and up to 6,000ft of altitude.

6.1.3 Thermal Margin

While efficient use of airflow is important for thermal design, reserving adequate margins on components is equally critical. These margins should be defined with respect to de-rated values, following the appropriate standards. Requirements are as follows:

- Component thermal margin of ≥7% or ≥5°C under worst-case conditions (100% load, input voltage lowest, output voltage lowest, with GPU pulse load) and **up to** 30°C inlet/ambient and 3050m (10,000ft) above sea-level. Target whichever margin value is larger.
- Component thermal margin of ≥4% or ≥3°C under worst-case conditions (100% load, input voltage lowest, output voltage lowest, with GPU pulse load), at **greater than** 30°C inlet/ambient and up to 3050m (10,000ft) above sea-level. Target whichever margin value is larger.
- Margin to de-rated temperatures should account for associated differences in reading and measurement location (more on this below). Impact to component and module reliability should also be considered when determining required margin.

6.2 Thermal design requirements

6.2.1 Sensor accuracy

For discrete and critical sensors (such as ambient temperature), an accuracy of ±2°C is required (≤±1°C is preferred). Exhaust and inlet temperature sensors are required and calibrated in the unit. If a component does not have an integrated temperature sensor, and uses a proxy, it needs to target an accuracy ≤±5°C (≤±2°C is preferred). If this component is temperature sensitive, thermal margin requirements defined above should account for sensor inaccuracy.

6.2.2 System fan(s)

Should be sized to support operation across environmental and loading envelopes, with an adequate operating range (speed) to achieve requirements outlined in this document. The fan(s) should also have adequate overhead to accommodate back-pressure resulting from shelf design, rack-level accessories and data center operation. As a starting point, head room to overcome a back-pressure of ≥ 0.3 inches of water is highly recommended; the must-have requirement will be driven by the shelf. The PSU fans must sustain long-term operation without performance degradation while accounting for shelf-level back-pressure. When the PSU module is plugged in, the fan(s) should stay operational irrespective of load and maintain front-to-back airflow direction (overcome potential back-pressure). Mounting of the fan(s) must meet any vibration and acoustic criteria and should not violate any physical constraints outlined. The fan(s) should be included within the power supply enclosure.

6.2.3 Surface temperature

To make the PSU module assembly safe for handling in-operation, accessible surfaces should not exceed a temperature of 75°C with full load and nominal conditions (nominal Vdc, 35°C and 6000 ft).

6.3 System Fan Failure

If a system fan fails, the power supplier must indicate the failure with a signal that will be reported via software as well as an LED indicator on the front panel. The power supplier shall not need to shut down because of a failed system fan and only shut down if there is a fault, i.e., over-temperature fault.

6.4 PSU Module Thermal Monitoring

Each power supplier shall provide the following parameters via the defined communication protocol (in addition to monitoring of power supplier components and operating parameters). The following thermal parameters must be available for each power supplier and labeled accordingly:

- Inlet temperature
- Exhaust temperature
- System fan RPM (average, if >1 system fan used in the power suppliers); percent is acceptable as long as full speed rpm is provided at some point
- System fan fail signals

6.5 Shelf output busbar clip temperature monitoring and protection (if selected)

- There are two thermistors attached to the busbar clip. One thermistor is in contact with the positive (+) metal contact, and the other thermistor is in contact with the negative (-) metal contact. The thermistor should meet the sensor accuracy specification for all operating conditions.
- The PSU shall report the temperatures through Modbus registers.
- The PSU shall set an alarm bit within a Modbus register if the temperature exceeds the warning threshold. This alarm bit serves as an indication that the temperature has reached a level that requires attention. Additionally, if the temperature exceeds the safety threshold, the PSU will initiate a shutdown process to ensure the safety of the system.

7. Mechanical

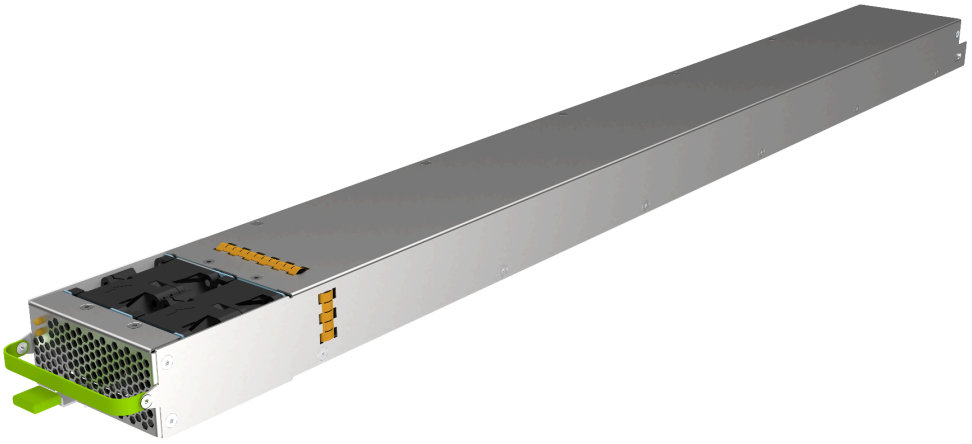


Figure 8: *PSU Assembly Overview*

7.1 PSU Physical Dimensions

The PSU power supplier size is 83.4mm x 40mm x 680mm [Width x Height x Depth]

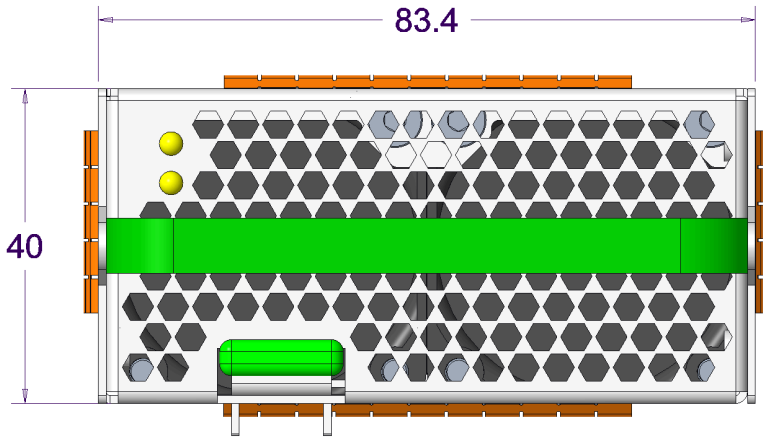


Figure 9: *PSU Physical Dimensions (Front View)*

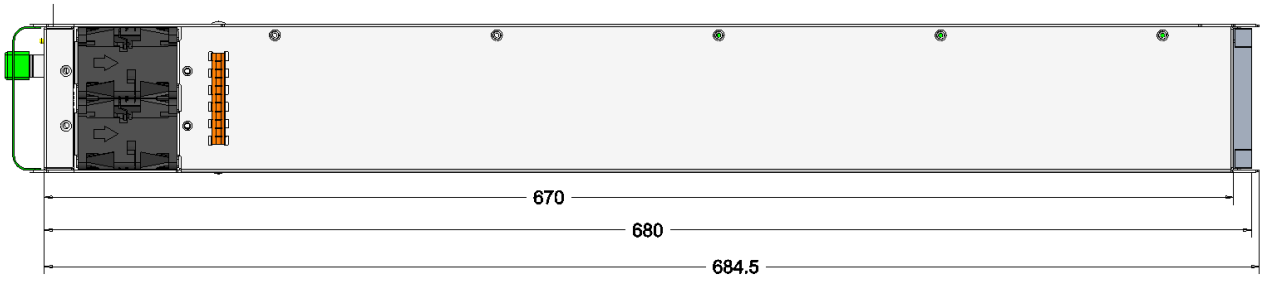


Figure 10: *PSU Physical Dimensions (Side View)*

7.2 Construction

The PSU base and cover shall be assembled using flathead screws. No rivets are allowed as the PSU must have the ability to be opened using a screwdriver. The individual base and cover can be welded, riveted or screwed together, consistent with meeting shock and vibration requirements. There shall be no corners or edges with a radius less than 0.5 mm; all edges shall be deburred and free of burrs.

The sheet metal material shall be steel, pre-plated hot-dip zinc coated, with 0.8-1.2mm of thickness.

7.3 Materials and Fasteners

The sheet metal material shall be steel, pre-plated hot-dip zinc coated, with 0.8mm - 1.2mm of thickness unless otherwise specified. Any plastic material used should meet UL 94-V0 specifications. The system shall contain a minimum of 40% post-consumer-recycled (PCR) plastic content and 15% recycled steel content. However, functionality and reliability are paramount. 65% recycled PC/ABS and 20% recycled SGCC shall be qualified and used in applicable parts to meet the overall recycled content requirement. The following PCR plastics have been qualified for use:

- GLite MBS-200BKR01
- GLite MBS-200GNR01
- Kingfa JH960-6950 C2B-S0759
- Kingfa JH960-6950 C7G-S0023
- Wistron WAM NCT50T#

7.4 Latch & Handle Requirements



Figure 11: *Latch and Handle Assembly*

A latch and handle are required for PSU removal. The latch shall be attached in the location shown on the mechanical drawing, to interface with the cutout in the chassis. The latch design may vary, but the finger interface of the latch must be Pantone 375C (Green).

A foldable handle is highly suggested. The handle shall be designed so that it does not protrude past the top and bottom surfaces when folded 90°. Handle touch points to be Pantone 375C (Green). Please note that the PSU will be heavy, and the handle should be sturdy enough to carry the entire weight of the PSU.

7.5 EMI Gaskets

EMI gaskets are to be placed on the left & right and/or top & bottom sides of the PSU. The main purpose of the gaskets is for PSU module to shelf grounding and secondary purpose is for EMI containment. Gaskets are to be placed towards the front of the PSU module so they make full contact with the walls of the PSU shelf.

Suggested placement distance from front panel along length of PSU module:
Right/Left Side: ~100mm
Top/Bottom Sides: ~100mm.

7.6 Chassis Interface

The handle of the power supply may not protrude from the front surface of the power supply by more than 23mm. The latch shall be located on the left side of the power supply and interface with a rectangular hole in the chassis wall. Please refer to the 3D drawing for latch location on the power supply. The latches should only lock into place when good electrical contact is made on the rear blind mate connectors. This scheme will allow a quick installation of the Power Supply in the tray, and without the need of using a screwdriver.

7.7 Rear Blind Mate Connector

The rear blind mate connector of the PSU shall be Amphenol 10169891-843202SLF or equivalent. This is a R/A plug connector with 8 high power pins, 24 signal pins, and 5 low power pins. Please refer to the drawing for more details.

The connector position within the PSU is fixed in X, Y, and Z direction according to the 3D drawing. This cannot be altered due to mix-and-match requirements for the power supplies into the shelf.

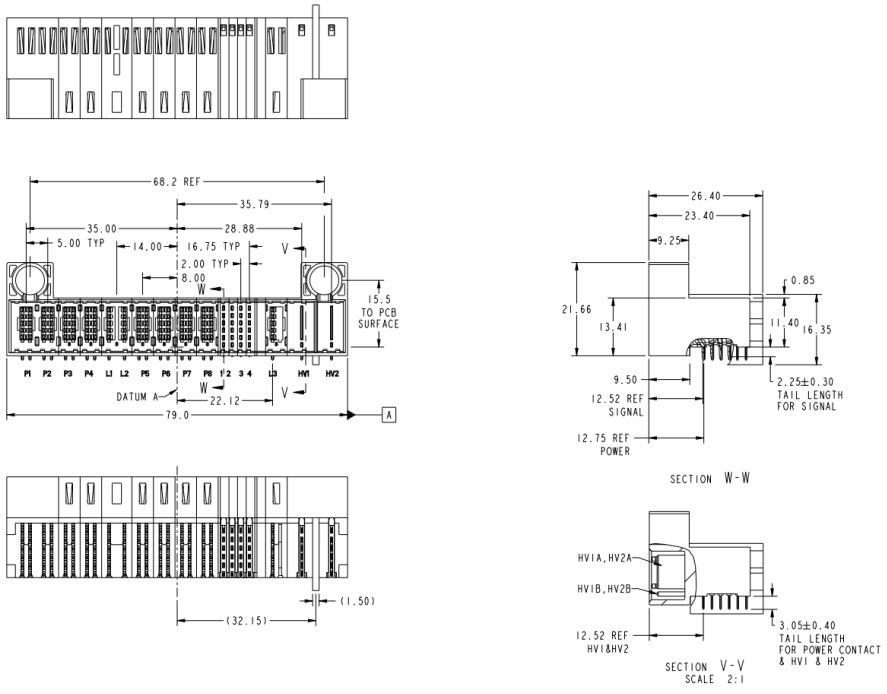


Figure 12: *PSU Connector*

7.8 Rear Blind Mate Connector Protection

A method of protecting the rear blind made connector on the PSU is required to prevent damage from accidental mishandling during manufacturing or end user handling of the module. Please review mechanical 3D CAD for reference design of protection tabs. These tabs should not interfere with any features on the PSU Shelf.

These tabs also double as a keying mechanism to prevent the PSU from being installed upside down.



Figure 13: *Rear Blind Mate Connector Protection*

7.9 Mechanical Drawings

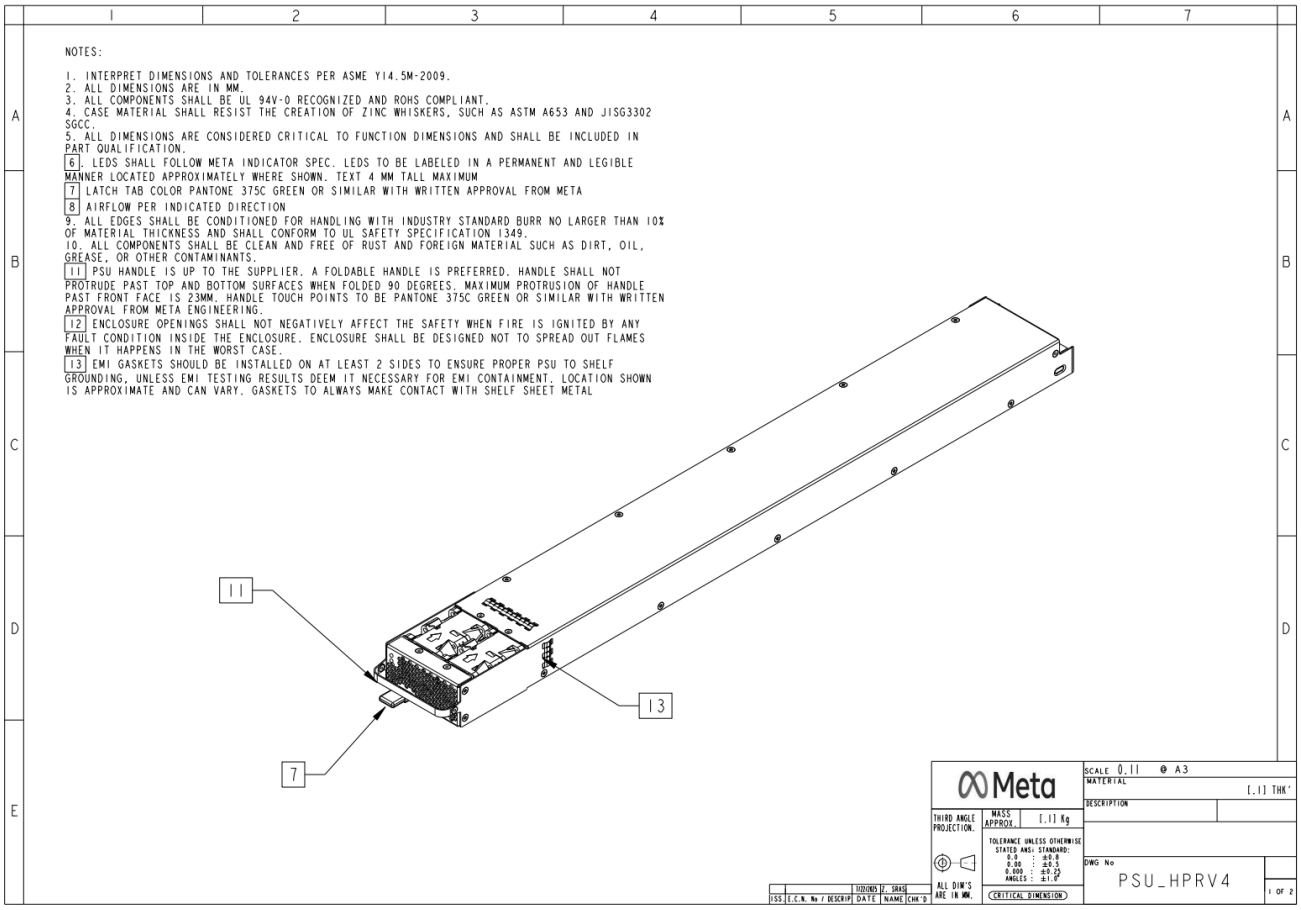
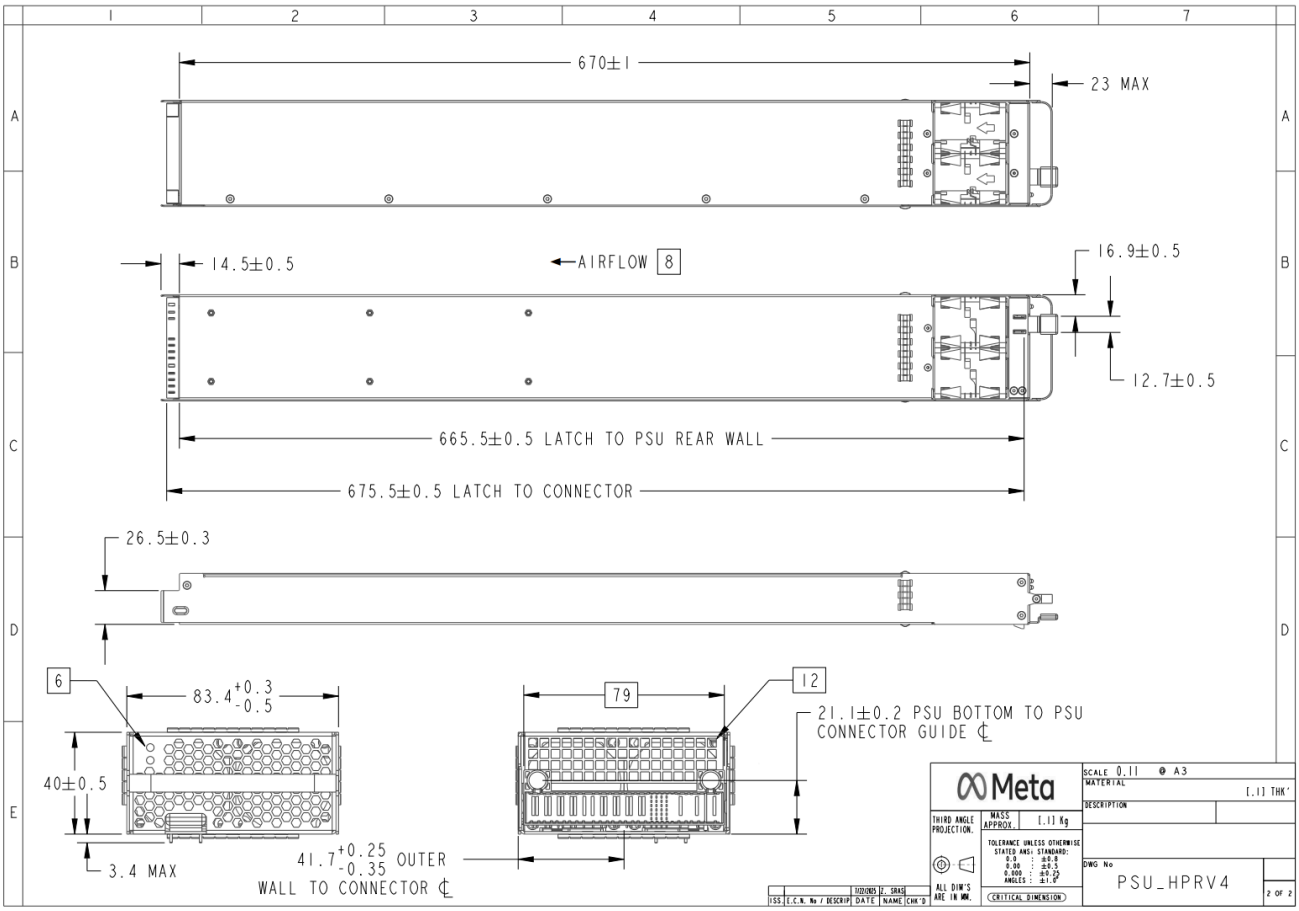


Figure 14: *Mechanical Drawing*



8. Reliability and Quality

8.1 Component Derating Analysis (WCSA)

- Component stress analyses must include Thermal and Electrical stress analyses, and the analyses must consider the worst case operating Thermal and Electrical conditions (defined in Section 5 Environment Requirements and Section 3 Electrical Requirements of this document respectively) applied to all applicable components in the Power Shelf; Capacitor life must be included in the overall analysis as well when applicable.
- IPC-9592B may serve as a reference document for defining the derating specifications of various components, and all components must meet or exceed the specifications defined in IPC-9592B (Class II) as a minimum requirement.
- All Capacitors must meet/exceed > 6 years operation life requirement.
- This activity must be completed at each phase of development (both Primary and Mixed Source, if applicable).

8.2 MTBF Requirements

- Vendor shall provide Calculated MTBF using Telcordia SR-332 latest version (Method 1 Case 1/Parts Count in EVT and Method 1 Case 3/Parts stress in DVT). Target MTBF is 500K hours and calculation should be at 45°C of ambient temperature, 400Vdc of input voltage, and 100% load. The system fan is not included (MTBF of the system fan will be provided separately).
- The PSU shall meet a demonstrated MTBF of minimum 500K hours at 90% confidence level prior to first customer shipment (Pilots samples, Mass Production units). DMTBF is to be performed with PSUs installed in the shelf using PSUs and power shelves from mix-source build.
- MTBF goal: the Vendor shall provide the best MTBF numbers that the PSU will be able to meet, no matter the minimum requested. Designers will use this information for an overall reliability study of the whole system.
- The system fan L10 life shall be at least 6 years at 45°C inlet air temp and full speed (to be verified with the system fan vendor)

8.3 Design Failure Mode and Effect Analysis (DFMEA)

- The risk assessment must be performed with a focus on the long term exposure to environmental, electrical, mechanical stresses, and based on the Power Shelf design as well as worst case operational requirements that are outlined in this document.
- The assessment must start as soon as a design of any of the critical elements within a Power Shelf is available for assessment.
- The risk assessment must include failure modes, impact to the functional/appearance of the Power Shelf, and failure occurrence that must be based on historical data or simulation results.
- Risk levels that are classified as High and Medium risks must have mitigation plans in place before Design Freeze of the next stage of development.

8.4 High Accelerated Life Test (HALT)

- A comprehensive HALT shall be performed on the Power Shelf + PMM. The HALT equipment, testing procedure, sample size, testing report and documentation, and root cause analysis and corrective action requirements shall follow the requirements specified in IPC-9592B, Section 5.2.3.

- HALT test is to be performed on PSU samples from mix-source build.

8.5 NPI Reliability Tests

- The Power Shelf must pass a set of reliability tests that comprises environmental stress (defined in Section 5 Environment Requirements of this document), electrical stress (defined in Section 3 Electrical Requirements of this document), and mechanical stress (defined in Section 5 Environment Requirements of this document) conditions. IPC9592BL may serve as a baseline reference for the reliability test plan development, but the exact test item and the respective test conditions should be defined based on the product specifications and DFMEA results.
- Reliability tests must be performed at each phase of the NPI development starting from EVT, and continue in DVT and PVT.

- Test durations for some of the test items must meet or exceed > 6 years of Power Shelf operation life. The acceleration factors that are based on thermal, electrical, etc may be employed to reduce the test duration for the purpose of demonstrating the robustness of the design under the most extreme operational requirements as defined in this document.
- Sample types include Power Shelf + PMM

8.6 Disallowed Components

The design team reserves the right to select some preferred/mandatory parts, during the development phase (selection of an approved vendor list (AVL) subset). The Vendor will help solve system integration problems, should any issues arise.

- Trimmers and/or potentiometers.
- Tantalum capacitors.
- Dip switches.
- High side driver ICs
- Paralleled power MOS are allowed provided that the design prevents parasitic oscillations
- SMT ceramic capacitors are allowed with the case size < 1206. The size 1206 can still be used when SMT capacitors are placed far from the PCBs edge, and with a correct orientation that minimizes risks of cracks [any size > 1206 must be highlighted during DFM review].
- Allowed ceramics materials for SMT capacitors are: X7R or better material. The COG or NPO types should be used in critical portions of the design, such as feedback loop, PWM clock settings, etc. [any changes shall be highlighted and brought up during DFM review].
- Relays: the use of any electro-mechanical relays, and type shall be discussed up front before any approval is given to include them in the design.
- Resistors to be used from approved vendor list.
- The company design team will approve all control ICs.

8.6.1 Capacitors

- The bulk electrolytic capacitors shall be rated at 105°C, no less than 450V and shall be selected from Japanese and US manufactures only.
- All capacitors shall have a predicted life of at least 6 years at 45°C inlet air temperature under worst conditions, including the GPU pulse load conditions.

8.6.2 Sheet Metal Material and Zinc Whisker Implications

- Sheet Metal Chassis Material is hot-dip Zinc coated, JIS G3302
- SGCC (Z18 to Z22), with 0.8mm - 1mm of thickness. The ‘Z’ parameter defines the metal coating thickness: Z20 is for 40µm of thickness, and Z22 is for 43µm.
- The Japanese standard is ‘JIS G3302’, while the US standard is ‘ASTM A653’.
- Mechanical design shall prevent sharp edges and possible metal oxidation in the critical points of the sheet metal (e.g. in the cut & bends portions, etc.).

- Both chassis design and metal base material will not promote the growth and propagation of zinc and tin whiskers.
- Metal base materials with electro-zinc plating, or poor conductivity plating, are not allowed.
- Alloy materials are a possible option, while stainless steel is another possibility provided that it makes cost sense (both options are subject to approval)
- Aluminum material is not allowed for the enclosures.
- The chassis enclosure, as well as the whole electronics, shall meet certain contamination requirements (see EIA 364-65 IIA).

8.6.3 Mix-source Builds

Suppliers are required to conduct a mix-source build ideally at DVT using prime and 2nd source/alternate parts in the BOM. These samples are to be used in all Reliability and Environmental tests as agreed and approved by the design team.

9. Manufacturing Quality Control and Testing

The Vendor's manufacturing plan shall be designed to meet the quality process requirements as specified in IPC-9592B, Section 6 ("Quality Process"), which includes PFMEA, statistical process control (SPC), corrective action process, yield control, materials traceability, product change notice (PCN), qualification of change, etc.

The PVT samples shall be manufactured in the mass production line. Samples shall be shipped using the approved for production shipping boxes, are certified and with safety labels applied ("Pending Certification" sticker may be allowed until the certification process is complete).

During PVT and before production release, the following shall be submitted for review.

a. Manufacturing Quality Plan
b. Manufacturing Test Plan
c. PVT Build Report with yield of >98% and issues analyzed with validated corrective actions in place
d. First Article Inspection (FAI) CPK report for electrical parameters and mechanical dimensions - >1.33 on at least 32 samples
e. Design for Test, Design for Manufacturability and PFMEA reports
f. System Component Traceability
g. Full specification compliance matrix with corresponding test reports
h. RMA process including flowchart and turnaround time

9.1 Manufacturing Testing

9.1.1 Incoming Quality Inspection

All assembly inspection dimensions and tolerances in the drawings provided must be met. Inspection shall include critical components and mechanical dimensions as defined.

9.1.2 In-Circuit and Parametric Test

For all the boards used in the PSU design: the in-circuit test coverage and test point access shall be > 95% or higher. The rest shall be covered by functional testing.

Functional parametric testing shall be done on an automated tester before and after burn-in to check drifting. The tester shall be subjected to Gage Repeatability and Reproducibility (GR&R) and bench correlation testing before release to production.

9.1.3 Burn-In (BI) and Ongoing Reliability Testing (ORT)

Burn-in test duration starts at a minimum of 24 hours. Unit-hours, acceptable failure rate, production yield requirements are defined and agreed upon before products are released to production.

No reduction is allowed during NPI. An approved PCN with the supporting documents (including but not limited to BI test history, closed RCCA) is required before implementation. Any manufacturing location change will reset test time and unit count to 24 hours.

With agreement, test time may be increased if needed and as applicable depending on the failure mechanism.

Unless otherwise agreed upon, the required test conditions are as follow:
Input Voltage: Nominal input voltage with cycling
Output Loading: 95 +/-5% of maximum rating with cycling
Current sharing: Yes
Ambient Temperature: 50deg C +/-5deg C (or maximum operating temperature)
Monitoring: Automated monitoring of input and output voltage and FW status reporting

Ongoing Reliability Testing (ORT) shall be performed when the minimum burn-in time is reached. Sampling size will be agreed between the customer and the supplier.

9.1.4 Hipot and Ground Continuity Test

The PSU shall be tested 100% in production for both Hi-Pot (with the applicable limits for the AC leakage current) and ground continuity (per the applicable standard). Stamps shall be applied accordingly to the chassis.

9.1.5 Ongoing Quality Assurance

Sampling testing shall be conducted on each batch of finished goods. It will include, but not limited to parametric testing, burn-in, hipot and final visual inspection.

9.2 Automation and Continuous Improvement

Certain areas of production shall be planned for automation before and after the product is released to production. At a minimum, it shall include SMT and wave soldering, conformal coating, burn-in and others. Continuous improvement plans shall be submitted on a regular basis to ensure uniformity of process and quality control.

9.2.1 Conformal Coating

The gate terminals of all high-voltage MOSFETs as well as the most sensitive areas of the electronic circuitry in the boards must be protected against potential resistive contacts with other voltage potentials (e.g. MOS Drain leads, etc.) due to whiskers, pollutant particles, dust, moisture (for example contaminant substances can become conductive in presence of moisture), and up to some local wet condensation occurrences.

Local automated, conformal coating shall be applied to critical areas of the boards to protect sensitive circuitries, using an atomized spray process (no dipping process is considered here). The thickness of the coating shall be ~50µm to ~150µm. The Vendor (mainly the ultimate Manufacturing Facility) shall demonstrate to possess good skills, experience, and long years of experience on automated conformal coating application and process. The power modules main board shall be partially conformal coated (top & bottom); critical board areas shall be agreed upon, typically the DC high- voltage input section at shelf level, like the DC input, board-mount connector area.

9.3 Quality Control Process

The vendor shall submit a production yield report and RMA summary on a biweekly basis. This shall include yield per station, Pareto of failures and assignable causes, root cause analysis with related risk assessment, corrective and/or screening actions as applicable. The RMA report shall include both overall and year to date historical data with identification of RMAs from the integrators and the field. It is the vendor's responsibility to inform the customer when failure excursions occur in the manufacturing, integrator and/or the field upon discovery.

9.4 Warranty and Failure Analysis

- The Vendor is responsible for the PSU to meet the specifications as stand-alone unit as well as at system level, and for assuring that the power supplies shipped in production will conform to the specifications with no deviations.
- Standard failure analysis turnaround time on RMA units shall be 7 days upon receipt at the Vendor's facility. For urgent units, FA (Failure Analysis) may be requested to be provided within 24hrs upon receipt or as agreed upon. An 8D report may be required on trending issues and/or those causing thermal events.
- The Vendor shall warrant the power supply for defects and workmanship for a period of three (3) years from the date of shipment when the device is operated within specifications. The warranty is fully transferable to any end user. A standard "VOID" warranty sticker may be applied.
- Failure analysis support may be requested and further actions as needed, even if the power supplies are outside the warranty period. These are on special cases including, but not limited to a thermal or safety event and early wearout.

9.5 Product Change Notification

A PCN shall be submitted for any change that affects form, fit, function, compliance, revision, version, process, material (including deletion), testing (i.e., BI reduction) and other modifications.

If uncertain, please contact the customer. The PCN shall be issued with an assigned unique number for traceability and formally submitted via email. The supplier shall give a minimum of one month's notice before target implementation of the proposed changes unless urgent (i.e., resolve design, quality, process or supply issue, customer request). PCN approval is required before implementation of any changes.

The PCN document shall include the following:
a. Vendor PN and revision/version (from and to, retain if not changed)
b. Vendor PN HW and FW (if applicable) (from and to, retain if not changed)
c. Date of Issuance
d. Reason of change
e. Description of changes
f. Form, fit, function changes (if any)
g. Before and after drawing with mark-up of changes if applicable
h. Traceability (i.e., cut-in SN, date code)

In addition, a PCN shall be issued upon initial release to production and includes (or the links to) the required documents. It shall include the formal and controlled releases of specifications, drawings, manufacturing plans and others.

10. Compliance requirements

The power supply unit shall be designed for compliance to allow worldwide deployment. Additionally, the manufacturer is fully responsible for:

- ensuring the complete compliance of the power supply shelf in the environment it is intended to function (as described by the Rack Specification)
- maintaining and updating the power supply shelf safety reports to current requirements and all new released requirements.
- all design and recertification costs required to update the power supply to meet the new
- requirements.
- Meeting EMC requirements
- Meeting Safety requirements

The manufacturer is responsible for obtaining the safety certifications specified below.

10.1 Safety Standards

The product is to be designed to comply with the latest edition, revision, and amendment of the following standards (UL 62368-1, IEC 62368-1 and EN 62368-1; hazard-based performance standard for Audio video, IT & Communication Technology Equipment)

The manufacturer shall obtain the following safety certifications for the power shelf as applicable. Only requirements that absolutely rely on or are affected by the system may be left to the system level evaluation [i.e., no Conditions of Acceptability]. Below are common requirements for North America and Europe. For other countries, different certifications may be required:

- UL or an equivalent NRTL for the US with follow-up service (e.g. UL or CSA).
- CB Certificate and test report issued by CSA or UL
- CE Marking for EU

10.1.1 Safety requirements

Following (but not limited) safety requirements are applicable:

- All Fans shall be certified by safety agencies
- All current limiting devices shall be certified and be rated for the application where the device in its application complies with IEC/UL 62368-1.
- All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printed wiring board manufacturer.
- All connectors shall be UL recognized and have a UL flame rating of UL94V-0.
- All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer. SELV Cable to be rated minimum 80V, 125C.
- Product safety labels must be printed on UL approved label stock and printer ribbon. Alternatively, labels can be purchased from a UL approved label manufacturer.
- The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.
- Any single fault condition applied on the safety critical component shall not cause any electrical or mechanical unsafe conditions (such as electric shock to the user, arcing to ignite fire...)
- The power shelf shall meet the acoustic noise requirement specified by the design team.
- PCBA and connectors shall meet the clearance and creepage requirements specified in the relevant safety standard such as IEC/UL62368-1.

10.2 EMC Requirements

The power supply shall meet the following requirements in the latest edition of standards when operating under typical load conditions and with all ports fully loaded;

The Power supply integrated into the shelf is called the component power supply. The manufacturer shall provide the proof of compliance for the component power supply that is required for spare parts shipment. The component power supply shall not contribute any noncompliant conditions to the end-use product.
If at any time it is found that a supplier's component power supply causes the end-use product to fail emissions and/or immunity testing, the supplier will be instructed to investigate and resolve the problem.
The power shelf shall have a minimum 6dB margin from the Class A limit for the radiated and conducted emissions. Depending on the system manufacturer's design goals and business needs, more margin may be required when it is integrated into the final end system.
The following EMC Standards (the latest version) are applicable to the product.

- FCC /ICES-003
- CISPR 32/EN55032
- CISPR 35/EN55035 - Immunity

Each individual basic standard for immunity test has the following minimum passing requirement. Testing can be waived for the PSU if it is tested in the fully populated shelf. Higher level of passing criteria may be applied depending on the system manufacturer's design goals and business needs.

- EN61000-4-2 Electrostatic Discharge Immunity
  - Contact discharge: >5.6kV
  - Air discharge: >11.2kV
- EN61000-4-3 Radiated Immunity
  - > 3V/m
- EN61000-4-4 Electrical Fast Transient Immunity

    - Signal Line (such as PMM) and DC power lines >1.0kV
- EN61000-4-5 Surge
    - DC power lines: >0.5kV
- EN61000-4-6 Immunity to Conducted Disturbances
    - DC Power Line: > 3Vrms
- EN61000-4-8 Power Frequency Magnetic Field Immunity, when applicable
    - > 1A/m

10.3 Environmental Compliance

The power shelf (including all components inside) shall comply with the following minimum environmental requirement and manufacturer shall provide full material disclosure, Declaration of Conformity and technical documentations to demonstrate compliance. The system manufacturer may have additional requirements depending on its design goals and business needs.

- RoHS Directive (2011/65/EU and 2015/863/EU); aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture
- REACH Regulation (EC) No 1907/2006 including the restriction of PFAS substances; registration with the European Chemicals Agency (ECHA), evaluation, authorization and restriction of chemicals.
- Halogen Free: IEC 61249-2-21, Definition of Halogen Free, 900ppm for Br or Cl, or 1500ppm combined
- US SEC conflict mineral regulation to source mineral materials from socially responsible countries, if applicable
- Waste Electrical and Electronic Equipment ("**WEEE**") Directive (2012/19/EU) if applicable; aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture
- The vendor shall provide the declaration of compliance document stating that a product does not contain any substances regulated by EPA 40 CFR751.

10.4 Documentation

The manufacturer shall provide reproducible copies of all pertinent documentation relating to the following:

- Product Information
- Bill of Materials
- Schematics
- functional test report
- Final Compliance Approval
- NRTL certificate and report, Conditions of Acceptability and test report plus User documentation that explains safe installation and operating procedures.
- CB Certificate and report, including schematics
- Manufacturer's Declaration of Conformity to EN 62368-1, EN55032, EN55035 and ROHS
- FCC Part 15 Class A and CISPR32 Class A test data
- Other applicable certificates required by the system manufacturer.

Appendix A – Communication Specification

	fault triggers						
	Main Output over voltage fault			File Record			
	Main Output under voltage fault			Latest Power Supply Event Data			
	Main Output over current fault			2nd to the Latest Power Supply Event Data			
	DC Input under voltage fault			3rd to the Latest Power Supply Event Data			
	DC Input over voltage fault			4th to the Latest Power Supply Event Data			
	Over temperature fault						
		# of Bytes	296	the Max 245 Bytes in one Read File			
Hex Address	Record Number (Suggested Mapping) in Word		Number of Word	Data to store	Encoding		
	0	39	40	DC Input Voltage - rectified (40 samples @ 1ms)	unsign N=6		
	40	79	40	DC Input Current - rectified (40 samples @ 1ms)	unsign N=10		
	80	119	40	Main Output Voltage (40 samples @ 1ms)	unsign N=10	1st Request	240
	120	159	40	Main Output Current (40 samples @ 1ms)	unsign N=6		
	160	164	5	Temp0 – Inlet (5 samples @ 5 sec)	2's comp+sign N=7		
	165	169	5	Temp1 – Outlet (5 samples @ 5 sec)	2's comp+sign N=7		
	170	174	5	RPM Fan 0 (5 samples @ 5 sec)	unsign		AE
AF	175	176	2	Total_Up_Time	unsign		AF
B1	177	178	2	Time_Since_Last_On	unsign		B1
B3	179	179	1	DC_Power_Cycle_Counter	unsign		B3
B4	180	180	1	DC_Outage_Counter	unsign		B4
B5	181	182	2	Reserved_003A	0		B5
B7	183	183	1	General_Alarm_Status_Register	Bit mapped per failure		B7
B8	184	184	1	~~PFC_Alarm_Status_Register~~	Bit mapped per failure		B8
B9	185	185	1	DCDC_Alarm_Status_Register	Bit mapped per failure		B9
BA	186	186	1	Temperature_Alarm_Status_Register	Bit mapped per failure		BA
BB	187	187	1	Communication_Alarm_Status_Register	Bit mapped per failure		BB
BC	188	188	1	PSU_Input_Power_Inst	unsign N=3		BC
BD	189	189	1	PSU_Input_Current_DC_Inst	unsign N=10		BD
BE	190	190	1	PSU_RPM_Fan0	unsign		BE
BF	191	191	1	PSU_RPM_Fan1	unsign		BF
C0	192	192	1	PSU_Temp0_Inlet	2's comp+sign N=7		C0
C1	193	193	1	PSU_Temp1_Outlet	2's comp+sign N=7		C1
C2	194	194	1	PSU_Max_Temp	2's comp+sign N=7		C2
C3	195	195	1	PSU_Min_Temp	2's comp+sign N=7		C3
C4	196	197	2	PSU_Position_Number	unsign 32 bit		C4
C6	198	199	2	CRC_Error_Counter	unsign 32 bit		C6
C8	200	201	2	Timeout_Error_Counter	unsign 32 bit		C8
CA	202	202	1	PSU_Output_Voltage	unsign N=10		CA
CB	203	203	1	PSU_Output_Current	unsign N=6		CB
CC	204	204	1	I_Share_Current_Value	unsign N=6		CC
CD	205	205	1	PSU_Output_Power	unsign N=3		CD
CE	206	206	1	PSU_Bulk_Cap_Voltage	unsign N=6		CE
CF	207	207	1	PSU_Input_Frequency_AC	unsign N=0		CF
D0	208	208	1	PSU_ITHD	unsign N=9		D0
D1	209	209	1	~~PSU_Power_Factor~~	unsign N=9		D1
D2	210	210	1	PSU_Input_Power	unsign N=3		D2
D3	211	211	1	PSU_Input_Voltage_DC	unsign N=6		D3
D4	212	212	1	PSU_Input_Current_DC	unsign N=10		D4
D5	213	214	2	Unix_Time	unsign		D5
D7	215	216	2	Power_Cycle_Unix_Time	unsign		D7
D9	217	217	1	PSU_Setting_Register	Bit mapped		D9
DA	218	218	1	Communication_Baud_Rate	unsign		DA
DB	219	219	1	Fan_Duty_Cycle_Override	unsign		DB
DC	220	220	1	LED_Override	Bitmapped		DC
DD	221	221	1	PSU_Fault_Counter	unsign 16 bit		DD
DE	222	222	1	Turn_Off_Time_Of_Power_Cycle_Unix_Time	unsign 16 bit		DE
DF	223	223	1	Reserved_0064	0		DF
E0	224	224	1	Vin_Min	unsign N=6		E0
E1	225	225	1	Vin_Max	unsign N=6		E1
E2	226	226	1	Vout_Setpoint	unsign N=10		E2
E3	227	227	1	Bus_Clip_OTP_Set	unsign N=6		E3
E4	228	231	4	PSU_FBL_FW_Revision	ASCII		E4
E8	232	233	2	Power_Off_Unix_Time	unisgn		E8
EA	234	234	1	Bus_Clip_Temp_Pos	2's comp+sign N=7		EA
EB	235	235	1	Bus_Clip_Temp_Neg	2's comp+sign N=7		EB
EC	236	236	1	Bus_Voltage_Max_Since_Power_On	unsign N=10		EC
ED	237	237	1	Bus_Voltage_Min_Since_Power_On	unsign N=10		ED
EE	238	238	1	Bus_Voltage_Max_Over_Period	unsign N=10		EE
EF	239	239	1	Bus_Voltage_Min_Over_Period	unsign N=10	2nd Request	EF
F0	240	240	1	Input_Power_Planned	unsign		F0
F1	241	241	1	PSU_Output_Voltage_ORing	unsign N=10		F1
F2	242	242	1	Region	unsign		F2
F3	243	243	1	Hardware_Singal	Bit mapped		F3
F4	244	244	1	DC_Loss_Count_Requested	unsign		F4
F5	245	245	1	Pulse_Mgmt_Count_Requested	unsign		F5
F6	246	246	1	Size_Module_Reg_Map	unsign		F6
F7	247	247	1	Shelf_Location	unsign		F7
F8	248	248	1	reserved_007D	0		F8
F9	249	249	1	Reserved_007E	0	3rd Request	F9